1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
D		428208	PRODUCTION RELEASED	03/04/06	

SCHEM,MLB,M1

03/03/2006

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7099	1	SCHEM,MLB,M1	SCH	CRITICAL	
820-1881	1	PCBF,MLB,M1	PCB	CRITICAL	

DRAWING
TITLE=M1_MLB
ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 3 15:00:30 2006

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

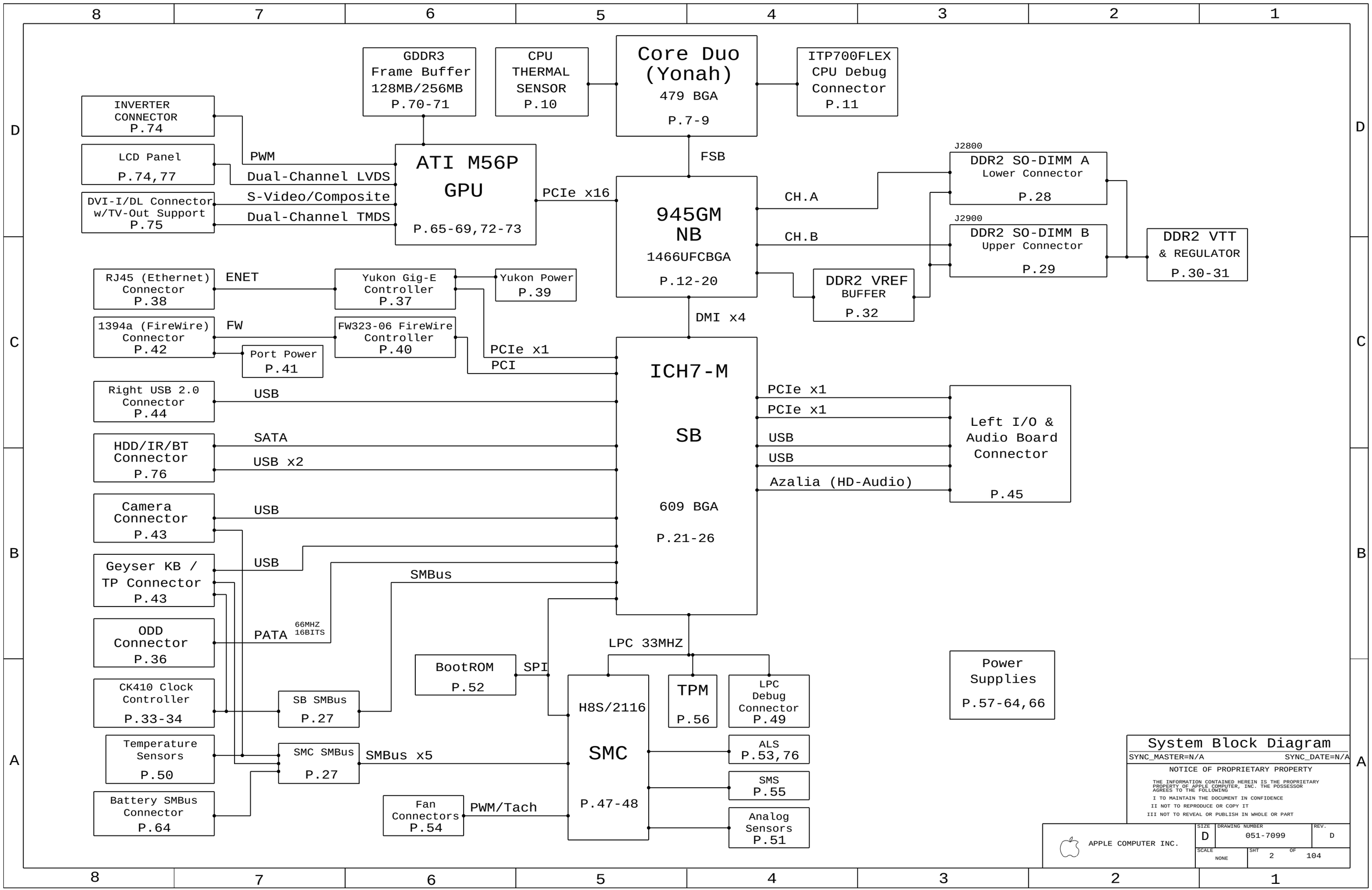
MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MLB,M1

DRAWING NUMBER 051-7099 REV. D

SHT 1 OF 104


GDDR3
Frame Buffer
128MB/256MB
P.70-71
CPU
THERMAL
SENSOR
P.10
Core Duo
(Yonah)
479 BGA
P.7-9
ITP700FLEX
CPU Debug
Connector
P.11
INVERTER
CONNECTOR
P.74
LCD Panel
P.74,77
DVI-I/DL Connector
w/TV-Out Support
P.75
PWM
Dual-Channel LVDS
S-Video/Composite
Dual-Channel TMDS
ATI M56P
GPU
P.65-69,72-73
PCIe x16
FSB
945GM
NB
1466UFCBGA
P.12-20
J2800
DDR2 SO-DIMM A
Lower Connector
P.28
J2900
DDR2 SO-DIMM B
Upper Connector
P.29
CH.A
CH.B
DDR2 VTT
& REGULATOR
P.30-31
DDR2 VREF
BUFFER
P.32
RJ45 (Ethernet)
Connector
P.38
ENET
Yukon Gig-E
Controller
P.37
Yukon Power
P.39
1394a (FireWire)
Connector
P.42
FW
FW323-06 FireWire
Controller
P.40
Port Power
P.41
PCIe x1
PCI
DMI x4
ICH7-M
SB
609 BGA
P.21-26
Right USB 2.0
Connector
P.44
USB
HDD/IR/BT
Connector
P.76
SATA
USB x2
Camera
Connector
P.43
USB
Geyser KB /
TP Connector
P.43
USB
SMBus
ODD
Connector
P.36
PATA
66MHZ
16BITS
PCIe x1
PCIe x1
USB
USB
Azalia (HD-Audio)
Left I/O &
Audio Board
Connector
P.45
LPC 33MHZ
BootROM
P.52
SPI
CK410 Clock
Controller
P.33-34
SB SMBus
P.27
H8S/2116
SMC
P.47-48
TPM
P.56
LPC
Debug
Connector
P.49
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Supplies
P.57-64,66
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Sensors
P.50
SMC SMBus
P.27
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SMS
P.55
Analog
Sensors
P.51
Battery SMBus
Connector
P.64
Fan
Connectors
P.54
PWM/Tach
System Block Diagram
SYNC_MASTER=N/A
SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY
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SCALE
NONE
SHT
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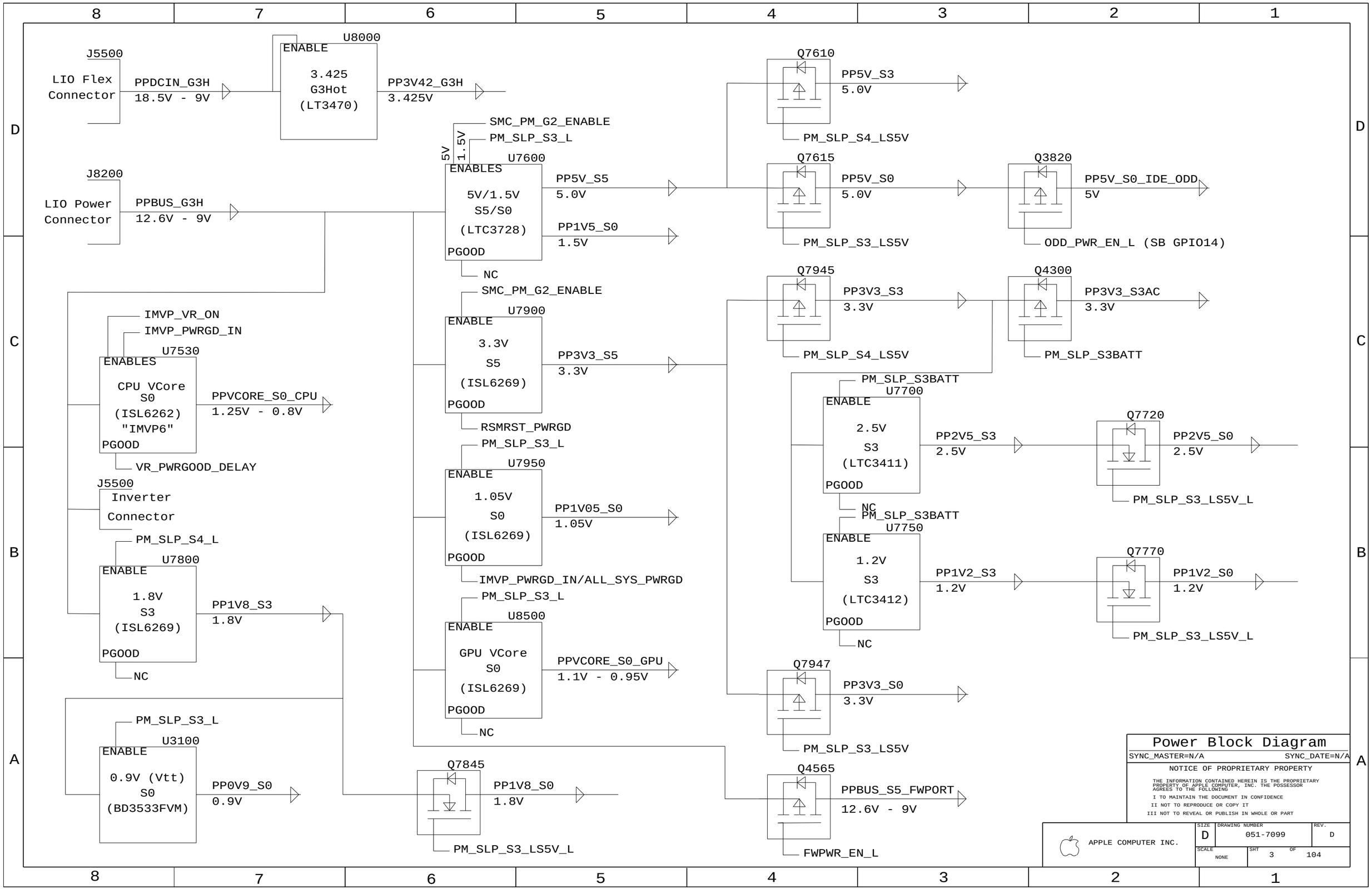
OF
104


J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H
12.6V - 9V
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q7610
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q7615
PP5V_S0
5.0V
PM_SLP_S3_LS5V
Q3820
PP5V_S0_IDE_ODD
5V
ODD_PWR_EN_L (SB GPIO14)
IMVP_VR_ON
IMVP_PWRGD_IN
U7530
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
PPVCORE_S0_CPU
1.25V - 0.8V
VR_PWRGOOD_DELAY
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
PP1V8_S3
1.8V
NC
SMC_PM_G2_ENABLE
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
PP3V3_S5
3.3V
RSMRST_PWRGD
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
PM_SLP_S3_L
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
PPVCORE_S0_GPU
1.1V - 0.95V
NC
Q7945
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
Q4300
PP3V3_S3AC
3.3V
PM_SLP_S3BATT
PM_SLP_S3BATT
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
PP2V5_S3
2.5V
NC
Q7720
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
PM_SLP_S3BATT
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
PP1V2_S3
1.2V
NC
Q7770
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
Q7947
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
PM_SLP_S3_L
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PP0V9_S0
0.9V
Q7845
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN_L
Power Block Diagram
SYNC_MASTER=N/A
SYNC_DATE=N/A
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NONE
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"Better" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7569	PCBA,1.83GHZ,128VRAM_M1_MBPRO_15	EEE_VHT,M1_COMMON,CPU_1_83GHZ,VRAM_SAM128

"Best" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7570	PCBA,2.0GHZ,256VRAM_M1_MBPRO_15	EEE_VHU,M1_COMMON,CPU_2_0GHZ,VRAM_SAM256

"CTO" BOM

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7571	PCBA,2.16GHZ,256VRAM_M1_MBPRO_15	EEE_VHV,M1_COMMON,CPU_2_16GHZ,VRAM_SAM256

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M1_COMMON	ALTERNATE,COMMON,M1_COMMON1,M1_COMMON2,M1_COMMON3
M1_COMMON1	BOOTROM_DEVEL,ENET_LOM_DISABLE,ENETPWR_S3AC,GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS
M1_COMMON2	ITP,INVERTER_BUF,KBDLED_HAS,LPCPLUS,LVDS_PD,MEMVREF_S3,MEMVTT_EN_PU
M1_COMMON3	RTUSB_ESD,SMC_PRGRM,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
VRAM_HY128	GPU_MEM_HYNIX,VRAM_128_HYNIX
VRAM_SAM128	VRAM_128_SAMSUNG
VRAM_HY256	GPU_MEM_256M,GPU_MEM_HYNIX,VRAM_256_HYNIX
VRAM_SAM256	GPU_MEM_256M,VRAM_256_SAMSUNG

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VHT]	CRITICAL	EEE_VHT	M1,1.83GHZ,SAM128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VHU]	CRITICAL	EEE_VHU	M1,2.0GHZ,SAM256
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:VHV]	CRITICAL	EEE_VHV	M1,2.16GHZ,SAM256

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
337S3282	1	IC,YDC,CO,1.83G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_1_83GHZ
337S3267	1	IC,YDC,CO,2.0G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_2_0GHZ
337S3268	1	IC,YDC,CO,2.16G,31W,667M,2M,479BGA	U0700	CRITICAL	CPU_2_16GHZ
341S1873	1	IC,EFI,BOOTROM DEVELOPMENT (NEW),M1	U6301	CRITICAL	BOOTROM_DEVEL
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1875	1	IC,PRGRM,SMC (NEW),M1	U5800	CRITICAL	SMC_PRGRM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0309	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060		ALL	330uF,2V,9MOHM,D2
128S0095	128S0060		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	150uF,6.3V,25MOHM,C2
128S0077	128S0086		ALL	7mOhm alt for 8mOhm

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7099 | REV. D

SCALE NONE | SHT 4 OF 104

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	57
TRUE		IMVP6_COMP	57
TRUE		P5VS5_RUNSS	58 62
TRUE		P1V5S0_RUNSS	58 62
TRUE		P2V5S3_MODE	59
TRUE		P2V5S3_SHDNRT	59
TRUE		P1V2S3_RT	59
TRUE		P1V2S3_RUNSS	39 59
TRUE		P1V8S3_COMP	60
TRUE		P1V8S3_FSET	60
TRUE		P3V3S5_COMP	61
TRUE		P3V3S5_FSET	61
TRUE		P1V05S0_COMP	61
TRUE		P1V05S0_FSET	61
TRUE		P3V42G3H_FB	62
TRUE		GPUVCORE_COMP	66
TRUE		GPUVCORE_FSET	66
TRUE		GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7 12 79
TRUE		FSB_ADS_L	7 12 79
TRUE	TRUE	FSB_ADSTB_L<1..0>	7 12 79
TRUE		FSB_BNR_L	7 12 79
TRUE		FSB_BREQ0_L	7 12 79
TRUE		FSB_D_L<63..0>	7 12 79
TRUE		FSB_DBSY_L	7 12 79
TRUE	TRUE	FSB_DINV_L<3..0>	7 12 79
TRUE		FSB_DRDY_L	7 12 79
TRUE	TRUE	FSB_DSTBN_L<3..0>	7 12 79
TRUE	TRUE	FSB_DSTBP_L<3..0>	7 12 79
TRUE		FSB_HIT_L	7 12 79
TRUE		FSB_HITM_L	7 12 79
TRUE		FSB_LOCK_L	7 12 79
TRUE		FSB_REQ_L<4..0>	7 12 79

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14 22
TRUE	DMI_N2S_N<1..0>	14 22
TRUE	SB_CLK100M_SATA_P	21 34
TRUE	SB_CLK100M_SATA_N	21 34

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST		
	=PP5V_S0_FAN_LT	54 63
	FAN_LT_PWM	54
	FAN_LT_TACH	54
	FAN_RT_PWM	54
	FAN_RT_TACH	54

LPC+ Debug Connector

FUNC_TEST		
TRUE	=PP3V3_S5_LPCPLUS	49 63
TRUE	=PP5V_S0_LPCPLUS	49 63
TRUE	LPC_AD<0>	21 47 49 56
TRUE	LPC_AD<1>	21 47 49 56
TRUE	LPC_FRAME_L	21 47 49 56
TRUE	PM_CLKRUN_L	23 40 47 49 56
TRUE	BOOT_LPC_SPI_L	22 47 49
TRUE	SMC_TMS	47 48 49
TRUE	DEBUG_RST_L	26 49
TRUE	SMC_TRST_L	47 49
TRUE	SMC_TDO	47 48 49
TRUE	SMC_MD1	47 49
TRUE	SMC_TX_L	47 48 49
TRUE	FWH_INIT_L	21 48 49
TRUE	PCI_CLK_PORT80_LPC	34 49
TRUE	LPC_AD<2>	21 47 49 56
TRUE	LPC_AD<3>	21 47 49 56
TRUE	INT_SERIRQ	23 47 49 56
TRUE	PM_SUS_STAT_L	23 47 48 49 56
TRUE	SMC_TDI	47 48 49
TRUE	SMC_TCK	47 48 49
TRUE	SMC_RST_L	47 48 49
TRUE	SMC_NMI	47 49
TRUE	SMC_RX_L	47 48 49
TRUE	SV_SET_UP	23 49

Left ALS Connector

FUNC_TEST		
TRUE	=PP3V3_S3_LTALS	63 76
TRUE	ALS_GAIN	6 47 76
TRUE	LTALS_OUT	53 76
TRUE	GND	

Camera Connector

FUNC_TEST		
TRUE	=PP5V_S3_CAMERA	43 63
TRUE	=USB2_CAMERA_N	6 43
TRUE	=USB2_CAMERA_P	6 43
TRUE	=SMBUS_ATS_SDA	27 43
TRUE	=SMBUS_ATS_SCL	27 43
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST		
TRUE	HSTHMSNS_DX_P	50
TRUE	HSTHMSNS_DX_N	50
TRUE	RSFSTHMSNS_D_P	50
TRUE	RSFSTHMSNS_D_N	50

Other Func Test Points

FUNC_TEST		
TRUE	=PP1V05_S0_REG	51 61 63
TRUE	PM_SYSRST_L	23 26 47
TRUE	SMC_ONOFF_L	43 47 48 51

Current Sense Calibration

FUNC_TEST		
TRUE	ISENSE_CAL_EN	
TRUE	=PP5V_S0_ISENSECAL	
TRUE	=PP1V8_S3_REG	51 60 63
TRUE	=PP1V5_S0_REG	58 63
TRUE	PPVCORE_S0_GPU	63
TRUE	PPVCORE_S0_CPU	63
TRUE	GND	

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST		
TRUE	SMC_BS_ALRT_L	47 48 64
TRUE	=SMBUS_BATT_SCL	27 64
TRUE	=SMBUS_BATT_SDA	27 64
TRUE	GND_BATT	64

Left I/O Data Connector

FUNC_TEST		
TRUE	=PP1V5_S0_LIO	45 63
TRUE	=PPDCIN_G3H_LIO	45 63
TRUE	=PP5V_S5_LIO	45 63
TRUE	=PP3V42_G3H_LIO	45 63
TRUE	PP5V_S0_AUDIO_PWR	45
TRUE	PP5V_S0_AUDIO	45
TRUE	GND_AUDIO_PWR	45
TRUE	GND_AUDIO	45
TRUE	ACZ_SDATAIN<0>	21 45 79
TRUE	ACZ_SDATAOUT	21 45 79
TRUE	ACZ_BITCLK	21 45 79
TRUE	ACZ_RST_L	21 45 79
TRUE	EXCARD_OC_L	6 45 48
TRUE	LTUSB_OC_L	6 45
TRUE	LIO_BATT_ISENSE	45 51
TRUE	SMC_SYS_ISET	45 47
TRUE	SMC_BATT_ISET	45 47
TRUE	SMC_BATT_CHG_EN	45 47 48
TRUE	SMC_BC_ACOK	45 47 48
TRUE	SMC_ADAPTER_EN	41 45 47 48
TRUE	LIO_P3V3S0_EN_L	45 62
TRUE	LIO_DCIN_ISENSE	45 51
TRUE	LIO_P3V3S3_EN	45 62
TRUE	SMC_BATT_TRICKLE_EN_L	45 47 48
TRUE	SYS_ONEWIRE	45 47 48
TRUE	MINI_CLKREQ_L	34 45
TRUE	SMC_EXCARD_CP	45 47 48
TRUE	EXCARD_CLKREQ_L	34 45
TRUE	SMC_EXCARD_PWR_EN	45 47
TRUE	LIO_PLT_RESET_L	26 45
TRUE	ACZ_SYNC	21 45 79
TRUE	=USB2_LT_N	6 45
TRUE	=USB2_LT_P	6 45
TRUE	=USB2_EXCARD_N	6 45
TRUE	=USB2_EXCARD_P	6 45
TRUE	=PCIE_EXCARD_R2D_N	45 46
TRUE	=PCIE_EXCARD_R2D_P	45 46
TRUE	=PCIE_EXCARD_D2R_N	45 46
TRUE	=PCIE_EXCARD_D2R_P	45 46
TRUE	PCIE_CLK100M_EXCARD_P	34 45
TRUE	PCIE_CLK100M_EXCARD_N	34 45
TRUE	=PCIE_MINI_R2D_N	45 46
TRUE	=PCIE_MINI_R2D_P	45 46
TRUE	=PCIE_MINI_D2R_N	45 46
TRUE	=PCIE_MINI_D2R_P	45 46
TRUE	PCIE_CLK100M_MINI_P	34 45
TRUE	PCIE_CLK100M_MINI_N	34 45
TRUE	=SMBUS_LIO_SMC_SCL	27 45
TRUE	=SMBUS_LIO_SMC_SDA	27 45
TRUE	=SMBUS_LIO_SB_SCL	27 45
TRUE	=SMBUS_LIO_SB_SDA	27 45
TRUE	PCIE_WAKE_L	23 37 45

Left I/O Power Connector

FUNC_TEST		
TRUE	=PPBUS_G3H_LIO_CONN	63 64
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

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NC_CPU_A32_L — TP_CPU_A32_L (7)
NC_CPU_A33_L — TP_CPU_A33_L (7)
NC_CPU_A34_L — TP_CPU_A34_L (7)
NC_CPU_A35_L — TP_CPU_A35_L (7)
NC_CPU_A36_L — TP_CPU_A36_L (7)
NC_CPU_A37_L — TP_CPU_A37_L (7)
NC_CPU_A38_L — TP_CPU_A38_L (7)
NC_CPU_A39_L — TP_CPU_A39_L (7)
NC_CPU_APM0_L — TP_CPU_APM0_L (7)
NC_CPU_APM1_L — TP_CPU_APM1_L (7)
NC_CPU_EXTBREF — TP_CPU_EXTBREF (7)
NC_CPU_HFPLL — TP_CPU_HFPLL (7)
NC_CPU_SPARE0 — TP_CPU_SPARE0 (7)
NC_CPU_SPARE1 — TP_CPU_SPARE1 (7)
NC_CPU_SPARE2 — TP_CPU_SPARE2 (7)
NC_CPU_SPARE4 — TP_CPU_SPARE4 (7)

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28)
NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29)
TP_NB_CFG<4..3> — NB_CFG<4..3> (14)
TP_NB_CFG<6> — NB_CFG<6> (14)
TP_NB_CFG<8> — NB_CFG<8> (14)
TP_NB_CFG<11..10> — NB_CFG<11..10> (14)
TP_NB_CFG<15..14> — NB_CFG<15..14> (14)
TP_NB_CFG<17> — NB_CFG<17> (14)

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14)

TP_SB_SUS_CLK — SUS_CLK_SB (23)

NC_SB_XOR_T5 — TP_SB_XOR_T5 (21)
NC_SB_XOR_U5 — TP_SB_XOR_U5 (21)
NC_SB_XOR_V3 — TP_SB_XOR_V3 (21)
NC_SB_XOR_V4 — TP_SB_XOR_V4 (21)
NC_SB_XOR_W3 — TP_SB_XOR_W3 (21)

TP_SMC_RSTGATE_L — SMC_RSTGATE_L (47)
ALS_GAIN (76 47 5) — =RTALS_GAIN (53)

NC_ENET_CTRL12 — ENET_CTRL12 (37)
NC_ENET_CTRL25 — ENET_CTRL25 (37)

Ethernet Power Management Support

ENET_LOM_DISABLE
R0600
0
5%
1/16W
MF-LF
402
22 IN SB_GPIO30 — ENET_LOM_DIS_L 37 OUT

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOM_DISABLE" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P (44) — USB2_RT_P — USB_A_P (22)
=USB2_RT_N (44) — USB2_RT_N — USB_A_N (22)
=RTUSB_OC_L (44) — RTUSB_OC_L — USB_A_OC_L (22)

USB Port "B" = Trackpad (Geyser)

=USB_TRACKPAD_P (43) — USB_TRACKPAD_P — USB_B_P (22)
=USB_TRACKPAD_N (43) — USB_TRACKPAD_N — USB_B_N (22)
UNUSED_USB_B_OC_L — USB_B_OC_L (22)

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P (45 5) — USB2_LT_P — USB_C_P (22)
=USB2_LT_N (45 5) — USB2_LT_N — USB_C_N (22)
LTUSB_OC_L — USB_C_OC_L (22)

USB Port "D" = Camera

=USB2_CAMERA_P (43 5) — USB2_CAMERA_P — USB_D_P (22)
=USB2_CAMERA_N (43 5) — USB2_CAMERA_N — USB_D_N (22)
UNUSED_USB_D_OC_L — USB_D_OC_L (22)

USB Port "E" = ExpressCard

=USB2_EXCARD_P (45 5) — USB2_EXCARD_P — USB_E_P (22)
=USB2_EXCARD_N (45 5) — USB2_EXCARD_N — USB_E_N (22)
EXCARD_OC_L (48 45 5) — USB_E_OC_L (22)

USB Port "F" = IR Receiver

=USB_IR_P (76) — USB_IR_P — USB_F_P (22)
=USB_IR_N (76) — USB_IR_N — USB_F_N (22)

USB Port "G" = Bluetooth (M13P)

=USB_BT_P (76) — USB_BT_P — USB_G_P (22)
=USB_BT_N (76) — USB_BT_N — USB_G_N (22)

USB Port "H" = Reserved (PCI-E Mini Card)

TP_USB2_HP — USB_H_P (22)
TP_USB2_HN — USB_H_N (22)

Trace deleted to make room for other diffpairs over RAM connector.

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1
GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
— =GND_CHASSIS_DVI2 (75)
— =GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1
GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
— =GND_CHASSIS_DVI1 (75)
— =GND_CHASSIS_DVI3 (75)
— =GND_CHASSIS_DVI5 (75)
— =GND_CHASSIS_ENET (38)
— =GND_CHASSIS_FW_EMI (42)
— =GND_CHASSIS_FW_PORT1 (42)
— =GND_CHASSIS_RTUSB (44)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
1
GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
— =GND_CHASSIS_LCD1 (74)
— =GND_CHASSIS_LCD2 (74)
— =GND_CHASSIS_LCD3 (74)
— =GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
1
2
3
GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
MAKE_BASE=TRUE
— =GND_CHASSIS_INVERTER (74)

Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7099 | REV. D

SCALE NONE | SHT 6 OF 104

OMIT

U0700
YONAH
CPU
BGA
(1 OF 4)

ADDR GROUP0

FSB_A_L<3> J4 A3*
FSB_A_L<4> L4 A4*
FSB_A_L<5> M3 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M1 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L1 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> U2 ADSTB0*

FSB_REQ_L<0> K3 REQ0*
FSB_REQ_L<1> H2 REQ1*
FSB_REQ_L<2> K2 REQ2*
FSB_REQ_L<3> J3 REQ3*
FSB_REQ_L<4> L5 REQ4*

ADDR GROUP1

FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U2 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W3 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> W2 A30*
FSB_A_L<31> Y1 A31*
FSB_ADSTB_L<1> AB1 ADSTB1*

CONTROL

ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 FSB_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* B1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

XDP/ITP SIGNALS

BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERM

PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC A25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

HCLK

BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

RESERVED

RSVD1 A1 TP_CPU_A32_L
RSVD2 AA4 TP_CPU_A33_L
RSVD3 AB2 TP_CPU_A34_L
RSVD4 AA3 TP_CPU_A35_L
RSVD5 M4 TP_CPU_A36_L
RSVD6 N5 TP_CPU_A37_L
RSVD7 T2 TP_CPU_A38_L
RSVD8 V3 TP_CPU_A39_L
RSVD9 R2 TP_CPU_APM0_L
RSVD10 C3 TP_CPU_APM1_L
RSVD11 B25 TP_CPU_HFPLL
RSVD12 T22 TP_CPU_EXTBREF
RSVD13 D2 TP_CPU_SPARE0
RSVD14 F6 TP_CPU_SPARE1
RSVD15 D3 TP_CPU_SPARE2
RSVD16 C1 TP_CPU_SPARE3
RSVD17 AF1 TP_CPU_SPARE4
RSVD18 D22 TP_CPU_SPARE5
RSVD19 C23 TP_CPU_SPARE6
RSVD20 C24 TP_CPU_SPARE7

SPARE[7-0],HFPLL:
ROUTE TO TP VIA AND
PLACE GND VIA W/IN 1000 MILS

=PP1V05_S0_CPU 7 8 9 11 63

R0702 54.9 1% 1/16W MF-LF 402

PLACE TESTPOINT ON
FSB_IERR_L WITH A GND
0.1" AWAY

=PP1V05_S0_CPU 7 8 9 11 63

R0703 54.9 1% 1/16W MF-LF 402

R0704 68 5% 1/16W MF-LF 402

CPU_PROCHOT_L TO SMC
AND CPU VR TO INFORM
CPU IS HOT

PM_THRMTRIP#
SHOULD CONNECT TO
ICH7-M AND GMCH
WITHOUT T-ING (NO
STUB)

OMIT

U0700
YONAH
CPU
BGA
(2 OF 4)

DATA GRP0

FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> H22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H26 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H25 D15*
FSB_DSTBN_L<0> K26 DSTBN0*
FSB_DSTBP_L<0> L24 DSTBP0*
FSB_DINV_L<0> G26 DINV0*

DATA GRP1

FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L25 D20*
FSB_D_L<21> L22 D21*
FSB_D_L<22> L23 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P22 D25*
FSB_D_L<26> P23 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L26 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N24 D31*
FSB_DSTBN_L<1> M24 DSTBN1*
FSB_DSTBP_L<1> N25 DSTBP1*
FSB_DINV_L<1> L26 DINV1*

DATA GRP2

D32* AA23 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* W25 FSB_D_L<36>
D37* U23 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U22 FSB_D_L<39>
D40* AB25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* AA26 FSB_D_L<43>
D44* Y26 FSB_D_L<44>
D45* Y22 FSB_D_L<45>
D46* AC26 FSB_D_L<46>
D47* AA24 FSB_D_L<47>
DSTBN2* W24 FSB_DSTBN_L<2>
DSTBP2* Y25 FSB_DSTBP_L<2>
DINV2* V23 FSB_DINV_L<2>

DATA GRP3

D48* AC22 FSB_D_L<48>
D49* AC23 FSB_D_L<49>
D50* AB22 FSB_D_L<50>
D51* AA21 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC25 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AD24 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AE25 FSB_D_L<60>
D61* AF25 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AF26 FSB_D_L<63>
DSTBN3* AD23 FSB_DSTBN_L<3>
DSTBP3* AE24 FSB_DSTBP_L<3>
DINV3* AC20 FSB_DINV_L<3>

MISC

GTLREF AD26
NC A2
TEST1 C26 CPU_TEST1
TEST2 D25 CPU_TEST2
BSEL0 B22 CPU_BSEL<0>
BSEL1 B23 CPU_BSEL<1>
BSEL2 C21 CPU_BSEL<2>

COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 U1 CPU_COMP<2>
COMP3 V1 CPU_COMP<3>

DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_SLPCPU_L
PSI* AE6 CPU_PSI_L

=PP1V05_S0_CPU 63 11 9 8 7

R0705 1K 1% 1/16W MF-LF 402

CPU_GTLREF 25

R0706 2.0K 1% 1/16W MF-LF 402

LAYOUT NOTE: 0.5" MAX LENGTH

NOSTUFF
R0730 0 1 2 402

R0712 5K 5% 1/16W MF-LF 402

NOSTUFF
R0707 1K 5% 1/16W MF-LF 402

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".

R0716 27.4 1% 402
R0717 54.9 1% 402
R0718 27.4 1% 402
R0719 54.9 1% 402

=PP1V05_S0_CPU 7 8 9 11 63

XDP_TMS 11 7
R0720 54.9 1% 402

XDP_TDI 11 7
R0721 54.9 1% 402

XDP_TCK 11 7
R0722 54.9 1% 402

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

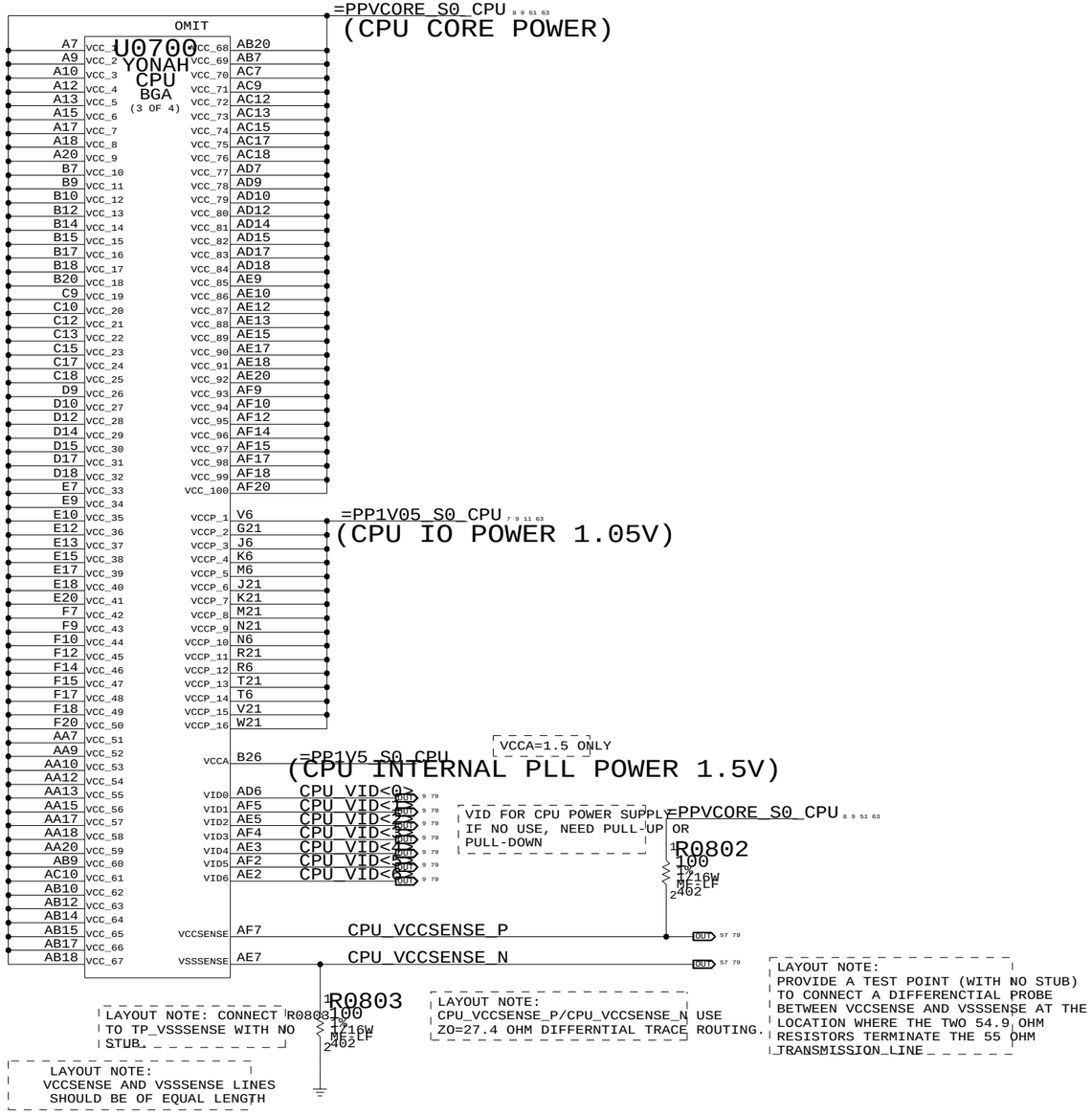
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

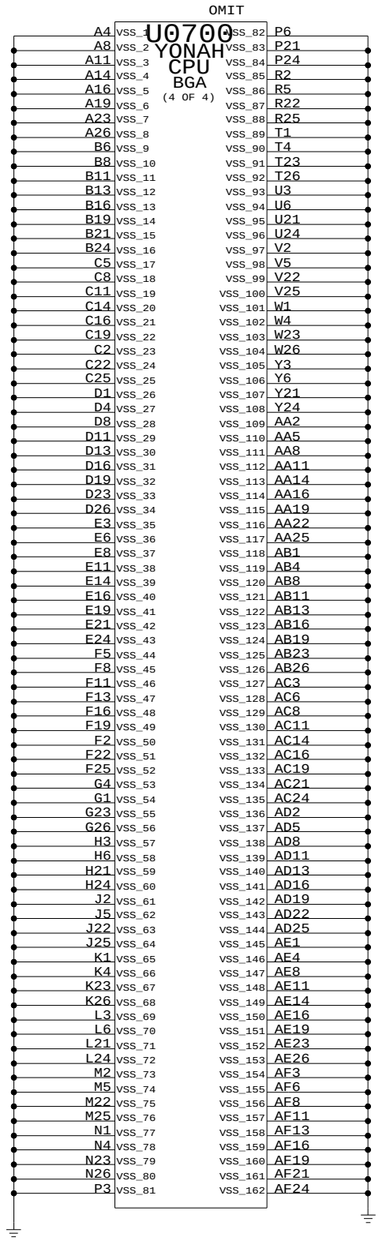
CPU 1 OF 2-FSB

SYNC_MASTER=M42 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 7 OF 104	





CPU 2 OF 2-PWR/GND

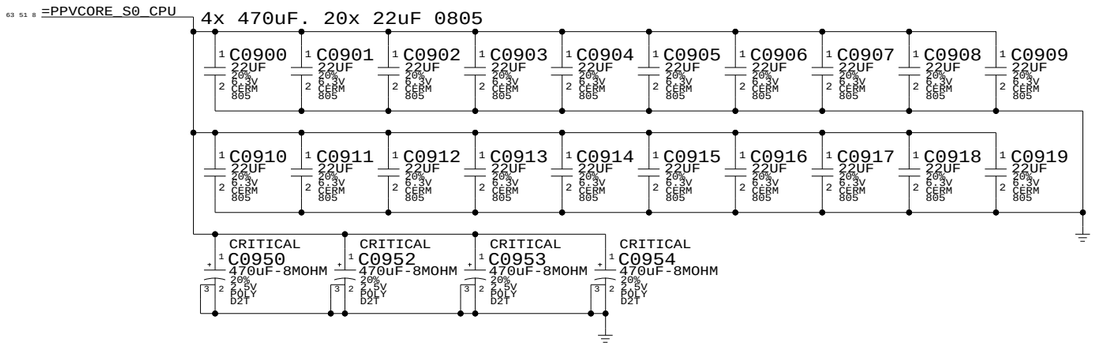
SYNC_MASTER=M42 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

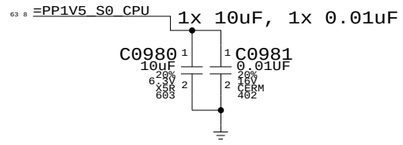
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	8	104

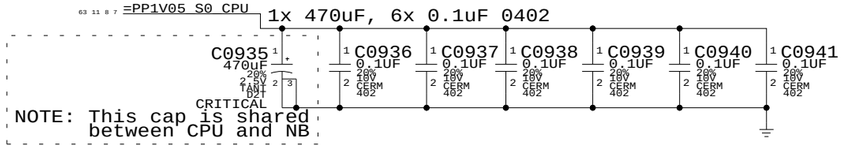
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

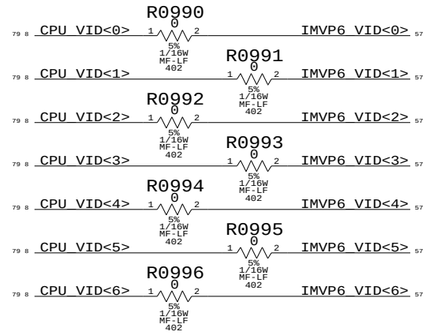


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



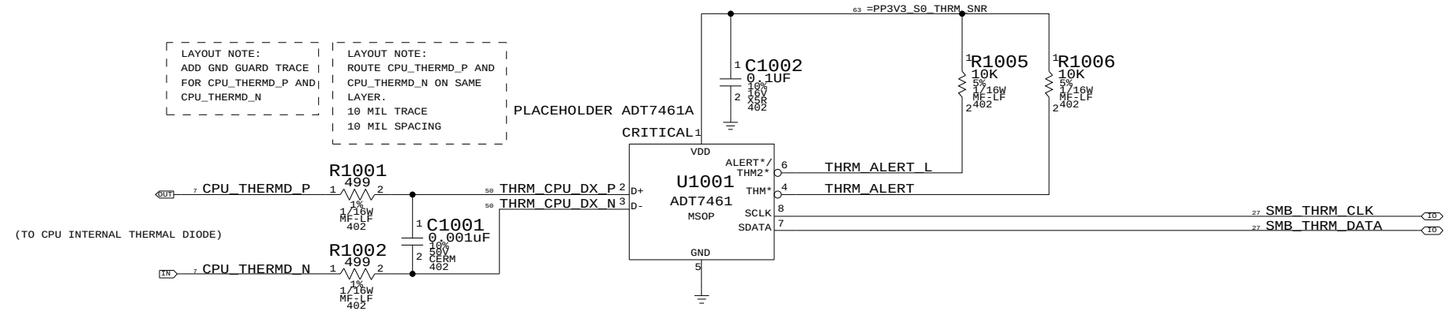
CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 9 OF 104	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

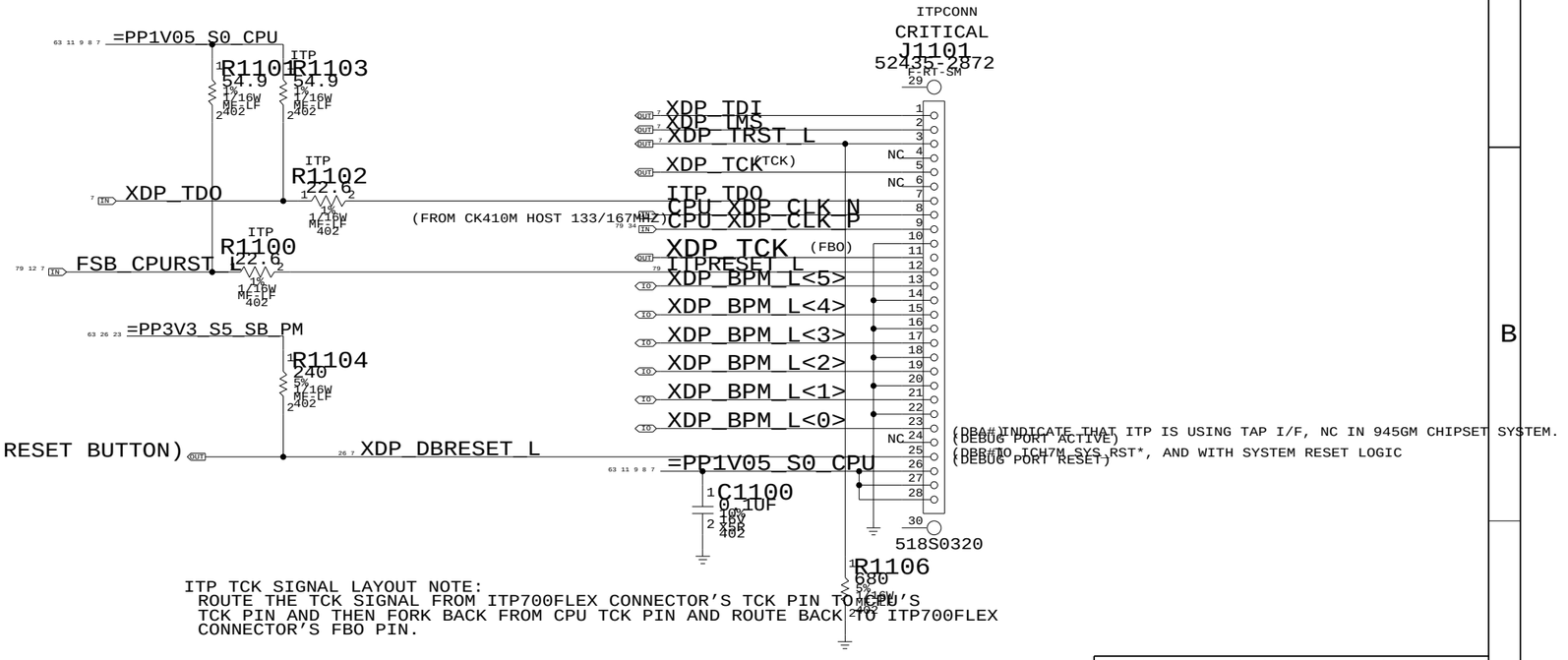
SYNC_MASTER=M42 SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	10	104

CPU ITP700FLEX DEBUG SUPPORT

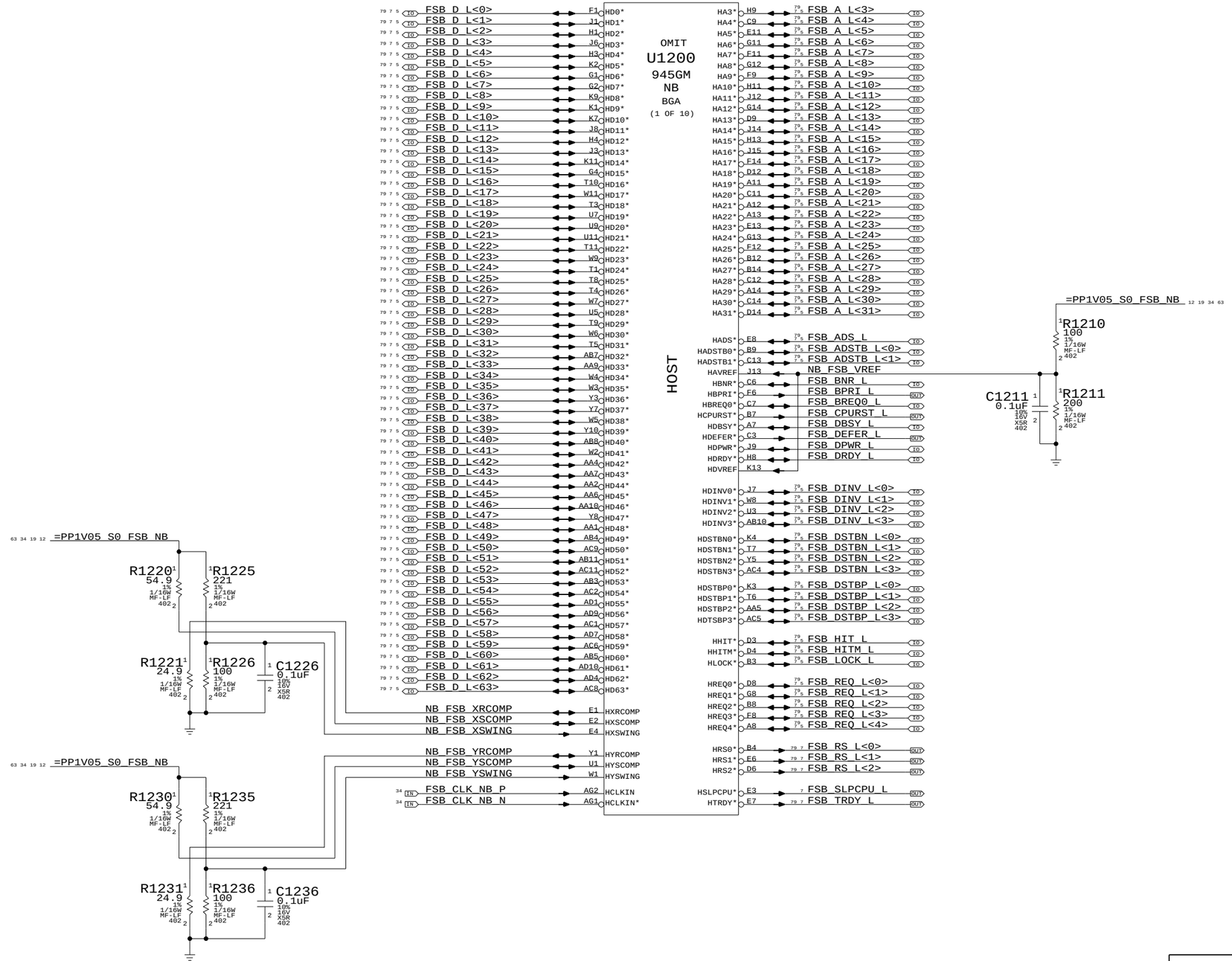


ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=M52 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7099	D
	SCALE	SHT	OF
	NONE	11	104



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	12	104

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

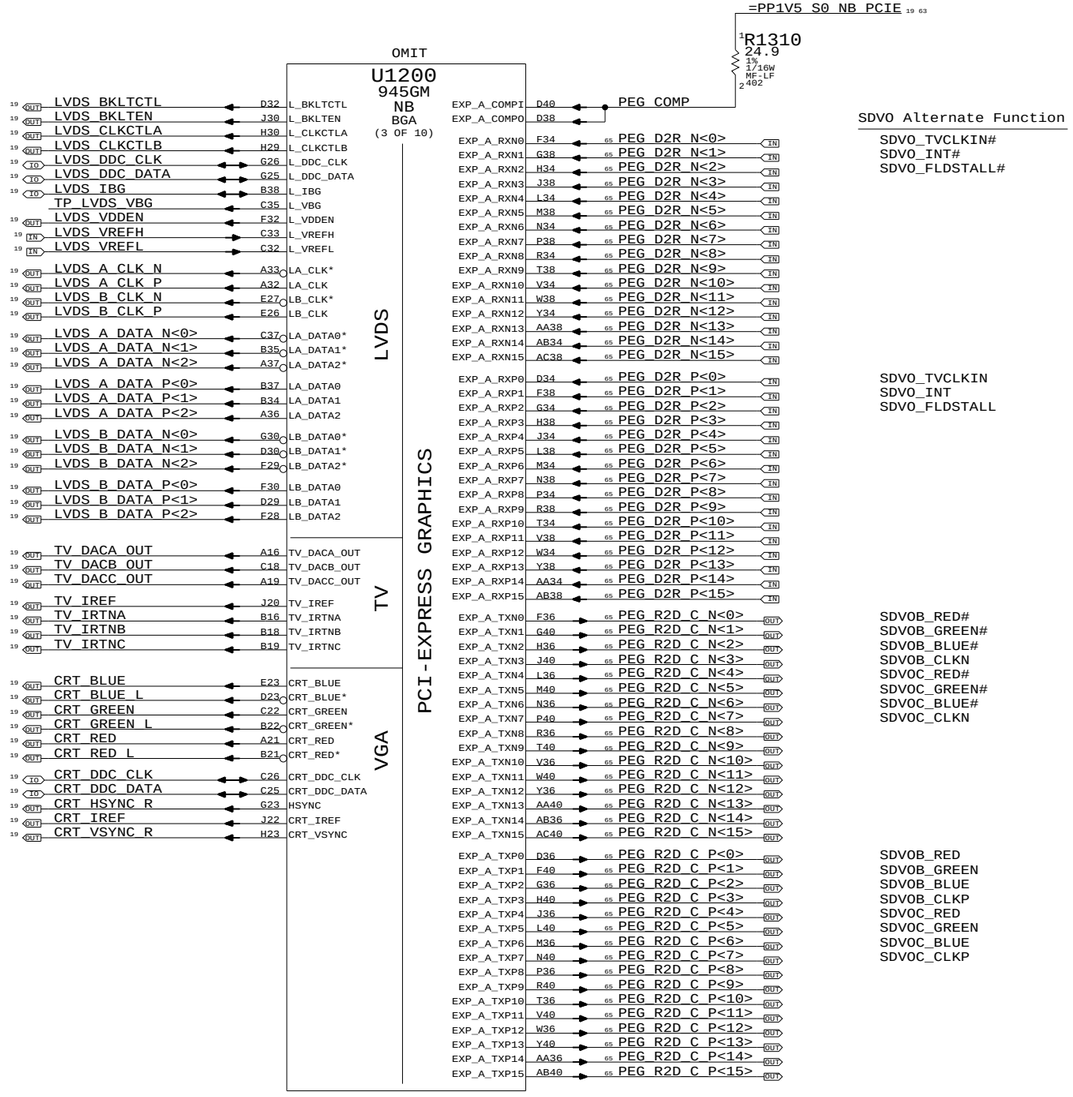
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



NB PEG / Video Interfaces

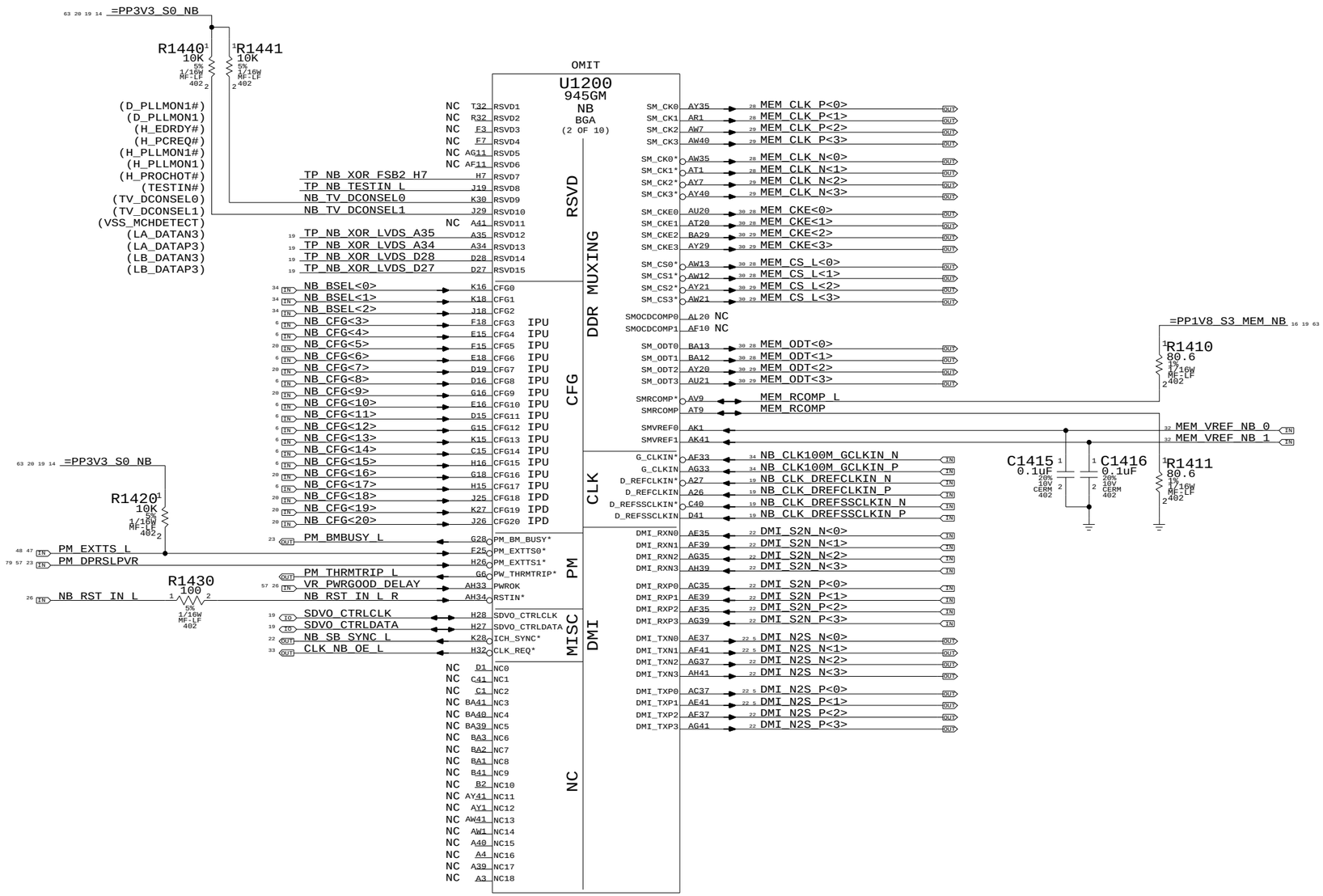
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE

SHT 13 OF 104



NB Misc Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	14	104

OMIT

U1200
945GM
NB
BGA
(4 OF 10)

DDR SYSTEM MEMORY A

28	MEM_A_DQ<0>	AJ35	SA_DQ0	SA_BS0	AU12
28	MEM_A_DQ<1>	AJ34	SA_DQ1	SA_BS1	AV14
28	MEM_A_DQ<2>	AM31	SA_DQ2	SA_BS2	BA20
28	MEM_A_DQ<3>	AM33	SA_DQ3	SA_CAS*	AY13
28	MEM_A_DQ<4>	AJ36	SA_DQ4	SA_DM0	AJ33
28	MEM_A_DQ<5>	AK35	SA_DQ5	SA_DM1	AM35
28	MEM_A_DQ<6>	AJ32	SA_DQ6	SA_DM2	AL26
28	MEM_A_DQ<7>	AH31	SA_DQ7	SA_DM3	AN22
28	MEM_A_DQ<8>	AN35	SA_DQ8	SA_DM4	AM14
28	MEM_A_DQ<9>	AP33	SA_DQ9	SA_DM5	AL9
28	MEM_A_DQ<10>	AR31	SA_DQ10	SA_DM6	AR3
28	MEM_A_DQ<11>	AP31	SA_DQ11	SA_DM7	AH4
28	MEM_A_DQ<12>	AN38	SA_DQ12		
28	MEM_A_DQ<13>	AM36	SA_DQ13	SA_DQS0	AK33
28	MEM_A_DQ<14>	AM34	SA_DQ14	SA_DQS1	AT33
28	MEM_A_DQ<15>	AN33	SA_DQ15	SA_DQS2	AN28
28	MEM_A_DQ<16>	AK26	SA_DQ16	SA_DQS3	AM22
28	MEM_A_DQ<17>	AL27	SA_DQ17	SA_DQS4	AN12
28	MEM_A_DQ<18>	AM26	SA_DQ18	SA_DQS5	AN8
28	MEM_A_DQ<19>	AN24	SA_DQ19	SA_DQS6	AP3
28	MEM_A_DQ<20>	AK28	SA_DQ20	SA_DQS7	AG5
28	MEM_A_DQ<21>	AL28	SA_DQ21	SA_DQS0*	AK32
28	MEM_A_DQ<22>	AM24	SA_DQ22	SA_DQS1*	AU33
28	MEM_A_DQ<23>	AP26	SA_DQ23	SA_DQS2*	AN27
28	MEM_A_DQ<24>	AP23	SA_DQ24	SA_DQS3*	AM21
28	MEM_A_DQ<25>	AL22	SA_DQ25	SA_DQS4*	AM12
28	MEM_A_DQ<26>	AP21	SA_DQ26	SA_DQS5*	AL8
28	MEM_A_DQ<27>	AN20	SA_DQ27	SA_DQS6*	AN3
28	MEM_A_DQ<28>	AL23	SA_DQ28	SA_DQS7*	AH5
28	MEM_A_DQ<29>	AP24	SA_DQ29		
28	MEM_A_DQ<30>	AP20	SA_DQ30	SA_MA0	AY16
28	MEM_A_DQ<31>	AT21	SA_DQ31	SA_MA1	AU14
28	MEM_A_DQ<32>	AR12	SA_DQ32	SA_MA2	AW16
28	MEM_A_DQ<33>	AR14	SA_DQ33	SA_MA3	BA16
28	MEM_A_DQ<34>	AP13	SA_DQ34	SA_MA4	BA17
28	MEM_A_DQ<35>	AP12	SA_DQ35	SA_MA5	AU16
28	MEM_A_DQ<36>	AT13	SA_DQ36	SA_MA6	AV17
28	MEM_A_DQ<37>	AT12	SA_DQ37	SA_MA7	AU17
28	MEM_A_DQ<38>	AL14	SA_DQ38	SA_MA8	AW17
28	MEM_A_DQ<39>	AL12	SA_DQ39	SA_MA9	AT16
28	MEM_A_DQ<40>	AK9	SA_DQ40	SA_MA10	AU13
28	MEM_A_DQ<41>	AN7	SA_DQ41	SA_MA11	AT17
28	MEM_A_DQ<42>	AK8	SA_DQ42	SA_MA12	AV20
28	MEM_A_DQ<43>	AK7	SA_DQ43	SA_MA13	AV12
28	MEM_A_DQ<44>	AP9	SA_DQ44		
28	MEM_A_DQ<45>	AN9	SA_DQ45	SA_RAS*	AW14
28	MEM_A_DQ<46>	AT5	SA_DQ46	SA_RCVENIN*	AK23 NC
28	MEM_A_DQ<47>	AL5	SA_DQ47	SA_RCVENOUT*	AK24 NC
28	MEM_A_DQ<48>	AY2	SA_DQ48	SA_WE*	AY14
28	MEM_A_DQ<49>	AW2	SA_DQ49		
28	MEM_A_DQ<50>	AP1	SA_DQ50		
28	MEM_A_DQ<51>	AN2	SA_DQ51		
28	MEM_A_DQ<52>	AV2	SA_DQ52		
28	MEM_A_DQ<53>	AT3	SA_DQ53		
28	MEM_A_DQ<54>	AN1	SA_DQ54		
28	MEM_A_DQ<55>	AL2	SA_DQ55		
28	MEM_A_DQ<56>	AG7	SA_DQ56		
28	MEM_A_DQ<57>	AF9	SA_DQ57		
28	MEM_A_DQ<58>	AG4	SA_DQ58		
28	MEM_A_DQ<59>	AF6	SA_DQ59		
28	MEM_A_DQ<60>	AG9	SA_DQ60		
28	MEM_A_DQ<61>	AH6	SA_DQ61		
28	MEM_A_DQ<62>	AF4	SA_DQ62		
28	MEM_A_DQ<63>	AF8	SA_DQ63		

SA_BS0	AU12	30 28	MEM_A_BS<0>		OUT
SA_BS1	AV14	30 28	MEM_A_BS<1>		OUT
SA_BS2	BA20	30 28	MEM_A_BS<2>		OUT
SA_CAS*	AY13	30 28	MEM_A_CAS_L		OUT
SA_DM0	AJ33	28	MEM_A_DM<0>		OUT
SA_DM1	AM35	28	MEM_A_DM<1>		OUT
SA_DM2	AL26	28	MEM_A_DM<2>		OUT
SA_DM3	AN22	28	MEM_A_DM<3>		OUT
SA_DM4	AM14	28	MEM_A_DM<4>		OUT
SA_DM5	AL9	28	MEM_A_DM<5>		OUT
SA_DM6	AR3	28	MEM_A_DM<6>		OUT
SA_DM7	AH4	28	MEM_A_DM<7>		OUT
SA_DQS0	AK33	28	MEM_A_DQS_P<0>		IO
SA_DQS1	AT33	28	MEM_A_DQS_P<1>		IO
SA_DQS2	AN28	28	MEM_A_DQS_P<2>		IO
SA_DQS3	AM22	28	MEM_A_DQS_P<3>		IO
SA_DQS4	AN12	28	MEM_A_DQS_P<4>		IO
SA_DQS5	AN8	28	MEM_A_DQS_P<5>		IO
SA_DQS6	AP3	28	MEM_A_DQS_P<6>		IO
SA_DQS7	AG5	28	MEM_A_DQS_P<7>		IO
SA_DQS0*	AK32	28	MEM_A_DQS_N<0>		IO
SA_DQS1*	AU33	28	MEM_A_DQS_N<1>		IO
SA_DQS2*	AN27	28	MEM_A_DQS_N<2>		IO
SA_DQS3*	AM21	28	MEM_A_DQS_N<3>		IO
SA_DQS4*	AM12	28	MEM_A_DQS_N<4>		IO
SA_DQS5*	AL8	28	MEM_A_DQS_N<5>		IO
SA_DQS6*	AN3	28	MEM_A_DQS_N<6>		IO
SA_DQS7*	AH5	28	MEM_A_DQS_N<7>		IO
SA_MA0	AY16	30 28	MEM_A_A<0>		OUT
SA_MA1	AU14	30 28	MEM_A_A<1>		OUT
SA_MA2	AW16	30 28	MEM_A_A<2>		OUT
SA_MA3	BA16	30 28	MEM_A_A<3>		OUT
SA_MA4	BA17	30 28	MEM_A_A<4>		OUT
SA_MA5	AU16	30 28	MEM_A_A<5>		OUT
SA_MA6	AV17	30 28	MEM_A_A<6>		OUT
SA_MA7	AU17	30 28	MEM_A_A<7>		OUT
SA_MA8	AW17	30 28	MEM_A_A<8>		OUT
SA_MA9	AT16	30 28	MEM_A_A<9>		OUT
SA_MA10	AU13	30 28	MEM_A_A<10>		OUT
SA_MA11	AT17	30 28	MEM_A_A<11>		OUT
SA_MA12	AV20	30 28	MEM_A_A<12>		OUT
SA_MA13	AV12	30 28	MEM_A_A<13>		OUT
SA_RAS*	AW14	30 28	MEM_A_RAS_L		OUT
SA_RCVENIN*	AK23	NC			
SA_RCVENOUT*	AK24	NC			
SA_WE*	AY14	30 28	MEM_A_WE_L		OUT

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DDR SYSTEM MEMORY B

29	MEM_B_DQ<0>	AK39	SB_DQ0	SB_BS0	AT24
29	MEM_B_DQ<1>	AJ37	SB_DQ1	SB_BS1	AV23
29	MEM_B_DQ<2>	AP39	SB_DQ2	SB_BS2	AY28
29	MEM_B_DQ<3>	AR41	SB_DQ3	SB_CAS*	AR24
29	MEM_B_DQ<4>	AJ38	SB_DQ4	SB_DM0	AK36
29	MEM_B_DQ<5>	AK38	SB_DQ5	SB_DM1	AR38
29	MEM_B_DQ<6>	AN41	SB_DQ6	SB_DM2	AT36
29	MEM_B_DQ<7>	AP41	SB_DQ7	SB_DM3	BA31
29	MEM_B_DQ<8>	AT40	SB_DQ8	SB_DM4	AL17
29	MEM_B_DQ<9>	AV41	SB_DQ9	SB_DM5	AH8
29	MEM_B_DQ<10>	AU38	SB_DQ10	SB_DM6	BA5
29	MEM_B_DQ<11>	AV38	SB_DQ11	SB_DM7	AN4
29	MEM_B_DQ<12>	AP38	SB_DQ12		
29	MEM_B_DQ<13>	AR40	SB_DQ13	SB_DQS0	AM39
29	MEM_B_DQ<14>	AW38	SB_DQ14	SB_DQS1	AT39
29	MEM_B_DQ<15>	AY38	SB_DQ15	SB_DQS2	AU35
29	MEM_B_DQ<16>	BA38	SB_DQ16	SB_DQS3	AR29
29	MEM_B_DQ<17>	AV36	SB_DQ17	SB_DQS4	AR16
29	MEM_B_DQ<18>	AR36	SB_DQ18	SB_DQS5	AR10
29	MEM_B_DQ<19>	AP36	SB_DQ19	SB_DQS6	AR7
29	MEM_B_DQ<20>	BA36	SB_DQ20	SB_DQS7	AN5
29	MEM_B_DQ<21>	AU36	SB_DQ21	SB_DQS0*	AM40
29	MEM_B_DQ<22>	AP35	SB_DQ22	SB_DQS1*	AU39
29	MEM_B_DQ<23>	AP34	SB_DQ23	SB_DQS2*	AT35
29	MEM_B_DQ<24>	AY33	SB_DQ24	SB_DQS3*	AP29
29	MEM_B_DQ<25>	BA33	SB_DQ25	SB_DQS4*	AP16
29	MEM_B_DQ<26>	AT31	SB_DQ26	SB_DQS5*	AT10
29	MEM_B_DQ<27>	AU29	SB_DQ27	SB_DQS6*	AT7
29	MEM_B_DQ<28>	AU31	SB_DQ28	SB_DQS7*	AP5
29	MEM_B_DQ<29>	AW31	SB_DQ29		
29	MEM_B_DQ<30>	AV29	SB_DQ30	SB_MA0	AY23
29	MEM_B_DQ<31>	AW29	SB_DQ31	SB_MA1	AW24
29	MEM_B_DQ<32>	AM19	SB_DQ32	SB_MA2	AY24
29	MEM_B_DQ<33>	AL19	SB_DQ33	SB_MA3	AR28
29	MEM_B_DQ<34>	AP14	SB_DQ34	SB_MA4	AT27
29	MEM_B_DQ<35>	AN14	SB_DQ35	SB_MA5	AT28
29	MEM_B_DQ<36>	AN17	SB_DQ36	SB_MA6	AU27
29	MEM_B_DQ<37>	AM16	SB_DQ37	SB_MA7	AV28
29	MEM_B_DQ<38>	AP15	SB_DQ38	SB_MA8	AV27
29	MEM_B_DQ<39>	AL15	SB_DQ39	SB_MA9	AW27
29	MEM_B_DQ<40>	AJ11	SB_DQ40	SB_MA10	AV24
29	MEM_B_DQ<41>	AH10	SB_DQ41	SB_MA11	BA27
29	MEM_B_DQ<42>	AJ9	SB_DQ42	SB_MA12	AY27
29	MEM_B_DQ<43>	AN10	SB_DQ43	SB_MA13	AR23
29	MEM_B_DQ<44>	AK13	SB_DQ44		
29	MEM_B_DQ<45>	AH11	SB_DQ45	SB_RAS*	AU23
29	MEM_B_DQ<46>	AK10	SB_DQ46	SB_RCVENIN*	AK16 NC
29	MEM_B_DQ<47>	AJ8	SB_DQ47	SB_RCVENOUT*	AK18 NC
29	MEM_B_DQ<48>	BA10	SB_DQ48	SB_WE*	AR27
29	MEM_B_DQ<49>	AW10	SB_DQ49		
29	MEM_B_DQ<50>	BA4	SB_DQ50		
29	MEM_B_DQ<51>	AW4	SB_DQ51		
29	MEM_B_DQ<52>	AY10	SB_DQ52		
29	MEM_B_DQ<53>	AY9	SB_DQ53		
29	MEM_B_DQ<54>	AW5	SB_DQ54		
29	MEM_B_DQ<55>	AY5	SB_DQ55		
29	MEM_B_DQ<56>	AV4	SB_DQ56		
29	MEM_B_DQ<57>	AR5	SB_DQ57		
29	MEM_B_DQ<58>	AK4	SB_DQ58		
29	MEM_B_DQ<59>	AK3	SB_DQ59		
29	MEM_B_DQ<60>	AT4	SB_DQ60		
29	MEM_B_DQ<61>	AK5	SB_DQ61		
29	MEM_B_DQ<62>	AJ5	SB_DQ62		
29	MEM_B_DQ<63>	AJ3	SB_DQ63		

SB_BS0	AT24	30 29	MEM_B_BS<0>		OUT
SB_BS1	AV23	30 29	MEM_B_BS<1>		OUT
SB_BS2	AY28	30 29	MEM_B_BS<2>		OUT
SB_CAS*	AR24	30 29	MEM_B_CAS_L		OUT
SB_DM0	AK36	29	MEM_B_DM<0>		OUT
SB_DM1	AR38	29	MEM_B_DM<1>		OUT
SB_DM2	AT36	29	MEM_B_DM<2>		OUT
SB_DM3	BA31	29	MEM_B_DM<3>		OUT
SB_DM4	AL17	29	MEM_B_DM<4>		OUT
SB_DM5	AH8	29	MEM_B_DM<5>		OUT
SB_DM6	BA5	29	MEM_B_DM<6>		OUT
SB_DM7	AN4	29	MEM_B_DM<7>		OUT
SB_DQS0	AM39	29	MEM_B_DQS_P<0>		IO
SB_DQS1	AT39	29	MEM_B_DQS_P<1>		IO
SB_DQS2	AU35	29	MEM_B_DQS_P<2>		IO
SB_DQS3	AR29	29	MEM_B_DQS_P<3>		IO
SB_DQS4	AR16	29	MEM_B_DQS_P<4>		IO
SB_DQS5	AR10	29	MEM_B_DQS_P<5>		IO
SB_DQS6	AR7	29	MEM_B_DQS_P<6>		IO
SB_DQS7	AN5	29	MEM_B_DQS_P<7>		IO
SB_DQS0*	AM40	29	MEM_B_DQS_N<0>		IO
SB_DQS1*	AU39	29	MEM_B_DQS_N<1>		IO
SB_DQS2*	AT35	29	MEM_B_DQS_N<2>		IO
SB_DQS3*	AP29	29	MEM_B_DQS_N<3>		IO
SB_DQS4*	AP16	29	MEM_B_DQS_N<4>		IO
SB_DQS5*	AT10	29	MEM_B_DQS_N<5>		IO
SB_DQS6*	AT7	29	MEM_B_DQS_N<6>		IO
SB_DQS7*	AP5	29	MEM_B_DQS_N<7>		IO
SB_MA0	AY23	30 29	MEM_B_A<0>		OUT
SB_MA1	AW24	30 29	MEM_B_A<1>		OUT
SB_MA2	AY24	30 29	MEM_B_A<2>		OUT
SB_MA3	AR28	30 29	MEM_B_A<3>		OUT
SB_MA4	AT27	30 29	MEM_B_A<4>		OUT
SB_MA5	AT28	30 29	MEM_B_A<5>		OUT
SB_MA6	AU27	30 29	MEM_B_A<6>		OUT
SB_MA7	AV28	30 29	MEM_B_A<7>		OUT
SB_MA8	AV27	30 29	MEM_B_A<8>		OUT
SB_MA9	AW27	30 29	MEM_B_A<9>		OUT
SB_MA10	AV24	30 29	MEM_B_A<10>		OUT
SB_MA11	BA27	30 29	MEM_B_A<11>		OUT
SB_MA12	AY27	30 29	MEM_B_A<12>		OUT
SB_MA13	AR23	30 29	MEM_B_A<13>		OUT
SB_RAS*	AU23	30 29	MEM_B_RAS_L		OUT
SB_RCVENIN*	AK16	NC			
SB_RCVENOUT*	AK18	NC			
SB_WE*	AR27	30 29	MEM_B_WE_L		OUT

NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE

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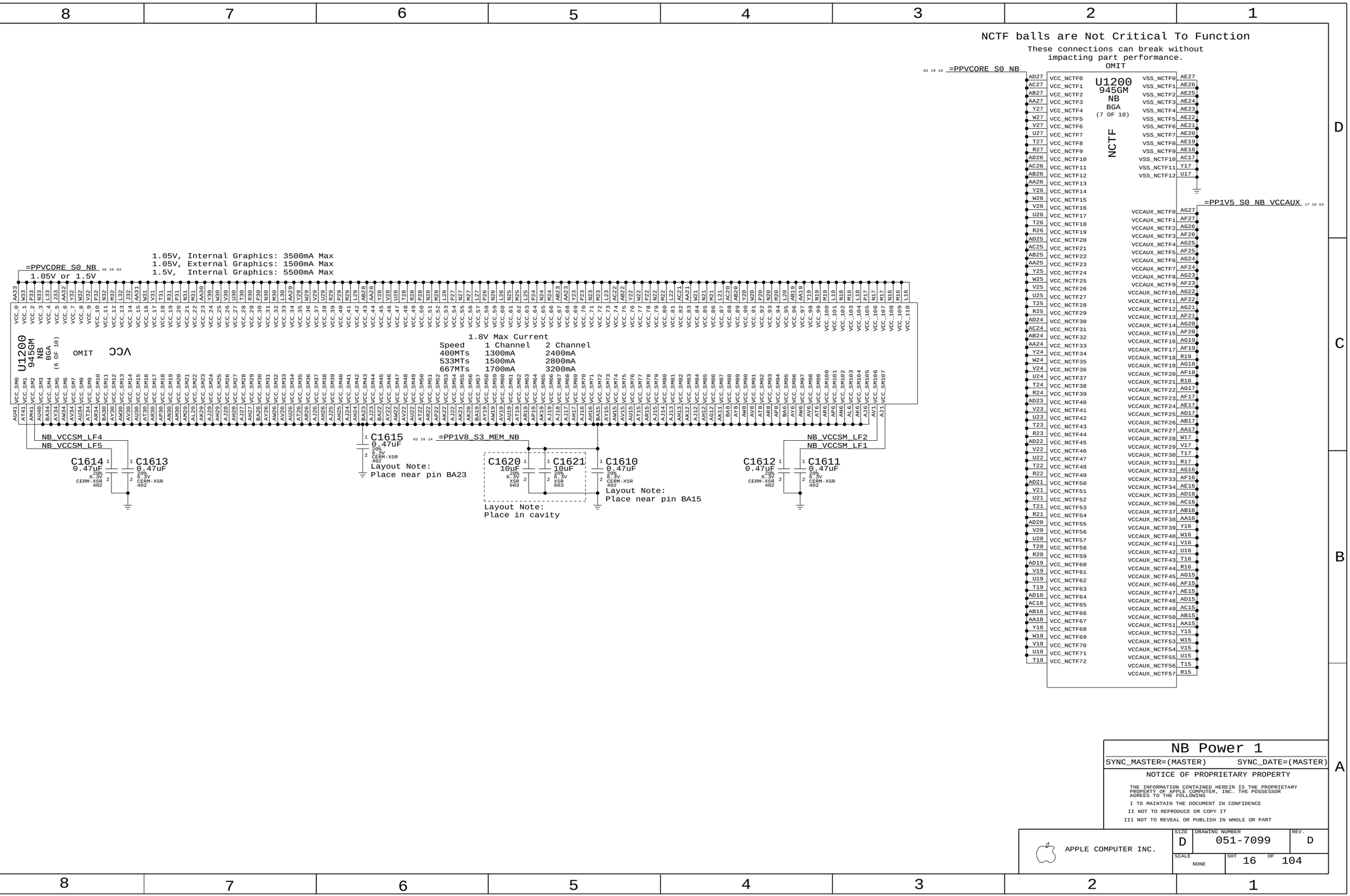


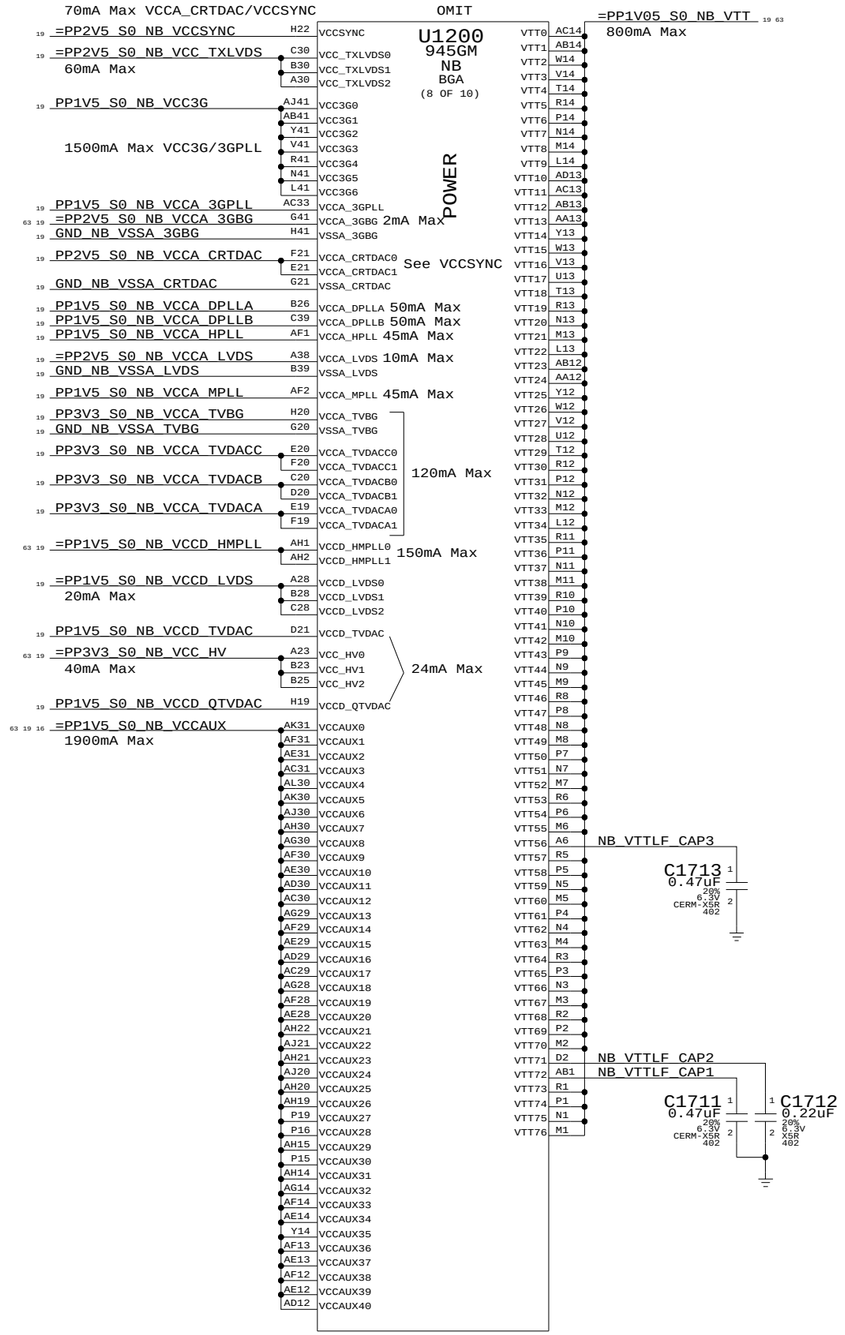
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	16	104



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 17 OF 104	

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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

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Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	1500mA Max
	=PP1V05_S0_FSB_NB	10mA Max?
	=PP1V05_S0_NB_VTT	800mA Max
	=PP1V05_S0_NB_CRT	?mA Max
3674mA Max	=PP1V5_S0_NB	?mA Max
	=PP1V5_S0_NB_3G	1500mA Max
	=PP1V5_S0_NB_3GPLL	
	=PP1V5_S0_NB_PCIE	?mA Max
	=PP1V5_S0_NB_PLL	100mA Max
	=PP1V5_S0_NB_TVDAC	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	150mA Max
	=PP1V5_S0_NB_VCCAUX	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	3200mA Max
	=PP2V5_S0_NB_VCCSYNC	70mA Max
132mA Max	=PP2V5_S0_NB_VCC_TXLVDS	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	2mA Max
	=PP3V3_S0_NB	?mA Max
40mA Max?	=PP3V3_S0_NB_VCC_HV	40mA Max

=PP1V05_S0_NB_CRT

CRT_RED
CRT_GREEN
CRT_BLUE
CRT_RED_L
CRT_GREEN_L
CRT_BLUE_L
CRT_IREF
CRT_HSYNC_R
CRT_VSYNC_R
TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA

=PP1V5_S0_NB_TVDAC

TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL
TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG
TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH
TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0>
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0>
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0>
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0>
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA

(MCH LVDS DATA/CLK TX 2.5V PWR)
=PP2V5_S0_NB_VCC_TXLVDS

(MCH LVDS DIGITAL 1.5V PWR)
=PP1V5_S0_NB_VCCD_LVDS

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS

=PPVCORE_S0_NB

(MCH CRTDAC ANALOG 2.5V PWR)
PP2V5_S0_NB_VCCA_CRTDAC
GND_NB_VSSA_CRTDAC

(MCH H/V SYNC 2.5V PWR)
=PP2V5_S0_NB_VCCSYNC

=PP1V5_S0_NB_TVDAC

(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC

(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA

(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB

(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC

(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG
GND_NB_VSSA_TVBG

(MCH DISPLAY A PLL 1.5V PWR)
TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA

(MCH DISPLAY B PLL 1.5V PWR)
TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB

NB_CLK_DREFCLKIN_P
NB_CLK_DREFCLKIN_N
NB_CLK_DREFSSCLKIN_P
NB_CLK_DREFSSCLKIN_N

=PPVCORE_S0_NB
1500mA Max

GMCH CORE PWR 1.05V BYPASS
CRITICAL
C1900 470uF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

=PP1V05_S0_NB_VTT
800mA Max

MCH VTT BYPASS
(MCH FSB 1.05V PWR)
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note: Place in cavity

(SHARE C0940 470UF)
C1967 0.22uF 20% 6.3V X5R 402
Layout Note: Place on the edge

=PP3V3_S0_NB_VCC_HV
40mA Max

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

=PP2V5_S0_NB_VCCA_3GBG
2mA Max

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)
C1916 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_VCCAUX
1900mA Max

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
C1918 0.1uF 20% 10V CERM 402

=PP1V5_S0_NB_PLL
100mA Max

L1934 FERR-120-OHM-0.2A 0603
C1934 22UF 20% 6.3V CERM 805
C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

L1936 FERR-120-OHM-0.2A 0603
C1936 22UF 20% 6.3V CERM 805
C1937 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
45mA Max

1500mA Max

=PP1V5_S0_NB_3G
L1970 91nH 1210
C1970 220UF 20% 2.5V POLY SMB2
Layout Note: Place L and C close to MCH
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603
Layout Note: 10uF caps should be close to MCH on opposite side.

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

=PP1V5_S0_NB_3GPLL
L1975 1.0UH-220MA-0.12-OHM 0805
R1975 0.51 1% 1/16W MF-LF 402
PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.5V
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402
Layout Note: 3GPLL 10uF cap should be placed in cavity
GND_NB_VSSA_3GBG
Layout Note: Route to caps, then GND

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

1500mA Max

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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SCALE: NONE	SHT 19 OF 104	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075
2.2K
5%
1/16W
MF-LF
2 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<17>	RESERVED

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

=PP3V3_S0_NB 14 19 20 63
NBCFG_VCC_1V5
1 R2058
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<18>
Internal pull-down

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

=PP3V3_S0_NB 14 19 20 63
NBCFG_DMI_REVERSE
1 R2059
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

=PP3V3_S0_NB 14 19 20 63
NBCFG_SDVO_AND_PCIE
1 R2060
2.2K
5%
1/16W
MF-LF
2 402

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

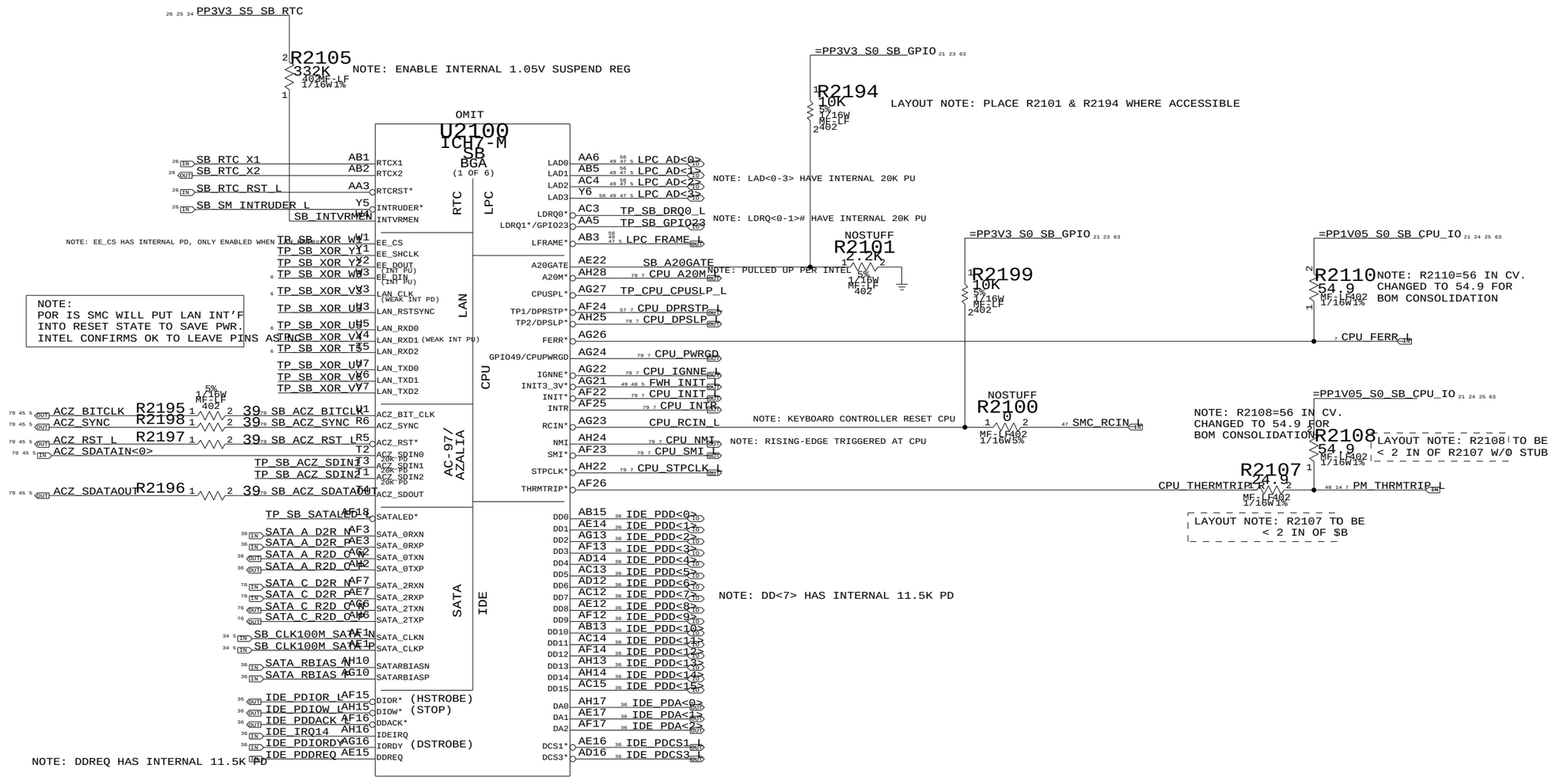
NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7099 | REV. D

SCALE NONE | SHT 20 OF 104



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
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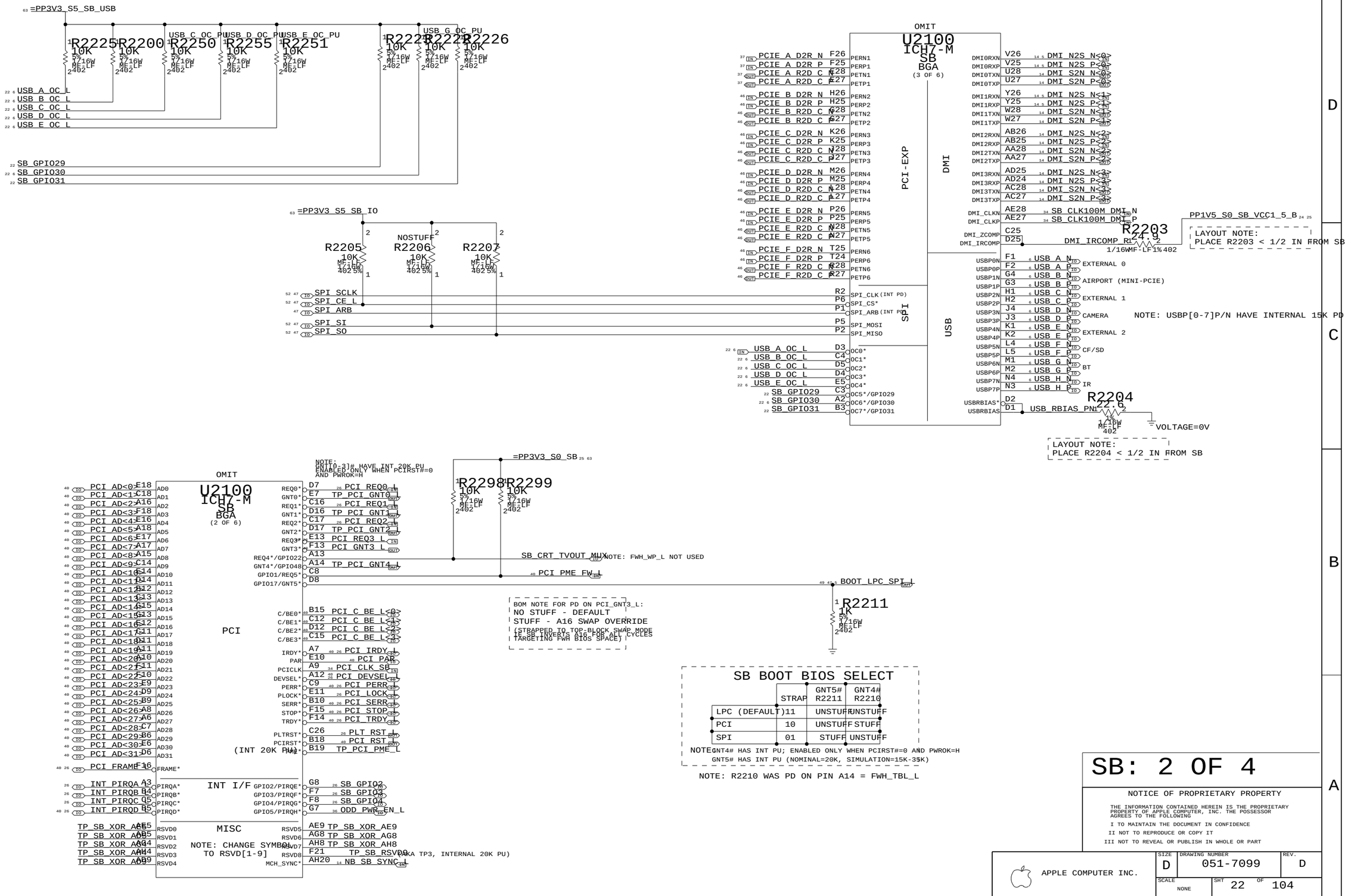
=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2252 10K 5% 1/16W MF-LF 402
R2253 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
USB_G_OC_PU
SB_GPIO29
SB_GPIO30
SB_GPIO31
=PP3V3_S5_SB_IO
R2205 10K 1/16W MF-LF 402 5%
R2206 NOSTUFF 10K 1/16W MF-LF 402 5%
R2207 10K 1/16W MF-LF 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCIE_A_D2R_N F26
PCIE_A_D2R_P F25
PCIE_A_R2D_C_N G28
PCIE_A_R2D_C_P G27
PCIE_B_D2R_N H26
PCIE_B_D2R_P H25
PCIE_B_R2D_C_N G28
PCIE_B_R2D_C_P G27
PCIE_C_D2R_N K26
PCIE_C_D2R_P K25
PCIE_C_R2D_C_N J28
PCIE_C_R2D_C_P J27
PCIE_D_D2R_N M26
PCIE_D_D2R_P M25
PCIE_D_R2D_C_N L28
PCIE_D_R2D_C_P L27
PCIE_E_D2R_N P26
PCIE_E_D2R_P P25
PCIE_E_R2D_C_N N28
PCIE_E_R2D_C_P N27
PCIE_F_D2R_N T25
PCIE_F_D2R_P T24
PCIE_F_R2D_C_N R28
PCIE_F_R2D_C_P R27
PCI-EXP
SPI_CLK (INT PD) R2
SPI_CS* P6
SPI_ARB (INT PU) P1
SPI_MOSI P5
SPI_MISO P2
SPI
USB_A_OC_L D3
USB_B_OC_L C4
USB_C_OC_L D5
USB_D_OC_L D4
USB_E_OC_L E5
SB_GPIO29 C3
SB_GPIO30 A2
SB_GPIO31 B3
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
DMI
DMI0RXN V26 DMI_N2S_N<0>
DMI0RXP V25 DMI_N2S_P<0>
DMI0TXN U28 DMI_S2N_N<0>
DMI0TXP U27 DMI_S2N_P<0>
DMI1RXN Y26 DMI_N2S_N<1>
DMI1RXP Y25 DMI_N2S_P<1>
DMI1TXN W28 DMI_S2N_N<1>
DMI1TXP W27 DMI_S2N_P<1>
DMI2RXN AB26 DMI_N2S_N<2>
DMI2RXP AB25 DMI_N2S_P<2>
DMI2TXN AA28 DMI_S2N_N<2>
DMI2TXP AA27 DMI_S2N_P<2>
DMI3RXN AD25 DMI_N2S_N<3>
DMI3RXP AD24 DMI_N2S_P<3>
DMI3TXN AC28 DMI_S2N_N<3>
DMI3TXP AC27 DMI_S2N_P<3>
DMI_CLKN AE28 SB_CLK100M_DMI_N
DMI_CLKP AE27 SB_CLK100M_DMI_P
DMI_ZCOMP C25
DMI_IRCOMP D25
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
USB
USBP0N F1 USB_A_N EXTERNAL 0
USBP0P F2 USB_A_P
USBP1N G4 USB_B_N AIRPORT (MINI-PCIE)
USBP1P G3 USB_B_P
USBP2N H1 USB_C_N EXTERNAL 1
USBP2P H2 USB_C_P
USBP3N J4 USB_D_N CAMERA
USBP3P J3 USB_D_P
USBP4N K1 USB_E_N EXTERNAL 2
USBP4P K2 USB_E_P
USBP5N L4 USB_F_N CF/SD
USBP5P L5 USB_F_P
USBP6N M1 USB_G_N BT
USBP6P M2 USB_G_P
USBP7N N4 USB_H_N IR
USBP7P N3 USB_H_P
USBRBIAS* D2
USBRBIAS D1
USB_RBIAS_PN1
R2204 22.6 1/16W MF-LF 1% 402
VOLTAGE=0V
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
=PP3V3_S0_SB
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
SB BOOT BIOS SELECT
STRAP | GNT5# R2211 | GNT4# R2210
LPC (DEFAULT) 11 | UNSTUFF | UNSTUFF
PCI 10 | UNSTUFF | STUFF
SPI 01 | STUFF | UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
OMIT
U2100
ICH7-M
SB
BGA
(2 OF 6)
PCI_AD<0> E18 AD0
PCI_AD<1> C18 AD1
PCI_AD<2> A16 AD2
PCI_AD<3> F18 AD3
PCI_AD<4> E16 AD4
PCI_AD<5> A18 AD5
PCI_AD<6> E17 AD6
PCI_AD<7> A17 AD7
PCI_AD<8> A15 AD8
PCI_AD<9> C14 AD9
PCI_AD<10> E14 AD10
PCI_AD<11> D14 AD11
PCI_AD<12> B12 AD12
PCI_AD<13> C13 AD13
PCI_AD<14> C15 AD14
PCI_AD<15> G13 AD15
PCI_AD<16> G12 AD16
PCI_AD<17> C11 AD17
PCI_AD<18> D11 AD18
PCI_AD<19> A11 AD19
PCI_AD<20> A10 AD20
PCI_AD<21> F11 AD21
PCI_AD<22> F10 AD22
PCI_AD<23> E9 AD23
PCI_AD<24> D9 AD24
PCI_AD<25> B9 AD25
PCI_AD<26> A8 AD26
PCI_AD<27> A6 AD27
PCI_AD<28> C7 AD28
PCI_AD<29> B6 AD29
PCI_AD<30> E6 AD30
PCI_AD<31> D6 AD31
PCI_FRAME_L F16 FRAME*
PCI
REQ0* D7 PCI_REQ0_L
GNT0* E7 TP_PCI_GNT0_L
REQ1* C16 PCI_REQ1_L
GNT1* D16 TP_PCI_GNT1_L
REQ2* C17 PCI_REQ2_L
GNT2* D17 TP_PCI_GNT2_L
REQ3* E13 PCI_REQ3_L
GNT3* F13 PCI_GNT3_L
REQ4*/GPIO22 A13
GNT4*/GPIO48 A14 TP_PCI_GNT4_L
GPIO1/REQ5* C8
GPIO17/GNT5* D8
C/BE0* B15 PCI_C_BE_L<0>
C/BE1* C12 PCI_C_BE_L<1>
C/BE2* D12 PCI_C_BE_L<2>
C/BE3* C15 PCI_C_BE_L<3>
IRDY* A7 PCI_IRDY_L
PAR E10 PCI_PAR
PCICLK A9 PCI_CLK_SB
DEVSEL* A12 PCI_DEVSEL_L
PERR* C9 PCI_PERR
PLOCK* E11 PCI_LOCK_L
SERR* B10 PCI_SERR
STOP* F15 PCI_STOP_L
TRDY* F14 PCI_TRDY_L
PLTRST* C26 PLT_RST_L
PCIRST* B18 PCI_RST_L
(INT 20K PU) B19 TP_PCI_PME_L
INT I/F
INT_PIRQA A3 PIRQA*
INT_PIRQB B4 PIRQB*
INT_PIRQC C5 PIRQC*
INT_PIRQD B5 PIRQD*
GPIO2/PIRQE* G8 SB_GPIO2
GPIO3/PIRQF* F7 SB_GPIO3
GPIO4/PIRQG* F8 SB_GPIO4
GPIO5/PIRQH* G7 ODD_PWR_EN_L
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
TP_SB_XOR_AE5 AE5 RSVD0
TP_SB_XOR_AD5 AD5 RSVD1
TP_SB_XOR_AG4 AG4 RSVD2
TP_SB_XOR_AH4 AH4 RSVD3
TP_SB_XOR_AD9 AD9 RSVD4
RSVD5 AE9 TP_SB_XOR_AE9
RSVD6 AG8 TP_SB_XOR_AG8
RSVD7 AH8 TP_SB_XOR_AH8
RSVD8 F21 TP_SB_RSVD8 (ALSO TP3, INTERNAL 20K PU)
MCH_SYNC* AH20 NB_SB_SYNC_L
SB: 2 OF 4
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REV. D
SCALE NONE
SHT 22 OF 104

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 63

=PP3V3_S5_SB 23 25 63

NO_REBOOT_MODE

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 10K 1/16W 402 2MF-LF 5%
R2326 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%
NOSTUFF NOSTUFF

RP2300 10K 5% 1/16W 5M-LF

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 63 25 23

OMIT
U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB_CLK 27 IO → SMBCLK C22
SMB_DATA 27 IO → SMBDATA B22
SMB_LINK_ALERT_L → SMLINKALERT* A16
SMLINK<0> → SMLINK0 B25
SMLINK<1> → SMLINK1 A25
NOT USED
PM_RI_L → RI* A28
SB_SPKR → SPKR (INT WEAK PD) A19
PM_SUS_STAT_L 56 49 48 47 5 OUT → SUS_STAT* A27
PM_SYSRST_L 47 26 5 IN → SYS_RST* A22
PM_BMBUSY_L 14 IN → GPIO0/BM_BUSY* AB18
SMB_ALERT_L → GPIO11/SMBALERT* B23
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L 33 OUT → GPIO18/STPPCI* AC20
PM_STPCPU_L 33 OUT → GPIO20/STPCPU* AF21
SB_GPIO26 → GPIO26 A21
BIOS_REC 23 → GPIO27 B21
FWH_MFG_MODE 23 → GPIO28 E23
PM_CLKRUN_L 56 49 47 40 5 IO → GPIO32/CLKRUN* AG18
TP_AZ_DOCK_EN → GPIO33/AZ_DOCK_EN* AC19
RESERVED FOR MOBILE AZALIA DOCKING INTF
AZ_DOCK_RST → GPIO34/AZ_DOCK_RST* U2
PCIE_WAKE_L 45 37 5 IN → WAKE* F20
INT_SERIRQ 56 49 47 5 IO → SERIRQ AH21
PM_THRM_L 47 IN → THRM* AF20
VR_PWRGD_CK410 26 IN → VRMPWRGD AD22
TP_SB_GPIO6 IO → GPIO6 AC21
SMC_RUNTIME_SCI_L 47 IN → GPIO7 AC18
SMC_EXTSMI_L 47 IN → GPIO8 E21

SMB
CLKS
SYS GPIO
PWR MNGT
GPIO

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

AF19 SB_GPIO21 100 1 2 R2302
AH18 SB_GPIO19 100 1 2 R2303
AH19
AE19 SB_GPIO37 100 1 2 R2305
SATA_C_DET_L 36 IN

AC1 CLK14 ← 34 SB_CLK14P3M_TIMER IN
B2 CLK48 ← 34 SB_CLK48M_USBC_LR IN
C20 SUSCLK ← 6 SUS_CLK_SB OUT

SLP_S3* ← B24 62 47 41 PM_SLP_S3_L OUT
SLP_S4* ← D23 62 47 39 PM_SLP_S4_L OUT
SLP_S5* ← F22 48 47 PM_SLP_S5_L OUT
PWROK ← AA4 26 PM_SB_PWROK IN
AC22 79 57 14 PM_DPRSLPVR OUT
GPIO16/DPRSLPVR
C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
TP0/BATLOW* ← 47 PM_BATLOW_L IN
PWRBTN* ← C23 47 PM_PWRBTN_L IN
(INT 20K PU)
LAN_RST* ← C19 47 PM_LAN_ENABLE IN
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* ← Y4 47 PM_RSMRST_L IN

GPIO9 E20 48 47 SMS_INT_L IN
GPIO10 A20 47 SMC_SB_NMI IN
DEF=GPI GPIO12 F19 23 PATA_PWR_EN_L OUT
GPIO13 E19
DEF=GPI GPIO14 R4 36 IDE_RESET_L OUT
GPIO15 E22 SV_SET_UP 5 23 49
GPIO24 R3 CRB_SV_DET 23
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 AD21 33 SB_CLK100M_SATA_OE_L OUT
GPIO38 AD20 TP_SB_GPIO38 IO
DEF=GPI GPIO39 AE20 23 SATA_C_PWR_EN_L OUT

GPIO

=PP3V3_S5_SB_PM 11 26 63

R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%

R2399 100K 5% 1/16W 402 2MF-LF

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB 63 25 23

R2306 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2308 10K 1/16W 402 2MF-LF 5%

SV_SET_UP 5 23 49
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 63 25 23

R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

R2314 NOSTUFF 0 1/16W 402 2MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 23 25 63

R2390 10K 5% 1/16W 2MF-LF 402

PATA_PWR_EN_L 23

=PP3V3_S0_SB_GPIO 21 23 63

R2388 10K 5% 1/16W 2MF-LF 402

SATA_C_PWR_EN_L 23

SB: 3 OF 4

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

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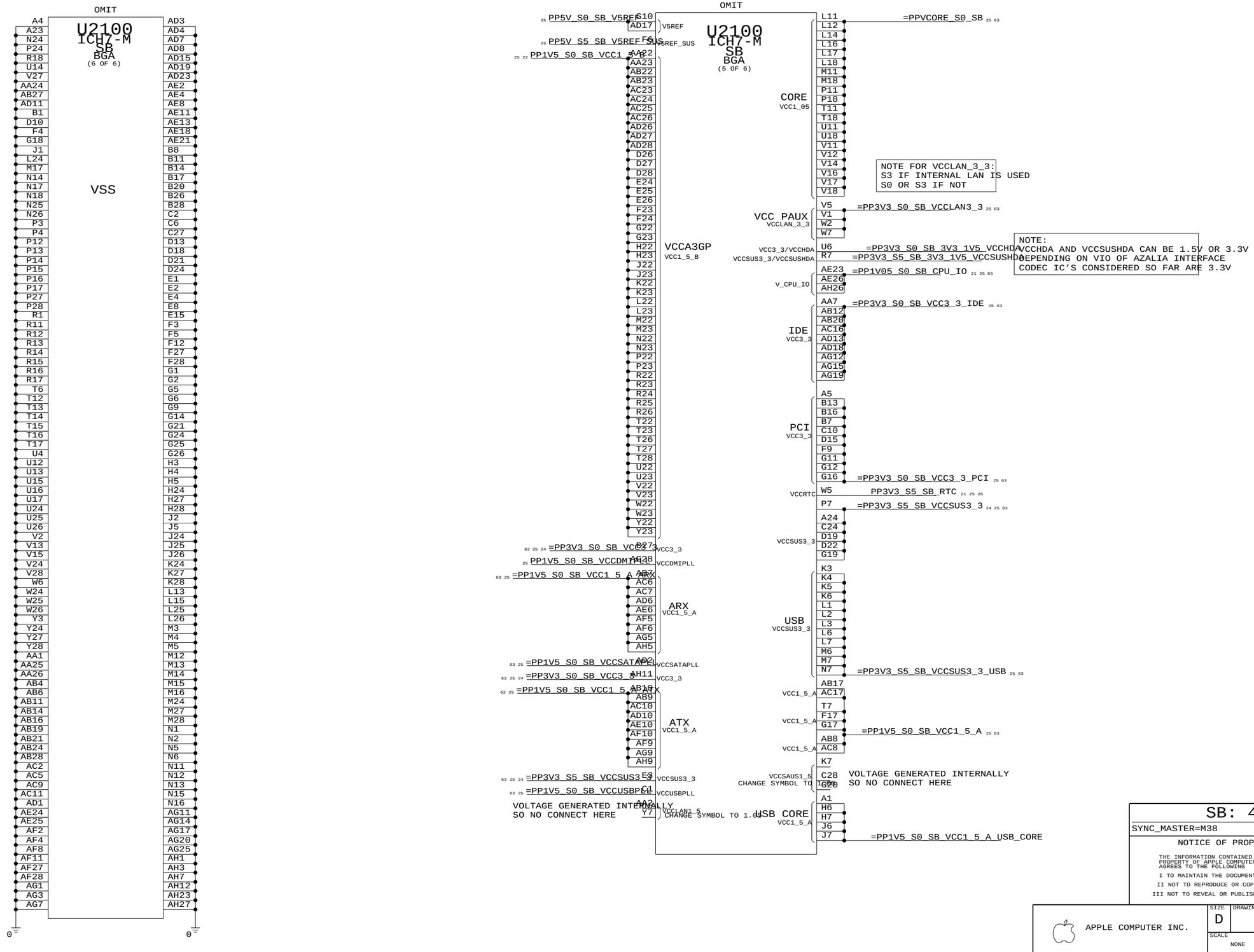
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	23	104


OMIT
U2100
ICH7-M
SB
BGA
(6 OF 6)
VSS
A4 A23 N24 P24 R18 U14 V27 AA24 AB27 AD11 B1 D10 F4 G18 J1 L24 M17 N14 N17 N18 N25 N26 P3 P4 P12 P13 P14 P15 P16 P17 P27 P28 R1 R11 R12 R13 R14 R15 R16 R17 T6 T12 T13 T14 T15 T16 T17 U4 U12 U13 U15 U16 U17 U24 U25 U26 V2 V13 V15 V24 V28 W6 W24 W25 W26 Y3 Y24 Y27 Y28 AA1 AA25 AA26 AB4 AB6 AB11 AB14 AB16 AB19 AB21 AB24 AB28 AC2 AC5 AC9 AC11 AD1 AE24 AE25 AF2 AF4 AF8 AF11 AF27 AF28 AG1 AG3 AG7
AD3 AD4 AD7 AD8 AD15 AD19 AD23 AE2 AE4 AE8 AE11 AE13 AE18 AE21 B8 B11 B14 B17 B20 B26 B28 C2 C6 C27 D13 D18 D21 D24 E1 E2 E4 E8 E15 F3 F5 F12 F27 F28 G1 G2 G5 G6 G9 G14 G21 G24 G25 G26 H3 H4 H5 H24 H27 H28 J2 J5 J24 J25 J26 K24 K27 K28 L13 L15 L25 L26 M3 M4 M5 M12 M13 M14 M15 M16 M24 M27 M28 N1 N2 N5 N6 N11 N12 N13 N15 N16 AG11 AG14 AG17 AG20 AG25 AH1 AH3 AH7 AH12 AH23 AH27
0 0
OMIT
U2100
ICH7-M
SB
BGA
(5 OF 6)
25 PP5V_S0_SB_V5REF
25 PP5V_S5_SB_V5REF_SUS
25 22 PP1V5_S0_SB_VCC1_5_A
G10 AD17 V5REF
F9 V5REF_SUS
AA22 AA23 AB22 AB23 AC23 AC24 AC25 AC26 AD26 AD27 AD28 D26 D27 D28 E24 E25 E26 F23 F24 G22 G23 H22 H23 J22 J23 K22 K23 L22 L23 M22 M23 N22 N23 P22 P23 R22 R23 R24 R25 R26 T22 T23 T26 T27 T28 U22 U23 V22 V23 W22 W23 Y22 Y23
VCCA3GP
VCC1_5_B
63 25 24 =PP3V3_S0_SB_VCC3_3
P27 VCC3_3
25 PP1V5_S0_SB_VCCDMIPLL
AG28 VCCDMIPLL
63 25 =PP1V5_S0_SB_VCC1_5_A_ARX
AB7 AC6 AC7 AD6 AE6 AF5 AF6 AG5 AH5
ARX
VCC1_5_A
63 25 =PP1V5_S0_SB_VCCSATAPLL
AD2 VCCSATAPLL
63 25 24 =PP3V3_S0_SB_VCC3_3
AH11 VCC3_3
63 25 =PP1V5_S0_SB_VCC1_5_A_ATX
AB10 AB9 AC10 AD10 AE10 AF10 AF9 AG9 AH9
ATX
VCC1_5_A
63 25 24 =PP3V3_S5_SB_VCCSUS3_3
F3 VCCSUS3_3
63 25 =PP1V5_S0_SB_VCCUSBPLL
C1 VCCUSBPLL
VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE
A2 Y7 VCCLAN1_5
CHANGE SYMBOL TO 1.0V
L11 =PPVCORE_S0_SB 25 63
L12 L14 L16 L17 L18 M11 M18 P11 P18 T11 T18 U11 U18 V11 V12 V14 V16 V17 V18
CORE
VCC1_05
NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT
V5 =PP3V3_S0_SB_VCCLAN3_3 25 63
V1 W2 W7
VCC_PAUX
VCCLAN_3_3
U6 =PP3V3_S0_SB_3V3_1V5_VCCHDA
VCC3_3/VCCHDA
R7 =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA
VCCSUS3_3/VCCSUSHDA
NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V
AE23 =PP1V05_S0_SB_CPU_IO 21 25 63
AE26 AH26
V_CPU_IO
AA7 =PP3V3_S0_SB_VCC3_3_IDE 25 63
AB12 AB20 AC16 AD13 AD18 AG12 AG15 AG19
IDE
VCC3_3
A5 B13 B16 B7 C10 D15 F9 G11 G12 G16 =PP3V3_S0_SB_VCC3_3_PCI 25 63
PCI
VCC3_3
W5 PP3V3_S5_SB_RTC 21 25 26
VCCRTC
P7 =PP3V3_S5_SB_VCCSUS3_3 24 25 63
A24 C24 D19 D22 G19
VCCSUS3_3
K3 K4 K5 K6 L1 L2 L3 L6 L7 M6 M7 N7 =PP3V3_S5_SB_VCCSUS3_3_USB 25 63
USB
VCCSUS3_3
AB17 AC17 T7 F17 G17 =PP1V5_S0_SB_VCC1_5_A 25 63 AB8 AC8
VCC1_5_A
K7 C28 VOLTAGE GENERATED INTERNALLY
VCCSAUS1_5 SO NO CONNECT HERE
CHANGE SYMBOL TO 1.0V G20
A1 H6 H7 J6 J7 =PP1V5_S0_SB_VCC1_5_A_USB_CORE
USB CORE
VCC1_5_A
SB: 4 OF 4
SYNC_MASTER=M38
SYNC_DATE=11/16/2005
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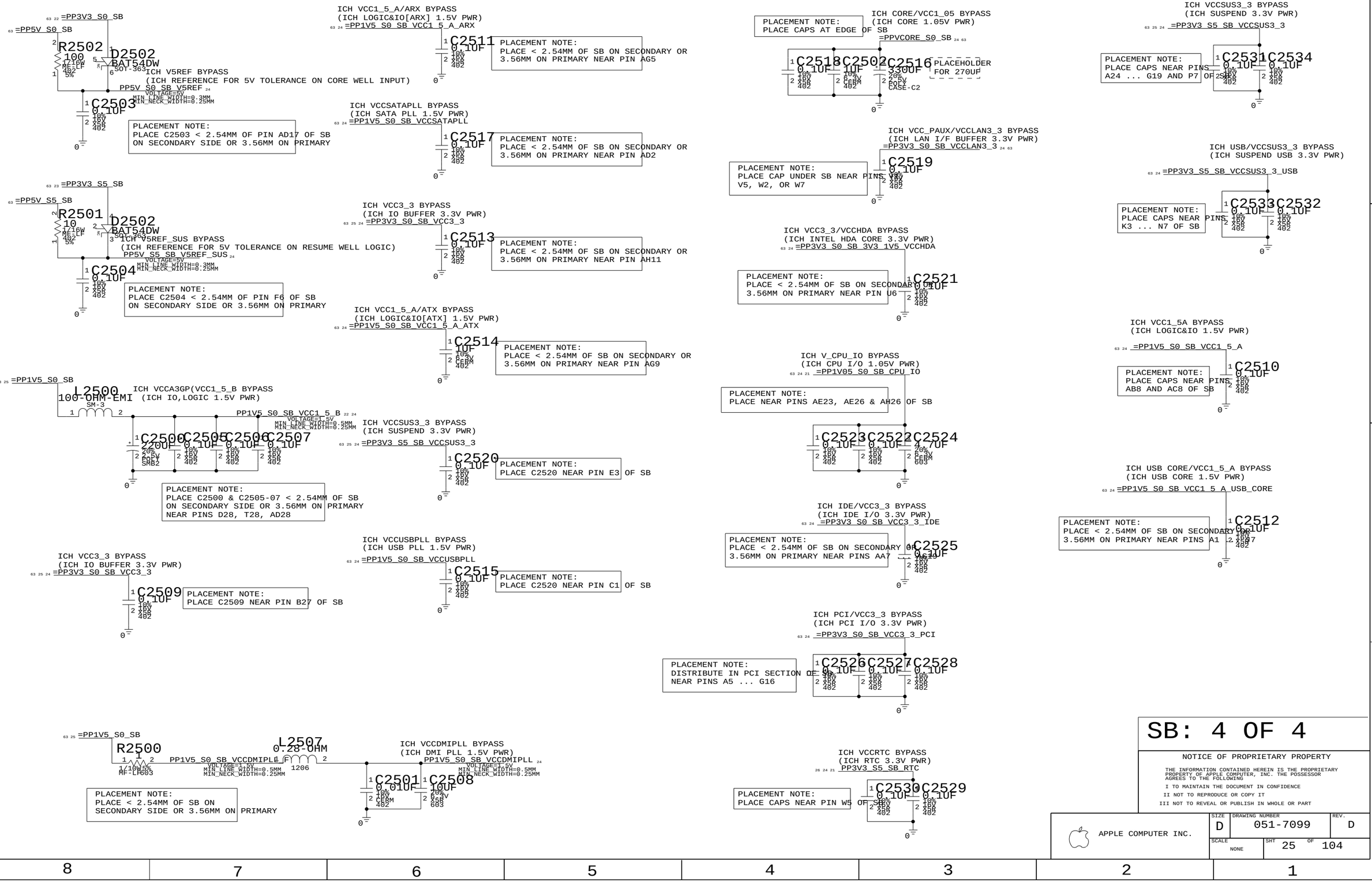
REV. D
SCALE NONE
SHT 24 OF 104


ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
100-OHM-EMI
PP1V5_S0_SB_VCC1_5_B
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
PLACEHOLDER
FOR 270UF
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V5,
V5, W2, OR W7
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1
SB: 4 OF 4
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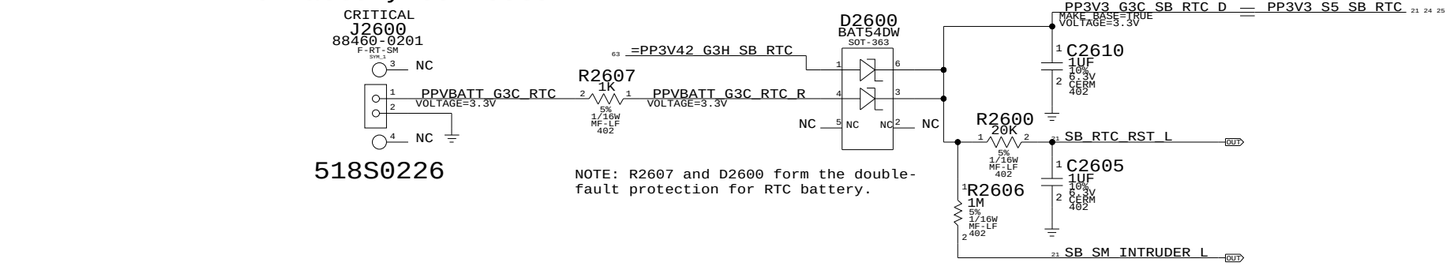
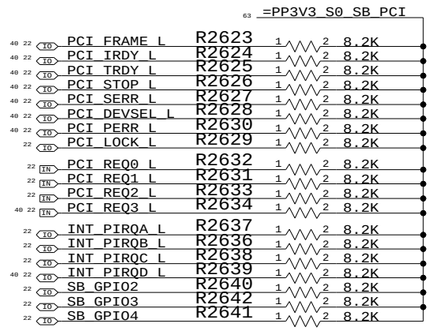
SHT 25 OF 104

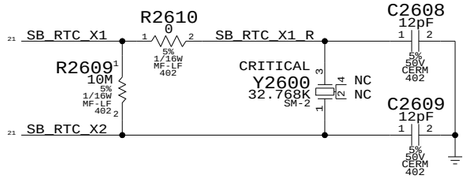
RTC Battery Connector

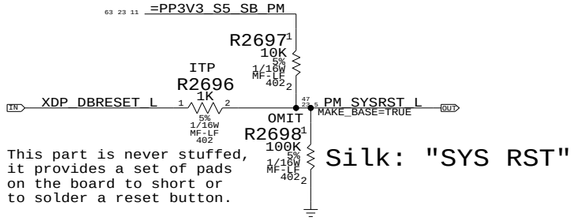


NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



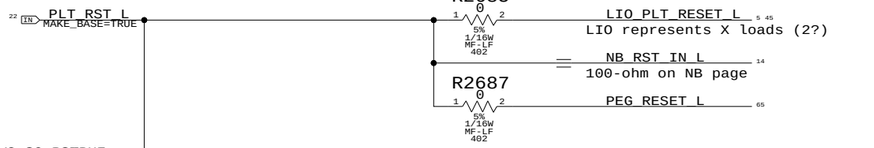


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

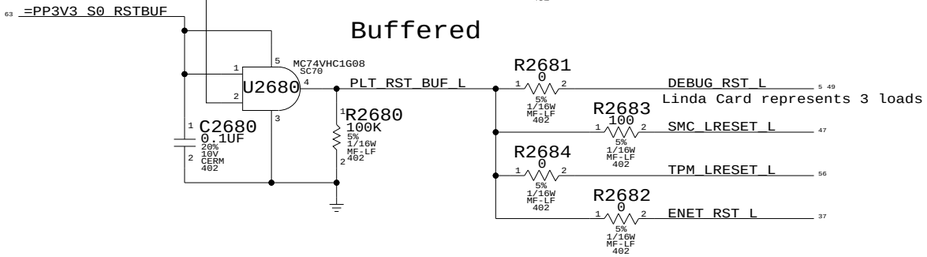
Silk: "SYS RST"

Platform Reset Connections

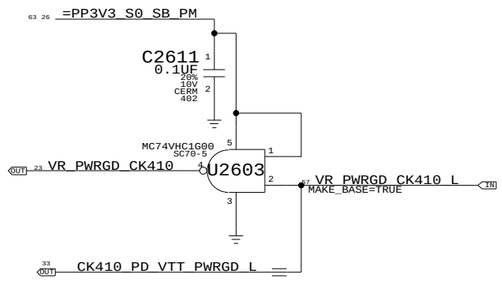
Unbuffered



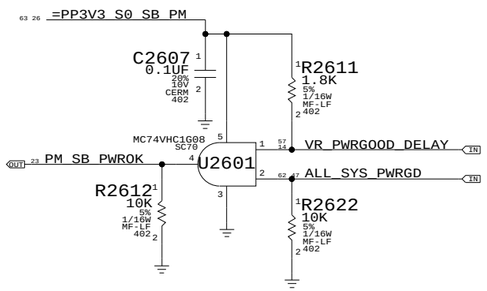
Buffered



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



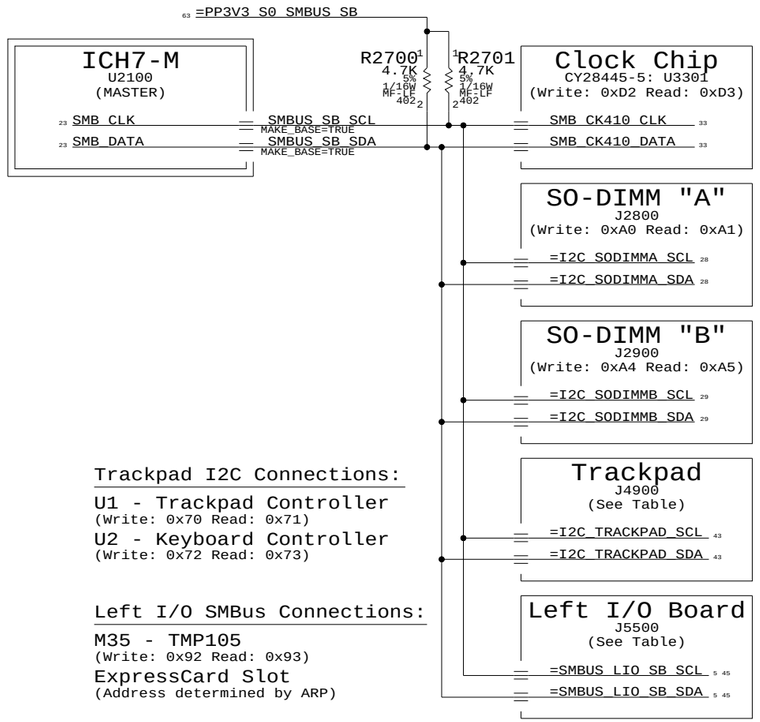
SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 26 OF 104	

ICH7-M SMBus Connections



Trackpad I2C Connections:

U1 - Trackpad Controller
(Write: 0x70 Read: 0x71)

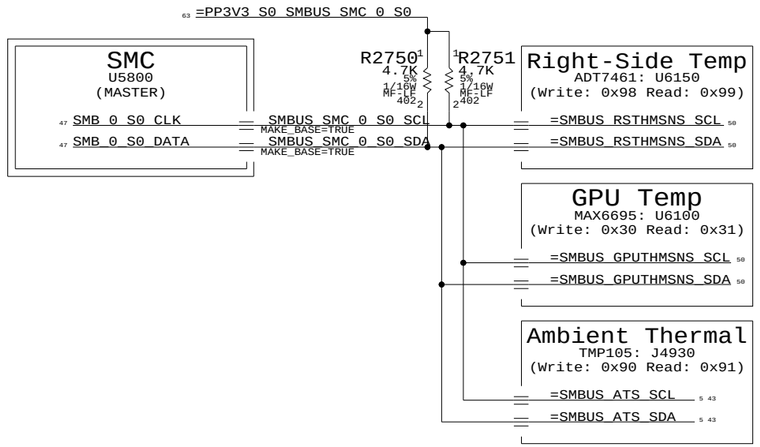
U2 - Keyboard Controller
(Write: 0x72 Read: 0x73)

Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

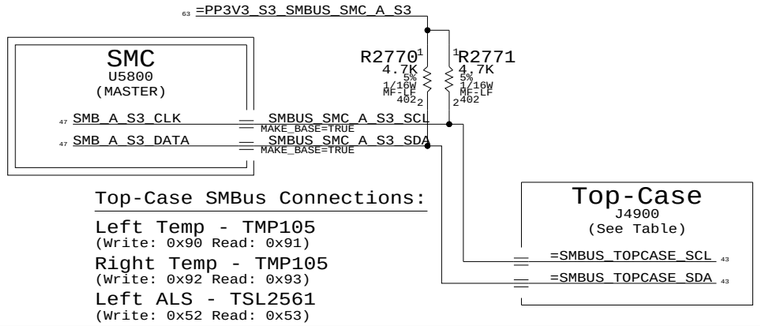
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



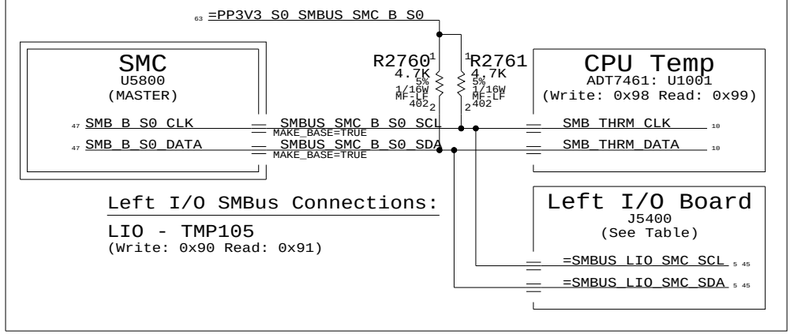
Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

Left ALS - TSL2561
(Write: 0x52 Read: 0x53)

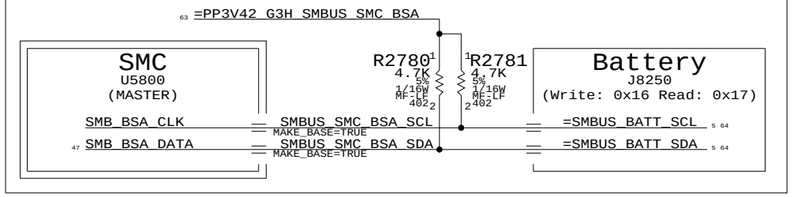
SMC "B" SMBus Connections



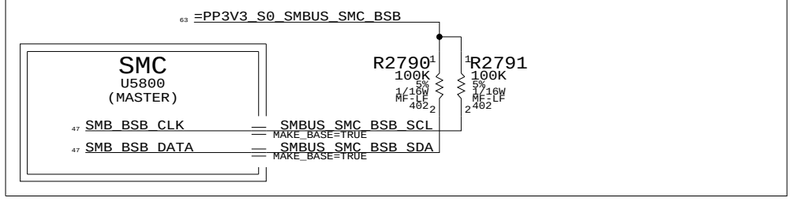
Left I/O SMBus Connections:

LIO - TMP105
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 27 OF 104

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (surface-mount) slot

32 29 MEM_VREF

C2801 2.2uF 20% 6.3V CERM 603

C2800 0.1uF 20% 10V CERM 402

63 29 28 =PP1V8_S3_MEM

203 201 NC

CRITICAL J2800 F-RT-SM

DDR2-SODIMM-DUAL

	1A	VREF	VSS0	2A			
	3A	VSS1	DQ4	4A	MEM_A_DQ<8>		15
15 MEM_A_DQ<14>	5A	DQ0	DQ5	6A	MEM_A_DQ<12>		15
15 MEM_A_DQ<13>	7A	DQ1	VSS2	8A			
	9A	VSS4	DM0	10A	MEM_A_DM<1>		15
15 MEM_A_DQS_N<1>	11A	DQS0*	VSS5	12A			
15 MEM_A_DQS_P<1>	13A	DQS0	DQ6	14A	MEM_A_DQ<15>		15
	15A	VSS6	DQ7	16A	MEM_A_DQ<9>		15
15 MEM_A_DQ<10>	17A	DQ2	VSS7	18A			
15 MEM_A_DQ<11>	19A	DQ3	DQ12	20A	MEM_A_DQ<2>		15
	21A	VSS8	DQ13	22A	MEM_A_DQ<3>		15
15 MEM_A_DQ<5>	23A	DQ8	VSS9	24A			
15 MEM_A_DQ<4>	25A	DQ9	DM1	26A	MEM_A_DM<0>		15
	27A	VSS10	VSS11	28A			
15 MEM_A_DQS_N<0>	29A	DQS1*	CK0	30A	MEM_CLK_P<0>		14
15 MEM_A_DQS_P<0>	31A	DQS1	CK0*	32A	MEM_CLK_N<0>		14
	33A	VSS12	VSS13	34A			
15 MEM_A_DQ<6>	35A	DQ10	DQ14	36A	MEM_A_DQ<1>		15
15 MEM_A_DQ<7>	37A	DQ11	DQ15	38A	MEM_A_DQ<0>		15
	39A	VSS14	VSS15	40A			
		KEY					
	41A	VSS16	VSS17	42A			
15 MEM_A_DQ<19>	43A	DQ16	DQ20	44A	MEM_A_DQ<23>		15
15 MEM_A_DQ<18>	45A	DQ17	DQ21	46A	MEM_A_DQ<22>		15
	47A	VSS18	VSS19	48A			
15 MEM_A_DQS_N<2>	49A	DQS2*	NC0	50A	DIMM_OVERTEMP_L	29	48
15 MEM_A_DQS_P<2>	51A	DQS2	DM2	52A	MEM_A_DM<2>		15
	53A	VSS21	VSS22	54A			
15 MEM_A_DQ<20>	55A	DQ18	DQ22	56A	MEM_A_DQ<21>		15
15 MEM_A_DQ<16>	57A	DQ19	DQ23	58A	MEM_A_DQ<17>		15
	59A	VSS23	VSS24	60A			
15 MEM_A_DQ<28>	61A	DQ24	DQ28	62A	MEM_A_DQ<29>		15
15 MEM_A_DQ<25>	63A	DQ25	DQ29	64A	MEM_A_DQ<24>		15
	65A	VSS25	VSS26	66A			
15 MEM_A_DM<3>	67A	DM3	DQS3*	68A	MEM_A_DQS_N<3>		15
NC	69A	NC1	DQS3	70A	MEM_A_DQS_P<3>		15
	71A	VSS27	VSS28	72A			
15 MEM_A_DQ<27>	73A	DQ26	DQ30	74A	MEM_A_DQ<26>		15
15 MEM_A_DQ<30>	75A	DQ27	DQ31	76A	MEM_A_DQ<31>		15
	77A	VSS29	VSS30	78A			
30 14 MEM_CKE<0>	79A	CKE0	NC/CKE1	80A	MEM_CKE<1>	14	30
	81A	VDD0	VDD1	82A			
NC	83A	NC2	NC/A15	84A	MEM_A_A<15>		6
30 15 MEM_A_BS<2>	85A	BA2	NC/A14	86A	MEM_A_A<14>		6
	87A	VDD2	VDD3	88A			
30 15 MEM_A_A<12>	89A	A12	A11	90A	MEM_A_A<11>	15	30
30 15 MEM_A_A<9>	91A	A9	A7	92A	MEM_A_A<7>	15	30
30 15 MEM_A_A<8>	93A	A8	A6	94A	MEM_A_A<6>	15	30
	95A	VDD4	VDD5	96A			
30 15 MEM_A_A<5>	97A	A5	A4	98A	MEM_A_A<4>	15	30
30 15 MEM_A_A<3>	99A	A3	A2	100A	MEM_A_A<2>	15	30
30 15 MEM_A_A<1>	101A	A1	A0	102A	MEM_A_A<0>	15	30
	103A	VDD6	VDD7	104A			
30 15 MEM_A_A<10>	105A	A10/AP	BA1	106A	MEM_A_BS<1>	15	30
30 15 MEM_A_BS<0>	107A	BA0	RAS*	108A	MEM_A_RAS_L	15	30
30 15 MEM_A_WE_L	109A	WE*	S0*	110A	MEM_CS_L<0>	14	30
	111A	VDD8	VDD9	112A			
30 15 MEM_A_CAS_L	113A	CAS*	ODT0	114A	MEM_ODT<0>	14	30
30 14 MEM_CS_L<1>	115A	NC/S1*	NC/A13	116A	MEM_A_A<13>	15	30
	117A	VDD10	VDD11	118A			
30 14 MEM_ODT<1>	119A	NC/ODT1	NC3	120A	NC		
	121A	VSS31	VSS32	122A			
15 MEM_A_DQ<35>	123A	DQ32	DQ36	124A	MEM_A_DQ<38>		15
15 MEM_A_DQ<39>	125A	DQ33	DQ37	126A	MEM_A_DQ<34>		15
	127A	VSS33	VSS34	128A			
15 MEM_A_DQS_N<4>	129A	DQS4*	DM4	130A	MEM_A_DM<4>		15
15 MEM_A_DQS_P<4>	131A	DQS4	VSS35	132A			
	133A	VSS36	DQ38	134A	MEM_A_DQ<32>		15
15 MEM_A_DQ<37>	135A	DQ34	DQ39	136A	MEM_A_DQ<36>		15
15 MEM_A_DQ<33>	137A	DQ35	VSS37	138A			
	139A	VSS38	DQ44	140A	MEM_A_DQ<57>		15
15 MEM_A_DQ<60>	141A	DQ40	DQ45	142A	MEM_A_DQ<63>		15
15 MEM_A_DQ<59>	143A	DQ41	VSS39	144A			
	145A	VSS40	DQS5*	146A	MEM_A_DQS_N<7>		15
15 MEM_A_DM<7>	147A	DM5	DQS5	148A	MEM_A_DQS_P<7>		15
	149A	VSS41	VSS42	150A			
15 MEM_A_DQ<58>	151A	DQ42	DQ46	152A	MEM_A_DQ<56>		15
15 MEM_A_DQ<61>	153A	DQ43	DQ47	154A	MEM_A_DQ<62>		15
	155A	VSS43	VSS44	156A			
15 MEM_A_DQ<43>	157A	DQ48	DQ52	158A	MEM_A_DQ<40>		15
15 MEM_A_DQ<45>	159A	DQ49	DQ53	160A	MEM_A_DQ<42>		15
	161A	VSS45	VSS46	162A			
NC	163A	NC_TEST	CK1	164A	MEM_CLK_P<1>		14
	165A	VSS47	CK1*	166A	MEM_CLK_N<1>		14
15 MEM_A_DQS_N<5>	167A	DQS6*	VSS48	168A			
15 MEM_A_DQS_P<5>	169A	DQS6	DM6	170A	MEM_A_DM<5>		15
	171A	VSS49	VSS50	172A			
15 MEM_A_DQ<41>	173A	DQ50	DQ54	174A	MEM_A_DQ<47>		15
15 MEM_A_DQ<46>	175A	DQ51	DQ55	176A	MEM_A_DQ<44>		15
	177A	VSS51	VSS52	178A			
15 MEM_A_DQ<51>	179A	DQ56	DQ60	180A	MEM_A_DQ<54>		15
15 MEM_A_DQ<50>	181A	DQ57	DQ61	182A	MEM_A_DQ<55>		15
	183A	VSS53	VSS54	184A			
15 MEM_A_DM<6>	185A	DM7	DQS7*	186A	MEM_A_DQS_N<6>		15
	187A	VSS55	DQS7	188A	MEM_A_DQS_P<6>		15
15 MEM_A_DQ<53>	189A	DQ58	VSS56	190A			
15 MEM_A_DQ<48>	191A	DQ59	DQ62	192A	MEM_A_DQ<52>		15
63 29 =PPSPD_S0_MEM	193A	VSS57	DQ63	194A	MEM_A_DQ<49>		15
			VSS58	196A			
27 =I2C_SODIMMA_SDA	195A	SDA	SA0	198A			
27 =I2C_SODIMMA_SCL	197A	SCL	SA1	200A	ADDR=0xA0(WR)/0xA1(RD)		
	199A	VDDSPD					

202 204 NC

516S0382

63 29 28 =PP1V8_S3_MEM

DDR2 Bypass Caps

(For return current)

63 29 28 =PP1V8_S3_MEM

C2808 10UF 20% 6.3V X5R 603

C2809 10UF 20% 6.3V X5R 603

C2810 0.1uF 20% 10V CERM 402

C2811 0.1uF 20% 10V CERM 402

C2812 0.1uF 20% 10V CERM 402

C2813 0.1uF 20% 10V CERM 402

C2814 0.1uF 20% 10V CERM 402

C2815 0.1uF 20% 10V CERM 402

C2816 0.1uF 20% 10V CERM 402

C2817 0.1uF 20% 10V CERM 402

C2818 0.1uF 20% 10V CERM 402

C2819 0.1uF 20% 10V CERM 402

C2820 0.1uF 20% 10V CERM 402

C2821 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7099 | REV. D

SCALE NONE | SHT 28 OF 104

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (thru-hole) slot

32 28 MEM_VREF

C2901 2.2uF 20% 6.3V CERM 603

C2900 0.1uF 20% 10V CERM 402

63 29 28 =PP1V8_S3_MEM

20 NC

CRITICAL
J2900
F-RT-TH1
DDR2-SODIMM-DUAL

	1B	VREF		2B	VSS0		
	3B	VSS1		4B	DQ4	15	MEM_B_DQ<9>
15	MEM_B_DQ<15>	5B	DQ0	6B	DQ5	15	MEM_B_DQ<11>
15	MEM_B_DQ<14>	7B	DQ1	8B	VSS2		
	9B	VSS4	DM0	10B		15	MEM_B_DM<1>
15	MEM_B_DQS_N<1>	11B	DQS0*	12B	VSS5		
15	MEM_B_DQS_P<1>	13B	DQS0	14B	DQ6	15	MEM_B_DQ<12>
	15B	VSS6	DQ7	16B		15	MEM_B_DQ<8>
15	MEM_B_DQ<10>	17B	DQ2	18B	VSS7		
15	MEM_B_DQ<13>	19B	DQ3	20B	DQ12	15	MEM_B_DQ<3>
	21B	VSS8	DQ13	22B		15	MEM_B_DQ<6>
15	MEM_B_DQ<7>	23B	DQ8	24B	VSS9		
15	MEM_B_DQ<2>	25B	DQ9	26B	DM1	15	MEM_B_DM<0>
	27B	VSS10	VSS11	28B			
15	MEM_B_DQS_N<0>	29B	DQS1*	30B	CK0	14	MEM_CLK_P<3>
15	MEM_B_DQS_P<0>	31B	DQS1	32B	CK0*	14	MEM_CLK_N<3>
	33B	VSS12	VSS13	34B			
15	MEM_B_DQ<1>	35B	DQ10	36B	DQ14	15	MEM_B_DQ<0>
15	MEM_B_DQ<4>	37B	DQ11	38B	DQ15	15	MEM_B_DQ<5>
	39B	VSS14	VSS15	40B			
			KEY				
	41B	VSS16	VSS17	42B			
15	MEM_B_DQ<21>	43B	DQ16	44B	DQ20	15	MEM_B_DQ<22>
15	MEM_B_DQ<19>	45B	DQ17	46B	DQ21	15	MEM_B_DQ<18>
	47B	VSS18	VSS19	48B			
15	MEM_B_DQS_N<2>	49B	DQS2*	50B	NC0	28 48	DIMM_OVERTEMP_L
15	MEM_B_DQS_P<2>	51B	DQS2	52B	DM2	15	MEM_B_DM<2>
	53B	VSS21	VSS22	54B			
15	MEM_B_DQ<20>	55B	DQ18	56B	DQ22	15	MEM_B_DQ<17>
15	MEM_B_DQ<23>	57B	DQ19	58B	DQ23	15	MEM_B_DQ<16>
	59B	VSS23	VSS24	60B			
15	MEM_B_DQ<29>	61B	DQ24	62B	DQ28	15	MEM_B_DQ<26>
15	MEM_B_DQ<24>	63B	DQ25	64B	DQ29	15	MEM_B_DQ<28>
	65B	VSS25	VSS26	66B			
15	MEM_B_DM<3>	67B	DM3	68B	DQS3*	15	MEM_B_DQS_N<3>
NC	69B	NC1	DQS3	70B		15	MEM_B_DQS_P<3>
	71B	VSS27	VSS28	72B			
15	MEM_B_DQ<27>	73B	DQ26	74B	DQ30	15	MEM_B_DQ<31>
15	MEM_B_DQ<25>	75B	DQ27	76B	DQ31	15	MEM_B_DQ<30>
	77B	VSS29	VSS30	78B			
30 14	MEM_CKE<2>	79B	CKE0	80B	NC/CKE1	14 30	MEM_CKE<3>
	81B	VDD0	VDD1	82B			
NC	83B	NC2	NC/A15	84B		6	MEM_B_A<15>
30 15	MEM_B_BS<2>	85B	BA2	86B	NC/A14	6	MEM_B_A<14>
	87B	VDD2	VDD3	88B			
30 15	MEM_B_A<12>	89B	A12	90B	A11	15 30	MEM_B_A<11>
30 15	MEM_B_A<9>	91B	A9	92B	A7	15 30	MEM_B_A<7>
30 15	MEM_B_A<8>	93B	A8	94B	A6	15 30	MEM_B_A<6>
	95B	VDD4	VDD5	96B			
30 15	MEM_B_A<5>	97B	A5	98B	A4	15 30	MEM_B_A<4>
30 15	MEM_B_A<3>	99B	A3	100B	A2	15 30	MEM_B_A<2>
30 15	MEM_B_A<1>	101B	A1	102B	A0	15 30	MEM_B_A<0>
	103B	VDD6	VDD7	104B			
30 15	MEM_B_A<10>	105B	A10/AP	106B	BA1	15 30	MEM_B_BS<1>
30 15	MEM_B_BS<0>	107B	BA0	108B	RAS*	15 30	MEM_B_RAS_L
30 15	MEM_B_WE_L	109B	WE*	110B	S0*	14 30	MEM_CS_L<2>
	111B	VDD8	VDD9	112B			
30 15	MEM_B_CAS_L	113B	CAS*	114B	ODT0	14 30	MEM_ODT<2>
30 14	MEM_CS_L<3>	115B	NC/S1*	116B	NC/A13	15 30	MEM_B_A<13>
	117B	VDD10	VDD11	118B			
30 14	MEM_ODT<3>	119B	NC/ODT1	120B	NC3	NC	
	121B	VSS31	VSS32	122B			
15	MEM_B_DQ<36>	123B	DQ32	124B	DQ36	15	MEM_B_DQ<32>
15	MEM_B_DQ<33>	125B	DQ33	126B	DQ37	15	MEM_B_DQ<37>
	127B	VSS33	VSS34	128B			
15	MEM_B_DQS_N<4>	129B	DQS4*	130B	DM4	15	MEM_B_DM<4>
15	MEM_B_DQS_P<4>	131B	DQS4	132B	VSS35		
	133B	VSS36	DQ38	134B		15	MEM_B_DQ<38>
15	MEM_B_DQ<34>	135B	DQ34	136B	DQ39	15	MEM_B_DQ<39>
15	MEM_B_DQ<35>	137B	DQ35	138B	VSS37		
	139B	VSS38	DQ44	140B		15	MEM_B_DQ<44>
15	MEM_B_DQ<40>	141B	DQ40	142B	DQ45	15	MEM_B_DQ<45>
15	MEM_B_DQ<41>	143B	DQ41	144B	VSS39		
	145B	VSS40	DQS5*	146B		15	MEM_B_DQS_N<5>
15	MEM_B_DM<5>	147B	DM5	148B	DQS5	15	MEM_B_DQS_P<5>
	149B	VSS41	VSS42	150B			
15	MEM_B_DQ<42>	151B	DQ42	152B	DQ46	15	MEM_B_DQ<46>
15	MEM_B_DQ<43>	153B	DQ43	154B	DQ47	15	MEM_B_DQ<47>
	155B	VSS43	VSS44	156B			
15	MEM_B_DQ<62>	157B	DQ48	158B	DQ52	15	MEM_B_DQ<58>
15	MEM_B_DQ<59>	159B	DQ49	160B	DQ53	15	MEM_B_DQ<63>
	161B	VSS45	VSS46	162B			
NC	163B	NC_TEST	CK1	164B		14	MEM_CLK_P<2>
	165B	VSS47	CK1*	166B		14	MEM_CLK_N<2>
15	MEM_B_DQS_N<7>	167B	DQS6*	168B	VSS48		
15	MEM_B_DQS_P<7>	169B	DQS6	170B	DM6	15	MEM_B_DM<7>
	171B	VSS49	VSS50	172B			
15	MEM_B_DQ<60>	173B	DQ50	174B	DQ54	15	MEM_B_DQ<56>
15	MEM_B_DQ<61>	175B	DQ51	176B	DQ55	15	MEM_B_DQ<57>
	177B	VSS51	VSS52	178B			
15	MEM_B_DQ<54>	179B	DQ56	180B	DQ60	15	MEM_B_DQ<55>
15	MEM_B_DQ<51>	181B	DQ57	182B	DQ61	15	MEM_B_DQ<50>
	183B	VSS53	VSS54	184B			
15	MEM_B_DM<6>	185B	DM7	186B	DQS7*	15	MEM_B_DQS_N<6>
	187B	VSS55	DQS7	188B		15	MEM_B_DQS_P<6>
15	MEM_B_DQ<52>	189B	DQ58	190B	VSS56		
15	MEM_B_DQ<49>	191B	DQ59	192B	DQ62	15	MEM_B_DQ<53>
63 29 28	=PPSPD_S0_MEM	193B	VSS57	194B	DQ63	15	MEM_B_DQ<48>
27	=I2C_SODIMMB_SDA	195B	SDA	196B	VSS58		
27	=I2C_SODIMMB_SCL	197B	SCL	198B	SA0		
	199B	VDDSPD	SA1	200B			

516-0140 202 NC

Resistor prevents pwr-gnd short

SODIMM_A_SA1
ADDR=0xA4(WR)/0xA5(RD)

=PPSPD_S0_MEM 28 29 63

R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

63 29 28 =PP1V8_S3_MEM

C2908 10UF 20% 6.3V X5R 603

C2909 10UF 20% 6.3V X5R 603

C2910 0.1uF 20% 10V CERM 402

C2911 0.1uF 20% 10V CERM 402

C2912 0.1uF 20% 10V CERM 402

C2913 0.1uF 20% 10V CERM 402

C2914 0.1uF 20% 10V CERM 402

C2915 0.1uF 20% 10V CERM 402

C2916 0.1uF 20% 10V CERM 402

C2917 0.1uF 20% 10V CERM 402

C2918 0.1uF 20% 10V CERM 402

C2919 0.1uF 20% 10V CERM 402

C2920 0.1uF 20% 10V CERM 402

C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

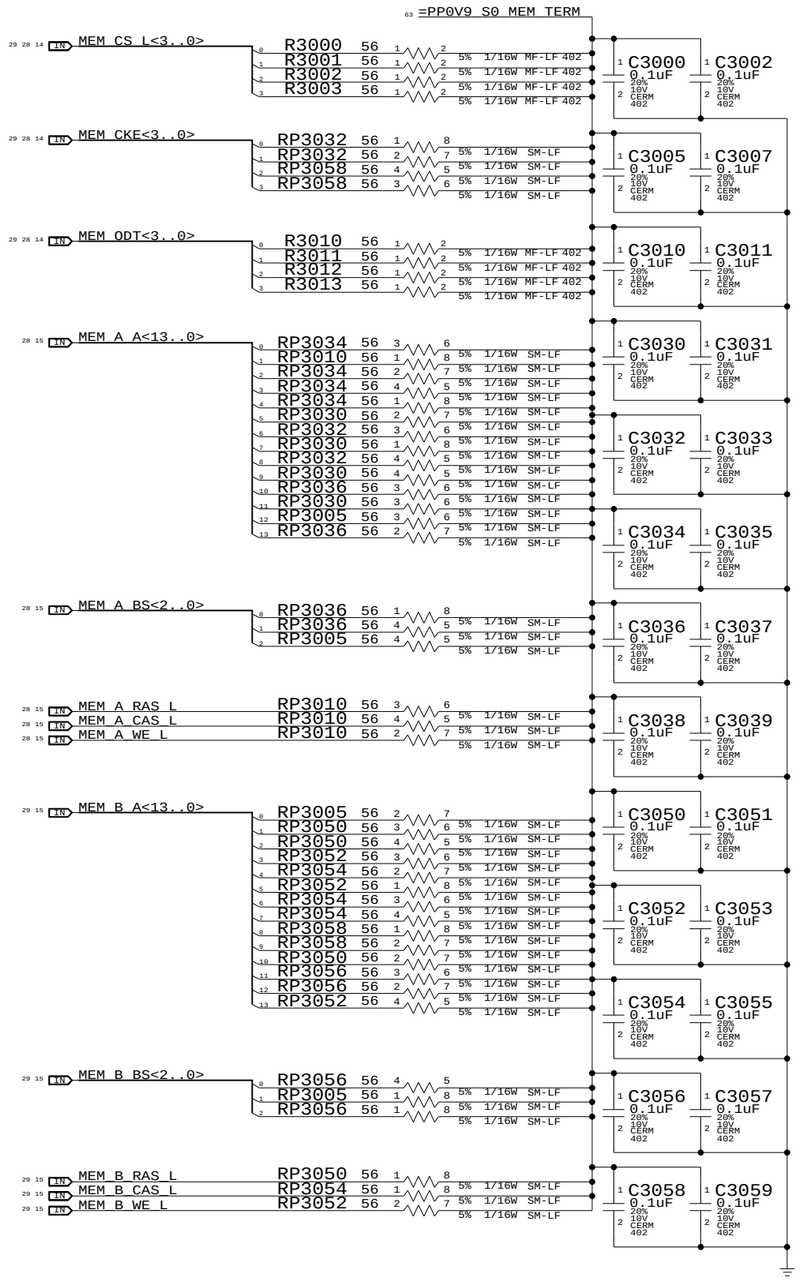
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 29 OF 104	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	30	104

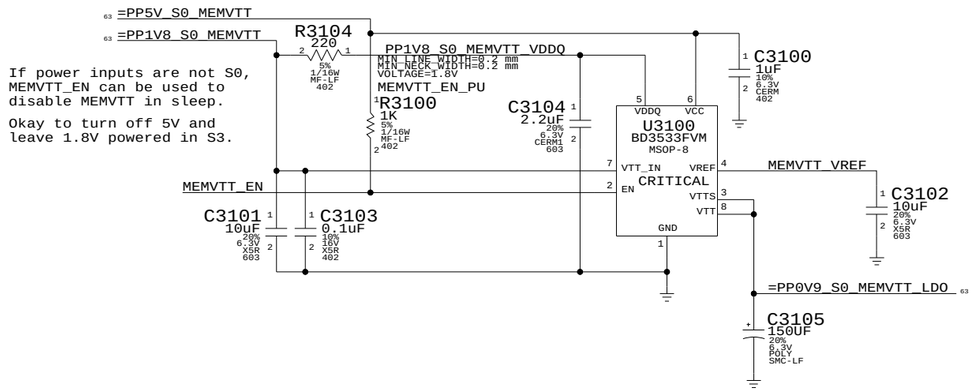
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

Memory Vtt Supply

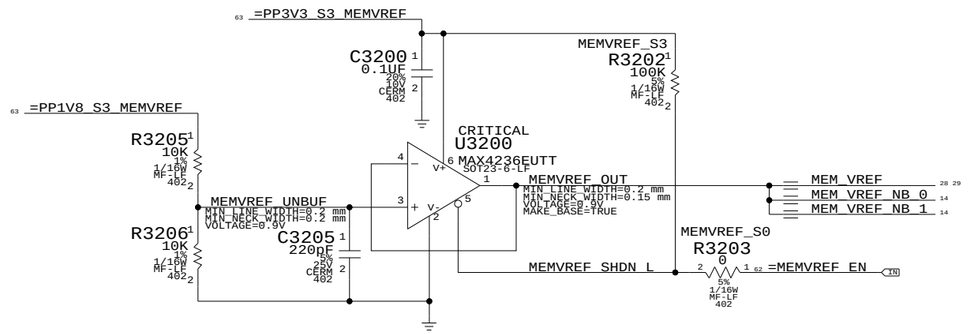
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 31 OF 104



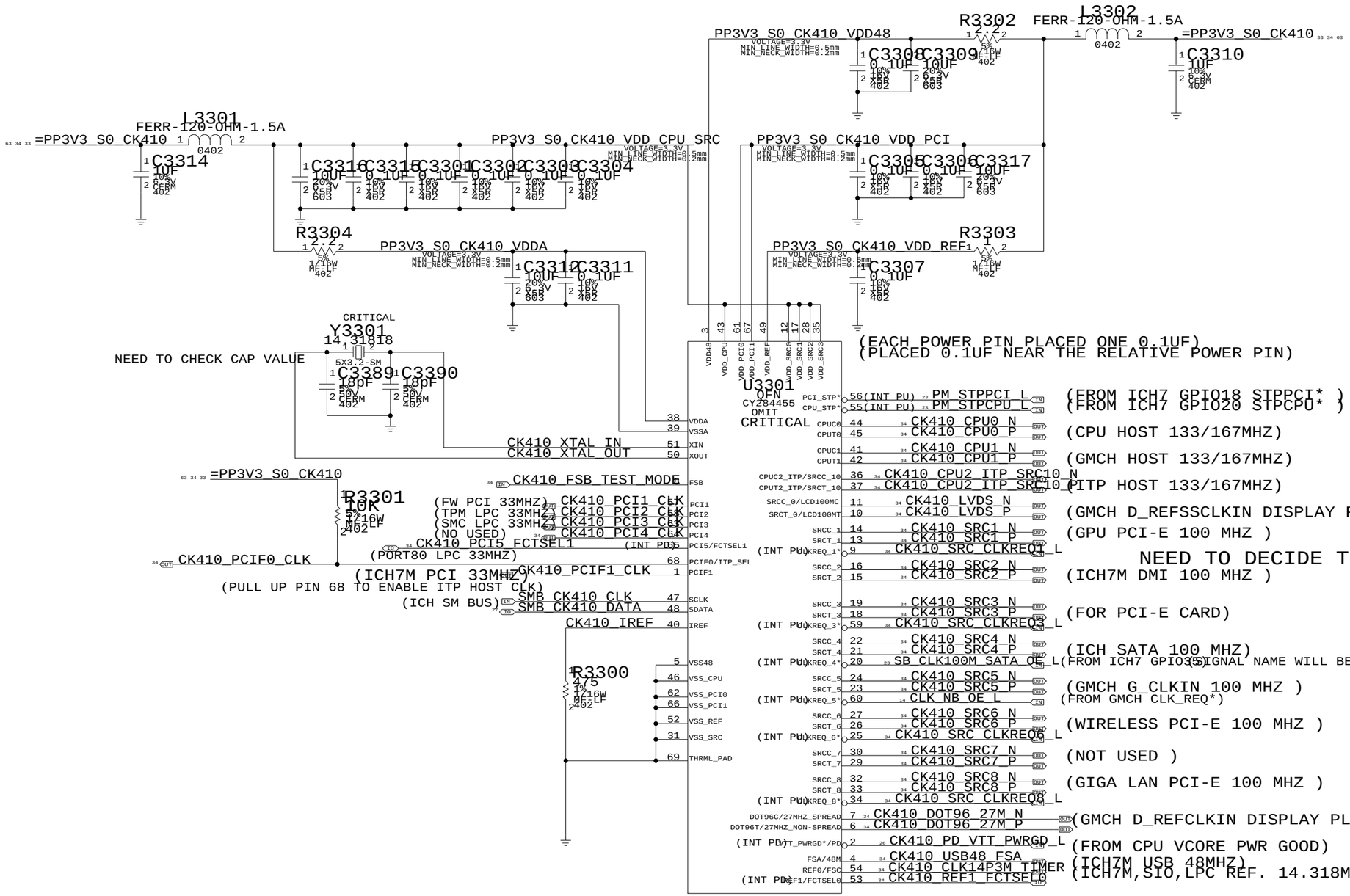
DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	32	104



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	BD	SRCT0	SRCC0	

CLOCKS

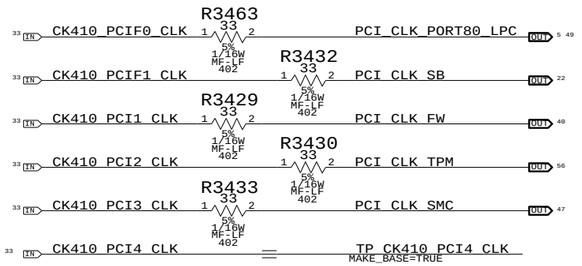
SYNC_MASTER=MAY SYNC_DATE=10/12/2005

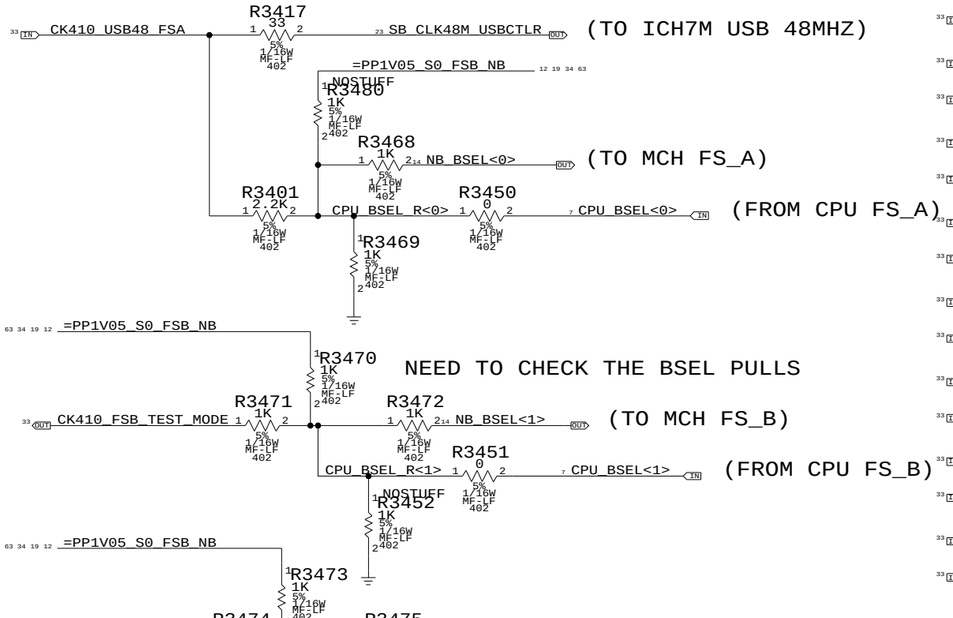
APPLE COMPUTER INC.

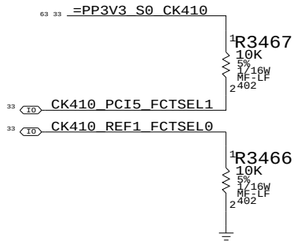
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 33 OF 104



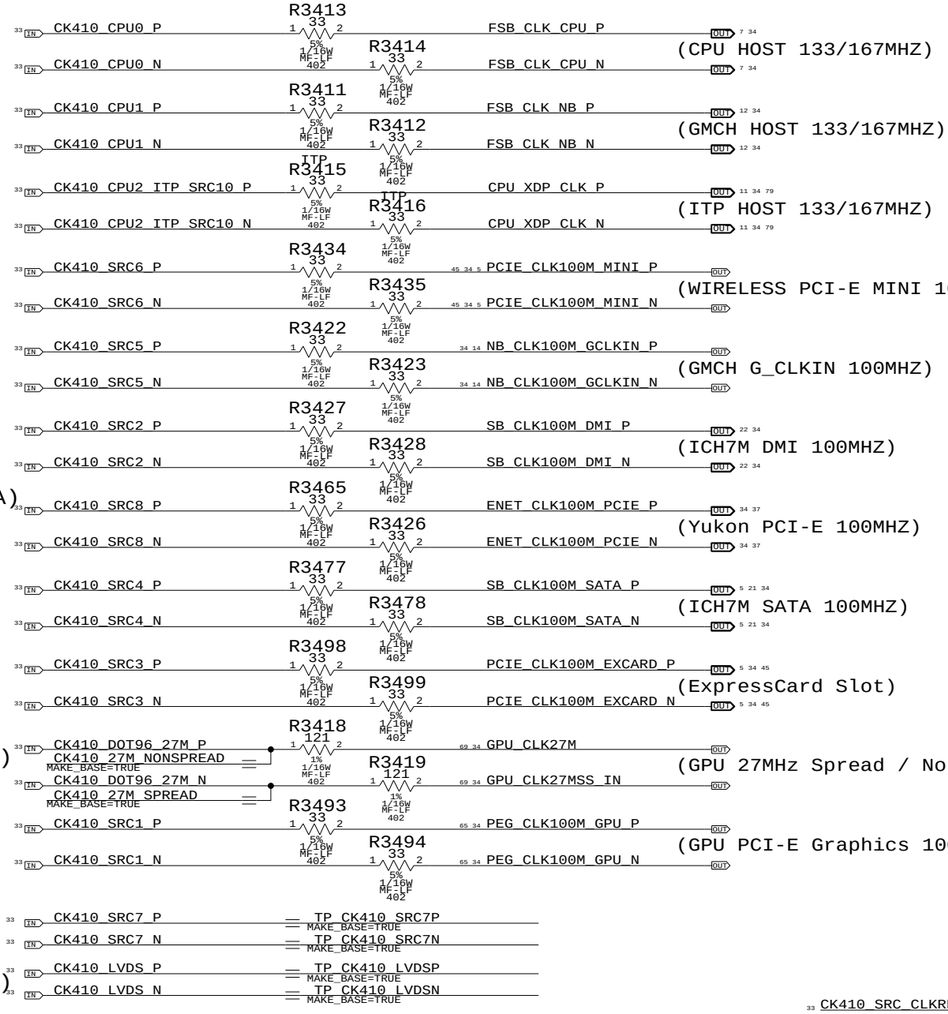


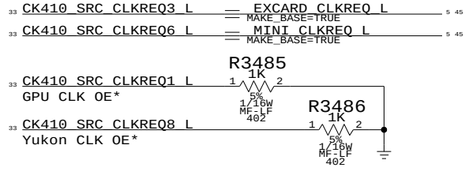


NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED





Clock Termination

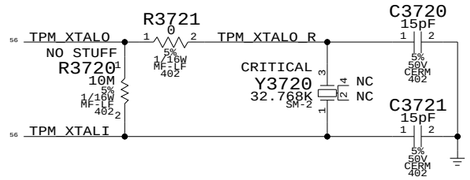
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

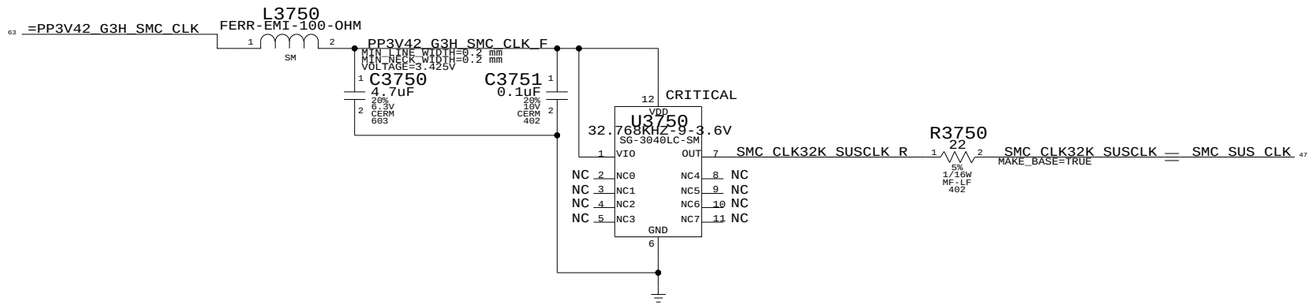
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	34	104

TPM Crystal Circuit



SMC G3Hot Oscillator



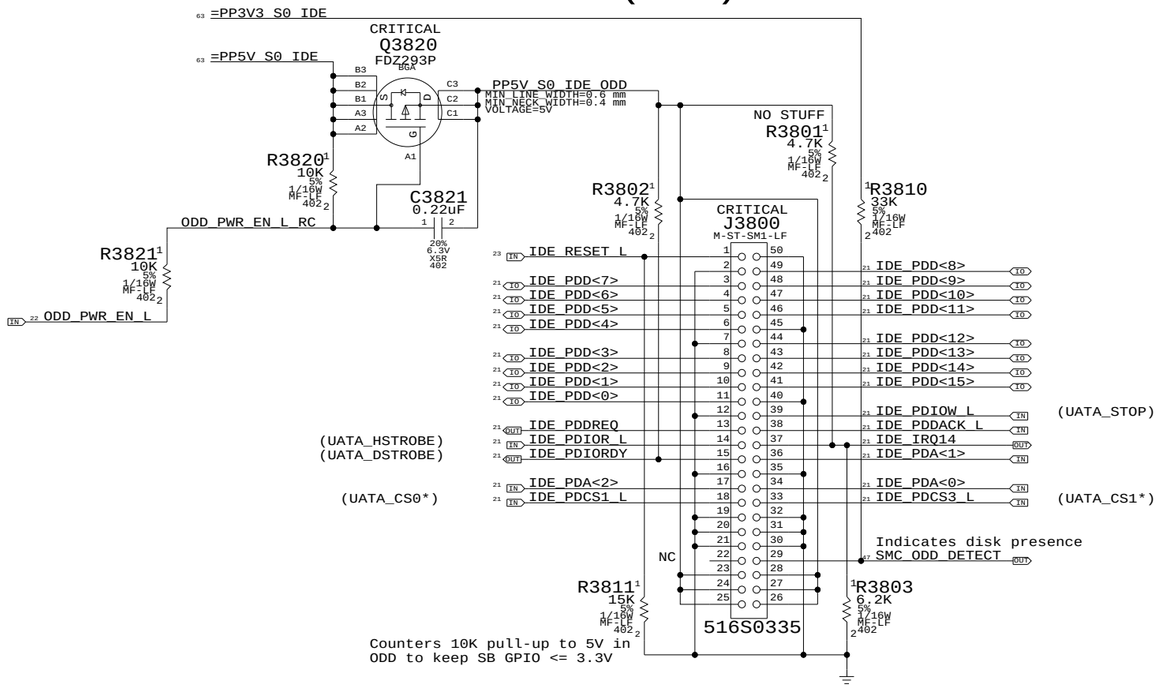
Mobile Clocking

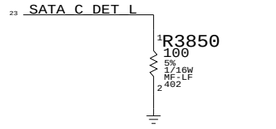
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

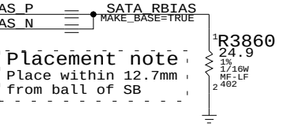
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 37 OF 104	

IDE (ODD) Connector





21 SATA_A_R2D_C_P — TP_SATA_A_R2DP (MAKE_BASE=TRUE)
21 SATA_A_R2D_C_N — TP_SATA_A_R2DN (MAKE_BASE=TRUE)
21 SATA_A_D2R_P — TP_SATA_A_D2RP (MAKE_BASE=TRUE)
21 SATA_A_D2R_N — TP_SATA_A_D2RN (MAKE_BASE=TRUE)



PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 38 OF 104	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01 MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

=PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402

=PP2V5_S3_ENET

PLACE C4107 NEAR U4101 AVDD

=PP3V3_S3_ENET
=PP1V2_S3_ENET
=PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
PCIE_A_D2R_P
PCIE_A_D2R_N
PCIE_A_R2D_P
PCIE_A_R2D_N
PCIE_A_R2D_C_P
PCIE_A_R2D_C_N

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

C4113 0.1UF 10% 16V X5R 402

ENET_CLK100M_PCIE_P
ENET_CLK100M_PCIE_N
PCIE_WAKE_L
ENET_RST_L

OMIT
CRITICAL
U4101
88E8053
QFN

OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED

ANALOG
PCI EXPRESS
LED
MEDIA
TEST
TWSI
SPI
MAIN CLK

ENET_LOM_DISABLE*
VAUX_AVLBL
VMAIN_AVLBL
SWITCH_VCC
SWITCH_VAUX
HSDACP
HSDACN
CTRL25
CTRL12
RSET
LED_ACT*
LED_LINK10/100*
LED_LINK1000*
LINK*
TSTPT
TESTMODE
VPD_CLK
VPD_DATA
PU_VDDO_TTL0
PU_VDDO_TTL1
SPI_DI
SPI_DO
SPI_CLK
SPI_CS
XTALI
XTALO
THRML_PAD

ENET_CTRL25
ENET_CTRL12
ENET_RSET

R4102 4.87K 1% 1/16W MF-LF 402

ENET_VPD_CLK
ENET_VPD_DATA
ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

ASF IS UNAVAILABLE ON 8053

INTERNAL PULL-UP

CRITICAL
ENET_XTALI
ENET_XTALO

Y4101 SM-3.2X2.5MM 25.0000M
C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0
ENET_MDI1
ENET_MDI2
ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

ENET_PU_VDD_TTL0
ENET_PU_VDD_TTL1

=PP3V3_S3_ENET

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL

U4102 M24C08 SO8
VCC E2 NC1 NC0 WC* VSS SDA SCL

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

ENET_VPD_DATA
ENET_VPD_CLK

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

=PP3V3_S3_ENET

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=10/12/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE SHT 41 OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

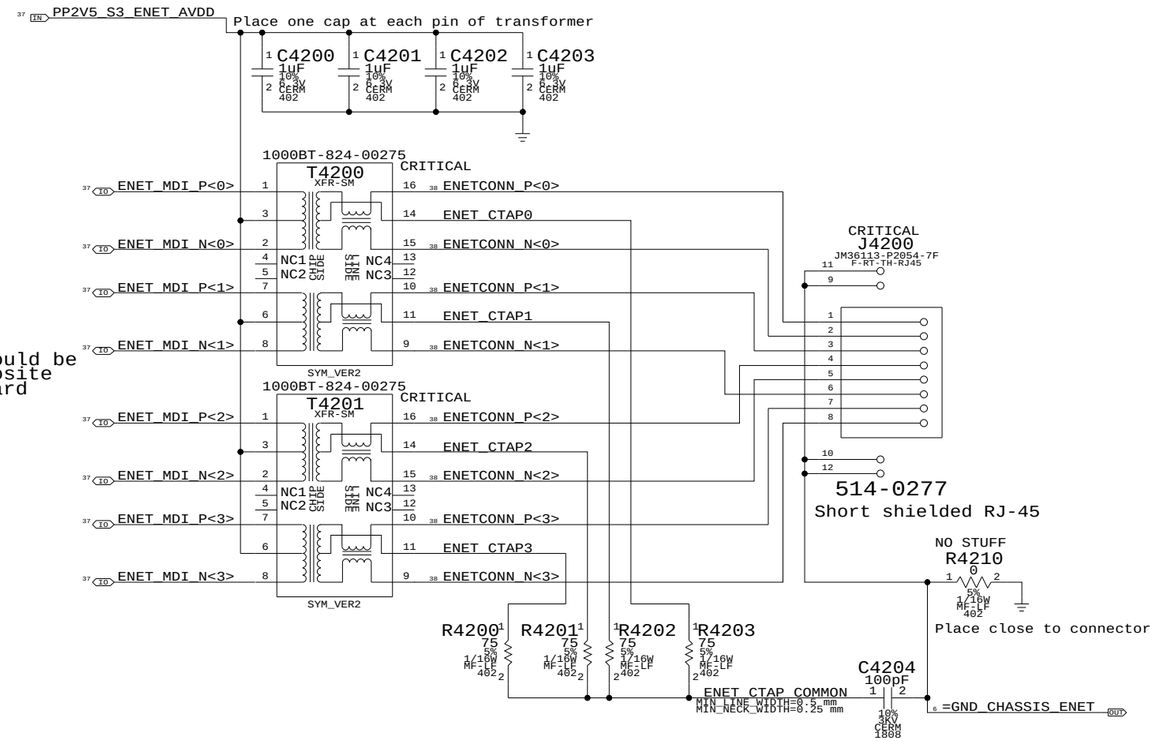
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

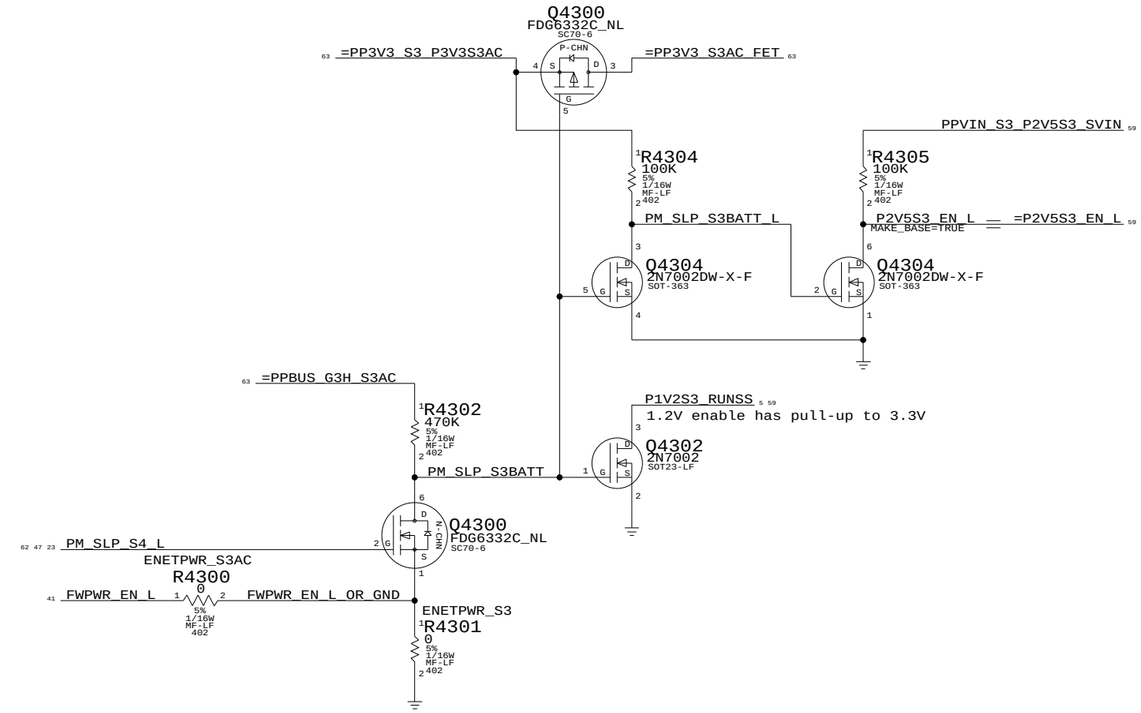
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 42 OF 104	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	3.3V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN_L	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	0V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	Hi-Z (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 43 OF 104

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23256 ADDED
6/21/2005 - CHANGED INT*_IO_INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IO TO ADIO (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT 10 REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST# AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW DIFF_PAIR_NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

0.001A DURING SLEEP

=PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 20% 16V CERM 402
C4422 0.1UF 20% 16V CERM 402
C4426 0.1UF 20% 16V CERM 402
C4428 0.1UF 20% 16V CERM 402
C4430 0.1UF 20% 16V CERM 402
C4432 0.1UF 20% 16V CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 16V X5R 402
C4429 0.1UF 10% 16V X5R 402
C4425 0.1UF 10% 16V X5R 402

=PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

GND_FW_VSSA
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

=PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

CRITICAL
U4400
FW32306
BGA
OMIT

PCI_AD<0>	F10	PCI_AD0
PCI_AD<1>	G10	PCI_AD1
PCI_AD<2>	H10	PCI_AD2
PCI_AD<3>	H12	PCI_AD3
PCI_AD<4>	J13	PCI_AD4
PCI_AD<5>	J12	PCI_AD5
PCI_AD<6>	K13	PCI_AD6
PCI_AD<7>	K10	PCI_AD7
PCI_AD<8>	L12	PCI_AD8
PCI_AD<9>	M13	PCI_AD9
PCI_AD<10>	L11	PCI_AD10
PCI_AD<11>	M12	PCI_AD11
PCI_AD<12>	M11	PCI_AD12
PCI_AD<13>	N12	PCI_AD13
PCI_AD<14>	M10	PCI_AD14
PCI_AD<15>	N11	PCI_AD15
PCI_AD<16>	M4	PCI_AD16
PCI_AD<17>	N5	PCI_AD17
PCI_AD<18>	N4	PCI_AD18
PCI_AD<19>	M3	PCI_AD19
PCI_AD<20>	M2	PCI_AD20
PCI_AD<21>	N3	PCI_AD21
PCI_AD<22>	K4	PCI_AD22
PCI_AD<23>	M1	PCI_AD23
PCI_AD<24>	K2	PCI_AD24
PCI_AD<25>	J4	PCI_AD25
PCI_AD<26>	K1	PCI_AD26
PCI_AD<27>	J2	PCI_AD27
PCI_AD<28>	J1	PCI_AD28
PCI_AD<29>	H2	PCI_AD29
PCI_AD<30>	H4	PCI_AD30
PCI_AD<31>	H1	PCI_AD31
PCI_C_BE_L<0>	K12	PCI_CBE0*
PCI_C_BE_L<1>	M9	PCI_CBE1*
PCI_C_BE_L<2>	L3	PCI_CBE2*
PCI_C_BE_L<3>	L1	PCI_CBE3*
PCI_PAR	N10	PCI_PAR
PCI_FRAME_L	N6	PCI_FRAME*
PCI_IRDY_L	M6	PCI_IRDY*
PCI_TRDY_L	N7	PCI_TRDY*
PCI_DEVSEL_L	N8	PCI_DEVSEL*
PCI_STOP_L	M7	PCI_STOP*
FW_PCI_IDSEL	L2	PCI_IDSEL
PCI_REQ3_L	E2	PCI_REQ*
PCI_GNT3_L	E1	PCI_GNT*
PCI_PERR_L	M8	PCI_PERR*
PCI_SERR_L	N9	PCI_SERR*
PCI_CLK_FW	G2	PCI_CLK
PM_CLKRUN_L	D1	CLKRUN*
FW_PCI_RST_L	F1	PCI_RST*
INT_PIRQD_L	D2	PCI_INTA*
PCI_PME_FW_L	F2	PCI_PME*

R4431 22 5% 1/16W MF-LF 402

R4432 100 5% 1/16W MF-LF 402
THIS IS FROM ICH-7M

197S0178 3.2MMX2.5MM CRITICAL
Y4403 SM-3.2X2.5MM 24.576MHZ

R4400 300 5% 1/16W MF-LF 402
C4411 22PF 5% 50V CERM 402
C4412 22PF 5% 50V CERM 402
NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5	FW_XI
XO	B5	FW_XO
RESET*	B4	FW_PWRON_RST_L
R1	A6	FW_R1
R0	B7	FW_R0

SPEC RECOMMENDS 2.49K

R4452 2.49K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 16V X5R 402
R4420 510K 5% 1/16W MF-LF 402

TPBIAS0	B8	FW_A_TPBIAS
TPA0_P	A9	FW_A_TPA_P
TPA0_N	B9	FW_A_TPA_N
TPB0_P	B10	FW_A_TPB_P
TPB0_N	A10	FW_A_TPB_N
TPBIAS1	D8	FW_B_TPBIAS
TPA1_P	A11	FW_B_TPA_P
TPA1_N	B11	FW_B_TPA_N
TPB1_P	B12	FW_B_TPB_P
TPB1_N	A12	FW_B_TPB_N
TPBIAS2	C13	FW_C_TPBIAS
TPA2_P	C11	FW_C_TPA_P
TPA2_N	C12	FW_C_TPA_N
TPB2_P	D13	FW_C_TPB_P
TPB2_N	D12	FW_C_TPB_N

MODE_420	M5	MODE FOR EXTERNAL LINK
MODE_A	B6	
PC0	E12	FW_PC0
PC1	F13	DUAL PORT DEVICES ARE POWER CLASS 4 (’100’)
PC2	F12	SINGLE PORT DEVICES ARE POWER CLASS 0 (’000’)
CONTENDER	G12	LOW = NOT BUS MANAGER
CARDBUSN	B1	LOW = PCI OPERATION
MPCI_ACTN_323	E10	

MANUFACTURING TEST PINS

TEST0	C2	
TEST1	C1	
TMEST	A4	
SE	A3	
SM	B3	

XW4400 SM

GND_FW_VSSA

FIREWIRE CONTROLLER

SYNC_MASTER=(M42) SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 44 OF 104	

Page Notes

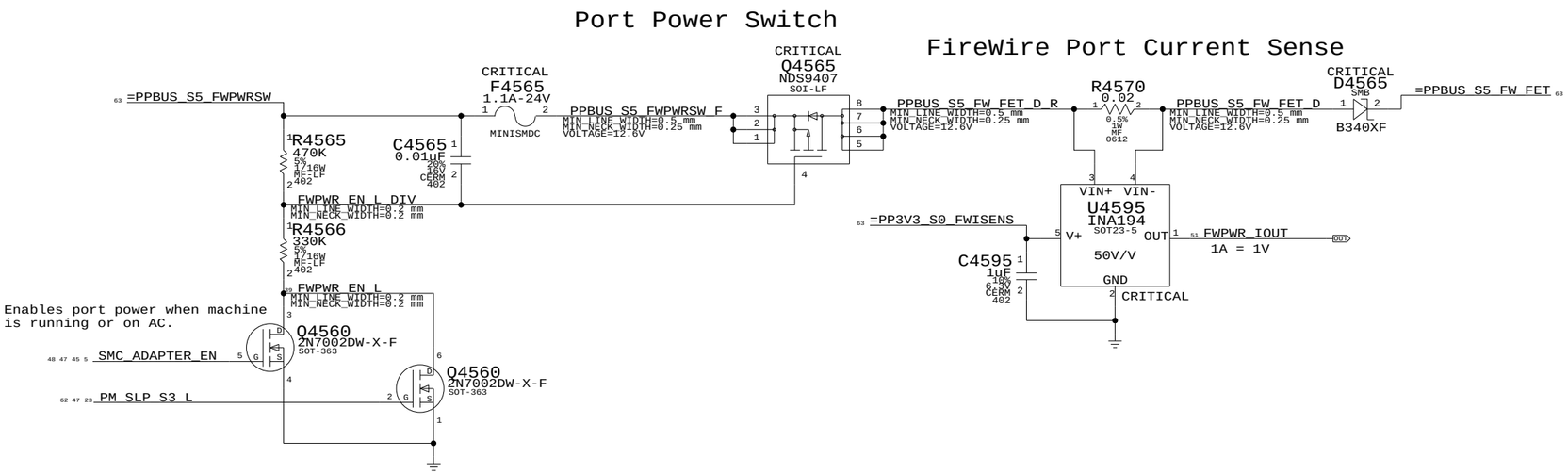
Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch

FireWire Port Current Sense



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 45 OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 42
	FW	FW_110D	FW_PORT1_TPA_FL_N 42
	FW	FW_110D	FW_PORT1_TPB_FL_P 42
	FW	FW_110D	FW_PORT1_TPB_FL_N 42

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

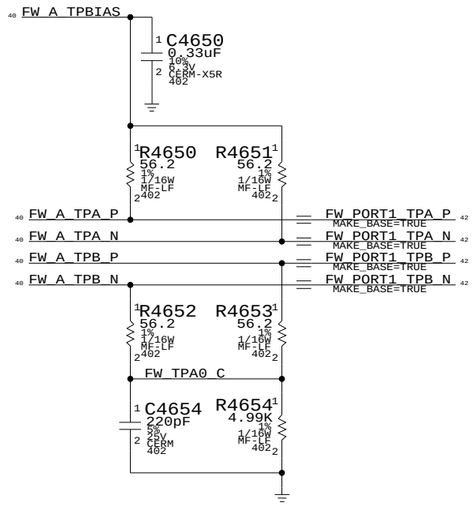
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

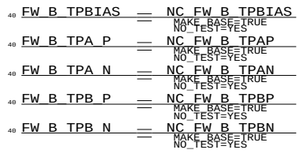
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

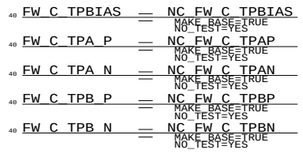
Place close to FireWire PHY



2nd TPA/TPB pair unused

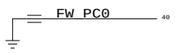


3rd TPA/TPB pair unused

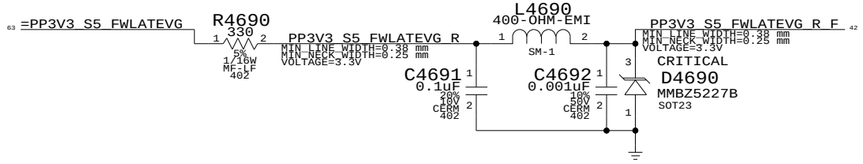


FW Power Class Strap

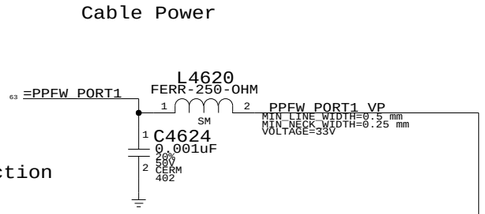
Single-port system sets PC=0



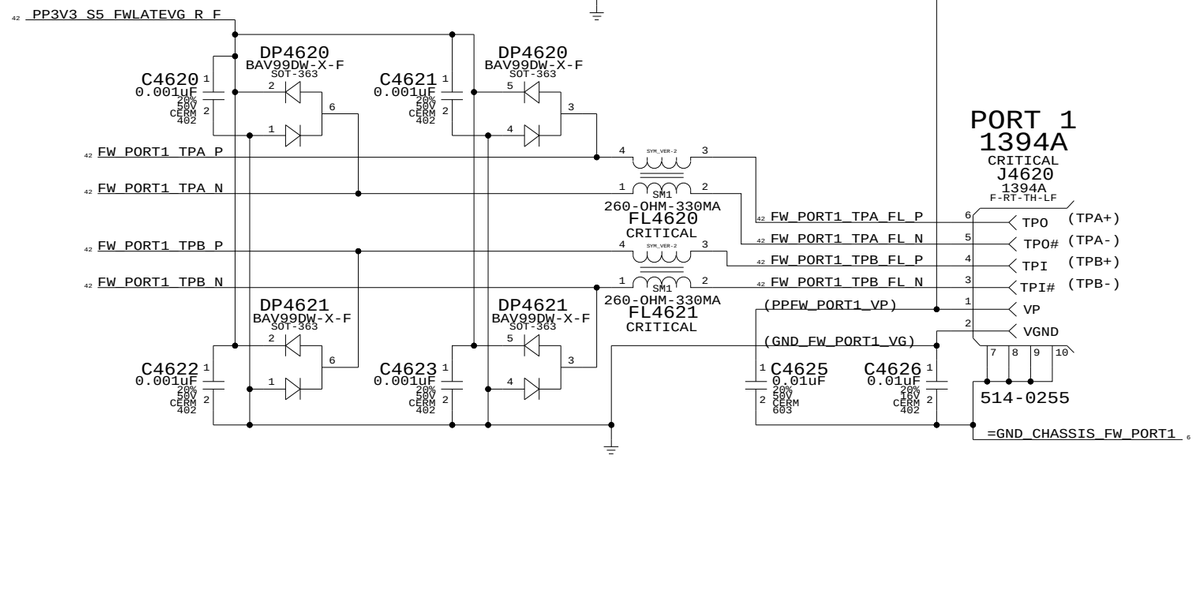
Late-VG Protection Power

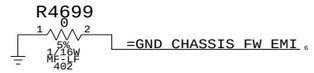


Cable Power



"Snapback" & "Late VG" Protection





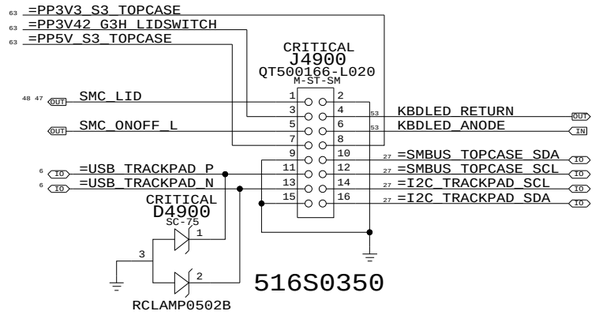
FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 46 OF 104	

Top-Case Connector



Camera Connector

Internal USB Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

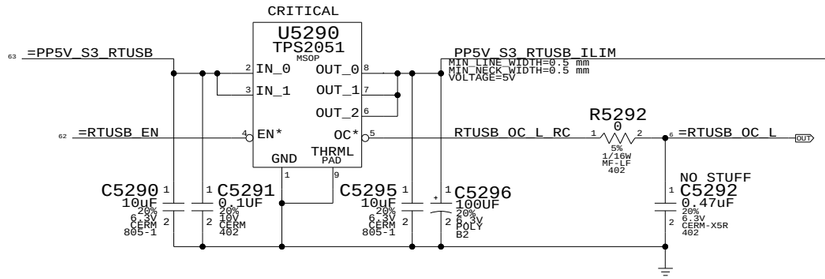
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

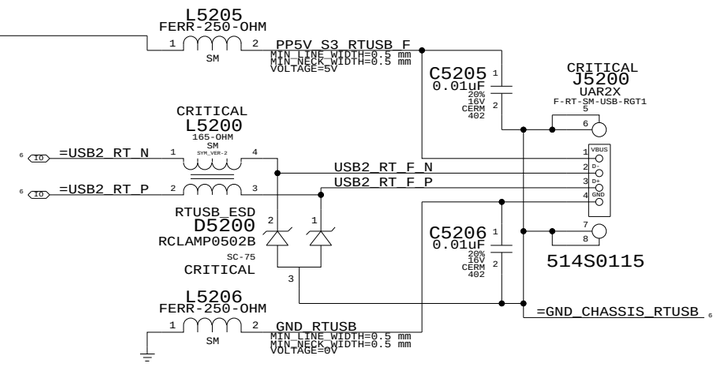
SCALE: NONE

SHT 49 OF 104

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

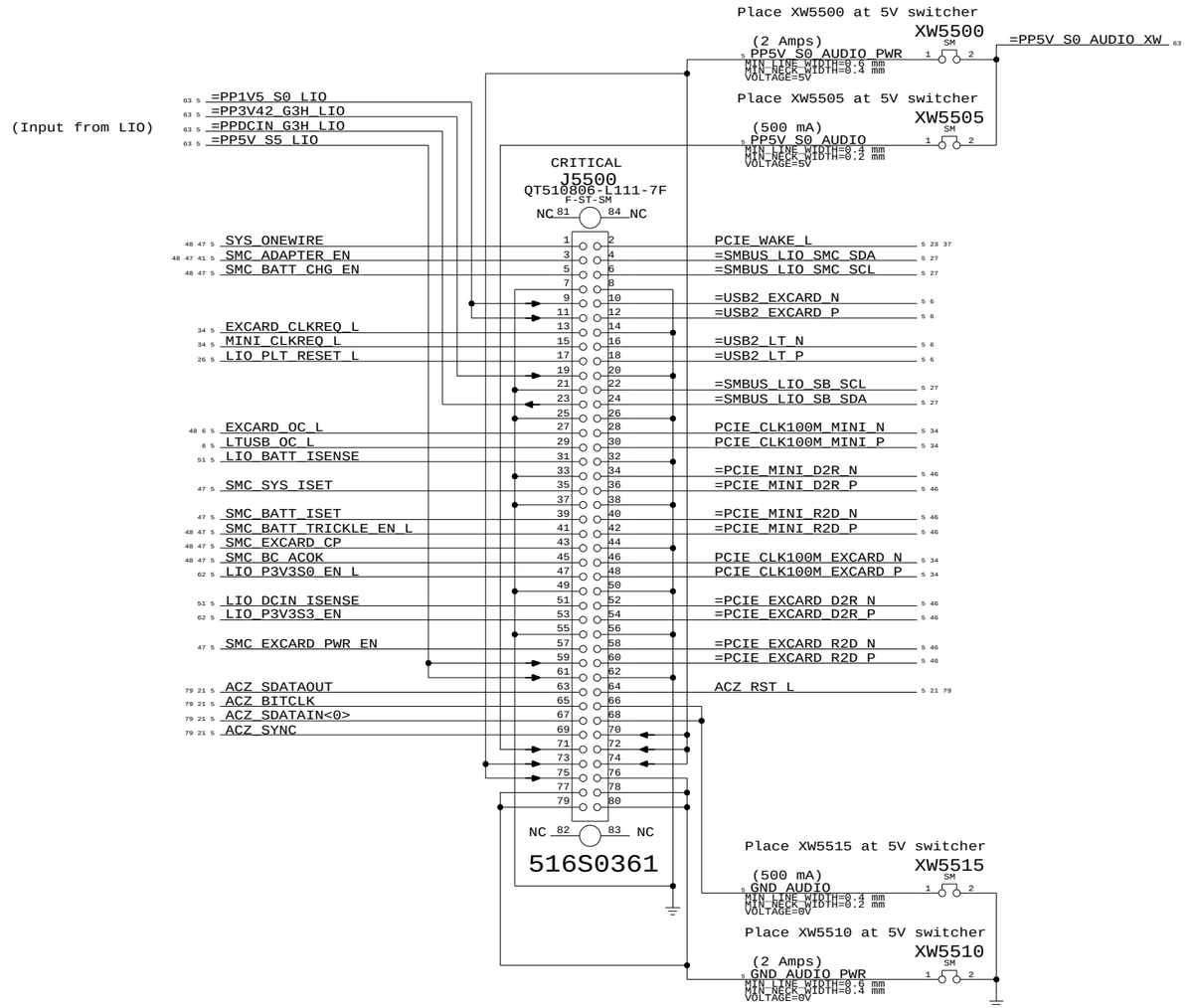
External USB Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 52 OF 104	

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE

SHT 55 OF 104

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

45 5	=PCIE_MINI_R2D_P	PCIE_MINI_R2D_C_P (MAKE_BASE=TRUE)	PCIE_B_R2D_C_P	22
45 5	=PCIE_MINI_R2D_N	PCIE_MINI_R2D_C_N (MAKE_BASE=TRUE)	PCIE_B_R2D_C_N	22
45 5	=PCIE_MINI_D2R_P	PCIE_MINI_D2R_P (MAKE_BASE=TRUE)	PCIE_B_D2R_P	22
45 5	=PCIE_MINI_D2R_N	PCIE_MINI_D2R_N (MAKE_BASE=TRUE)	PCIE_B_D2R_N	22

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

45 5	=PCIE_EXCARD_R2D_P	PCIE_EXCARD_R2D_C_P (MAKE_BASE=TRUE)	PCIE_C_R2D_C_P	22
45 5	=PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_C_N (MAKE_BASE=TRUE)	PCIE_C_R2D_C_N	22
45 5	=PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P (MAKE_BASE=TRUE)	PCIE_C_D2R_P	22
45 5	=PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N (MAKE_BASE=TRUE)	PCIE_C_D2R_N	22

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP (MAKE_BASE=TRUE)		PCIE_D_R2D_C_P 22
TP_PCIE_D_R2DN (MAKE_BASE=TRUE)		PCIE_D_R2D_C_N 22
TP_PCIE_D_D2RP (MAKE_BASE=TRUE)		PCIE_D_D2R_P 22
TP_PCIE_D_D2RN (MAKE_BASE=TRUE)		PCIE_D_D2R_N 22

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP (MAKE_BASE=TRUE)		PCIE_E_R2D_C_P 22
TP_PCIE_E_R2DN (MAKE_BASE=TRUE)		PCIE_E_R2D_C_N 22
TP_PCIE_E_D2RP (MAKE_BASE=TRUE)		PCIE_E_D2R_P 22
TP_PCIE_E_D2RN (MAKE_BASE=TRUE)		PCIE_E_D2R_N 22

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP (MAKE_BASE=TRUE)		PCIE_F_R2D_C_P 22
TP_PCIE_F_R2DN (MAKE_BASE=TRUE)		PCIE_F_R2D_C_N 22
TP_PCIE_F_D2RP (MAKE_BASE=TRUE)		PCIE_F_D2R_P 22
TP_PCIE_F_D2RN (MAKE_BASE=TRUE)		PCIE_F_D2R_N 22

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

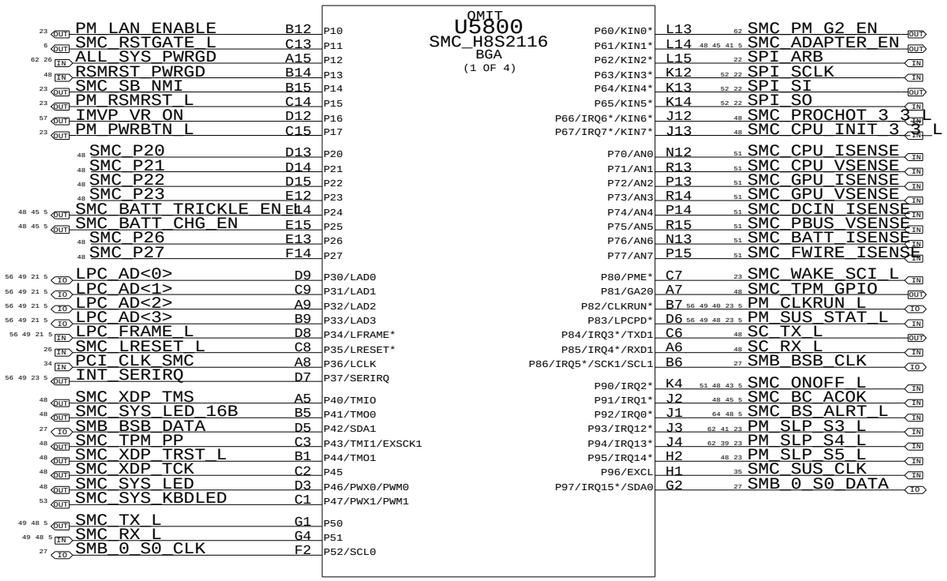
APPLE COMPUTER INC.

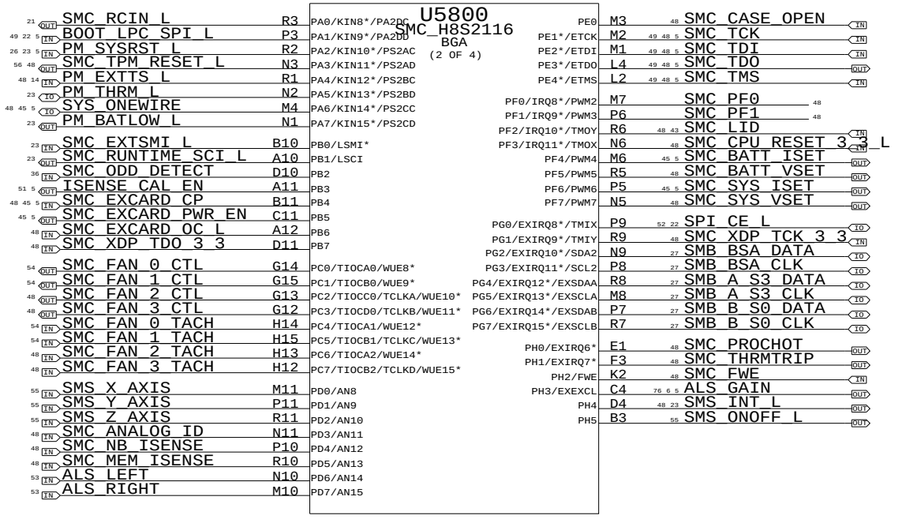
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

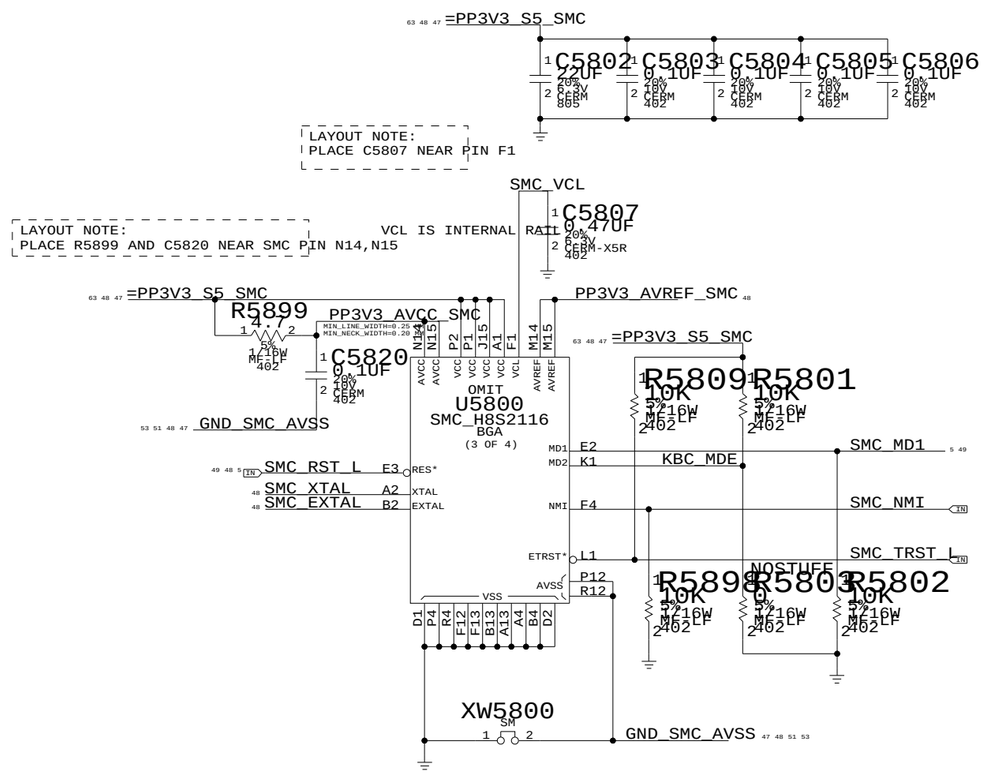
SCALE NONE

SHT 57 OF 104

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.







SMC

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APPLE COMPUTER INC.

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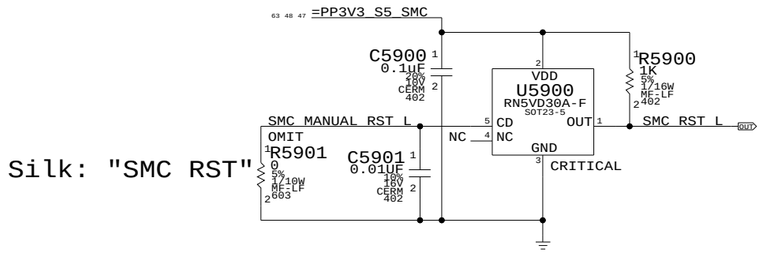
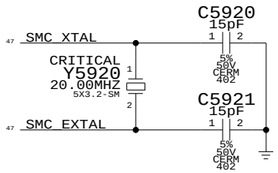
D	051-7099	D
SCALE: NONE	SHT 58 OF 104	

SMC Reset Button / Brownout Detect

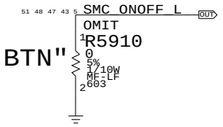


Silk: "SMC RST"

SMC Crystal Circuit

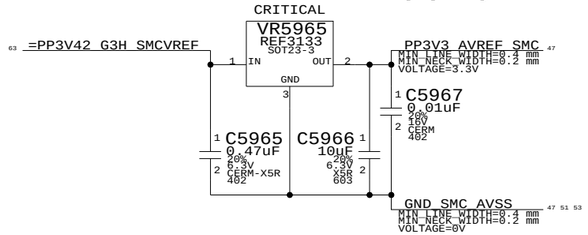


Debug Power Button

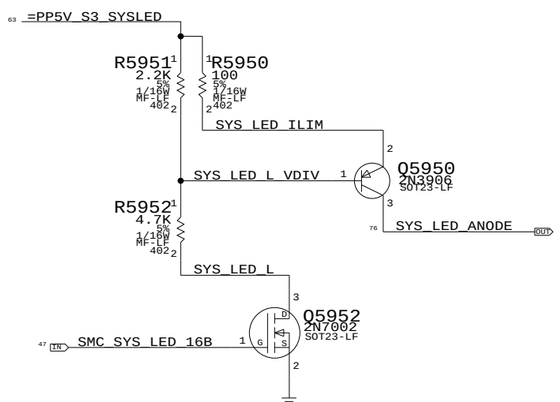


Silk: "PWR BTN"

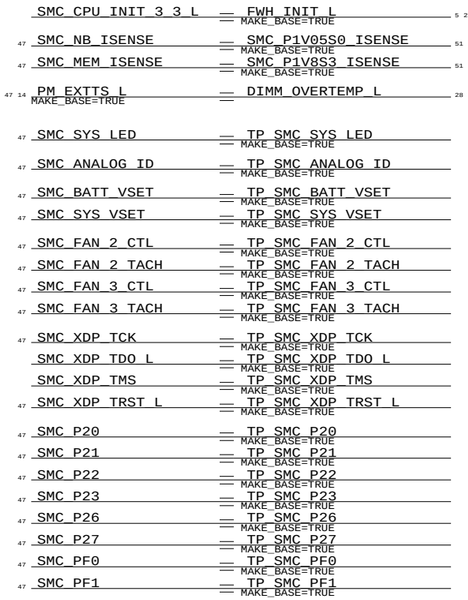
SMC AVREF Supply



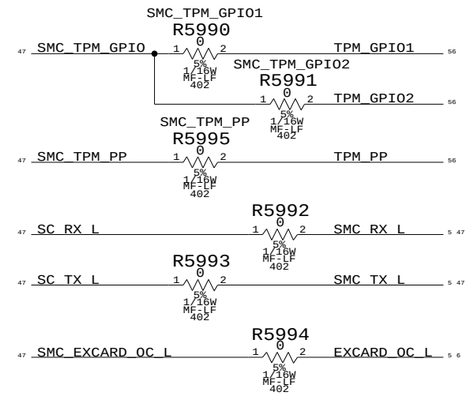
System (Sleep) LED Circuit



SMC_CPU_INIT_3_3_L

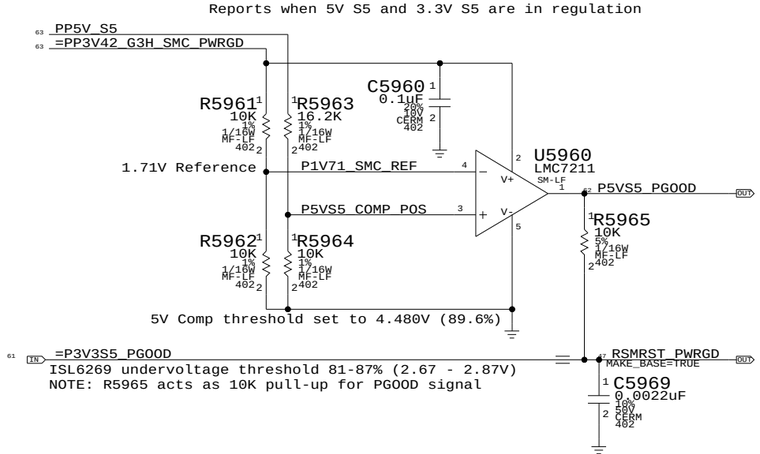


SMC_TPM_GPIO1

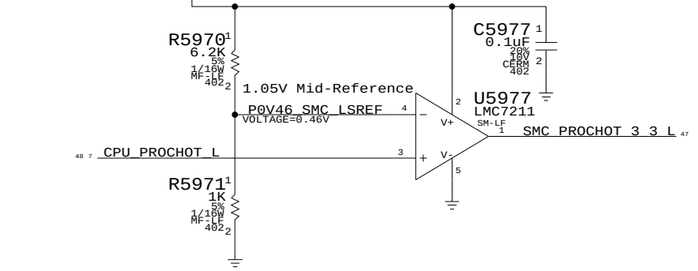


SMC PWRGD Circuit

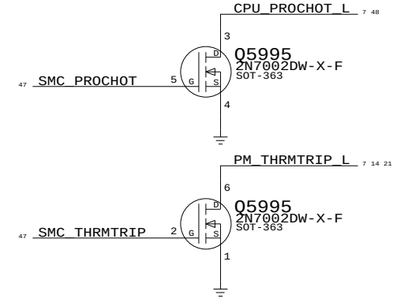
Reports when 5V S5 and 3.3V S5 are in regulation



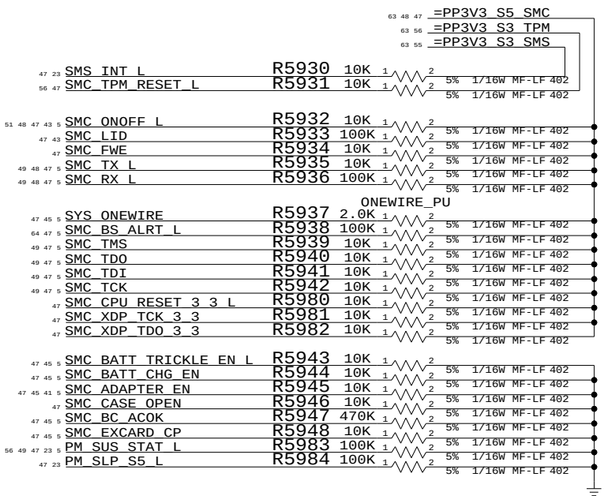
SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



SMC_ONOFF_L



SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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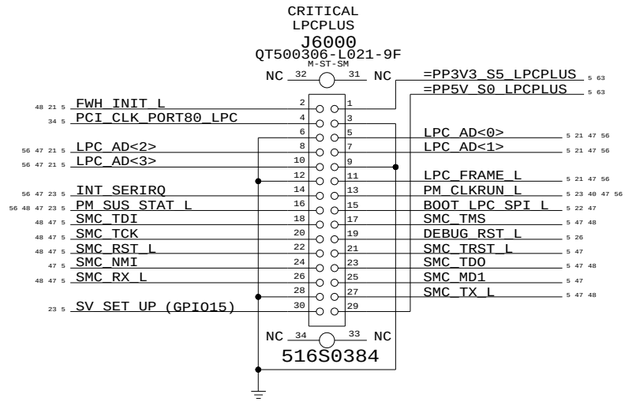
D	051-7099	D
SCALE: NONE	SHT 59 OF 104	



LPC+ Debug Connector

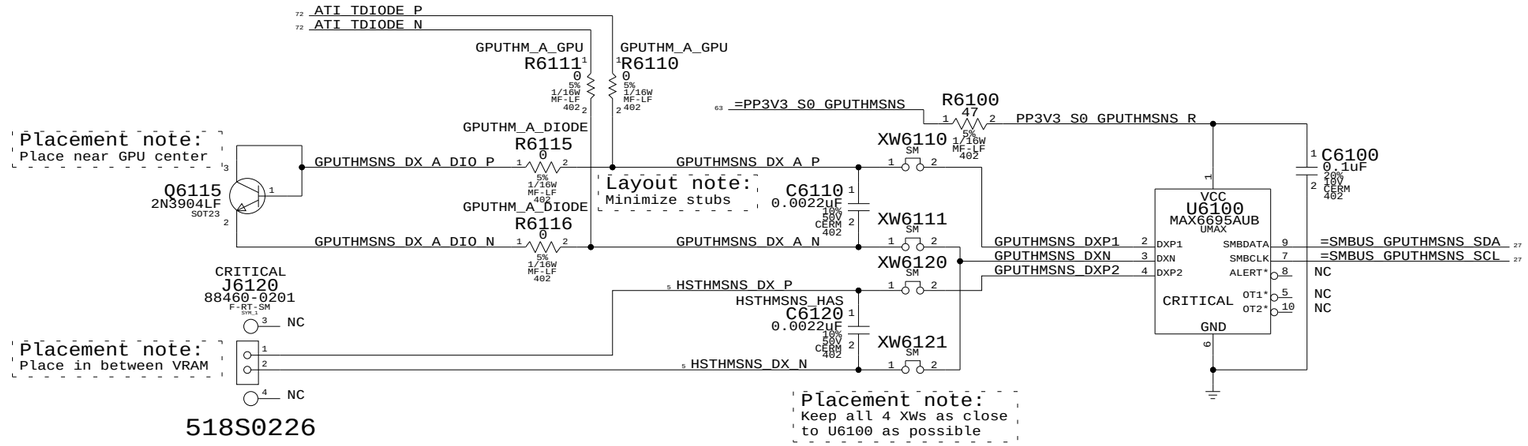
SYNC_MASTER=M42 SYNC_DATE=07/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

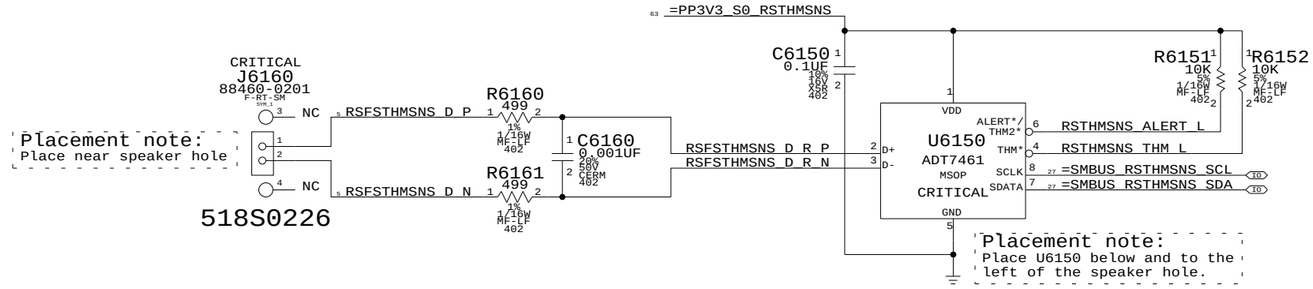
SCALE	SHT	OF
NONE	60	104

GPU / Heat Pipe Thermal Sensor

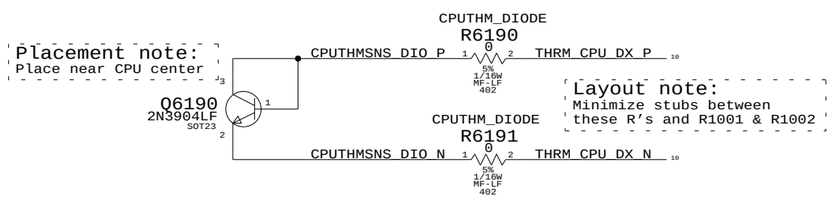


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

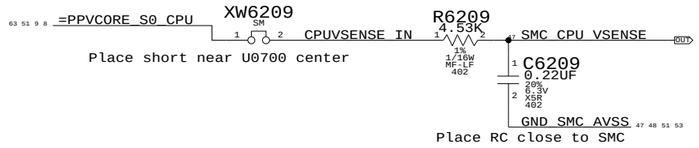
Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

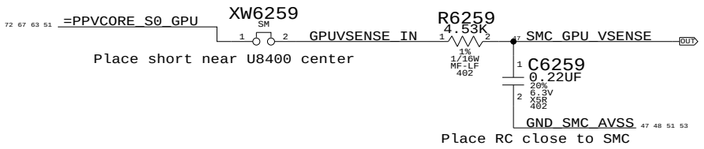
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 61 OF 104	

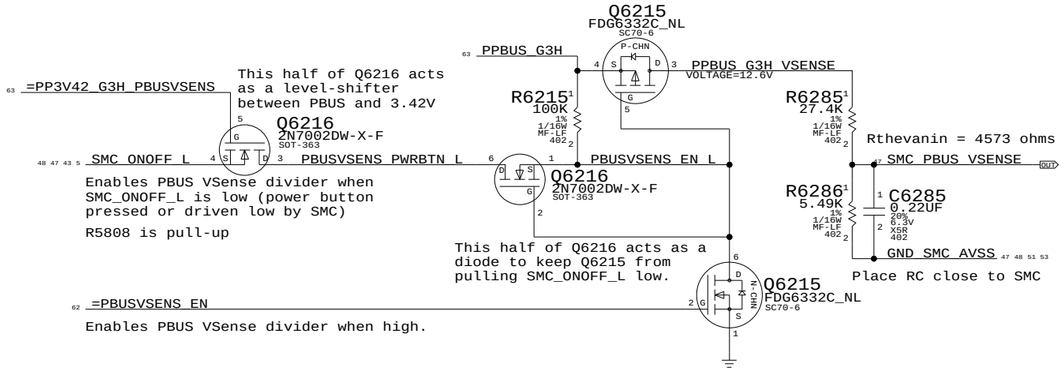
CPU Voltage Sense / Filter



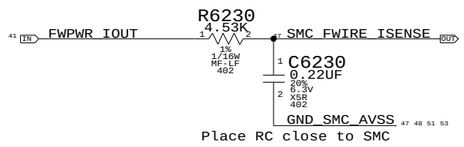
GPU Voltage Sense / Filter



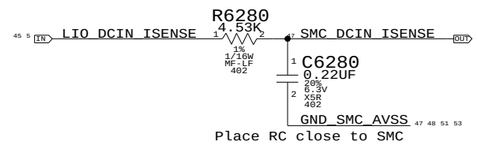
PBUS Voltage Sense Enable & Filter



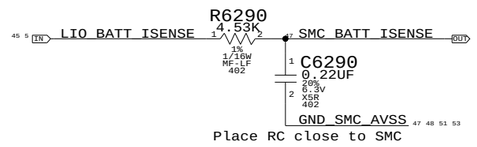
FireWire Current Sense Filter



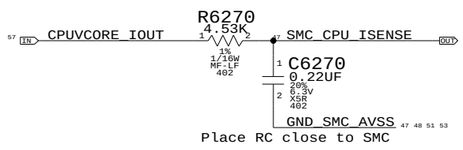
DCIN Current Sense Filter



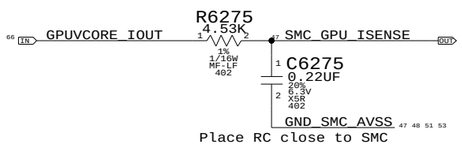
Battery Current Sense Filter



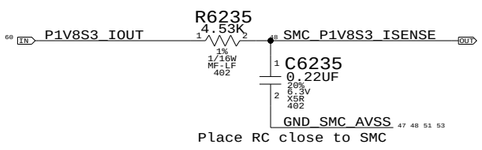
CPU Current Sense Filter



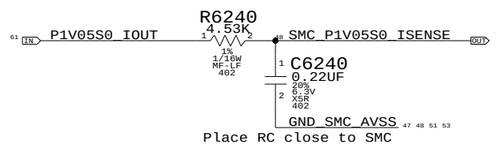
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

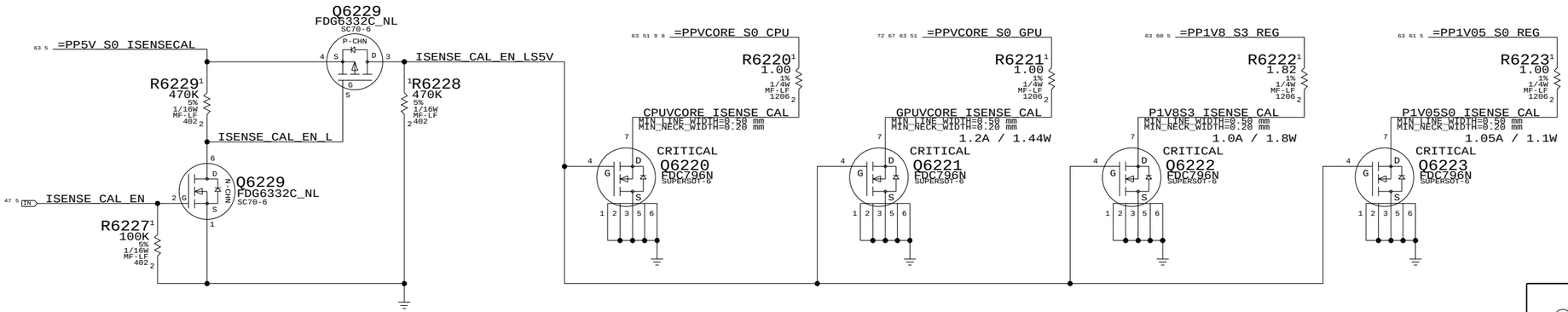


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



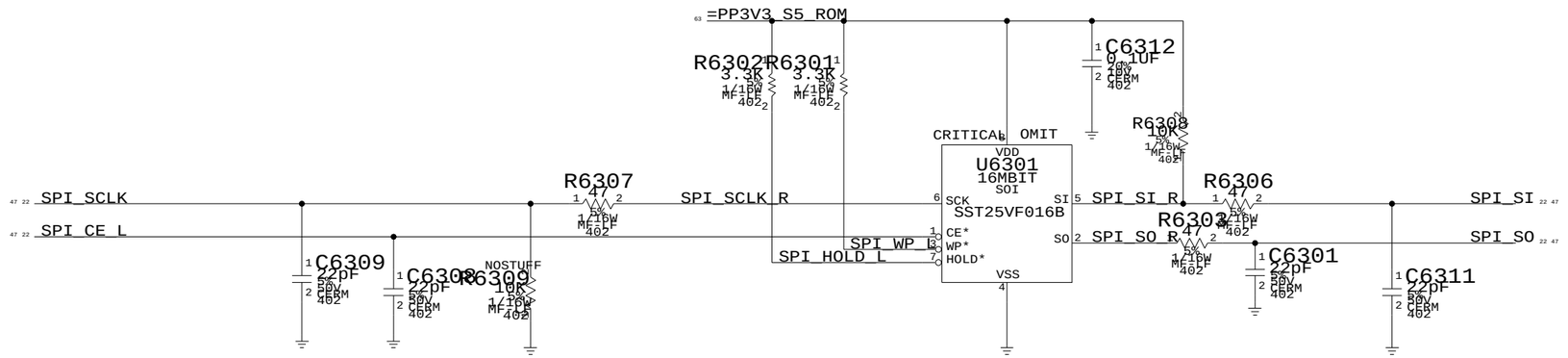
Current & Voltage Sensing

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	62	104



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

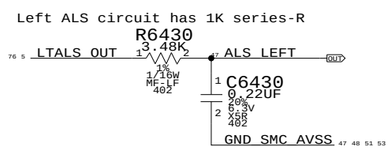
SYNC_MASTER=MSZ SYNC_DATE=11/16/2005

APPLE COMPUTER INC.

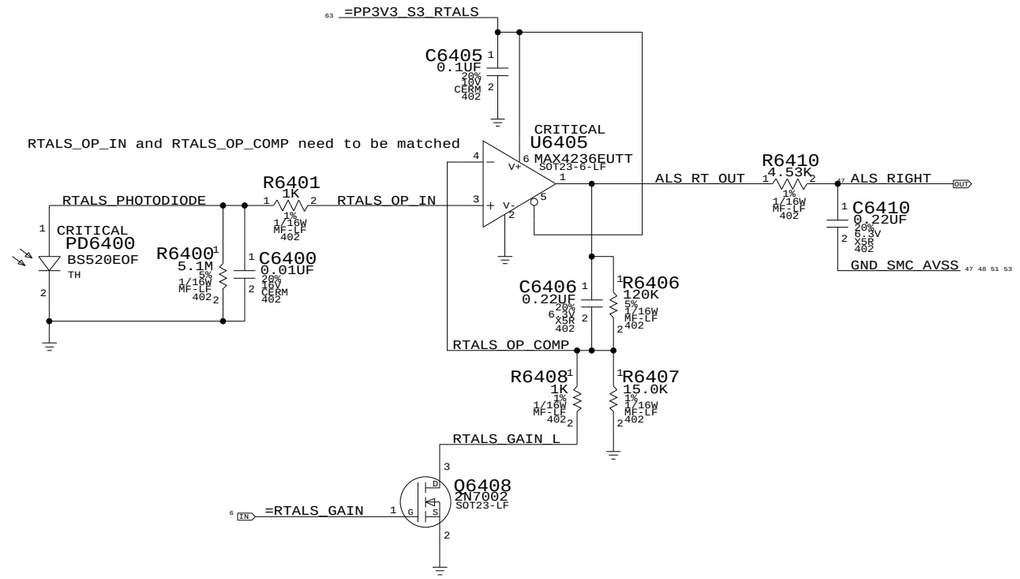
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	63	104

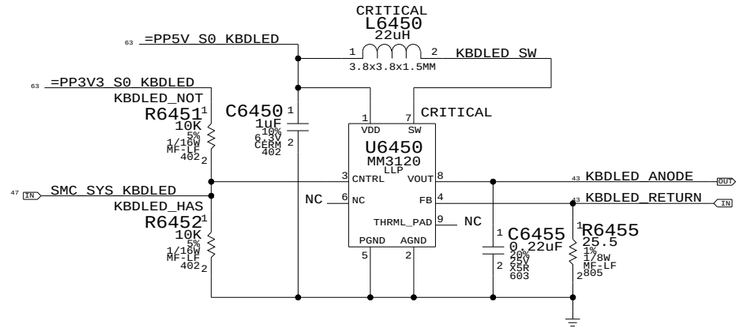
Left ALS Filter



Right ALS Circuit



Keyboard LED Driver



ALS Support			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		
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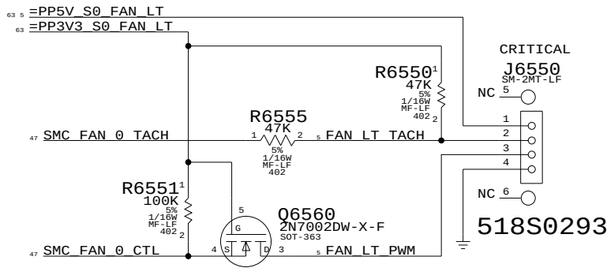
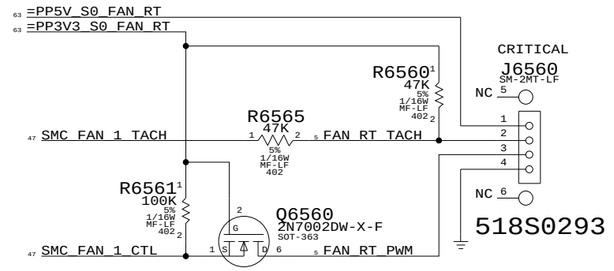
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7099	REV. D
	SCALE NONE	SHT 64 OF 104	

Left Fan



Right Fan



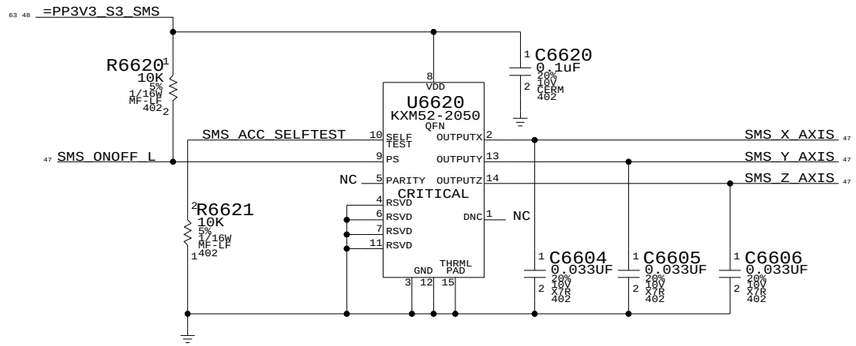
Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

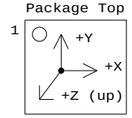
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	65	104



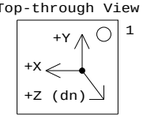
Desired orientation when placed on board top-side:

Package Top



Desired orientation when placed on board bottom-side:

Top-through View



M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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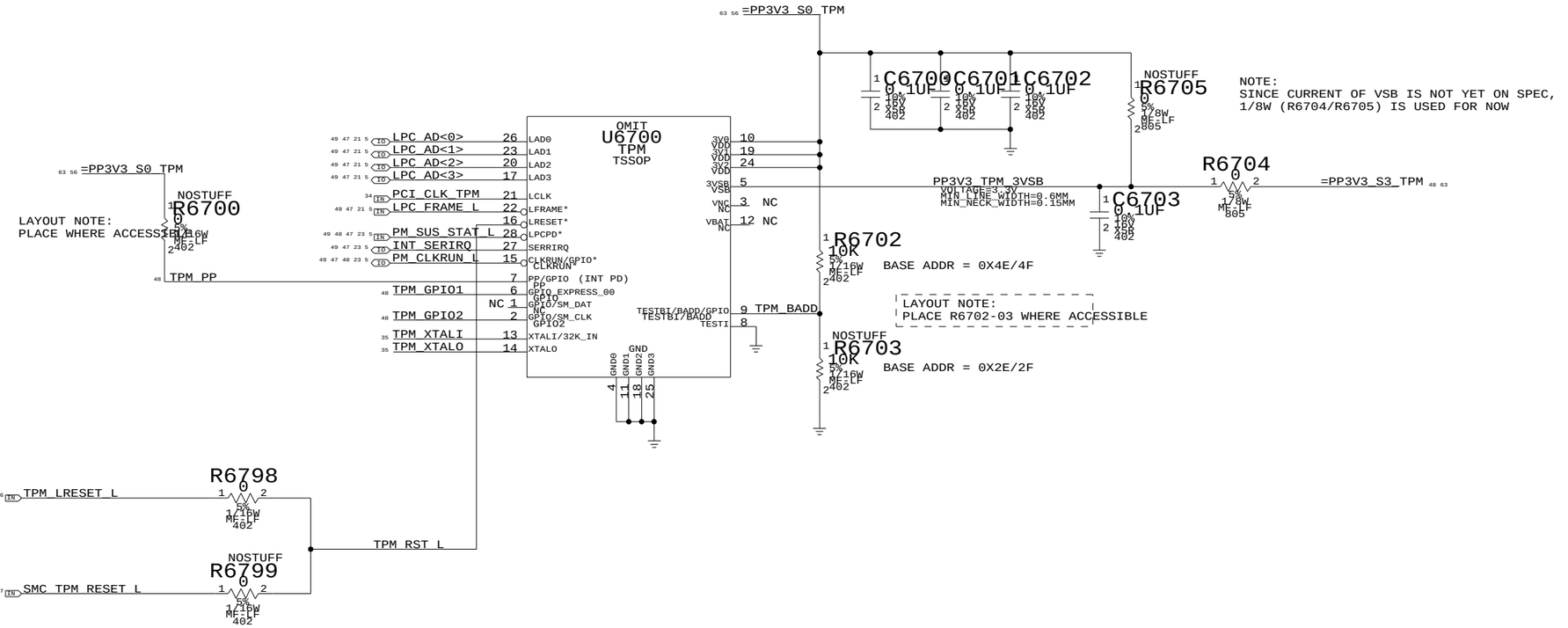
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 66 OF 104



TPM

SYNC_MASTER=M38 SYNC_DATE=11/16/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	67	104

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

CPU VCore Current Sense

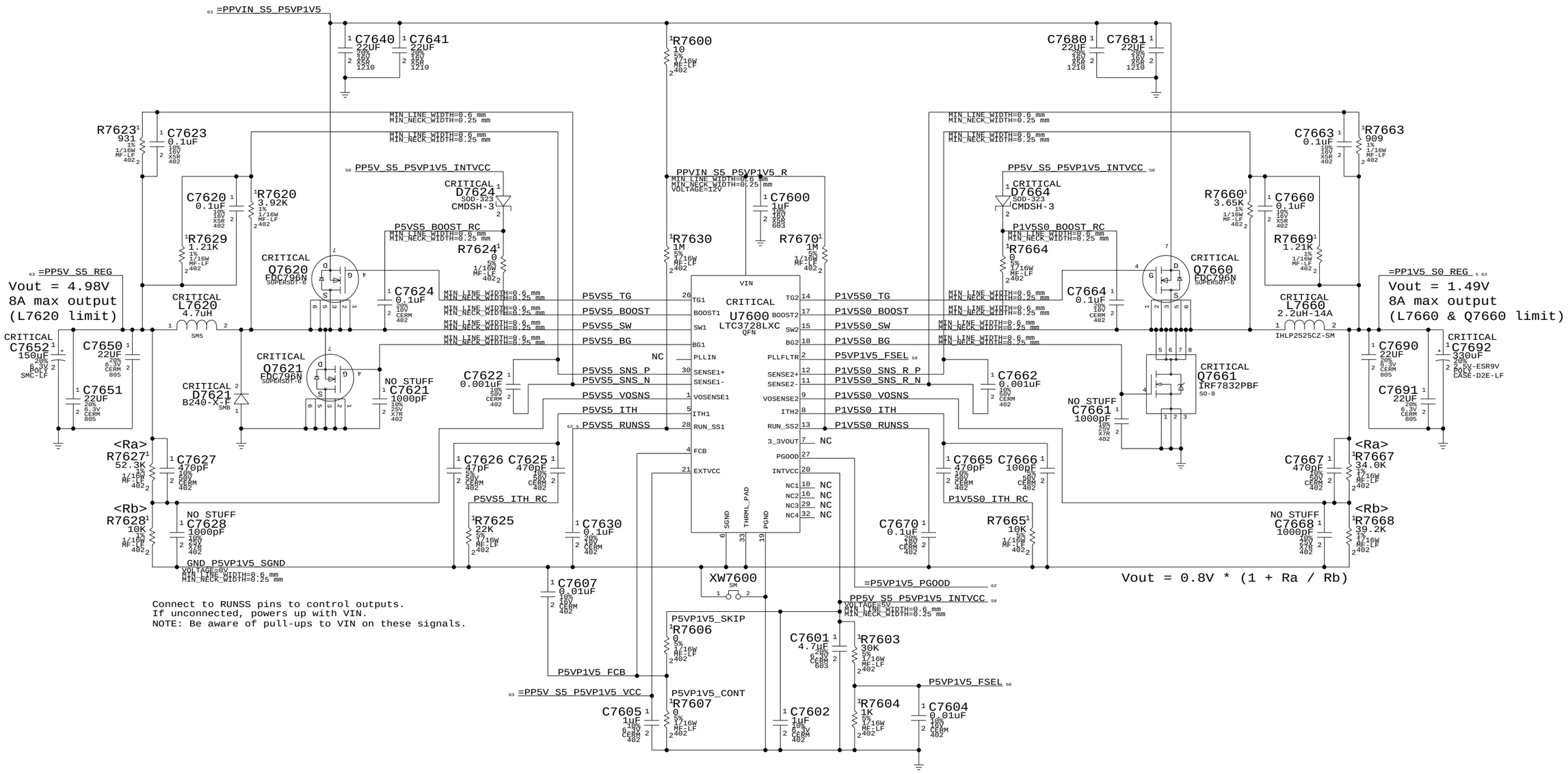
Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

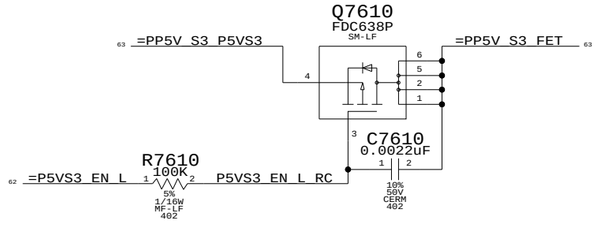
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

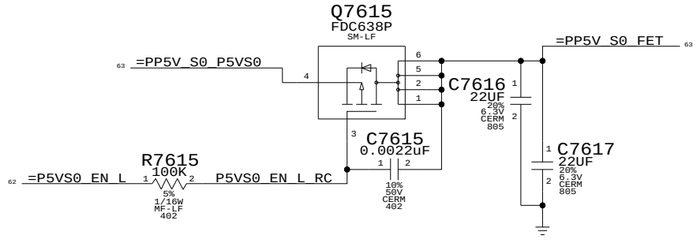
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 75 OF 104	



5V S3 FET



5V S0 FET



5V / 1.5V Power Supply

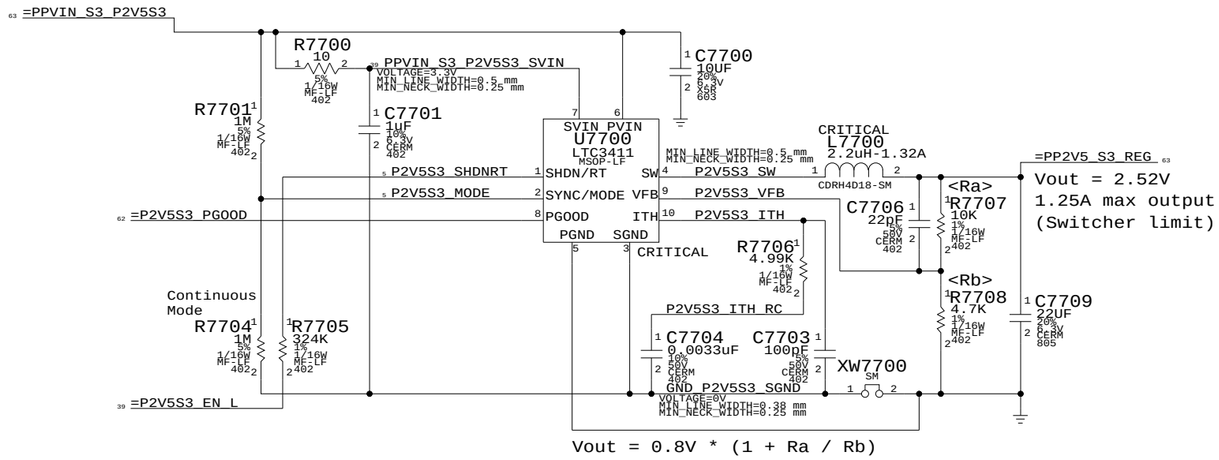
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

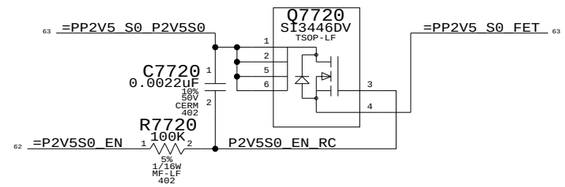
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	76	104

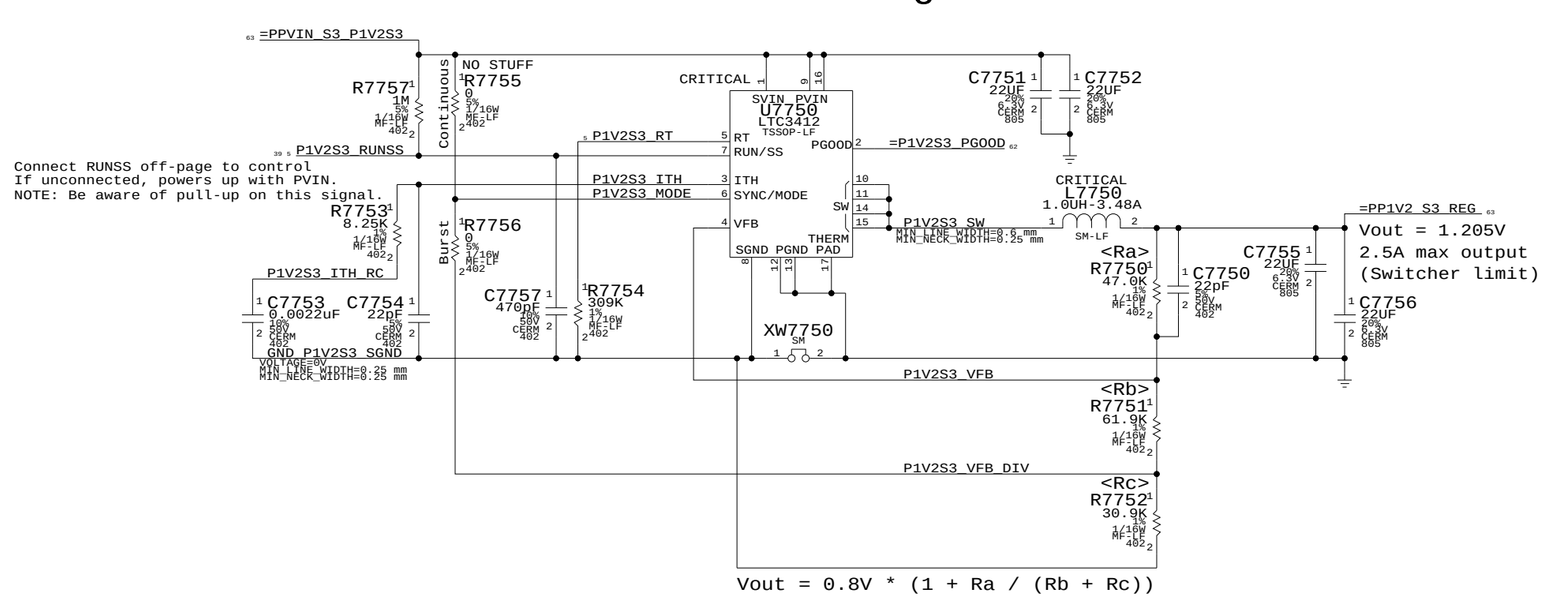
2.5V S3 Regulator



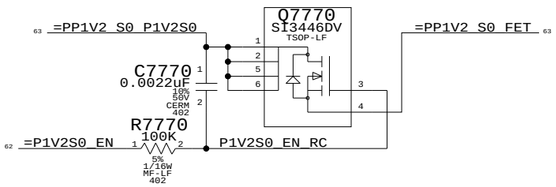
2.5V S0 FET



1.2V S3 Regulator



1.2V S0 FET



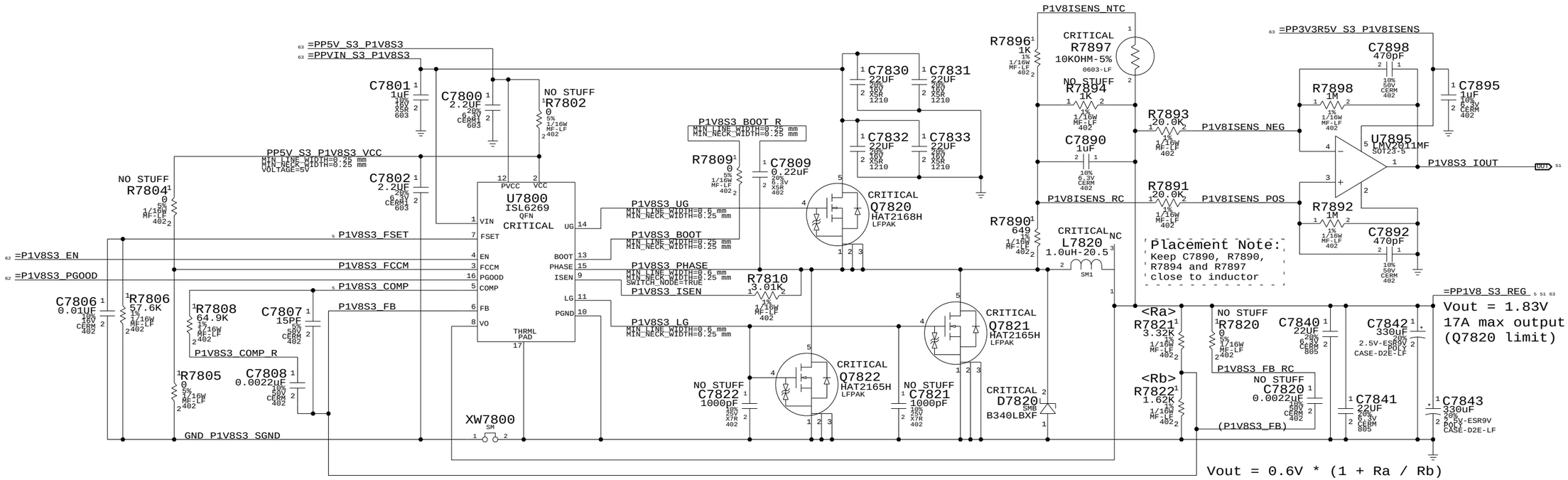
2.5V & 1.2V Regulators

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

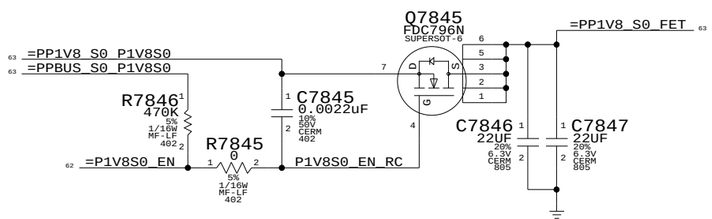
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 77 OF 104	

1.8V S3 Current Sense



1.8V S0 FET



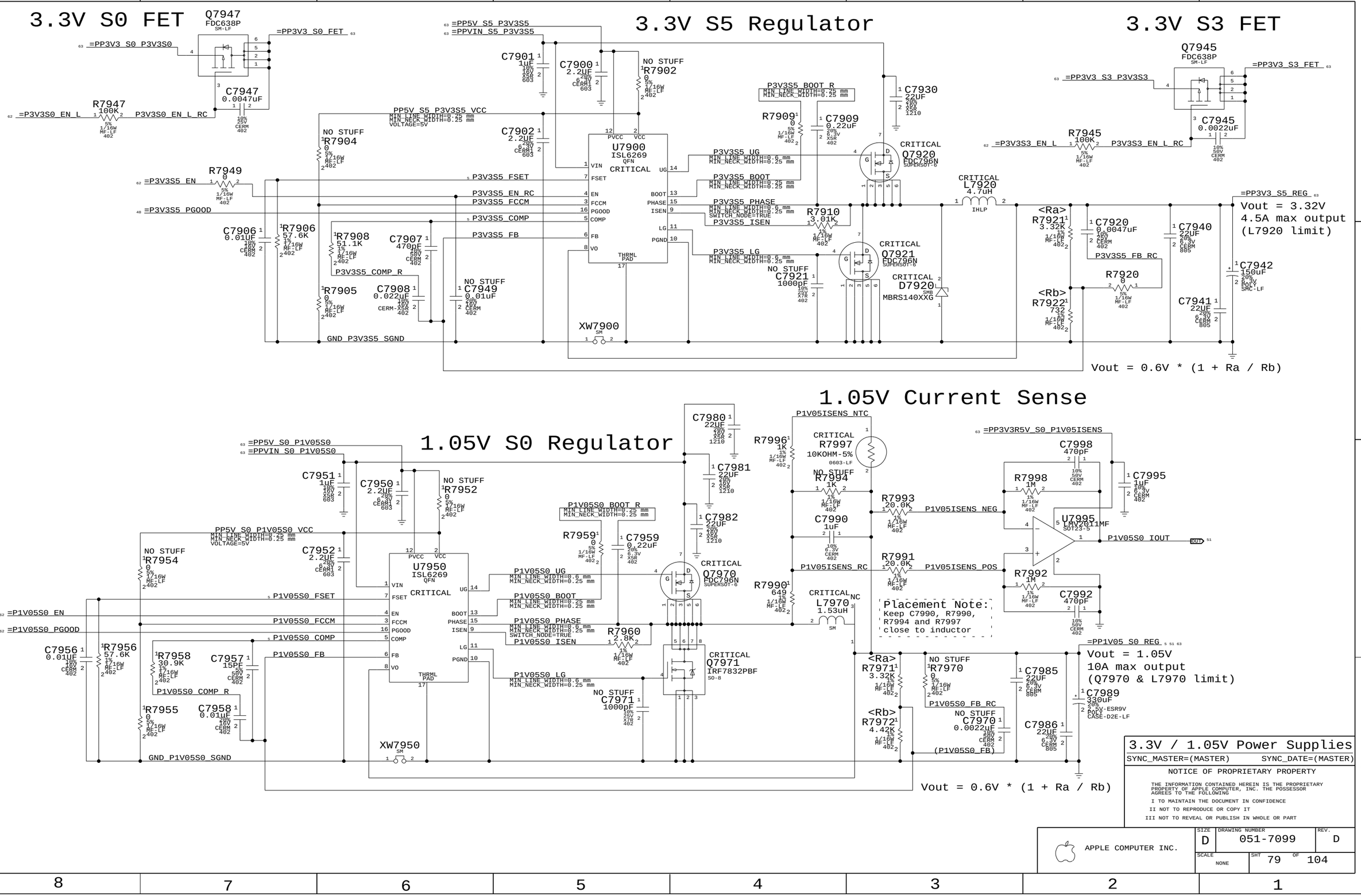
1.8V Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	78	104


3.3V S0 FET
Q7947
FDC638P
SM-LF
=PP3V3_S0_FET
=PP3V3_S0_P3V3S0
C7947
0.0047uF
R7947
100K
=P3V3S0_EN_L
P3V3S0_EN_L_RC
3.3V S5 Regulator
=PP5V_S5_P3V3S5
=PPVIN_S5_P3V3S5
C7901
1uF
C7900
2.2uF
NO STUFF
R7902
0
P3V3S5_BOOT_R
R7909
0
C7909
0.22uF
C7930
22UF
PP5V_S5_P3V3S5_VCC
C7902
2.2uF
NO STUFF
R7904
0
U7900
ISL6269
QFN
CRITICAL
VIN
FSET
EN
FCCM
PGOOD
COMP
FB
VO
PVCC
VCC
UG
BOOT
PHASE
ISEN
LG
PGND
THRML PAD
P3V3S5_UG
P3V3S5_BOOT
P3V3S5_PHASE
P3V3S5_ISEN
P3V3S5_LG
CRITICAL
Q7920
FDC796N
SUPERSOT-8
R7949
0
=P3V3S5_EN
=P3V3S5_PGOOD
P3V3S5_FSET
P3V3S5_EN_RC
P3V3S5_FCCM
P3V3S5_COMP
P3V3S5_FB
C7906
0.01UF
R7906
57.6K
R7908
51.1K
C7907
470PF
P3V3S5_COMP_R
R7905
0
C7908
0.022uF
NO STUFF
C7949
0.01uF
XW7900
SM
GND_P3V3S5_SGND
R7910
3.01K
CRITICAL
Q7921
FDC796N
SUPERSOT-8
NO STUFF
C7921
1000pF
CRITICAL
D7920
SMB
MBRS140XXG
CRITICAL
L7920
4.7uH
IHLP
=PP3V3_S5_REG
Vout = 3.32V
4.5A max output
(L7920 limit)
<Ra>
R7921
3.32K
C7920
0.0047uF
P3V3S5_FB_RC
R7920
0
<Rb>
R7922
732
C7940
22UF
C7941
22UF
C7942
150uF
Vout = 0.6V * (1 + Ra / Rb)
3.3V S3 FET
Q7945
FDC638P
SM-LF
=PP3V3_S3_FET
=PP3V3_S3_P3V3S3
C7945
0.0022uF
R7945
100K
=P3V3S3_EN_L
P3V3S3_EN_L_RC
1.05V Current Sense
P1V05ISENS_NTC
R7996
1K
CRITICAL
R7997
10KOHM-5%
0603-LF
NO STUFF
R7994
1K
R7993
20.0K
P1V05ISENS_NEG
C7990
1uF
R7991
20.0K
P1V05ISENS_RC
P1V05ISENS_POS
R7990
649
CRITICAL
L7970
1.53uH
NC
SM
Placement Note:
Keep C7990, R7990,
R7994 and R7997
close to inductor
=PP3V3R5V_S0_P1V05ISENS
C7998
470PF
R7998
1M
C7995
1UF
U7995
LMV2011MF
SOT23-5
P1V05S0_IOUT
OUT
R7992
1M
C7992
470PF
1.05V S0 Regulator
=PP5V_S0_P1V05S0
=PPVIN_S0_P1V05S0
C7951
1uF
C7950
2.2UF
NO STUFF
R7952
0
C7980
22UF
C7981
22UF
C7982
22UF
P1V05S0_BOOT_R
R7959
0
C7959
0.22uF
PP5V_S0_P1V05S0_VCC
C7952
2.2uF
NO STUFF
R7954
0
U7950
ISL6269
QFN
CRITICAL
P1V05S0_UG
P1V05S0_BOOT
P1V05S0_PHASE
P1V05S0_ISEN
P1V05S0_LG
CRITICAL
Q7970
FDC796N
SUPERSOT-8
R7960
2.8K
CRITICAL
Q7971
IRF7832PBF
SO-8
NO STUFF
C7971
1000pF
=P1V05S0_EN
=P1V05S0_PGOOD
P1V05S0_FSET
P1V05S0_FCCM
P1V05S0_COMP
P1V05S0_FB
C7956
0.01UF
R7956
57.6K
R7958
30.9K
C7957
15PF
P1V05S0_COMP_R
R7955
0
C7958
0.01uF
XW7950
SM
GND_P1V05S0_SGND
<Ra>
R7971
3.32K
NO STUFF
R7970
0
P1V05S0_FB_RC
<Rb>
R7972
4.42K
NO STUFF
C7970
0.0022uF
(P1V05S0_FB)
C7985
22UF
C7986
22UF
=PP1V05_S0_REG
Vout = 1.05V
10A max output
(Q7970 & L7970 limit)
C7989
330uF
Vout = 0.6V * (1 + Ra / Rb)
3.3V / 1.05V Power Supplies
SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
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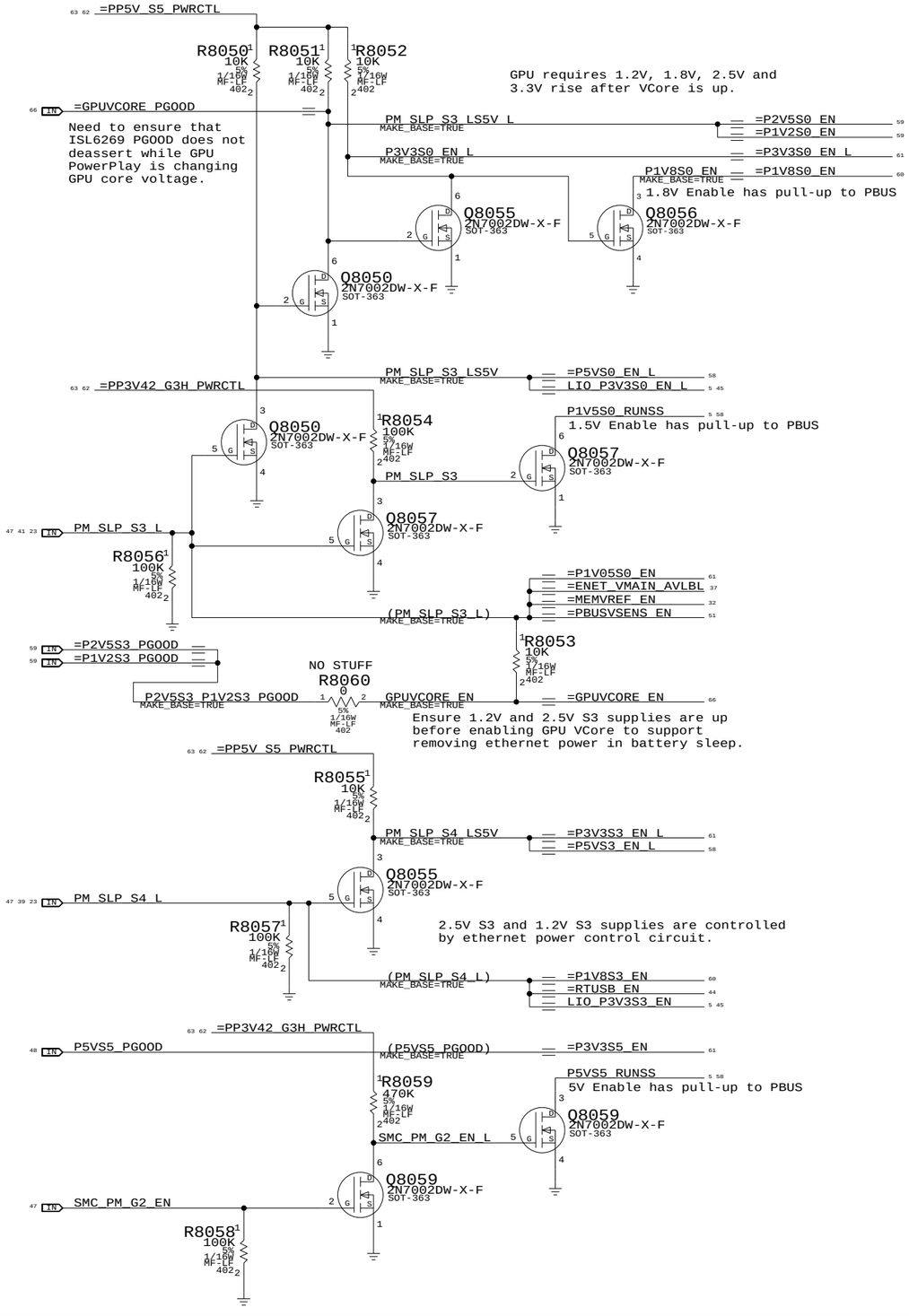
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-7099
REV. D
SCALE NONE
SHT 79 OF 104

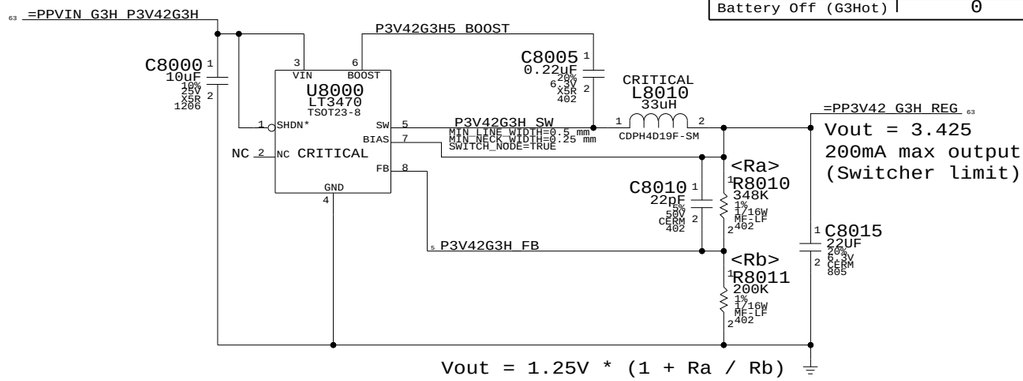
Power Control Signals



State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

3.425V "G3Hot" Supply

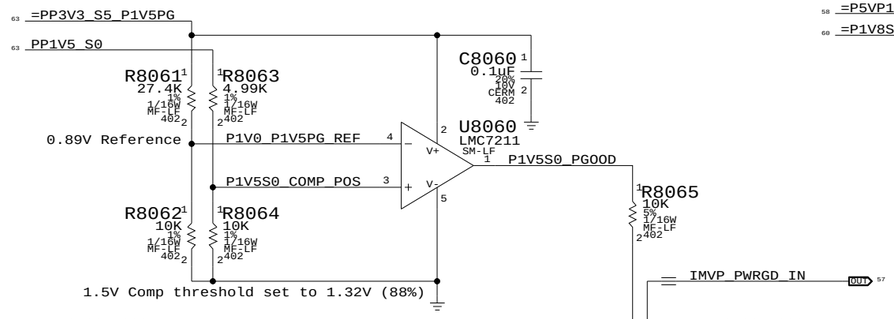
Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



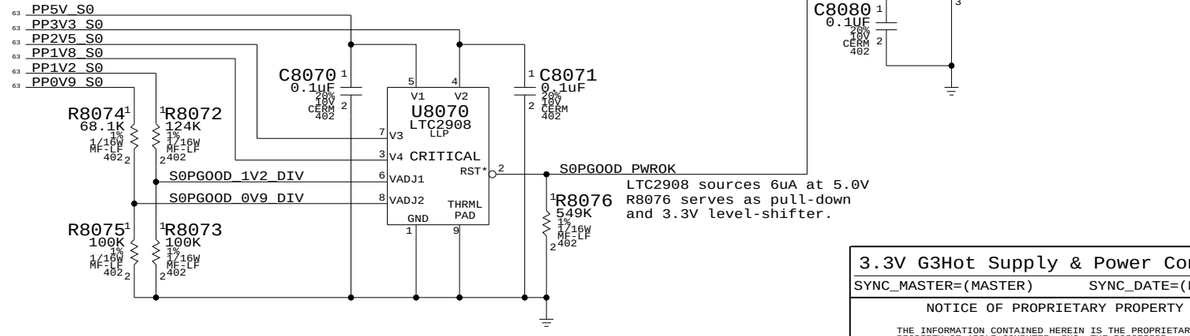
Unused PGOOD Signals

=P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD (MAKE_BASE=TRUE)

=P1V8S3_PGOOD — TP_P1V8S3_PGOOD (MAKE_BASE=TRUE)

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation



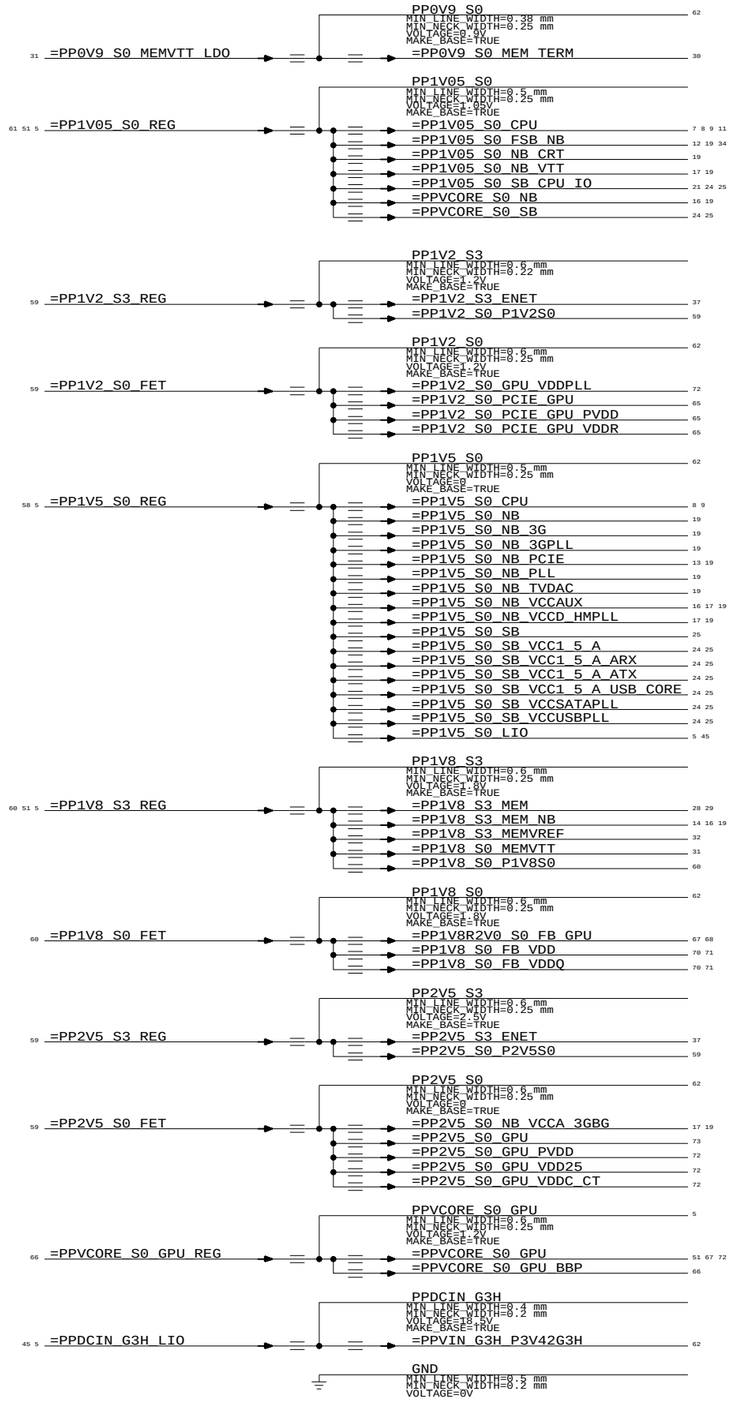
LTC2908 threshold is 95% (4.75V, 3.135V, 2.375V, 1.71V, 1.14V, 0.86V)

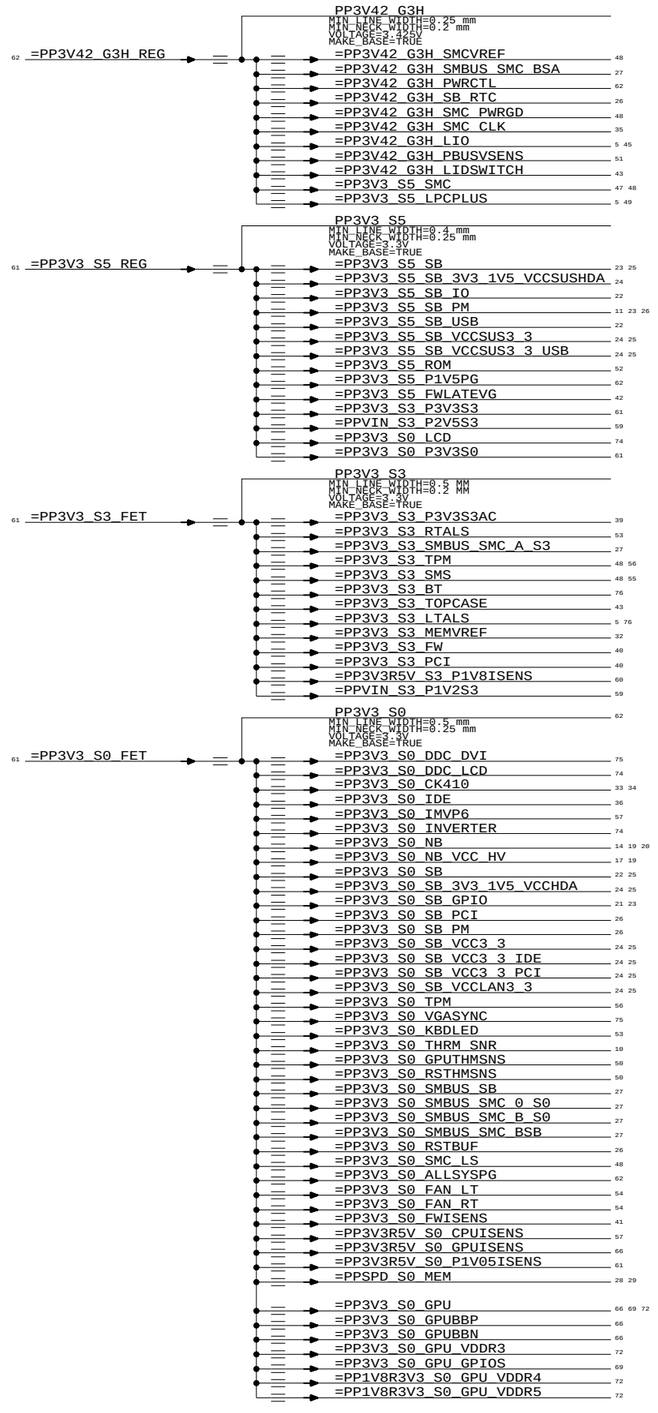
3.3V G3Hot Supply & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

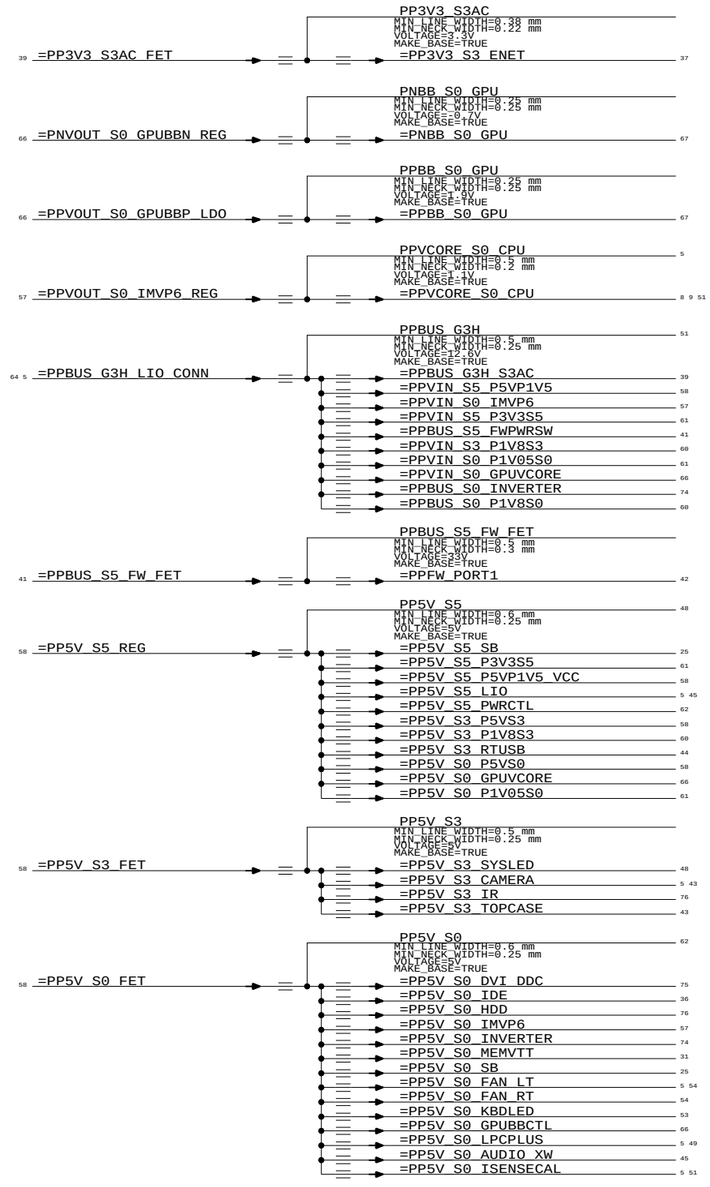
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 80 OF 104	





"S3AC" rail is ON in S3 on AC, OFF in S3 on battery



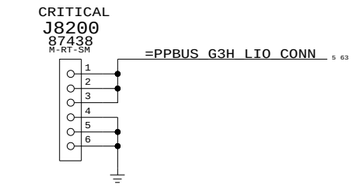
Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 81 OF 104	

Left I/O Power Connector



518S0368

Battery Connector (Digital Signals)

518S0293

PBus-In & Battery Connectors

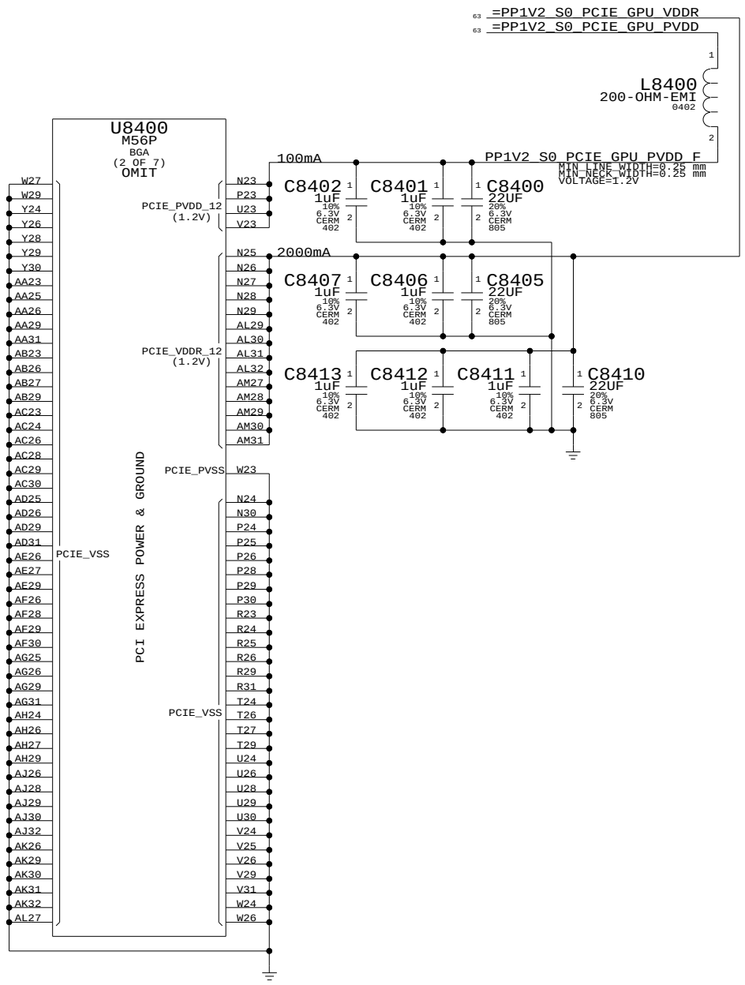
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

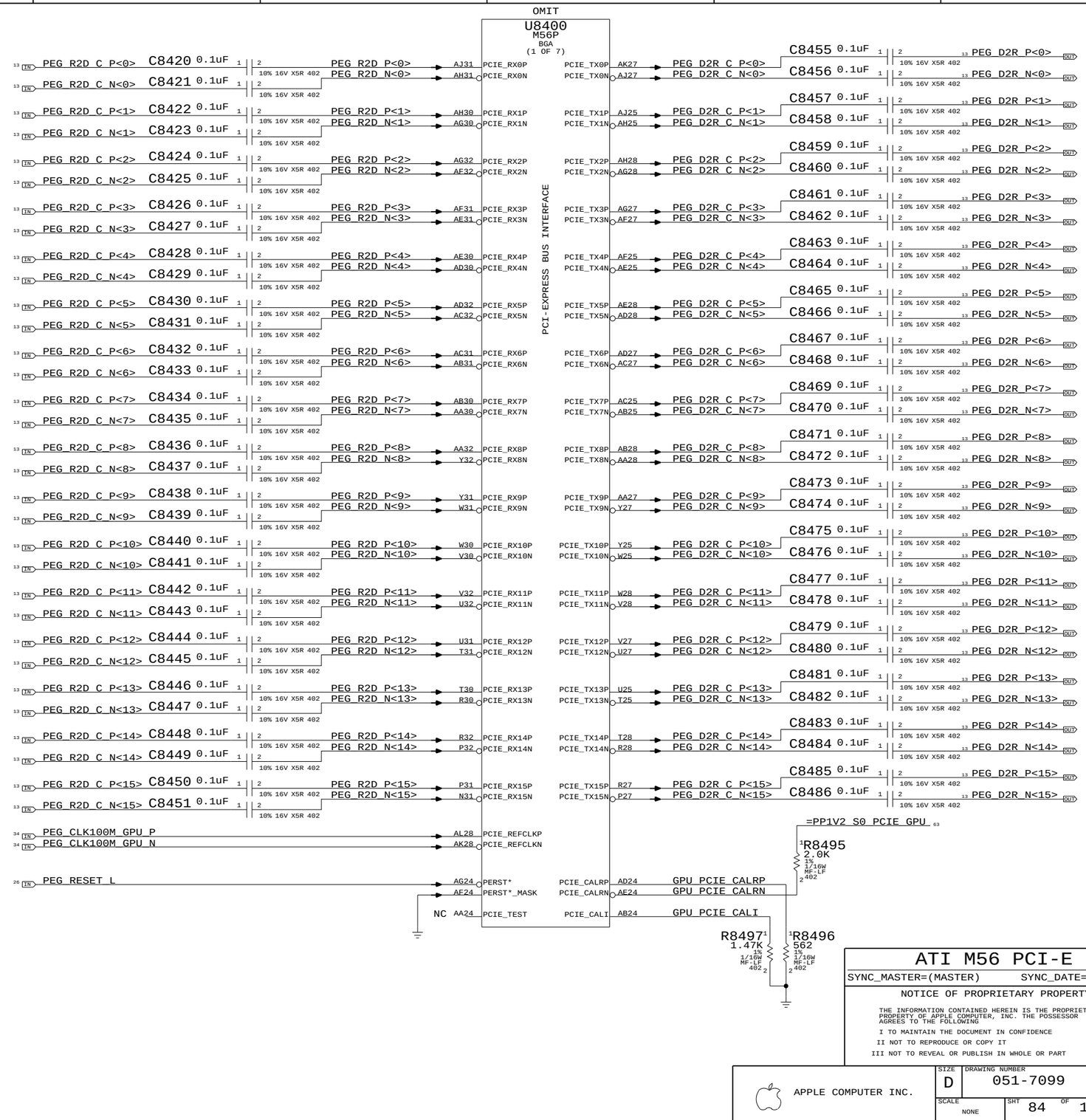
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE

SHT 82 OF 104





ATI M56 PCI-E

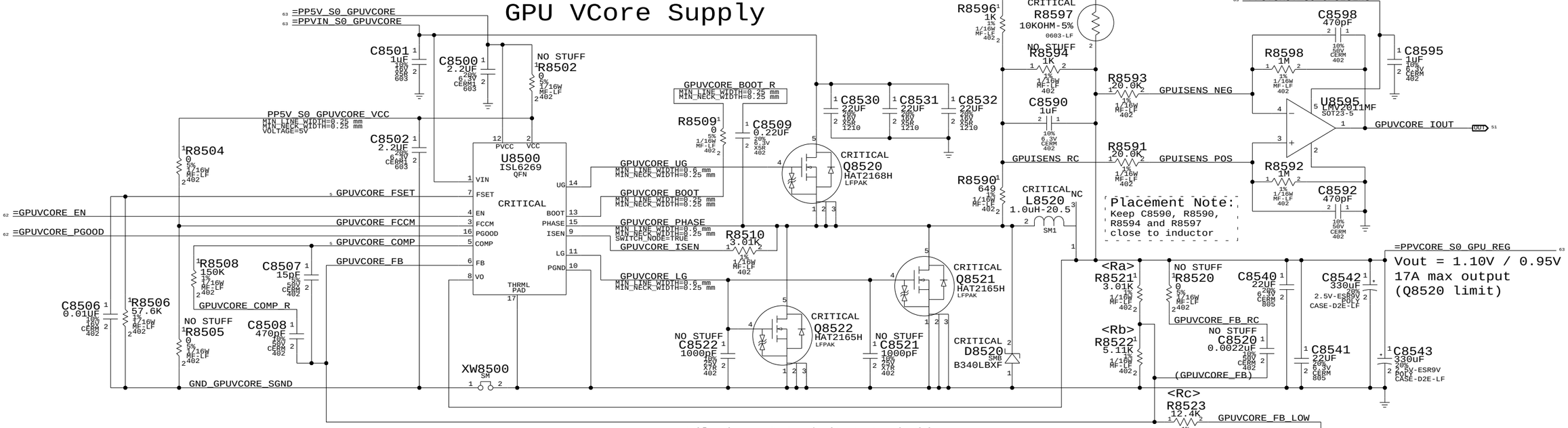
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	84	104

GPU VCore Supply

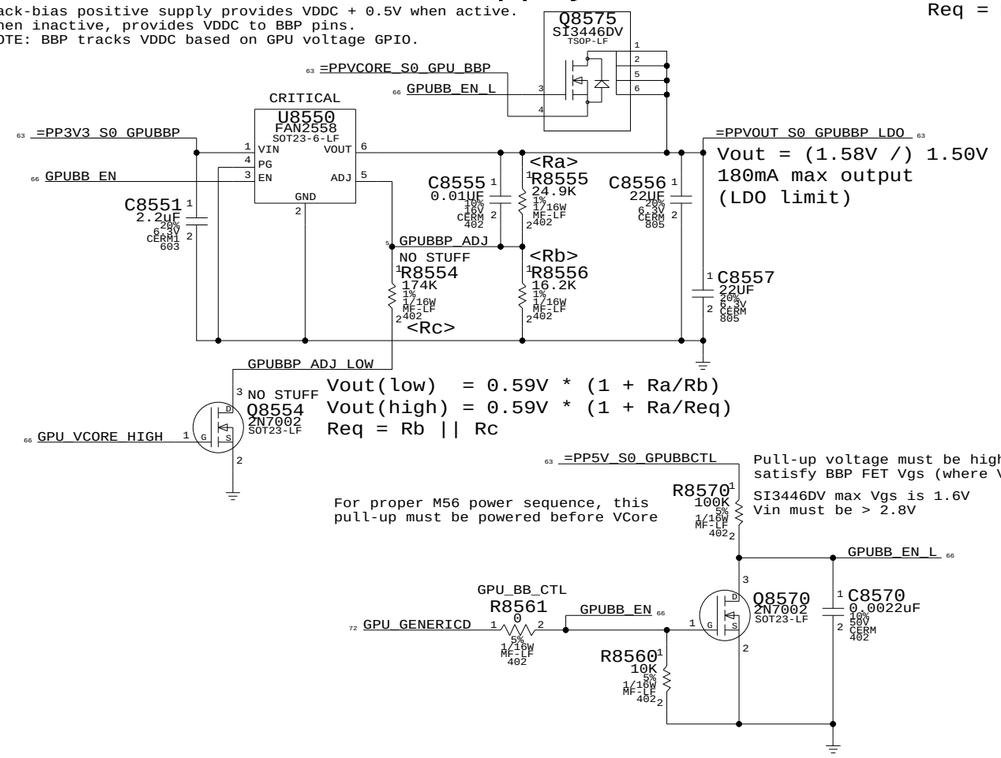


Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

GPU VCore Current Sense

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



=PP5V_S0_GPUBBCTL

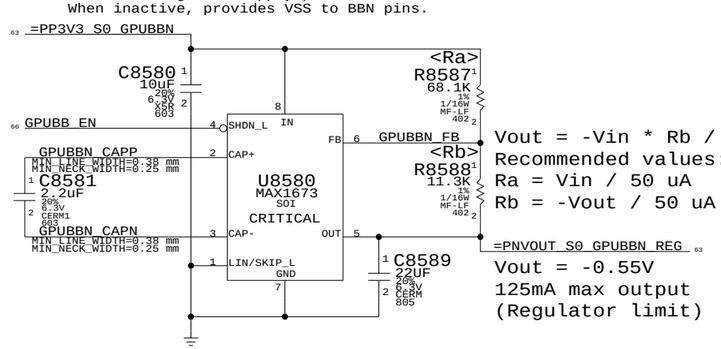
Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)

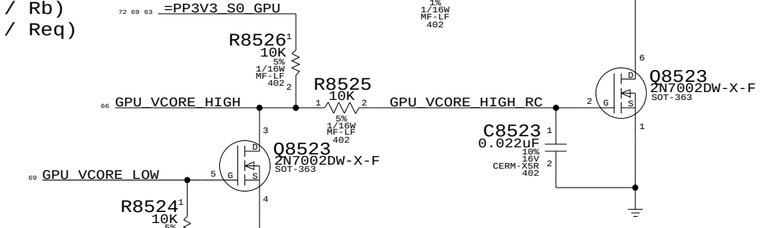
SI3446DV max Vgs is 1.6V
Vin must be > 2.8V

For proper M56 power sequence, this pull-up must be powered before VCore

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.



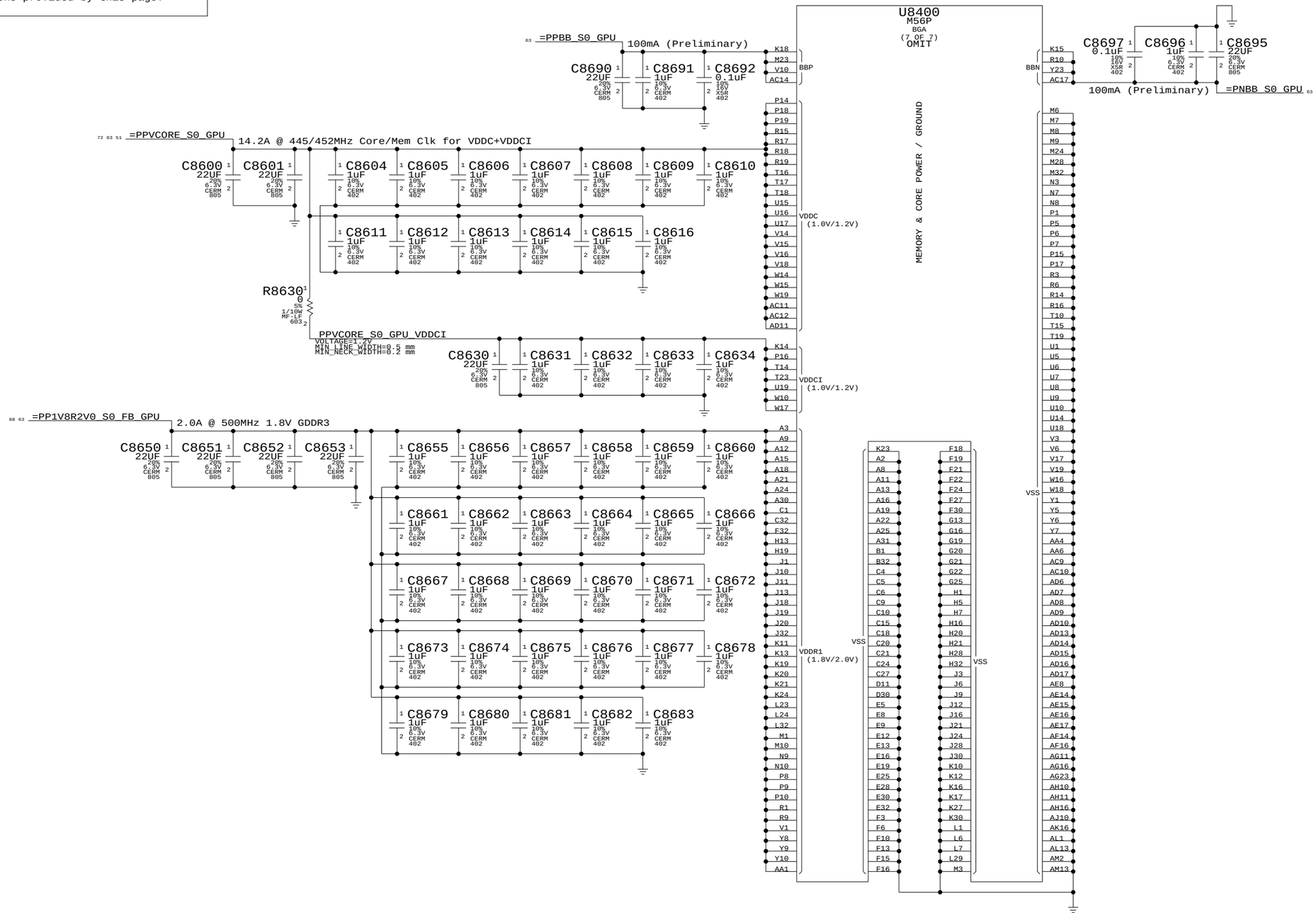


Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

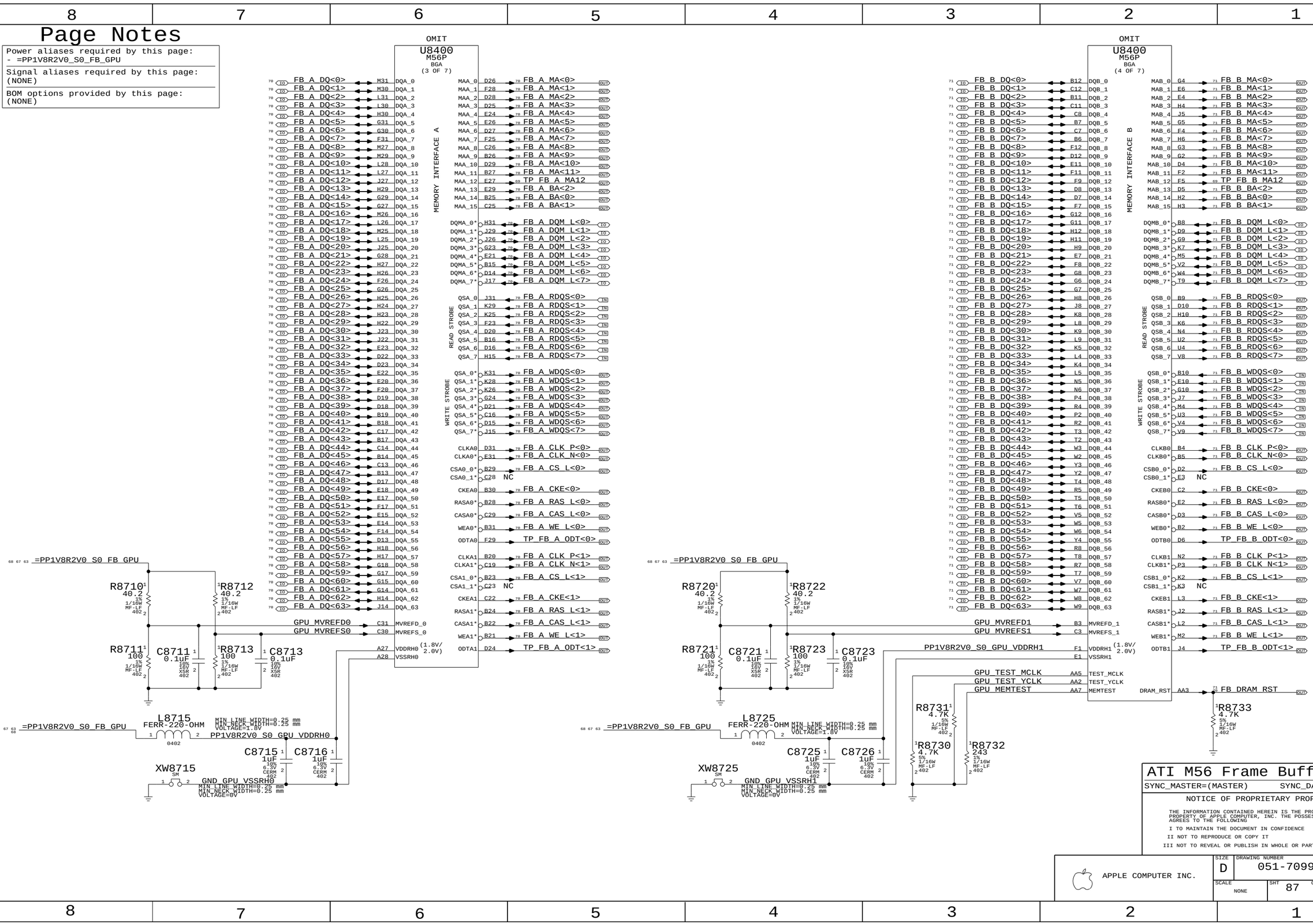
SCALE	SHT	OF
NONE	86	104

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Frame Buffer I/F

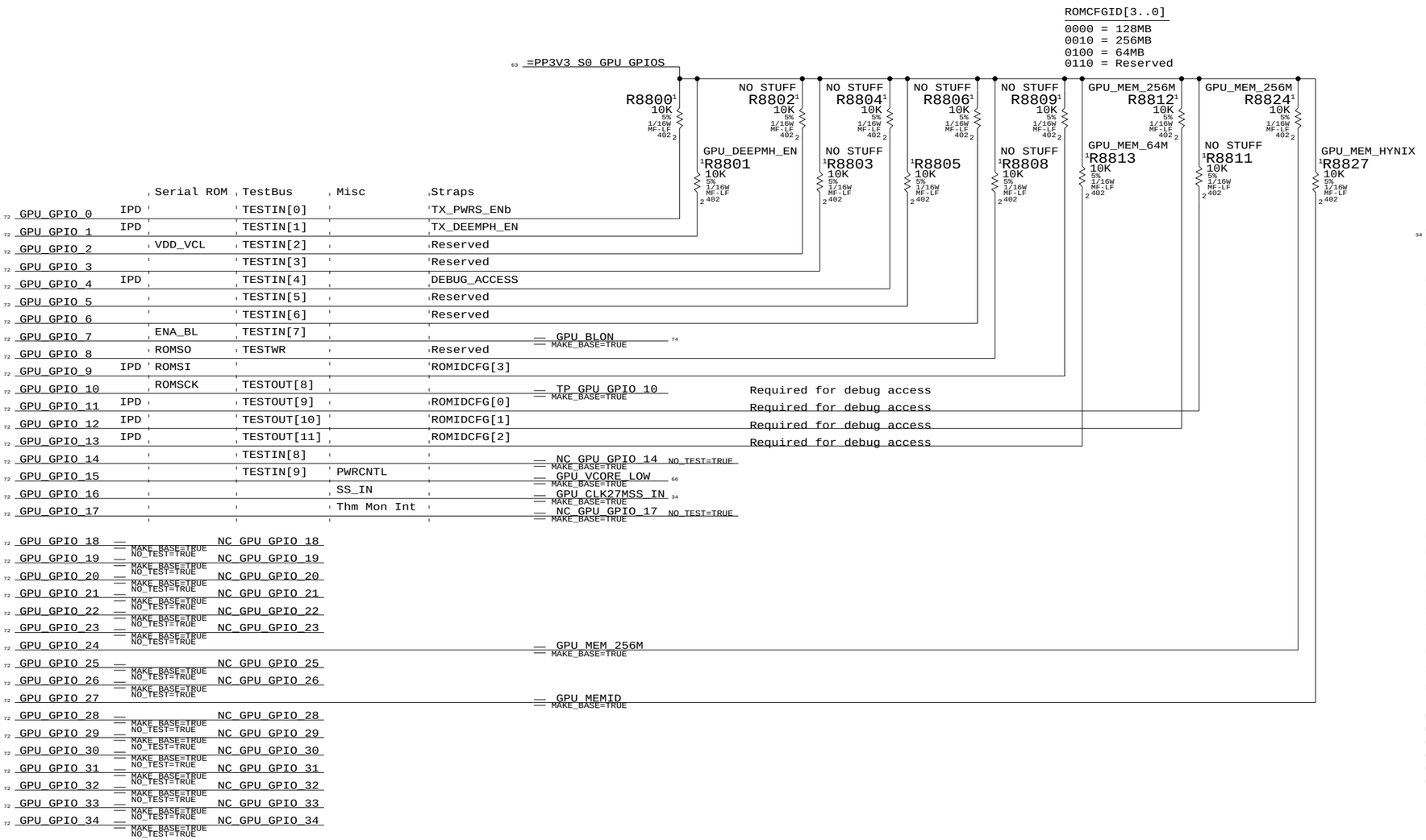
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

SHT 87 OF 104



GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 88 OF 104	

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_S0_FB_VDD

=PP1V8_S0_FB_VDDQ

C8900 C8901 C8902 C8903 C8904 C8910 C8915 — 22UF 20% 6.3V CERM 805; 0.1uF 10% 16V X5R 402

L8910 FERR-220-OHM 0402 — PP1V8_S0_FB_A0_VDDA0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

L8915 FERR-220-OHM 0402 — PP1V8_S0_FB_A0_VDDA1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

U8900.J1 U8900.J12

CRITICAL OMIT

U8900 FBGA (2 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

C8920 C8921 C8922 C8923 C8924 C8925 C8926 — 22UF 20% 6.3V CERM 805; 0.1uF 10% 16V X5R 402

R8930 R8932 — 2.37K 1% 1/10W MF-LF 402

FB_A0_VREF0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A0_VREF1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R8931 R8933 — 5.49K 1% 1/10W MF-LF 402

C8931 C8933 — 0.1uF 10% 16V X5R 402

R8940 R8942 — 121 1% 1/10W MF-LF 402

R8944 — 121 1% 1/10W MF-LF 402

R8946 — 60.4 1% 1/10W MF-LF 402

R8941 — 1K 5% 1/10W MF-LF 402

R8943 — 121 1% 1/10W MF-LF 402

R8945 — 60.4 1% 1/10W MF-LF 402

R8947 — 121 1% 1/10W MF-LF 402

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

FB_A_MA<0> FB_A_MA<1> FB_A_MA<2> FB_A_MA<3> FB_A_MA<4> FB_A_MA<5> FB_A_MA<6> FB_A_MA<7> FB_A_MA<8> FB_A_MA<9> FB_A_MA<10> FB_A_MA<11>

FB_A_CKE<0> FB_A_CLK_P<0> FB_A_CLK_N<0> FB_A_CS_L<0> FB_A_WE_L<0> FB_A_CAS_L<0> FB_A_RAS_L<0>

FB_A0_ZQ FB_A0_MF FB_A0_SEN

FB_DRAM_RST

FB_A_RDQS<0> FB_A_RDQS<1> FB_A_RDQS<2> FB_A_RDQS<3>

FB_A_WDQS<0> FB_A_WDQS<1> FB_A_WDQS<2> FB_A_WDQS<3>

FB_A_BA<0> FB_A_BA<1> FB_A_BA<2>

FB_A_DQM_L<0> FB_A_DQM_L<1> FB_A_DQM_L<2> FB_A_DQM_L<3>

FB_A_DQ<0> FB_A_DQ<1> FB_A_DQ<2> FB_A_DQ<3> FB_A_DQ<4> FB_A_DQ<5> FB_A_DQ<6> FB_A_DQ<7> FB_A_DQ<8> FB_A_DQ<9> FB_A_DQ<10> FB_A_DQ<11> FB_A_DQ<15> FB_A_DQ<14> FB_A_DQ<12> FB_A_DQ<13> FB_A_DQ<19> FB_A_DQ<16> FB_A_DQ<18> FB_A_DQ<17> FB_A_DQ<23> FB_A_DQ<21> FB_A_DQ<20> FB_A_DQ<22> FB_A_DQ<24> FB_A_DQ<25> FB_A_DQ<26> FB_A_DQ<27> FB_A_DQ<29> FB_A_DQ<30> FB_A_DQ<28> FB_A_DQ<31>

NC NC

R8948 — 243 1% 1/10W MF-LF 402

R8949 — 100 5% 1/10W MF-LF 402

C8950 C8951 C8952 C8953 C8954 C8960 C8965 — 22UF 20% 6.3V CERM 805; 0.1uF 10% 16V X5R 402

L8960 FERR-220-OHM 0402 — PP1V8_S0_FB_A1_VDDA0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

L8965 FERR-220-OHM 0402 — PP1V8_S0_FB_A1_VDDA1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.8V

Connect to designated pin, then GND

U8900.J1 U8900.J12

CRITICAL OMIT

U8950 FBGA (1 OF 2) 16MX32-GDDR3-500MHZ K4J52324QC-BC20

C8970 C8971 C8972 C8973 C8974 C8975 C8976 — 22UF 20% 6.3V CERM 805; 0.1uF 10% 16V X5R 402

R8980 R8982 — 2.37K 1% 1/10W MF-LF 402

FB_A1_VREF0 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

FB_A1_VREF1 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R8981 R8983 — 5.49K 1% 1/10W MF-LF 402

C8981 C8983 — 0.1uF 10% 16V X5R 402

R8990 R8992 — 121 1% 1/10W MF-LF 402

R8994 — 121 1% 1/10W MF-LF 402

R8996 — 60.4 1% 1/10W MF-LF 402

R8991 — 1K 5% 1/10W MF-LF 402

R8993 — 121 1% 1/10W MF-LF 402

R8995 — 60.4 1% 1/10W MF-LF 402

R8997 — 121 1% 1/10W MF-LF 402

FB_A_MA<0> FB_A_MA<1> FB_A_MA<2> FB_A_MA<3> FB_A_MA<4> FB_A_MA<5> FB_A_MA<6> FB_A_MA<7> FB_A_MA<8> FB_A_MA<9> FB_A_MA<10> FB_A_MA<11>

FB_A_CKE<1> FB_A_CLK_P<1> FB_A_CLK_N<1> FB_A_CS_L<1> FB_A_WE_L<1> FB_A_CAS_L<1> FB_A_RAS_L<1>

FB_A1_ZQ FB_A1_MF FB_A1_SEN

FB_DRAM_RST

FB_A_RDQS<4> FB_A_RDQS<5> FB_A_RDQS<6> FB_A_RDQS<7>

FB_A_WDQS<4> FB_A_WDQS<5> FB_A_WDQS<6> FB_A_WDQS<7>

FB_A_BA<0> FB_A_BA<1> FB_A_BA<2>

FB_A_DQM_L<4> FB_A_DQM_L<5> FB_A_DQM_L<6> FB_A_DQM_L<7>

FB_A_DQ<32> FB_A_DQ<34> FB_A_DQ<33> FB_A_DQ<35> FB_A_DQ<36> FB_A_DQ<37> FB_A_DQ<38> FB_A_DQ<39> FB_A_DQ<40> FB_A_DQ<41> FB_A_DQ<42> FB_A_DQ<43> FB_A_DQ<46> FB_A_DQ<44> FB_A_DQ<47> FB_A_DQ<45> FB_A_DQ<48> FB_A_DQ<49> FB_A_DQ<50> FB_A_DQ<51> FB_A_DQ<52> FB_A_DQ<55> FB_A_DQ<54> FB_A_DQ<53> FB_A_DQ<60> FB_A_DQ<59> FB_A_DQ<61> FB_A_DQ<57> FB_A_DQ<62> FB_A_DQ<56> FB_A_DQ<63> FB_A_DQ<58>

NC NC

R8998 — 243 1% 1/10W MF-LF 402

R8999 — 100 5% 1/10W MF-LF 402

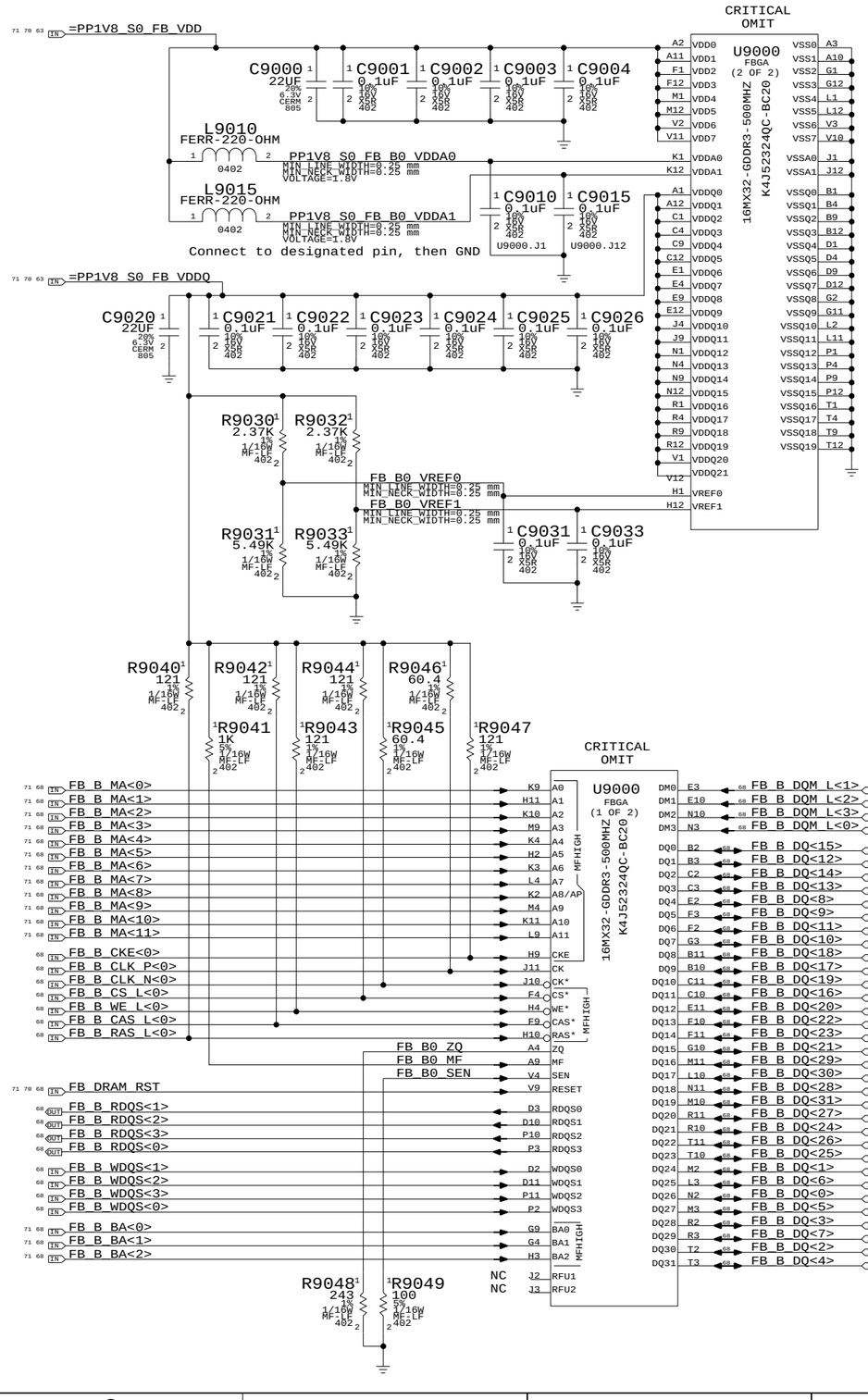
GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	89	104



Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

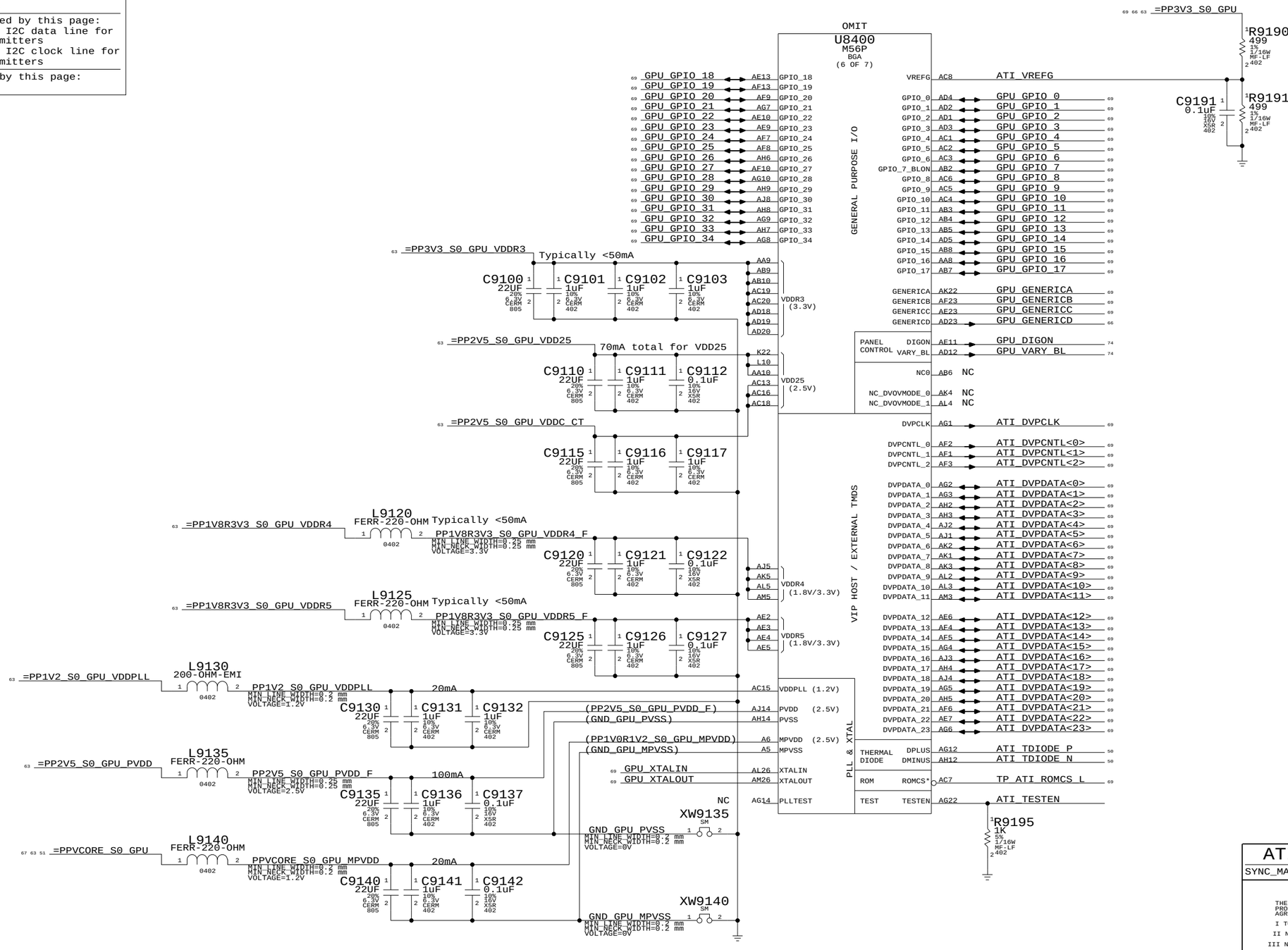
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 90 OF 104	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	91	104

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

63 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9300 22UF 20% 6.3V CERM 805; C9301 1UF 10% 6.3V CERM 402; C9302 1UF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9305 22UF 20% 6.3V CERM 805; C9306 1UF 10% 6.3V CERM 402; C9307 0.1UF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9310 22UF 20% 6.3V CERM 805; C9311 1UF 10% 6.3V CERM 402; C9312 0.1UF 10% 16V X5R 402

XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22UF 20% 6.3V CERM 805; C9316 1UF 10% 6.3V CERM 402; C9317 0.1UF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9320 22UF 20% 6.3V CERM 805; C9321 1UF 10% 6.3V CERM 402; C9322 0.1UF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V — 20mA peak
C9325 22UF 20% 6.3V CERM 805; C9326 1UF 10% 6.3V CERM 402; C9327 0.1UF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9330 22UF 20% 6.3V CERM 805; C9331 1UF 10% 6.3V CERM 402; C9332 1UF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9340 22UF 20% 6.3V CERM 805; C9345 22UF 20% 6.3V CERM 805; C9341 1UF 10% 6.3V CERM 402; C9342 0.1UF 10% 16V X5R 402; C9346 0.1UF 10% 16V X5R 402; C9347 0.1UF 10% 16V X5R 402

ATI_RSET 73 — R9350 499 1% 1/16W MF-LF 402
ATI_R2SET 73 — R9351 715 1% 1/16W MF-LF 402

OMIT
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR

DAC (CRT)
- AL25, AM25 AVDD (2.5V)
- AJ24, AK25 AVSS
- AK23 AVSSQ
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI
- AL22 RSET

DAC2 (TV/CRT2)
- AL16, AM16 A2VDD (2.5V)
- AL17, AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- AK14 R2SET

LVDS
- AE19 LPVDD (2.5V)
- AE18 LPVSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20 LVDDR (2.5V)
- AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- AF11 HPD1

TMDS outputs:
- TXCP AM9 — TMDS_CLK_P
- TXCM AL9 — TMDS_CLK_N
- TX0P AL10 — TMDS_DATA_P<0>
- TX0M AK10 — TMDS_DATA_N<0>
- TX1P AM11 — TMDS_DATA_P<1>
- TX1M AL11 — TMDS_DATA_N<1>
- TX2P AM12 — TMDS_DATA_P<2>
- TX2M AL12 — TMDS_DATA_N<2>
- TX3P AJ9 — TMDS_DATA_P<3>
- TX3M AK9 — TMDS_DATA_N<3>
- TX4P AJ11 — TMDS_DATA_P<4>
- TX4M AK11 — TMDS_DATA_N<4>
- TX5P AJ12 — TMDS_DATA_P<5>
- TX5M AK12 — TMDS_DATA_N<5>

DAC (CRT) outputs:
- R AK24 — GPU_VGA_R
- G AM24 — GPU_VGA_G
- B AL24 — GPU_VGA_B
- HSYNC AJ23 — GPU_VGA_HSYNC
- VSYNC AJ22 — GPU_VGA_VSYNC

DAC2 (TV/CRT2) outputs:
- R2 AK15 — GPU_R2
- G2 AM15 — GPU_G2
- B2 AL15 — GPU_B2
- H2SYNC AE15 — GPU_H2SYNC
- V2SYNC AG15 — GPU_V2SYNC
- Y AJ15 — GPU_TV_Y
- C AJ13 — GPU_TV_C
- COMP AH15 — GPU_TV_COMP

LVDS outputs:
- TXCLK_UP AJ21 — LVDS_U_CLK_P
- TXCLK_UN AK21 — LVDS_U_CLK_N
- TXOUT_U0P AG18 — LVDS_U_DATA_P<0>
- TXOUT_U0N AH18 — LVDS_U_DATA_N<0>
- TXOUT_U1P AK20 — LVDS_U_DATA_P<1>
- TXOUT_U1N AJ20 — LVDS_U_DATA_N<1>
- TXOUT_U2P AG20 — LVDS_U_DATA_P<2>
- TXOUT_U2N AH20 — LVDS_U_DATA_N<2>
- TXOUT_U3P AH21 — LVDS_U_DATA_P<3>
- TXOUT_U3N AG21 — LVDS_U_DATA_N<3>
- TXCLK_LP AM18 — LVDS_L_CLK_P
- TXCLK_LN AL18 — LVDS_L_CLK_N
- TXOUT_L0P AL19 — LVDS_L_DATA_P<0>
- TXOUT_L0N AK19 — LVDS_L_DATA_N<0>
- TXOUT_L1P AM20 — LVDS_L_DATA_P<1>
- TXOUT_L1N AL20 — LVDS_L_DATA_N<1>
- TXOUT_L2P AM21 — LVDS_L_DATA_P<2>
- TXOUT_L2N AL21 — LVDS_L_DATA_N<2>
- TXOUT_L3P AJ18 — LVDS_L_DATA_P<3>
- TXOUT_L3N AK18 — LVDS_L_DATA_N<3>

MONITOR IDENTIFICATION:
- DDC1CLK AH23 — GPU_DDC_A_CLK
- DDC1DATA AH22 — GPU_DDC_A_DATA
- DDC2CLK AG13 — GPU_DDC_B_CLK
- DDC2DATA AH13 — GPU_DDC_B_DATA
- DDC3CLK AF12 — GPU_DDC_C_CLK
- DDC3DATA AE12 — GPU_DDC_C_DATA

75 GPU_HPD

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

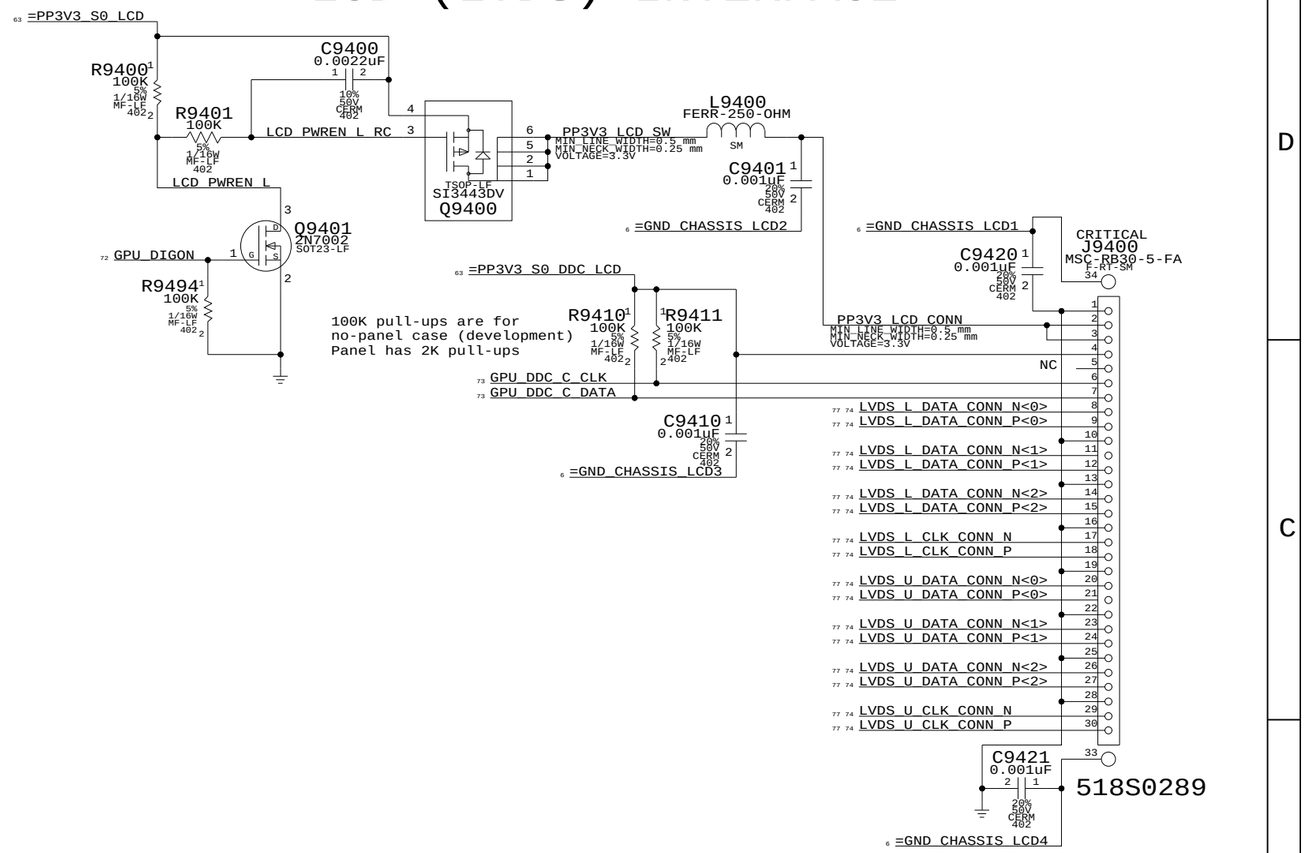
SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE: NONE

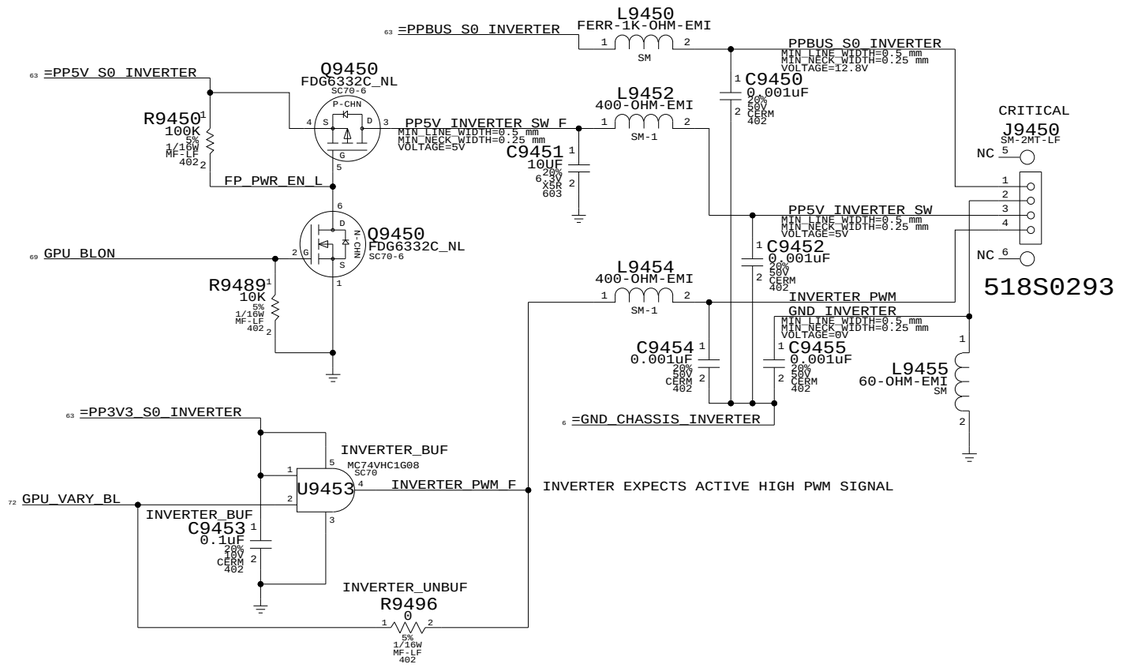
SHT 93 OF 104

LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 77
	LVDS	LVDS	LVDS_U_CLK_N	73 77
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 77
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 77
	LVDS	LVDS	LVDS_L_CLK_P	73 77
	LVDS	LVDS	LVDS_L_CLK_N	73 77
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 77
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 77
	LVDS	LVDS	LVDS_U_CLK_CONN_P	74 77
	LVDS	LVDS	LVDS_U_CLK_CONN_N	74 77
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	74 77
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	74 77
	LVDS	LVDS	LVDS_L_CLK_CONN_P	74 77
	LVDS	LVDS	LVDS_L_CLK_CONN_N	74 77
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	74 77
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	74 77
	TMDS	TMDS	TMDS_CLK_P	73 75 79
	TMDS	TMDS	TMDS_CLK_N	73 75 79
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 79
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 79
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 79



INVERTER INTERFACE



Internal Display Connectors

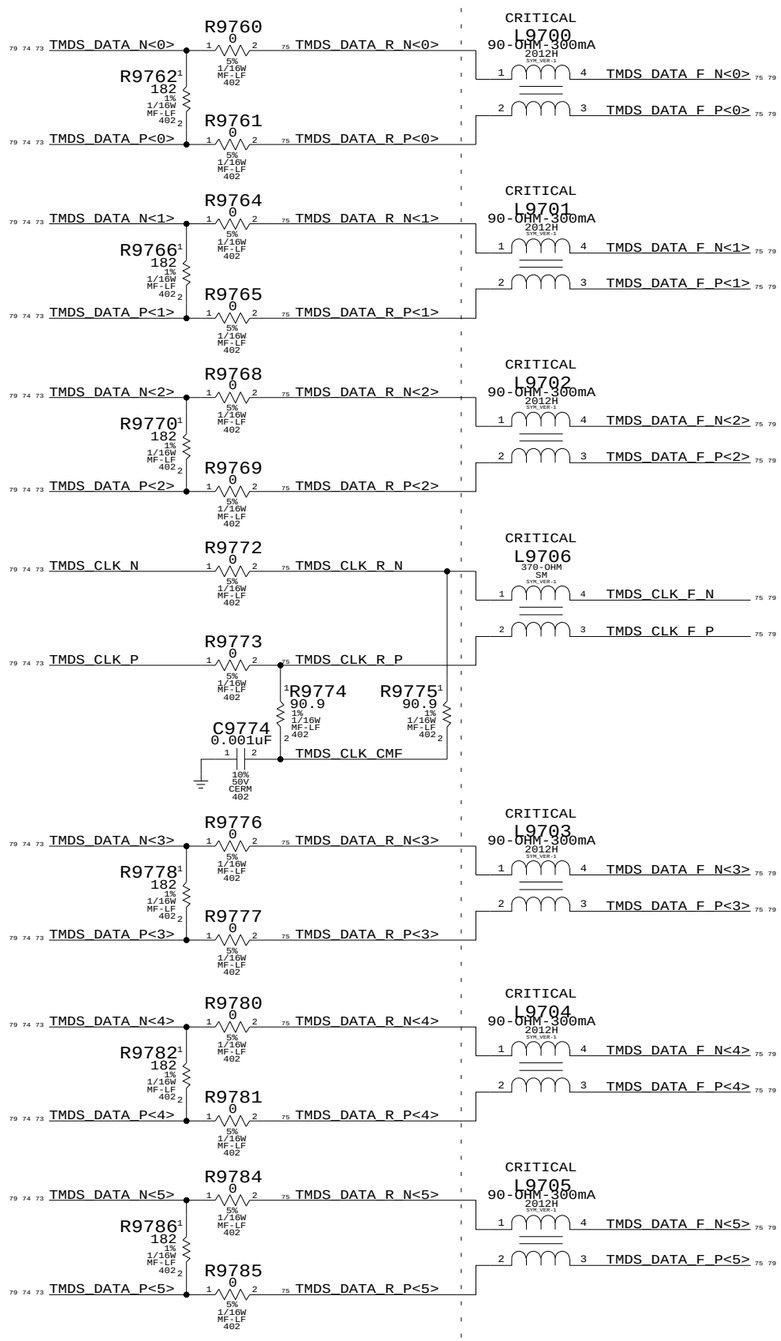
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

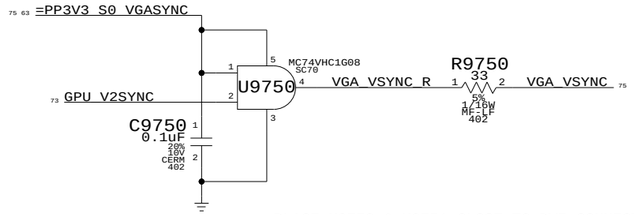
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 94 OF 104	

TMDS Filtering

Place series R's and common-mode filtering close to GPU, common mode chokes near connector.



VGA SYNC BUFFERS



DVI INTERFACE

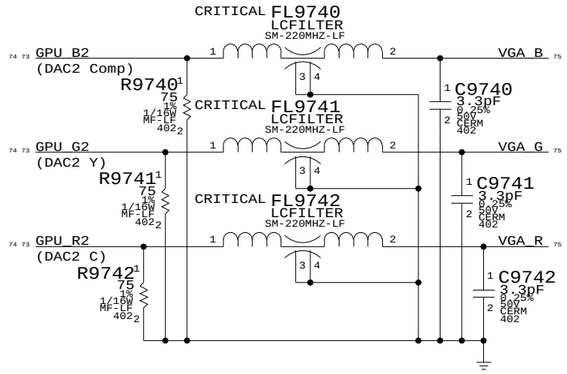
DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

Isolation required for DVI power switch

NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS_CLK_R_P
	TMDS	TMDS_CLK_R_N
	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDSCONN_CLK_F_P
	TMDSCONN	TMDSCONN_CLK_F_N
	TMDSCONN	TMDSCONN_DATA_F_P<5..0>
	TMDSCONN	TMDSCONN_DATA_F_N<5..0>

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



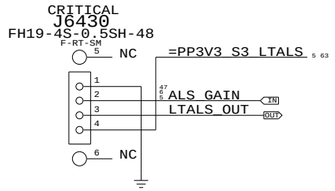
External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

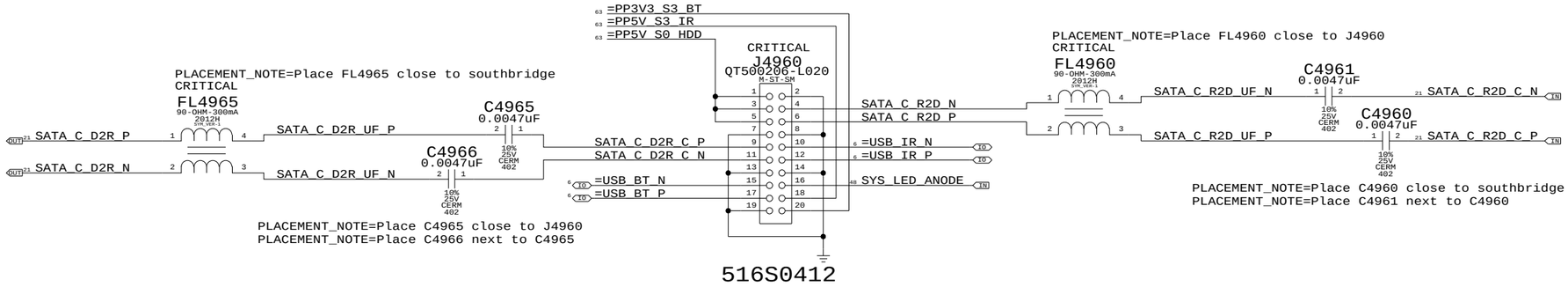
SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 97 OF 104	

Left ALS Connector



518S0395

Bluetooth (M13P), IR & SATA HDD Flex Connector



516S0412

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M1 Specific Connectors

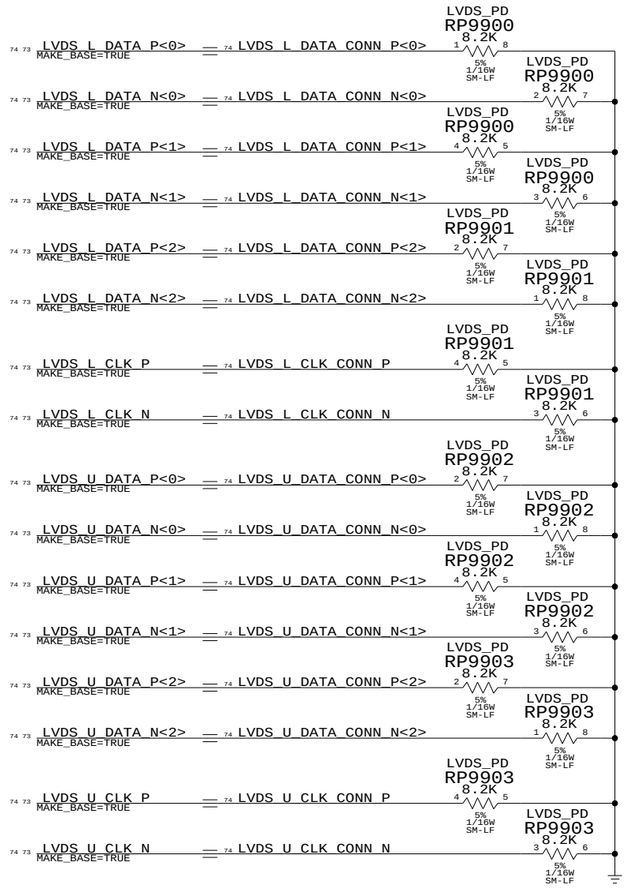
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE: NONE	SHT 98 OF 104	

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.



LVDS Interface Pull-downs

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D
SCALE	SHT	OF
NONE	99	104

Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42.
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
2005/09/19 - 4247941 - GND line/neck/voltage properties updated per PCB request.
2005/09/19 - 4235898 - Moved signal alias to improve schematic reuse.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/21 - 4227306 - Changed CPU VCore caps to proper production part number.
2005/09/21 - 4234952 - Replaced FDG6324L parts with FDG6332C for cost & supply.
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

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DMS Checkin #07001

2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.
2005/09/28 - 4278828 - Adjusted P5VS5_PGOOD R's, added cap on PM_RSMRST_L.
2005/09/29 - 4232826 - Swapped Vtt RPAK functions to free up unnecessary part.
2005/09/30 - 4261313 - Added placeholder connector for IR FFC connector.
2005/09/30 - 4282162 - Changed GPU BBN supply to MAX1673.
2005/09/30 - 4248911 - Sync with M38 & M42.
2005/09/30 - 4282349 - Added CRITICAL flags to parts identified in scrub.
2005/09/30 - 4274915 - C1001 stuffing change from Proto 2 MLB branch.

DMS Checkin #07002

2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.
2005/10/04 - 4261313 - Deleted placeholder connector, grew HDD connector for IR.
2005/10/04 - 4281394 - BOM option change to stuff right USB ESD protection part.
2005/10/06 - 4227330 - Added ESD protection on top-case USB port.
2005/10/07 - 4286888 - BOM restructuring per EVT build plan.
2005/10/07 - 4292633 - Changed IMVP6 10K NTC from 10% to 5% part.
2005/10/07 - 4248911 - Sync with M38 & M42.

DMS Checkin #07003

2005/10/08 - 4214493 - Simplified FireWire port power circuit for BOM consolidation.
2005/10/08 - 4293072 - Various BOM / connection changes at IMVP6 (CPU VCore).
2005/10/08 - 4286729 - Changed value of TPM Xtal caps.
2005/10/08 - 4290735 - Swapped trackpad & PCIe Mini Card USB connections.
2005/10/09 - 4235898 - Part moves & refdes changes to support sync with M9.
2005/10/09 - 4214494 - Changed GPU VCore supply enable to use 1.2V/2.5V S3 PGOODs.
2005/10/09 - 4272237 - Changed 2.5V S0 FET RC to 100K to slow down turn-on.

DMS Checkin #07004

2005/10/10 - 4232826 - Swapped Vtt RPAK functions to optimize layout.
2005/10/10 - 4247941 - Net property updates found via back-annotation.

DMS Checkin #07005

2005/10/10 - 4229560 - Removed Physical Security circuitry.
2005/10/10 - 4214493 - Cost reductions to GPU power supply circuitry.
2005/10/10 - 4214847 - Changed 0-ohm resistor to solder jumper.
2005/10/10 - 4248911 - Sync with M38 & M42.
2005/10/10 - 4295280 - Changed sleep LED connection per new SMC ERS.

DMS Checkin #07006

2005/10/11 - 4261313 - Updated SATA connector pinout to match latest flex.
2005/10/11 - 4227308 - Deleted unnecessary MCH TVDAC filtering.
2005/10/11 - 4229560 - Changed SB GNT3#/GNT4# back to test points.
2005/10/12 - 4248911 - Sync with M38 & M42.
2005/10/12 - 4298899 - Changed stuffing option to disable PLT_RST gating.
2005/10/12 - 4297684 - Split FW323 VSSA from VSS to reduce noise.
2005/10/12 - 4223808 - Power supply changes per vendor feedback.
2005/10/12 - 4227320 - Updated SB pin name for GPIO 5 (ODD_PWR_EN_L).
2005/10/12 - 4244539 - Retasked FET to control 3.3V S0 FET from GPU VCore PGOOD.
2005/10/12 - 4247941 - Added properties to resolve a PCB constraint issue.
2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.
2005/10/12 - 4298905 - Changed ethernet VMAIN_AVLBL connection.
2005/10/12 - 4298943 - Replaced last remaining non-RoHS compliant connector.
2005/10/12 - 4214494 - Implemented circuit to power down ethernet in S3 on battery.

DMS Checkin #07007

2005/10/13 - 4247941 - Swapped pins at trackpad ESD protection diode.

DMS Checkin #07008

2005/10/13 - 4247941 - Unswapped pins at trackpad ESD protection diode.

DMS Checkin #07009

2005/10/13 - 4247941 - Removed NO_TEST properties from CPU FSB strobe signals.
2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.
2005/10/14 - 4247941 - Restored NO_TEST properties, added EXPOSED_VIA properties.
2005/10/17 - 4292633 - Changed remaining 10K NTCs to new 5% part.
2005/10/17 - 4304248 - Updated GPU VCore / BBP voltages for B13/B24 support.

DMS Release #08000-11000 (EVT releases)

2005/10/20 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/10/21 - 4310267 - Synced 3 pages from mlb_evt branch back to trunk.
2005/10/21 - 4235898 - Synced 2 pages from m9/mlb.
2005/10/26 - 4310267 - Synced 4 pages from mlb_evt branch back to trunk.
2005/11/03 - 4310267 - Synced 6 pages from mlb_evt branch back to trunk.
2005/11/15 - 4310267 - Synced 5 pages from mlb_evt branch back to trunk.
2005/11/15 - 4298899 - Removed unused platform reset gate.
2005/11/15 - 4322537 - Updated thru-hole SO-DIMM connector part number.
2005/11/16 - 4345498 - Updated Ethernet & FireWire crystal part numbers.
2005/11/16 - 4235898 - Aliased connection to ALS_GAIN to support M9 request.
2005/11/16 - 4235898 - Changed Yukon power rail neck widths per M9 request.
2005/11/16 - 4227333 - Updated SMC net names per ERS v1.2.1.
2005/11/16 - 4345921 - FUNC_TEST updates per test team request.
2005/11/16 - 4346006 - Updated J5500 pinout to match updated LIO board pinout.
2005/11/16 - 4343202 - Changed USB overcurrent switch to TPS2051B, added OC* RC.
2005/11/16 - 4346184 - Inserted common-mode chokes on SATA R2D/D2R pairs.

DMS Checkin #11001

2005/11/16 - 4235898 - Sync with M38 & M42.
(11.1.0) 2005/11/16 - 4298899 - Fixed ethernet reset net name on page 26.
(11.2.0) 2005/11/16 - 4227333 - Fixed single-pin nets caused by SMC net name updates.
2005/11/18 - 4235898 - Changed R4210 package size per M9 request.
(11.3.0) 2005/11/18 - 4235898 - Changed C9710 GND connection per M9 request.
2005/11/19 - 4346184 - Fixed location of SATA R2D common-mode choke.
2005/11/19 - 4347717 - Changed SMS self-test pull-up to pull-down.
2005/11/19 - 4350840 - Simplified TMDS filtering to allow movement of filter.
2005/11/19 - 4229560 - Changed FW chip back to REQ/GNT3.
2005/11/19 - 4350849 - Added option to connect SB_GPIO30 to ENET_LOM_DIS_L.
2005/11/19 - 4340256 - Changed topcase flex trackpad power from 3.3V to 5V.
(11.4.0) 2005/11/19 - 4292165 - Refreshed schematic symbol for U3750 (library update).

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DMS Checkin #11002

2005/11/21 - 4351196 - Added 1K pull-down on IDE_RESET_L.
(11.5.0) 2005/11/21 - 4343202 - Changed RC value and net name for USB OC.
2005/11/22 - 4350840 - Swapped TMDS termination components for placement.
2005/11/22 - 4352020 - Changed 2.5V S3 supply inductor & compensation values.
(11.6.0) 2005/11/28 - 4347845 - Added pull-down resistors on LVDS interface.
(11.7.0) 2005/11/30 - 4227340 - Removed CPU VCore current sense input RC.
2005/11/30 - 4331670 - Added CRITICAL flags to some more parts.
2005/11/30 - 4343864 - Added EMI/ESD parts at camera connector.
2005/11/30 - 4351181 - Changed ITP connector BOM option.
2005/11/30 - 4351196 - Changed IDE_RESET_L pull-down from 1K to 15K.
2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.
2005/12/01 - 4362404 - Changed TMDS diff term from 100-ohm to 180-ohm.
2005/12/01 - 4352020 - Changed 2.5V supply inductor to RoHS-compliant part.
2005/12/01 - 4227340 - Changed supply for 1.8V S3 current sense amp.
2005/12/01 - 4362566 - Restructured BOM for thick/thin PCB versions.
2005/12/01 - 4347845 - RPAK pinswaps to LVDS pull-downs for PCB layout.
(11.8.0) 2005/11/30 - 4358831 - Added pull-downs on two SB-to-SMC signals.
(11.9.0)

DMS Checkin #11003

2005/12/02 - 4256256 - Added BOMOPTION to R8801 to allow per-project control.
2005/12/02 - 4363848 - Removed M56 GPU die rev B13 support from BOM.
2005/12/02 - 4363870 - Removed M1a support from BOM.
2005/12/02 - 4217524 - Updated part number for J6430.
(11.10.0)

DMS Release #12000-13000 (DVT releases)

2005/12/07 - 4375840 - Synced 4 pages from mlb_dvt branch back to trunk.
2005/12/12 - 4235898 - Changes to LVDS net names to support mux option.
2005/12/12 - 4362451 - Added MAKE_BASE=TRUE to SMC 32KHz SUSCLK net.
2006/01/03 - 4375840 - Synced 1 page from mlb_dvt branch back to trunk.
2006/01/03 - 4290282 - Removed BOM table, changed L9455 to 155S0002.
2006/01/03 - 4347845 - Changed LVDS pull-downs from 10K to 8.2K.
2006/01/03 - 4391436 - Swapped N/P signal names on one portion of SATA_R2D.
2006/01/03 - 4362451 - Changed SCH/PCB/BOM part descriptions for Rev A.
(13.1.0) 2006/01/03 - 4362451 - Removed power jumpers and 0-ohm resistor.
2006/01/05 - 4362566 - Removed 920- number for thin PCB option.
2006/01/05 - 4394079 - Added BOMOPTION to SYS_ONEWIRE pull-up.
2006/01/05 - 4362451 - Removed power jumpers and 0-ohm resistor.
2006/01/05 - 4362451 - Restructured BOM tables to eliminate LeMenu.
2006/01/06 - 4402184 - Changed R7540 value for IMVP6 load-line improvement.
2006/01/06 - 4362451 - Added System Block Diagram, updated Power Diagram.
2006/01/06 - 4362451 - Changed BOM options for production SMC, BootROM.

DMS Release #A000 (PVT Release)

2006/01/21 - 4412882 - Changed R7623 from 1.33K to 931 ohms.
(A.1.0) 2006/01/21 - 4414757 - Changed 138S0552 to 138S0580 & 138S0553 to 138S0581.
2006/01/26 - 4420815 - Changed 2x 128S0077 to 128S0068.
(B.0.0)

DMS Release #B000 (PVT BOM Update)

2006/02/09 - 4440116 - Pulled new schematic part number (051-7099).
2006/02/09 - 4440116 - Restructured BOM for 3 CPU configs.
2006/02/09 - 4440116 - Updated BootROM / SMC part numbers.
(A.0.0)

DMS Release #A000 (Ramp Config Update)

2006/02/13 - 4420815 - Changed remaining 128S0077 to 128S0086.
2006/02/13 - 4420815 - Added 128S0077 as alternate for 128S0086.
2006/02/13 - 4437189 - Changed R7757 to 1Mohm & R7770 to 100K.
(A.1.0) 2006/02/13 - 4431947 - Removed NO STUFF option from C3309.
(B.0.0)

DMS Release #B000 (PVT BOM Roll-In)

2006/02/17 - 4449123 - Changed C7537: 4.7nF -> 47pF, R7537: 3.57K -> 4.42K.
(C.0.0)

DMS Release #C000 (Ramp BOM Update)

2006/03/03 - 4457745 - Added 128S0094 & 128S0095 as alternates for 128S0060.
2006/03/03 - 4457801 - Added 128S0081 as alternate for 128S0061.
2006/03/03 - 4466770 - Changed R7920 from 5% to 1% to reduce variation.
2006/03/03 - 4399085 - Changed C7532 from 10nF to 15nF to slow CPU slew rate.
2006/03/03 - 4424175 - Changed 8 VRAM strap resistors to enable ICT testing.
(D.0.0)

DMS Release #D000 (Ramp BOM Update)

D

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE NONE SHT 100 OF 104

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 57
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	57
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 79
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 79
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 57
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	57
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	57

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 45
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 45
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 45

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7099	D

SCALE	SHT	OF
NONE	104	104