**Table of Contents**

<table>
<thead>
<tr>
<th>Page</th>
<th>Contents</th>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Table of Contents</td>
<td>N/A</td>
</tr>
<tr>
<td>2</td>
<td>System Block Diagram</td>
<td>N/A</td>
</tr>
<tr>
<td>3</td>
<td>BOM Configuration</td>
<td>N/A</td>
</tr>
<tr>
<td>4</td>
<td>Functional VCC Test</td>
<td>N/A</td>
</tr>
<tr>
<td>5</td>
<td>Signal Aliases</td>
<td>N/A</td>
</tr>
<tr>
<td>6</td>
<td>CPU 1 OF 2-PDB</td>
<td>M42</td>
</tr>
<tr>
<td>7</td>
<td>CPU 2 OF 2-PDB</td>
<td>M42</td>
</tr>
<tr>
<td>8</td>
<td>CPU Decoupling &amp; VID</td>
<td>N/A</td>
</tr>
<tr>
<td>9</td>
<td>CPU M38 SP INI 38</td>
<td>M42</td>
</tr>
<tr>
<td>10</td>
<td>CPU INI 38 DEBUG</td>
<td>M42</td>
</tr>
<tr>
<td>11</td>
<td>NB CPU Interface</td>
<td>N/A</td>
</tr>
<tr>
<td>12</td>
<td>NB PCI / Video Interfaces</td>
<td>N/A</td>
</tr>
<tr>
<td>13</td>
<td>NB Misc Interfaces</td>
<td>N/A</td>
</tr>
<tr>
<td>14</td>
<td>NB DDR2 Interfaces</td>
<td>M42</td>
</tr>
<tr>
<td>15</td>
<td>NB Power 1</td>
<td>N/A</td>
</tr>
<tr>
<td>16</td>
<td>NB Power 2</td>
<td>N/A</td>
</tr>
<tr>
<td>17</td>
<td>NB Grounds</td>
<td>N/A</td>
</tr>
<tr>
<td>18</td>
<td>NB (DRM) Decoupling</td>
<td>M42</td>
</tr>
<tr>
<td>19</td>
<td>NB Config Straps</td>
<td>M42</td>
</tr>
<tr>
<td>20</td>
<td>NB Misc</td>
<td>N/A</td>
</tr>
<tr>
<td>21</td>
<td>NB Misc</td>
<td>N/A</td>
</tr>
<tr>
<td>22</td>
<td>NB Misc</td>
<td>N/A</td>
</tr>
<tr>
<td>23</td>
<td>NB Misc</td>
<td>N/A</td>
</tr>
<tr>
<td>24</td>
<td>DR Misc</td>
<td>N/A</td>
</tr>
<tr>
<td>25</td>
<td>DR Misc</td>
<td>M42</td>
</tr>
<tr>
<td>26</td>
<td>M1 SMBus Connections</td>
<td>N/A</td>
</tr>
<tr>
<td>27</td>
<td>DDR2 32-DIMM Connector A</td>
<td>N/A</td>
</tr>
<tr>
<td>28</td>
<td>DDR2 32-DIMM Connector B</td>
<td>N/A</td>
</tr>
<tr>
<td>29</td>
<td>Memory Active Termination</td>
<td>N/A</td>
</tr>
<tr>
<td>30</td>
<td>Memory Vcc Supply</td>
<td>N/A</td>
</tr>
<tr>
<td>31</td>
<td>DDR2 2X8 Connector</td>
<td>N/A</td>
</tr>
<tr>
<td>32</td>
<td>CLKGEN</td>
<td>M42</td>
</tr>
<tr>
<td>33</td>
<td>Clock Termination</td>
<td>N/A</td>
</tr>
<tr>
<td>34</td>
<td>Mobile Clocking</td>
<td>N/A</td>
</tr>
<tr>
<td>35</td>
<td>PATA Connector</td>
<td>M42</td>
</tr>
<tr>
<td>36</td>
<td>Ethernet Connector</td>
<td>N/A</td>
</tr>
<tr>
<td>37</td>
<td>FIREWIRE CONTROLLER</td>
<td>M42</td>
</tr>
<tr>
<td>38</td>
<td>FIREWIRE CONTROLLER</td>
<td>M42</td>
</tr>
</tbody>
</table>

**Revision History**

- **09/26/2005**
- **07/26/2005**
- **07/20/2005**
- **09/08/2005**

**NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

**NOT TO REPRODUCE OR COPY IT**
NOTICE OF PROPRIETARY PROPERTY

I. AGREES NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
II. AGREES NOT TO REPRODUCE OR COPY IT
III. AGREES TO MAINTAIN THE DOCUMENT IN CONFIDENCE

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR OF THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

REV. 
implements System Block Diagram
to Apple Computer Inc.

SYNC_DATE=N/A
SYNC_MASTER=N/A

07001
2
81
www.laptop-schematics.com

2 81
051-6941
www.laptop-schematics.com

www.laptop-schematics.com

www.laptop-schematics.com
<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>BOM</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>1</td>
<td>VRAM_128</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>343S0385</td>
<td>1</td>
<td>IC, EEPROM</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>353S1235</td>
<td>1</td>
<td>IC, FW</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>333S0350</td>
<td>4</td>
<td>IC, ATI M56</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IC, TPM</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>075-0140</td>
<td>1</td>
<td>IFX_HILITE</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>075-0140</td>
<td>1</td>
<td>IFX_HILITE</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>075-0139</td>
<td>1</td>
<td>IFX_HILITE</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Phantom BOM #1's**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>BOM</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>1</td>
<td>VRAM_128</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>343S0385</td>
<td>1</td>
<td>IC, EEPROM</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>353S1235</td>
<td>1</td>
<td>IC, FW</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>333S0350</td>
<td>4</td>
<td>IC, ATI M56</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Module Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>BOM</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>1</td>
<td>VRAM_128</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>343S0385</td>
<td>1</td>
<td>IC, EEPROM</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>353S1235</td>
<td>1</td>
<td>IC, FW</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>333S0350</td>
<td>4</td>
<td>IC, ATI M56</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IC, TPM</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>075-0140</td>
<td>1</td>
<td>IFX_HILITE</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>075-0140</td>
<td>1</td>
<td>IFX_HILITE</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>075-0139</td>
<td>1</td>
<td>IFX_HILITE</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**LeMenu Stage #1 Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>1</td>
<td>U8900,U8950,U9000,U9050</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>343S0385</td>
<td>1</td>
<td>IC, EEPROM</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>353S1235</td>
<td>1</td>
<td>IC, FW</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>333S0350</td>
<td>4</td>
<td>IC, ATI M56</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IC, TPM</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

**LeMenu Stage #2 Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>1</td>
<td>U8900,U8950,U9000,U9050</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>343S0385</td>
<td>1</td>
<td>IC, EEPROM</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>353S1235</td>
<td>1</td>
<td>IC, FW</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>333S0350</td>
<td>4</td>
<td>IC, ATI M56</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IC, TPM</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

**LeMenu Stage #3 Parts**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>333S0354</td>
<td>1</td>
<td>U8900,U8950,U9000,U9050</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>343S0385</td>
<td>1</td>
<td>IC, EEPROM</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>353S1235</td>
<td>1</td>
<td>IC, FW</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td>333S0350</td>
<td>4</td>
<td>IC, ATI M56</td>
<td>CRITICAL</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>IC, TPM</td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>
TCK PULL DOWN THROUGH 54.9 OHM (FOLLOW UP XDP DESIGN REFERENCE)

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50

CHANGE THE PULL RESISTOR VALUE PER NASA PLATFORM DG REV 0.9

MS THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE ITP FULL UP THRU 54.9 OHM THE PULL UP THRU 54.9 OHM
TCK PULL DOWN THRU 54.9 OHM (FOLLOW UP XDP DESIGN REFERENCE)

CPU I OF 2-FSB

REMARKS OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.
CPU VCORE HF AND BULK DECOUPLING

- CPU VCORE HF Decoupling
  - 4x 470uF, 20x 22uF 0805

VCCA (CPU AVdd) Decoupling

- 1x 10uF, 1x 0.01uF

VCCP (CPU I/O) Decoupling

- 1x 470uF, 6x 0.1uF 0402
- 4x 470uF, 20x 22uF 0805

NOTE: This cap is shared between CPU and NB.
CPU ZONE THERMAL SENSOR

PLACE U1001 NEAR THE U1200

ADD GND GUARD TRACE

ROUTE CPU_THERMD_P AND CPU THERMD_N ON SAME LAYER.

10 MIL TRACES

LAYOUT NOTE:

CPU_THERMD_N (TO CPU INTERNAL THERMAL DIODE)

LAYOUT NOTE:

C1002 X5R 0.1UF 16V 10%

R1002 499 1% MF-LF 1/16W

C1001 NOSTUFF CERM 50V 0.001uF 10%

R1005 1/16W 5% 10K MF-LF

R1006 10K 1/16W MF-LF 5%

051-6941 07001

SYNC_MASTER=M42

SYNC_DATE=09/08/2005

CPU MISC1-TEMP SENSOR
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL layout note:
Route the TCK signal from ITP700FLEX Connector's TCK pin to CPU's TCK pin and then fork back from CPU TCK pin and route back to ITP700FLEX Connector's FBO pin.
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core.

Unused DAC outputs must remain powered, but can omit TV-Out Disable.

Connect to GND through 75-ohm resistors. TV-Out Signal Usage:

Component: DACA, DACB & DACC

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.

Otherwise, tie VCCD_LVDS to GND also.
NCTF balls are not critical to function.

These connections can break without impacting part performance.

---

Notice of proprietary property:

The reproduction or distribution of this material is the exclusive right of Apple Computer, Inc. and is subject to the following conditions:

1. To reproduce or distribute this material in any form or by any means.
2. To reproduce or distribute this material in whole or in part.

Therefore, no reproduction, distribution, or any other use of this material is permitted without the prior written consent of Apple Computer, Inc.

NOTE TO REPRODUCE OR COPY IT

TIENDA DE ALAMBRICOS

www.laptop-schematics.com

APPLE COMPUTER INC.

D 051-6941 07001

061-6941 81
NOTE: ENABLE INTERNAL 1.5V SUSPEND REG

NOTE: ELICIC INTERNAL 20K PD ENABLED WHEN
INTERNAL 20K PD
- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED

NOTE: INTO RESET STATE TO SAVE PWR.

NOTE: ENABLE INTERNAL 1.05V SUSPEND REG

NOTE: All IDE pins have internal 33-ohm series R's

NOTE: All ACZ pins have internal 11.5k ohm PD

NOTE: All ACZ pins have internal 11.5k ohm PD

NOTE: All IO pins have internal 33-ohm series R's

LBIC_RD
- Internal IO pins on board
- IO pins on board

LBIC_WR
- Internal IO pins on board
- IO pins on board

LBIC_RST
- Internal IO pins on board
- IO pins on board

LBIC_CSP
- Internal IO pins on board
- IO pins on board

LBIC_LCD
- Internal IO pins on board
- IO pins on board

LBIC Định
- Internal IO pins on board
- IO pins on board

LBIC_LCD
- Internal IO pins on board
- IO pins on board

LBIC Định
- Internal IO pins on board
- IO pins on board
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure C1_L and C2_T resistors are close to SD-DIMM connector.
TPM Crystal Circuit

SMC G3Hot Oscillator

Mobile Clocking

NOTICE OF PROPRIETARY PROPERTY

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

III NOT TO REPRODUCE OR COPY IT

AGREES TO THE FOLLOWING

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

The information contained herein is the proprietary

www.laptop-schematics.com
Should get the page updated.

IDE (ODD) Connector

Indicates disk presence

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=5V

PP5V_S0_IDE_ODD
PP3V3_S0_IDE

IDE (ODD) Connector

IDE PDDREQ
IDE PDD<1>
IDE PDD<5>
IDE PDD<6>
IDE PDD<7>
IDE PDD<0>
IDE PDD<3>
IDE PDD<4>
IDE PDDACK_L
IDE PDCS3_L
IDE_IRQ14
IDE PDA<0>
IDE PDA<1>
IDE PDA<2>
IDE_RESET_L

SMC_ODD_DETECT
Indicates disk presence

IDE PDD<9>
IDE PDD<8>
IDE PDD<11>
IDE PDD<10>
IDE PDD<12>
IDE PDD<13>
IDE PDD<14>
IDE PDD<15>

SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
NOTICE OF PROPRIETARY PROPERTY
APPLE COMPUTER INC.
II NOT TO REPRODUCE OR COPY IT
PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR TO MAINTAIN THE DOCUMENT IN CONFIDENCE
Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformer.

Short shielded RJ-45.
Port Power Switch

FireWire Port Current Sense

- =PP3V3_S0_FWPORTPWRSW (system supply for bus power)
- =FWPWR_PWRON (see related text note below)

**Power aliases required by this page:**
- =PPBUS_S0_FWPWRSW

**Signal aliases required by this page:**
- =PPBUS_S5_FWPWRSW_F

**BOM options provided by this page:**
(NONE)

**Signal notes provided by this page:**

**Page Notes**

- Critical Signal: Use critical components for these signals.

**Power notes required by this page:**

- Power: Use power components for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.

**Component notes required by this page:**

- Component: Use specific components for these signals.

**Text notes required by this page:**

- Text: Use specific text for these signals.
GPU / Heat Pipe Thermal Sensor

Right-Side/Fin Stack Thermal Sensor

CPU Back-Up Thermal Diode

**Placement note:**
- CPU Back-Up Thermal Diode: Place near speaker hole.
- GPUTHMSNS_DX_A_DIO_N: Place in between VRAM.
- GPUTHM_A_GPU: Minimize stubs between these R's and R1001 & R1002.
- GPUTHM_A_DIAG: Keep all 4 XWs as close to each other as possible.

**Part Number:**
- 518S0226
- XW6121
- XW6120
- XW6111
- XW6110

**Description:**
- RSFSTHMSNS_D_R_N
- GPUTHMSNS_DX_A_DIO_N
- HSTHMSNS_DX_P
- HSTHMSNS_DX_N

**Reference Design:**
- ADT7461
- MAX6695AUB

**Critical:**
- 1%
- 5%

**Outline:**
- 518S0226
- X5R402
- 0.0022uF
- 10%16V

**BOM Option:**
- R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.
R6309 is not needed when sharing SPI flash with ICH7M and TEGRA(LAN CHIP).

R6307 and R6306 should be placed less than 100 MILS from ICH7M.

R6303 should be placed less than 100 MILS from Flash ROM.

C6311
50V 5%
402 CERM
22PF
2
1
R6306
1/16W
5%
402 MF-LF
3.3K
2
1
R6307
402 MF-LF
1/16W
5%
47
2
1
C6308
50V 5%
402 CERM
22PF
2
1
C6309
50V 5%
402 CERM
22PF
2
1
C6301
50V 5%
402 CERM
22PF
2
1
R6301
1/16W
5%
402 MF-LF
3.3K
2
1
R6302
1/16W
5%
402 MF-LF
3.3K
2
1
R6303
1/16W
5%
402 MF-LF
47
2
1
C6301
50V 5%
402 CERM
22PF
2
1
R6306
1/16W
5%
402 MF-LF
47
2
1
R6307
402 MF-LF
1/16W
5%
47
2
1
C6312
50V 5%
402 CERM
22PF
2
1
R6309
1/16W
5%
402 MF-LF
10K
2
1
R6308
1/16W
5%
402 MF-LF
10K
2
1
C6302
50V 5%
402 CERM
22PF
2
1
R6304
1/16W
5%
402 MF-LF
10K
2
1
U6301
WSON
SST25VF016B
16MBIT
OMIT

www.laptop-schematics.com
Left ALS "Connector"

Right ALS Circuit

Keyboard LED Driver

ALS Support
PAGE NOTES

INPUT

- SMS_ONOFF_L - 3.3V POWER FOR SMS (STATE ALIVE IN SLEEP)

OUTPUT

- SMS_ACC_SELFTEST - SHOULD BE PULLED HIGH WHEN NOT USED

PAGE HISTORY

+Y (Placed on board topside)

+Z (up)

+X

INPUT

SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

OUTPUT

SMS_X_AXIS

SMS_Y_AXIS

SMS_Z_AXIS

SMS_X_AXIS

SMS_Y_AXIS

SMS_Z_AXIS

SMS_X_AXIS

SMS_Y_AXIS

SMS_Z_AXIS

Desired Orientation

(Placed on board topside)

Package Top
Connect to RBBX pin to control outputs.
If disconnected, power up with VIN.

NOTE: Be aware of pull-ups to VIN on these signals.
3.425V "G3Hot" Supply

Supply needs to guarantee 3.3V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

Vout = 3.425

200mA max output (Switcher limit)

3.3V G3Hot Supply
NOTE: BBP tracks VDDC based on GPU voltage GPIO. When inactive, provides VDDC to BBP pins. Back-bias positive supply provides VDDC + 0.5V when active.

\[ \text{Vout(high)} = 0.6V \times (1 + \frac{Ra}{Req}) \]
\[ \text{Vout(low)} = 0.59V \times (1 + \frac{Ra}{Rb}) \]

\[ \text{Req} = Rb \parallel Rc \]

Vout = 1.0V / 1.00V
17A max output
(Q8520 limit)

Pull-up voltage must be high enough to satisfy BBF FET Vgs (where Vgs = 1.2V).

GPUBB_CTL
- GPU-desktop
- GPU mobile

GPU VCore Current Sense

Back-Bias Negative Supply

Max-bias negative supply provides VSS - 0.5V when active.
Most sensitive, requires close R8594 placement.

\[ \text{Vout} = -0.50V \]

Vout = 1.0A
150mA max output
(Inductor & IC current limit)

R8594 and R8597

GPU (M56) Core Supplies

Sync Date = (Master)
Secure Signal List

Note: Must be buried with no exposed via between parts listed in SECURE_NET property. No test points allowed between the secure devices, test points are allowed on 

SECURE_NET=U0700:U9950:Q9955
SECURE_NET=U9950:U5800
SECURE_NET=U5800:U7530
SECURE_NET=U2100:U5800
SECURE_NET=U2100:U5800
SECURE_NET=U2100:U5800
SECURE_NET=U2100:U5800

NO_TEST=TRUE, no test points are allowed on those nets.

Between the secure devices, test points are allowed listed in SECURE_NET property. No test points allowed.

Nets must be buried with no exposed vias between parts.

SMC <-> CPU JTAG Level-Shifting

All of these parts will be covered in epoxy.

Place these parts on one side and as close together as possible, and keep enough room from other parts to leave room for epoxy covering. Nets that are local to this circuit do not need test points as they will not be accessible.

Physical Security

Notice of Proprietary Property

For the exclusive use of ADDRESS PENDING IN WHOLE OR PART

McElroy, Inc.

For the exclusive use of APPLE COMPUTER, INC. THE POSSESSOR

To maintain the document in confidence

I to reproduce or copy it

II to request the document again

III to reproduce or copy it
DMS Checkin #04001
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4248911 - Sync with M38 & M42
2005/09/08 - 4245803 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/26 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/28 - 4217524 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.
2005/08/31 - 4227308 - Various power supply R/C updates, pin join R/C adds.
2005/08/31 - 4227310 - Changed SMBus pull-ups from 3.3V S0 to 3.3V S3.
2005/08/29 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/29 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/08/31 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/27 - 4227325 - Removed SMC options for display/backlight, now GPU-only.
2005/08/28 - 4217535 - Added pull-up for SB SPI122 (MSQ4).
2005/08/27 - 4227334 - Changed P02A1 5VDC rails, added NC for 3.3V S0.
2005/08/27 - 4227320 - Changed FW22 failure pick from 3.3V S0 to 3.3V S3.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/27 - 4235401 - Changed U5900 to resolve ROHS issue.
2005/08/28 - 4215763 - Added Left ALS connector (J4450).
2005/08/28 - 4215763 - OMITs and tables to change 3-pin WTB connector parts.
2005/08/27 - 4221973 - Added pull-up for SB SPI122 (MSQ4).
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/27 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
### FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_CLK</td>
<td>85_OHM_DIFF</td>
<td>85_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>CPU_DQS</td>
<td>85_OHM_DIFF</td>
<td>85_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>CPU_DATA</td>
<td>70_OHM_DIFF</td>
<td>55_OHM_SE</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

**NOTE:** Design Guide allows closer spacing if signal lengths can be shortened.

**PHYSICAL_RULE_SET**

- **MEM_CTRL2MEM**
- **MEM_DATA2MEM**
- **CPU_VCCSENSE**

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

Some signals require 27.4-ohm single-ended impedance. Design Guide recommends each module/signal group be routed on the same layer. The Design Guide recommends FSB signals be routed only on internal layers. 

**NOTE:** Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

### CPU Signal Constraints

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 74-ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.2.4 & 4.3

### DDR2 Memory Bus Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2_DQ</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>DDR2_DQ</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>DDR2_DQ</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

**NOTE:** Need to support MEM_*-style wildcards!

**PHYSICAL_RULE_SET**

- **MEM_DATA2MEM**
- **CPU_VCCSENSE**

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 6.2

### PCI-Express / DMI Bus Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMI_DATA</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>DMI_DATA</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>DMI_DATA</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 7.3, 9.2 & 10.3.2

### Disk Interface Constraints

- **SATA_100D**
- **USB2_90D**
- **DMI_100D**

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

### Audio Interface Constraints

- **AUDIOMEDIA**
- **MICROPHONE**
- **SPEAKER**
- **LINE OUT**
- **LINE IN**
- **MICROPHONE IN**
- **SPDIF IN**
- **SPDIF OUT**
- **SPEAKER IN**

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.9.3

### USB 2.0 Interface Constraints

- **60 m** minimum spacing 60 mils to clocks

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

### Internal Interface Constraints

- **SAME BOARD**
- **DIAG BOARD**
- **SMB**
- **SATA**
- **PCMCIA**
- **USB**
- **SPDIF**
- **SPEAKER**
- **MICROPHONE**
- **LINE OUT**
- **LINE IN**
- **MICROPHONE IN**
- **SPDIF IN**
- **SPDIF OUT**
- **SPEAKER IN**

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

### Clock Signal Constraints

<table>
<thead>
<tr>
<th>Signal</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_CLKC</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>CPU_CLKC</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>CPU_CLKC</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 6.2

**SOURCE:** www.laptop-schematics.com
**Video Signal Constraints**

- **LVDS** and **TMDS** pairs should be kept at least 25 mils apart.
- **CTRL** lines are 55-ohm single-ended impedance.

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

- VGA signals should be kept at least 15 mils from other traces.
- Ground shields can be used around each pair if spacing cannot be met.

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

**NOTE:** CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.

- **DQ/DQM/DQS** lines are 40-ohm single-ended impedance.

**High-Speed I/O Interface Constraints**

- **PCI** bus constraints are specified in Layout Guide as 55-ohm differential, unless otherwise noted.

**PCI** bus constraints are specified in Layout Guide as 55-ohm differential, unless otherwise noted.

**More System Constraints**

- **ENET** and **PCI** signals are specified in Layout Guide as 55-ohm differential, unless otherwise noted.

**NOTE:** Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close".

**PHYSICAL RULE SET**

- **TMDS**, **LVDS**, **VGA**

**TABLE SPACING RULE**

- **TMDS_PAIR2PAIR**, **LVDS_PAIR2PAIR**, **VGA_PAIR2PAIR**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM LINE WIDTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
</tr>
</tbody>
</table>

**TABLE PHYSICAL RULE**

- **ENET**, **PCI**, **GDDR3** (Frame Buffer) Memory Bus Constraints

**TABLE SPACING ASSIGNMENT**

- **TMDS**, **LVDS**, **VGA**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>55_OHM_SE</td>
<td>100_OHM_DIFF</td>
</tr>
</tbody>
</table>

**TABLE PHYSICAL RULE**

- **ENET**, **PCI**

**TABLE SPACING ASSIGNMENT**

- **TMDS**, **LVDS**, **VGA**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>55_OHM_SE</td>
<td>100_OHM_DIFF</td>
</tr>
</tbody>
</table>

**TABLE PHYSICAL RULE**

- **GDDR3** (Frame Buffer) Memory Bus Constraints

**TABLE SPACING ASSIGNMENT**

- **TMDS**, **LVDS**, **VGA**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>55_OHM_SE</td>
<td>100_OHM_DIFF</td>
</tr>
</tbody>
</table>

**TABLE PHYSICAL RULE**

- **ENET**, **PCI**

**TABLE SPACING ASSIGNMENT**

- **TMDS**, **LVDS**, **VGA**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>55_OHM_SE</td>
<td>100_OHM_DIFF</td>
</tr>
</tbody>
</table>

**TABLE PHYSICAL RULE**

- **GDDR3** (Frame Buffer) Memory Bus Constraints

**TABLE SPACING ASSIGNMENT**

- **TMDS**, **LVDS**, **VGA**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>55_OHM_SE</td>
<td>100_OHM_DIFF</td>
</tr>
</tbody>
</table>

**TABLE PHYSICAL RULE**

- **ENET**, **PCI**

**TABLE SPACING ASSIGNMENT**

- **TMDS**, **LVDS**, **VGA**

<table>
<thead>
<tr>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>55_OHM_SE</td>
<td>100_OHM_DIFF</td>
</tr>
</tbody>
</table>