ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT 1/4%.
ALL CAPACITANCE VALUES ARE IN MICROFARADS.
ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Reference Design

1. Table of Contents
2. System Block Diagram
3. Power Block Diagram
4. BCM Configuration
5. Functional / ICT Test
6. Signal Aliases
7. CPU 1 OF 2-FSB
8. CPU 2 OF 2-FSB/GND
9. CPU Decoupling & VIO
10. CPU 82800-I/F DEBUG
11. NB CPU Interface
12. NB FSB / Video Interfaces
13. NB Misc Interfaces
14. NB DDR2 Interfaces
15. NB Power 1
16. NB Power 2
17. NB Grounds
18. NB Misc Decoupling
19. NB Core Power
20. NB Config Straps
21. SBI 2 OF 4
22. SBI 3 OF 4
23. SBI 4 OF 4
24. SBI Decoupling
25. SB Misc
26. SB MUSB Connections
27. DDR2 204-Pin Connector A
28. DDR2 204-Pin Connector B
29. Memory Active Termination
30. Memory VDD Supply
31. PLL Clocks
32. Clock Termination
33. Mobile Clocking
34. ATA Connector
35. Ethernet Connector
36. Yukon Power Control
37. FireWire Controller
38. FireWire Port Power
### BOM OPTION Groups

<table>
<thead>
<tr>
<th>BOM GROUP</th>
<th>ALTERTAT, COMMON, EEE COMMON, PCBA, M1, COMMON, COMMON, M1</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1, COMMON</td>
<td>ATN_REV, ENET, EEE, ENET, M1, COMMON, EEE, M1, COMMON, M1</td>
<td>BOM OPTIONS</td>
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<tr>
<td>M1, COMMON</td>
<td>EEEE, M1, COMMON, EEE, M1, COMMON, EEE, M1, COMMON</td>
<td>BOM OPTIONS</td>
</tr>
</tbody>
</table>

### Bar Code Label / EEE #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>630-7672</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>341S1789</td>
<td>1</td>
<td></td>
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</tr>
<tr>
<td>338S0315</td>
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<td>338S0268</td>
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<td>337S3267</td>
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<td>333S0358</td>
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<tr>
<td>826-4393</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VRAM_SAM256</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>VRAM_SAM128</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VRAM_HY256</td>
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</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
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<th>CRITICAL</th>
<th>BOM OPTION</th>
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<tbody>
<tr>
<td>337S3268</td>
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<td>337S3282</td>
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<td>333S0350</td>
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### Alternate Parts

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<th>BOM OPTION</th>
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<tbody>
<tr>
<td>330uF, 2V</td>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7mOhm</td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### BOM Configuration

- **BOM Number:** 051-7099
- **Revision:** H
- **Date:** 08/31/2001
- **Document Title:** BOM Configuration
- **Document Type:** Hardware Configuration
- **Department:** Engineering
- **Contact:** Support
- **Note:** This document is the property of Apple Computer, Inc. and is intended for internal use only.
**Power Supply NO_TESTS**

<table>
<thead>
<tr>
<th>Net</th>
<th>EXPOSED_VIA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tbody>
</table>

**CPU FSB NO_TESTS**

<table>
<thead>
<tr>
<th>Net</th>
<th>EXPOSED_VIA</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
</tr>
</tbody>
</table>

**Misc EXPOSED_VIA Nets**

<table>
<thead>
<tr>
<th>EXPOSED_VIA</th>
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</table>

**Functional Test Points**

**Fan Connectors**

<table>
<thead>
<tr>
<th>Net</th>
<th>FUNC_TEST</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Battery Digital Connector**

<table>
<thead>
<tr>
<th>Net</th>
<th>FUNC_TEST</th>
</tr>
</thead>
<tbody>
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<td></td>
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</tbody>
</table>

**LPC+ Debug Connector**

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<tr>
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<th>FUNC_TEST</th>
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<tbody>
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<td></td>
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**Left I/O Data Connector**

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<th>Net</th>
<th>FUNC_TEST</th>
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<tbody>
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</table>

**Left ALS Connector**

<table>
<thead>
<tr>
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<th>FUNC_TEST</th>
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</thead>
<tbody>
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</table>

**Camera Connector**

<table>
<thead>
<tr>
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<th>FUNC_TEST</th>
</tr>
</thead>
<tbody>
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<td></td>
</tr>
</tbody>
</table>

**Thermal Diode Connectors**

<table>
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<th>FUNC_TEST</th>
</tr>
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<tbody>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**Other Func Test Points**

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<thead>
<tr>
<th>Net</th>
<th>FUNC_TEST</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</table>

**Current Sense Calibration**

<table>
<thead>
<tr>
<th>Net</th>
<th>FUNC_TEST</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Functional / ICT Test**

<table>
<thead>
<tr>
<th>Net</th>
<th>FUNC_TEST</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

Note: EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTES:
- Route the TCK signal from ITP700FLEX connector's TCK pin to CPU's TCK pin and then fork back from CPU TCK pin and route back to ITP700FLEX connector's FBO pin.

CPU ITP700FLEX DEBUG SUPPORT

SYNC_DATE=10/12/2005
SYNC_MASTER=M42

www.laptop-schematics.com
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used, unused DAC outputs must remain powered with proper decoupling. Otherwise, tie VCC_LVDS to GND also.

**LVDS Disable**

Tie VCC_LVDS and VCCA_LVDS to GND, CRT_VSYNC_R, CRT_HSYNC_R, TV_DACB_OUT, TV_DACA_OUT, CRT_VSYNC, CRT_DDC_CLK, CRT_RED, CRT_GREEN, CRT_BLUE, CRT_DDC_DATA, CRT_GREEN*, CRT_BLUE*, CRT_VSYNC_R, CRT_HSYNC_R, SDVO_INT#, SDVO_FLDSTALL#, and SDVO_B# to GND also.

**CRT Disable**

Tie VCCD_LVDS to GND also.

**TV-Out Signal Usage**

- **Composite:** DACC only
- **Component:** DAC, DAC & DACC
- **TV-Out Disable:** Tie GND, CRT_VSYNC_R, CRT_HSYNC_R, and CRT to 1.0V power rail. Tie VSSA_CRTDAC and VCCA_LVDS to GND.
- **CRT Disable:** Tie CRT_VSYNC_R and CRT_HSYNC_R to 1.0V power rail. Tie VSSA_LVDS to GND.
- **LVDS Disable:** Tie VCC_TXLVDS and VCCA_LVDS to GND.

TV-Out Disable

- Tie GND, CRT_VSYNC_R, and CRT_HSYNC_R to 1.0V power rail. Tie VSSA_CRTDAC and VCCA_LVDS to GND.

CRT Disable

- Tie CRT_VSYNC_R and CRT_HSYNC_R to 1.0V power rail. Tie VSSA_LVDS to GND.

LVDS Disable

- Tie VCC_TXLVDS and VCCA_LVDS to GND.
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

LAYOUT NOTE:
1. PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE
2. OUT
3. IN
4. IO

OUT

IN

IO

=PP3V3_S5_SB

PCIE_WAKE_L

PM_STPCPU_L

SMC_EXTSMI_L

INT_SERIRQ

1K

MF-LF

402

5%

R2320

MF-LF

25

23

=PP3V3_S5_SB

=PP3V3_S5_SB

1

R2317

10K

402

2

R2316

10K

1/16W

R2314

R2307

R2306

10K

0

5%

402

R2318

10K

402

402

MF-LF

1/16W

SV_SET_UP

NOTE:

SV_SET_UP IS LINDACARD DETECT

NOTE:

INTEGRATED 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN

NOTE:

INET WEAK PD

NOTE:

INTERNATIONAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS

NOTE:

SYS_GPIO

NOTE:

SATA_GPIO

NOTE:

GPIO25

NOTE:

DEF=GPI

NOTE:

DEF=GPI

NOTE:

DEF=GPI

NOTE:

DEF=GPI

NOTE:

GPIO16/DPRSLPVR

NOTE:

GPIO11/SMBALERT*

NOTE:

GPIO32/CLKRUN*

NOTE:

GPIO33/AZ_DOCK_EN*
RTC Battery Connector

SB RTC Crystal Circuit

Platform Reset Connections

Unbuffered

Buffered

SB Misc

Initial resistor values are based on CRB, but may change after characterization.
"Lower" (surface-mount) slot
**NOTE:** This page does not supply VREF. The reference voltage must be provided by another page.

**BOM options provided by this page:**
- =PPSPD_S0_MEM (2.5V - 3.3V)
- =I2C_SODIMMB_SDA

---

### DDR2 Bypass Caps

(For return current)

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1μF 20% CERM 10V</td>
<td>1</td>
<td>0.1μF 20% CERM 10V</td>
</tr>
<tr>
<td>0.1μF 20% CERM 10V</td>
<td>1</td>
<td>0.1μF 20% CERM 10V</td>
</tr>
<tr>
<td>0.1μF 20% CERM 10V</td>
<td>1</td>
<td>0.1μF 20% CERM 10V</td>
</tr>
<tr>
<td>0.1μF 20% CERM 10V</td>
<td>1</td>
<td>0.1μF 20% CERM 10V</td>
</tr>
</tbody>
</table>

---

"Upper" (thru-hole) slot

---

**DDR2 SO-DIMM Connector**

- [Image of DDR2 SO-DIMM Connector with annotations]

---

**Page Notes**

Power output required by this page:
- Apple1_S0_MEM (±5V - ±3V)

Signal alignment required by this page:
- -DCDC_S0MEM_125

BOM options provided by this page:
- =PPSPD_S0_MEM (2.5V - 3.3V)
- =I2C_SODIMMB_SDA
One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure C2_L and C2_T resistors are close to ED-DIMM connector

Memory Active Termination

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WWW.LAPTOP-SCHMATICs.COM
Page Notes

- Power aliases required by this page:
  - VTT
  - VTT_IN
  - VREF
  - GND

- Signal aliases required by this page:
  - VDDQ
  - VCC

- BOM options provided by this page:
  - =PP5V_S0_MEMVTT
  - =PP1V8_S0_MEMVTT
  - =PP0V9_S0_MEMVTT

- DDR2 Vtt Regulator

- Memory Vtt Supply

- Page Notes

Okay to turn off 5V and leave 1.8V powered in S3.

DDR2 Vtt Regulator

If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

C3101

1

2

6.3V

20%

X5R

603

10uF

C3102

1

2

6.3V

X5R

603

10uF

C3103

1

2

10%16V

X5R

0.1uF

C3105

6.3V

SMC-LF

POLY

20%

150UF

R3100

1

2

MEMVTT_EN_PU

1K

402

MF-LF

1/16W

5%

R3104

12

220

5%

1/16W

MF-LF

402

C3100

1

2

6.3V

10%

1uF

CERM

402

C3104

1

2

CERM1

20%

6.3V

2.2uF

603

Memory Vtt Supply
Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformer.

Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:

BOM options provided by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Ethernet Connector
When ENETPWR_S3AC BOMOPTION is active:

<table>
<thead>
<tr>
<th>State</th>
<th>FWPWR_EN_L</th>
<th>PM_SLP_S4_L</th>
<th>PM_SLP_S3BATT</th>
<th>PM_SLP_S3BATT_L</th>
<th>P2V5S3_EN_L</th>
<th>P1V2S3_RUNSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Batt</td>
<td>PBUS</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
<td>0V (1.2V OFF)</td>
</tr>
<tr>
<td>S5 Batt</td>
<td>PBUS</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
<td>0V (1.2V OFF)</td>
</tr>
<tr>
<td>S5 AC</td>
<td>0V</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
<td>0V (1.2V OFF)</td>
</tr>
<tr>
<td>S3 Batt</td>
<td>PBUS</td>
<td>3.3V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>3.3V (2.5V OFF)</td>
<td>0V (1.2V OFF)</td>
</tr>
<tr>
<td>S3 AC</td>
<td>0V</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V</td>
<td>0V (2.5V ON)</td>
<td>3.3V (1.2V ON)</td>
</tr>
<tr>
<td>S0 Batt</td>
<td>0V</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V</td>
<td>0V (2.5V ON)</td>
<td>3.3V (1.2V ON)</td>
</tr>
<tr>
<td>S0 AC</td>
<td>0V</td>
<td>3.3V</td>
<td>0V (3.3V ON)</td>
<td>3.3V</td>
<td>0V (2.5V ON)</td>
<td>3.3V (1.2V ON)</td>
</tr>
</tbody>
</table>

Yukon Power Control

Allows powering Yukon down during battery sleep to save power.

Yukon Power Control

APPLE COMPUTER INC.
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03) to apply to entire TPA/TPB XNets.

NOTE: FireWire TPA/TPB pairs are NOT assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to in their appropriate connections and to properly terminate unused signals.

ELECTRICAL_CONSTRAINT_SET

Place close to FireWire PHY

2nd TPA/TPB pair unused

3rd TPA/TPB pair unused

FW Power Class Strap

Single-port system sets PC=0

Late-VG Protection Power

SOT-363

BAV99DW-X-F

051-7099

REV.

12345678

www.laptop-schematics.com

www.laptop-schematics.com
Place L5200, L5205 and L5206 across mois.
R6309 is not needed when sharing SPI flash with ICH7M and TEKOA (LAN CHIP).

R6307 and R6306 should be placed less than 100 mils from ICH7M.

R6303 should be placed less than 100 mils from flash ROM.
Sudden Motion Sensor (SMS)

SYNC_MASTER="MASTER"
SYNC_DATE="MASTER"
SMS_Z_AXIS="PP3V3_S3_SMS"
SMS_X_AXIS="SMS_X_AXIS"
SMS_Y_AXIS="SMS_Y_AXIS"
SMS_ONOFF_L="SMS_ONOFF_L"
SMS_ACC_SELFTEST="SMS_ACC_SELFTEST"

---

H 051-7099

www.laptop-schematics.com
1.8V S3 Current Sense

Vout = 0.6V * (1 + Ra / Rb)

1.8V S0 FET

1.8V Supply

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SYNC_DATE=(MASTER)
Power Control Signals

Ensure 1.2V and 2.5V S3 supplies are up and 3.3V level-shifter.

3.425V "G3Hot" Supply

Supply needs to guarantee 3.42V delivered to SMC Vref generator.

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S3 and 1.05V S3 are in regulation.

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.2V S0, 2.5V S0, 1.2V S0, 1.2V S3 and 0.9V S3 are in regulation.

3.3V G3Hot Supply & Power Control

LTC2908 threshold is 9% (4.7V, 2.185V, 2.75V, 1.71V, 1.15V, 0.86V)
**INVERTER INTERFACE**

- **PP5V_INVERTER_SW_F**: 6.3V
- **PP BUS_S0_INVERTER**: 5V
- **SYNC_DATE** = (MASTER)

**Internal Display Connectors**

- **SYNC_MASTER** = (MASTER)
- **I/O_VIC**: SOT23-LF
- **MF-LF**: 20% 50V
- **CERM**: 0.001uF
- **SM**: 20% 50V

Panel has 2K pull-ups:
- **no-panel case (development)**

---

**VOLTAAGE=12.8V**

**VOLTAAGE=3.3V**

---

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TMDS Filtering
Place series R's and common-mode filtering close to GPU, common-mode chokes near connector.

TMDS Filtering

VGA Sync Buffers

Analog Filtering
Place close to connector

DVI Interface

DVI DDC Current Limit

Isolation required for DVI power switch

3V Level Shifters

External Display Connector

Apple Computer Inc.
Bluetooth (M13P), IR & SATA HDD Flex Connector

**Left ALS Connector**

- **Critical**: FL4965
- **Placement note**: Place FL4965 close to southbridge
- **CRITICAL**: ALS_GAIN
- **LTALS_OUT**
- **Note**: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from DATA signals.

**M1 Specific Connectors**

- **SYNC_MASTER=(MASTER)**
- **SYNC_DATE=(MASTER)**
- **SYS_LED_ANODE**
- **ALS_GAIN**
- **LTALS_OUT**
- **USB_BT_N**
- **USB_BT_P**
- **USB_IR_N**
- **USB_IR_P**
- **SATA_C_D2R_C_P**
- **SATA_C_D2R_C_N**
- **SATA_C_D2R_UF_P**
- **SATA_C_D2R_UF_N**
- **SATA_C_R2D_C_P**
- **SATA_C_R2D_C_N**
- **SATA_C_R2D_UF_P**
- **SATA_C_R2D_UF_N**
- **SATA_C_R2D_P**
- **SATA_C_R2D_N**
- **PP3V3_S3_BT**
- **PP3V3_S3_LTALS**
- **PP5V_S0_HDD**
- **PP5V_S3_IR**
- **SCNLED**
- **PH4960**
- **P4960**
- **S4960**
- **C4960**
- **C4961**
- **C4965**
- **C4966**
- **C4969**
- **J6430**
- **FH19-4S-0.5SH-48**
- **J4960**
- **FL4965**
- **FL4966**
- **F-RT-SM**
- **QT500206-L020**

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LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the hot part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be off.

- LVDS_PD
  - RP9900
  - RP9901
  - RP9902
  - RP9903
  - RP9904
  - RP9905
  - RP9906
  - RP9907
  - RP9908

- LVDS_PD
  - SM-LF 8.2K 1/16W 5%
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