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<td>EM DDR Interface</td>
</tr>
<tr>
<td>14</td>
<td>EM DDR Interface</td>
</tr>
<tr>
<td>15</td>
<td>EM DDR Interface</td>
</tr>
<tr>
<td>16</td>
<td>EM DDR Interface</td>
</tr>
<tr>
<td>17</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>18</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>19</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>20</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>21</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>22</td>
<td>EM Power 2</td>
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<tr>
<td>23</td>
<td>EM Power 2</td>
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<tr>
<td>24</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>25</td>
<td>EM Power 2</td>
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<tr>
<td>26</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>27</td>
<td>EM Power 2</td>
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<td>28</td>
<td>EM Power 2</td>
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<tr>
<td>29</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>30</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>31</td>
<td>EM Power 2</td>
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<tr>
<td>32</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>33</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>34</td>
<td>EM Power 2</td>
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<tr>
<td>35</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>36</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>37</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>38</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>39</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>40</td>
<td>EM Power 2</td>
</tr>
<tr>
<td>41</td>
<td>EM Power 2</td>
</tr>
</tbody>
</table>

---

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</tr>
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</tr>
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<td>HMC 1</td>
</tr>
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</tr>
<tr>
<td>53</td>
<td>IMVP6 3.3V Regulators</td>
</tr>
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</tr>
<tr>
<td>55</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>56</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>57</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>58</td>
<td>1.5V / 1.8V Power Supply</td>
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<tr>
<td>59</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>60</td>
<td>1.5V / 1.8V Power Supply</td>
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<tr>
<td>61</td>
<td>1.5V / 1.8V Power Supply</td>
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<tr>
<td>62</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>63</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>64</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>65</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>66</td>
<td>1.5V / 1.8V Power Supply</td>
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<td>67</td>
<td>1.5V / 1.8V Power Supply</td>
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<tr>
<td>68</td>
<td>1.5V / 1.8V Power Supply</td>
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<tr>
<td>69</td>
<td>1.5V / 1.8V Power Supply</td>
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<tr>
<td>70</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>71</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>72</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>73</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>74</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>75</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>76</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>77</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>78</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>79</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
<tr>
<td>80</td>
<td>1.5V / 1.8V Power Supply</td>
</tr>
</tbody>
</table>

---

## Schematic, MLB, M1

### Post Ramp Revision

07/14/2006
<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>128S0077</td>
<td>IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO</td>
</tr>
<tr>
<td>128S0081</td>
<td>IC, YDC, CO, 2.16G, 31W, 667M, 2M, 479BGA</td>
</tr>
<tr>
<td>128S0061</td>
<td>IC, ATI, M56-LP, GPH XCRTL, LF 880BGA</td>
</tr>
<tr>
<td>343S0385</td>
<td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td>
</tr>
<tr>
<td>341S1789</td>
<td>IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA</td>
</tr>
<tr>
<td>338S0270</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
</tr>
<tr>
<td>337S3282</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
</tr>
<tr>
<td>333S0358</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
</tr>
<tr>
<td>826-4393</td>
<td>VRAM_HY256, GPU_MEM_256M, GPU_MEM_HYNIX, VRAM_256_HYNIX</td>
</tr>
<tr>
<td>826-4393</td>
<td>GPU_MEM_HYNIX, VRAM_128_HYNIX</td>
</tr>
<tr>
<td>826-4393</td>
<td>VRAM_128_SAMSUNG</td>
</tr>
<tr>
<td>128S0086</td>
<td>ALTERNATE FOR</td>
</tr>
<tr>
<td></td>
<td>EEE:WB3, EEE:WB2, EEE_WB3, EEE_WB2, EEE_WB6</td>
</tr>
<tr>
<td>U2100</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>U4102</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>U8400</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>U4101</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>U4400</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>330uF, 2V, 9MOHM, D2</td>
<td>COMMENTS:</td>
</tr>
<tr>
<td>CPU_1_83GHZ</td>
<td>Bootrom_devel</td>
</tr>
<tr>
<td>CPU_2_0GHZ</td>
<td>ATI_REV_B24</td>
</tr>
<tr>
<td>CPU_2_16GHZ</td>
<td>EEE_WB0, M1_COMMON, CPU_2_16GHZ, VRAM_SAM256</td>
</tr>
<tr>
<td>CPU_2_0GHZ</td>
<td>EEE_WB2, M1_COMMON, CPU_2_0GHZ, VRAM_SAM128</td>
</tr>
<tr>
<td>VRAM_SAM256</td>
<td>EEE_WB3, M1_COMMON, CPU_2_0GHZ, VRAM_SAM256</td>
</tr>
</tbody>
</table>
Chassis connection to be made at the mounting hole southwest of the USB connector.

Chassis connection to be made at the mounting hole northwest of the DVI connector.

NO_TEST = TRUE

MAKE_BASE = TRUE

NC_CPU_HFPLL

NC_CPU_A39_L

NC_CPU_A36_L

NC_CPU_A35_L

NC_CPU_A33_L

NC_CPU_SPARE2

NC_CPU_SPARE0

NC_CPU_APM1_L

TP_CPU_HFPLL

TP_CPU_A38_L

TP_CPU_A36_L

TP_CPU_A34_L

TP_CPU_A33_L

TP_CPU_A32_L

TP_CPU_A31_L

TP_CPU_A30_L

TP_CPU_APM1_L

TP_CPU_APM0_L

MEM_B_A<15..14>

NB_CFG<4..3>

NB_CFG<8>

NB_CFG<6>

SUS_CLK_SB

NB_CFG<15..14>

NB_CFG<11..10>

TP_NB_CFG<15..14>

TP_NB_CFG<11..10>

TP_NB_CFG<8>

TP_NB_CFG<6>

NOTE: NB_CFG<13..12> require test access

IN

OUT

R0600

MF-LF

1/16W

402

5%

0

R0600

MF-LF

1/16W

402

5%

0

MEM_B_A<15..14>

NB_CFG<4..3>

NB_CFG<8>

NB_CFG<6>

SUS_CLK_SB

NB_CFG<15..14>

NB_CFG<11..10>

TP_NB_CFG<15..14>

TP_NB_CFG<11..10>

TP_NB_CFG<8>

TP_NB_CFG<6>

NOTE: NB_CFG<13..12> require test access

IN

OUT

R0600

MF-LF

1/16W

402

5%

0

MEM_B_A<15..14>

NB_CFG<4..3>

NB_CFG<8>

NB_CFG<6>

SUS_CLK_SB

NB_CFG<15..14>

NB_CFG<11..10>

TP_NB_CFG<15..14>

TP_NB_CFG<11..10>

TP_NB_CFG<8>

TP_NB_CFG<6>

NOTE: NB_CFG<13..12> require test access

IN

OUT

R0600

MF-LF

1/16W

402

5%

0

MEM_B_A<15..14>

NB_CFG<4..3>

NB_CFG<8>

NB_CFG<6>

SUS_CLK_SB

NB_CFG<15..14>

NB_CFG<11..10>

TP_NB_CFG<15..14>

TP_NB_CFG<11..10>

TP_NB_CFG<8>

TP_NB_CFG<6>

NOTE: NB_CFG<13..12> require test access

IN

OUT
NOTE: This cap is shared between CPU and NB
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
- ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PROB PIN.

ITPRESET_L
- XDP_DBRESET_L
- XDP_TCK
- XDP_BPM_L<5>
- XDP_BPM_L<4>
- XDP_BPM_L<3>
- XDP_BPM_L<2>
- XDP_BPM_L<1>
- XDP_BPM_L<0>

ITP_TDO
- CPU_XDP_CLK_P
- XDP_TMS
- XDP_TDI
- XDP_TCK
- XDP_BPM_L<5>
- XDP_BPM_L<4>
- XDP_BPM_L<3>
- XDP_BPM_L<2>
- XDP_BPM_L<1>
- XDP_BPM_L<0>

ITP_RESET_L
- CPU_XDP_CLK_N
- XDP_TRST_L
- FSB_CPURST_L
- XDP_CPURST_L
- XDP_XDP_RST_N
- XDP_XDP_RST_P
- XDP_TDO
- XDP_TDI
- XDP_TCK
- XDP_BPM_L<5>
- XDP_BPM_L<4>
- XDP_BPM_L<3>
- XDP_BPM_L<2>
- XDP_BPM_L<1>
- XDP_BPM_L<0>

www.laptop-schematics.com
TV-Out Disable
Component: DACA, DACB & DACC

LVDS Disable
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
Unused DAC outputs must remain powered, but can omit
Can leave all signals NC if LVDS is not implemented

CRT Disable
tie to GND through 75-ohm resistors.

TV-Out Signal Usage:
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.

www.laptop-schematics.com
These are the power signals that leave the NB “block”:

- **PP2V5_S0_NB_VCCA_CRTDAC**
- **PP1V5_S0_NB_TVDAC**
- **PP1V5_S0_NB_PLL**
- **PP1V5_S0_NB_VCCAUX**
- **PP1V5_S0_NB_PCIE**
- **PP1V05_S0_NB_CRT**
- **PP1V5_S0_NB_VCC3G**
- **PP1V5_S0_NB_VCCA_3GPLL**
- **NC_GND_NB_VSSA_LVDS**
- **NC_LVDS_IBG**
- **TP_LVDS_VREFL**
- **TP_LVDS_VDDEN**
- **NC_LVDS_B_DATAP<2..0>**
- **TP_LVDS_BKLTEN**
- **TP_LVDS_BKLTCTL**
- **TP_SDVO_CTRLDATA**
- **TP_SDVO_CTRLCLK**
- **NC_LVDS_CLKP**
- **NC_LVDS_CLKN**
- **NC_LVDS_IBG**
- **NC_NB_XOR_LVDS_D27**
- **NC_NB_XOR_LVDS_A35**

Layout Notes:

- CERM (Ceramic) 6.3V 22UF X5R 20%
- 6.3V 805 20%
- 6.3V 21%
- 6.3V 402 10V 20%
- L1936 0603
- L1975
- Layout Note: Route to caps, then ground.
- Layout Note: Do not reveal or publish in whole or part, property of Apple Computer Inc.

MIN_NECK_WIDTH = 0.25 mm
VOLTAGE = 1.5V
MIN_LINE_WIDTH = 0.38 mm

Scale: None
Size: A
<table>
<thead>
<tr>
<th>NB_CFG&lt;0&gt;</th>
<th>RESERVED</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB_CFG&lt;1&gt;</td>
<td>RESERVED</td>
</tr>
<tr>
<td>NB_CFG&lt;2&gt;</td>
<td>High = Reversed</td>
</tr>
<tr>
<td></td>
<td>Low = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;3&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;4&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;5&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;6&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;7&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;8&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;9&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;10&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
<tr>
<td>NB_CFG&lt;11&gt;</td>
<td>Internal pull-up</td>
</tr>
<tr>
<td></td>
<td>Low = Reversed</td>
</tr>
<tr>
<td></td>
<td>High = Normal</td>
</tr>
</tbody>
</table>

**PROBABLY NOT NEEDED**

- NB_CFG<12>: Reserved
- NB_CFG<13>: Reserved
- NB_CFG<14>: Reserved
- NB_CFG<15>: Reserved
- NB_CFG<16>: Reserved
- NB_CFG<17>: Reserved
- NB_CFG<18>: Reserved
- NB_CFG<19>: Reserved

**PROBABLY NOT NEEDED**

- NB_CFG<20>: Reserved
- NB_CFG<21>: Reserved
- NB_CFG<22>: Reserved
- NB_CFG<23>: Reserved
- NB_CFG<24>: Reserved
- NB_CFG<25>: Reserved
- NB_CFG<26>: Reserved
- NB_CFG<27>: Reserved

**NB Config Straps**

- NB_CFG_DMI_X2: Reserved
- NB_CFG_DMI_REVERSE: Reserved
- NB_CFG_SDVO_AND_PCIE: Reserved
- NB_CFG_PEG_REVERSE: Reserved
- NB_CFG_DYN_ODT_DISABLE: Reserved
- NB_CFG_VCC_1V5: Reserved
- NB_CFG_DMI_LANE: Reserved
- NB_CFG_PCIE_INTEROP_MODE: Reserved
- NB_CFG_PCIE_BACKWARD_COMPATIBILITY: Reserved

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Ensure CS_L and ODT resistors are close to SO-DIMM connector.
If power inputs are not S0, 
MEMVTT_DIS can be used to 
leave 1.8V powered in S3.

Okay to turn off 5V and
 disable MEMVTT in sleep.

Power aliases required by this page:

-BOM options provided by this page:

-Signal aliases required by this page:
NEED TO CHECK CAP VALUE

C3301
34
33
0402
=PP3V3_S0_CK410
21
2
1
10UF
6.3V
20%
2.2
5%
14.31818
21
C3315
402
2
1
C3390
(ICH7M PCI 33MHZ)
34
2
1
CK410_PCI5_FCTSEL1
0.1UF
10%16VX5R
VOLTAGE=3.3V
(FW PCI 33MHZ)
(VSM LPC 33MHZ)
2
C3302
0.1UF
10%16VX5R
VOLTAGE=3.3V
(ICH SM BUS)
34
IN
IO
X5R603
10%
6.3V
34
34
34
OUT
CK410_PCI4_CLK
CK410_PCI3_CLK
CK410_IREF
R3300
475
MF-LF
1%
C3311
16V
10%
402
FERR-120-OHM-1.5A
MIN_NECK_WIDTH=0.2mm
MIN_LINE_WIDTH=0.5mm
SYNC_MASTER=M42
WWW.LAPTOP-SCHEMATICS.COM
APLLE COMPUTER INC. D 055-1160 m
C
B
D
NO PULL-UP NEEDED
PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101

PLACE C4110 AND C4111 WITHIN 12 MIL OF U4101 PIN 49 AND 50
SCHEME MATCHES DOC MVL100258-01

PLACE C4113 AND C4112 WITHIN 0.1UF 402 10% X5R

APPLE COMPUTER INC.
Transformers should be mirrored on opposite sides of the board.
When ENETPWR_S3 BOMOPTION is active:

When ENETPWR_S3AC BOMOPTION is active:

<table>
<thead>
<tr>
<th>State</th>
<th>PM_SLP_S4_L</th>
<th>PM_SLP_S3BATT</th>
<th>PM_SLP_S3BATT_L</th>
<th>P2V5S3_EN_L</th>
<th>P1V2S3_RUNSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>G3H</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
<td>0V (1.2V OFF)</td>
</tr>
<tr>
<td>S5</td>
<td>0V</td>
<td>PBUS (3.3V OFF)</td>
<td>0V</td>
<td>Hi-Z (2.5V OFF)</td>
<td>0V (1.2V OFF)</td>
</tr>
</tbody>
</table>

State     FWPWR_EN_L  PM_SLP_S4_L  PM_SLP_S3BATT    PM_SLP_S3BATT_L  P2V5S3_EN_L      P1V2S3_RUNSS

| S3      | 3.3V        | 0V  (3.3V ON) | 3.3V             | 0V  (2.5V ON) | 3.3V (1.2V ON)|
| S0      | 3.3V        | 0V  (3.3V ON) | 3.3V             | 0V  (2.5V ON) | 3.3V (1.2V ON)|
| S3 AC   | 0V          | 3.3V (3.3V ON)| 0V              | 3.3V (2.5V ON)| 3.3V (1.2V ON)|
| S0 Batt | 0V          | 3.3V (3.3V ON)| 0V              | 3.3V (2.5V ON)| 3.3V (1.2V ON)|
| S0 AC   | 0V          | 3.3V (3.3V ON)| 0V              | 3.3V (2.5V ON)| 3.3V (1.2V ON)|
| G3H Batt| PBUS        | 0V  (3.3V ON) | 0V              | Hi-Z (2.5V OFF)| 0V (1.2V OFF)|
| S5 Batt | PBUS        | 0V  (3.3V ON) | 0V              | Hi-Z (2.5V OFF)| 0V (1.2V OFF)|
| S5 AC   | 0V          | 0V  (3.3V ON) | PBUS (3.3V OFF) | Hi-Z (2.5V OFF)| 0V (1.2V OFF)|
| S3 Batt | PBUS        | 3.3V (3.3V ON)| PBUS (3.3V OFF) | 0V  (3.3V OFF) | 3.3V (2.5V OFF)|

Yukon Power Control

allows powering Yukon down during battery sleep to save power

ENETPWR_S3

R4300

MF-LF

1/16W

402

5%
Port Power Switch

Right USB Port

Place L5200, L5205 and L5206 across moat
PCI-E x1 Port "A" = Ethernet (Yukon)
PCI-E x1 Port "B" = PCI-E Mini Card
PCI-E x1 Port "C" = ExpressCard
PCI-E x1 Port "D" = Unused
PCI-E x1 Port "E" = Unused
PCI-E x1 Port "F" = Unused

TP_PCIE_F_D2RP
MAKE_BASE=TRUE
TP_PCIE_F_D2RN
MAKE_BASE=TRUE
TP_PCIE_F_R2DP
PCIE_F_D2RP
PCIE_F_D2R_P
PCIE_F_D2R_N
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P

TP_PCIE_E_D2RP
MAKE_BASE=TRUE
TP_PCIE_E_D2RN
MAKE_BASE=TRUE
TP_PCIE_E_R2DN
PCIE_E_D2RN
PCIE_E_D2R_P
PCIE_E_D2R_N
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P

TP_PCIE_D_D2RN
MAKE_BASE=TRUE
TP_PCIE_D_D2RP
MAKE_BASE=TRUE
TP_PCIE_D_R2DP
PCIE_D_R2DP
PCIE_D_R2D_C_P
PCIE_D_R2D_C_N
PCIE_D_D2R_P
PCIE_D_D2R_N

PCIE_EXCARD_D2R_N
MAKE_BASE=TRUE
PCIE_EXCARD_D2R_P
MAKE_BASE=TRUE
PCIE_EXCARD_R2D_C_N
MAKE_BASE=TRUE
PCIE_EXCARD_R2D_C_P
MAKE_BASE=TRUE

PCIE_MINI_D2R_P
MAKE_BASE=TRUE
PCIE_MINI_D2R_N
MAKE_BASE=TRUE
PCIE_MINI_R2D_C_N
MAKE_BASE=TRUE
PCIE_MINI_R2D_C_P
MAKE_BASE=TRUE
PCIE_MINI_D2R_N
MAKE_BASE=TRUE
PCIE_MINI_D2R_P
MAKE_BASE=TRUE
PCIE_B_D2R_P
MAKE_BASE=TRUE
PCIE_B_D2R_N
MAKE_BASE=TRUE
PCIE_B_R2D_C_N
MAKE_BASE=TRUE
PCIE_B_R2D_C_P
MAKE_BASE=TRUE

PCIE_C_D2R_P
MAKE_BASE=TRUE
PCIE_C_D2R_N
MAKE_BASE=TRUE
PCIE_C_R2D_C_N
MAKE_BASE=TRUE
PCIE_C_R2D_C_P
MAKE_BASE=TRUE

PCIE_D_R2D_C_P
MAKE_BASE=TRUE
PCIE_D_R2D_C_N
MAKE_BASE=TRUE
PCIE_D_D2R_P
PCIE_D_D2R_N

PCIE_EXCARD_D2R_N
=
PCIE_EXCARD_D2R_P
=
PCIE_EXCARD_R2D_C_N
=
PCIE_EXCARD_R2D_C_P
=

www.laptop-schematics.com
UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER.
DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.
**GPU / Heat Pipe Thermal Sensor**

**Right-Side/Fin Stack Thermal Sensor**

**CPU Back-Up Thermal Diode**

---

**Part Number**

- CPU BACK-UP THERMAL DIODE
- R6190 SOT23

R1001 / R1002 are not currently BOM OPTIONed. Cannot be programatically unstuff those parts to stuff these.

**Placement note:**

- Place near GPU center
- Minimize stubs between these R's and R1001 & R1002
- Minimize stubs between SOT23 parts
- Minimize stubs between R's

**CRITICAL**

**Layout note:**

- Keep all 4 pads on R1001 as possible
- Do not block R1001
- Do not block R1002

---

**Thermal Sensors**

[www.laptop-schematics.com](http://www.laptop-schematics.com)
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEGOA (LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FROM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FROM FLASH ROM
**Left ALS Filter**

- Left ALS circuit has 1K series-R

**Right ALS Circuit**

- ALS_RT_OUT

**Keyboard LED Driver**

- KBDLED_SW

---

**ALS Support**

- CRITICAL

---

**Notice of Proprietary Property**

- Sync Date: (Master)

---

**www.laptop-schematics.com**
Sudden Motion Sensor (SMS)

**Critical Components**

- U6620: CRITICAL
- C6604: 0.033 UF X7R 10V 20%
- C6605: 10V 20% 402X7R
- C6606: 0.033 UF X7R 10V
- R6620: 1/16W 5% MF-LF 10K
- R6621: 1/16W 5% MF-LF
- KXM52-2050 QFN

**Schematic Details**

- Desired orientation when placed on board top-side:
  - Top-through view
- Desired orientation when placed on board bottom-side:
  - Top-through view

**Part Placement**

- M1 placement: Bottom-side
  - placed on board bottom-side:
- placed on board top-side:

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APPLE COMPUTER INC. 2005-7141 3
If unconnected, powers up with VIN. Connect to RUNSS pins to control outputs.

5V S3 FET

5V S0 FET

5V / 1.5V Power Supply

APPLE COMPUTER INC.

www.laptop-schematics.com
NOTE: Be aware of pull-up on this signal.

Vout = 0.8V * (1 + Ra / (Rb + Rc))

Vout = 2.52V

Vout = 1.205V

Vout = 0.8V * (1 + Ra / (Rb + Rc))

Vout = 2.5V S3 Regulator

Vout = 1.20V

2.5V S0 FET

1.2V S3 Regulator

1.2V S0 FET

2.5V & 1.2V Regulators

SYNC/MODE

ITH

RUN/SS

PGOOD

PAD

SYNC_DATE=(MASTER)

REV.

WWW.LAPTOP-SCHEMATICS.COM

APPLE COMPUTER INC.

CRITICAL
Power Control Signals

3.425V "G3Hot" Supply

Supply needs to guarantee 3.13V delivered to GPU (other than generator)

NOTE: R8065 acts as 10K pull-up for PGOOD signal

1.5v / 1.05v PWRGD Circuit

Reports when 1.5V DD and 1.05V DD are in regulation

Unused PGOOD Signals

Unused signals, if unused should be pulled down to VSS or left as open

Other 50 Rails PWRGD Circuit

Reports when 50 DD, 3.5v DD, 1.8v DD, 1.8v DD and 0.9v DD are in regulation

3.3v G3Hot Supply & Power Control

Voltage levels and power consumption

Note: All pads are 10% tolerance unless otherwise specified

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Place series R's and common-mode filtering close to GPU, common mode chokes near connector.

TMDS Filtering

VGA Sync Buffers

Analog Filtering

Place close to connector

DVI Interface

3V Level Shifters

External Display Connector

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Left ALS Connector

Bluetooth (M13P), IR & SATA HDD Flex Connector

Placements:
- Place FL4960 close to J4960
- Place C4960 close to southbridge
- Place C4961 next to C4960
- Place FL4965 close to southbridge
- Place C4965 close to J4960
- Place C4966 next to C4965

SATA_C_D2R_UF_N
SATA_C_D2R_N
SATA_C_D2R_P
SATA_C_D2R_UF_P
SATA_C_D2R_C_P
SATA_C_D2R_C_N

SATA_C_R2D_P
SATA_C_R2D_N
SATA_C_R2D_UF_P
SATA_C_R2D_UF_N
SATA_C_R2D_C_P
SATA_C_R2D_C_N

PP5V_S3_IR
PP3V3_S3_BT
PP5V_S0_HDD

USB_IR_P
USB_IR_N
USB_BT_P
USB_BT_N
LVDS Interface Pull-downs

NOTE: These parts are to ensure an invalid state Ramsey by the LVDS pull-ups. This voltage is present on LVDS interface pins even when the LVDS driver is low. These parts are to ensure the pull-up is not always on, which helps to prevent any leakage current from damaging the LVDS signals.

- LVDS_U_CLK_CONN_P
  - LVDS_U_CLK_CONN_N
- LVDS_L_CLK_N
  - LVDS_L_CLK_P
- LVDS_U_DATA_CONN_N
  - LVDS_U_DATA_CONN_P
- LVDS_L_DATA_CONN_N
  - LVDS_L_DATA_CONN_P
- LVDS_PD
  - 8.2K
  - 5%
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.
2005/09/08 - 4248911 - Sync with M38 & M42.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.
2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/28 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/29 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/09/28 - 4221965 - Added 2.2uF caps on SO-DIMM VREF pins.
2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.
2005/10/12 - 4214493 - Consolidated 0.22uF caps in design.
2005/10/13 - 4247941 - Spacing/Physical rule updates to match latest board database.
2005/09/29 - 4235179 - Removed NO STUFF option from R8805 per ATI request.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/28 - 4235179 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
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2005/10/04 - 4256409 - Changed fan CTL series R's to 2N7002 level-shifter.
ANGLED CAPS FOR C4 NOISE

CPU AREA

- Connection to unstuffed comp. pads

GPU AREA

- Connection to unstuffed comp. pads

SB AREA

- Connection to unstuffed comp. pads

**PART NUMBER| QTY| DESCRIPTION| MARKING CODE| MANUFACTURER| NON OPTION**

- 33UF 16V 20% POLY CASED2E-SM
- OMIT
- CRWK09
- CRWK10
- CRWK11
- CRWK12
- CRWK13
- CRWK14
- CRWK15

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