

# M42A, MLB

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
07		355269	ENGINEERING RELEASED		
				DATE	DATE
				12/10/04	?

11/27/2006 PVT

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19	19	NB (GM) Decoupling	DK	NB	06/22/2005
20	20	NB Config Straps	DK	NB	06/28/2005
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37	37	ETHERNET CONNECTOR	ES	ENET	11/14/2005
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42	42		ES	ENET	11/01/2005
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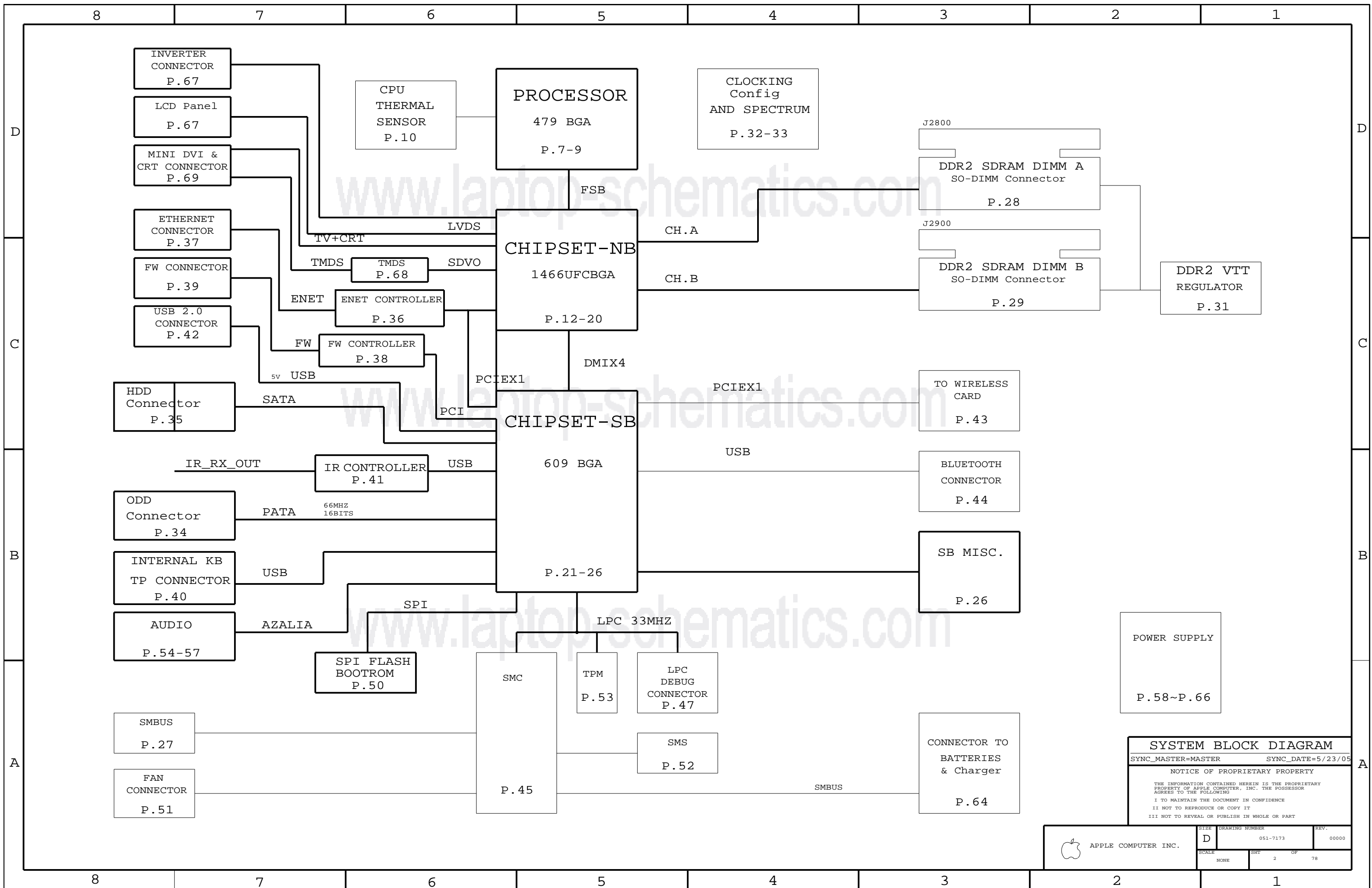
M42A EE DRIS:

- RX-RAYMOND XU
- DK-DINESH KUMAR
- RC-RAY CHANG
- MK-MARC KLINGELHOFER
- LT-LAWRENCE TAN
- ES-ERIC SMITH
- LD-LINDA DUNN

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7173	1	SCHEM, M42A, MLB	SCH	
820-1889	1	PCBF, M42, MLB	PCB	

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	WRAPPER ENG APPD QA APPD RELEASE	DESIGN CR MFG APPD DESIGNER SCALE	
 THIRD ANGLE PROJECTION	MATERIAL/FINISH NOTED AS APPLICABLE	SIZE <b>D</b>	REV. <b>00000</b> SHIT 1 OF 78



**SYSTEM BLOCK DIAGRAM**

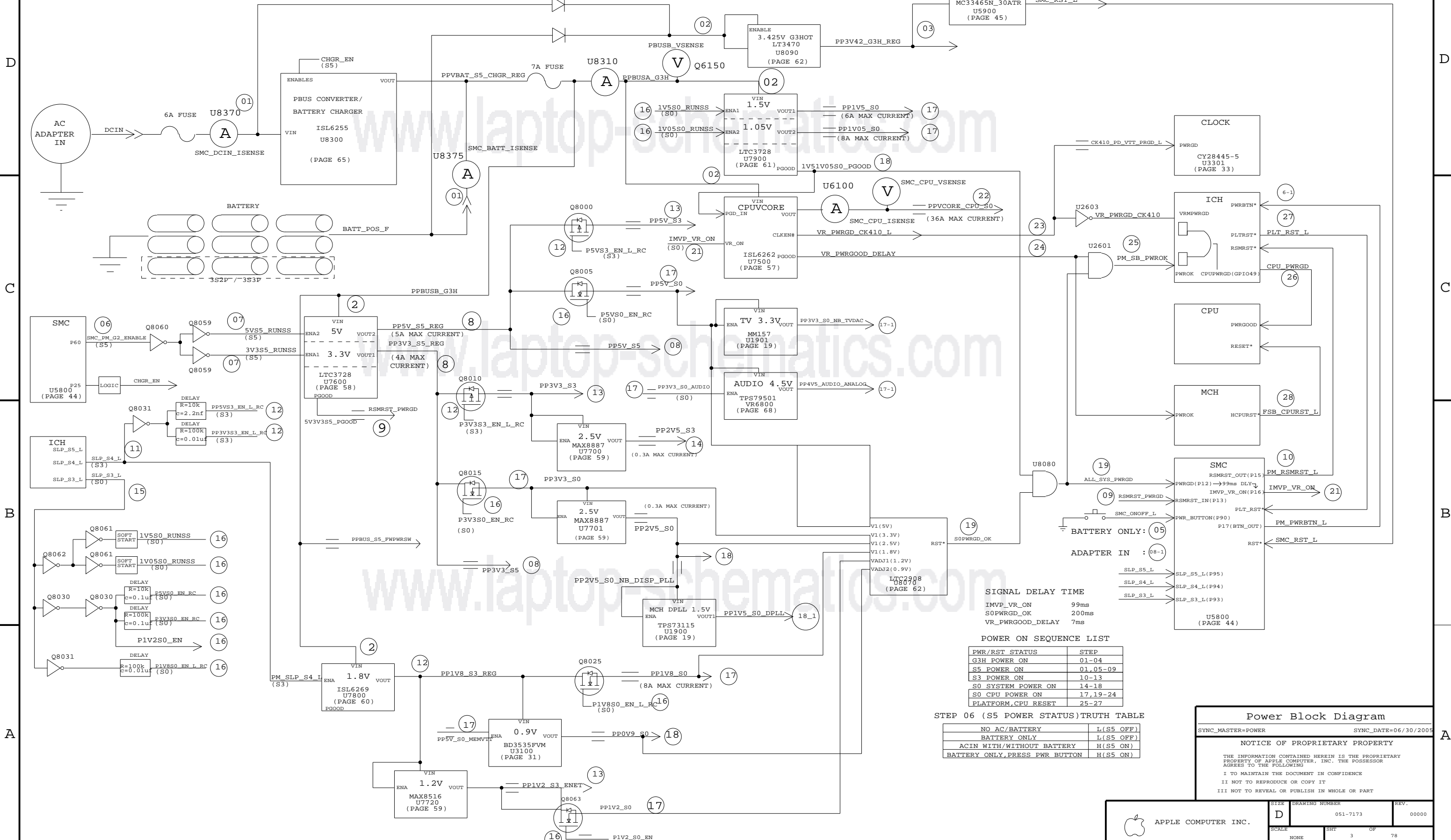
SYNC\_MASTER=MASTER SYNC\_DATE=5/23/05

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NONE	2		78

# M42A POWER SYSTEM ARCHITECTURE



**SIGNAL DELAY TIME**

IMVP_VR_ON	99ms
SOPWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

**POWER ON SEQUENCE LIST**

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01,05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17,19-24
PLATFORM,CPU RESET	25-27

**STEP 06 (S5 POWER STATUS) TRUTH TABLE**

NO AC/BATTERY	L(S5 OFF)
BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	H(S5 ON)
BATTERY ONLY, PRESS PWR BUTTON	H(S5 ON)

**Power Block Diagram**

SYNC\_MASTER=POWER SYNC\_DATE=06/30/2005

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Page Notes

Power aliases required by this page:  
(NONE)

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	v	v	v	v	v	v
5V3V3S3_CONT						
5V3V3S3_SKIP	v	v	v	v	v	v
ACCEL_KIONIX			v	v	v	
ACCEL_ST	v	v				v
INVERTER_BUF	v	v	v	v	v	v
INVERTER_UNBUF						
ITP						
LEMENU	v	v	v	v	v	v
MEMVIT_EN_PU	v	v	v	v	v	v
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	v	v	v	v	v	v
USB_D_OC_PU	v	v	v	v	v	v
USB_E_OC_PU	v	v	v	v	v	v
GOOD	v			v		
BETTER		v			v	
BEST			v			v
M42A_PGM	v	v	v	v	v	v
ONEWIRE_PULLUP	v	v	v	v	v	v
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	v	v	v	v	v	v
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	v	v	v	v	v	v
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	v	v	v	v	v	v
3V3_IND_3MM						
NORMAL	v	v		v	v	
FANCY			v			v
STANDOFF	v	v	v	v	v	v
FET_FDN6296	v	v	v	v	v	v
FET_STL8NH3LL						
GOOD-ST	v					
BETTER-ST		v				
BEST-KIONIX			v			
GOOD-KIONIX				v		
BETTER-KIONIX					v	
BEST-ST						v
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	v	v	v	v	v	v
M42						
M42A	v	v	v	v	v	v

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

MLB STACKUP		
LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3387	1	IC, MEMOM, CPU B2 DC 1.83GHZ, 479 PGA	U0700	GOOD
337S3389	1	IC, MEMOM, CPU B2 DC 2.0GHZ, 479 PGA	U0700	BETTER
337S3389	1	IC, MEMOM, CPU B2 DC 2.0GHZ, 479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC, FW32306, 1394A LIME, BGA, 129P	U4400	LEMENU
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	LEMENU
359S0109	1	IC, SLOBLP436, CLOCK GEN, 68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1941	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, 8028	U6301	M42A_PGM
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, 808	U4102	M42A_PGM
341S1946	1	IC, SMC, 176P BGA, MS8/2116	U5800	M42A_PGM
341S1890	1	IC, PSOC-W/USB, 56P, MLP, CY8C24794	U5100	M42A_PGM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WES	CRITICAL	GOOD-ST
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WET	CRITICAL	BETTER-ST
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEW	CRITICAL	BEST-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEV	CRITICAL	GOOD-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:W6V	CRITICAL	BETTER-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEU	CRITICAL	BEST-ST

CONFIGURATION OPTIONS

SYNC\_MASTER=SMC SYNC\_DATE=07/18/2005

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	NONE	4	78

# Functional Test Points

## Power Supply NO\_TESTS

NO_TEST	TEST	VALUE	LOC
	IMVP6_RBIAS		58
	IMVP6_COMP		58
	5VS5_RUNSS		59 63
	1V5S0_RUNSS		52 63
	1V8S3_COMP		61
	1V8S3_FSET		61
	TRUE 3V3S5_COMP		
	TRUE 3V3S5_FSET		
	TRUE 1V05S0_COMP		
	TRUE 1V05S0_FSET		
	TRUE P3V42G3H_FB		63

## CLOCK NO\_TESTS

NO_TEST	TEST	VALUE	LOC
	TRUE CK410_CPU0_N		32 33
	TRUE CK410_CPU0_P		32 33
	TRUE CK410_CPU1_N		32 33
	TRUE CK410_CPU1_P		32 33
	TRUE CK410_CPU2_ITP_SRC10_N		32 33
	TRUE CK410_CPU2_ITP_SRC10_P		32 33
	TRUE CK410_DOT96_27M_N		32 33
	TRUE CK410_DOT96_27M_P		32 33
	TRUE CK410_LVDS_N		32 33
	TRUE CK410_LVDS_P		32 33
	TRUE CK410_PCI4_CLK_SPN		
	TRUE CK410_PCF1_CLK		32 33
	TRUE CK410_SRC1_N_SPN		6
	TRUE CK410_SRC1_P_SPN		6
	TRUE CK410_SRC2_N		32 33
	TRUE CK410_SRC2_P		32 33
	TRUE CK410_SRC3_N_SPN		6
	TRUE CK410_SRC3_P_SPN		6
	TRUE CK410_SRC4_N		32 33
	TRUE CK410_SRC4_P		32 33
	TRUE CK410_SRC5_N		32 33
	TRUE CK410_SRC5_P		32 33
	TRUE CK410_SRC6_N		32 33
	TRUE CK410_SRC6_P		32 33
	TRUE CK410_SRC7_N_SPN		6
	TRUE CK410_SRC7_P_SPN		6
	TRUE CK410_SRC8_N		32 33
	TRUE CK410_SRC8_P		32 33
	TRUE CK410_SRC_CLKREQ01_L_SPN		6
	TRUE CK410_SRC_CLKREQ03_L_SPN		6
	TRUE CK410_SRC_CLKREQ08_L		32 33

## FIREWARE NO\_TESTS

NO_TEST	TEST	VALUE	LOC
	TRUE FW_B_TPA_N_SPN		6
	TRUE FW_B_TPA_P_SPN		6
	TRUE FW_B_TPBIAS_SPN		6
	TRUE FW_B_TPB_N_SPN		6
	TRUE FW_B_TPB_P_SPN		6
	TRUE FW_C_TPA_N_SPN		6
	TRUE FW_C_TPA_P_SPN		6
	TRUE FW_C_TPBIAS_SPN		6
	TRUE FW_C_TPB_N_SPN		6
	TRUE FW_C_TPB_P_SPN		6

## LVDS NO\_TESTS

NO_TEST	TEST	VALUE	LOC
	TRUE LVDS_B_CLK_N_SPN		6
	TRUE LVDS_B_CLK_P_SPN		6
	TRUE LVDS_B_DATA_N0_SPN		6
	TRUE LVDS_B_DATA_N1_SPN		6
	TRUE LVDS_B_DATA_N2_SPN		6
	TRUE LVDS_B_DATA_P1_SPN		6
	TRUE LVDS_B_DATA_P2_SPN		6

## ETHERNET NO\_TESTS

NO_TEST	TEST	VALUE	LOC
	TRUE ENET_MDI_TRAN_P<2>		37
	TRUE ENET_MDI_TRAN_N<2>		37
	TRUE ENET_MDI_TRAN_P<3>		37

NO_TEST	TEST	VALUE	LOC
	TRUE SMC_FAN_3_TACH		45 46
	TRUE ALS_LEFT		45 46

## Fan Connectors

FUNC_TEST	TEST	VALUE	LOC
	TRUE =PP5V_S0_FAN_RT		51 64
	TRUE FAN_RT_PWM		51
	TRUE FAN_RT_TACH		51
	TRUE =PP3V3_S0_FAN_RT		51 64
	TRUE SMC_FAN_1_CTL		45 51
	TRUE SMC_FAN_1_TACH		45 51

## LPC+ Debug Connector

FUNC_TEST	TEST	VALUE	LOC
	TRUE =PP3V42_G3H_LPCPLUS		47 64
	TRUE =PP5V_S0_LPCPLUS		47 64
	TRUE LPC_AD<0>		21 45 47 53
	TRUE LPC_AD<1>		21 45 47 53
	TRUE LPC_FRAME_L		21 45 47 53
	TRUE PM_CLKRUN_L		23 38 45 47 53
	TRUE BOOT_LPC_SPI_L		22 45 47
	TRUE SMC_TMS		45 46 47
	TRUE DEBUG_RST_L		26 47
	TRUE SMC_TRST_L		45 47
	TRUE SMC_TDO		45 46 47
	TRUE SMC_MD1		45 47
	TRUE SMC_TX_L		45 46 47
	TRUE FWH_INIT_L		5 21 47
	TRUE PCI_CLK_PORT80_LPC		33 47
	TRUE LPC_AD<2>		21 45 47 53
	TRUE LPC_AD<3>		21 45 47 53
	TRUE INT_SERIRO		23 45 47 53
	TRUE PM_SUS_STAT_L		23 45 46 47 53
	TRUE SMC_TDI		45 46 47
	TRUE SMC_TCK		45 46 47
	TRUE SMC_RST_L		45 46 47
	TRUE SMC_NMI		45 47
	TRUE SMC_RX_L		45 46 47
	TRUE SV_SET_UP		23 47

## Other Func Test Points

FUNC_TEST	TEST	VALUE	LOC
	TRUE =PP1V05_S0_REG		52 64
	SMBus FUNC_TEST		
	TRUE SMBUS_SMC_MLB_SCL		27
	TRUE SMBUS_SMC_MLB_SDA		27
	FIREWIRE FUNC_TEST		
	TRUE PPFW_SWITCH		39
	SLEEP_LED_FUNC_TEST		
	TRUE SYS_LED_ANODE		35 46
	SMC FUNC_TEST		
	TRUE SMC_LID		40 45 46 65
	TRUE SMC_MANUAL_RST_L		46
	TRUE SMC_CPU_VSENSE		45 48
	Power Supply FUNC_TEST		
	TRUE ALL_SYS_PWRGD		26 45 63
	TRUE PPVCORE_CPU_S0		64
	TRUE PP1V05_S0		64
	TRUE PP1V5_S0		64
	TRUE PP1V8_S0		64
	TRUE PP2V5_S0		64
	TRUE PP3V3_S0		64
	TRUE PP5V_S0		64
	TRUE PP1V2_S3		64
	TRUE PP1V8_S3		64
	TRUE PP2V5_S3		64
	TRUE PP3V3_S3		64
	TRUE PP5V_S3		64
	TRUE PP3V3_S5		64
	TRUE PP5V_S5		64
	TRUE PP3V42_G3H		64
	TRUE PPBUSA_G3H		64
	TRUE PPBUSB_G3H		64
	TRUE PP18V5_G3H		64
	TRUE PP0V9_S0		64

## Battery Digital Connector

FUNC_TEST	TEST	VALUE	LOC
	TRUE SMC_BS_ALRT_L		45 46 65
	TRUE SMBUS_BATT_SCL_F		65
	TRUE SMBUS_BATT_SDA_F		65
	TRUE BATT_IN		65
	TRUE BATT_POS		65
	TRUE BATT_NEG		65

## Audio FUNC\_TEST

FUNC_TEST	TEST	VALUE	LOC
	TRUE PP5V_S0_AUDIO_PWR		21 64
	TRUE PP5V_S0_AUDIO		21 64
	TRUE GND_AUDIO_PWR		64
	TRUE GND_AUDIO_CODEC		64
	TRUE ACZ_SDATAIN<0>		21 64
	TRUE ACZ_SDATAOUT		21 64
	TRUE ACZ_BITCLK		21 64
	TRUE ACZ_RST_L		21 54 57
	TRUE ACZ_SYNC		21 64

## Battery FUNC\_TEST

FUNC_TEST	TEST	VALUE	LOC
	TRUE SMC_BATT_ISET		45 66
	TRUE SMC_BATT_CHG_EN		45 46 66
	TRUE SMC_BC_ACOK		45 46 65 66
	TRUE SMC_PS_ON		39 45 46 65
	TRUE SMC_BATT_TRICKLE_EN_L		45 46 66
	TRUE SYS_ONEWIRE		45 46 65

## USB FUNC\_TEST

FUNC_TEST	TEST	VALUE	LOC
	TRUE TP_USBP_E		6
	TRUE TP_USBN_E		6
	TRUE TP_USBP_F		6
	TRUE TP_USBN_F		6

## DC-JACK FUNC\_TEST

FUNC_TEST	TEST	VALUE	LOC
	TRUE ACIN_ENABLE_GATE		65

## Battery charger FUNC\_TEST

FUNC_TEST	TEST	VALUE	LOC
	TRUE PPVBAT_G3H_CHGR_OUT		66

## INVERTER CONNECTOR FUNC\_TEST

FUNC_TEST	TEST	VALUE	LOC
	TRUE PPBUS_ALL_INV_CONN		67
	TRUE INV_GND		67
	TRUE PP5V_INV_F		67
	TRUE INV_BKLIGHT_PWM_L		67

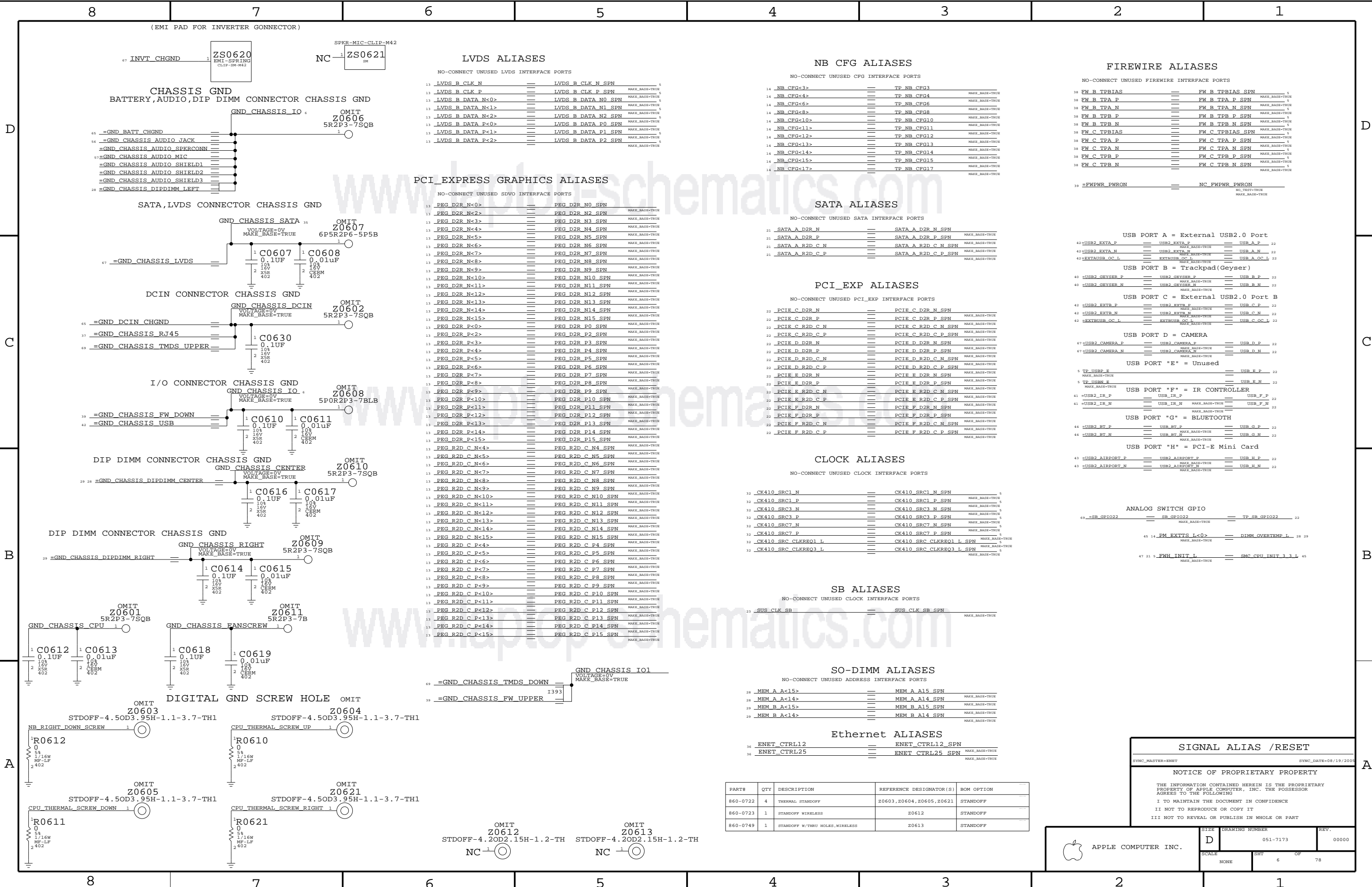
FUNC TEST 1 OF 2

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	5	78	





### LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

13	LVDS B CLK N	LVDS B CLK N SPN	MAKE_BASE-TRUE	5
13	LVDS B CLK P	LVDS B CLK P SPN	MAKE_BASE-TRUE	5
13	LVDS B DATA N<0>	LVDS B DATA N0 SPN	MAKE_BASE-TRUE	5
13	LVDS B DATA N<1>	LVDS B DATA N1 SPN	MAKE_BASE-TRUE	5
13	LVDS B DATA N<2>	LVDS B DATA N2 SPN	MAKE_BASE-TRUE	5
13	LVDS B DATA P<0>	LVDS B DATA P0 SPN	MAKE_BASE-TRUE	5
13	LVDS B DATA P<1>	LVDS B DATA P1 SPN	MAKE_BASE-TRUE	5
13	LVDS B DATA P<2>	LVDS B DATA P2 SPN	MAKE_BASE-TRUE	5

### PCI EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

13	PEG D2R N<0>	PEG D2R N0 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<2>	PEG D2R N2 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<3>	PEG D2R N3 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<4>	PEG D2R N4 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<5>	PEG D2R N5 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<6>	PEG D2R N6 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<7>	PEG D2R N7 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<8>	PEG D2R N8 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<9>	PEG D2R N9 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<10>	PEG D2R N10 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<11>	PEG D2R N11 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<12>	PEG D2R N12 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<13>	PEG D2R N13 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<14>	PEG D2R N14 SPN	MAKE_BASE-TRUE	5
13	PEG D2R N<15>	PEG D2R N15 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<0>	PEG D2R P0 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<2>	PEG D2R P2 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<3>	PEG D2R P3 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<4>	PEG D2R P4 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<5>	PEG D2R P5 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<6>	PEG D2R P6 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<7>	PEG D2R P7 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<8>	PEG D2R P8 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<9>	PEG D2R P9 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<10>	PEG D2R P10 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<11>	PEG D2R P11 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<12>	PEG D2R P12 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<13>	PEG D2R P13 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<14>	PEG D2R P14 SPN	MAKE_BASE-TRUE	5
13	PEG D2R P<15>	PEG D2R P15 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<4>	PEG R2D C N4 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<5>	PEG R2D C N5 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<6>	PEG R2D C N6 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<7>	PEG R2D C N7 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<8>	PEG R2D C N8 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<9>	PEG R2D C N9 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<10>	PEG R2D C N10 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<11>	PEG R2D C N11 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<12>	PEG R2D C N12 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<13>	PEG R2D C N13 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<14>	PEG R2D C N14 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C N<15>	PEG R2D C N15 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<4>	PEG R2D C P4 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<5>	PEG R2D C P5 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<6>	PEG R2D C P6 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<7>	PEG R2D C P7 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<8>	PEG R2D C P8 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<9>	PEG R2D C P9 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<10>	PEG R2D C P10 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<11>	PEG R2D C P11 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<12>	PEG R2D C P12 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<13>	PEG R2D C P13 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<14>	PEG R2D C P14 SPN	MAKE_BASE-TRUE	5
13	PEG R2D C P<15>	PEG R2D C P15 SPN	MAKE_BASE-TRUE	5

### NB CFG ALIASES

NO-CONNECT UNUSED CFG INTERFACE PORTS

14	NB_CFG<3>	TP_NB_CFG3	MAKE_BASE-TRUE	5
14	NB_CFG<4>	TP_NB_CFG4	MAKE_BASE-TRUE	5
14	NB_CFG<6>	TP_NB_CFG6	MAKE_BASE-TRUE	5
14	NB_CFG<8>	TP_NB_CFG8	MAKE_BASE-TRUE	5
14	NB_CFG<10>	TP_NB_CFG10	MAKE_BASE-TRUE	5
14	NB_CFG<11>	TP_NB_CFG11	MAKE_BASE-TRUE	5
14	NB_CFG<12>	TP_NB_CFG12	MAKE_BASE-TRUE	5
14	NB_CFG<13>	TP_NB_CFG13	MAKE_BASE-TRUE	5
14	NB_CFG<14>	TP_NB_CFG14	MAKE_BASE-TRUE	5
14	NB_CFG<15>	TP_NB_CFG15	MAKE_BASE-TRUE	5
14	NB_CFG<17>	TP_NB_CFG17	MAKE_BASE-TRUE	5

### FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

38	FW_B_TPBIAIS	FW_B_TPBIAIS_SPN	MAKE_BASE-TRUE	5
38	FW_B_TPA_P	FW_B_TPA_P_SPN	MAKE_BASE-TRUE	5
38	FW_B_TPA_N	FW_B_TPA_N_SPN	MAKE_BASE-TRUE	5
38	FW_B_TPB_P	FW_B_TPB_P_SPN	MAKE_BASE-TRUE	5
38	FW_B_TPB_N	FW_B_TPB_N_SPN	MAKE_BASE-TRUE	5
38	FW_C_TPBIAIS	FW_C_TPBIAIS_SPN	MAKE_BASE-TRUE	5
38	FW_C_TPA_P	FW_C_TPA_P_SPN	MAKE_BASE-TRUE	5
38	FW_C_TPA_N	FW_C_TPA_N_SPN	MAKE_BASE-TRUE	5
38	FW_C_TPB_P	FW_C_TPB_P_SPN	MAKE_BASE-TRUE	5
38	FW_C_TPB_N	FW_C_TPB_N_SPN	MAKE_BASE-TRUE	5
39	FWPWR_PWRON	NC_FWPWR_PWRON	NO_TEST-TRUE	5

### SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

21	SATA_A_D2R_N	SATA_A_D2R_N_SPN	MAKE_BASE-TRUE	5
21	SATA_A_D2R_P	SATA_A_D2R_P_SPN	MAKE_BASE-TRUE	5
21	SATA_A_R2D_C_N	SATA_A_R2D_C_N_SPN	MAKE_BASE-TRUE	5
21	SATA_A_R2D_C_P	SATA_A_R2D_C_P_SPN	MAKE_BASE-TRUE	5

### PCI\_EXP ALIASES

NO-CONNECT UNUSED PCI\_EXP INTERFACE PORTS

22	PCIE_C_D2R_N	PCIE_C_D2R_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_C_D2R_P	PCIE_C_D2R_P_SPN	MAKE_BASE-TRUE	5
22	PCIE_C_R2D_C_N	PCIE_C_R2D_C_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_C_R2D_C_P	PCIE_C_R2D_C_P_SPN	MAKE_BASE-TRUE	5
22	PCIE_D_D2R_N	PCIE_D_D2R_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_D_D2R_P	PCIE_D_D2R_P_SPN	MAKE_BASE-TRUE	5
22	PCIE_D_R2D_C_N	PCIE_D_R2D_C_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_D_R2D_C_P	PCIE_D_R2D_C_P_SPN	MAKE_BASE-TRUE	5
22	PCIE_E_D2R_N	PCIE_E_D2R_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_E_D2R_P	PCIE_E_D2R_P_SPN	MAKE_BASE-TRUE	5
22	PCIE_E_R2D_C_N	PCIE_E_R2D_C_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_E_R2D_C_P	PCIE_E_R2D_C_P_SPN	MAKE_BASE-TRUE	5
22	PCIE_F_D2R_N	PCIE_F_D2R_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_F_D2R_P	PCIE_F_D2R_P_SPN	MAKE_BASE-TRUE	5
22	PCIE_F_R2D_C_N	PCIE_F_R2D_C_N_SPN	MAKE_BASE-TRUE	5
22	PCIE_F_R2D_C_P	PCIE_F_R2D_C_P_SPN	MAKE_BASE-TRUE	5

### CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

32	CK410_SRC1_N	CK410_SRC1_N_SPN	MAKE_BASE-TRUE	5
32	CK410_SRC1_P	CK410_SRC1_P_SPN	MAKE_BASE-TRUE	5
32	CK410_SRC3_N	CK410_SRC3_N_SPN	MAKE_BASE-TRUE	5
32	CK410_SRC3_P	CK410_SRC3_P_SPN	MAKE_BASE-TRUE	5
32	CK410_SRC7_N	CK410_SRC7_N_SPN	MAKE_BASE-TRUE	5
32	CK410_SRC7_P	CK410_SRC7_P_SPN	MAKE_BASE-TRUE	5
32	CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L_SPN	MAKE_BASE-TRUE	5
32	CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L_SPN	MAKE_BASE-TRUE	5

### SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

23	SUS_CLK_SB	SUS_CLK_SB_SPN	MAKE_BASE-TRUE	5
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### SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

28	MEM_A_A<15>	MEM_A_A15_SPN	MAKE_BASE-TRUE	5
28	MEM_A_A<14>	MEM_A_A14_SPN	MAKE_BASE-TRUE	5
29	MEM_B_A<15>	MEM_B_A15_SPN	MAKE_BASE-TRUE	5
29	MEM_B_A<14>	MEM_B_A14_SPN	MAKE_BASE-TRUE	5

### Ethernet ALIASES

36	ENET_CTRL12	ENET_CTRL12_SPN	MAKE_BASE-TRUE	5
36	ENET_CTRL25	ENET_CTRL25_SPN	MAKE_BASE-TRUE	5

### SIGNAL ALIAS /RESET

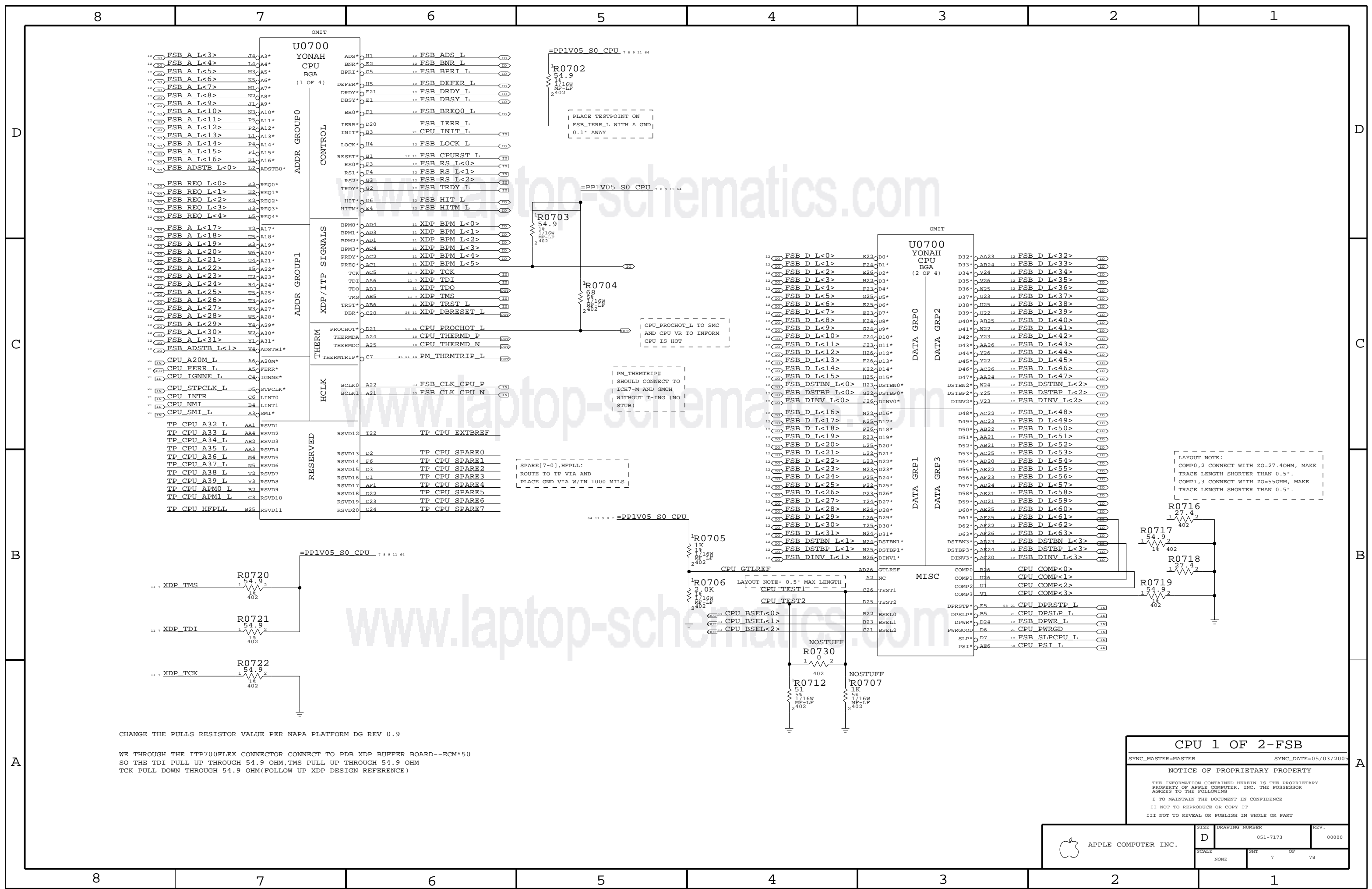
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0722	4	THERMAL STANDOFF	Z0603,Z0604,Z0605,Z0621	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0612	STANDOFF
860-0749	1	STANDOFF W/TBU HOLES,WIRELESS	Z0613	STANDOFF

APPLE COMPUTER INC.

DRAWING NUMBER: 051-7173  
 REV: 00000

SCALE: NONE  
 SHEET: 6 OF 78



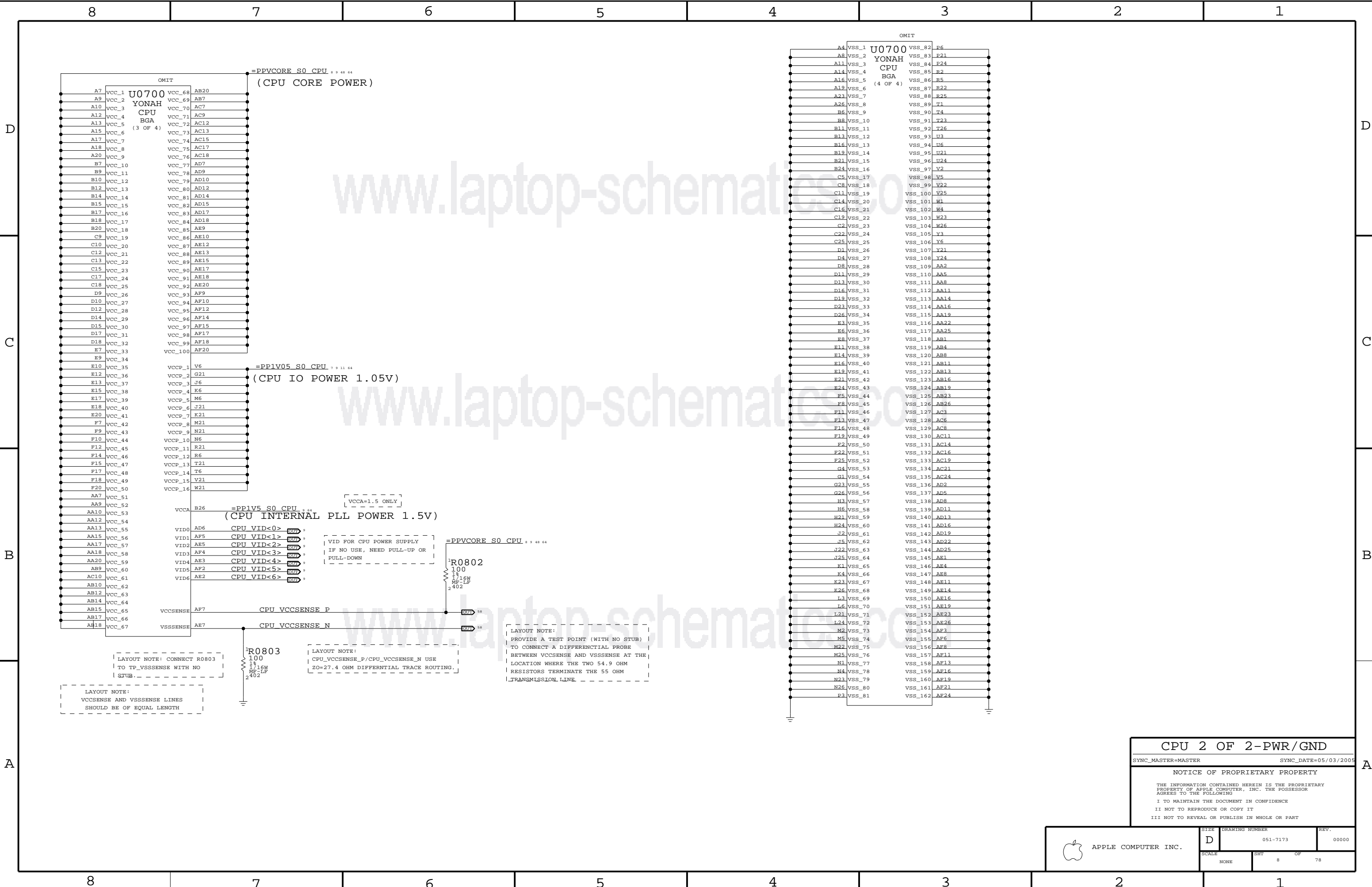
CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM\*50 SO THE TDI PULL UP THROUGH 54.9 OHM, TMS PULL UP THROUGH 54.9 OHM TCK PULL DOWN THROUGH 54.9 OHM (FOLLOW UP XDP DESIGN REFERENCE)

**CPU 1 OF 2-FSB**  
 SYNC\_MASTER=MASTER SYNC\_DATE=05/03/2005

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NONE	7		



**CPU 2 OF 2-PWR/GND**

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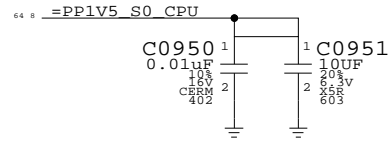
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NONE	8		78

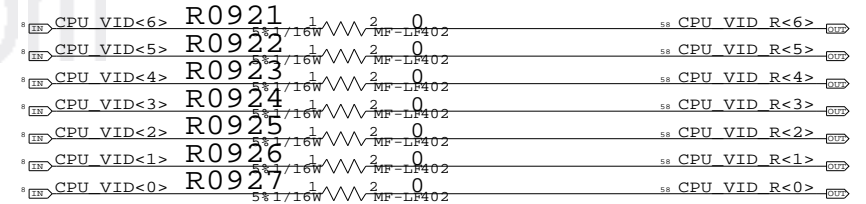


VCCA DECOUPLING  
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY

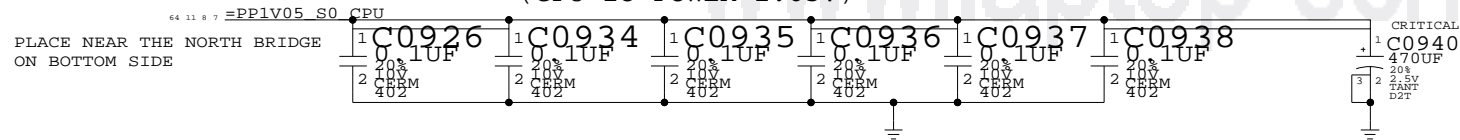
CPU CORE VID<> SETTINGS



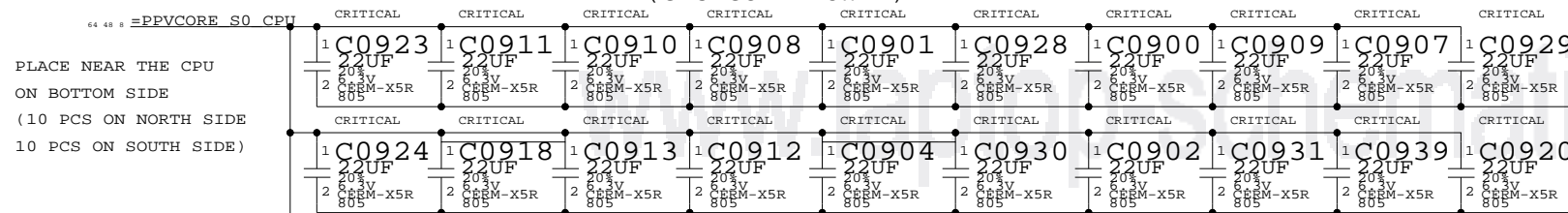
R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

VCCP CORE DECOUPLING  
(CPU IO POWER 1.05V)

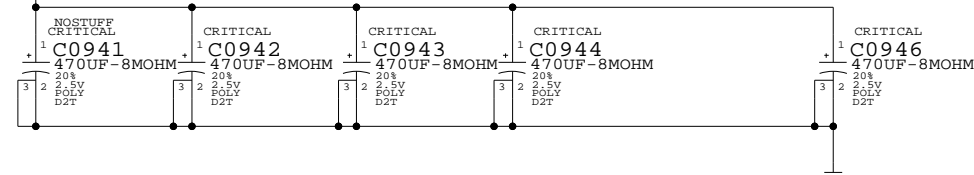
THIS 470UF FOR CPU, GMCH FSB BUS 1.05V



VCC CORE DECOUPLING  
(CPU CORE POWER)



IF WE USE LOW ESL CAP, THEN WE CAN USE 20 PCS 22UF CAP



	MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM	1.1625	1.30
	VCCLFM	TBD	TBD
SINGLE CORE SV CPU	VCCHFM	1.1625	1.30
	VCCLFM		TBD
DUAL CORE LV CPU	VCCHFM	1.0	1.1625
	VCCLFM		TBD
ULV CPU	VCCHFM	TBD	TBD
	VCCLFM		TBD

UNIT: V

- # ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
- # TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE (VCORE VOLTAGE)!
- # REFER TO YONAH PROCESSOR EMTS REV 1.0
- # VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
- # VCCLFM: VCORE AT LOWEST FREQUENCY MODE

CPU DECAPS & VID<>

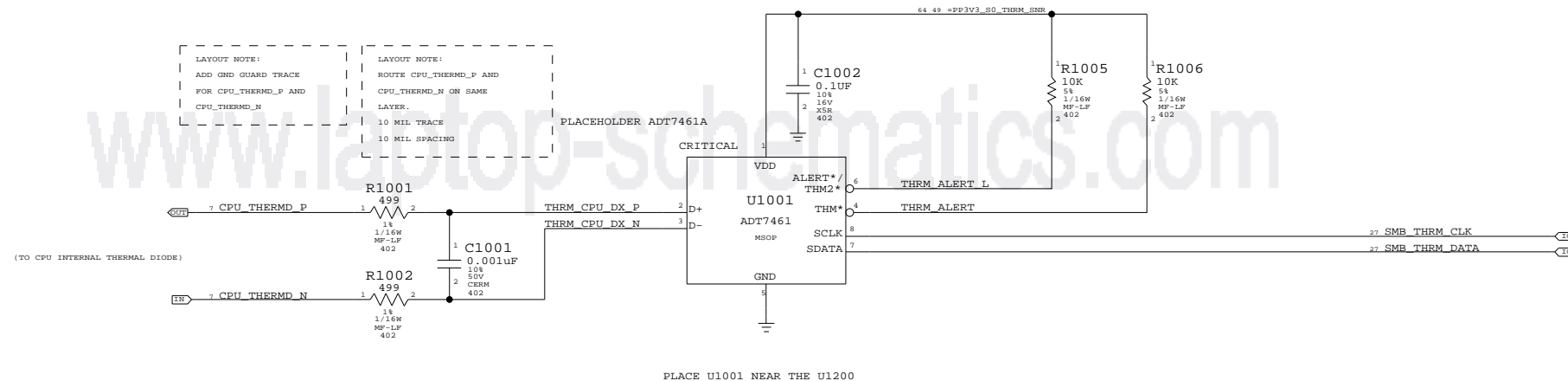
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NONE	9	78	

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### CPU ZONE THERMAL SENSOR



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CPU MISC1-TEMP SENSOR  
SYNC\_MASTER=ENET SYNC\_DATE=08/19/2005  
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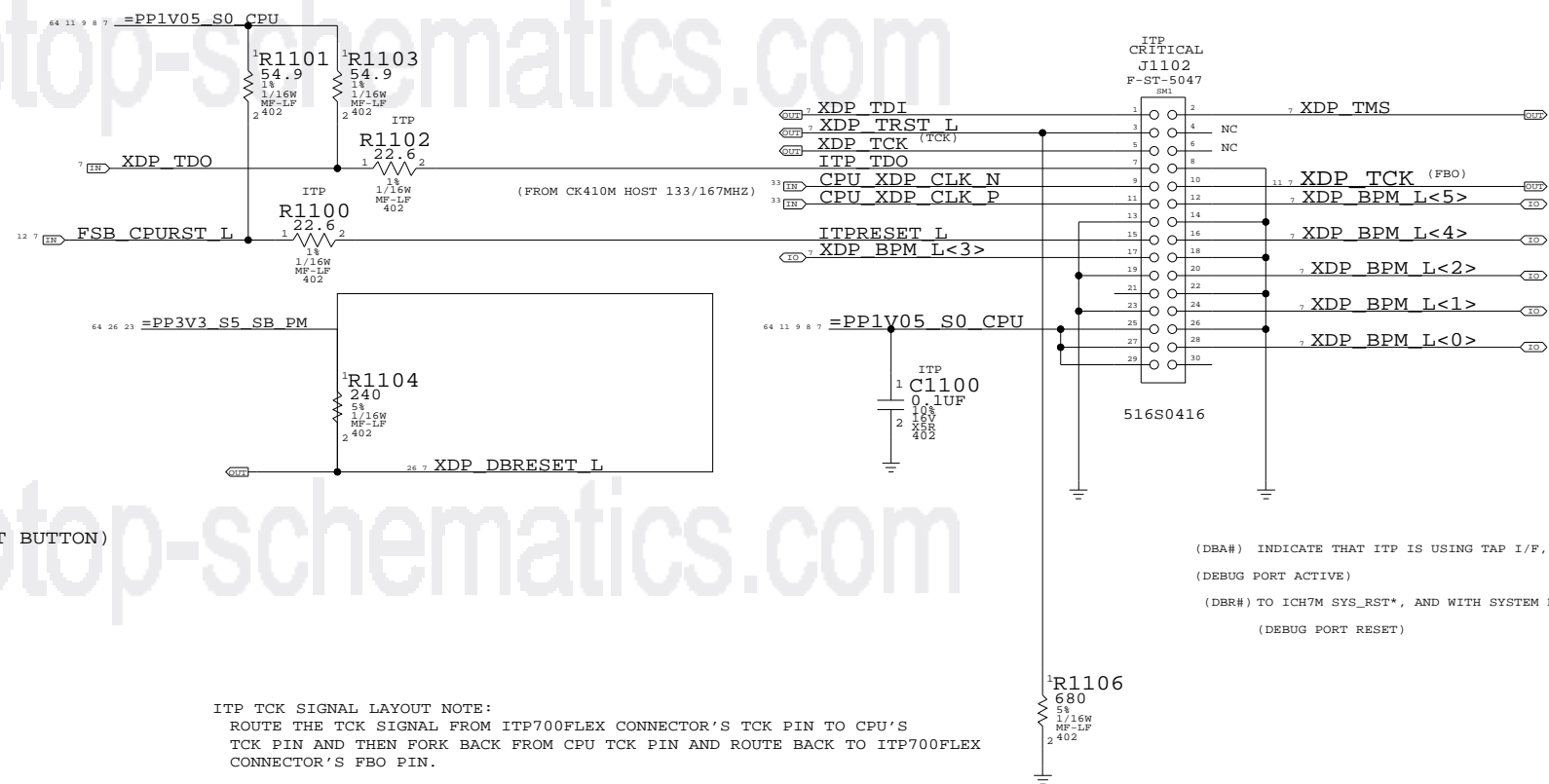
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NONE	10	78	

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### CPU ITP700FLEX DEBUG SUPPORT

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(AND WITH RESET BUTTON)

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.  
(DEBUG PORT ACTIVE)  
(DBR#) TO ICH7M SYS\_RST\*, AND WITH SYSTEM RESET LOGIC  
(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:  
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
CONNECTOR'S FBO PIN.

**CPU ITP700FLEX DEBUG**  
SYNC\_MASTER=MASTER SYNC\_DATE=5/23/05  
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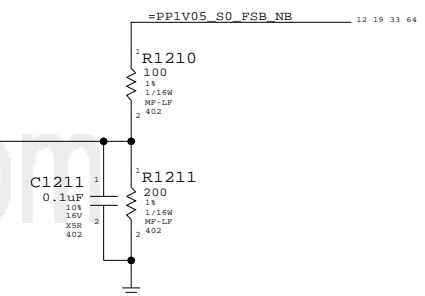
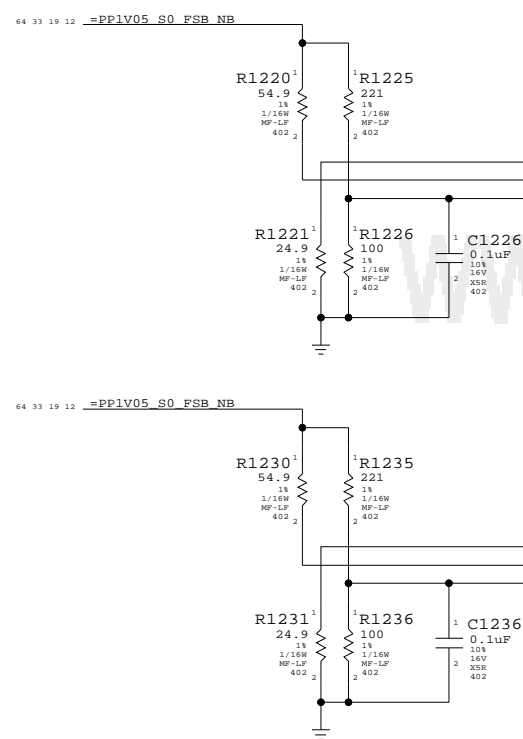
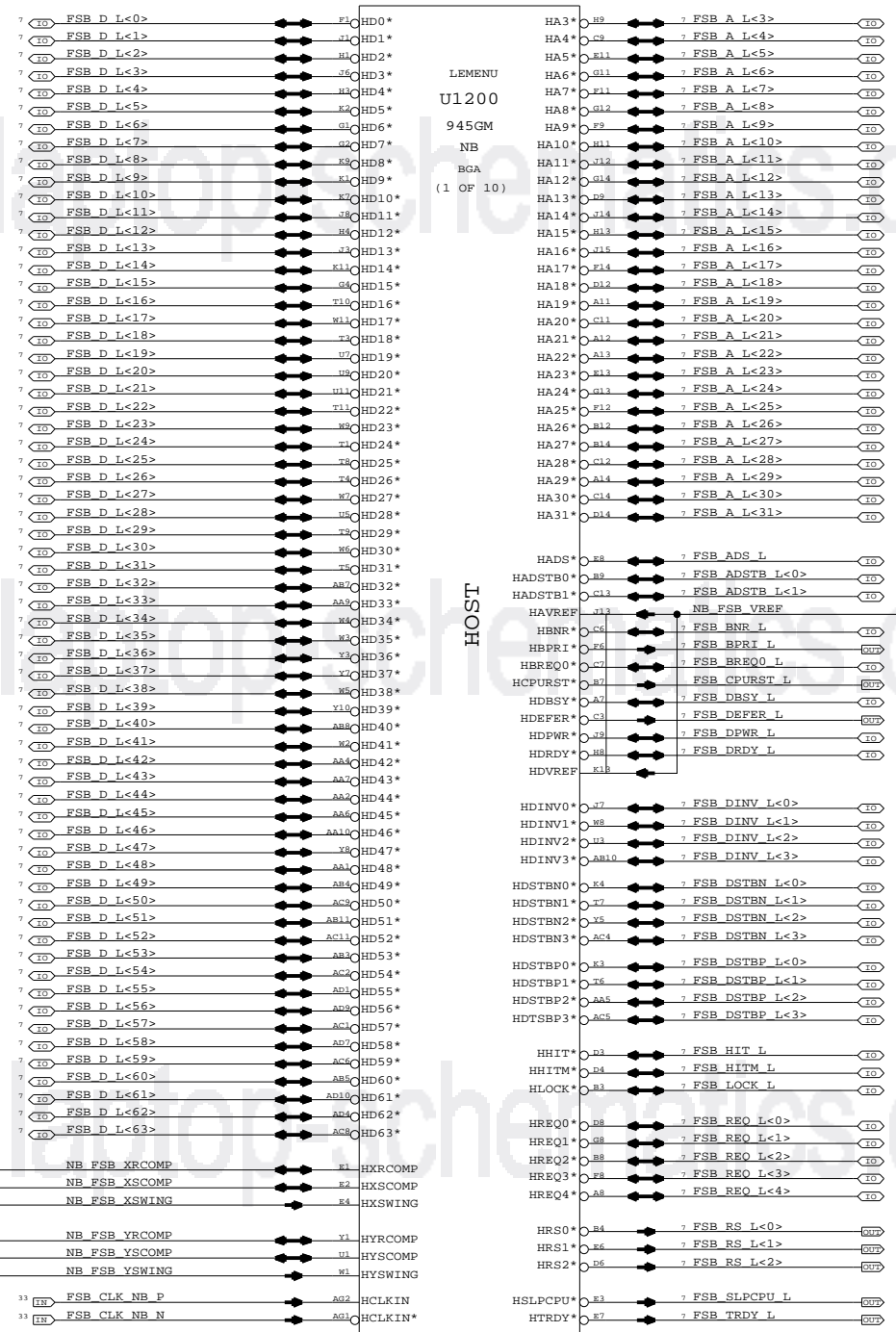
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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	11		

D

C

B

A



NB CPU Interface

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

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SCALE	SHT	OF	78
NONE	12		



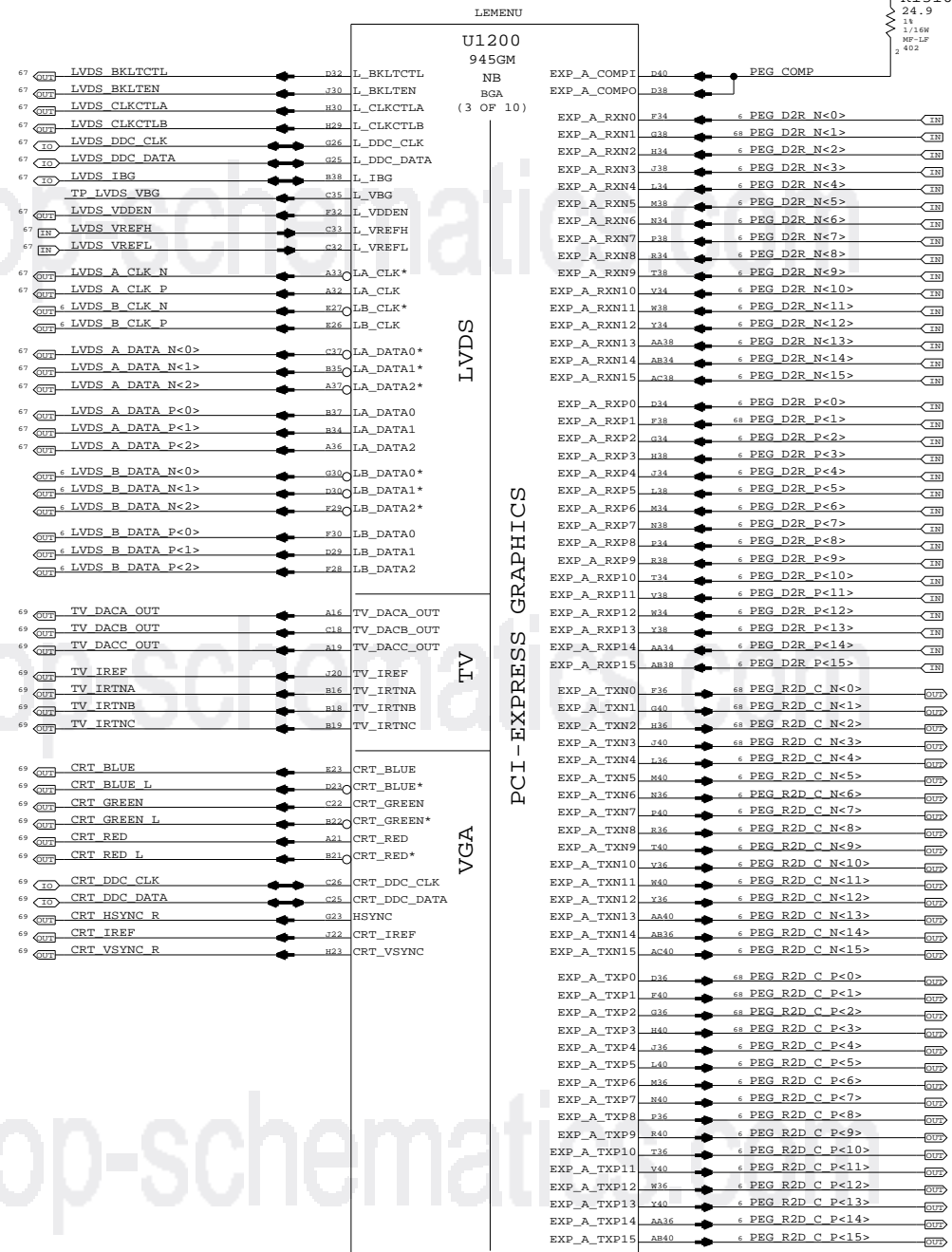
**LVDS Disable**  
 Can leave all signals NC if LVDS is not implemented  
 Tie VCC\_TXLVDS and VCCA\_LVDS to GND. If SDVO is used  
 VCCD\_LVDS must remain powered with proper decoupling.  
 Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**  
 Composite: DACA only  
 S-Video: DACB & DACC only  
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit  
 filtering components. Unused DAC outputs should  
 connect to GND through 75-ohm resistors.

**TV-Out Disable**  
 Tie DACx\_OUT, IRTNx, and IREF to 1.5V power rail.  
 Tie VCCD\_TVDAC, VCCD\_QTVDAC, VCCA\_TVDACx, and  
 VCCA\_TVVBG to 1.5V power rail. Tie VSSA\_TVVBG to GND.

**CRT Disable**  
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie  
 HSYNC and VSYNC to GND. Tie VCCA\_CRTDAC to VCC Core  
 rail, and tie VSSA\_CRTDAC and VCC\_SYNC to GND.



SDVO Alternate Function

SDVO\_TVCLKIN#  
 SDVO\_INT#  
 SDVO\_FLDSTALL#

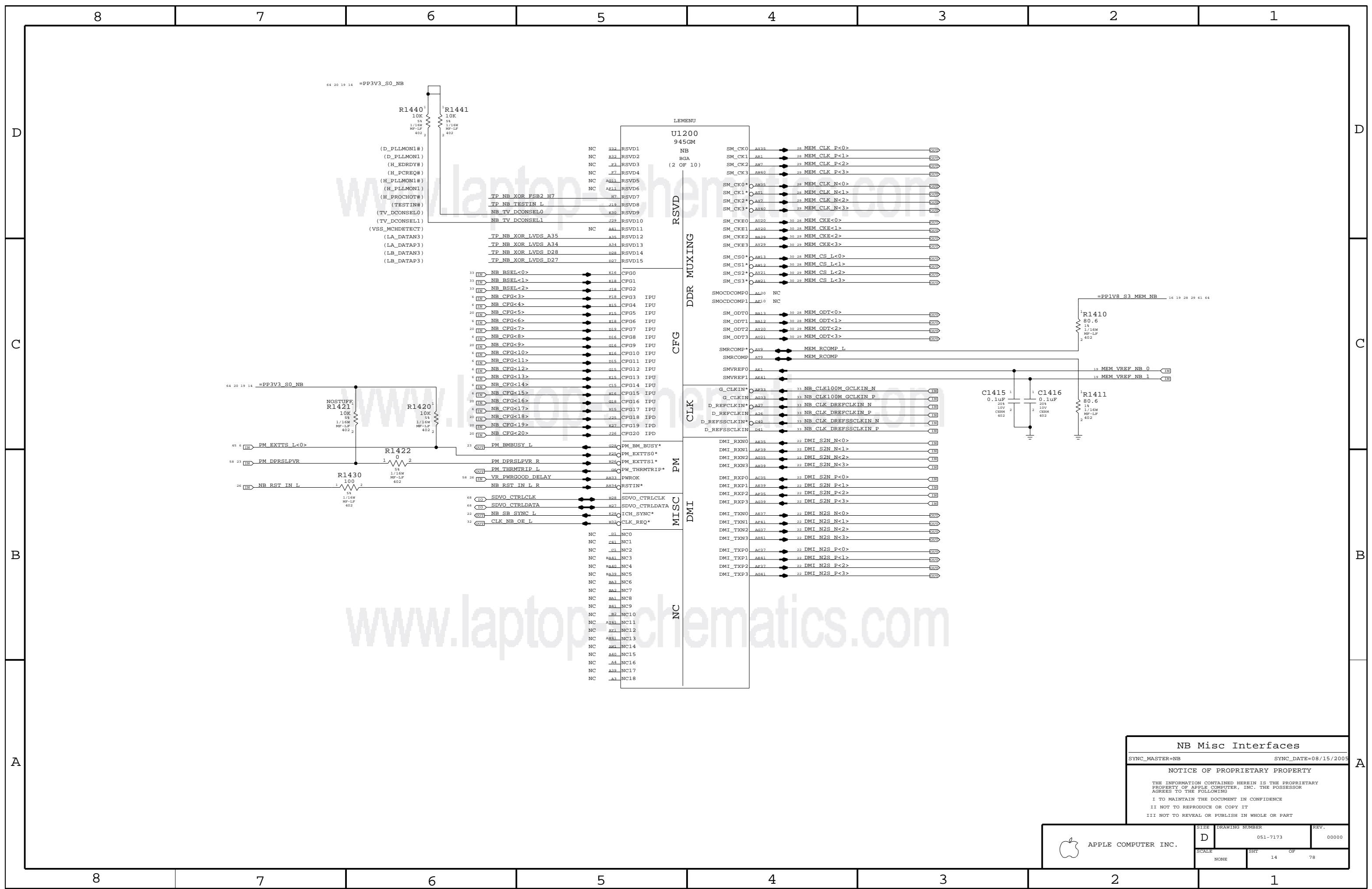
SDVO\_TVCLKIN  
 SDVO\_INT  
 SDVO\_FLDSTALL

SDVOB\_RED#  
 SDVOB\_GREEN#  
 SDVOB\_BLUE#  
 SDVOB\_CLKN  
 SDVOC\_RED#  
 SDVOC\_GREEN#  
 SDVOC\_BLUE#  
 SDVOC\_CLKN

SDVOB\_RED  
 SDVOB\_GREEN  
 SDVOB\_BLUE  
 SDVOB\_CLKP  
 SDVOC\_RED  
 SDVOC\_GREEN  
 SDVOC\_BLUE  
 SDVOC\_CLKP

**NB PEG / Video Interfaces**  
 SYNC\_MASTER=NB SYNC\_DATE=07/25/2005  
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NONE	13		78



**NB Misc Interfaces**

SYNC\_MASTER=NB SYNC\_DATE=08/15/2005

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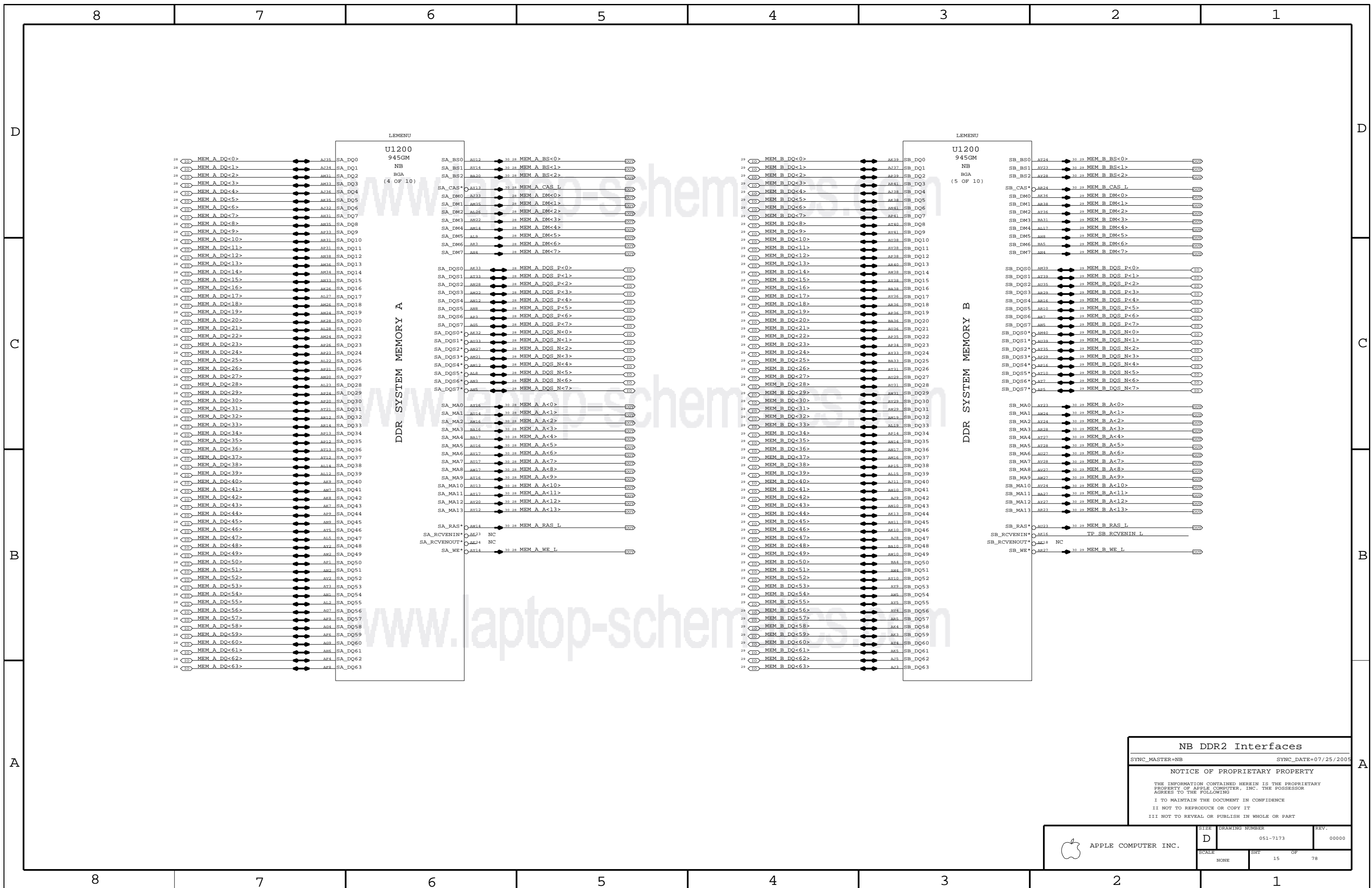
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 14	OF 78



**NB DDR2 Interfaces**

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

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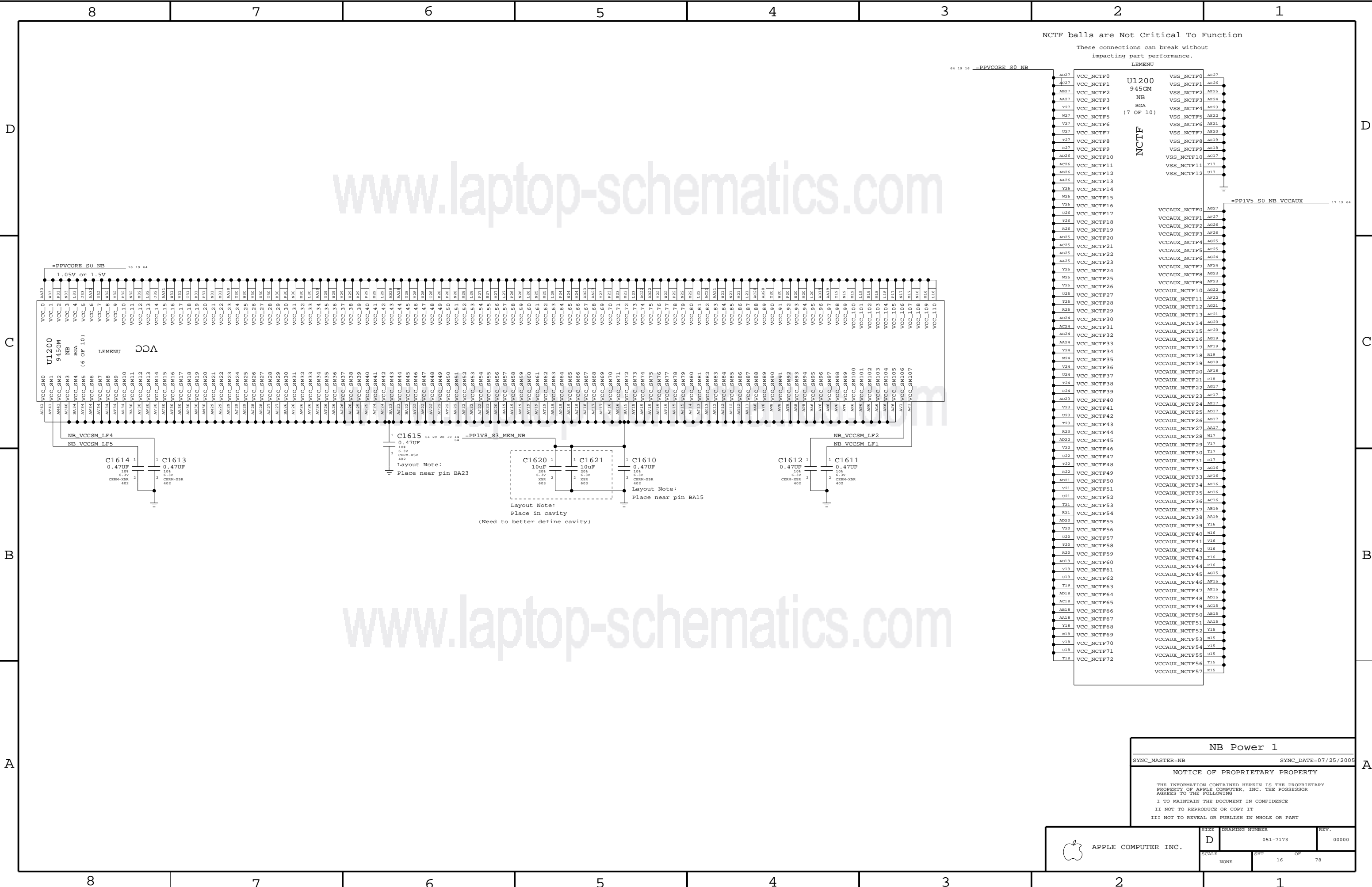
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	SCALE: NONE	SHEET: 15	OF: 78



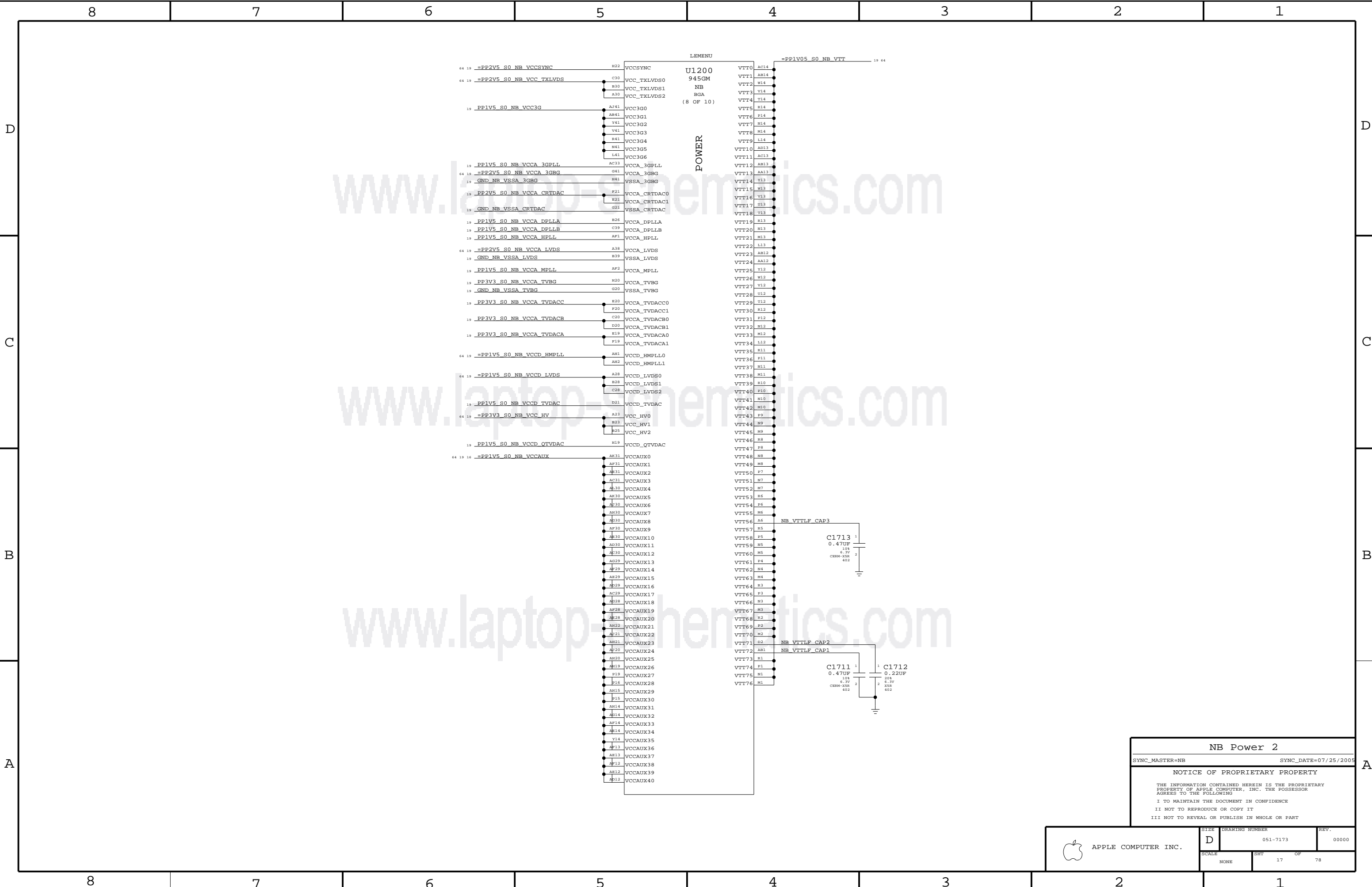
NCTF balls are Not Critical To Function  
 These connections can break without impacting part performance.

U1200  
 945GM  
 NB  
 BGA  
 (7 OF 10)  
 NCTF

VCC NCTF0  
 VCC NCTF1  
 VCC NCTF2  
 VCC NCTF3  
 VCC NCTF4  
 VCC NCTF5  
 VCC NCTF6  
 VCC NCTF7  
 VCC NCTF8  
 VCC NCTF9  
 VCC NCTF10  
 VCC NCTF11  
 VCC NCTF12  
 VCC NCTF13  
 VCC NCTF14  
 VCC NCTF15  
 VCC NCTF16  
 VCC NCTF17  
 VCC NCTF18  
 VCC NCTF19  
 VCC NCTF20  
 VCC NCTF21  
 VCC NCTF22  
 VCC NCTF23  
 VCC NCTF24  
 VCC NCTF25  
 VCC NCTF26  
 VCC NCTF27  
 VCC NCTF28  
 VCC NCTF29  
 VCC NCTF30  
 VCC NCTF31  
 VCC NCTF32  
 VCC NCTF33  
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 VCC NCTF35  
 VCC NCTF36  
 VCC NCTF37  
 VCC NCTF38  
 VCC NCTF39  
 VCC NCTF40  
 VCC NCTF41  
 VCC NCTF42  
 VCC NCTF43  
 VCC NCTF44  
 VCC NCTF45  
 VCC NCTF46  
 VCC NCTF47  
 VCC NCTF48  
 VCC NCTF49  
 VCC NCTF50  
 VCC NCTF51  
 VCC NCTF52  
 VCC NCTF53  
 VCC NCTF54  
 VCC NCTF55  
 VCC NCTF56  
 VCC NCTF57

NB Power 1  
 SYNC\_MASTER=NB SYNC\_DATE=07/25/2005  
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**NB Power 2**

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

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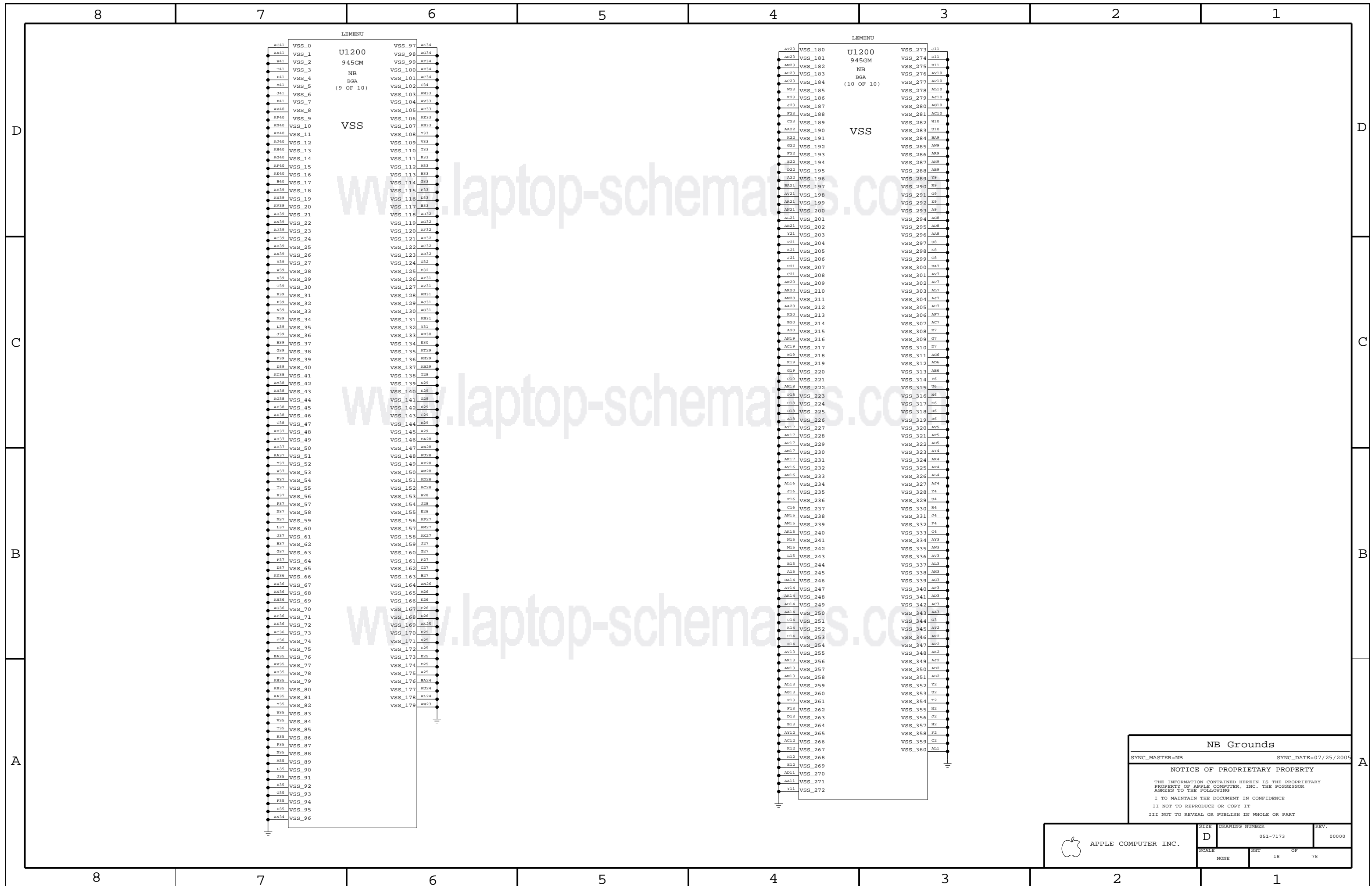
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	SCALE NONE	SHEET 17	OF 78



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NB Grounds

SYNC\_MASTER=NB SYNC\_DATE=07/25/2005

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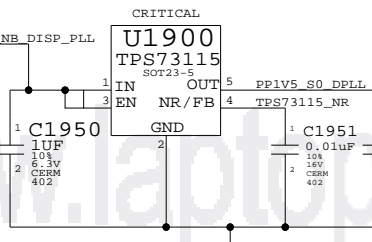
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	NONE	SHT	18 OF 78

Power Interface

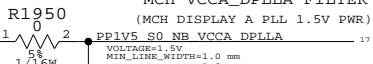
These are the power signals that leave the NB "block"

- =PP1V05\_S0\_FSB\_NB
=PPVCORE\_S0\_NB
=PP1V05\_S0\_NB
=PP1V05\_S0\_NB\_VTT
=PP1V5\_S0\_NB
=PP1V5\_S0\_NB\_PCIE
=PP1V5\_S0\_NB\_PLL
=PP1V5\_S0\_NB\_TV DAC
=PP1V5\_S0\_NB\_VCCD\_HMPLL
=PP1V5\_S0\_NB\_VCCD\_LVDS
=PP1V5\_S0\_NB\_VCCAUX
=PP1V8\_S3\_MEM\_NB
=PP2V5\_S0\_NB\_CRTDAC
=PP2V5\_S0\_NB\_VCCSYNC
=PP2V5\_S0\_NB\_VCC\_TXLVDS
=PP2V5\_S0\_NB\_VCCA\_3GBG
=PP2V5\_S0\_NB\_VCCA\_LVDS
=PP3V3\_S0\_NB
=PP3V3\_S0\_NB\_VCC\_HV
=PP5V\_S0\_NB\_TV DAC

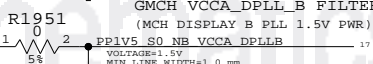
MCH DISPLAY PLL POWER LDO



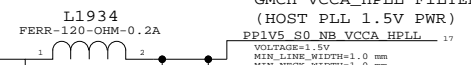
MCH VCCA\_DPLL FILTER



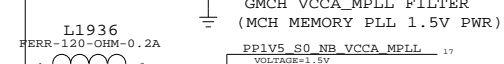
GMCH VCCA\_DPLL\_B FILTER



GMCH VCCA\_HPLL FILTER

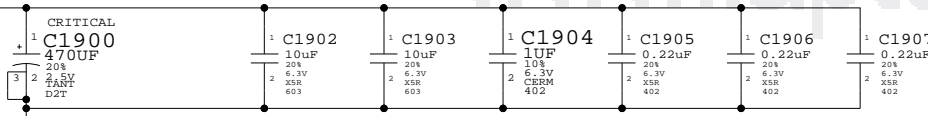


GMCH VCCA\_MPLL FILTER

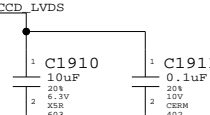


GMCH CORE PWR 1.05V BYPASS

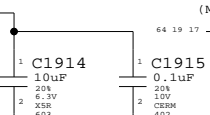
THIS 470UF FOR GMCH CORE 1.05V



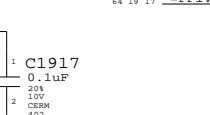
GMCH VCCD\_LVDS BYPASS



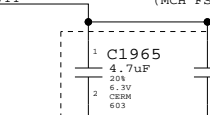
MCH VCC\_HV BYPASS



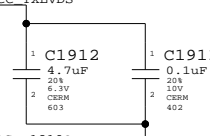
MCH VCCSYNC BYPASS



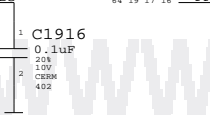
MCH VTT BYPASS



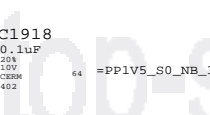
GMCH VCC\_TX LVDS BYPASS



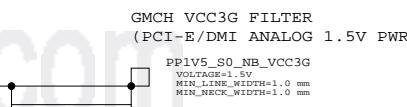
MCH VCCA\_3GBG BYPASS



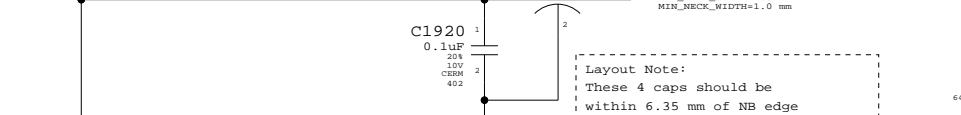
GMCH VCCAUX FILTER



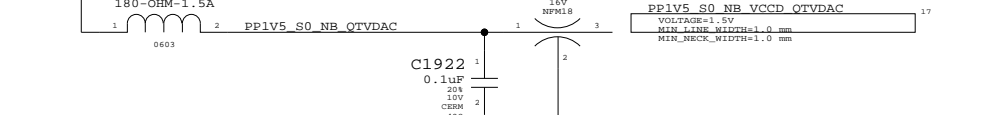
GMCH VCC3G FILTER



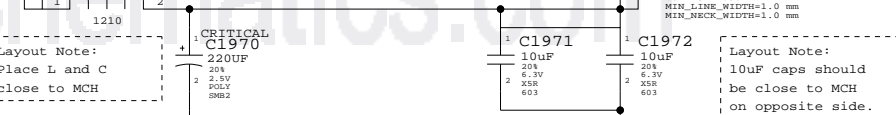
GMCH VCCD\_TV DAC FILTER



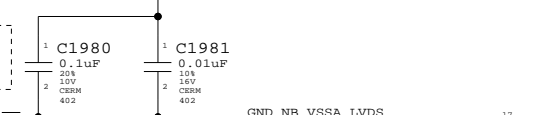
GMCH VCCD\_QTV DAC FILTER



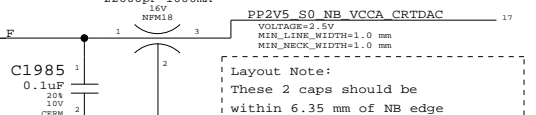
GMCH VCCA\_3GPLL FILTER



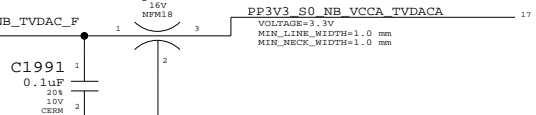
MCH VCCA\_LVDS FILTER



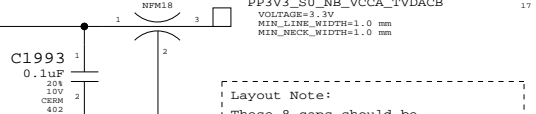
MCH VCCA\_CRTDAC BYPASS



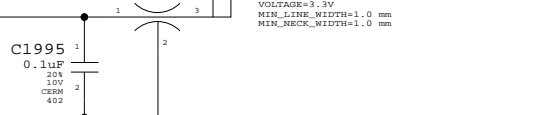
MCH VCCA\_TV DAC FILTER



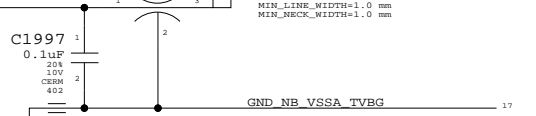
MCH VCCA\_TV DAC FILTER



MCH VCCA\_TV DAC FILTER



MCH VCCA\_TV DAC FILTER



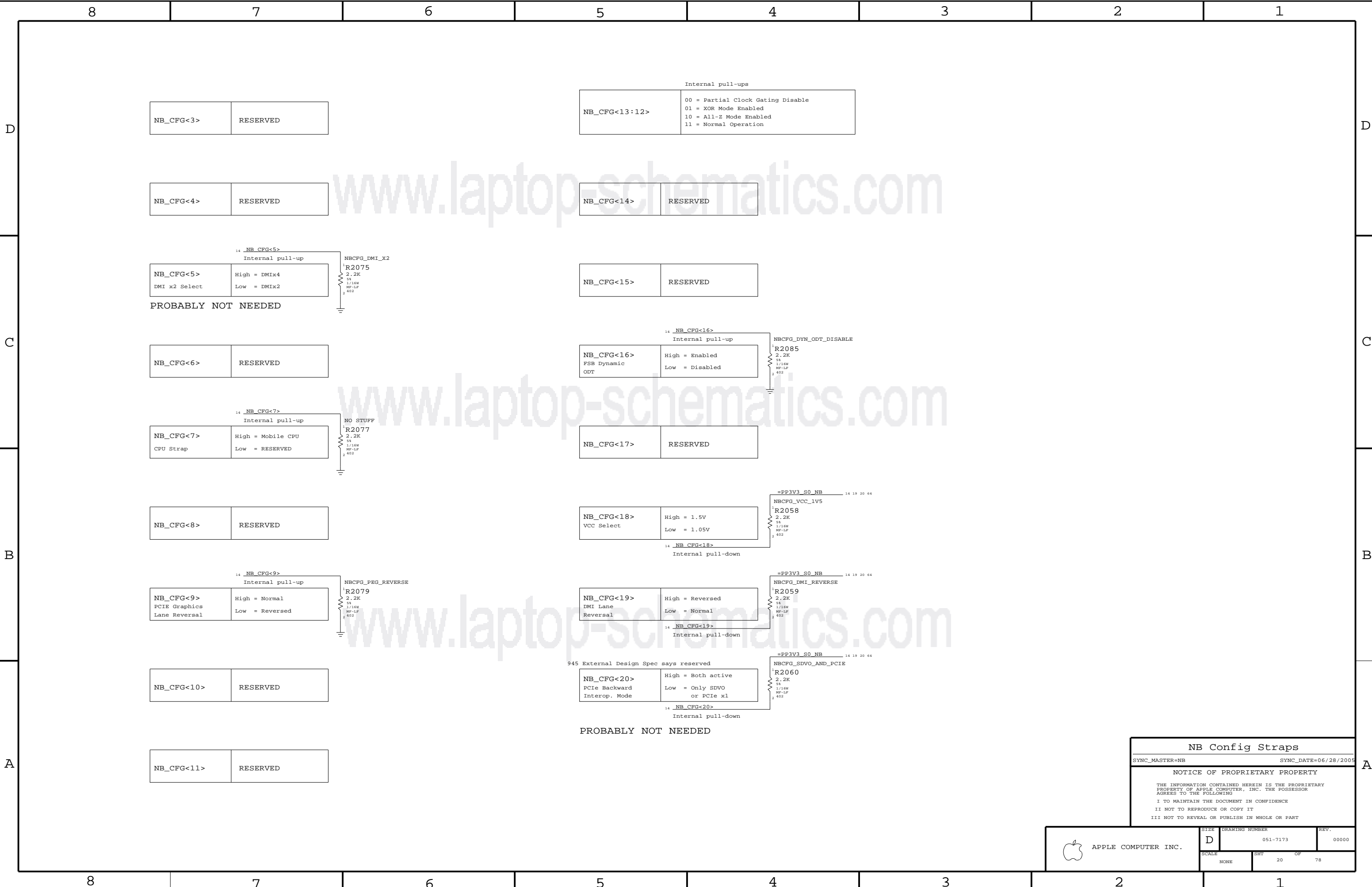
NB (GM) Decoupling

SYNC\_MASTER=NB SYNC\_DATE=06/22/2005

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Table with columns: DRAWING NUMBER (D 051-7173), REV. (00000), SCALE (NONE), SHEET (19 OF 78).





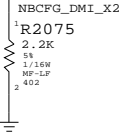
NB_CFG<3>	RESERVED
-----------	----------

Internal pull-ups	
NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<4>	RESERVED
-----------	----------

NB_CFG<14>	RESERVED
------------	----------

14 NB_CFG<5> Internal pull-up	
NB_CFG<5>	High = DMiX4 DMI x2 Select Low = DMiX2



PROBABLY NOT NEEDED

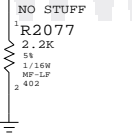
NB_CFG<15>	RESERVED
------------	----------

NB_CFG<6>	RESERVED
-----------	----------

14 NB_CFG<16> Internal pull-up	
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled



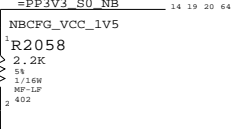
14 NB_CFG<7> Internal pull-up	
NB_CFG<7>	High = Mobile CPU CPU Strap Low = RESERVED



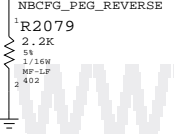
NB_CFG<17>	RESERVED
------------	----------

NB_CFG<8>	RESERVED
-----------	----------

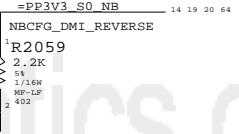
14 NB_CFG<18> Internal pull-down	
NB_CFG<18>	High = 1.5V VCC Select Low = 1.05V



14 NB_CFG<9> Internal pull-up	
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed

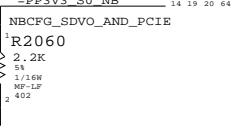


14 NB_CFG<19> Internal pull-down	
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal



NB_CFG<10>	RESERVED
------------	----------

945 External Design Spec says reserved	
14 NB_CFG<20> Internal pull-down	
NB_CFG<20>	High = Both active PCIe Backward Interop. Mode Low = Only SDVO or PCIe x1



PROBABLY NOT NEEDED

NB_CFG<11>	RESERVED
------------	----------

**NB Config Straps**

SYNC\_MASTER=NB SYNC\_DATE=06/28/2005

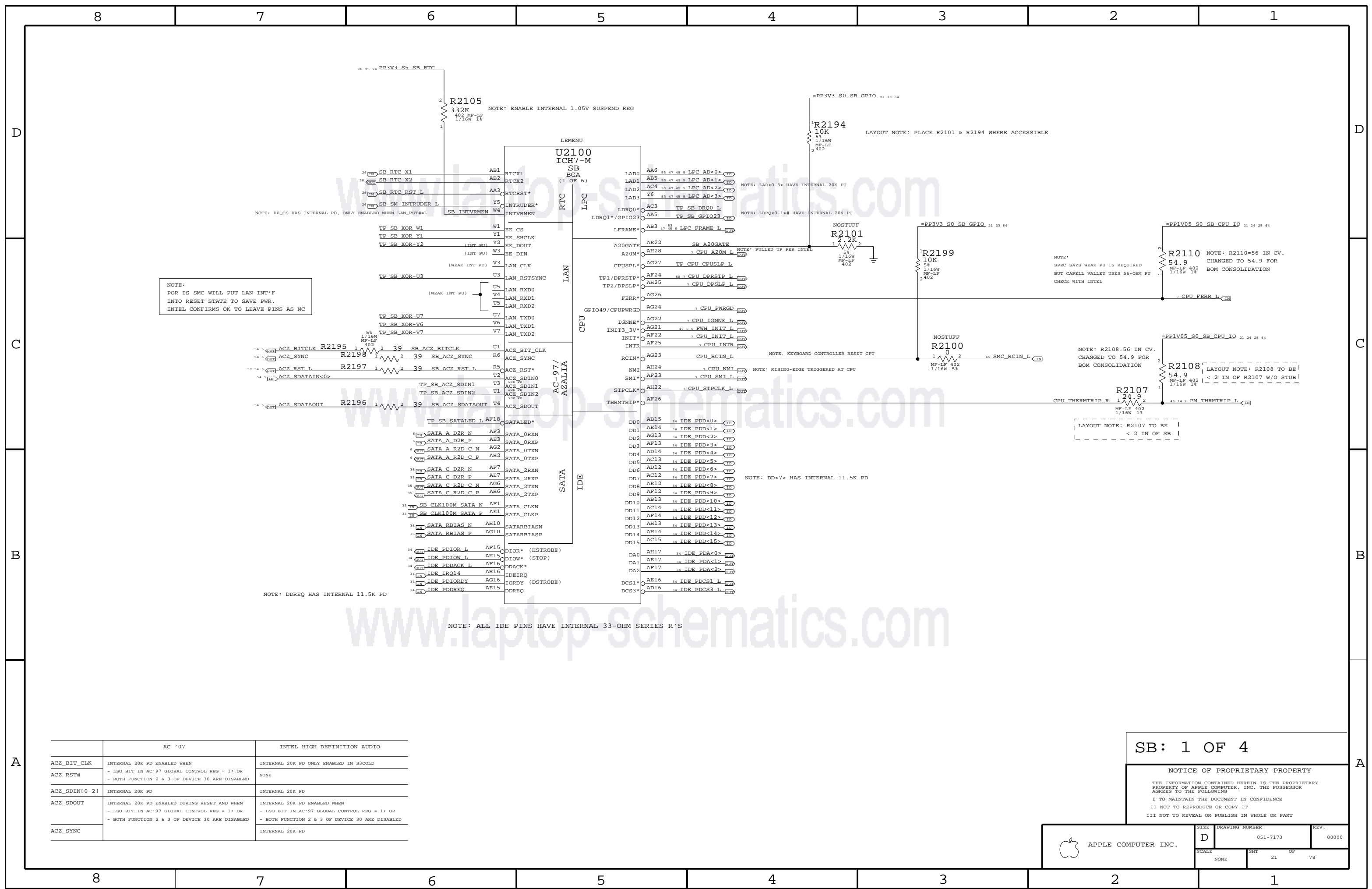
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SCALE	SHT	OF	78
NONE	20		





NOTE:  
POR IS SMC WILL PUT LAN INT'F  
INTO RESET STATE TO SAVE PWR.  
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: ER\_CS HAS INTERNAL PD, ONLY ENABLED WHEN LAN\_RST# = L

NOTE: LAD<0-3> HAVE INTERNAL 20K PU

NOTE: LDRQ<0-1># HAVE INTERNAL 20K PU

NOTE: PULLED UP PER INTEL

NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: DD<7> HAS INTERNAL 11.5K PD

LAYOUT NOTE: PLACE R2101 & R2194 WHERE ACCESSIBLE

NOTE:  
SPEC SAYS WEAK PU IS REQUIRED  
BUT CAPELL VALLEY USES 56-OHM PU  
CHECK WITH INTEL

NOTE: R2108=56 IN CV.  
CHANGED TO 54.9 FOR  
BOM CONSOLIDATION

LAYOUT NOTE: R2107 TO BE  
< 2 IN OF SB

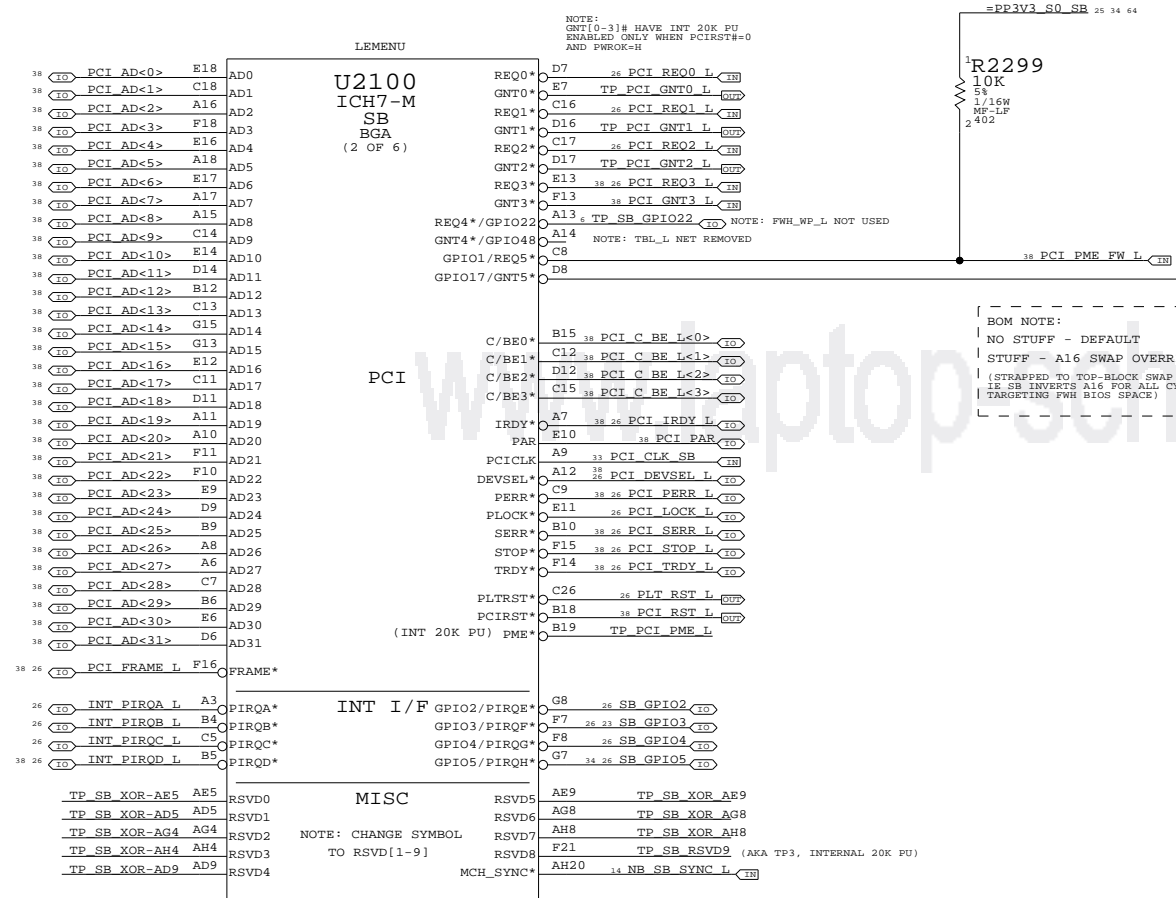
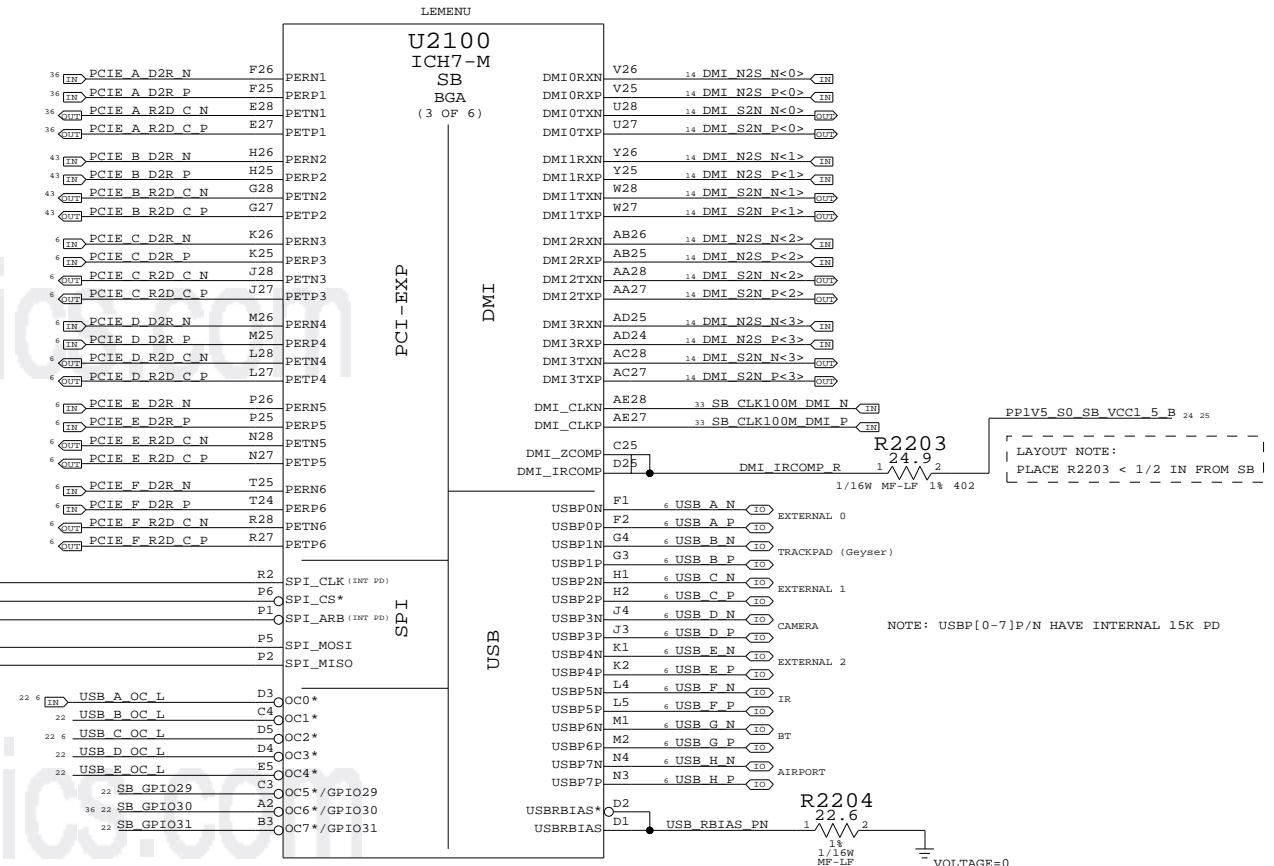
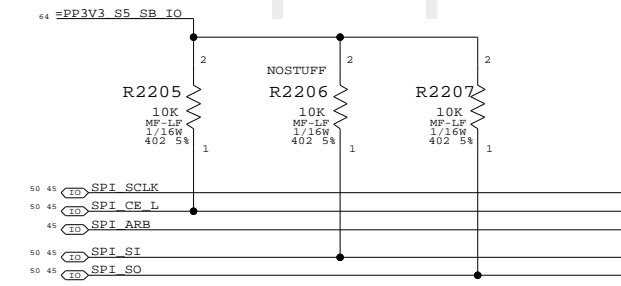
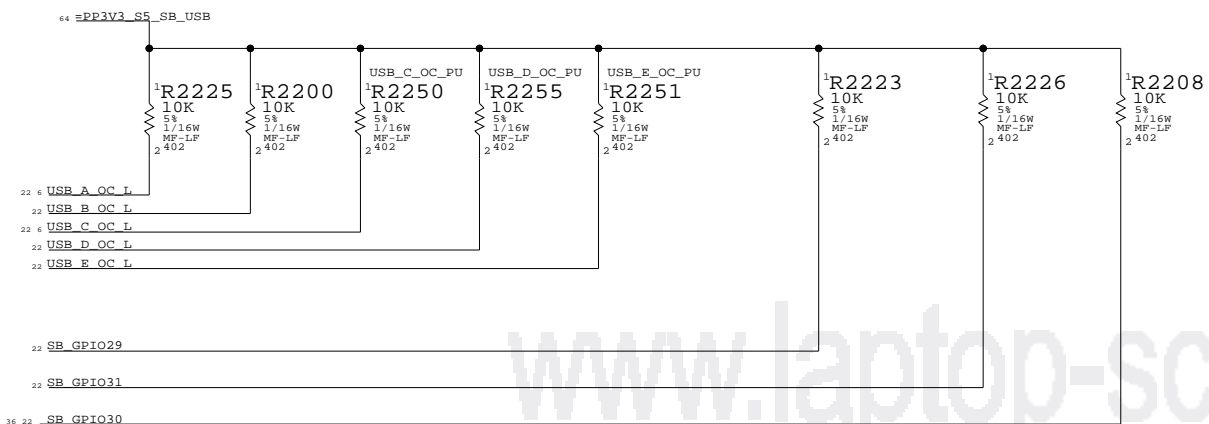
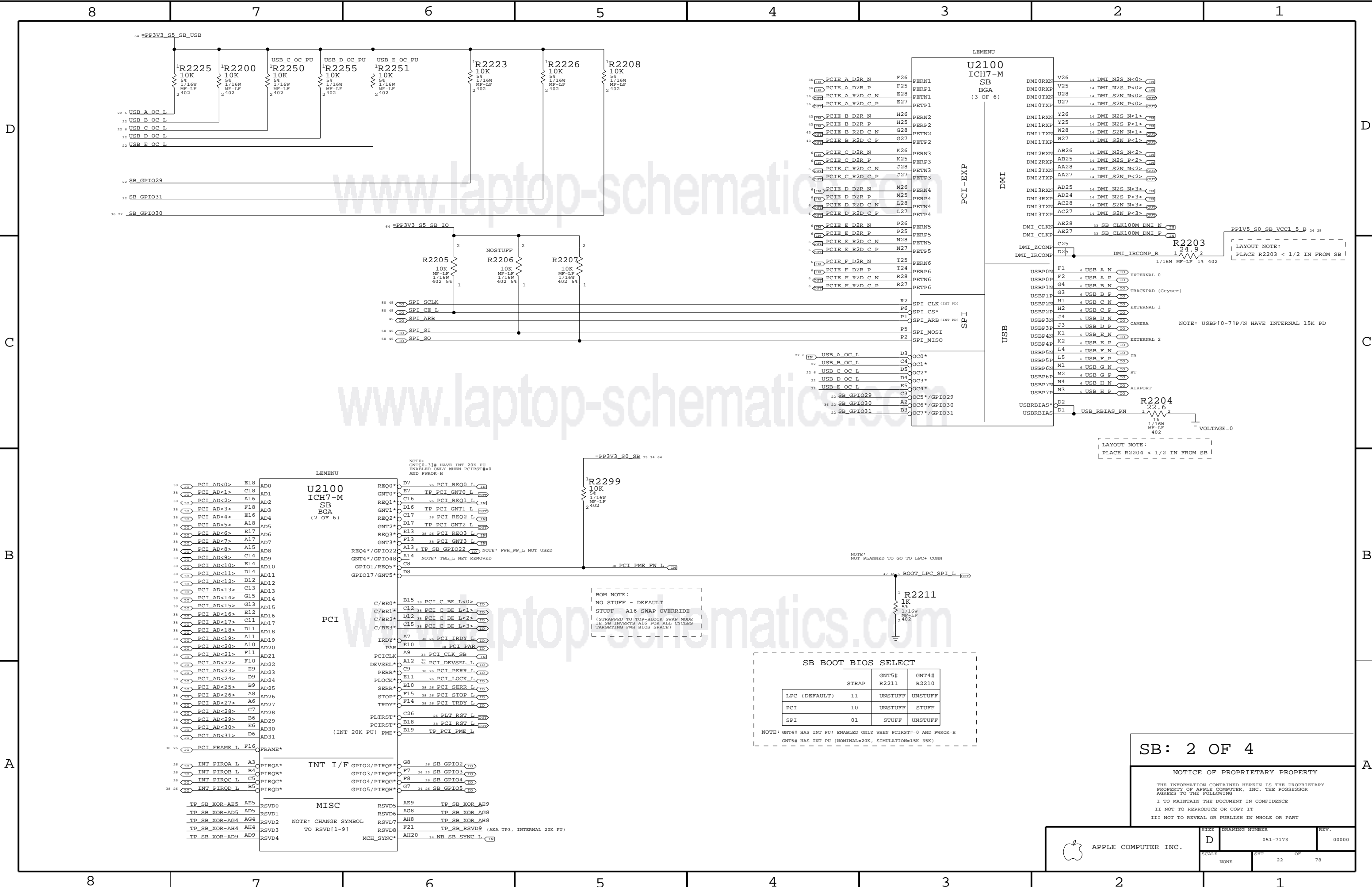
NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	NONE - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD	INTERNAL 20K PD

SB: 1 OF 4

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	NONE	SHT	21 OF 78



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU: ENABLED ONLY WHEN PCIRST#0 AND FWRC#-H

NOTE: GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB: 2 OF 4

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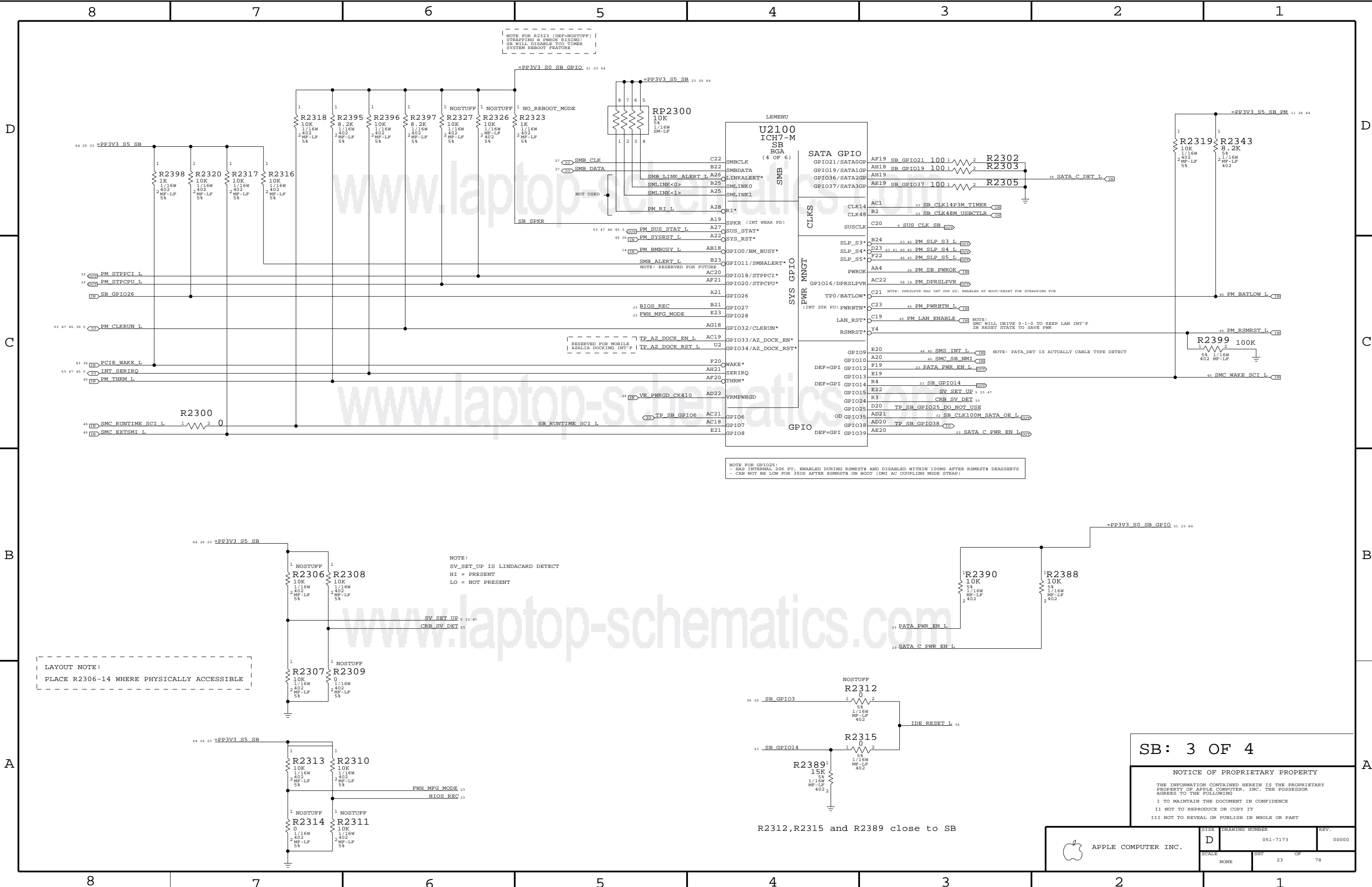
APPLE COMPUTER INC.

SCALE: NONE

SHEET: 22 OF 78

DRAWING NUMBER: 051-7173

REV: 00000



NOTE FOR R2333 (DEF-NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

NOTE FOR GPIO25:  
 - HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS  
 - CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (EMI AC COUPLING MODE STRAP)

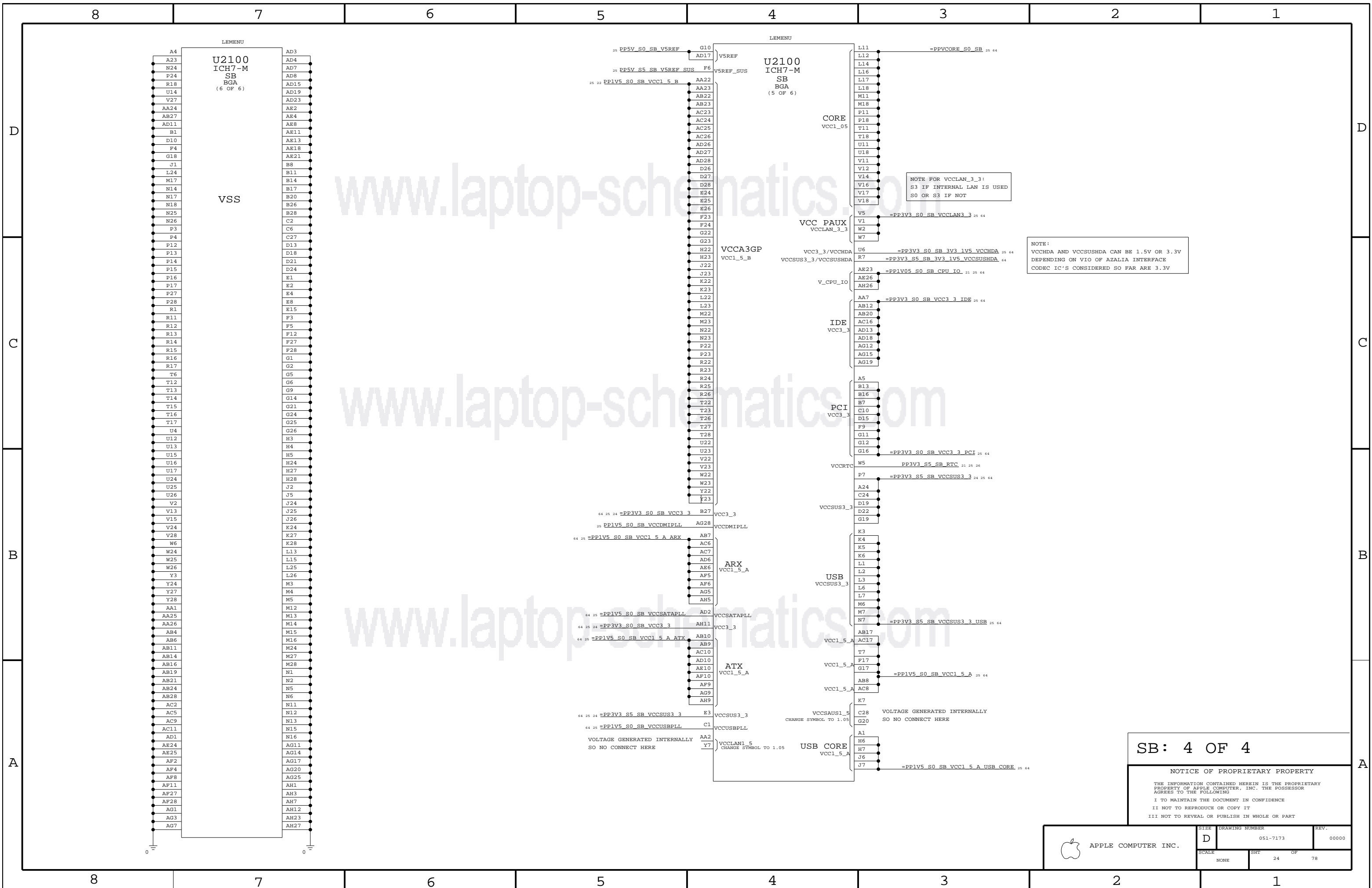
LAYOUT NOTE:  
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	NONE	SHT	23 OF 78

R2312, R2315 and R2389 close to SB



NOTE FOR VCCLAN\_3\_3:  
S3 IF INTERNAL LAN IS USED  
S0 OR S3 IF NOT

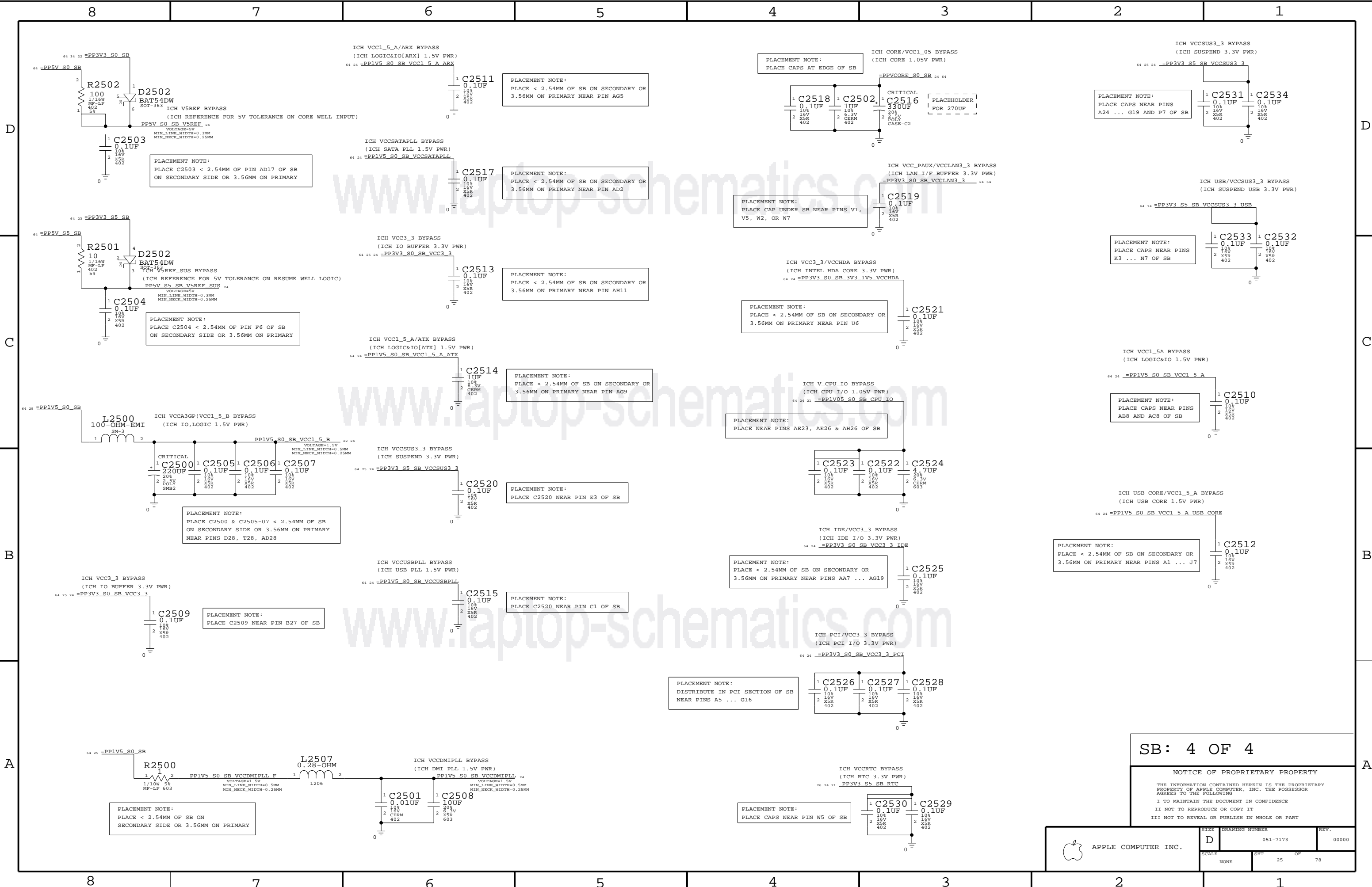
NOTE:  
VCCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V  
DEPENDING ON VIO OF AZALIA INTERFACE  
CODACC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

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SCALE	NONE	SHT	24 OF 78





SB: 4 OF 4

NOTICE OF PROPRIETARY PROPERTY

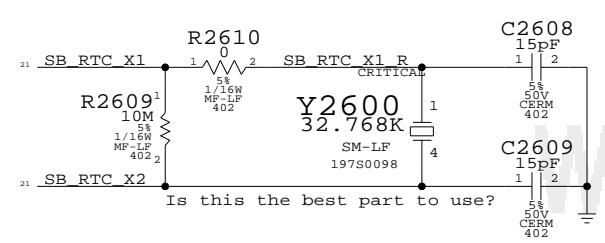
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	25	78	00000

### RTC Battery Connector



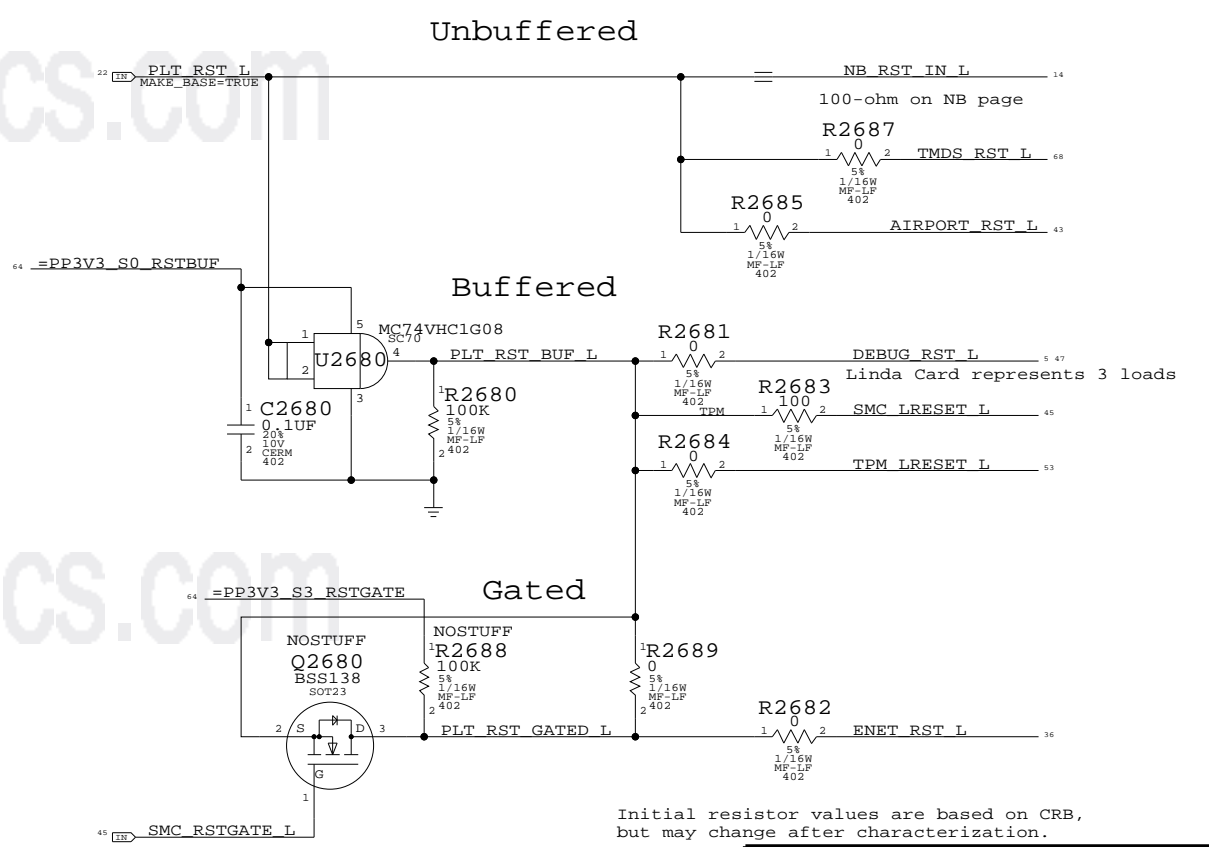
### SB RTC Crystal Circuit



This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

### Platform Reset Connections

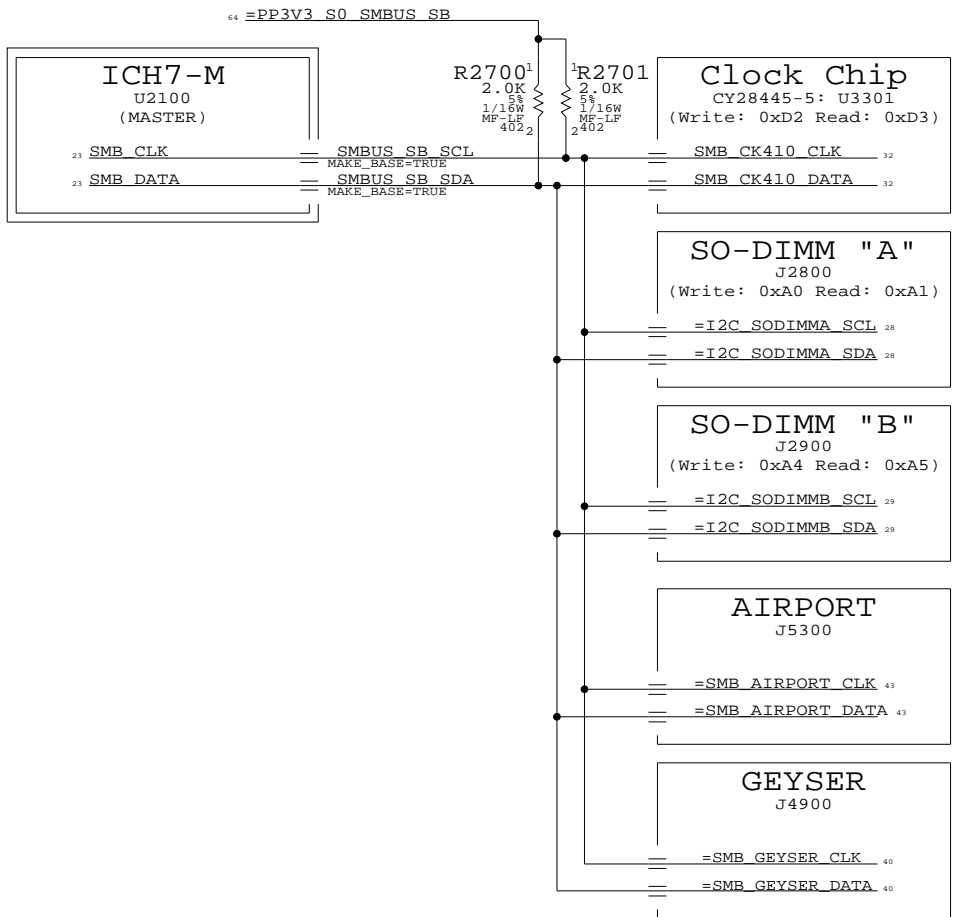


Initial resistor values are based on CRB, but may change after characterization.

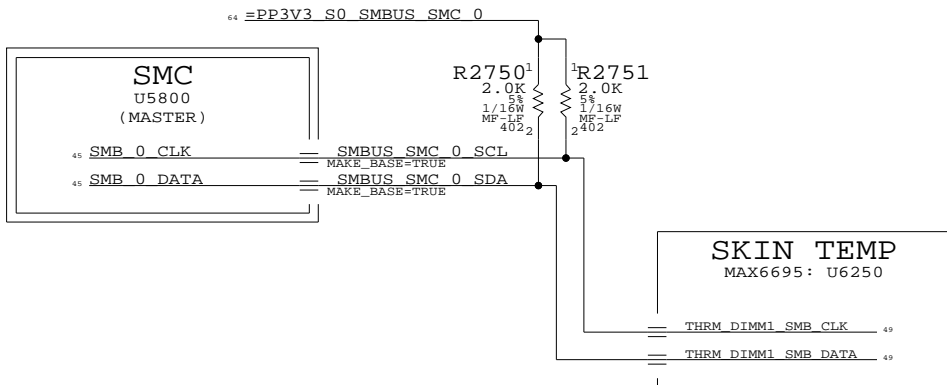
SB Misc		
SYNC_MASTER=NB	SYNC_DATE=07/26/2005	
NOTICE OF PROPRIETARY PROPERTY		
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	78
NONE	26		

### ICH7-M SMBus Connections

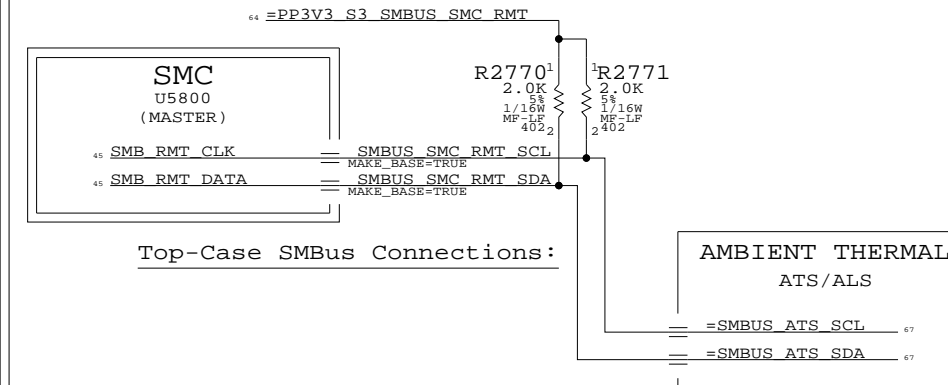


### SMC "0" SMBus Connections

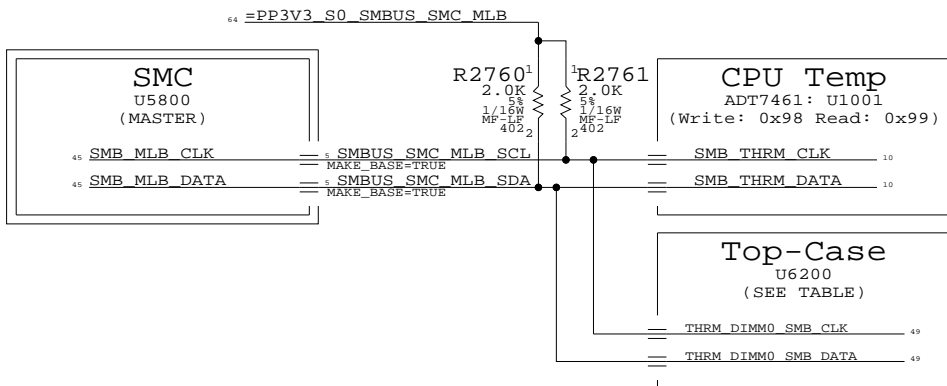


### SMC "RMT" SMBus Connections

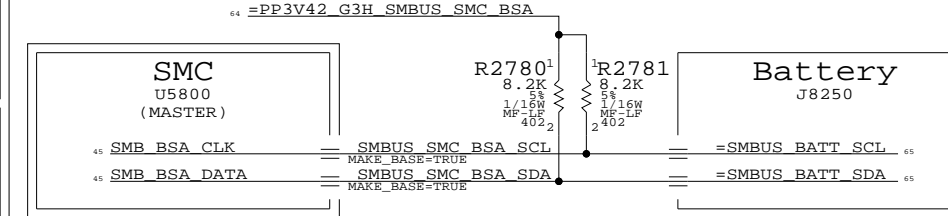
NOTE: SMC RMT bus remains powered and may be active in S3 state



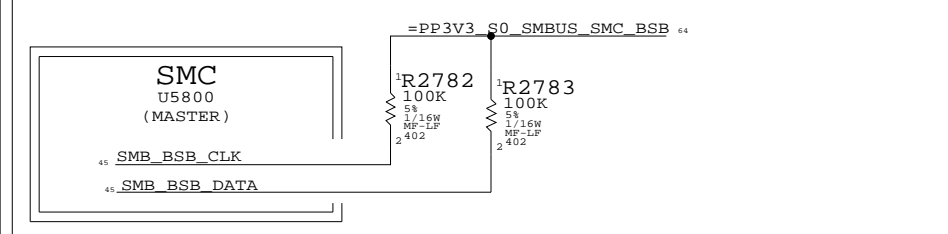
### SMC "MLB" SMBus Connections



### SMC "Battery A" SMBus Connections



### SMC "Battery B" SMBus Connections



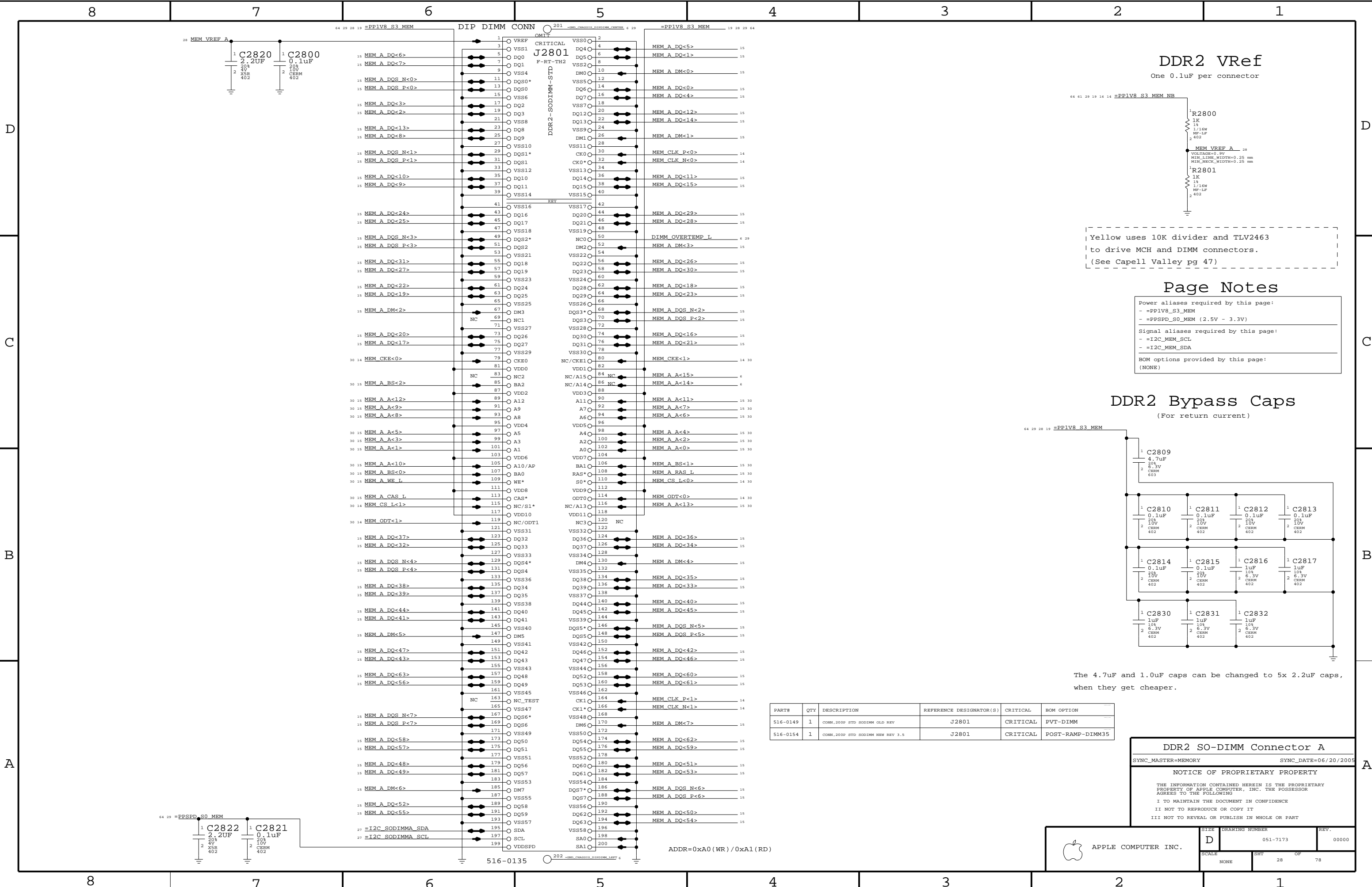
### M42 SMBUS CONNECTIONS

SYNC\_MASTER=ENET SYNC\_DATE=08/30/2005

#### NOTICE OF PROPRIETARY PROPERTY

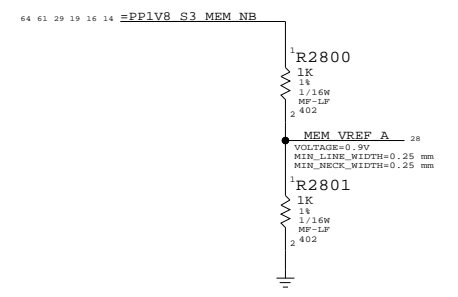
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	NONE	SHT	27 OF 78



### DDR2 VRef

One 0.1uF per connector

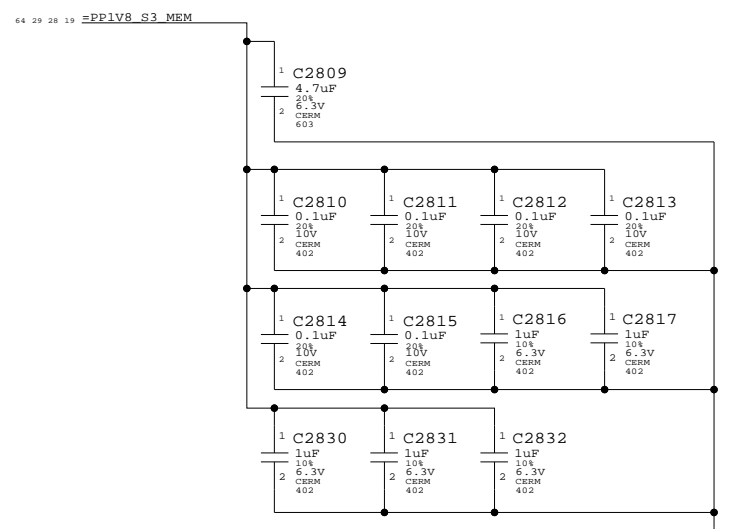


### Page Notes

- Power aliases required by this page:
  - =P1V8\_S3\_MEM
  - =PPSPD\_S0\_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
  - =I2C\_MEM\_SCL
  - =I2C\_MEM\_SDA
- BOM options provided by this page:
  - (NONE)

### DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN_200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN_200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

### DDR2 SO-DIMM Connector A

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

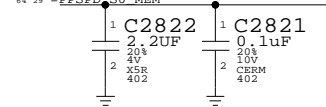
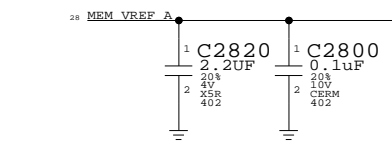
#### NOTICE OF PROPRIETARY PROPERTY

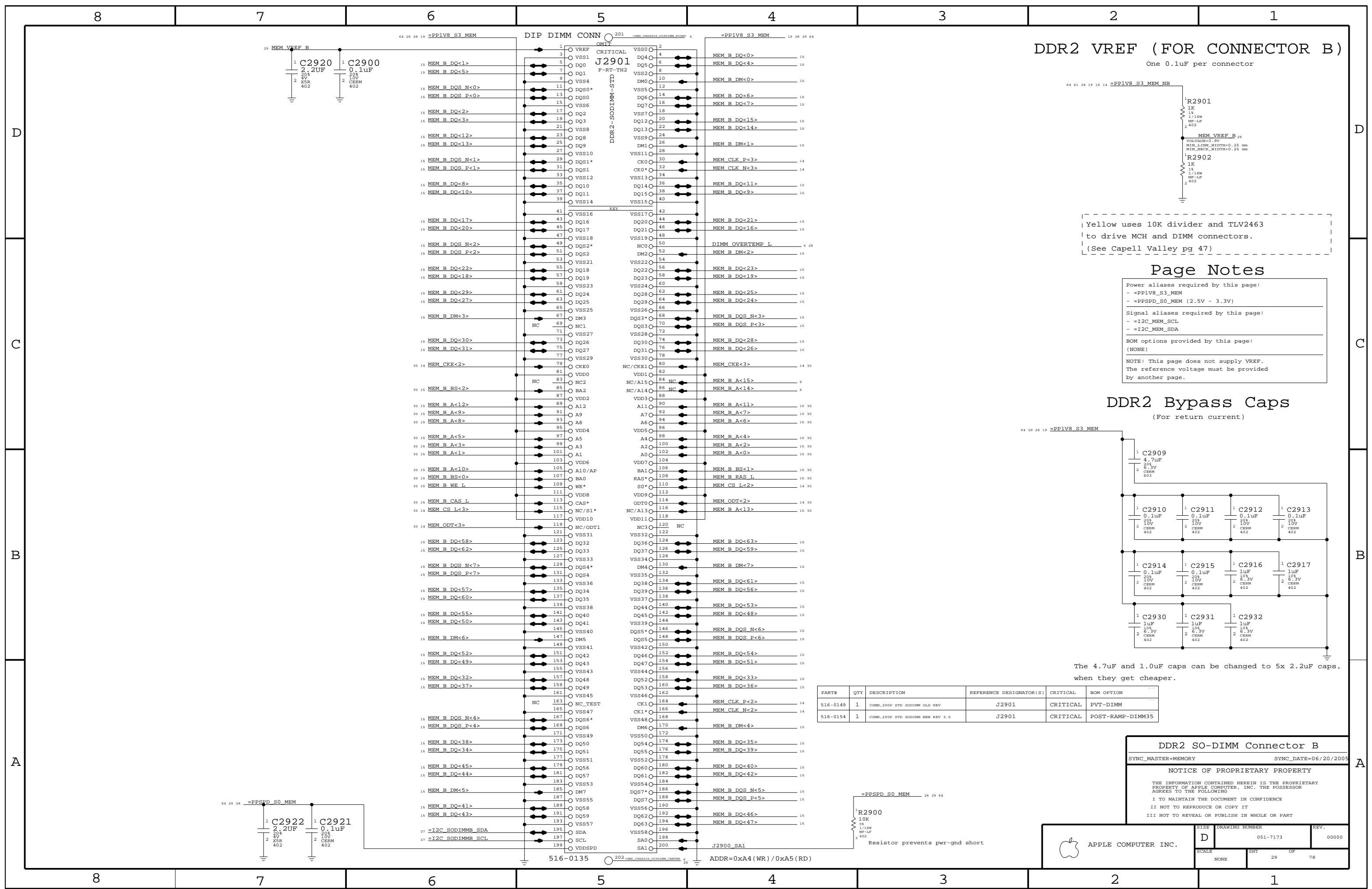
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SCALE	DRAWING NUMBER	REV.
NONE	D 051-7173	00000
SHT	28	OF
		78

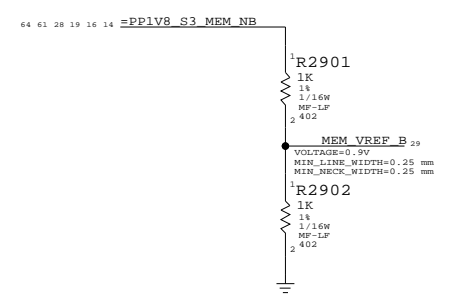
ADDR=0xA0 (WR) / 0xA1 (RD)





### DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector



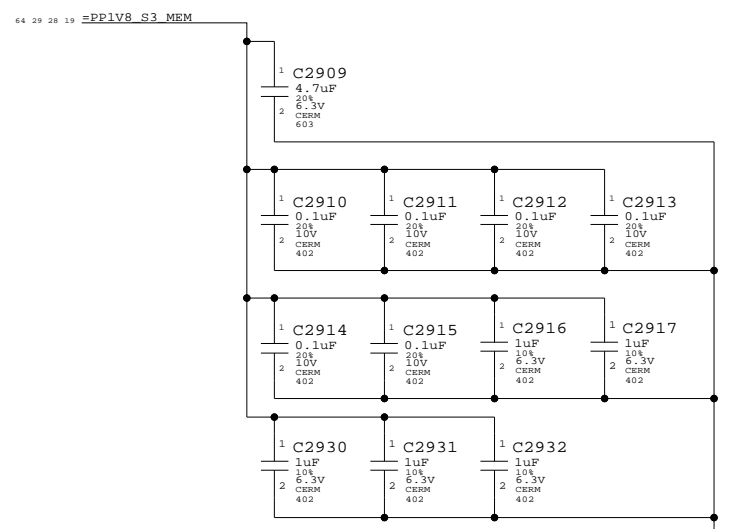
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

### Page Notes

- Power aliases required by this page:
    - =PP1V8\_S3\_MEM
    - =PPSPD\_S0\_MEM (2.5V - 3.3V)
  - Signal aliases required by this page:
    - =I2C\_MEM\_SCL
    - =I2C\_MEM\_SDA
  - BOM options provided by this page:
    - (NONE)
- NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

### DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 1.5	J2901	CRITICAL	POST-RAMP-DIMM35

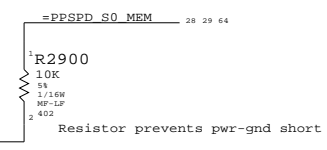
### DDR2 SO-DIMM Connector B

SYNC\_MASTER=MEMORY SYNC\_DATE=06/20/2005

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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	29	78	00000



516-0135 ADDR=0xA4 (WR) / 0xA5 (RD)



8

7

6

5

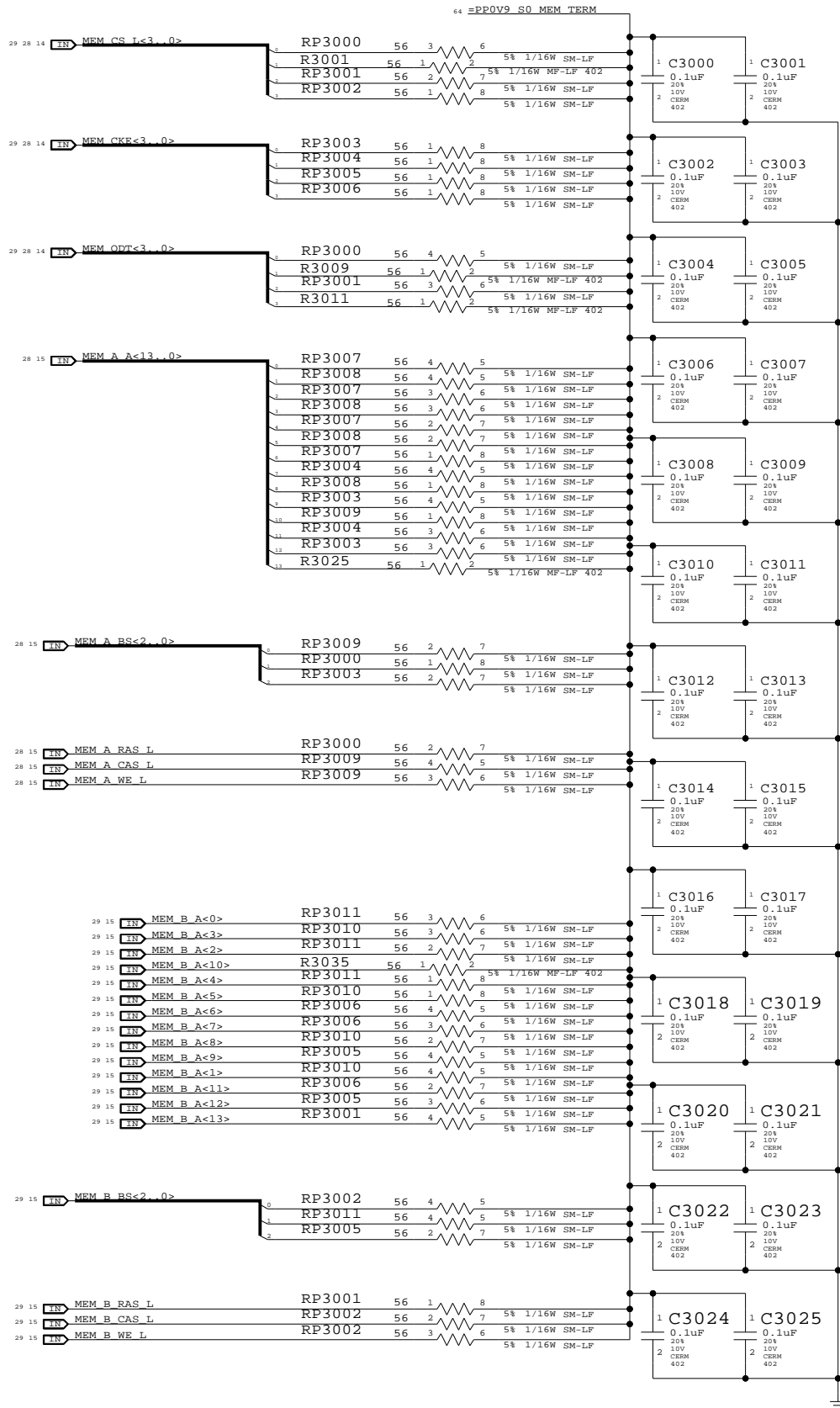
4

3

2

1

One cap for each side of every RPAK, one cap for every two discrete resistors  
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9\_S0\_MEM\_TERM

Memory Active Termination

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	30	78	

8

7

6

5

4

3

2

1

Page Notes

Power aliases required by this page:  
 - =PP5V\_S0\_MEMVTT  
 - =PP1V8\_S0\_MEMVTT  
 - =PP0V9\_S0\_MEMVTT\_LDO

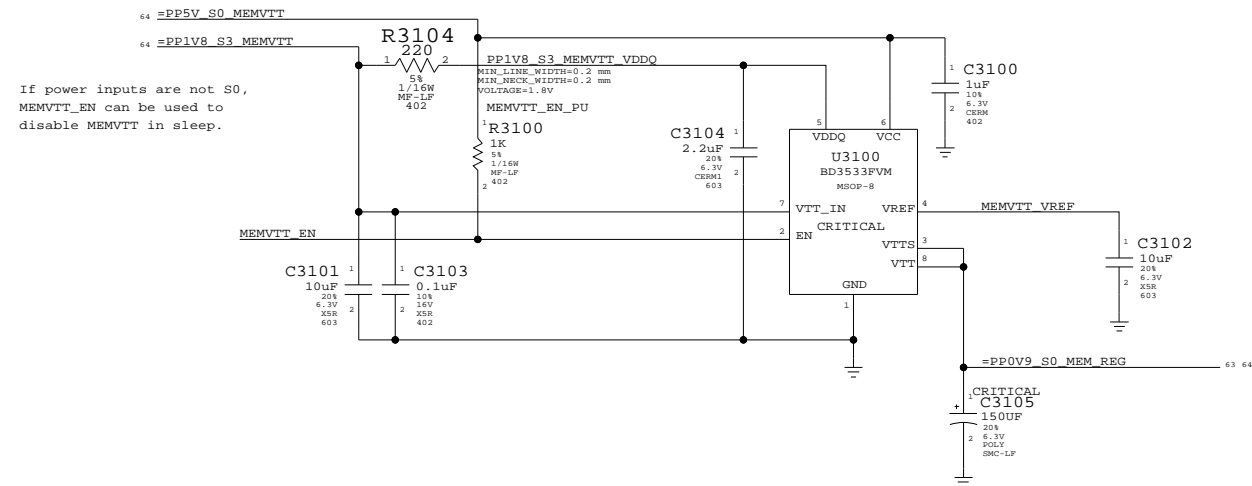
---

Signal aliases required by this page:  
 (NONE)

---

BOM options provided by this page:  
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

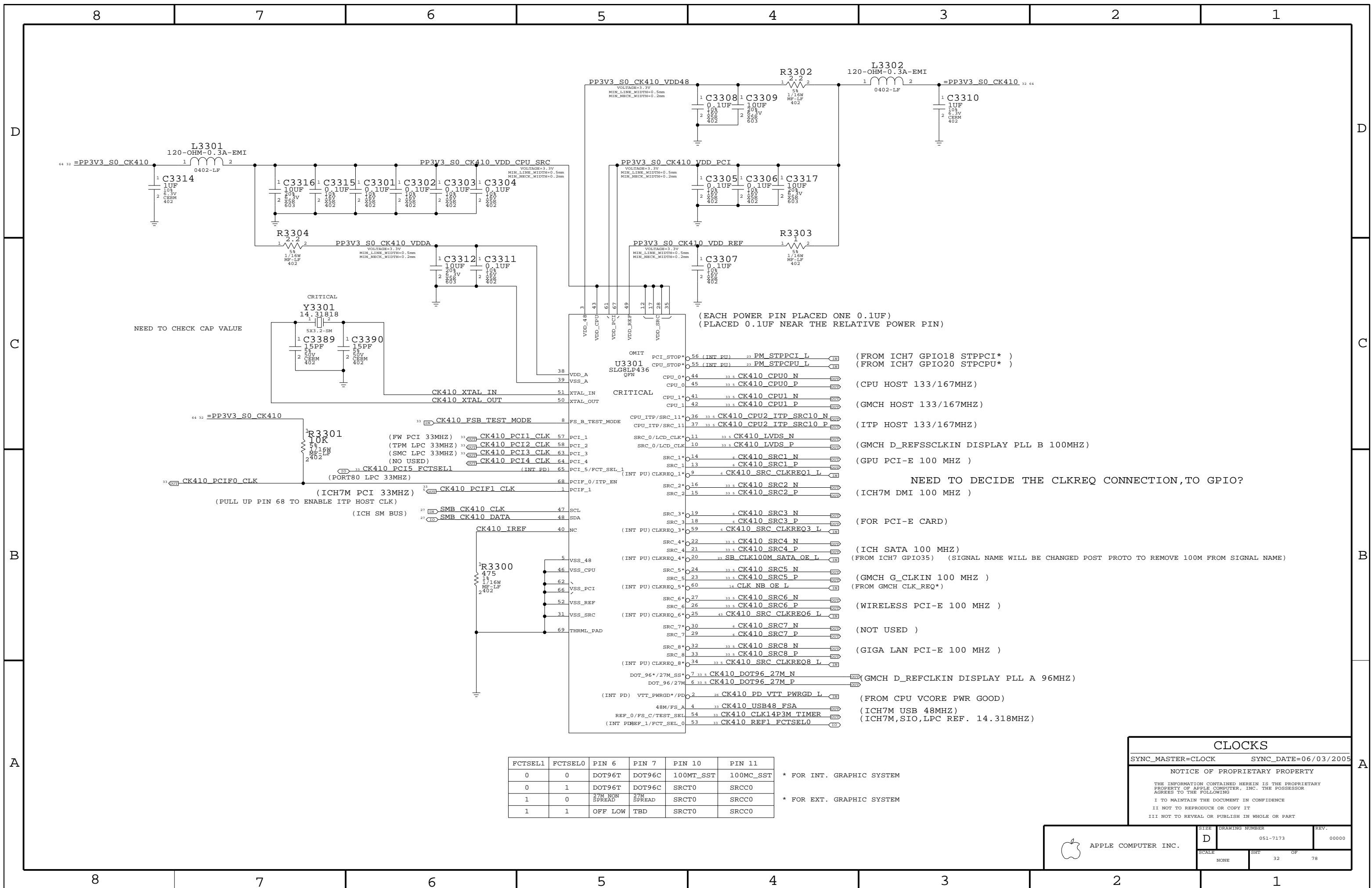
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	31	78	



NEED TO CHECK CAP VALUE

(EACH POWER PIN PLACED ONE 0.1UF)  
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

(FROM ICH7 GPIO18 STPPCI\* )  
(FROM ICH7 GPIO20 STPCPU\* )

(CPU HOST 133/167MHZ)

(GMCH HOST 133/167MHZ)

(ITP HOST 133/167MHZ)

(GMCH D\_REFSSCLKIN DISPLAY PLL B 100MHZ)

(GPU PCI-E 100 MHZ )

NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?  
(ICH7M DMI 100 MHZ )

(FOR PCI-E CARD)

(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)

(GMCH G\_CLKIN 100 MHZ )

(FROM GMCH CLK\_REQ\*)

(WIRELESS PCI-E 100 MHZ )

(NOT USED )

(GIGA LAN PCI-E 100 MHZ )

(GMCH D\_REFCLKIN DISPLAY PLL A 96MHZ)

(FROM CPU VCORE PWR GOOD)

(ICH7M USB 48MHZ)

(ICH7M,SIO,LPC REF. 14.318MHZ)

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

\* FOR INT. GRAPHIC SYSTEM

\* FOR EXT. GRAPHIC SYSTEM

**CLOCKS**

SYNC\_MASTER=CLOCK      SYNC\_DATE=06/03/2005

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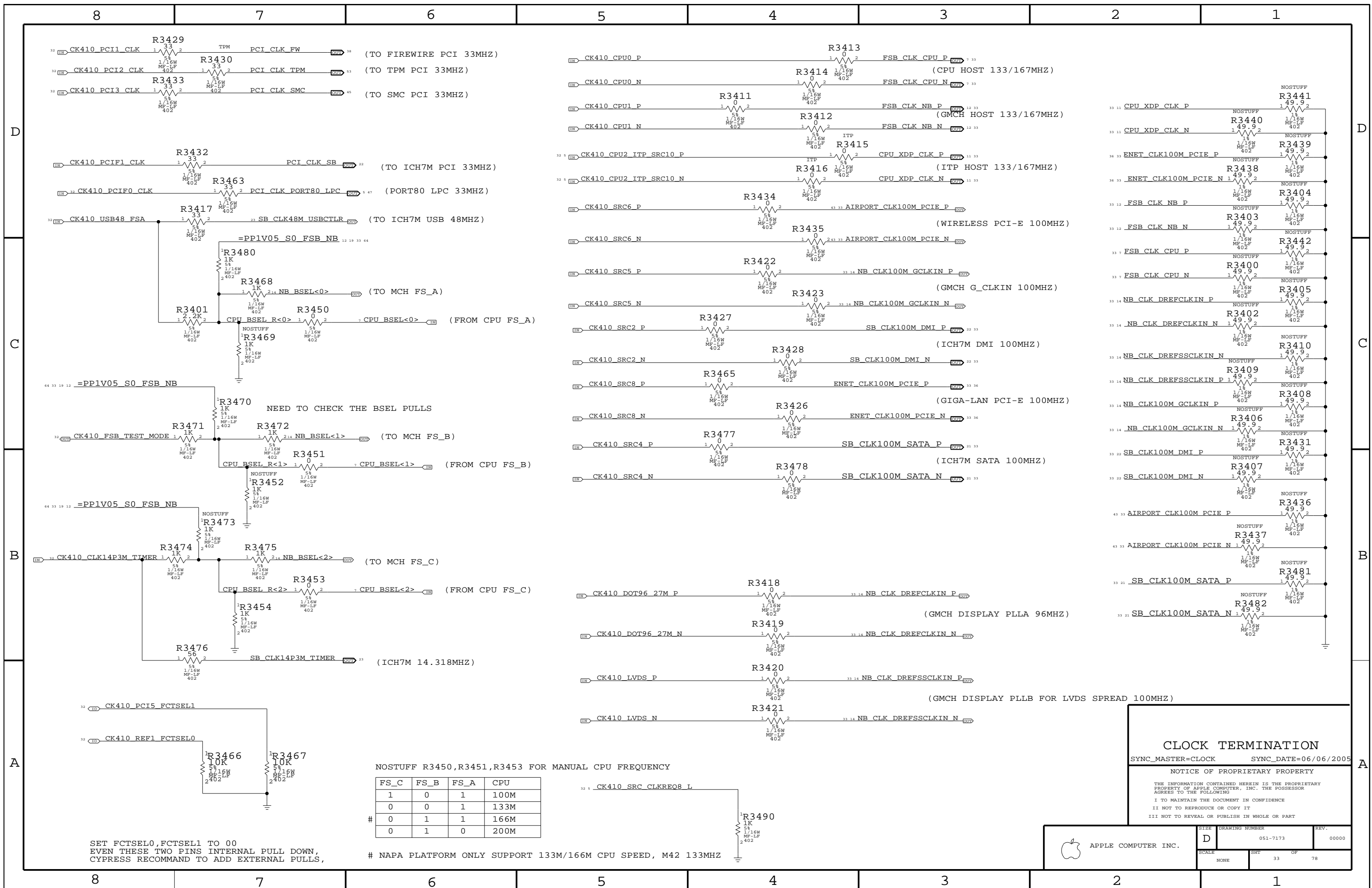
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	00000
SCALE	SHT	OF
NONE	32	78



NOSTUFF R3450, R3451, R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M

# NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ

SET FCTSEL0, FCTSEL1 TO 00  
EVEN THESE TWO PINS INTERNAL PULL DOWN,  
CYPRESS RECOMMEND TO ADD EXTERNAL PULLS,

**CLOCK TERMINATION**

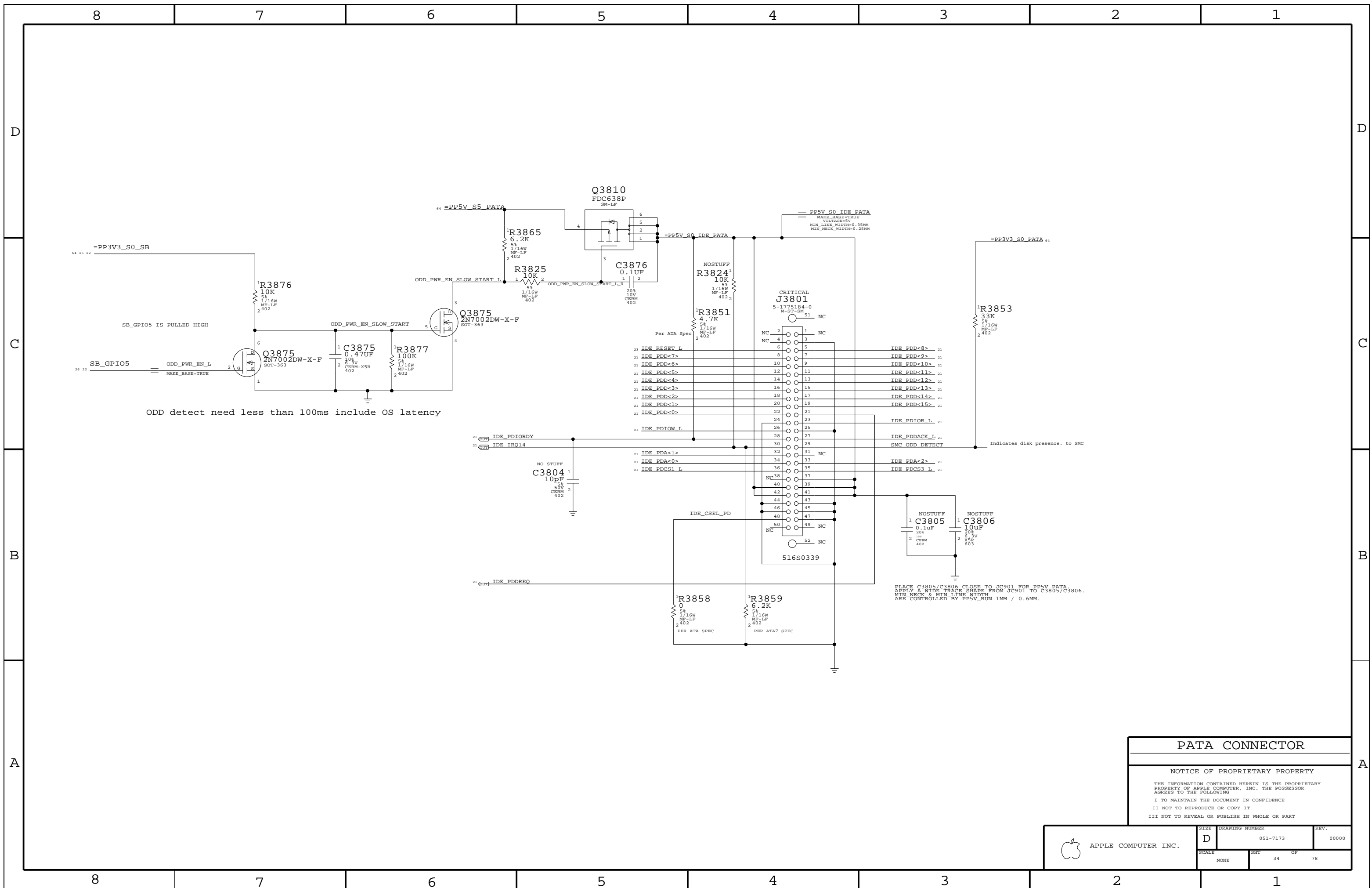
SYNC\_MASTER=CLOCK      SYNC\_DATE=06/06/2005

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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	33	78	00000



**PATA CONNECTOR**

---

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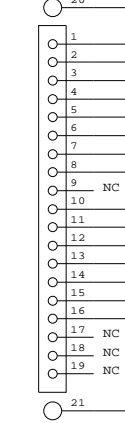
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 34	OF 78



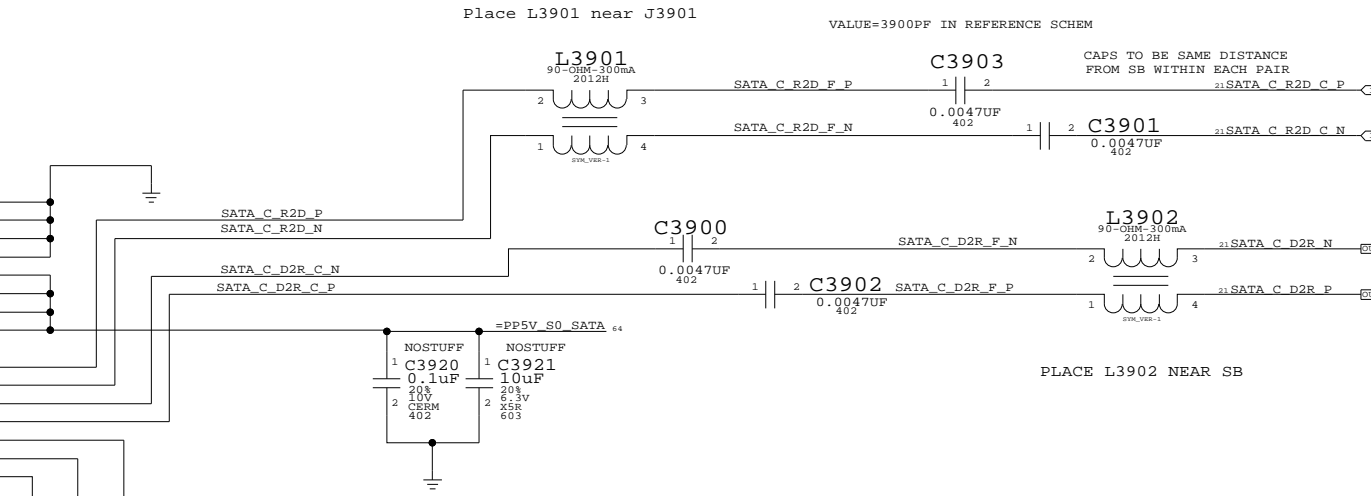
SATA CONNECTOR

518S0390

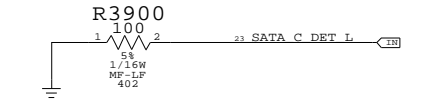
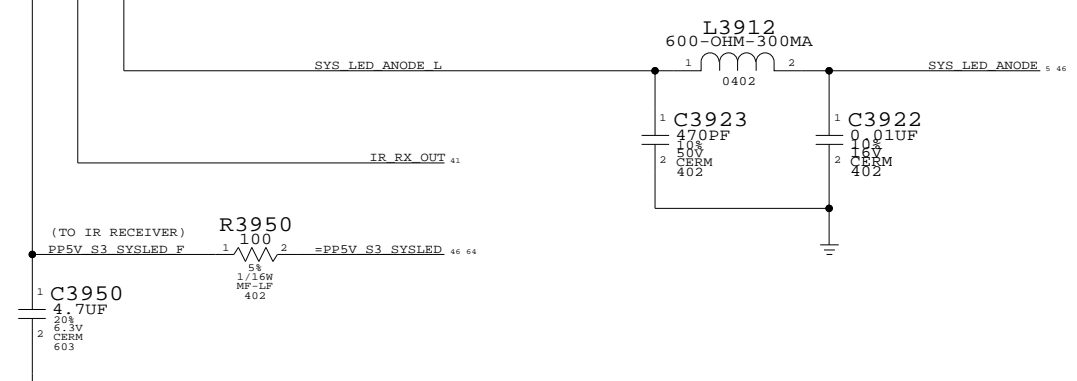
CRITICAL  
J3901  
20247-019E  
F-ST-2M  
20



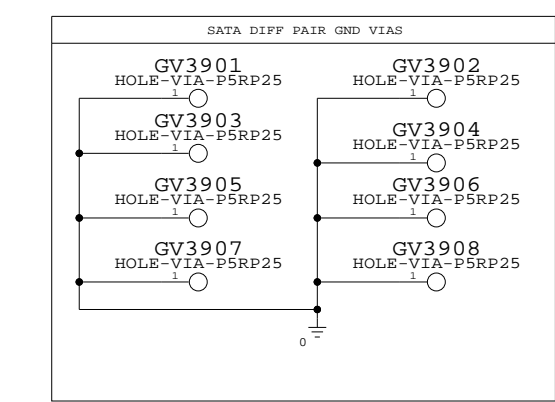
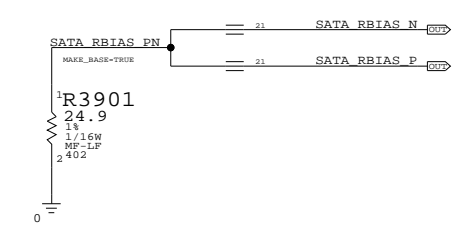
GND\_CHASSIS\_SATA



SYSTEM (SLEEP) LED FILTER



PLACE NEAR ICH7 PIN

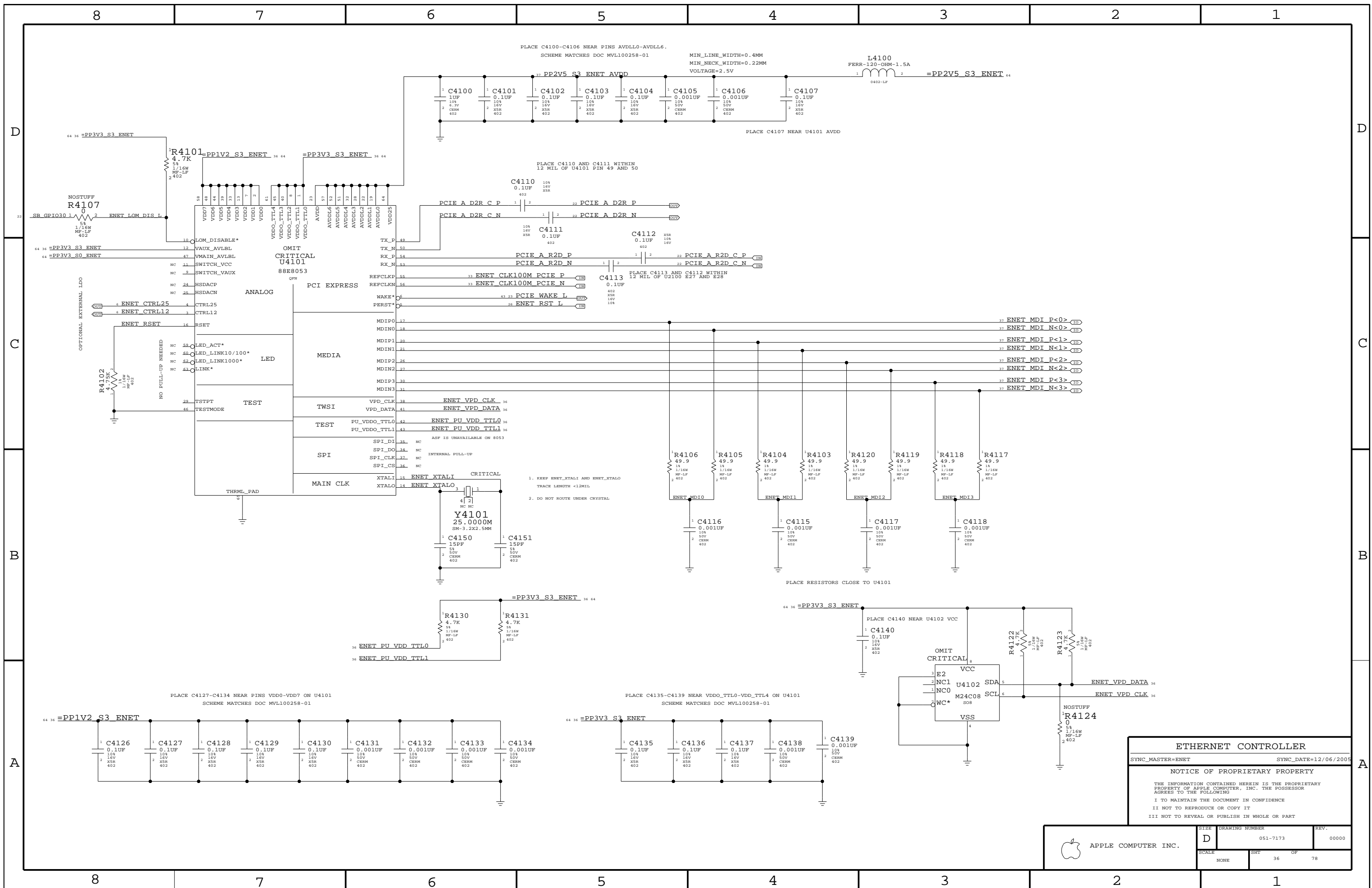


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901, L3902	KEEP MAG. LAYER IN BOM

SATA CONNECTOR

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	78
NONE		35	

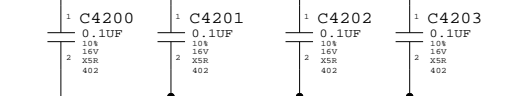


8 7 6 5 4 3 2 1

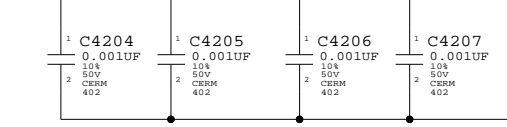
D  
C  
B  
A

L4250  
120-OHM-0.3A-EMI  
PP2V5\_S3\_ENET\_AVDD 1 0402-LF PP2V5\_S3\_ENET\_AVDD\_F

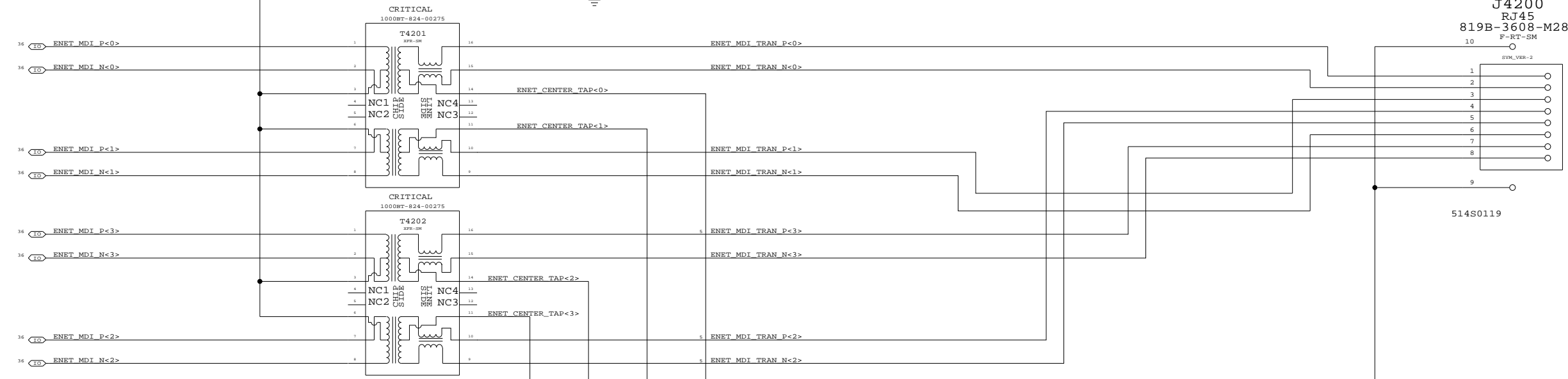
PLACE ONE CAP AT EACH PIN 3 AND 6 OF TRANSFORMERS



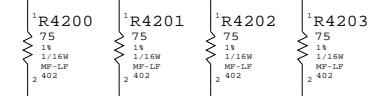
PLACE ONE CAP NEAR EACH PIN 3 AND 6 OF TRANSFORMERS



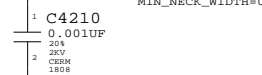
CROSS-OVERS ARE IN SCHEMATIC TO EASE ROUTING



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
157S0037	157S0011	?	T4201, T4202	SEE AND DELTA TRANSFORMER

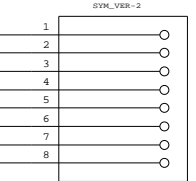


ENET\_BOB\_SMITH\_CAP  
MIN LINE WIDTH=0.6MM  
MIN NECK WIDTH=0.25MM



PLACE C4211 AND C4212 ON EACH SIDE OF J4200

OMIT CRITICAL  
J4200  
RJ45  
819B-3608-M280  
F-RT-SM



514S0119

ETHERNET CONNECTOR  
SYNC\_MASTER=ENET SYNC\_DATE=11/14/2005

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN, SP RJ-45 JACK, MIDDLEPLANE, M33, LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN, SP RJ-45 JACK, MIDDLEPLANE, BLACK, LF	J4200	CRITICAL	FANCY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7173	00000
SCALE	SHT	OF
NONE	37	78

8 7 6 5 4 3 2 1

PAGE NOTES

INPUT
=PP3V3\_S0\_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3\_S0\_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI\_GNT3\_L - PCI GRANT FROM SB
PCI\_CLK\_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI\_RST\_L - PCI RESET FROM SB
FW\_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI\_AD<0..31>, PCI\_C\_BE\_L<0..3>, PCI\_FRAME\_L, PCI\_IRDY\_L, PCI\_TRDY\_L,
PCI\_DEVSEL\_L, PCI\_STOP\_L, PCI\_PAR, PCI\_PERR\_L, PCI\_SERR\_L
FW\_A\_TPA\_P/N, FW\_A\_TPB\_P/N, FW\_A\_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW\_B\_TPA\_P/N, FW\_B\_TPB\_P/N, FW\_B\_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW\_C\_TPA\_P/N, FW\_C\_TPB\_P/N, FW\_C\_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

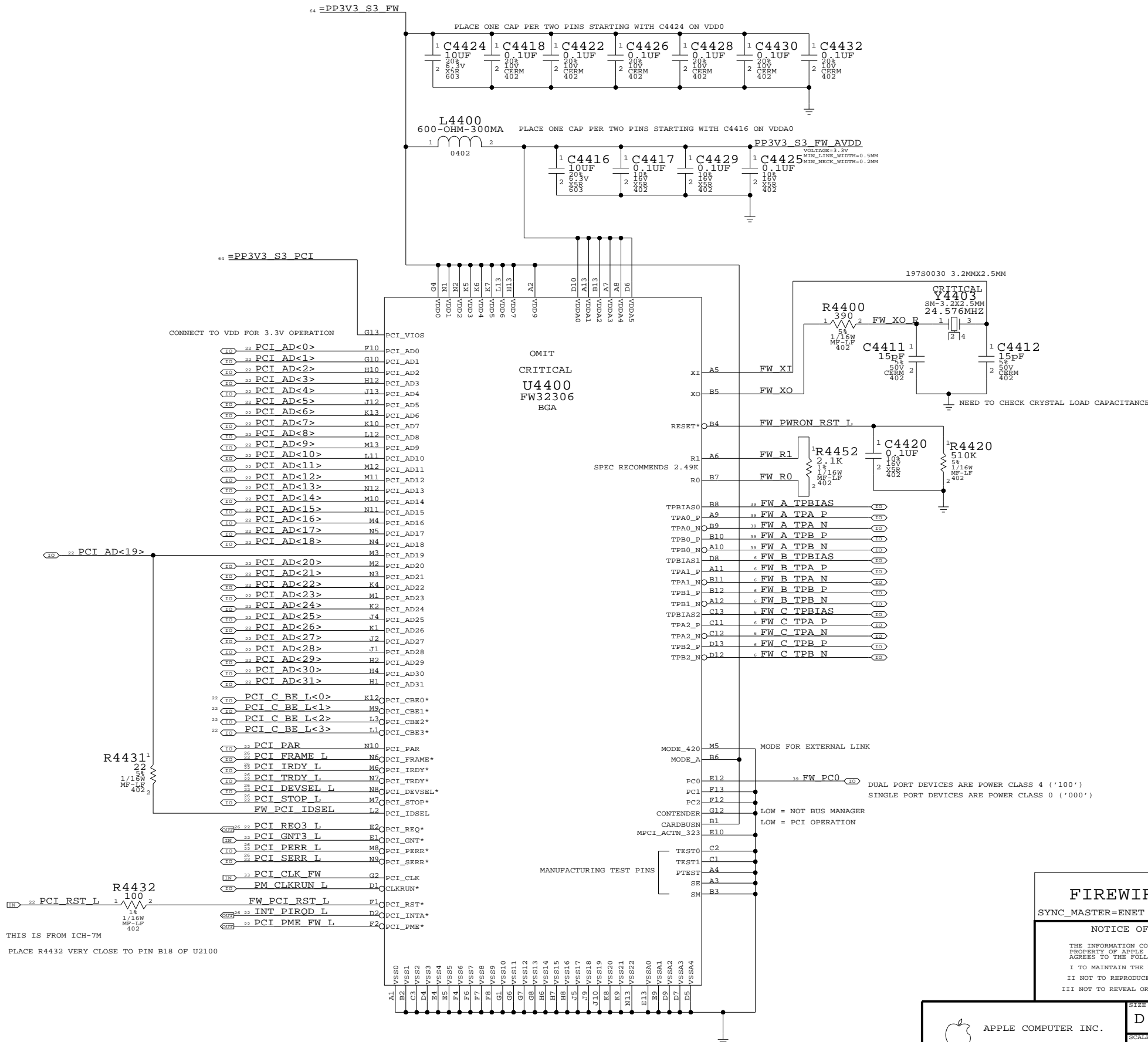
OUTPUT

PCI\_REQ3\_L - PCI REQUEST TO SB
PM\_CLKRUN\_L - CLOCK-RUN PCI PROTOCOL
INT\_PIRQD\_L - INTERRUPT TO SB
PCI\_PME\_FW\_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT\* TO INT\_PIRQD (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI\_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST\* AND REMOVED CONNECTION TO PLT\_RST\_L
6/22/2005 - CHANGED CLK\_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - CHANGED CLK\_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP



FIREWIRE CONTROLLER

SYNC\_MASTER=ENET SYNC\_DATE=08/30/2005

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Apple Computer Inc. logo and drawing information: DRAWING NUMBER 051-7173, REV. 00000, SCALE NONE, SHEET 38 OF 78.

Page Notes

INPUT:  
 =PPBUS\_S5\_FWPWRSW - PORT POWER  
 =PP3V3\_S5\_FW - DIGITAL POWER  
 =GND\_CHASSIS\_FW\_PORT0 - CHASSIS GROUND  
 =FWPWR\_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:  
 FW\_TPA0\_P/N,FW\_TPB0\_P/N,FW\_TPBIA50 - FIREWIRE DIFF PAIRS

OUTPUT:  
 FW\_PCO - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

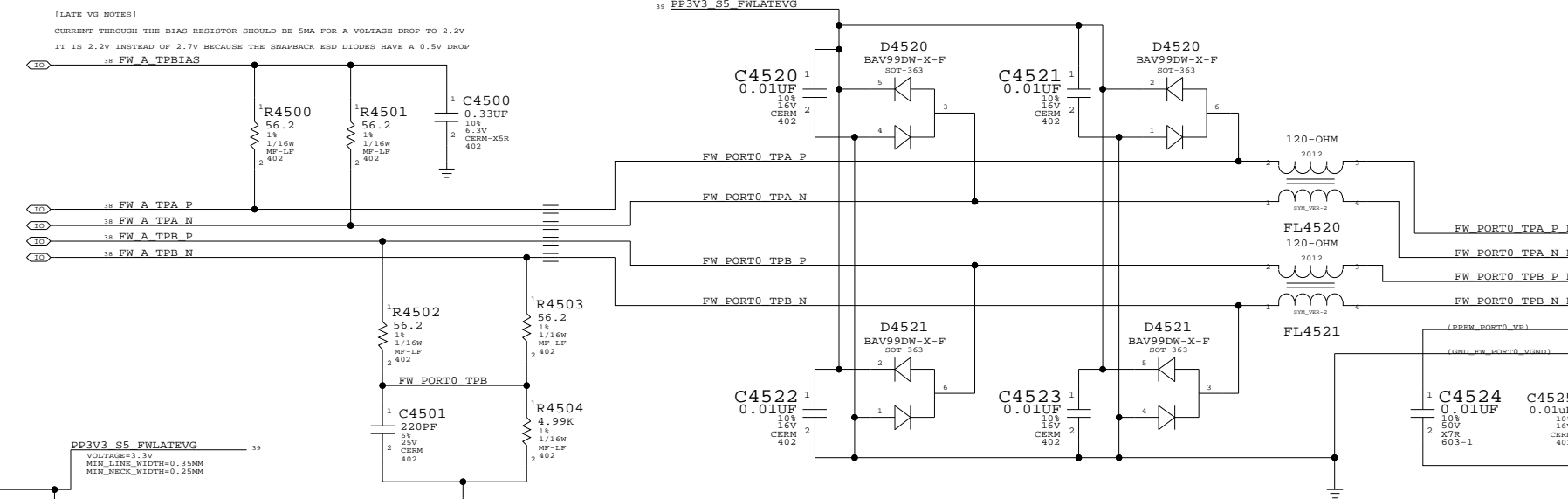
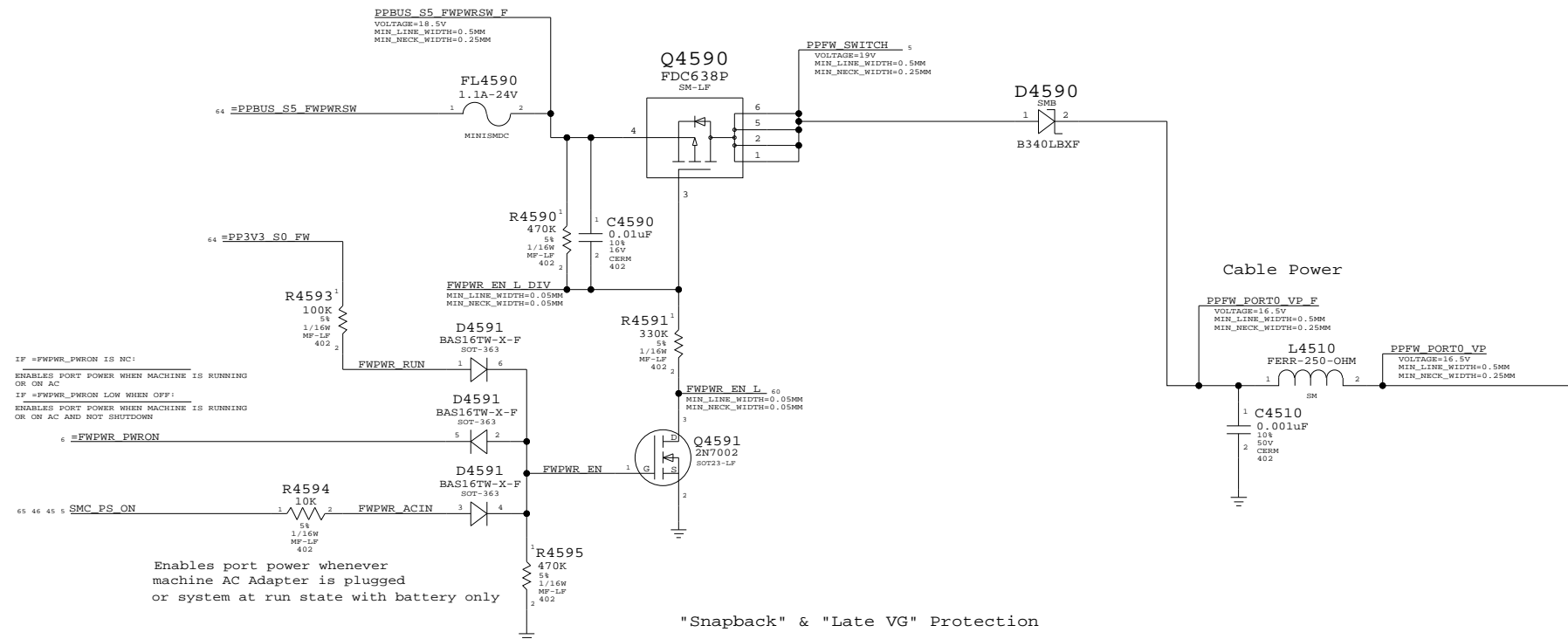
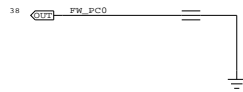
PAGE HISTORY

5/19/05 - INITIAL REVISION  
 6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE  
 6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER  
 6/22/05 - CONNECTED FW\_PCO FOR SINGLE PORT  
 7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1  
 7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0  
 7/26/05 - SWITCHED TO 514-0124 FOR FIREWIRE CONNECTOR  
 7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS  
 7/26/05 - CHANGED FL4590 TO 1.1A VERSION  
 7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT  
 7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

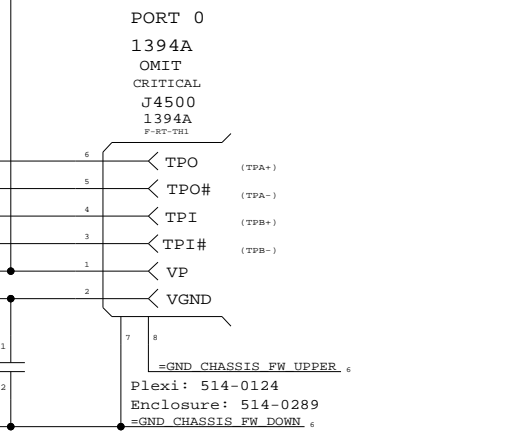
1394b implementation based on Apple  
 FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT  
 1 FOR DUAL PORT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN,6P 1394A RCPT,MIDPLANE,M33_LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK_LF	J4500	CRITICAL	FANCY



**FIREWIRE PORT**

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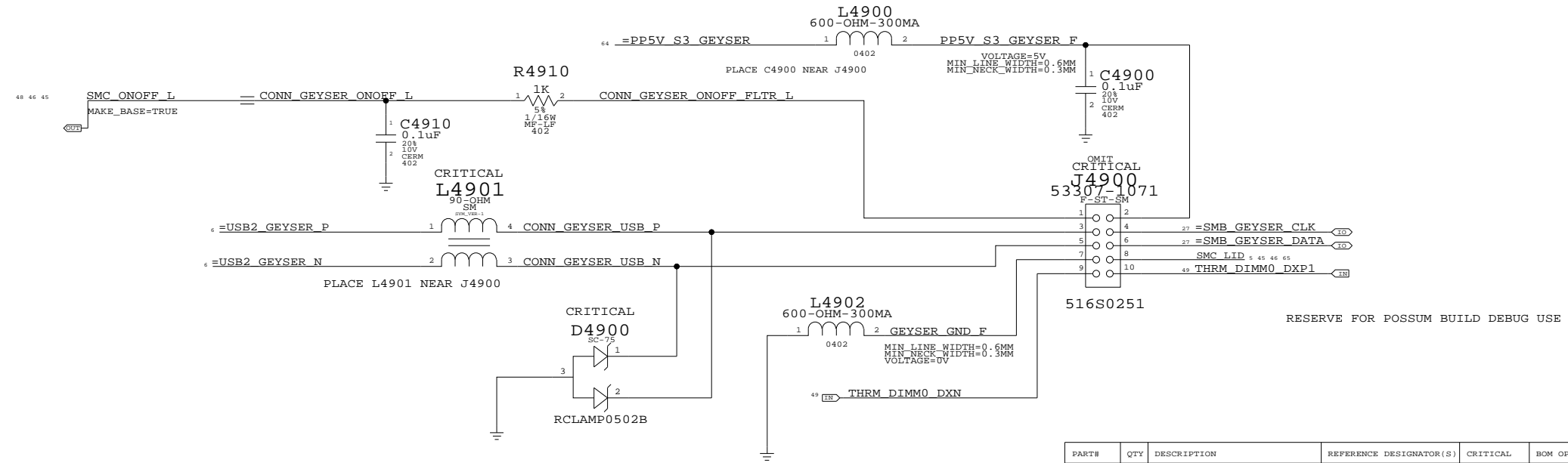
APPLE COMPUTER INC.

SIZE: DRAWING NUMBER: REV. 051-7173 00000

SCALE: NONE SHEET: 39 OF 78



# GEYSER AND DIMMO REMOTE TEMP SENSORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY

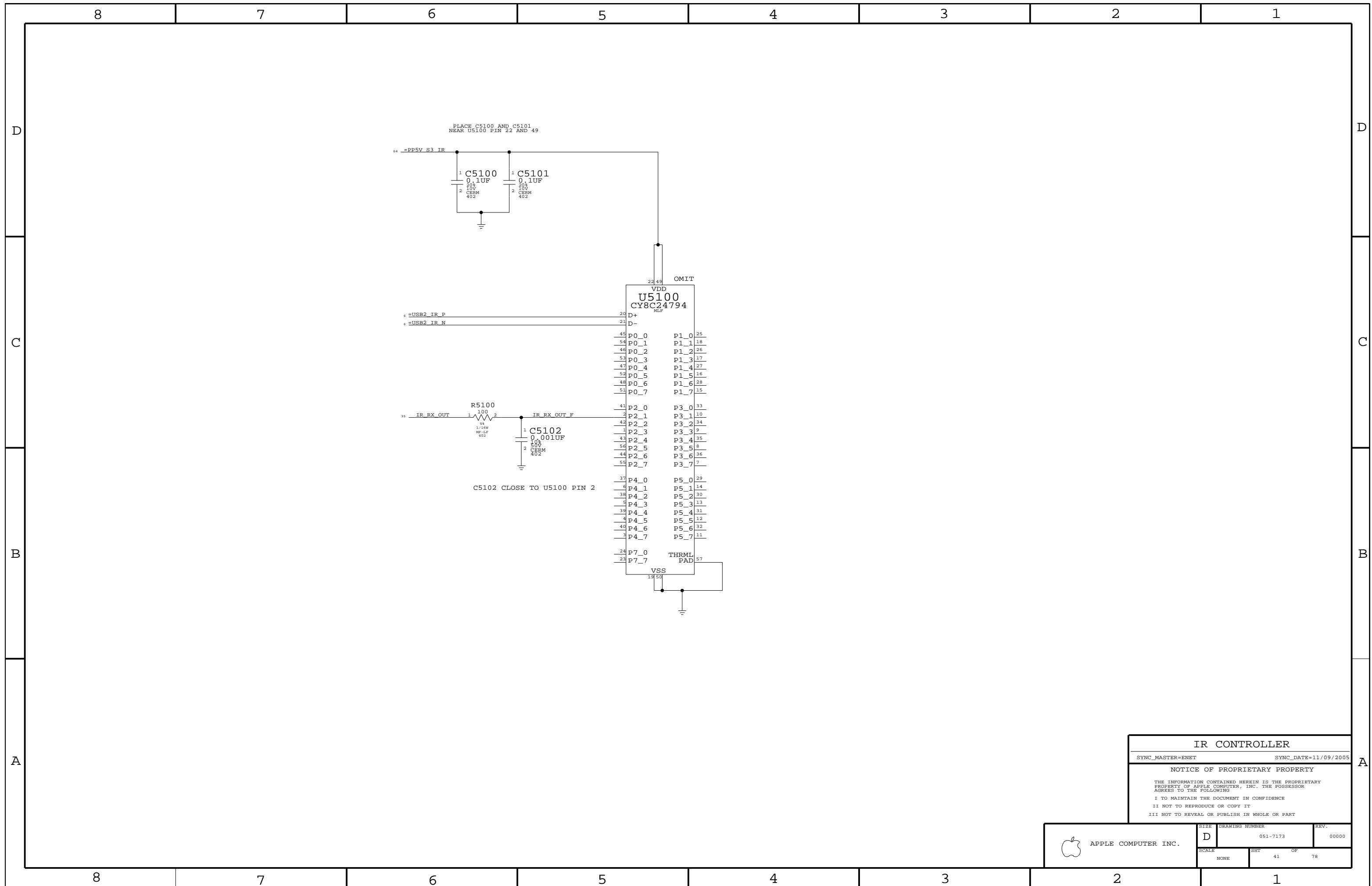
**CONNECTOR MISC**  
 SYNC\_MASTER=ENET      SYNC\_DATE=11/16/2005

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	SCALE: NONE	SHEET: 40	OF: 78



**IR CONTROLLER**

SYNC\_MASTER=ENET SYNC\_DATE=11/09/2005

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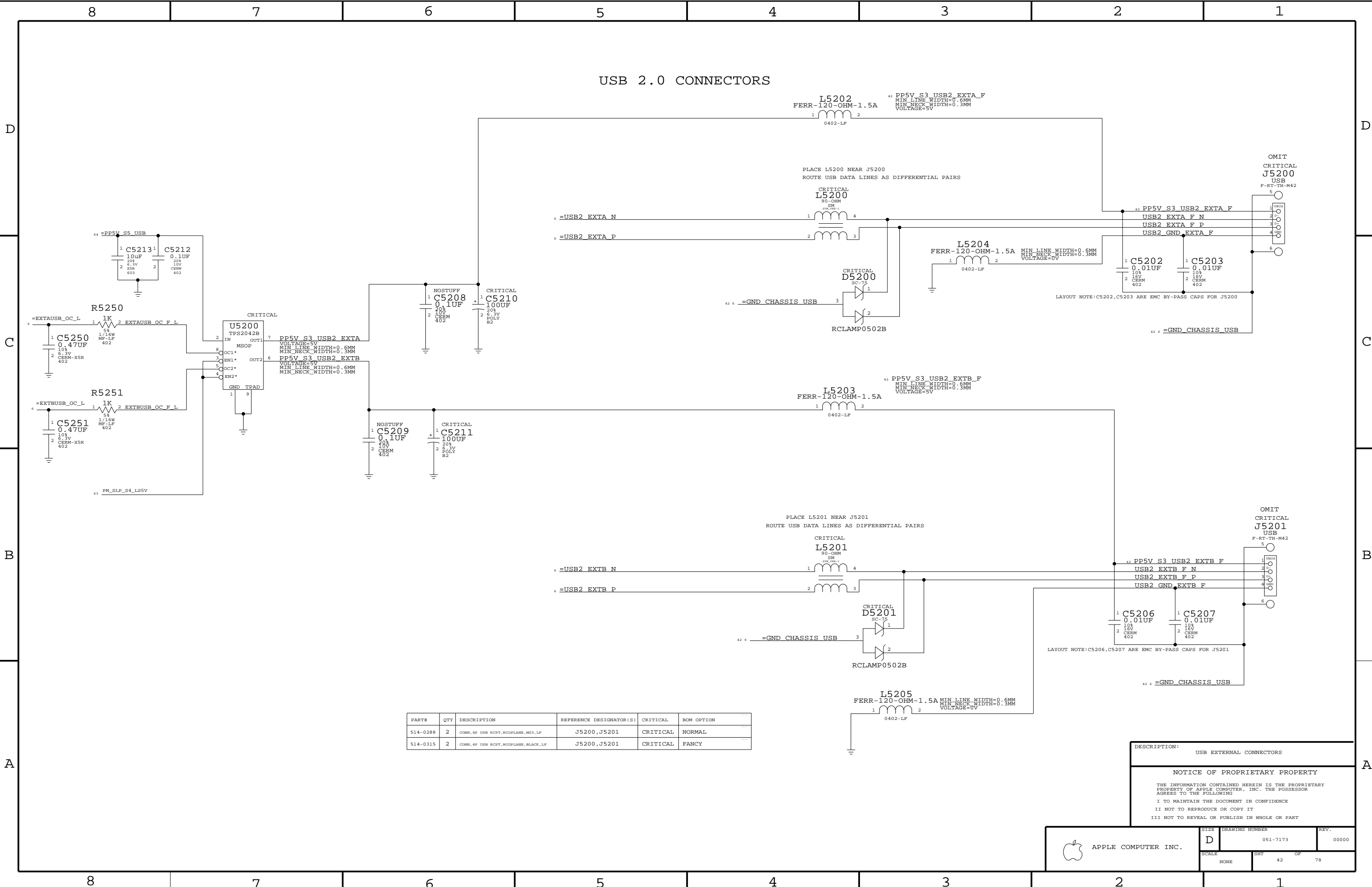
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 41	OF 78

# USB 2.0 CONNECTORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN, 4P USB RCPT, MIDPLANE, W3, LF	J5200, J5201	CRITICAL	NORMAL
514-0315	2	CONN, 4P USB RCPT, MIDPLANE, BLACK, LF	J5200, J5201	CRITICAL	FANCY

DESCRIPTION:  
USB EXTERNAL CONNECTORS

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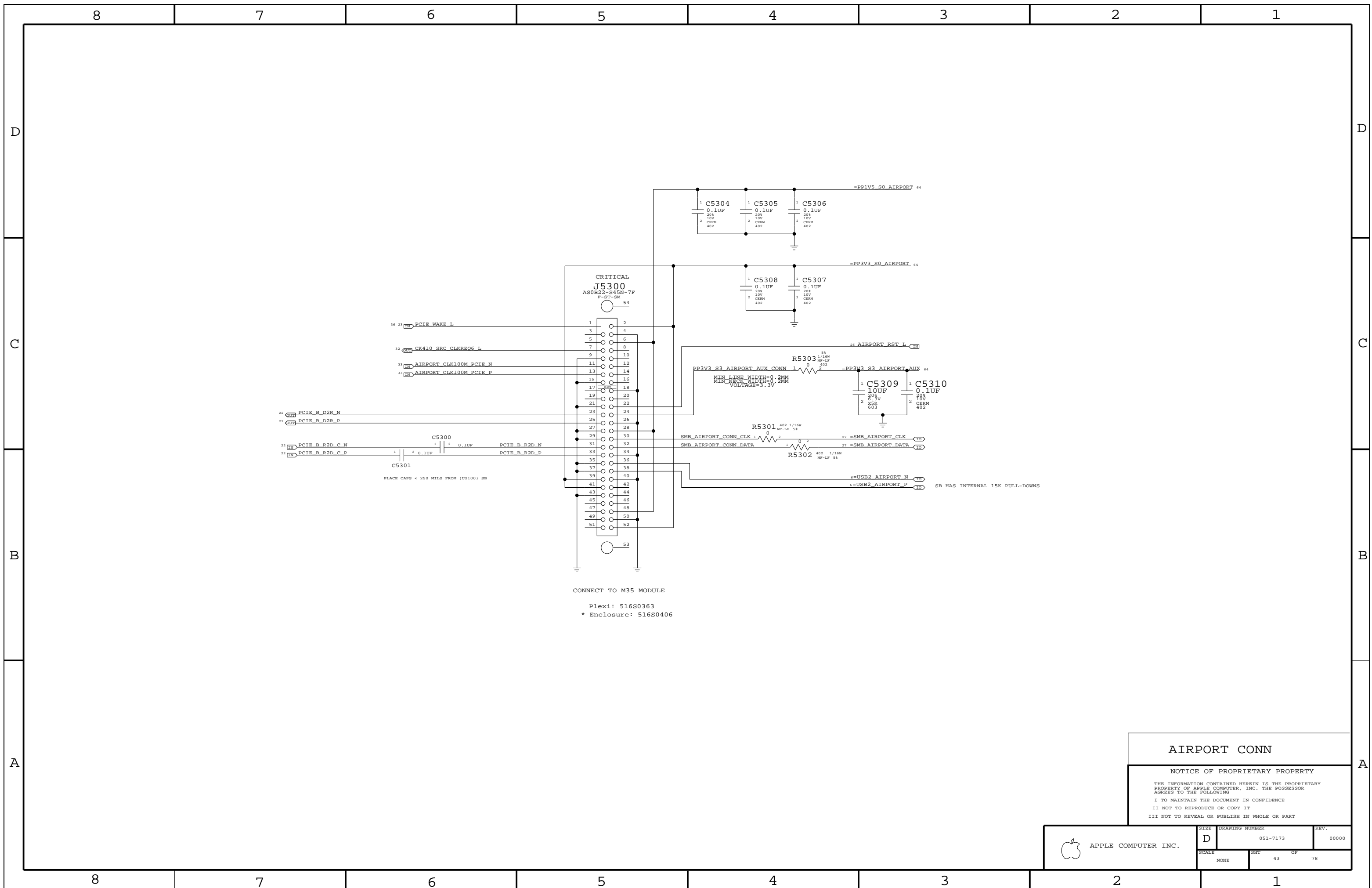
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APPLE COMPUTER INC.

SCALE	DRAWING NUMBER	REV.
NONE	D 051-7173	00000
SHT	42	OF 78




CONNECT TO M35 MODULE

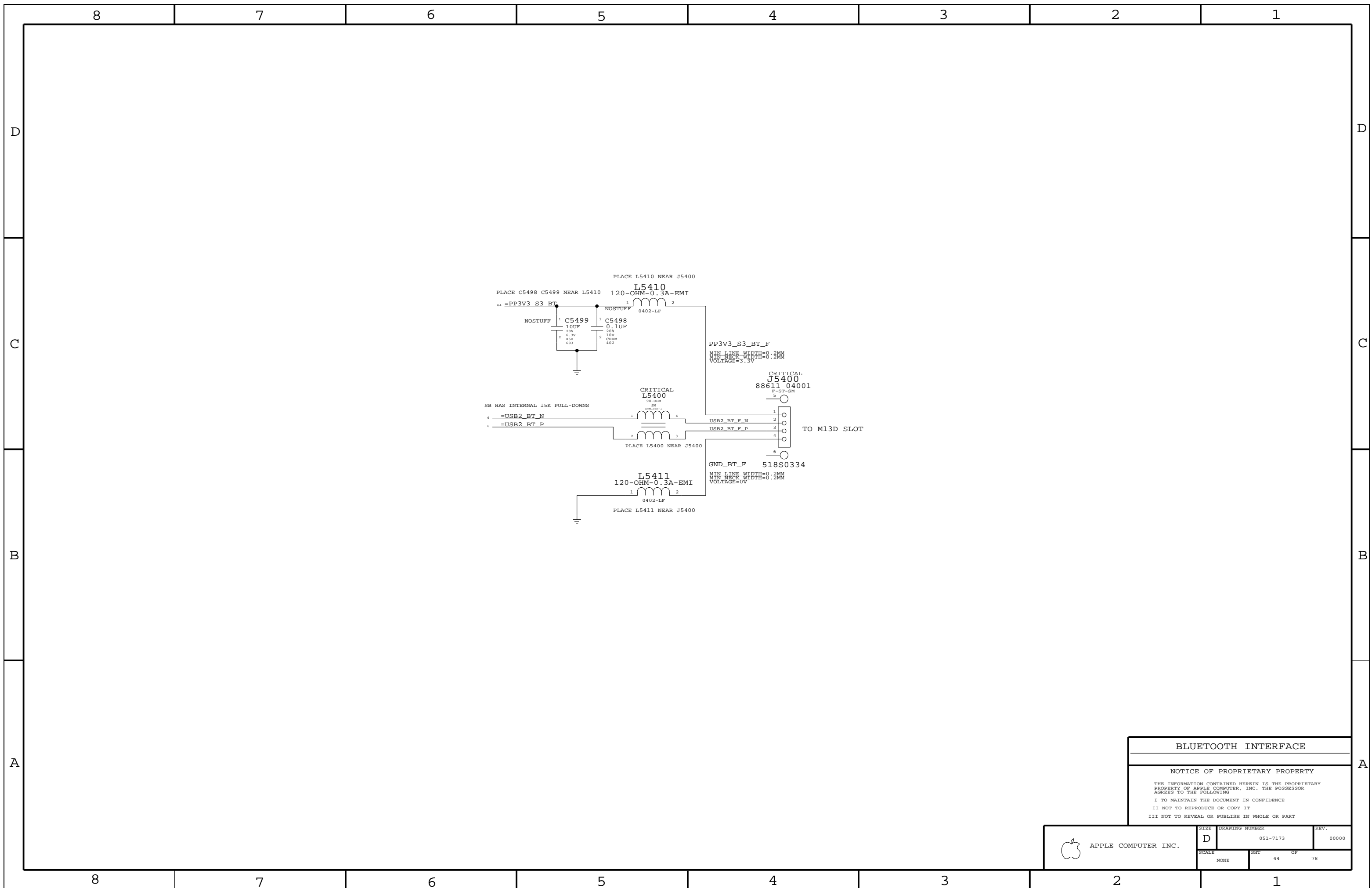
Plexi: 516S0363  
 \* Enclosure: 516S0406

### AIRPORT CONN

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	43	78	



**BLUETOOTH INTERFACE**

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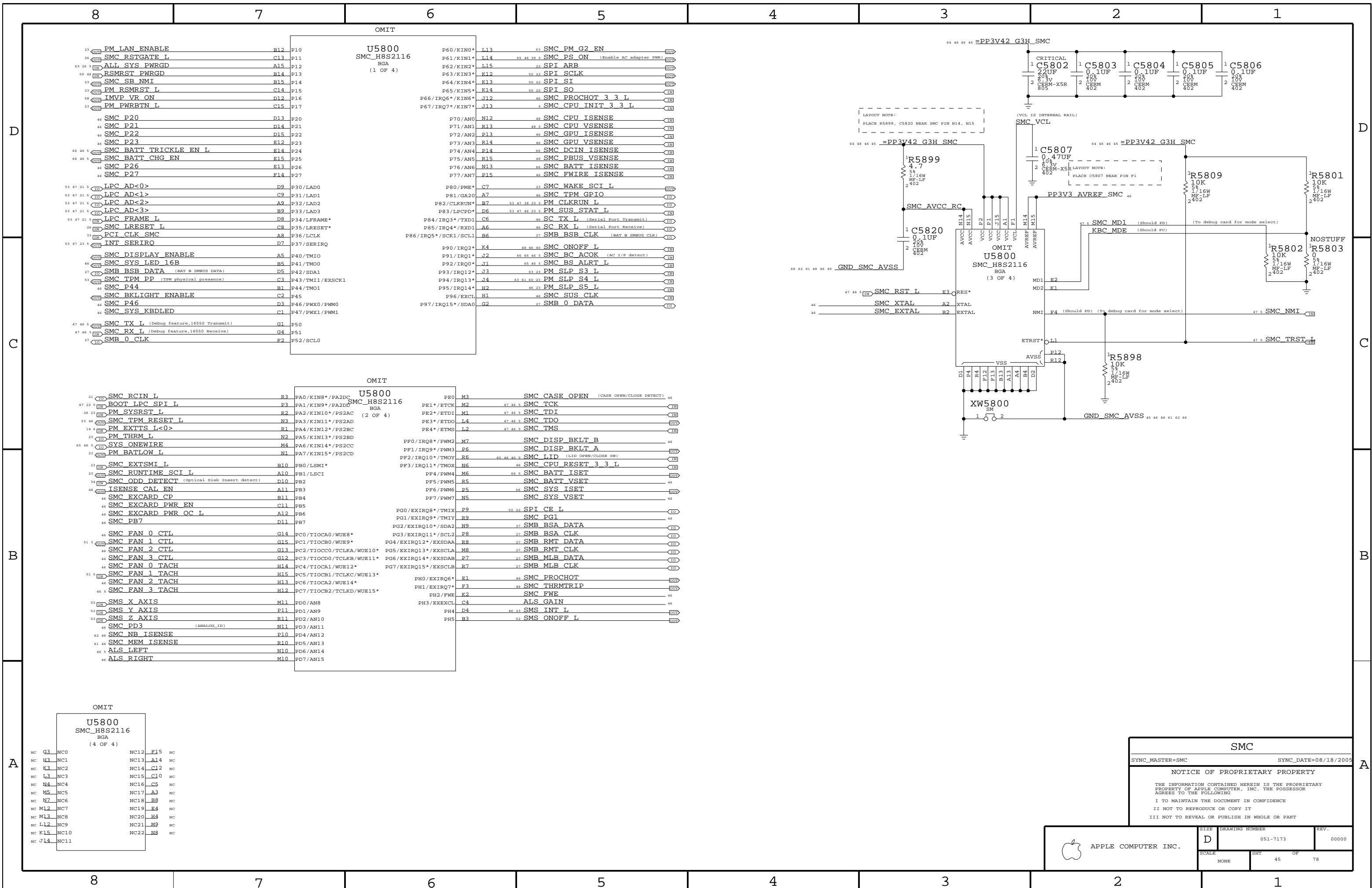
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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 44	OF 78





8 7 6 5 4 3 2 1

D

C

B

A

D

C

B

A

OMIT

**U5800 SMC\_H8S2116**  
BGA  
(1 OF 4)

P60/KIN0*	L13	61	SMC PM G2 EN	INT
P61/KIN1*	L14	65 46 39 5	SMC PS ON (Enable AC adapter PMR)	INT
P62/KIN2*	L15	23	SPI ARB	INT
P63/KIN3*	K12	50 22	SPI SCLK	INT
P64/KIN4*	K13	50 22	SPI SI	INT
P65/KIN5*	K14	50 22	SPI SO	INT
P66/IRQ6*/KIN6*	J12	46	SMC PROCHOT 3 3 L	INT
P67/IRQ7*/KIN7*	J13	4	SMC CPU INIT 3 3 L	INT
P70/AN0	N12	46	SMC CPU ISENSE	INT
P71/AN1	R13	46 5	SMC CPU VSENSE	INT
P72/AN2	P13	46	SMC GPU ISENSE	INT
P73/AN3	R14	46	SMC GPU VSENSE	INT
P74/AN4	P14	46	SMC DCIN ISENSE	INT
P75/AN5	R15	46	SMC PBUS VSENSE	INT
P76/AN6	N13	46	SMC BATT ISENSE	INT
P77/AN7	P15	46	SMC FWIRE ISENSE	INT
P80/PME*	C7	21	SMC WAKE SCI L	INT
P81/GA20	A7	46	SMC TPM GPIO	IO
P82/CLKRUN*	B7	53 47 38 23 5	PM CLKRUN L	IO
P83/LPCPD*	D6	53 47 46 23 5	PM SUS STAT L	IO
P84/IRQ3*/TXD1	C6	46	SC TX L (Serial Port Transmit)	IO
P85/IRQ4*/RXD1	A6	46	SC RX L (Serial Port Receive)	IO
P86/IRQ5*/SCK1/SCL1	B6	27	SMB BSB CLK (BAT B SMBUS CLK)	IO
P90/IRQ2*	K4	46 46 46	SMC ONOFF L	INT
P91/IRQ1*	J2	66 65 46 5	SMC BC ACOK (AC I/P detect)	INT
P92/IRQ0*	J1	65 46 5	SMC BS ALRT L	INT
P93/IRQ12*	J3	63 21	PM SLP S3 L	INT
P94/IRQ13*	J4	63 61 50 21	PM SLP S4 L	INT
P95/IRQ14*	H2	46 21	PM SLP S5 L	INT
P96/EXCL	H1	46	SMC SUS CLK	INT
P97/IRQ15*/SDA0	G2	27	SMB 0 DATA	IO

OMIT

**U5800 SMC\_H8S2116**  
BGA  
(2 OF 4)

PE0	M3	46	SMC CASE OPEN (CASE OPEN/CLOSE DETECT)	INT
PE1*/ETCK	M2	47 46 5	SMC TCK	INT
PE2*/ETDI	M1	47 46 5	SMC TDI	INT
PE3*/ETDO	L4	47 46 5	SMC TDO	INT
PE4*/ETMS	L2	47 46 5	SMC TMS	INT
PF0/IRQ8*/PWM2	M7	46	SMC DISP BKLT B	INT
PF1/IRQ9*/PWM3	P6	46	SMC DISP BKLT A	INT
PF2/IRQ10*/TMOY	R6	65 46 40 5	SMC LID (LID OPEN/CLOSE SW)	INT
PF3/IRQ11*/TMOX	N6	46	SMC CPU RESET 3 3 L	INT
PF4/PWM4	M6	66 5	SMC BATT ISET	INT
PF5/PWM5	R5	46	SMC BATT VSET	INT
PF6/PWM6	P5	46	SMC SYS ISET	INT
PF7/PWM7	N5	46	SMC SYS VSET	INT
PG0/EXIRQ8*/TMIX	P9	50 22	SPI CE L	INT
PG1/EXIRQ9*/TMIX	R9	46	SMC PG1	INT
PG2/EXIRQ10*/SDA2	N9	27	SMB BSA DATA	IO
PG3/EXIRQ11*/SCL2	P8	27	SMB BSA CLK	IO
PG4/EXIRQ12*/EXSDAA	RR	27	SMB RMT DATA	IO
PG5/EXIRQ13*/EXSCLA	M8	27	SMB RMT CLK	IO
PG6/EXIRQ14*/EXSDAB	P7	27	SMB MLB DATA	IO
PG7/EXIRQ15*/EXSCLB	R7	27	SMB MLB CLK	IO
PH0/EXIRQ6*	E1	46	SMC PROCHOT	INT
PH1/EXIRQ7*	F3	46	SMC THRMTRIP	INT
PH2/FWE	K2	46	SMC FWE	INT
PH3/EXEXCL	C4	46	ALS GAIN	INT
PH4	D4	46 23	SMS INT L	INT
PH5	B3	62	SMS ONOFF L	INT

OMIT

**U5800 SMC\_H8S2116**  
BGA  
(4 OF 4)

NC3	NC0	NC12	E15	NC
NC4	NC1	NC13	A14	NC
NC5	NC2	NC14	C12	NC
NC6	NC3	NC15	C10	NC
NC7	NC4	NC16	C5	NC
NC8	NC5	NC17	A3	NC
NC9	NC6	NC18	B8	NC
NC10	NC7	NC19	E4	NC
NC11	NC8	NC20	H4	NC
NC12	NC9	NC21	M9	NC
NC13	NC10	NC22	N8	NC
NC14	NC11			

**U5800 SMC\_H8S2116**  
BGA  
(4 OF 4)

NC3	NC0	NC12	E15	NC
NC4	NC1	NC13	A14	NC
NC5	NC2	NC14	C12	NC
NC6	NC3	NC15	C10	NC
NC7	NC4	NC16	C5	NC
NC8	NC5	NC17	A3	NC
NC9	NC6	NC18	B8	NC
NC10	NC7	NC19	E4	NC
NC11	NC8	NC20	H4	NC
NC12	NC9	NC21	M9	NC
NC13	NC10	NC22	N8	NC
NC14	NC11			

**SMC**  
SYNC\_MASTER=SMC SYNC\_DATE=08/18/2005

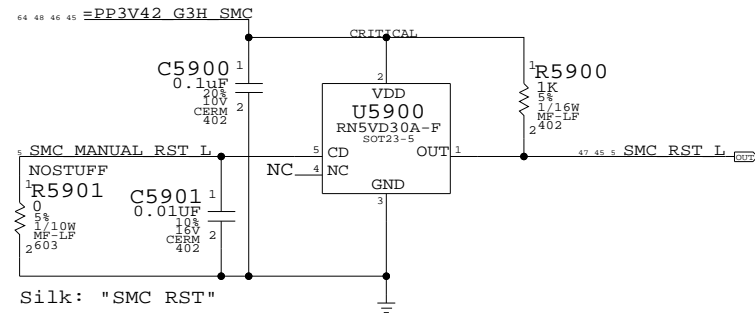
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SCALE	D	DRAWING NUMBER	051-7173	REV.	00000
SHEET	NONE	OF	45	OF	78

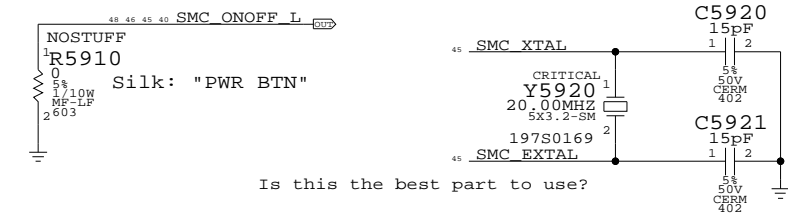
APPLE COMPUTER INC.

8 7 6 5 4 3 2 1

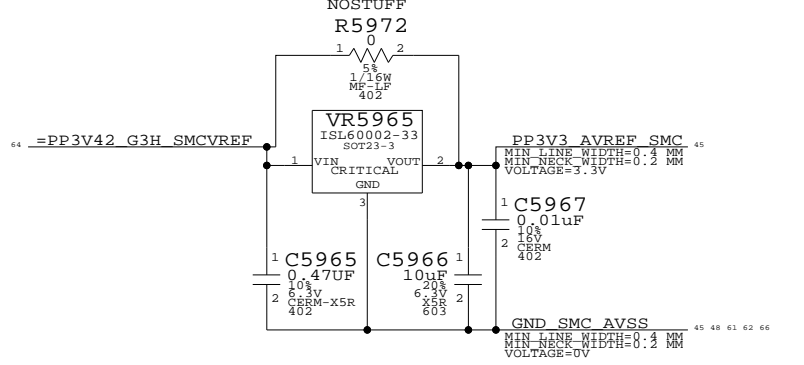
SMC Reset Button / Brownout Detect



Debug Power Button SMC Crystal Circuit

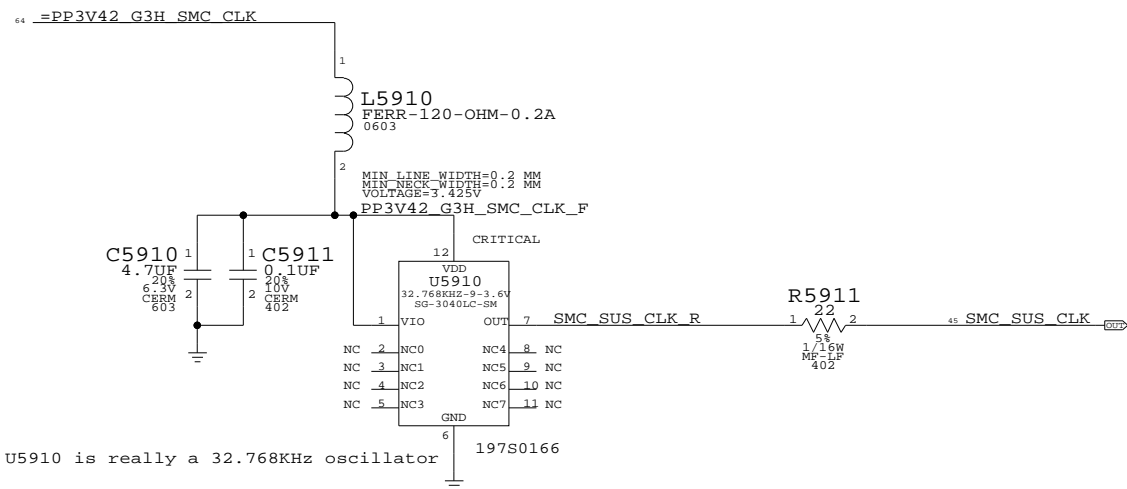


SMC AVREF Supply



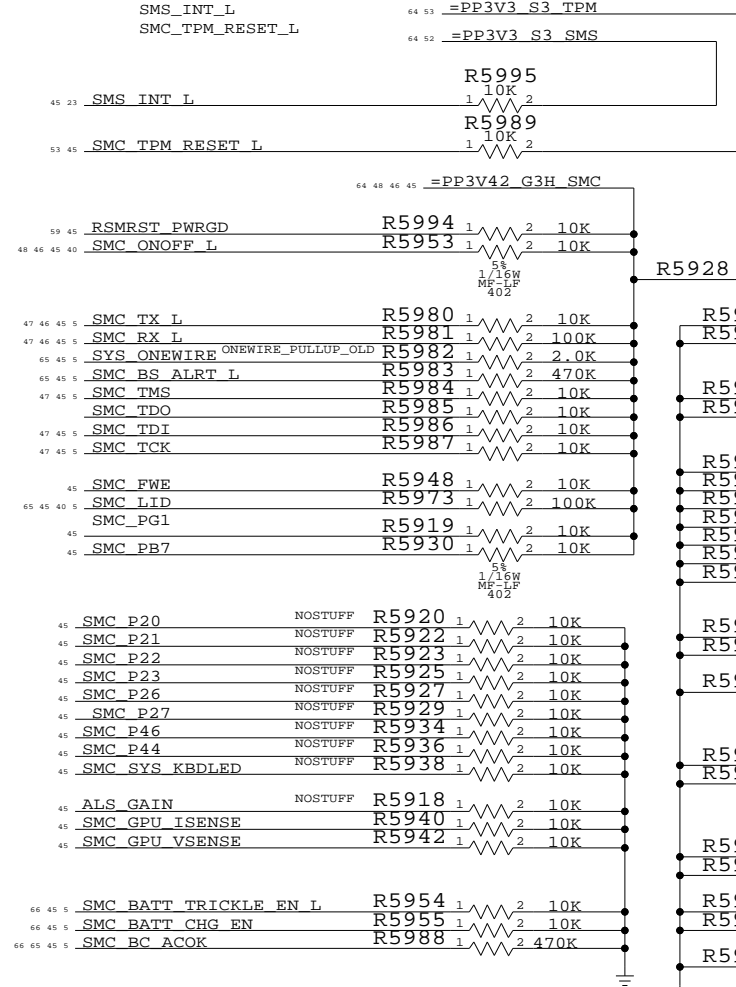
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

SMC G3HOT OSCILLATOR

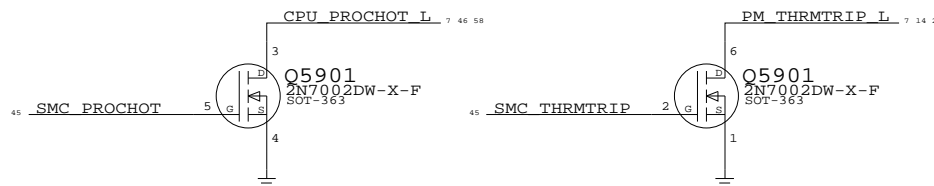


U5910 is really a 32.768KHz oscillator 197S0166

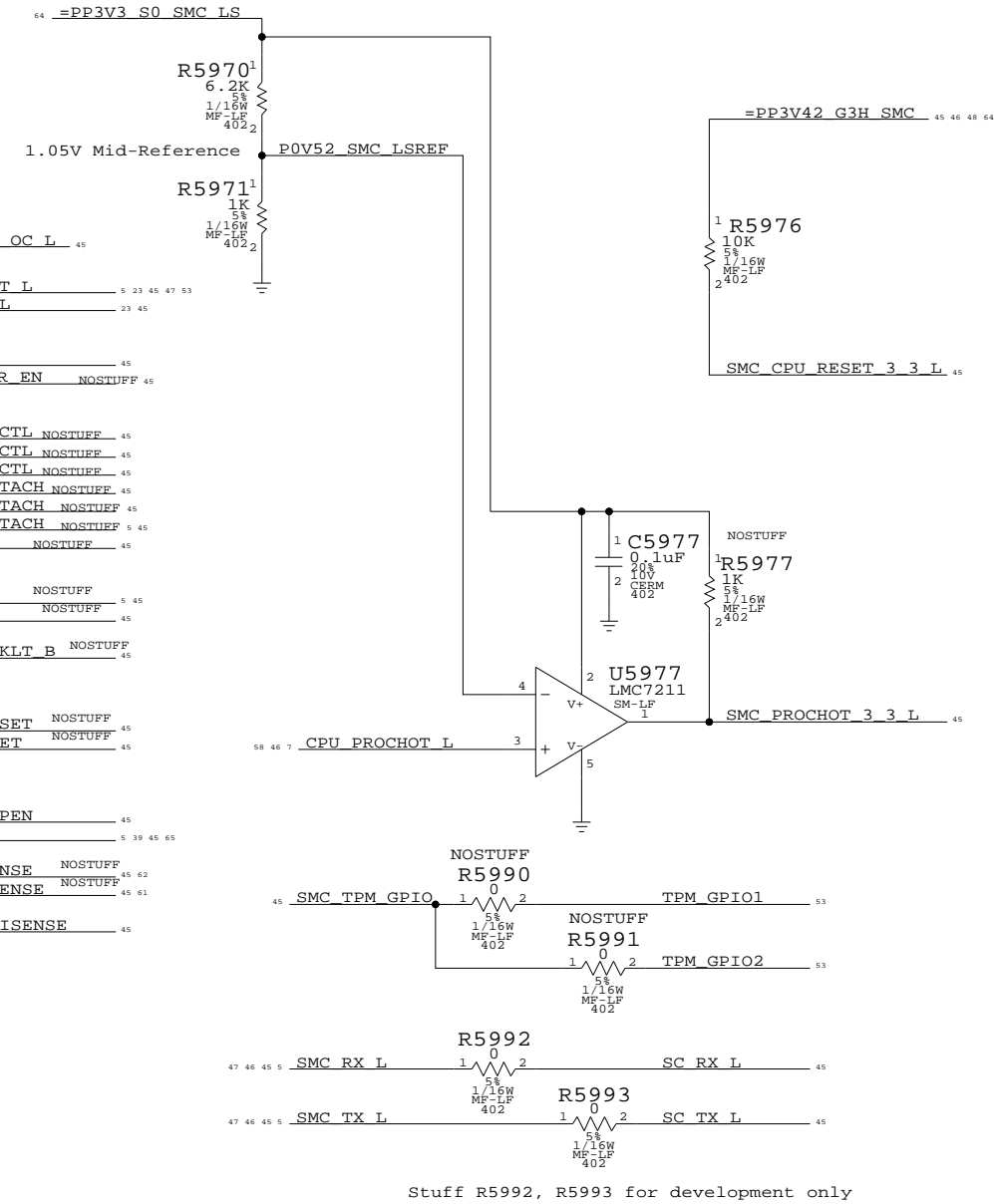
THESE NEED TO BE PULLED TO THE PROPER RAIL:



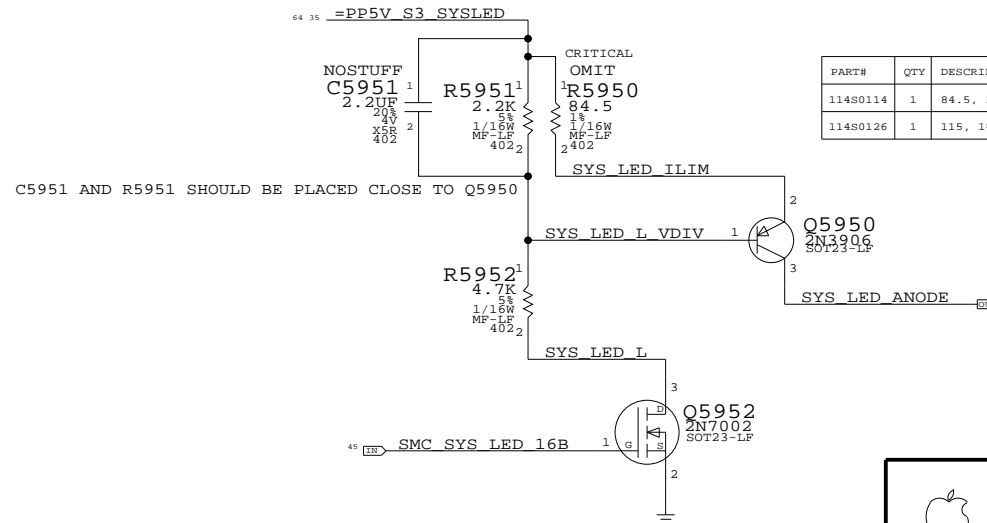
SMC 3.3V to 1.05V Level Shifting



SMC 1.05V to 3.3V Level Shifting



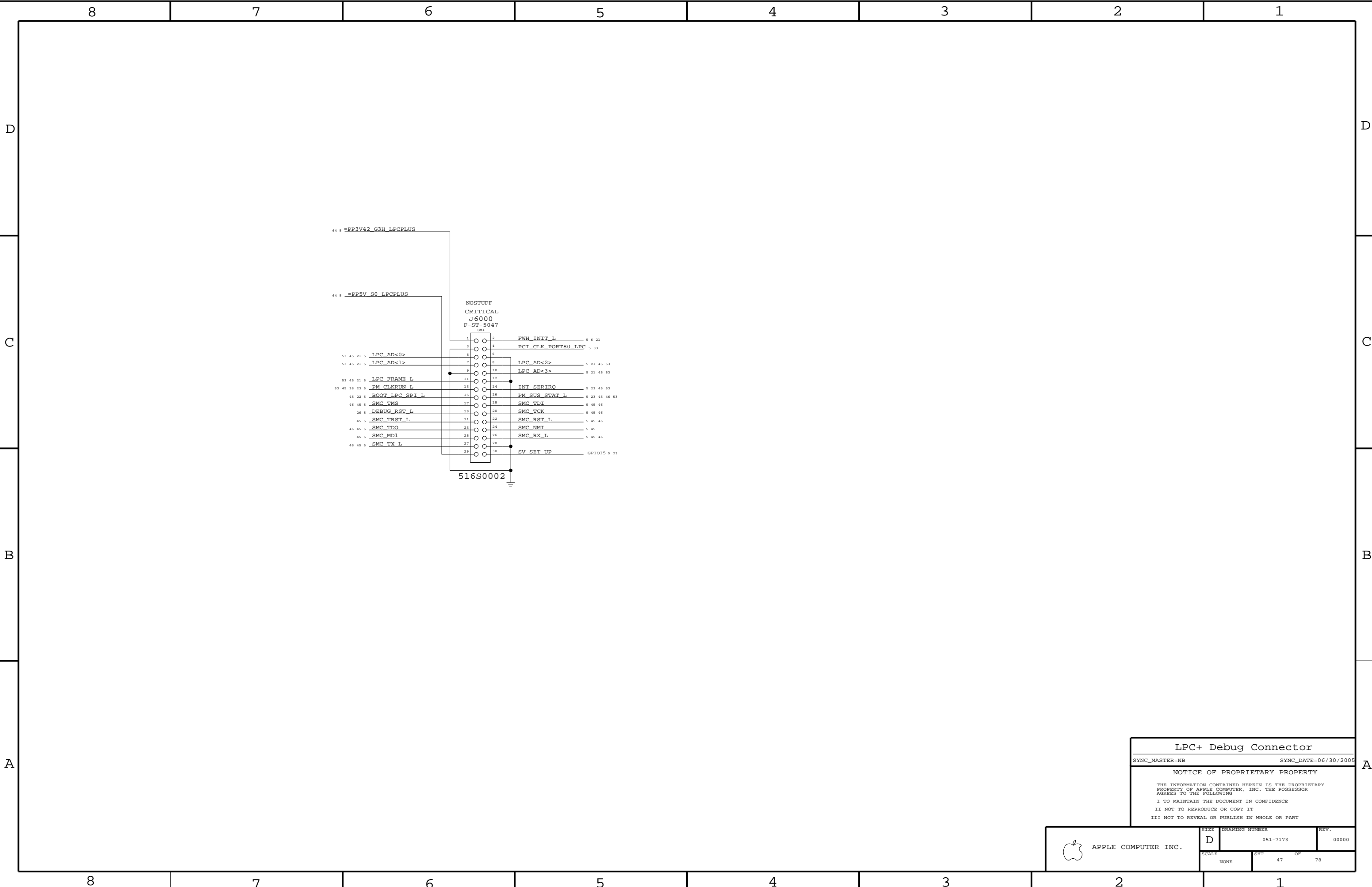
System (Sleep) LED Circuit



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480114	1	84.5, 18, 1/16W, MF-LF, 402	R5950	NORMAL
11480126	1	115, 18, 1/16W, MF-LF, 402	R5950	FANCY

**SMC SUPPORT**  
 SYNC\_MASTER=SMC SYNC\_DATE=08/23/2005  
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 DRAWING NUMBER: D 051-7173  
 SCALE: NONE SHEET: 46 OF 78  
 REV: 00000



**LPC+ Debug Connector**

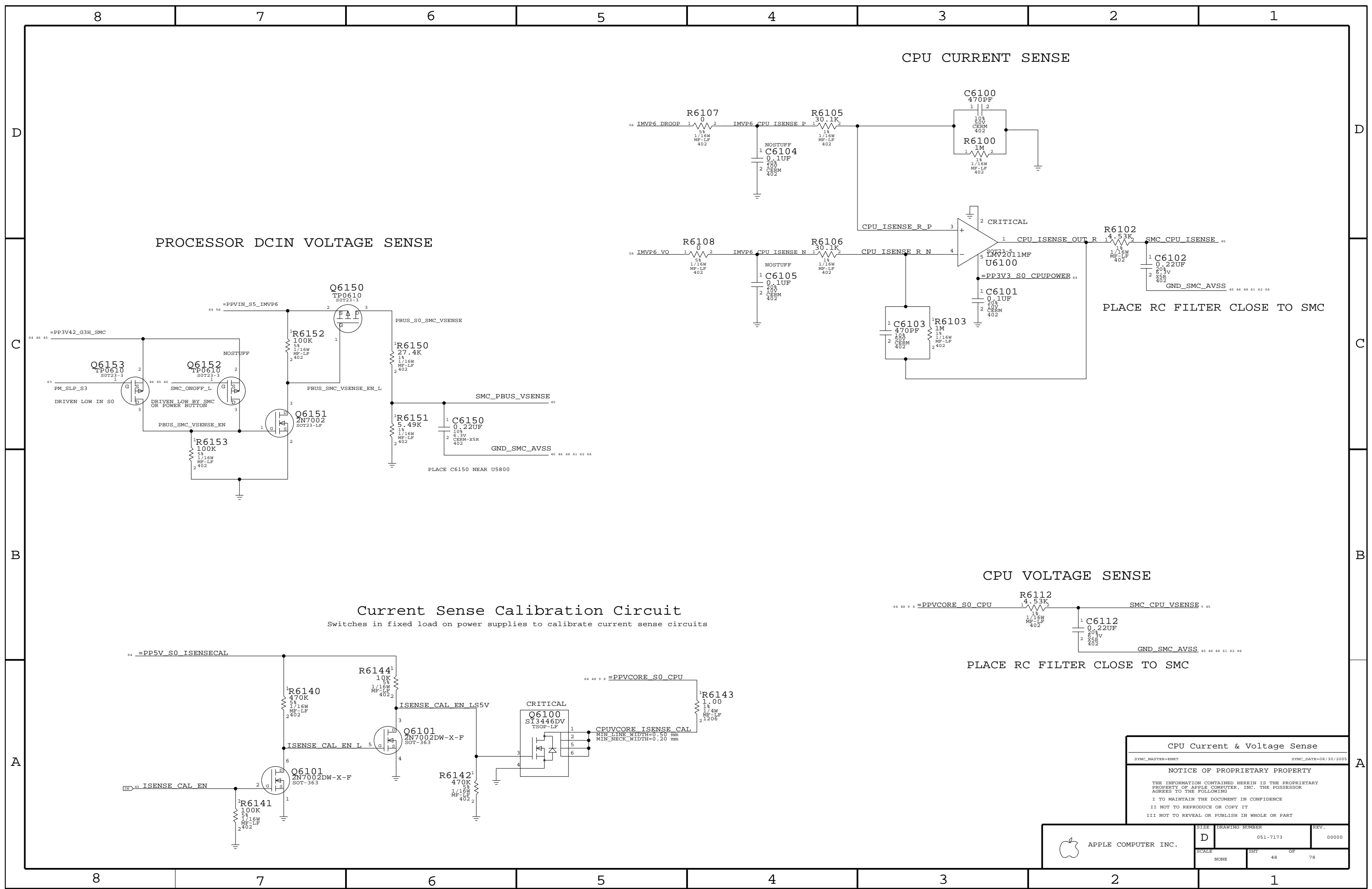
SYNC\_MASTER=NB SYNC\_DATE=06/30/2005

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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	47		



PROCESSOR DCIN VOLTAGE SENSE

CPU CURRENT SENSE

CPU VOLTAGE SENSE

Current Sense Calibration Circuit  
Switches in fixed load on power supplies to calibrate current sense circuits

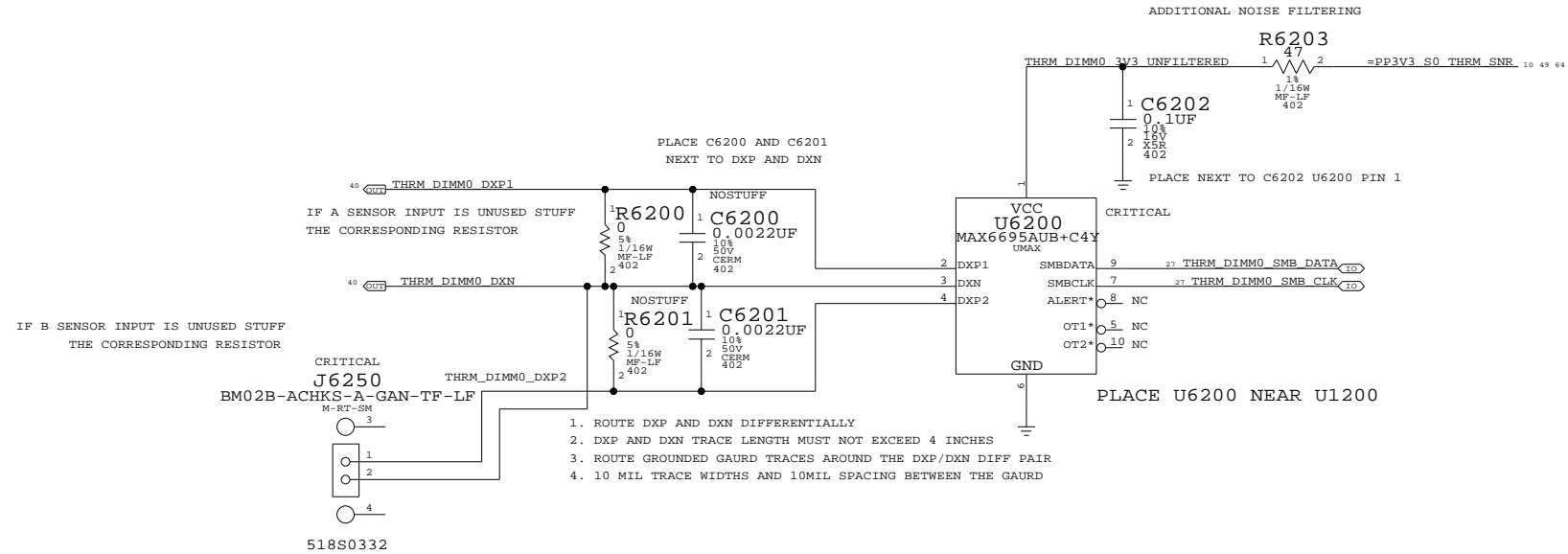
PLACE RC FILTER CLOSE TO SMC

PLACE RC FILTER CLOSE TO SMC

CPU Current & Voltage Sense  
 SYNC\_MASTER=ENBT SYNC\_DATE=08/30/2005  
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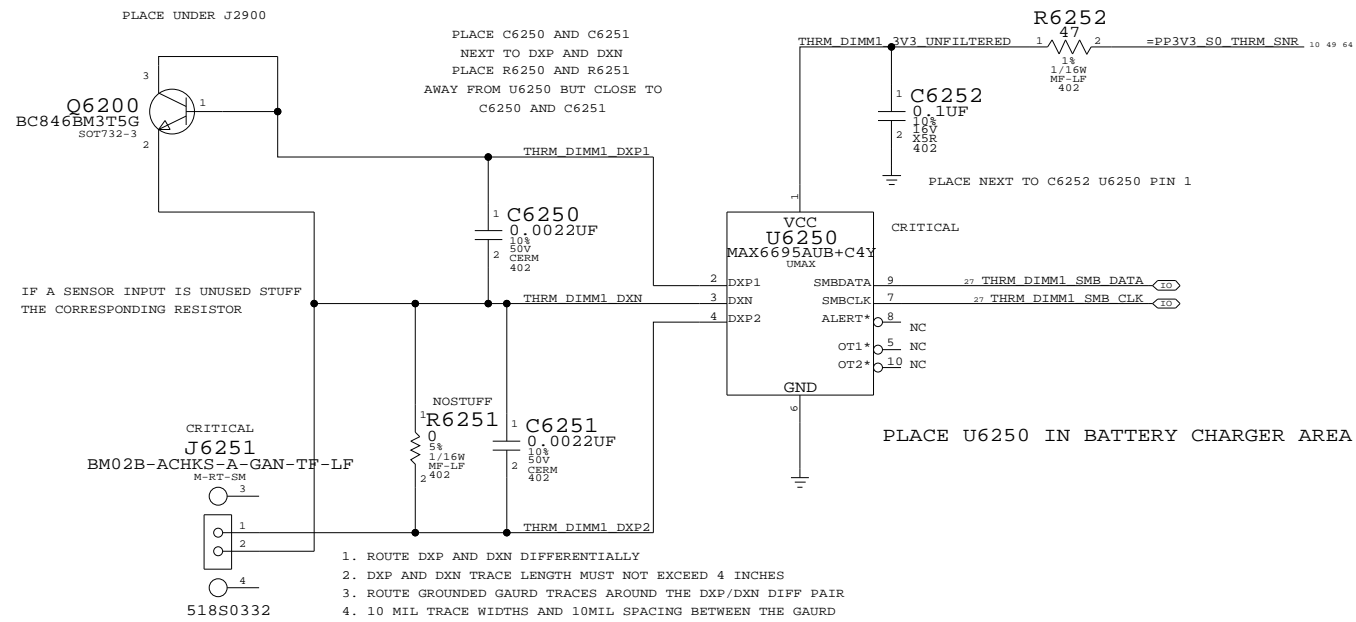
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	48	78	

### DIMM0 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452  
 AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

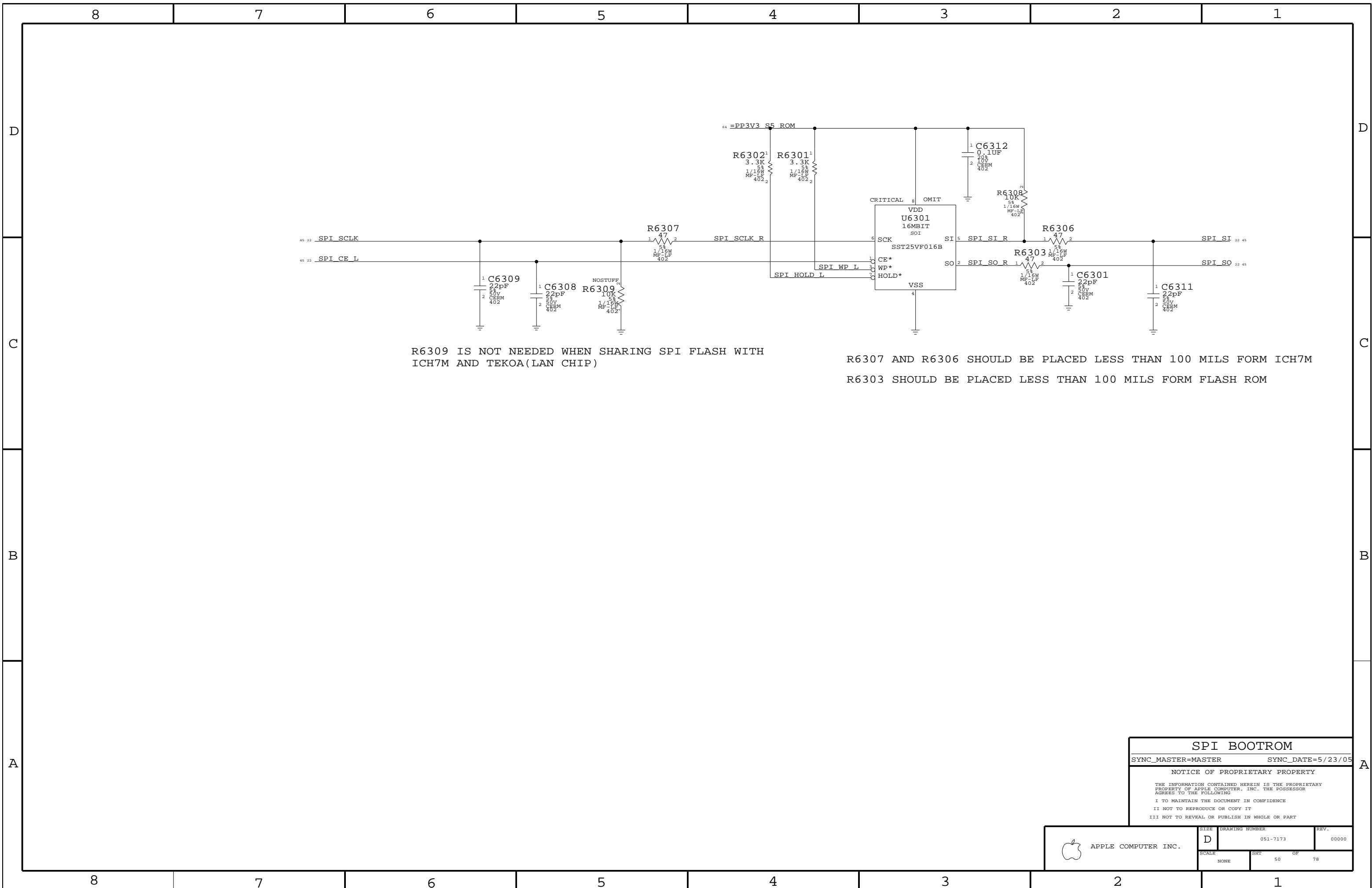
### DIMM1 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452  
 AFTER THIS CHANGE, THE SCHEAMTIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

TEMPERATURE SENSE	
SYNC_MASTER=ENET	SYNC_DATE=11/09/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	49	78	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M  
 R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

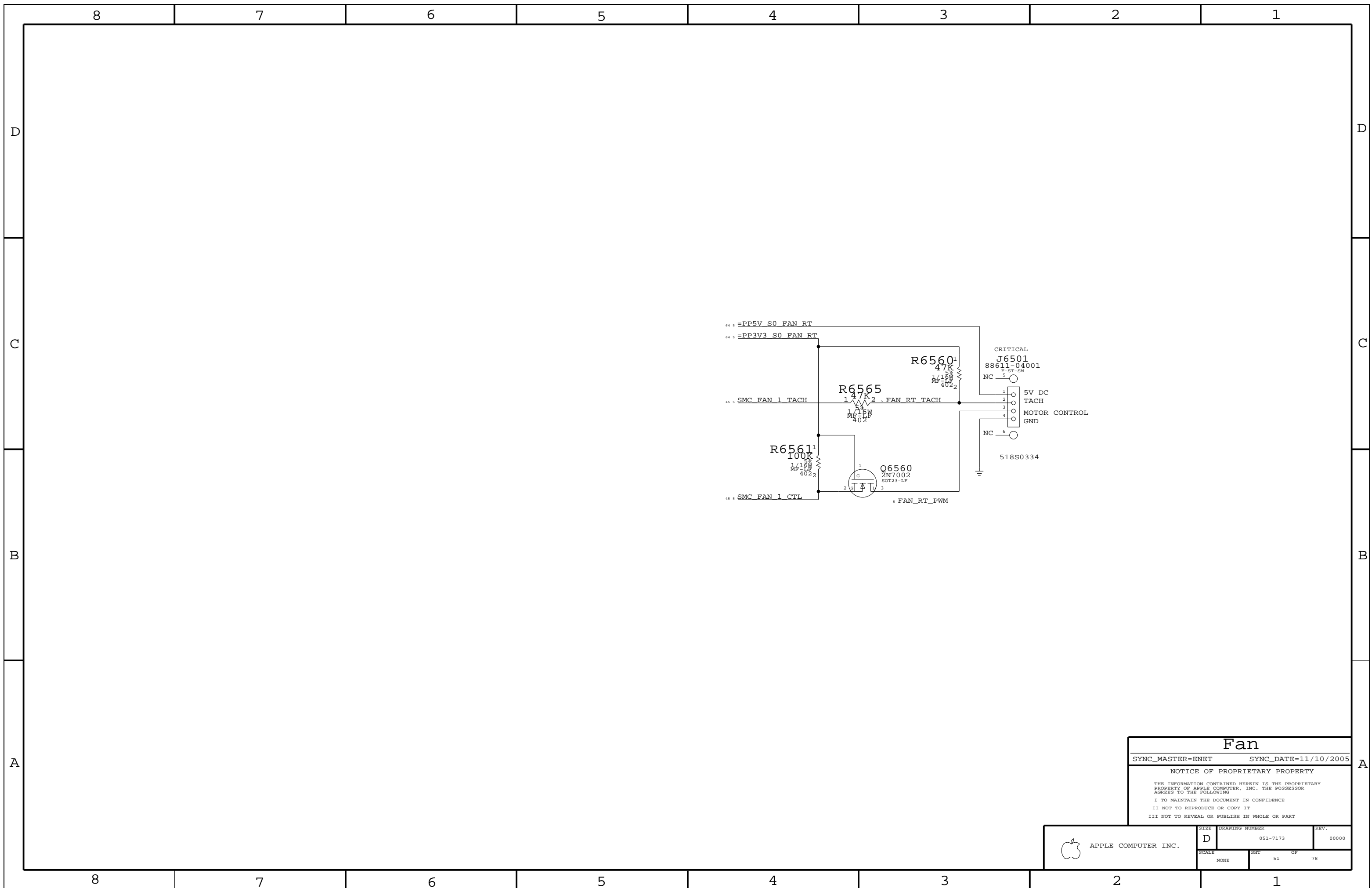
**SPI BOOTROM**  
 SYNC\_MASTER=MASTER SYNC\_DATE=5/23/05

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SCALE	SHT	OF	78
NONE	50		



**Fan**

SYNC\_MASTER=ENET      SYNC\_DATE=11/10/2005

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	SCALE NONE	SHEET 51	OF 78



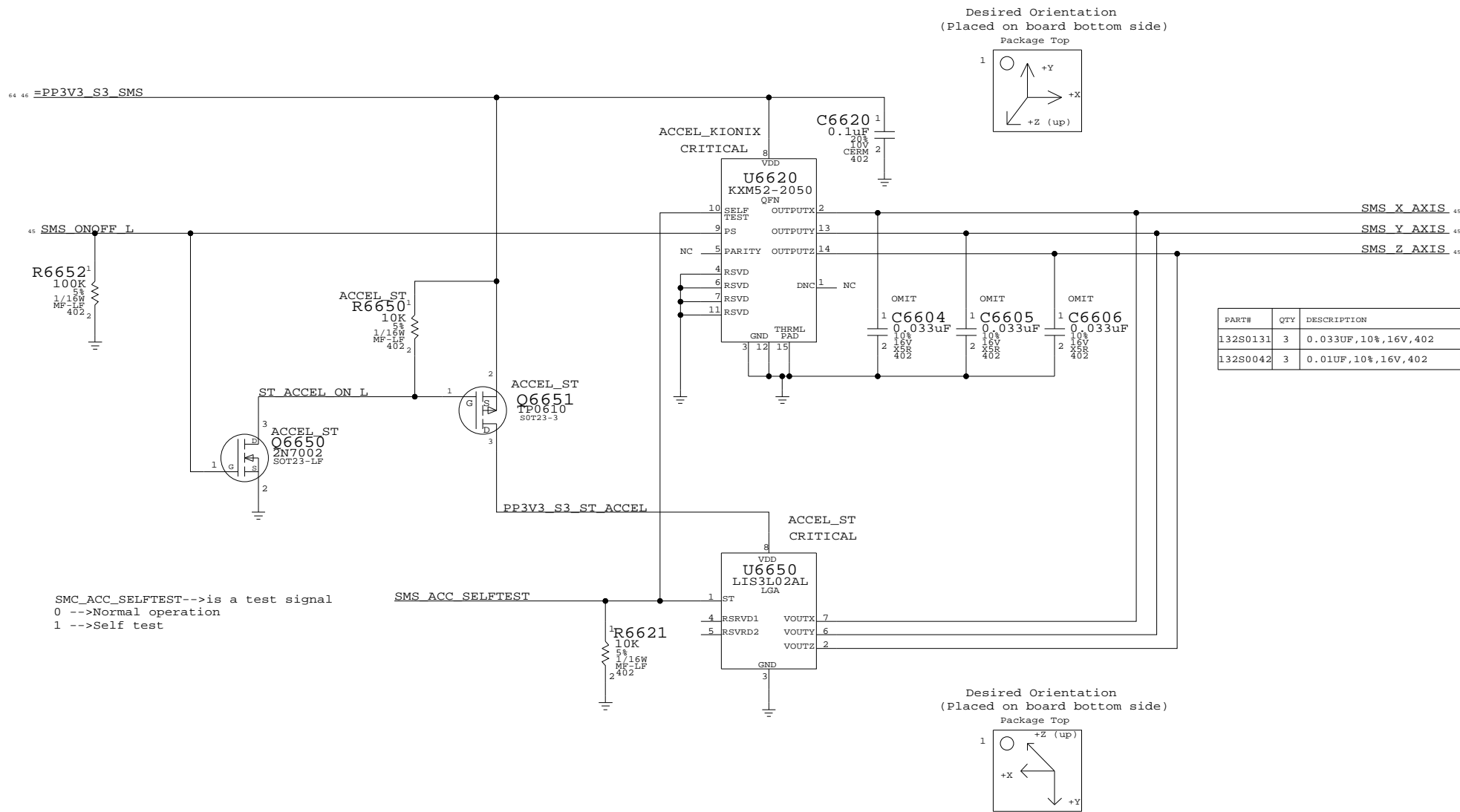
PAGE NOTES

INPUT  
 =PP3V3\_S3\_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)  
 SMS\_ONOFF\_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT  
 SMS\_ACC\_\*\_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE  
 7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050  
 7/26/2005 - CONNECTED PD PIN TO SMC'S SMS\_ONOFF\_L  
 7/26/2005 -



R6652  
 100K  
 5%  
 1/16W  
 MF-LF  
 402

R6650  
 10K  
 5%  
 1/16W  
 MF-LF  
 402

Q6650  
 2N7002  
 SOT23-LF

Q6651  
 TP0610  
 SOT23-3

R6621  
 10K  
 5%  
 1/16W  
 MF-LF  
 402

C6620  
 0.1uF  
 10%  
 CERM  
 402

C6604  
 0.033uF  
 10%  
 16V  
 X5R  
 402

C6605  
 0.033uF  
 10%  
 16V  
 X5R  
 402

C6606  
 0.033uF  
 10%  
 16V  
 X5R  
 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

SMC\_ACC\_SELFTEST-->is a test signal  
 0 -->Normal operation  
 1 -->Self test

**SMS**

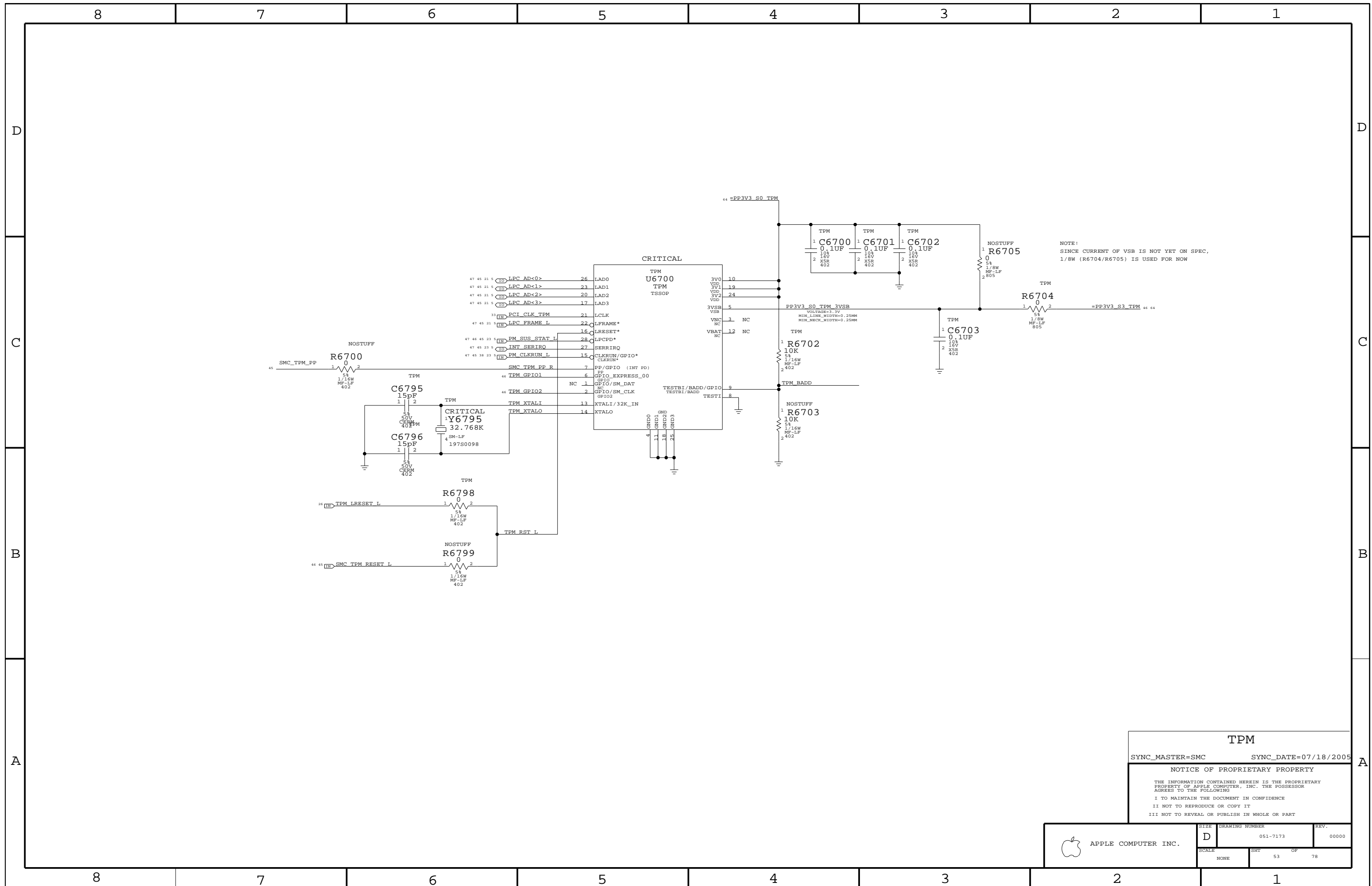
SYNC\_MASTER=SMC      SYNC\_DATE=08/23/2005

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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	52		



NOTE:  
 SINCE CURRENT OF VSB IS NOT YET ON SPEC,  
 1/8W (R6704/R6705) IS USED FOR NOW

**TPM**

SYNC\_MASTER=SMC      SYNC\_DATE=07/18/2005

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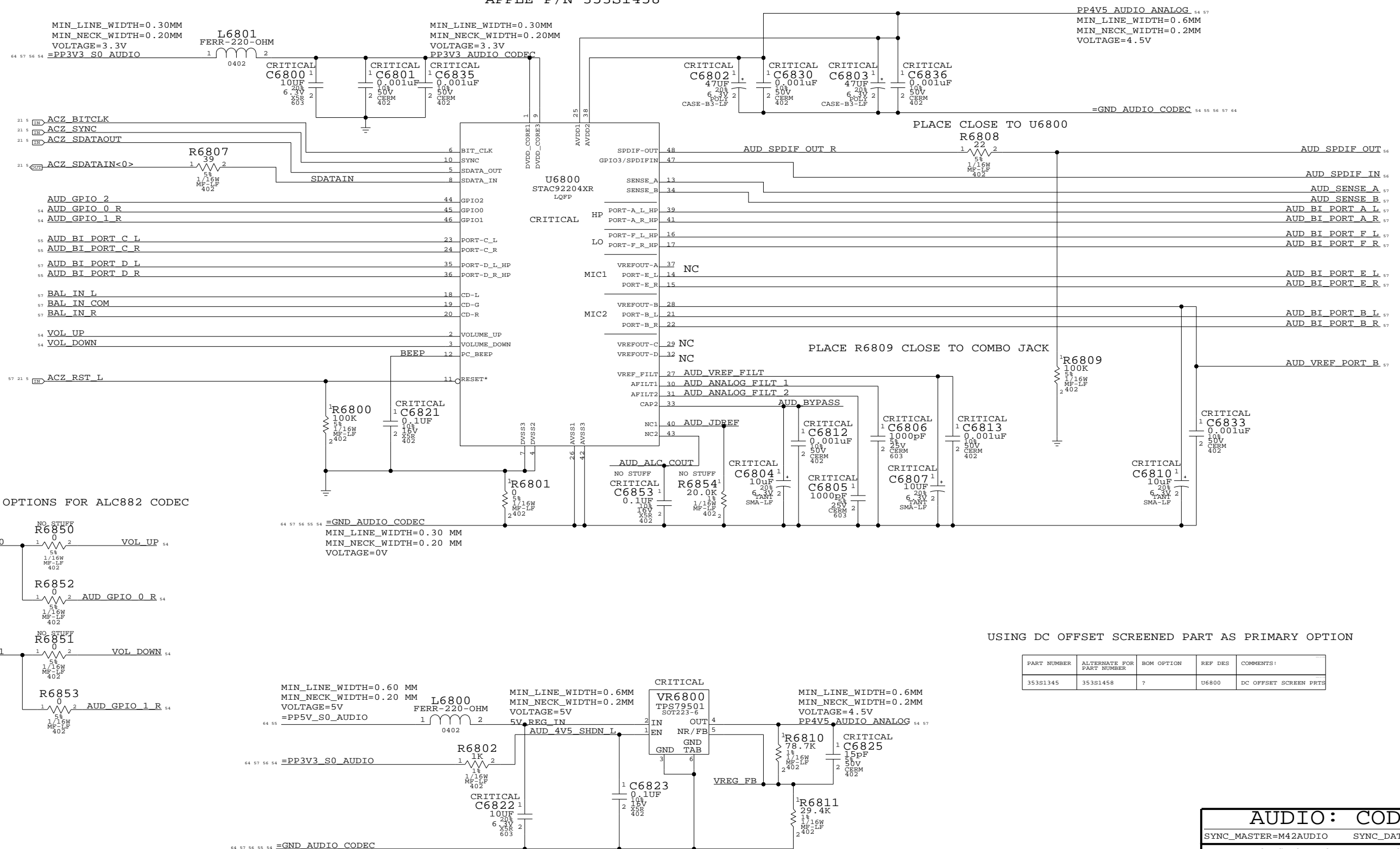
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 53	OF 78

# AUDIO CODEC

## APPLE P/N 353S1458



### 4.5V POWER SUPPLY FOR CODEC

USING DC OFFSET SCREENED PART AS PRIMARY OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
353S1345	353S1458	?	U6800	DC OFFSET SCREEN PRTS

**AUDIO: CODEC**

SYNC\_MASTER=M42AUDIO    SYNC\_DATE=08/05/2006

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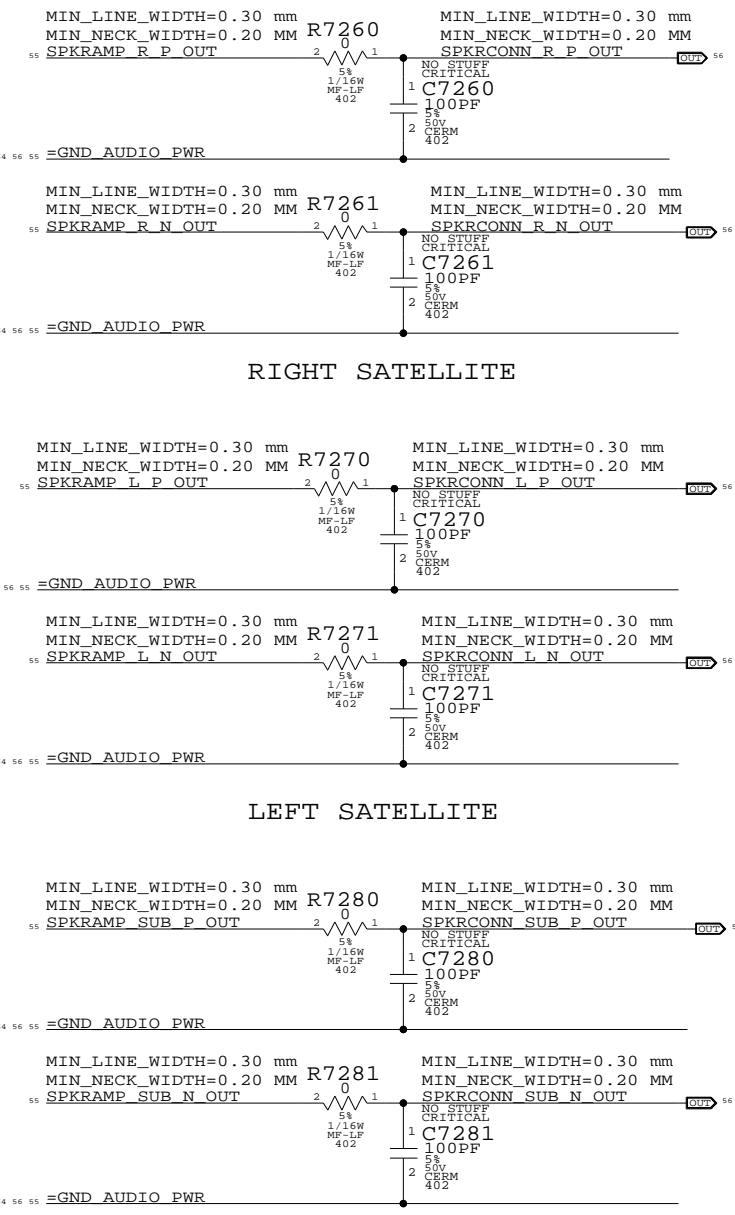
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	NONE	D 051-7173	00000
SCALE	SHT	OF	78
		54	

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 442 Hz < FC < 736 Hz  
 SUB 169 Hz < FC < 282 Hz

SPEAKER OUTPUT EMI FILTERS



RIGHT SATELLITE

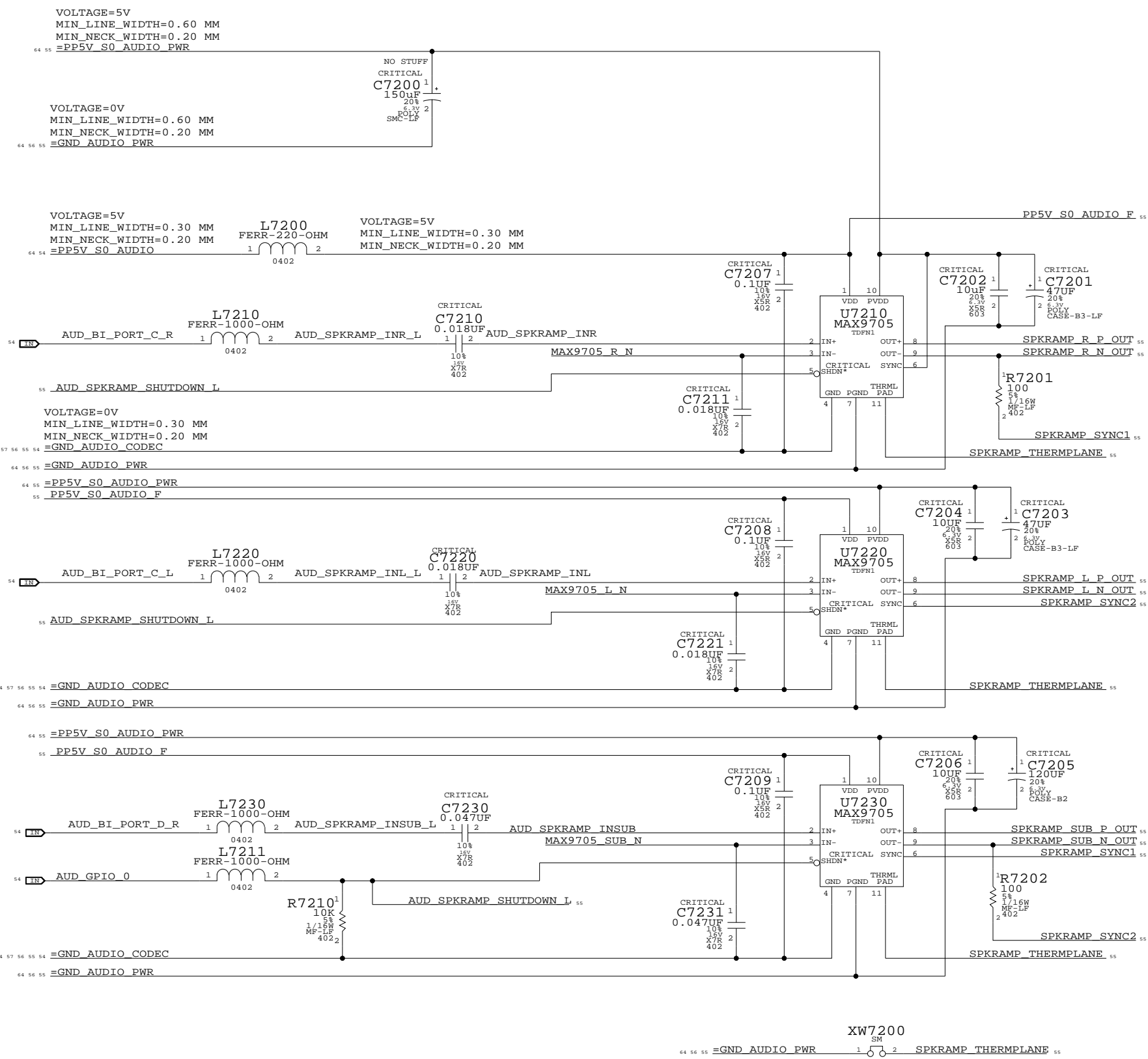
LEFT SATELLITE

SUB-TWEETER

AUDIO: SPEAKER AMP

SYNC\_MASTER=M42AUDIO SYNC\_DATE=08/05/2006  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	NONE	SHT	OF
		55	78



XW7200

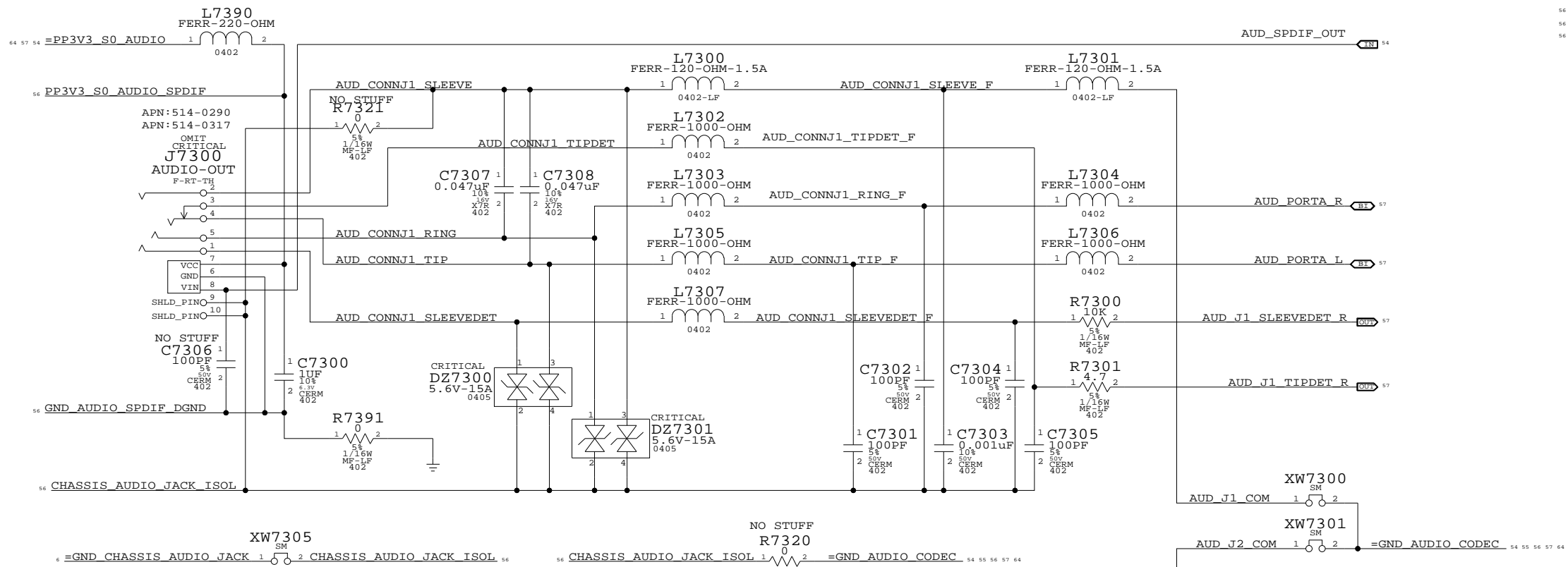
D  
C  
B  
A

D  
C  
B  
A

8 7 6 5 4 3 2 1

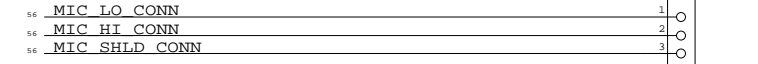
8 7 6 5 4 3 2 1

### AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX



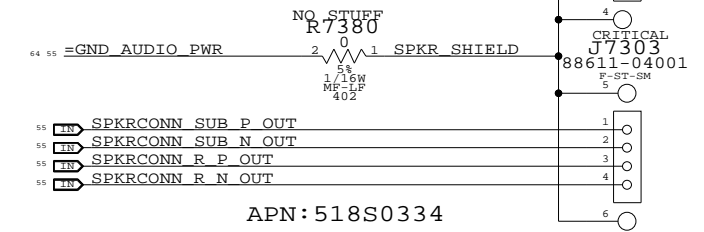
### MIC CONNECTOR

APN: 514S0392

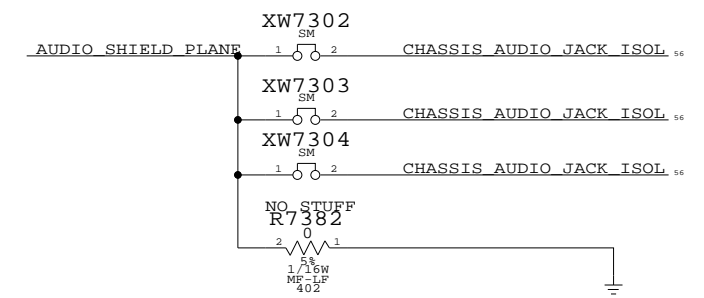


### SPEAKER CONNECTOR

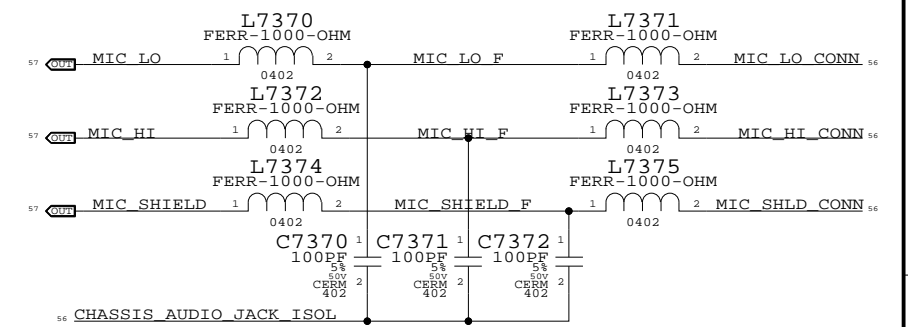
APN: 518S0332



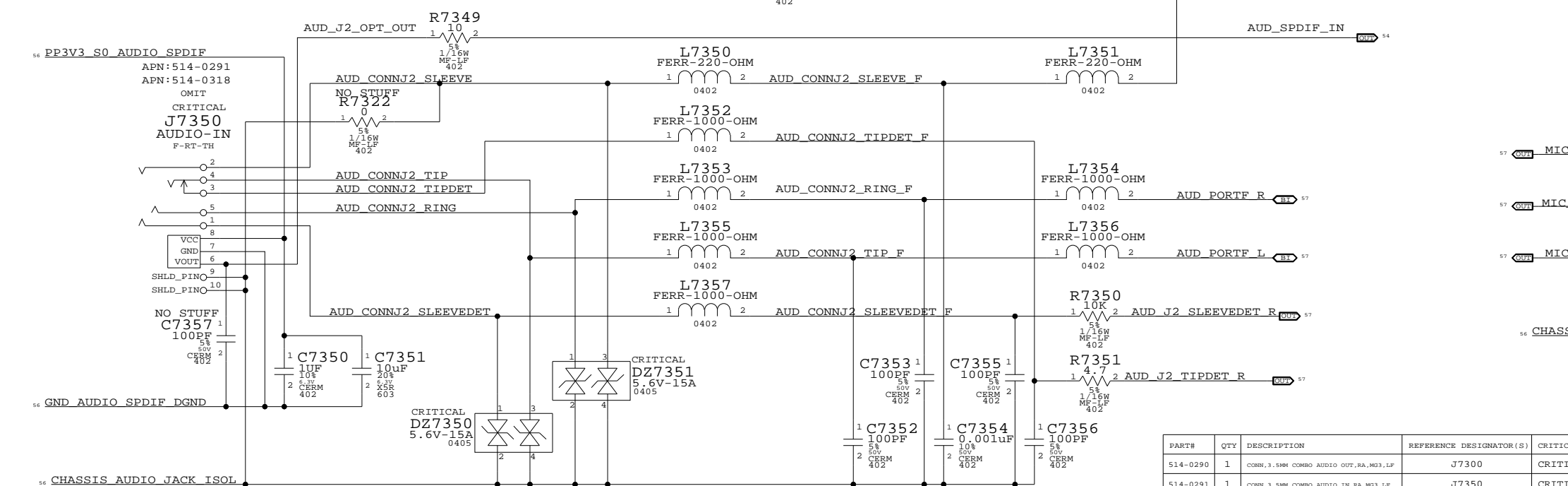
### AUDIO SHIELD FILL



### MIC EMI FILTER



### AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0290	1	CONN, 3.5MM COMBO AUDIO OUT, RA, MG3, LF	J7300	CRITICAL	NORMAL
514-0291	1	CONN, 3.5MM COMBO AUDIO IN, RA, MG3, LF	J7350	CRITICAL	NORMAL
514-0317	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J7300	CRITICAL	FANCY
514-0318	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J7350	CRITICAL	FANCY

**AUDIO: JACK**

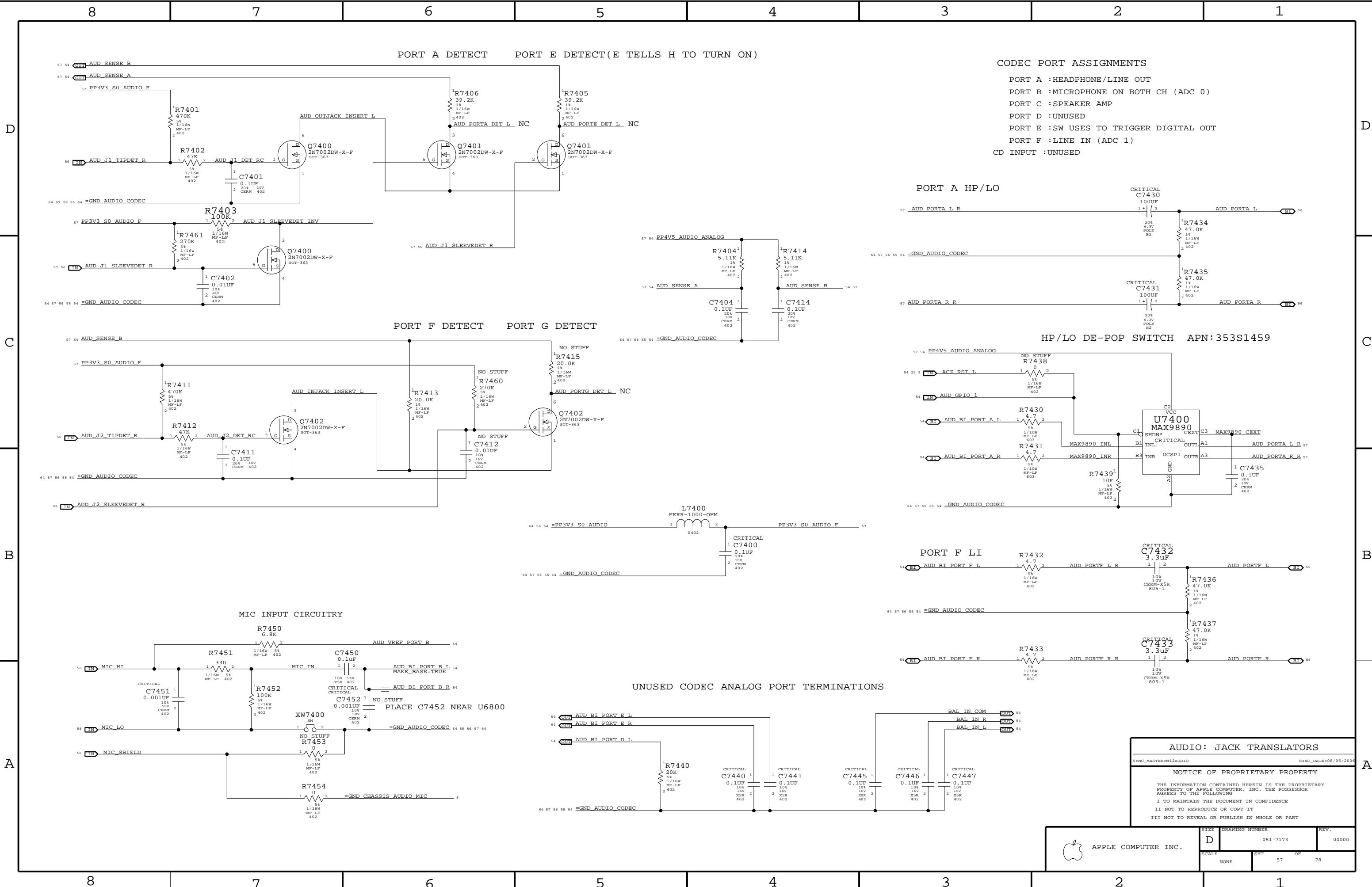
SYNC\_MASTER=M42AUDIO SYNC\_DATE=08/05/2006

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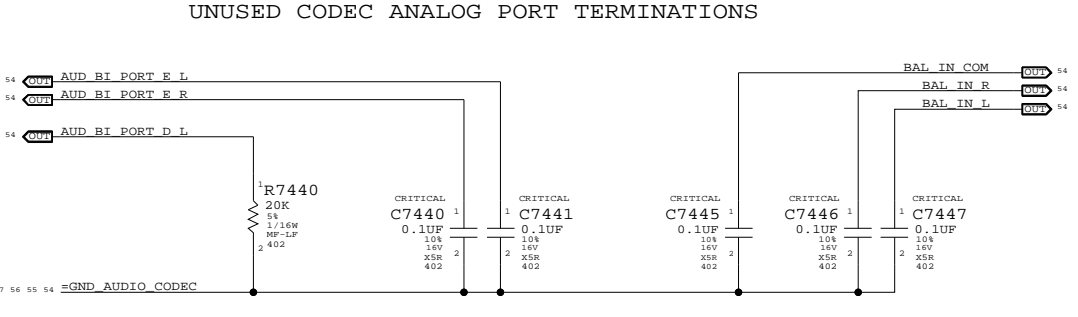
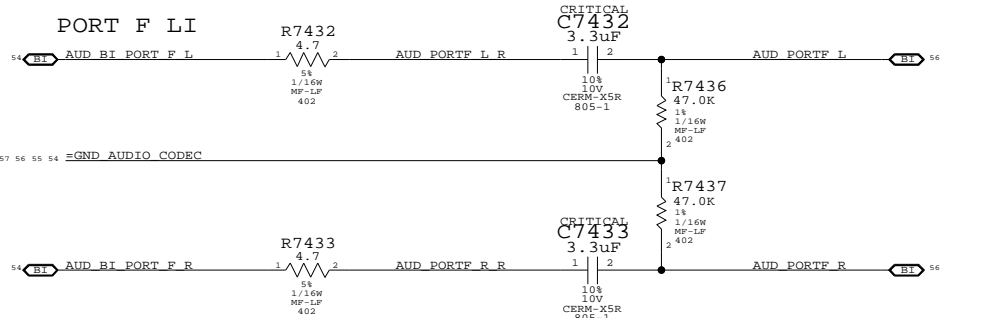
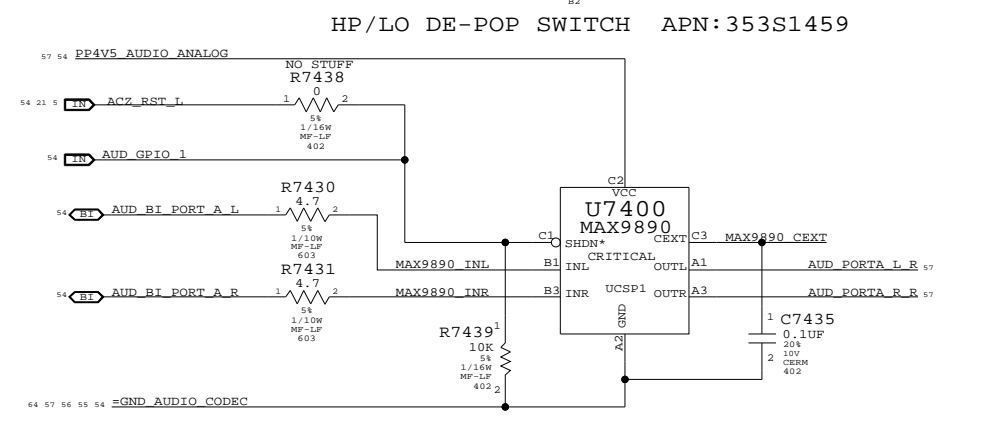
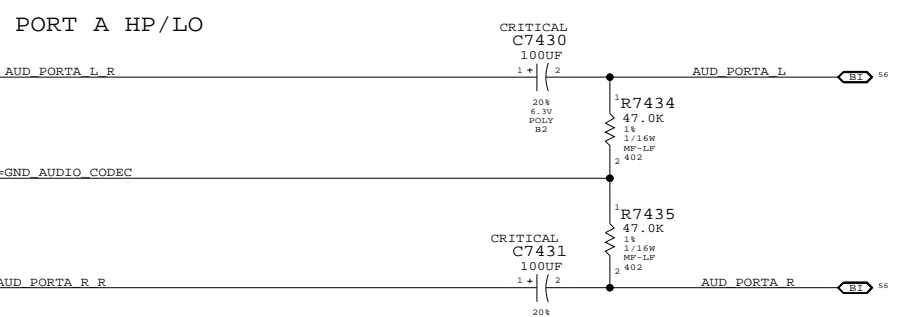
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHEET		OF
NONE	56		78

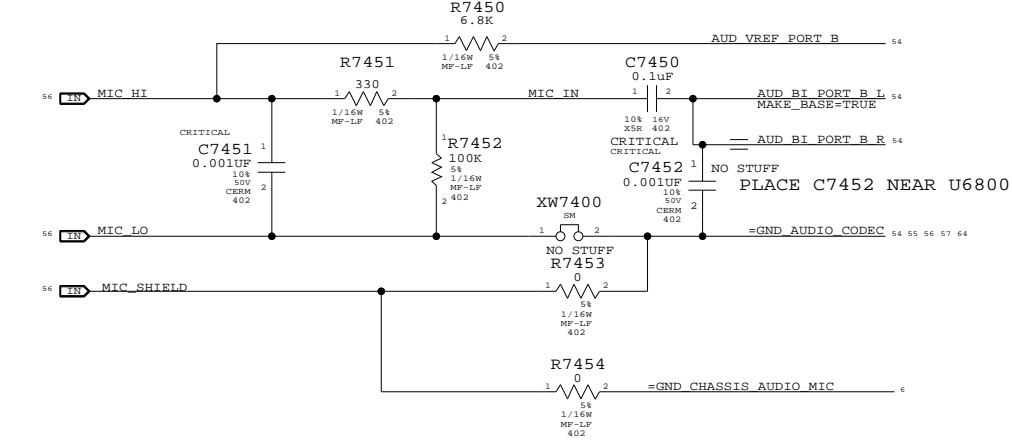


**CODEC PORT ASSIGNMENTS**

PORT A : HEADPHONE/LINE OUT  
 PORT B : MICROPHONE ON BOTH CH (ADC 0)  
 PORT C : SPEAKER AMP  
 PORT D : UNUSED  
 PORT E : SW USES TO TRIGGER DIGITAL OUT  
 PORT F : LINE IN (ADC 1)  
 CD INPUT : UNUSED



**MIC INPUT CIRCUITRY**



**AUDIO: JACK TRANSLATORS**

SYNC\_MASTER=M42AUDIO SYNC\_DATE=08/05/2006

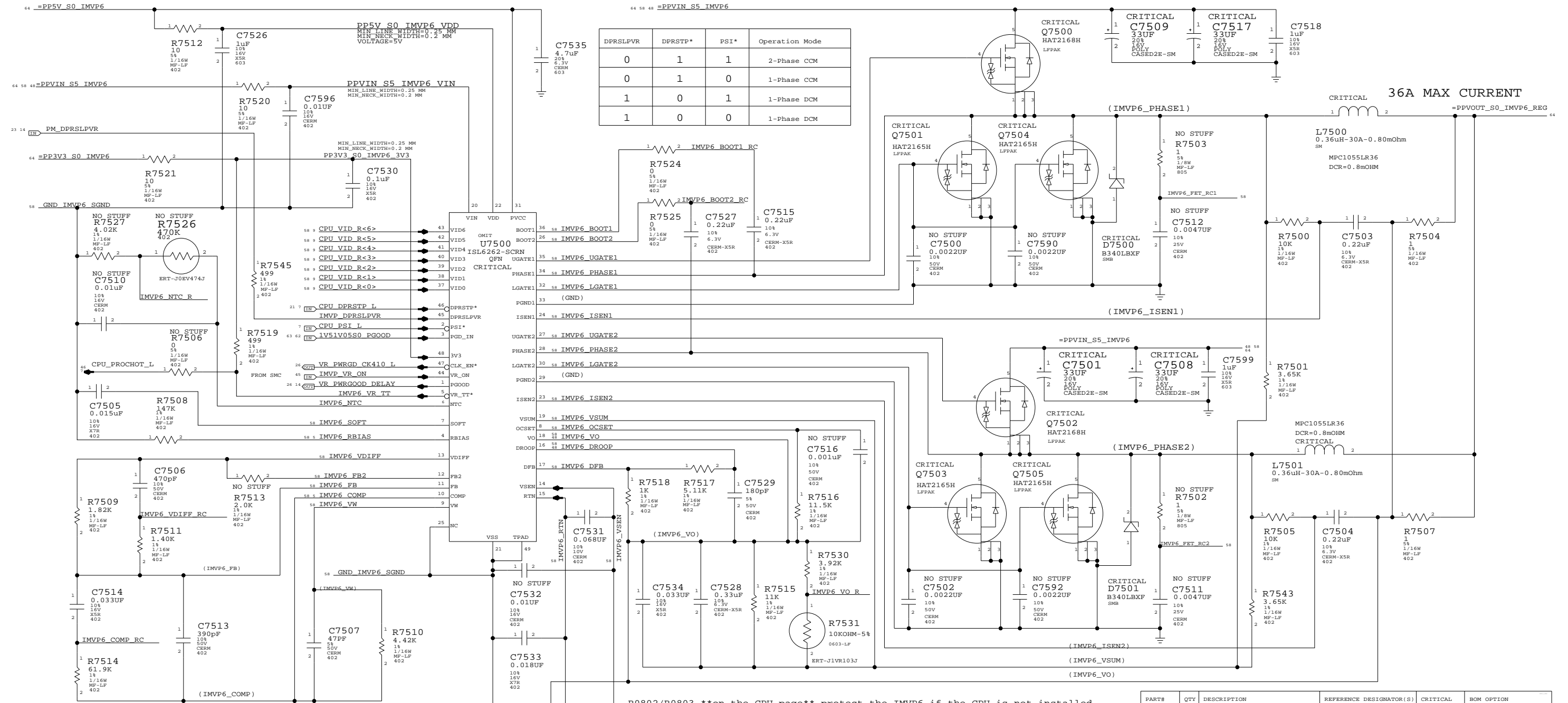
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	7	C7501_C7508	RENET T520V3300016AT0457650
128S0093	128S0092	7	C7509_C7517	RENET T520V3300016AT0457650

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM



Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

R0802/R0803 \*\*on the CPU page\*\* protect the IMVP6 if the CPU is not installed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

# IMVP6 CPU VCore Regulator

Pin Name	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

Pin Name	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

Pin Name	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

## IMVP6 CPU VCore Regulator

SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

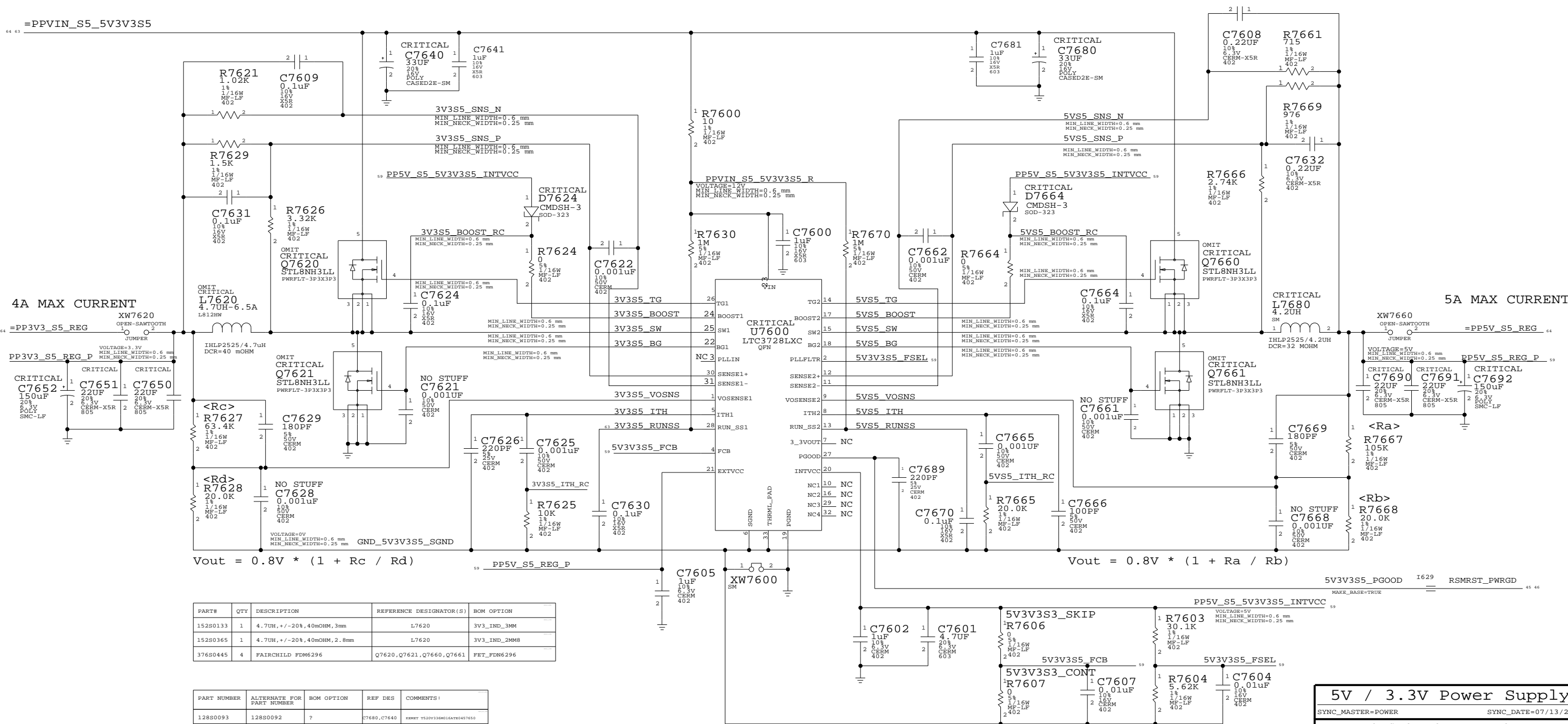
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APPLE COMPUTER INC.	SCALE	SHEET	OF	REV.
	NONE	58	78	00000



# 5V / 3.3V POWER SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0133	1	4.7UH, +/-20%, 40mOHM, 3mm	L7620	3V3_IND_3MM
152S0365	1	4.7UH, +/-20%, 40mOHM, 2.8mm	L7620	3V3_IND_2MM8
376S0445	4	FAIRCHILD FDM6296	Q7620, Q7621, Q7660, Q7661	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7680, C7640	RENET VS20V330M16ATE0487650
376S0448	376S0445	?	Q7620, Q7621	VISHAY SI7806ADN
376S0448	376S0445	?	Q7660, Q7661	VISHAY SI7806ADN

$V_{out} = 0.8V * (1 + R_c / R_d)$

$V_{out} = 0.8V * (1 + R_a / R_b)$

## 5V / 3.3V Power Supply

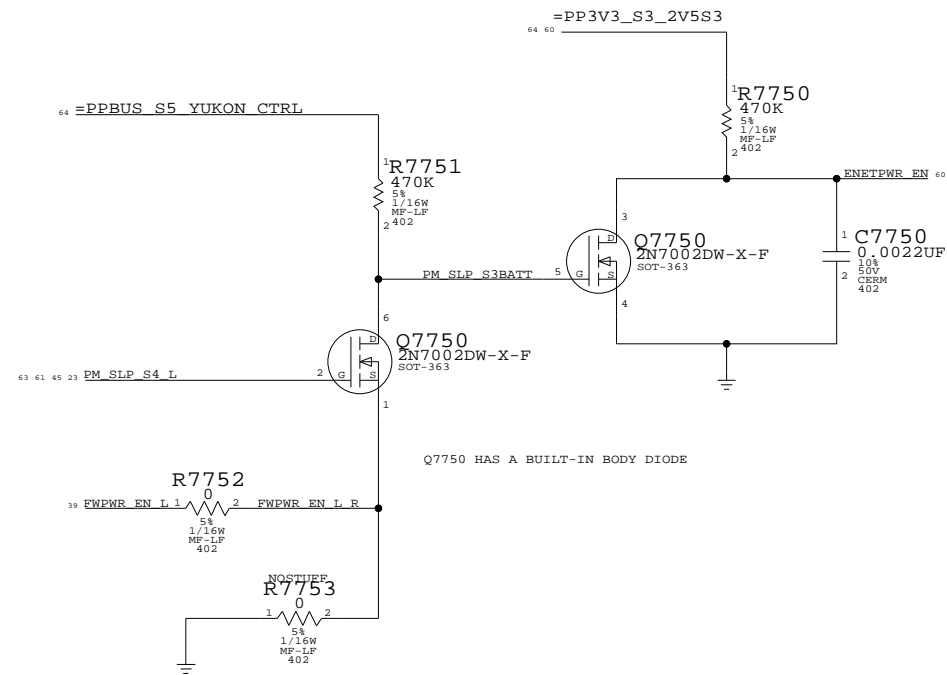
SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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APPLE COMPUTER INC.	DRAWING NUMBER <b>D</b> 051-7173	REV. 00000
	SCALE NONE	SHEET 59 OF 78

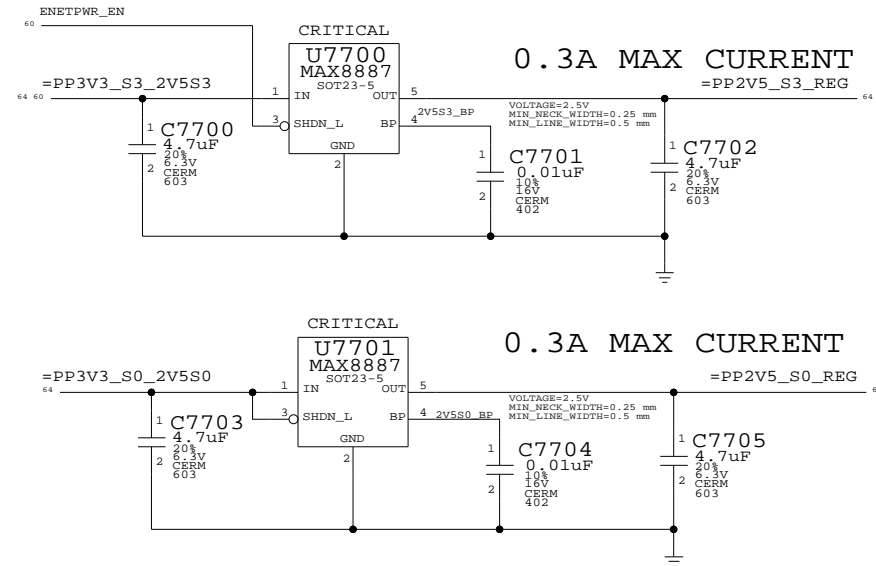
# YUKON POWER CONTROL



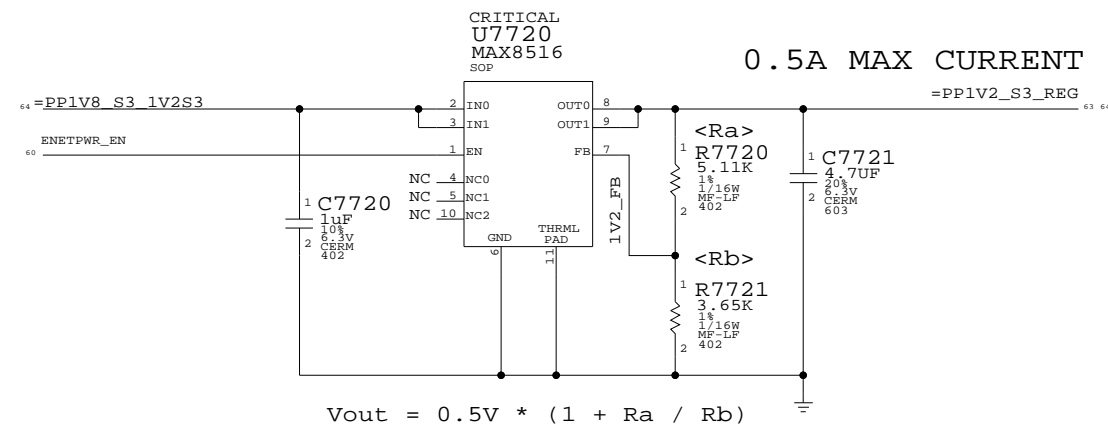
NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3   S0	~S0   ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR\_EN IS BUFFERED PM\_SLP\_S4\_L

# 2.5V REGULATORS



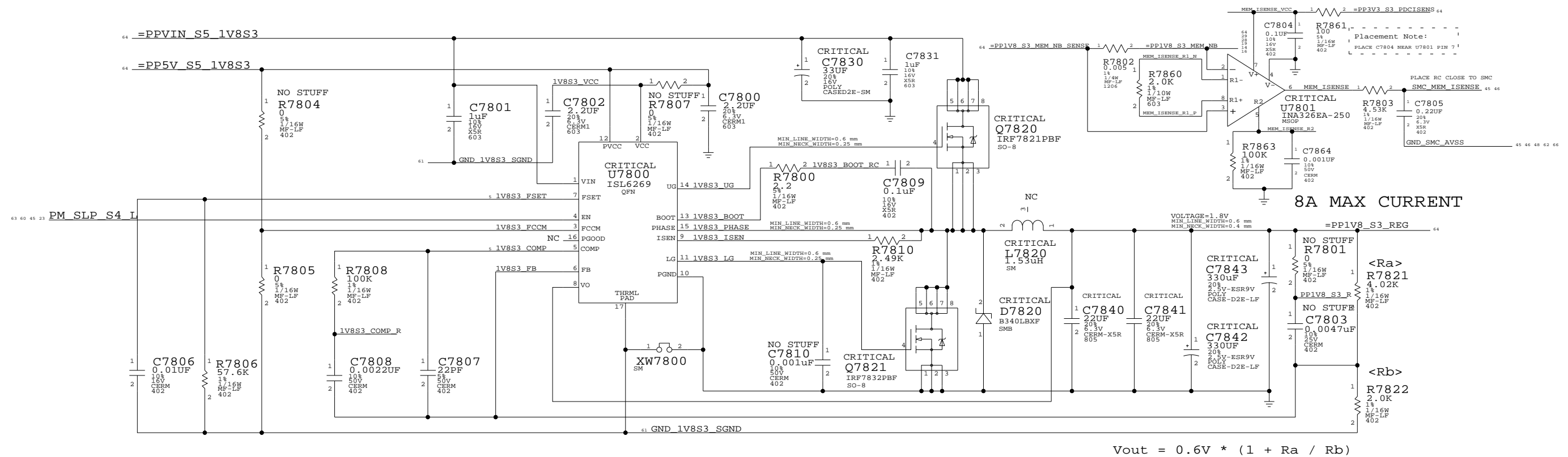
# 1.2V REGULATOR



**2.5V/1.2V Regulator**  
 SYNC\_MASTER=ENET SYNC\_DATE=12/06/2005  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	78
NONE		60	

# 1.8V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	ERRY 7520V330M16AT0457450

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842, C7843	PANASONIC KEPSX0D331ER
128S0095	128S0060	?	C7842, C7843	PANASONIC KEPSX0D331EK

**1.8V Supply**

SYNC\_MASTER=POWER      SYNC\_DATE=07/13/2005

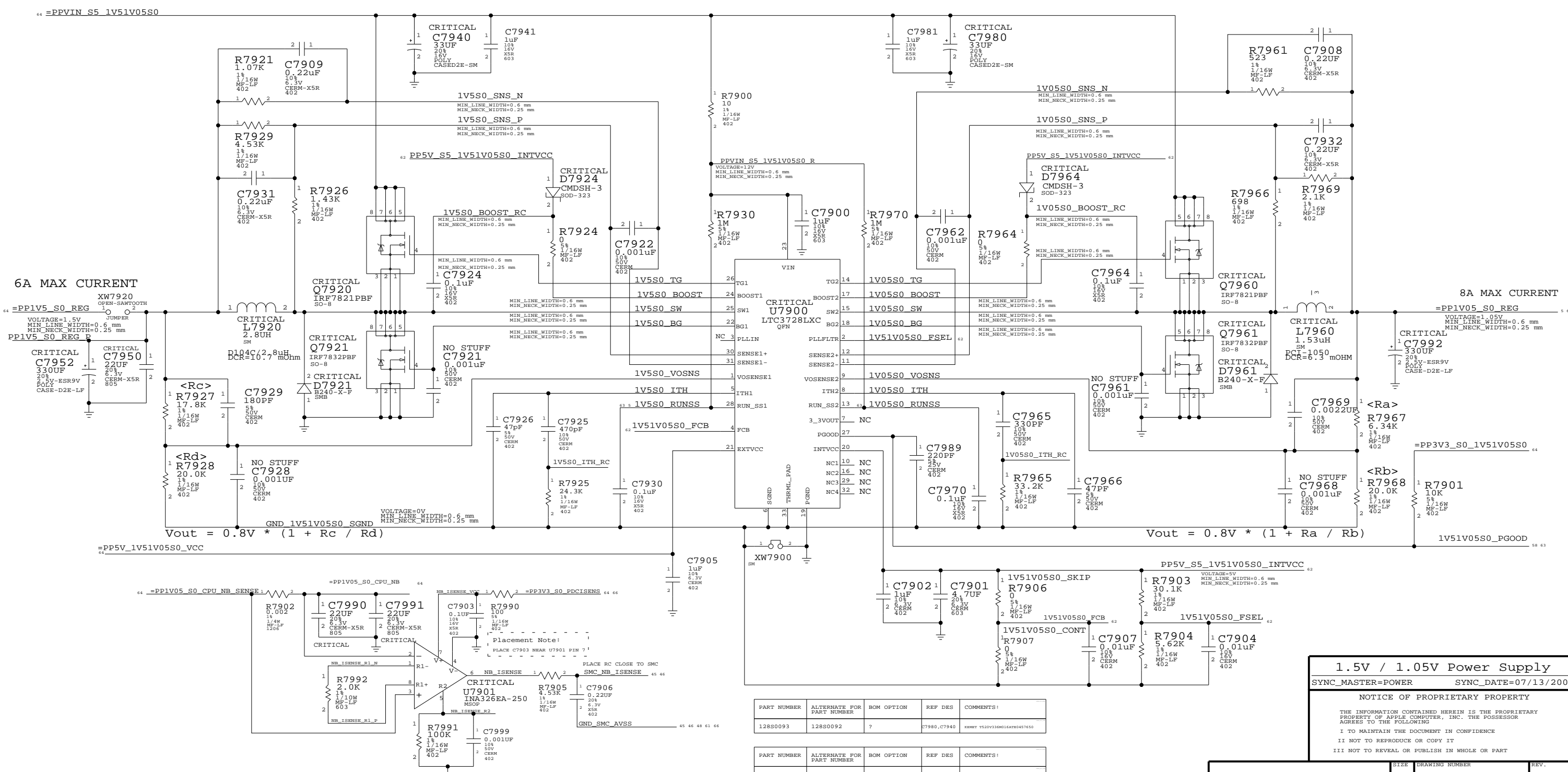
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	78
NONE		61	

# 1.5V/1.05V POWER SUPPLY



$V_{out} = 0.8V * (1 + R_c / R_d)$

$V_{out} = 0.8V * (1 + R_a / R_b)$

1.5V / 1.05V Power Supply  
 SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7980, C7940	RENT 7520V3H001A040457450

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7952, C7992	PANASONIC EEPX003311E
128S0095	128S0060	?	C7952, C7992	PANASONIC EEPX003311E

APPLE COMPUTER INC.

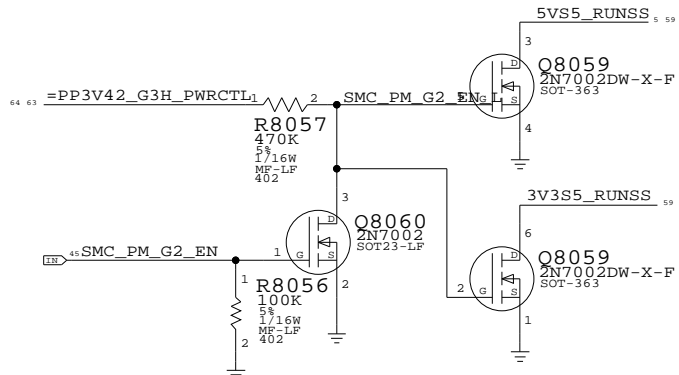
SCALE	DRAWING NUMBER	REV.
NONE	D 051-7173	00000
SHT	62	OF 78

# POWER CONTROL SIGNALS

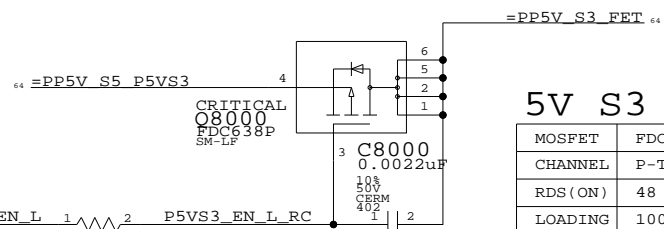
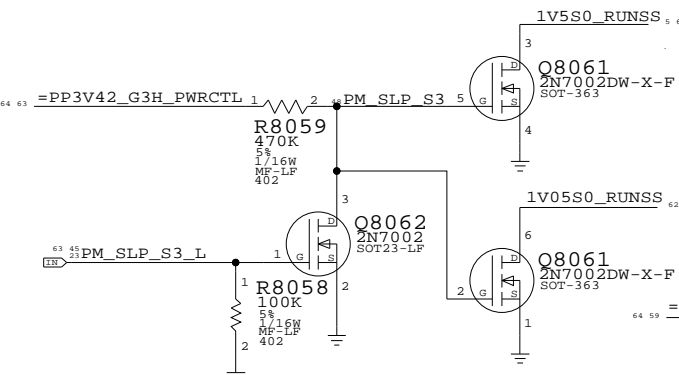
These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

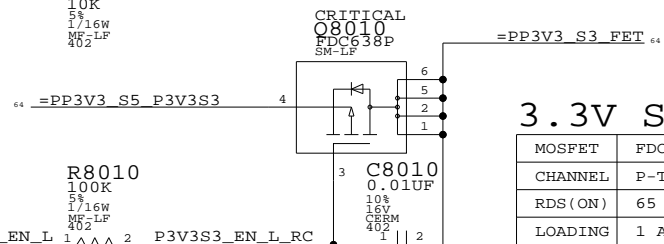
## 5V/3.3V S5 RUN/SS CONTROL



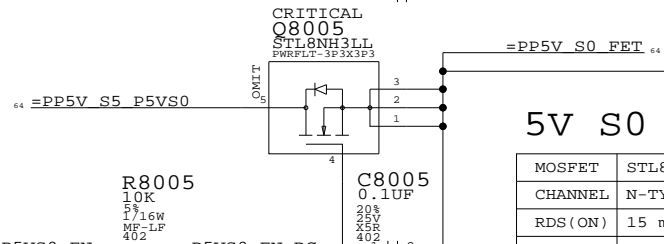
## 1.5V/1.05V S0 RUN/SS CONTROL



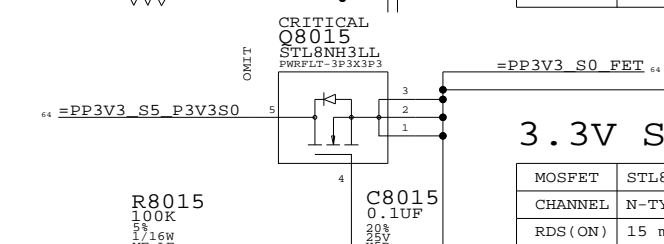
5V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	100 mA



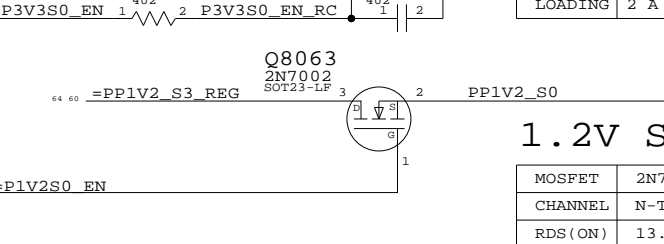
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	1 A



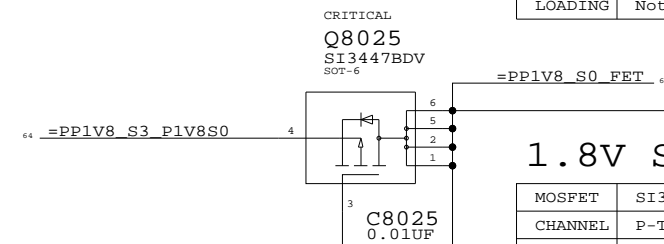
5V S0 FET	
MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	3 A



3.3V S0 FET	
MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	2 A



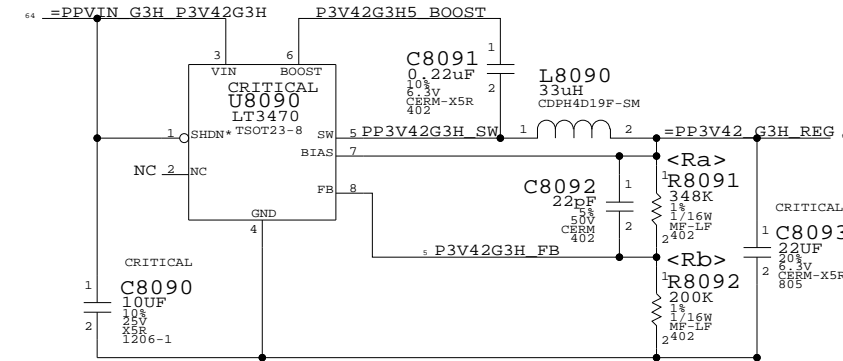
1.2V S0 FET	
MOSFET	2N7002
CHANNEL	N-TYPE
RDS(ON)	13.5 Ohm
LOADING	Nothing



1.8V S0 FET	
MOSFET	SI3447BDV
CHANNEL	P-TYPE
RDS(ON)	72 mOhm @1.8V
LOADING	320 mA

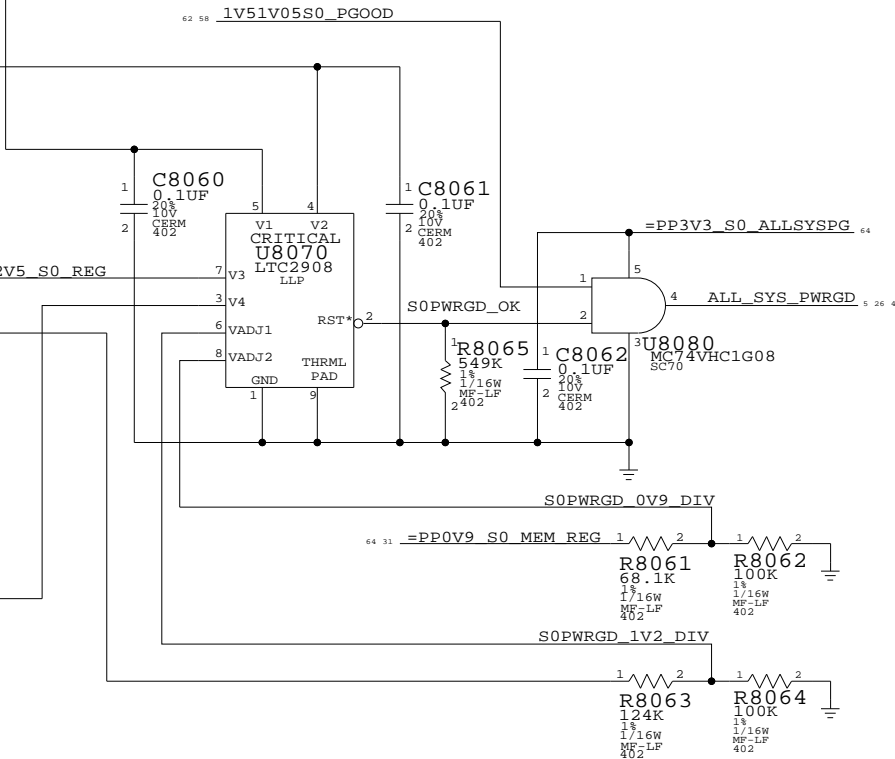
## 3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



$$V_{out} = 1.25V * (1 + R_a / R_b)$$

## ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005,Q8015	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005,Q8015	VISHAY SI7806ADN

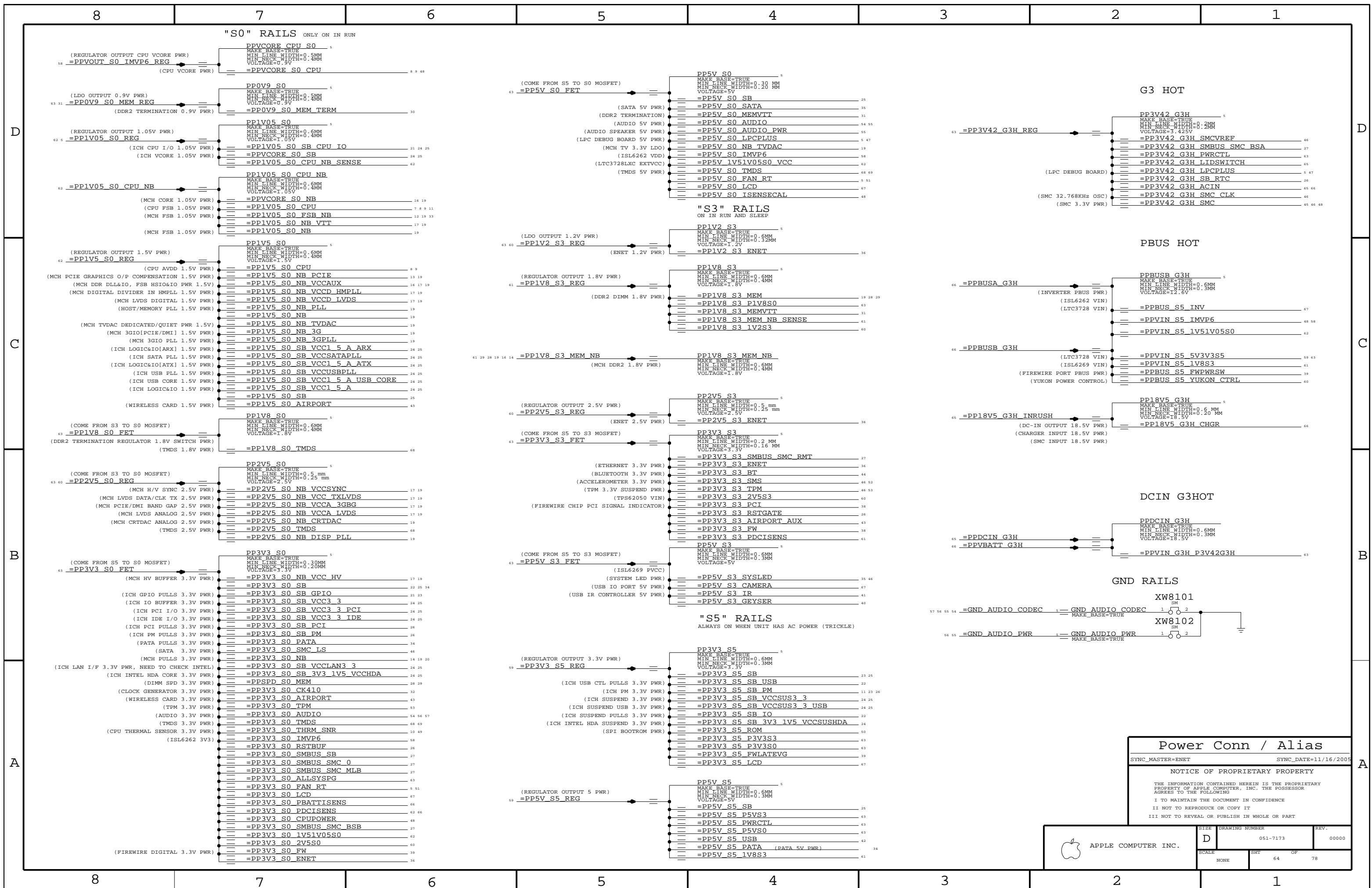
## S3/S0 FETS, G3H SUPPLY

SYNC\_MASTER=ENET SYNC\_DATE=08/30/2005

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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	63		



"S0" RAILS ONLY ON IN RUN

"S3" RAILS ON IN RUN AND SLEEP

"S5" RAILS ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

G3 HOT

PBUS HOT

DCIN G3HOT

GND RAILS

Power Conn / Alias		
SYNC_MASTER=ENET	SYNC_DATE=11/16/2005	
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		

APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	64	78	00000

# DC-JACK INTERFACE

8 7 6 5 4 3 2 1

D

D

C

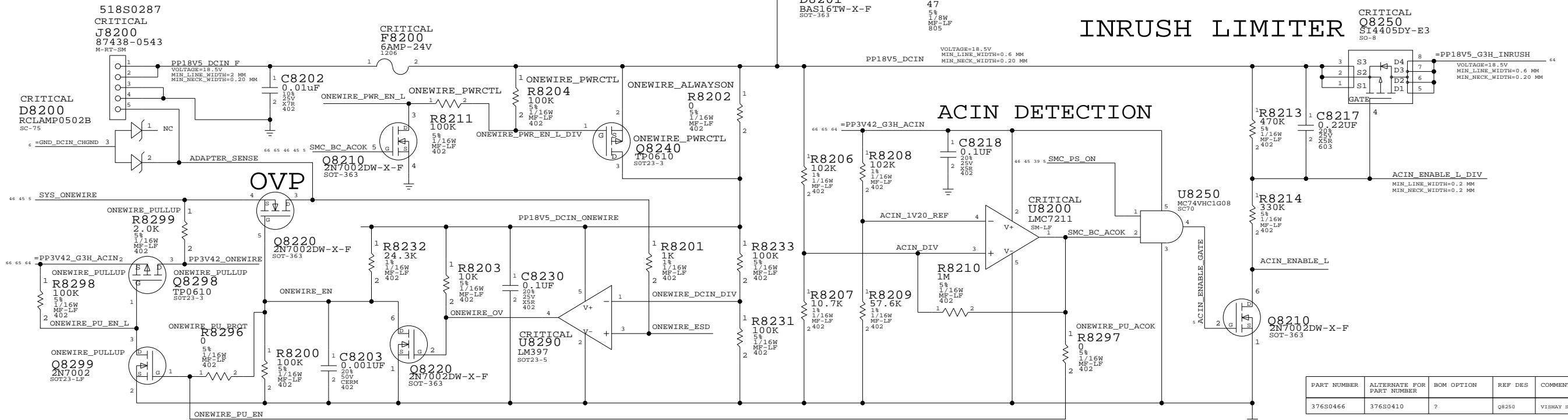
C

B

B

A

A



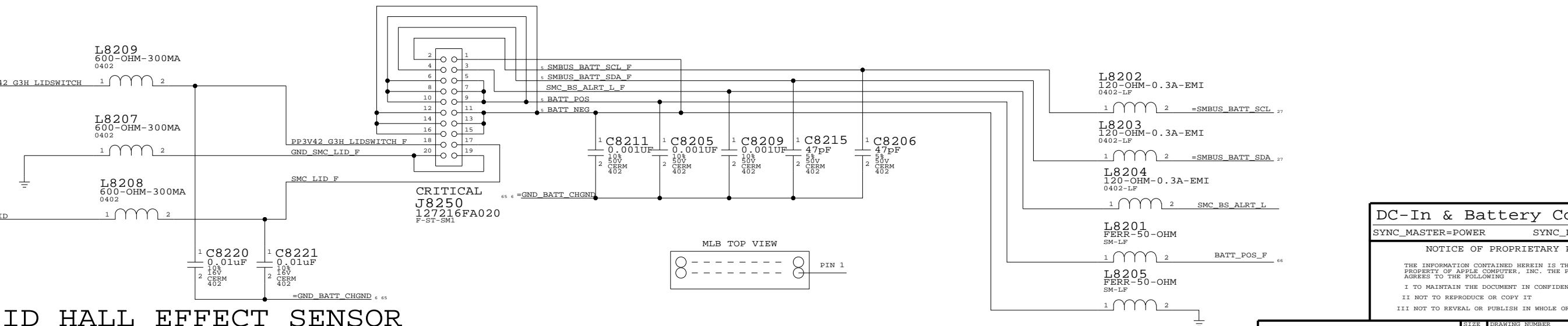
## INRUSH LIMITER

## ACIN DETECTION

## OVP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
376S0466	376S0410	?	Q8250	VISHAY SI4413ADY

# BATTERY INTERFACE



## LID HALL EFFECT SENSOR

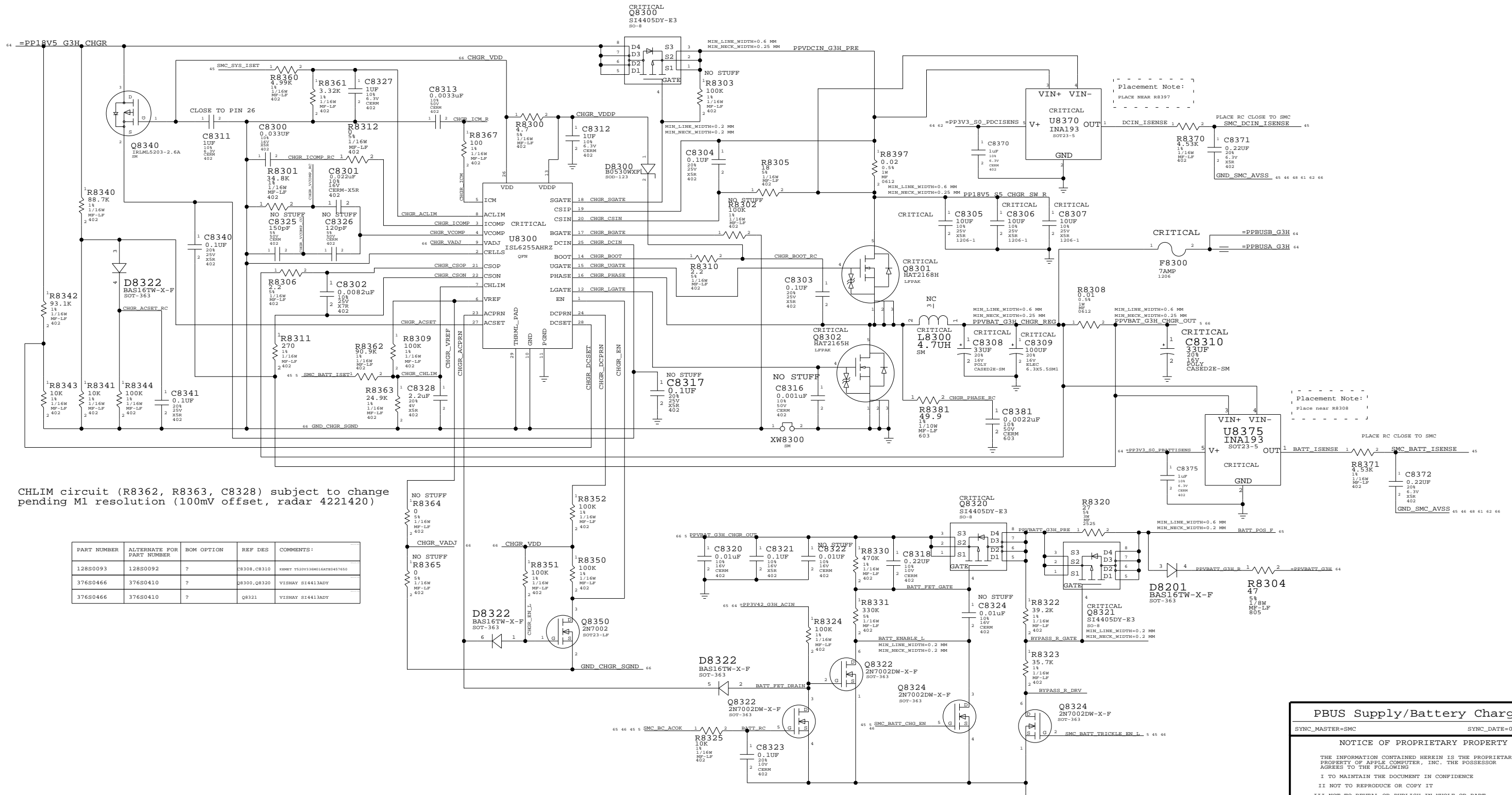
DC-In & Battery Connectors  
 SYNC\_MASTER=POWER SYNC\_DATE=07/13/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	65	78	

8 7 6 5 4 3 2 1

# PBUS SUPPLY / BATTERY CHARGER



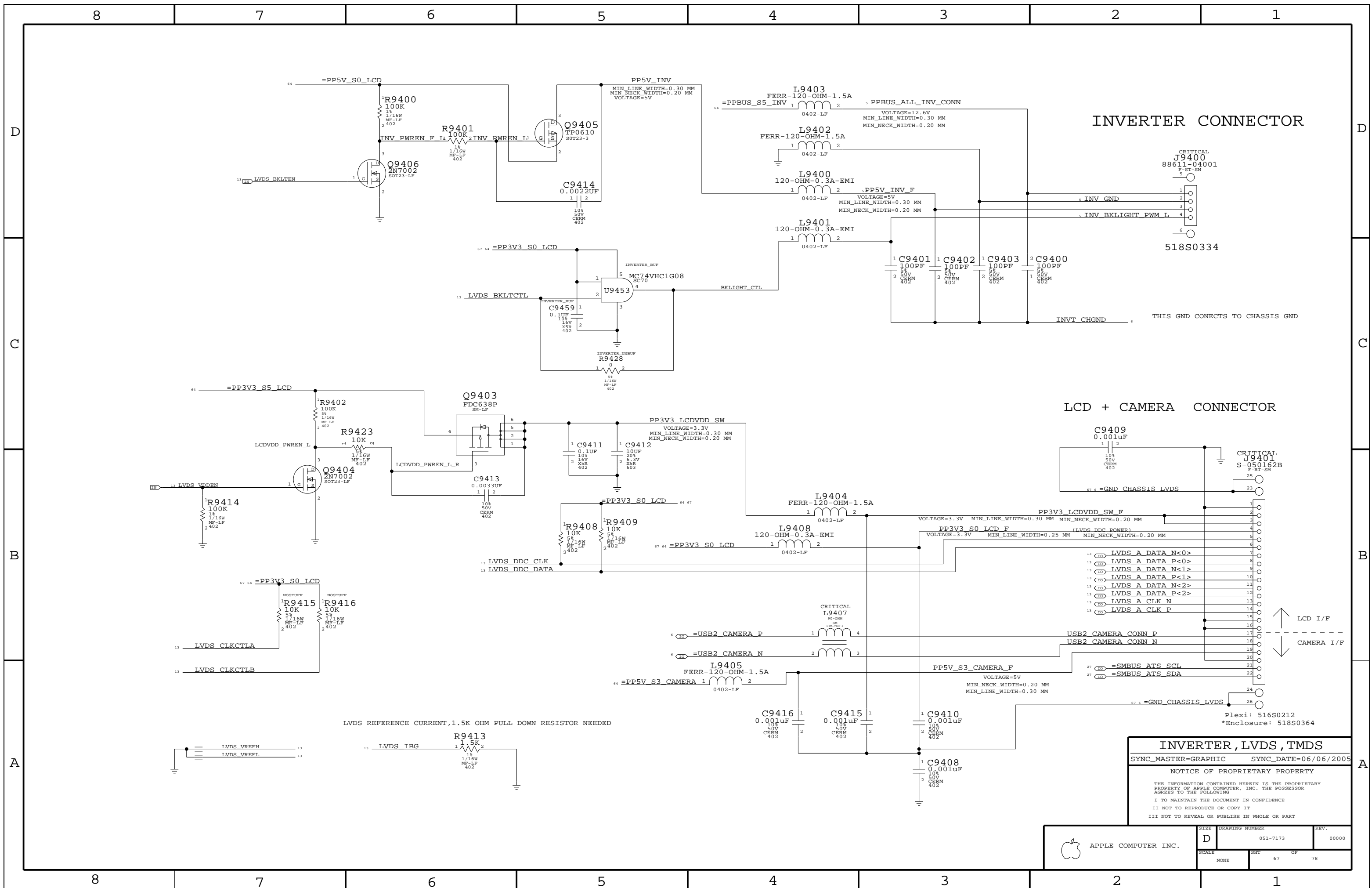
CHLIM circuit (R8362, R8363, C8328) subject to change pending M1 resolution (100mV offset, radar 4221420)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C8308, C8310	KEMET T520V33M018AT040457650
376S0466	376S0410	?	Q8300, Q8320	VISHAY S14413ADY
376S0466	376S0410	?	Q8321	VISHAY S14413ADY

**PBUS Supply/Battery Charger**  
 SYNC\_MASTER=SMC SYNC\_DATE=08/19/2005  
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APPLE COMPUTER INC.	SCALE	SHEET	OF	REV.
	NONE	66	78	00000





INVERTER CONNECTOR

LCD + CAMERA CONNECTOR

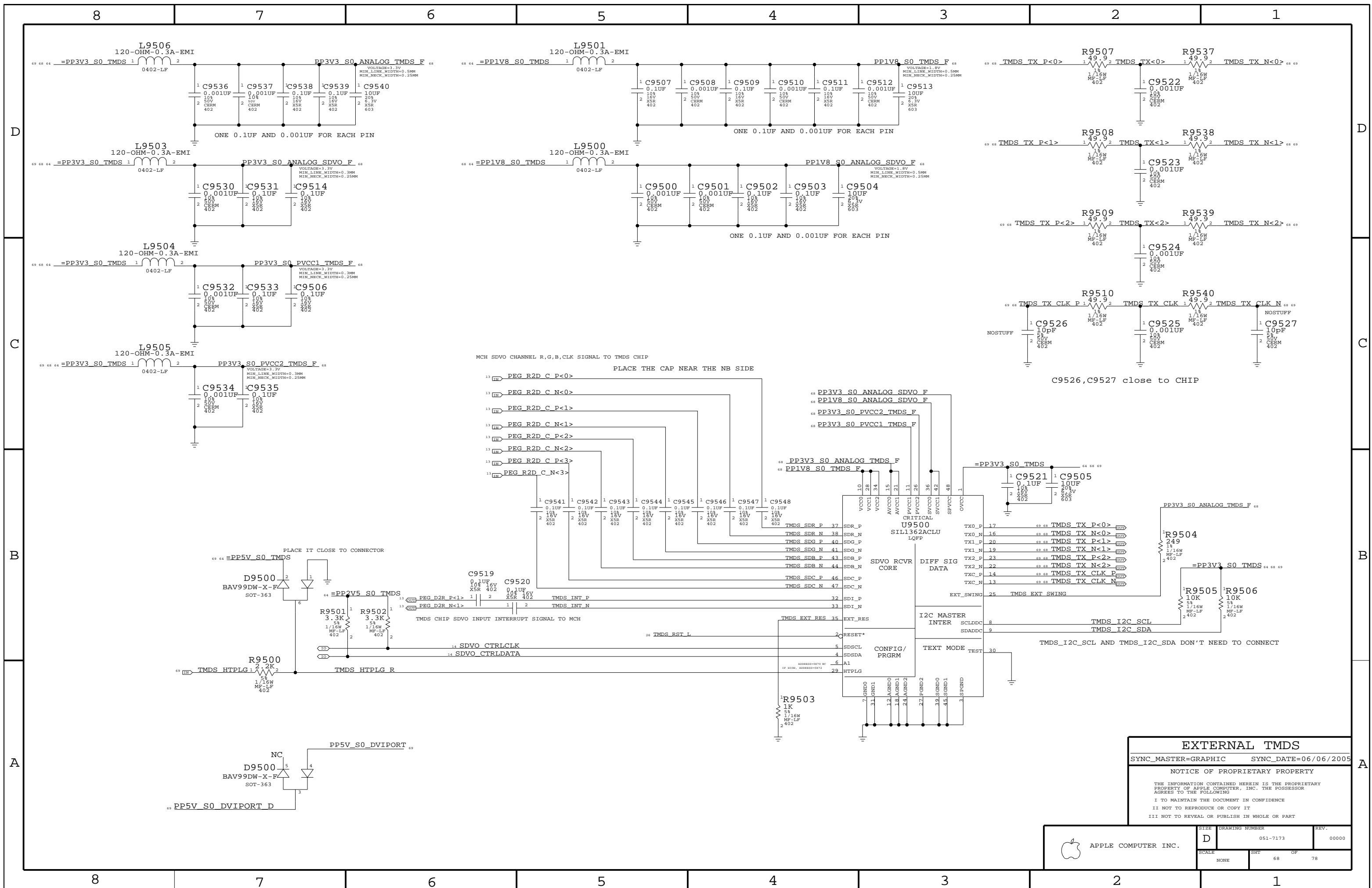
INVERTER, LVDS, TMDs

SYNC\_MASTER=GRAPHIC SYNC\_DATE=06/06/2005

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	NONE	SHT	OF
		67	78



**EXTERNAL TMD5**

SYNC\_MASTER=GRAPHIC    SYNC\_DATE=06/06/2005

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 68	OF 78

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
15580227	15580164	?	REF: 15580164	KEEP MAG LAYER IN BOX

## Video Connectors

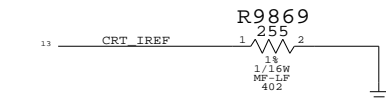
EXTERNAL VIDEO (VGA) INTERFACE

TMDS(MINI DVI) INTERFACE

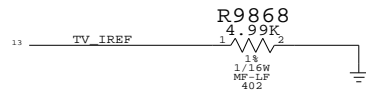
PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

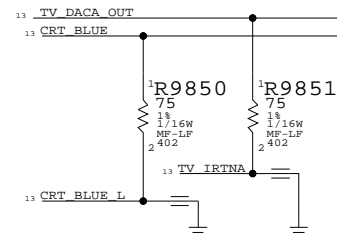
A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT\_IREF AND GROUND



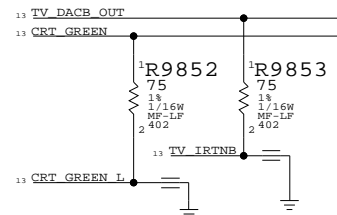
TV REFERENCE CURRENT, USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS



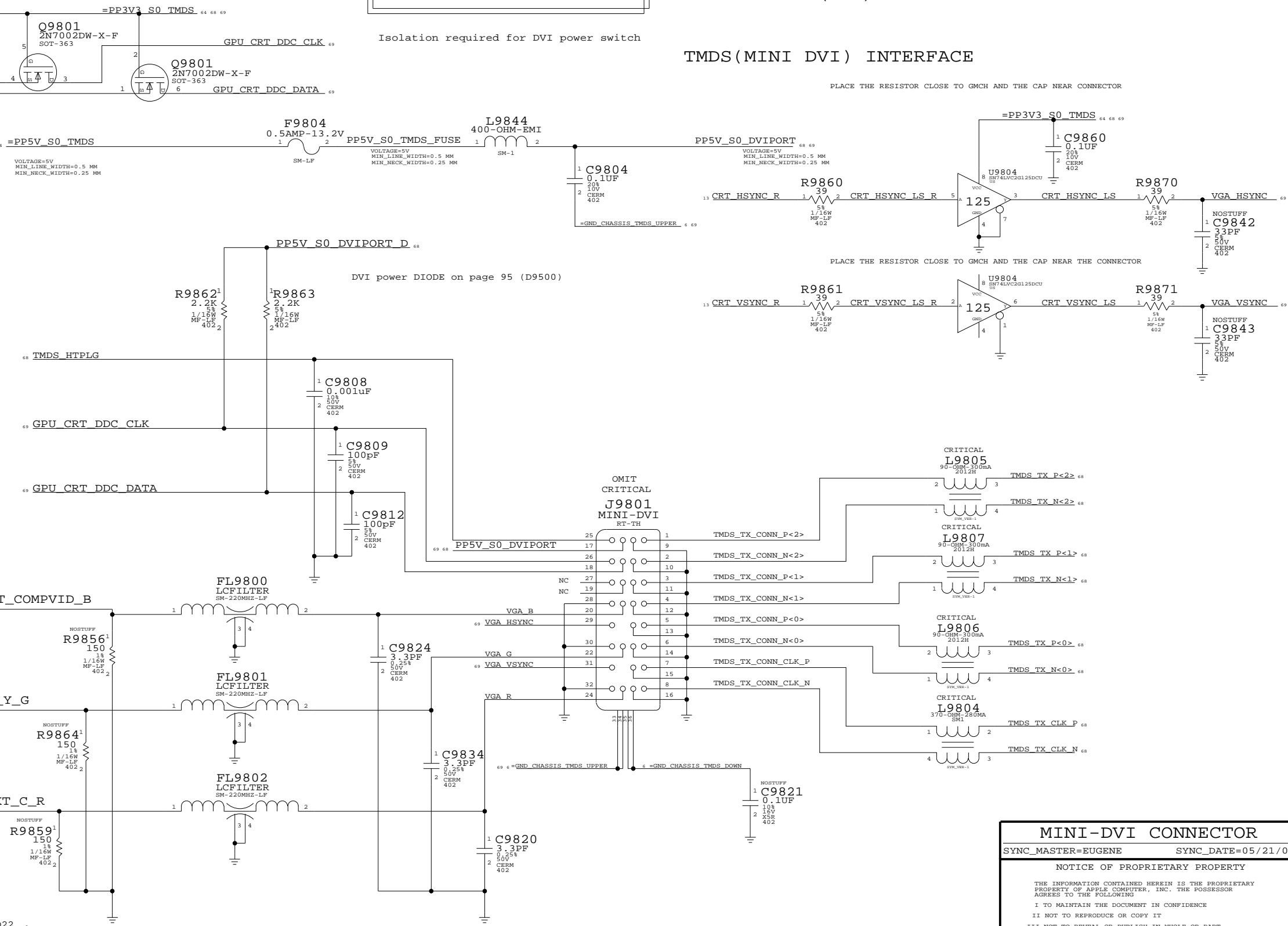
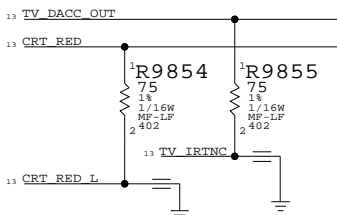
PLACE THE RESISTOR CLOSE TO GMCH



PLACE THE RESISTOR CLOSE TO GMCH



PLACE THE RESISTOR CLOSE TO GMCH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN, 32P MINI-DVI BCDF, RA, MG3, LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN, 32P MINI-DVI BCDF, RA, BLACK, LF	J9801	CRITICAL	FANCY

### MINI-DVI CONNECTOR

SYNC\_MASTER=EUGENE SYNC\_DATE=05/21/05

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	SCALE	SHEET	OF	REV.
	NONE	69	78	00000







Table with columns labeled 8, 7, 6, 5, 4, 3, 2, 1 and rows labeled A, B, C, D. Each cell contains a list of identifiers (e.g., NB\_CFG<10>, PCIE\_F\_R2D\_C\_P) and their corresponding values.



8	7	6	5	4	3	2	1
D							D
C							C
B							B
A							A
8	7	6	5	4	3	2	1



	8	7	6	5	4	3	2	1																																																																																																																																																																																																																																																																																																																																																																																							
D	<table border="1"><tr><td>TP_NR_XOR_LVDS_D27</td><td>TP_NR_XOR_LVDS_D27 - @m42a_lib.M42A</td><td>14C6</td></tr><tr><td>TP_NR_XOR_LVDS_D28</td><td>TP_NR_XOR_LVDS_D28 - @m42a_lib.M42A</td><td>14C6</td></tr><tr><td>TP_PCI_GNT0_L</td><td>TP_PCI_GNT0_L - @m42a_lib.M42A</td><td>22B6</td></tr><tr><td>TP_PCI_GNT1_L</td><td>TP_PCI_GNT1_L - @m42a_lib.M42A</td><td>22B6</td></tr><tr><td>TP_PCI_GNT2_L</td><td>TP_PCI_GNT2_L - @m42a_lib.M42A</td><td>22B6</td></tr><tr><td>TP_PCI_PME_L</td><td>TP_PCI_PME_L - @m42a_lib.M42A</td><td>22A6</td></tr><tr><td>TP_SB_ACZ_SDIN1</td><td>TP_SB_ACZ_SDIN1 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_ACZ_SDIN2</td><td>TP_SB_ACZ_SDIN2 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_DRQ0_L</td><td>TP_SB_DRQ0_L - @m42a_lib.M42A</td><td>21D4</td></tr><tr><td>TP_SB_GPI06</td><td>TP_SB_GPI06 - @m42a_lib.M42A</td><td>23C5</td></tr><tr><td>TP_SB_GPI022</td><td>TP_SB_GPI022 - @m42a_lib.M42A</td><td>6B1 22B6</td></tr><tr><td></td><td>=SB_GPI022 - @m42a_lib.M42A</td><td>6B2 69A6</td></tr><tr><td></td><td>SB_GPI022 - @m42a_lib.M42A</td><td>6B2</td></tr><tr><td></td><td>=SB_GPI022 - @m42a_lib.M42A</td><td>6B2 69A6</td></tr><tr><td>TP_SB_GPI023</td><td>TP_SB_GPI023 - @m42a_lib.M42A</td><td>21D5</td></tr><tr><td>TP_SB_GPI025_DO_NOT_USE</td><td>TP_SB_GPI025_DO_NOT_USE - @m42a_lib.M42A</td><td>23C3</td></tr><tr><td>TP_SB_GPI038</td><td>TP_SB_GPI038 - @m42a_lib.M42A</td><td>23C3</td></tr><tr><td>TP_SB_RCVENIN_L</td><td>TP_SB_RCVENIN_L - @m42a_lib.M42A</td><td>15B2</td></tr><tr><td>TP_SB_RSVD9</td><td>TP_SB_RSVD9 - @m42a_lib.M42A</td><td>22A6</td></tr><tr><td>TP_SB_SATALED_L</td><td>TP_SB_SATALED_L - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_XOR-AD5</td><td>TP_SB_XOR-AD5 - @m42a_lib.M42A</td><td>22A7</td></tr><tr><td>TP_SB_XOR-AD9</td><td>TP_SB_XOR-AD9 - @m42a_lib.M42A</td><td>22A7</td></tr><tr><td>TP_SB_XOR-AE5</td><td>TP_SB_XOR-AE5 - @m42a_lib.M42A</td><td>22A7</td></tr><tr><td>TP_SB_XOR-AG4</td><td>TP_SB_XOR-AG4 - @m42a_lib.M42A</td><td>22A7</td></tr><tr><td>TP_SB_XOR-AH4</td><td>TP_SB_XOR-AH4 - @m42a_lib.M42A</td><td>22A7</td></tr><tr><td>TP_SB_XOR-U3</td><td>TP_SB_XOR-U3 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_XOR-U7</td><td>TP_SB_XOR-U7 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_XOR-V6</td><td>TP_SB_XOR-V6 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_XOR-V7</td><td>TP_SB_XOR-V7 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_XOR-Y1</td><td>TP_SB_XOR-Y1 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_XOR-Y2</td><td>TP_SB_XOR-Y2 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_SB_XOR-AE9</td><td>TP_SB_XOR-AE9 - @m42a_lib.M42A</td><td>22A6</td></tr><tr><td>TP_SB_XOR-AG8</td><td>TP_SB_XOR-AG8 - @m42a_lib.M42A</td><td>22A6</td></tr><tr><td>TP_SB_XOR-AH8</td><td>TP_SB_XOR-AH8 - @m42a_lib.M42A</td><td>22A6</td></tr><tr><td>TP_SB_XOR-W1</td><td>TP_SB_XOR-W1 - @m42a_lib.M42A</td><td>21C6</td></tr><tr><td>TP_USBN_F</td><td>TP_USBN_F - @m42a_lib.M42A</td><td>5C1</td></tr><tr><td>TP_USBP_F</td><td>TP_USBP_F - @m42a_lib.M42A</td><td>5C1</td></tr><tr><td>TV_DACA_OUT</td><td>TV_DACA_OUT - @m42a_lib.M42A</td><td>13C5 69B8</td></tr><tr><td>TV_DACB_OUT</td><td>TV_DACB_OUT - @m42a_lib.M42A</td><td>13C5 69A8</td></tr><tr><td>TV_DACC_OUT</td><td>TV_DACC_OUT - @m42a_lib.M42A</td><td>13C5 69A8</td></tr><tr><td>TV_IREF</td><td>TV_IREF - @m42a_lib.M42A</td><td>13C5 69C8</td></tr><tr><td>USB2_BT_F_N</td><td>USB2_BT_F_N - @m42a_lib.M42A</td><td>44C4</td></tr><tr><td>USB2_BT_F_P</td><td>USB2_BT_F_P - @m42a_lib.M42A</td><td>44B4</td></tr><tr><td>USB2_CAMERA_CONN_N</td><td>USB2_CAMERA_CONN_N - @m42a_lib.M42A</td><td>67A2</td></tr><tr><td>USB2_CAMERA_CONN_P</td><td>USB2_CAMERA_CONN_P - @m42a_lib.M42A</td><td>67B2</td></tr><tr><td>USB2_EXTB_F_N</td><td>USB2_EXTB_F_N - @m42a_lib.M42A</td><td>42C2</td></tr><tr><td>USB2_EXTB_F_P</td><td>USB2_EXTB_F_P - @m42a_lib.M42A</td><td>42C2</td></tr><tr><td>USB2_EXTR_F_N</td><td>USB2_EXTR_F_N - @m42a_lib.M42A</td><td>42B2</td></tr><tr><td>USB2_EXTR_F_P</td><td>USB2_EXTR_F_P - @m42a_lib.M42A</td><td>42B2</td></tr><tr><td>USB2_GND_EXTB_F</td><td>USB2_GND_EXTB_F - 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@m42a_lib.M42A</td><td>6C2 42B5</td></tr><tr><td></td><td>USB2_EXTB_P - @m42a_lib.M42A</td><td>6C2</td></tr><tr><td></td><td>=USB2_EXTB_P - @m42a_lib.M42A</td><td>6C2 42B5</td></tr><tr><td>USB_D_OC_L</td><td>USB_D_OC_L - @m42a_lib.M42A</td><td>22C4 22D8</td></tr><tr><td>USB_E_N</td><td>USB_E_N - @m42a_lib.M42A</td><td>6C1 22C2</td></tr><tr><td></td><td>TP_USBN_E - @m42a_lib.M42A</td><td>5C1 6C2</td></tr><tr><td>USB_E_OC_L</td><td>USB_E_OC_L - @m42a_lib.M42A</td><td>22C4 22D8</td></tr><tr><td>USB_E_P</td><td>USB_E_P - @m42a_lib.M42A</td><td>6C1 22C2</td></tr><tr><td></td><td>TP_USBP_E - @m42a_lib.M42A</td><td>5C1 6C2</td></tr><tr><td>USB_F_N</td><td>USB_F_N - @m42a_lib.M42A</td><td>6C1 22C2</td></tr><tr><td></td><td>=USB2_IR_N - @m42a_lib.M42A</td><td>6C2 41C6</td></tr><tr><td></td><td>USB2_IR_N - @m42a_lib.M42A</td><td>6C2</td></tr><tr><td></td><td>=USB2_IR_N - @m42a_lib.M42A</td><td>6C2 41C6</td></tr><tr><td>USB_F_P</td><td>USB_F_P - @m42a_lib.M42A</td><td>6C1 22C2</td></tr><tr><td></td><td>=USB2_IR_P - @m42a_lib.M42A</td><td>6C2 41C6</td></tr><tr><td></td><td>USB2_IR_P - @m42a_lib.M42A</td><td>6C2</td></tr><tr><td></td><td>=USB2_IR_P - @m42a_lib.M42A</td><td>6C2 41C6</td></tr><tr><td>USB_G_N</td><td>USB_G_N - @m42a_lib.M42A</td><td>6B1 22C2</td></tr><tr><td></td><td>=USB2_BT_N - @m42a_lib.M42A</td><td>6B2 44C6</td></tr><tr><td></td><td>USB2_BT_N - @m42a_lib.M42A</td><td>6B2</td></tr><tr><td></td><td>=USB2_BT_N - @m42a_lib.M42A</td><td>6B2 44C6</td></tr><tr><td>USB_G_P</td><td>USB_G_P - @m42a_lib.M42A</td><td>6B1 22C2</td></tr><tr><td></td><td>=USB2_BT_P - @m42a_lib.M42A</td><td>6C2 44C6</td></tr><tr><td></td><td>USB2_BT_P - @m42a_lib.M42A</td><td>6C2</td></tr><tr><td></td><td>=USB2_BT_P - @m42a_lib.M42A</td><td>6C2 44C6</td></tr><tr><td>USB_RBIA5_PN</td><td>USB_RBIA5_PN - @m42a_lib.M42A</td><td>22C2</td></tr><tr><td>VGA_B</td><td>VGA_B - @m42a_lib.M42A</td><td>69B4</td></tr><tr><td>VGA_G</td><td>VGA_G - @m42a_lib.M42A</td><td>69B4</td></tr><tr><td>VGA_HSYNC</td><td>VGA_HSYNC - @m42a_lib.M42A</td><td>69B4 69C1</td></tr><tr><td>VGA_R</td><td>VGA_R - @m42a_lib.M42A</td><td>69A4</td></tr><tr><td>VGA_VSYNC</td><td>VGA_VSYNC - @m42a_lib.M42A</td><td>69B4 69C1</td></tr><tr><td>VOL_DOWN</td><td>VOL_DOWN - @m42a_lib.M42A</td><td>54B7 54C7</td></tr><tr><td>VOL_UP</td><td>VOL_UP - @m42a_lib.M42A</td><td>54B7 54C7</td></tr><tr><td>VREG_FB</td><td>VREG_FB - @m42a_lib.M42A</td><td>54A4</td></tr><tr><td>VR_PWRGD_CK410</td><td>VR_PWRGD_CK410 - @m42a_lib.M42A</td><td>23C5 26A8</td></tr><tr><td>VR_PWRGOOD_DELAY</td><td>VR_PWRGOOD_DELAY - @m42a_lib.M42A</td><td>14B6 26B5 58C7</td></tr><tr><td>XDP_BPM_L&lt;0&gt;</td><td>XDP_BPM_L&lt;0&gt; - @m42a_lib.M42A</td><td>7C6 11B2</td></tr><tr><td>XDP_BPM_L&lt;1&gt;</td><td>XDP_BPM_L&lt;1&gt; - @m42a_lib.M42A</td><td>7C6 11B2</td></tr><tr><td>XDP_BPM_L&lt;2&gt;</td><td>XDP_BPM_L&lt;2&gt; - @m42a_lib.M42A</td><td>7C6 11B2</td></tr><tr><td>XDP_BPM_L&lt;3&gt;</td><td>XDP_BPM_L&lt;3&gt; - @m42a_lib.M42A</td><td>7C6 11B3</td></tr><tr><td>XDP_BPM_L&lt;4&gt;</td><td>XDP_BPM_L&lt;4&gt; - @m42a_lib.M42A</td><td>7C6 11B2</td></tr><tr><td>XDP_BPM_L&lt;5&gt;</td><td>XDP_BPM_L&lt;5&gt; - @m42a_lib.M42A</td><td>7C6 11B2</td></tr><tr><td>XDP_DBRESET_L</td><td>XDP_DBRESET_L - @m42a_lib.M42A</td><td>7C6 11B4 26C6</td></tr><tr><td>XDP_TCK</td><td>XDP_TCK - @m42a_lib.M42A</td><td>7A8 7C6 11B2 11B3</td></tr><tr><td>XDP_TDI</td><td>XDP_TDI - @m42a_lib.M42A</td><td>7B8 7C6 11B3</td></tr><tr><td>XDP_TDO</td><td>XDP_TDO - @m42a_lib.M42A</td><td>7C6 11B5</td></tr></table>	TP_NR_XOR_LVDS_D27	TP_NR_XOR_LVDS_D27 - @m42a_lib.M42A	14C6	TP_NR_XOR_LVDS_D28	TP_NR_XOR_LVDS_D28 - @m42a_lib.M42A	14C6	TP_PCI_GNT0_L	TP_PCI_GNT0_L - @m42a_lib.M42A	22B6	TP_PCI_GNT1_L	TP_PCI_GNT1_L - @m42a_lib.M42A	22B6	TP_PCI_GNT2_L	TP_PCI_GNT2_L - @m42a_lib.M42A	22B6	TP_PCI_PME_L	TP_PCI_PME_L - @m42a_lib.M42A	22A6	TP_SB_ACZ_SDIN1	TP_SB_ACZ_SDIN1 - @m42a_lib.M42A	21C6	TP_SB_ACZ_SDIN2	TP_SB_ACZ_SDIN2 - @m42a_lib.M42A	21C6	TP_SB_DRQ0_L	TP_SB_DRQ0_L - @m42a_lib.M42A	21D4	TP_SB_GPI06	TP_SB_GPI06 - @m42a_lib.M42A	23C5	TP_SB_GPI022	TP_SB_GPI022 - @m42a_lib.M42A	6B1 22B6		=SB_GPI022 - @m42a_lib.M42A	6B2 69A6		SB_GPI022 - @m42a_lib.M42A	6B2		=SB_GPI022 - @m42a_lib.M42A	6B2 69A6	TP_SB_GPI023	TP_SB_GPI023 - @m42a_lib.M42A	21D5	TP_SB_GPI025_DO_NOT_USE	TP_SB_GPI025_DO_NOT_USE - @m42a_lib.M42A	23C3	TP_SB_GPI038	TP_SB_GPI038 - @m42a_lib.M42A	23C3	TP_SB_RCVENIN_L	TP_SB_RCVENIN_L - @m42a_lib.M42A	15B2	TP_SB_RSVD9	TP_SB_RSVD9 - @m42a_lib.M42A	22A6	TP_SB_SATALED_L	TP_SB_SATALED_L - @m42a_lib.M42A	21C6	TP_SB_XOR-AD5	TP_SB_XOR-AD5 - @m42a_lib.M42A	22A7	TP_SB_XOR-AD9	TP_SB_XOR-AD9 - @m42a_lib.M42A	22A7	TP_SB_XOR-AE5	TP_SB_XOR-AE5 - @m42a_lib.M42A	22A7	TP_SB_XOR-AG4	TP_SB_XOR-AG4 - @m42a_lib.M42A	22A7	TP_SB_XOR-AH4	TP_SB_XOR-AH4 - @m42a_lib.M42A	22A7	TP_SB_XOR-U3	TP_SB_XOR-U3 - @m42a_lib.M42A	21C6	TP_SB_XOR-U7	TP_SB_XOR-U7 - @m42a_lib.M42A	21C6	TP_SB_XOR-V6	TP_SB_XOR-V6 - @m42a_lib.M42A	21C6	TP_SB_XOR-V7	TP_SB_XOR-V7 - @m42a_lib.M42A	21C6	TP_SB_XOR-Y1	TP_SB_XOR-Y1 - @m42a_lib.M42A	21C6	TP_SB_XOR-Y2	TP_SB_XOR-Y2 - @m42a_lib.M42A	21C6	TP_SB_XOR-AE9	TP_SB_XOR-AE9 - @m42a_lib.M42A	22A6	TP_SB_XOR-AG8	TP_SB_XOR-AG8 - @m42a_lib.M42A	22A6	TP_SB_XOR-AH8	TP_SB_XOR-AH8 - @m42a_lib.M42A	22A6	TP_SB_XOR-W1	TP_SB_XOR-W1 - @m42a_lib.M42A	21C6	TP_USBN_F	TP_USBN_F - @m42a_lib.M42A	5C1	TP_USBP_F	TP_USBP_F - @m42a_lib.M42A	5C1	TV_DACA_OUT	TV_DACA_OUT - @m42a_lib.M42A	13C5 69B8	TV_DACB_OUT	TV_DACB_OUT - @m42a_lib.M42A	13C5 69A8	TV_DACC_OUT	TV_DACC_OUT - @m42a_lib.M42A	13C5 69A8	TV_IREF	TV_IREF - @m42a_lib.M42A	13C5 69C8	USB2_BT_F_N	USB2_BT_F_N - @m42a_lib.M42A	44C4	USB2_BT_F_P	USB2_BT_F_P - @m42a_lib.M42A	44B4	USB2_CAMERA_CONN_N	USB2_CAMERA_CONN_N - @m42a_lib.M42A	67A2	USB2_CAMERA_CONN_P	USB2_CAMERA_CONN_P - @m42a_lib.M42A	67B2	USB2_EXTB_F_N	USB2_EXTB_F_N - @m42a_lib.M42A	42C2	USB2_EXTB_F_P	USB2_EXTB_F_P - @m42a_lib.M42A	42C2	USB2_EXTR_F_N	USB2_EXTR_F_N - @m42a_lib.M42A	42B2	USB2_EXTR_F_P	USB2_EXTR_F_P - @m42a_lib.M42A	42B2	USB2_GND_EXTB_F	USB2_GND_EXTB_F - @m42a_lib.M42A	42C2	USB2_GND_EXTR_F	USB2_GND_EXTR_F - @m42a_lib.M42A	42B2	USB_A_N	USB_A_N - @m42a_lib.M42A	6C1 22C2		=USB2_EXTB_N - @m42a_lib.M42A	6C2 42C5		USB2_EXTB_N - @m42a_lib.M42A	6C2		=USB2_EXTB_N - @m42a_lib.M42A	6C2 42C5	USB_A_OC_L	USB_A_OC_L - @m42a_lib.M42A	6C1 22C4 22D8		=EXTAUSB_OC_L - @m42a_lib.M42A	6C2 42C8		EXTAUSB_OC_L - @m42a_lib.M42A	6C2		=EXTAUSB_OC_L - @m42a_lib.M42A	6C2 42C8	USB_A_P	USB_A_P - @m42a_lib.M42A	6C1 22C2		=USB2_EXTB_P - @m42a_lib.M42A	6C2 42C5		USB2_EXTB_P - @m42a_lib.M42A	6C2		=USB2_EXTB_P - @m42a_lib.M42A	6C2 42C5	USB_B_N	USB_B_N - @m42a_lib.M42A	6C1 22C2		=USB2_GEYSER_N - @m42a_lib.M42A	6C2 40C7		USB2_GEYSER_N - @m42a_lib.M42A	6C2		=USB2_GEYSER_N - @m42a_lib.M42A	6C2 40C7	USB_B_OC_L	USB_B_OC_L - @m42a_lib.M42A	22C4 22D8	USB_B_P	USB_B_P - @m42a_lib.M42A	6C1 22C2		=USB2_GEYSER_P - @m42a_lib.M42A	6C2 40C7		USB2_GEYSER_P - @m42a_lib.M42A	6C2		=USB2_GEYSER_P - @m42a_lib.M42A	6C2 40C7	USB_C_N	USB_C_N - @m42a_lib.M42A	6C1 22C2		=USB2_EXTB_N - @m42a_lib.M42A	6C2 42B5		USB2_EXTB_N - @m42a_lib.M42A	6C2		=USB2_EXTB_N - @m42a_lib.M42A	6C2 42B5	USB_C_P	USB_C_P - @m42a_lib.M42A	6C1 22C2		=USB2_EXTB_P - @m42a_lib.M42A	6C2 42B5		USB2_EXTB_P - @m42a_lib.M42A	6C2		=USB2_EXTB_P - @m42a_lib.M42A	6C2 42B5	USB_D_OC_L	USB_D_OC_L - @m42a_lib.M42A	22C4 22D8	USB_E_N	USB_E_N - @m42a_lib.M42A	6C1 22C2		TP_USBN_E - @m42a_lib.M42A	5C1 6C2	USB_E_OC_L	USB_E_OC_L - @m42a_lib.M42A	22C4 22D8	USB_E_P	USB_E_P - @m42a_lib.M42A	6C1 22C2		TP_USBP_E - @m42a_lib.M42A	5C1 6C2	USB_F_N	USB_F_N - @m42a_lib.M42A	6C1 22C2		=USB2_IR_N - @m42a_lib.M42A	6C2 41C6		USB2_IR_N - @m42a_lib.M42A	6C2		=USB2_IR_N - @m42a_lib.M42A	6C2 41C6	USB_F_P	USB_F_P - @m42a_lib.M42A	6C1 22C2		=USB2_IR_P - @m42a_lib.M42A	6C2 41C6		USB2_IR_P - @m42a_lib.M42A	6C2		=USB2_IR_P - @m42a_lib.M42A	6C2 41C6	USB_G_N	USB_G_N - @m42a_lib.M42A	6B1 22C2		=USB2_BT_N - @m42a_lib.M42A	6B2 44C6		USB2_BT_N - @m42a_lib.M42A	6B2		=USB2_BT_N - @m42a_lib.M42A	6B2 44C6	USB_G_P	USB_G_P - @m42a_lib.M42A	6B1 22C2		=USB2_BT_P - @m42a_lib.M42A	6C2 44C6		USB2_BT_P - @m42a_lib.M42A	6C2		=USB2_BT_P - @m42a_lib.M42A	6C2 44C6	USB_RBIA5_PN	USB_RBIA5_PN - @m42a_lib.M42A	22C2	VGA_B	VGA_B - @m42a_lib.M42A	69B4	VGA_G	VGA_G - @m42a_lib.M42A	69B4	VGA_HSYNC	VGA_HSYNC - @m42a_lib.M42A	69B4 69C1	VGA_R	VGA_R - @m42a_lib.M42A	69A4	VGA_VSYNC	VGA_VSYNC - @m42a_lib.M42A	69B4 69C1	VOL_DOWN	VOL_DOWN - @m42a_lib.M42A	54B7 54C7	VOL_UP	VOL_UP - @m42a_lib.M42A	54B7 54C7	VREG_FB	VREG_FB - @m42a_lib.M42A	54A4	VR_PWRGD_CK410	VR_PWRGD_CK410 - @m42a_lib.M42A	23C5 26A8	VR_PWRGOOD_DELAY	VR_PWRGOOD_DELAY - @m42a_lib.M42A	14B6 26B5 58C7	XDP_BPM_L<0>	XDP_BPM_L<0> - @m42a_lib.M42A	7C6 11B2	XDP_BPM_L<1>	XDP_BPM_L<1> - @m42a_lib.M42A	7C6 11B2	XDP_BPM_L<2>	XDP_BPM_L<2> - @m42a_lib.M42A	7C6 11B2	XDP_BPM_L<3>	XDP_BPM_L<3> - @m42a_lib.M42A	7C6 11B3	XDP_BPM_L<4>	XDP_BPM_L<4> - @m42a_lib.M42A	7C6 11B2	XDP_BPM_L<5>	XDP_BPM_L<5> - @m42a_lib.M42A	7C6 11B2	XDP_DBRESET_L	XDP_DBRESET_L - @m42a_lib.M42A	7C6 11B4 26C6	XDP_TCK	XDP_TCK - @m42a_lib.M42A	7A8 7C6 11B2 11B3	XDP_TDI	XDP_TDI - @m42a_lib.M42A	7B8 7C6 11B3	XDP_TDO	XDP_TDO - @m42a_lib.M42A	7C6 11B5	<table border="1"><tr><td>XDP_TMS</td><td>XDP_TMS - @m42a_lib.M42A</td><td>7B8 7C6 11B2</td></tr><tr><td>XDP_TRST_L</td><td>XDP_TRST_L - @m42a_lib.M42A</td><td>7C6 11B3</td></tr></table>	XDP_TMS	XDP_TMS - @m42a_lib.M42A	7B8 7C6 11B2	XDP_TRST_L	XDP_TRST_L - @m42a_lib.M42A	7C6 11B3						
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