

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
07		355269	ENGINEERING RELEASED		
				DATE	DATE
				12/10/04	?

M42 / M42A MLB-GM-CS

10/16/2006 PVT

M42 EE DRIS:

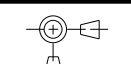
RX-RAYMOND XU
 DK-DINESH KUMAR
 RC-RAY CHANG
 MK-MARC KLINGELHOFER
 LT-LAWRENCE TAN
 ES-ERIC SMITH
 LD-LINDA DUNN

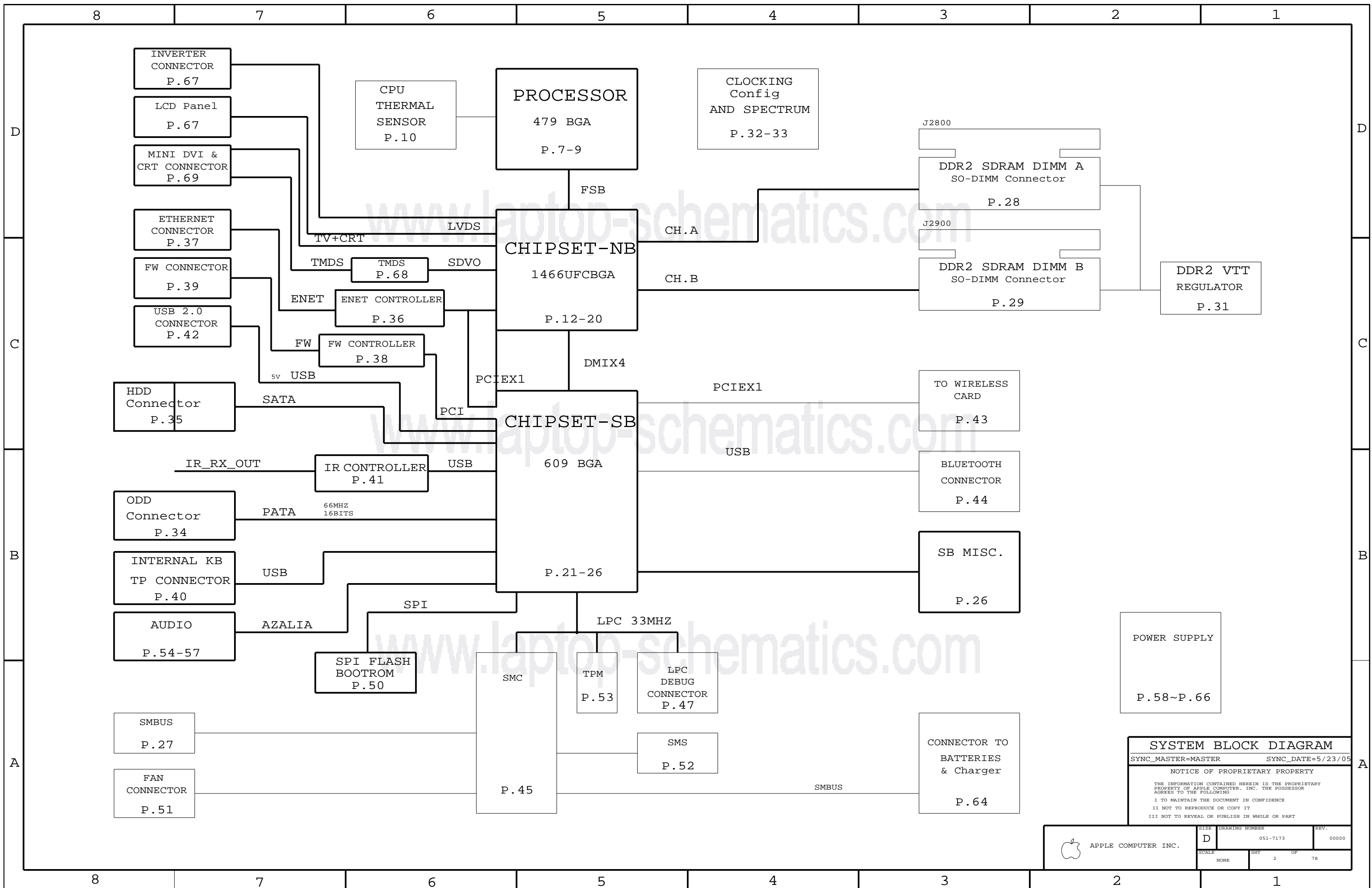
Page	(.csa)	Contents	M42-DRI	Sync	Date
1	1	Table of Contents	RX	N/A	N/A
2	2	SYSTEM BLOCK DIAGRAM	RX	MASTER	5/23/05
3	3	Power Block Diagram	MK	POWER	06/30/2005
4	4	CONFIGURATION OPTIONS	RX	SMC	07/18/2005
5	5	FUNC TEST 1 OF 2	RX	TP	07/25/2005
6	6	SIGNAL ALIAS /RESET	RX	ENET	08/19/2005
7	7	CPU 1 OF 2-FSB	RX	MASTER	05/03/2005
8	8	CPU 2 OF 2-PWR/GND	MK	MASTER	05/03/2005
9	9	CPU DECAPS & VID<>	MK	SMC	08/19/2005
10	10	CPU MISC1-TEMP SENSOR	ES	ENET	08/19/2005
11	11	CPU ITP700FLEX DEBUG	RX	MASTER	5/23/05
12	12	NB CPU Interface	MK	NB	07/25/2005
13	13	NB PEG / Video Interfaces	DK	NB	07/25/2005
14	14	NB Misc Interfaces	RX	NB	08/15/2005
15	15	NB DDR2 Interfaces	LT	NB	07/25/2005
16	16	NB Power 1	DK	NB	07/25/2005
17	17	NB Power 2	DK	NB	07/25/2005
18	18	NB Grounds	DK	NB	07/25/2005
19	19	NB (GM) Decoupling	DK	NB	06/22/2005
20	20	NB Config Straps	DK	NB	06/28/2005
21	21		RX	SB	08/05/2005
22	22		RX	ENET	11/16/2005
23	23		RX	ENET	11/28/2005
24	24		RX	SB	08/05/2005
25	25		RX	SB	06/28/2005
26	26	SB Misc	RX	NB	07/26/2005
27	27	M42 SMBUS CONNECTIONS	ES	ENET	08/30/2005
28	28	DDR2 SO-DIMM Connector A	LT	MEMORY	06/20/2005
29	29	DDR2 SO-DIMM Connector B	LT	MEMORY	06/20/2005
30	30	Memory Active Termination	LT	MEMORY	06/20/2005
31	31	Memory Vtt Supply	LT	(MASTER)	(MASTER)
32	32	CLOCKS	DK	CLOCK	06/03/2005
33	33	CLOCK TERMINATION	DK	CLOCK	06/06/2005
34	34	PATA CONNECTOR	ES	ENET	11/01/2005
35	35	SATA CONNECTOR	ES	ENET	11/14/2005
36	36	ETHERNET CONTROLLER	ES	ENET	12/06/2005
37	37	ETHERNET CONNECTOR	ES	ENET	11/14/2005
38	38	FIREWIRE CONTROLLER	ES	ENET	08/30/2005
39	39	FIREWIRE PORT	ES	ENET	11/16/2005
40	40	CONNECTOR MISC	ES	ENET	11/16/2005
41	41	IR CONTROLLER	ES	ENET	11/09/2005
42	42		ES	ENET	11/01/2005
43	43		ES	ENET	08/19/2005
44	44	BLUETOOTH INTERFACE	MK	ENET	08/29/2005
45	45	SMC	MK	ENET	08/18/2005
46	46	SMC SUPPORT	LD	SMC	08/23/2005
47	47	LPC+ Debug Connector	MK	NB	06/30/2005
48	48	CPU Current & Voltage Sense	ES	ENET	08/30/2005

Page	(.csa)	Contents	M42-DRI	Sync	Date
49	49	TEMPERATURE SENSE	RX	ENET	11/09/2005
50	50	SPI BOOTROM	ES	MASTER	5/23/05
51	51	Fan	MK	ENET	11/10/2005
52	52	SMS	RX	SMC	08/23/2005
53	53	TPM	DK	SMC	07/18/2005
54	54	AUDIO: CODEC	DK	M42AUDIO	08/05/2006
55	55	AUDIO: SPEAKER AMP	DK	M42AUDIO	08/05/2006
56	56	AUDIO: JACK	DK	M42AUDIO	08/05/2006
57	57	AUDIO: JACK TRANSLATORS	MK	M42AUDIO	08/05/2006
58	58	IMVP6 CPU VCore Regulator	MK	POWER	07/13/2005
59	59	5V / 3.3V Power Supply	MK	POWER	07/13/2005
60	60	2.5V/1.2V Regulator	MK	ENET	12/06/2005
61	61	1.8V Supply	MK	POWER	07/13/2005
62	62	1.5V / 1.05V Power Supply	MK	POWER	07/13/2005
63	63	S3/S0 FETS, G3H SUPPLY	MK	ENET	08/30/2005
64	64	Power Conn / Alias	MK	ENET	11/16/2005
65	65	DC-In & Battery Connectors	MK	POWER	07/13/2005
66	66	PBUS Supply/Battery Charger	ES	SMC	08/19/2005
67	67	INVERTER, LVDS, TMDS	DK	GRAPHIC	06/06/2005
68	68	EXTERNAL TMDS	DK	GRAPHIC	06/06/2005
69	69	MINI-DVI CONNECTOR		EUGENE	05/21/05
70	70	Cross Reference Page			
71	71	Cross Reference Page			
72	72	Cross Reference Page			
73	73	Cross Reference Page			
74	74	Cross Reference Page			
75	75	Cross Reference Page			
76	76	Cross Reference Page			
77	77	Cross Reference Page			
78	78	Cross Reference Page			

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7173	1	SCHEM, M42, MLB	SCH	
820-1889	1	PCBF, M42, MLB	PCB	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.																
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X.XX :	_____	<table border="1"> <tr><td>WRAPPER</td><td>/</td><td>DESIGN CR</td><td>/</td></tr> <tr><td>ENG APPD</td><td>/</td><td>MFG APPD</td><td>/</td></tr> <tr><td>QA APPD</td><td>/</td><td>DESIGNER</td><td>/</td></tr> <tr><td>RELEASE</td><td>/</td><td>SCALE</td><td>/</td></tr> </table>	WRAPPER			/	DESIGN CR	/	ENG APPD	/	MFG APPD	/	QA APPD	/	DESIGNER	/	RELEASE	/	SCALE	/
WRAPPER	/	DESIGN CR	/																	
ENG APPD	/	MFG APPD	/																	
QA APPD	/	DESIGNER	/																	
RELEASE	/	SCALE	/																	
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ANGLES :	_____																			
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 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		DRAWING NUMBER 051-7173 REV. 00000																
		SIZE D		SHT 1 OF 78																



SYSTEM BLOCK DIAGRAM
 SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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	D	051-7173	00000
SCALE	NONE	SHT	2 OF 78

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOM OPTION

BOMOPTION	M42A GOOD ST MICRO 630-7795 EVT	M42A BETTER ST MICRO 630-7796 EVT	M42A BEST KIONIX 630-7799 EVT	M42A GOOD KIONIX 630-7798 EVT	M42A BETTER KIONIX 630-7736 EVT	M42A BEST ST MICRO 630-7797 EVT
1V51V05S0_CONT						
1V51V05S0_SKIP	v	v	v	v	v	v
5V3V3S3_CONT						
5V3V3S3_SKIP	v	v	v	v	v	v
ACCEL_KIONIX			v	v	v	
ACCEL_ST	v	v				v
INVERTER_BUF	v	v	v	v	v	v
INVERTER_UNBUF						
ITP						
LEMENU	v	v	v	v	v	v
MEMVIT_EN_PU	v	v	v	v	v	v
NBCFG_DMI_REVERSE						
NBCFG_DMI_X2						
NBCFG_DYN_ODT_DISABLE						
NBCFG_PEG_REVERSE						
NBCFG_SDVO_AND_PCIE						
NBCFG_VCC_1V5						
NO_REBOOT_MODE						
USB_C_OC_PU	v	v	v	v	v	v
USB_D_OC_PU	v	v	v	v	v	v
USB_E_OC_PU	v	v	v	v	v	v
GOOD	v			v		
BETTER		v			v	
BEST			v			v
M42A_PGM	v	v	v	v	v	v
ONEWIRE_PULLUP	v	v	v	v	v	v
ONEWIRE_PULLUP_OLD						
ONEWIRE_PU_PROT	v	v	v	v	v	v
ONEWIRE_PU_ACOK						
ONEWIRE_PWRCTL	v	v	v	v	v	v
ONEWIRE_ALWAYSON						
3V3_IND_2MM8	v	v	v	v	v	v
3V3_IND_3MM						
NORMAL	v	v		v	v	
FANCY			v			v
STANDOFF	v	v	v	v	v	v
FET_FDN6296	v	v	v	v	v	v
FET_STL8NH3LL						
GOOD-ST	v					
BETTER-ST		v				
BEST-KIONIX			v			
GOOD-KIONIX				v		
BETTER-KIONIX					v	
BEST-ST						v
TPM						
PVT-DIMM						
POST-RAMP-DIMM35	v	v	v	v	v	v
M42						
M42A	v	v	v	v	v	v

BOARD STACK-UP AND CONSTRUCTION

Top	SIGNAL
2	GROUND
3	SIGNAL(High Speed)
4	SIGNAL(High Speed)
5	GROUND
6	POWER
7	POWER
8	GROUND
9	SIGNAL(High Speed)
10	SIGNAL(High Speed)
11	GROUND
BOTTOM	SIGNAL

MLB STACKUP		
LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT		
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT		
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3387	1	IC, MEMOM, CPU B2 DC 1.83GHZ, 479 PGA	U0700	GOOD
337S3389	1	IC, MEMOM, CPU B2 DC 2.0GHZ, 479 PGA	U0700	BETTER
337S3389	1	IC, MEMOM, CPU B2 DC 2.0GHZ, 479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC, FW32306, 1394A LIM, BGA, 129P	U4400	LEMENU
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	LEMENU
359S0109	1	IC, SLOBLP436, CLOCK GEN, 68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1941	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, 8028	U6301	M42A_PGM
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, 808	U4102	M42A_PGM
341S1946	1	IC, SMC, 176P BGA, MS8/2116	U5800	M42A_PGM
341S1890	1	IC, PSOC-W/USB, 56P, MFP, CY8C24794	U5100	M42A_PGM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WES	CRITICAL	GOOD-ST
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WET	CRITICAL	BETTER-ST
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEW	CRITICAL	BEST-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEV	CRITICAL	GOOD-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:W6V	CRITICAL	BETTER-KIONIX
826-4393	1	LBL, P/N LABEL, PCB, 28MMX6MM	EEE:WEU	CRITICAL	BEST-ST

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

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	D	051-7173	00000
	SCALE	SHT	OF
	NONE	4	78

Functional Test Points

Power Supply NO_TESTs

NO_TEST	Value	Page
IMVP6_RBIAS	TRUE	58
IMVP6_COMP	TRUE	58
5VS5_RUNSS	TRUE	59 63
1V5S0_RUNSS	TRUE	59 63
1V8S3_COMP	TRUE	61
1V8S3_FSET	TRUE	61
3V3S5_COMP	TRUE	
3V3S5_FSET	TRUE	
1V05S0_COMP	TRUE	
1V05S0_FSET	TRUE	
P3V42G3H_FB	TRUE	63

CLOCK NO_TESTs

NO_TEST	Value	Page
CK410_CPU0_N	TRUE	32 33
CK410_CPU0_P	TRUE	32 33
CK410_CPU1_N	TRUE	32 33
CK410_CPU1_P	TRUE	32 33
CK410_CPU2_ITP_SRC10_N	TRUE	32 33
CK410_CPU2_ITP_SRC10_P	TRUE	32 33
CK410_DOT96_27M_N	TRUE	32 33
CK410_DOT96_27M_P	TRUE	32 33
CK410_LVDS_N	TRUE	32 33
CK410_LVDS_P	TRUE	32 33
CK410_PCI4_CLK_SPN	TRUE	
CK410_PCF1_CLK	TRUE	32 33
CK410_SRC1_N_SPN	TRUE	6
CK410_SRC1_P_SPN	TRUE	6
CK410_SRC2_N	TRUE	32 33
CK410_SRC2_P	TRUE	32 33
CK410_SRC3_N_SPN	TRUE	6
CK410_SRC3_P_SPN	TRUE	6
CK410_SRC4_N	TRUE	32 33
CK410_SRC4_P	TRUE	32 33
CK410_SRC5_N	TRUE	32 33
CK410_SRC5_P	TRUE	32 33
CK410_SRC6_N	TRUE	32 33
CK410_SRC6_P	TRUE	32 33
CK410_SRC7_N_SPN	TRUE	6
CK410_SRC7_P_SPN	TRUE	6
CK410_SRC8_N	TRUE	32 33
CK410_SRC8_P	TRUE	32 33
CK410_SRC_CLKRE01_L_SPN	TRUE	6
CK410_SRC_CLKRE03_L_SPN	TRUE	6
CK410_SRC_CLKRE08_L	TRUE	32 33

FIREWARE NO_TESTs

NO_TEST	Value	Page
FW_B_TPA_N_SPN	TRUE	6
FW_B_TPA_P_SPN	TRUE	6
FW_B_TPBIAS_SPN	TRUE	6
FW_B_TPB_N_SPN	TRUE	6
FW_B_TPB_P_SPN	TRUE	6
FW_C_TPA_N_SPN	TRUE	6
FW_C_TPA_P_SPN	TRUE	6
FW_C_TPBIAS_SPN	TRUE	6
FW_C_TPB_N_SPN	TRUE	6
FW_C_TPB_P_SPN	TRUE	6

LVDS NO_TESTs

NO_TEST	Value	Page
LVDS_B_CLK_N_SPN	TRUE	6
LVDS_B_CLK_P_SPN	TRUE	6
LVDS_B_DATA_N0_SPN	TRUE	6
LVDS_B_DATA_N1_SPN	TRUE	6
LVDS_B_DATA_N2_SPN	TRUE	6
LVDS_B_DATA_P1_SPN	TRUE	6
LVDS_B_DATA_P2_SPN	TRUE	6

ETHERNET NO_TESTs

NO_TEST	Value	Page
ENET_MDI_TRAN_P<2>	TRUE	37
ENET_MDI_TRAN_N<2>	TRUE	37
ENET_MDI_TRAN_P<3>	TRUE	37

NO_TEST	Value	Page
SMC_FAN_3_TACH	TRUE	45 46
ALS_LEFT	TRUE	45 46

Fan Connectors

FUNC_TEST	Value	Page
=PP5V_S0_FAN_RT	TRUE	51 64
FAN_RT_PWM	TRUE	51
FAN_RT_TACH	TRUE	51
=PP3V3_S0_FAN_RT	TRUE	51 64
SMC_FAN_1_CTL	TRUE	45 51
SMC_FAN_1_TACH	TRUE	45 51

LPC+ Debug Connector

FUNC_TEST	Value	Page
=PP3V42_G3H_LPCPLUS	TRUE	47 64
=PP5V_S0_LPCPLUS	TRUE	47 64
LPC_AD<0>	TRUE	21 45 47 53
LPC_AD<1>	TRUE	21 45 47 53
LPC_FRAME_L	TRUE	21 45 47 53
PM_CLKRUN_L	TRUE	23 38 45 47 53
BOOT_LPC_SPI_L	TRUE	22 45 47
SMC_TMS	TRUE	45 46 47
DEBUG_RST_L	TRUE	26 47
SMC_TRST_L	TRUE	45 47
SMC_TDO	TRUE	45 46 47
SMC_MD1	TRUE	45 47
SMC_TX_L	TRUE	45 46 47
FWH_INIT_L	TRUE	5 21 47
PCI_CLK_PORT80_LPC	TRUE	33 47
LPC_AD<2>	TRUE	21 45 47 53
LPC_AD<3>	TRUE	21 45 47 53
INT_SERIRO	TRUE	23 45 47 53
PM_SUS_STAT_L	TRUE	23 45 46 47 53
SMC_TDI	TRUE	45 46 47
SMC_TCK	TRUE	45 46 47
SMC_RST_L	TRUE	45 46 47
SMC_NMI	TRUE	45 47
SMC_RX_L	TRUE	45 46 47
SV_SET_UP	TRUE	23 47

Other Func Test Points

FUNC_TEST	Value	Page
=PP1V05_S0_REG	TRUE	52 64
SMBus_FUNC_TEST	TRUE	
SMBUS_SMC_MLB_SCL	TRUE	27
SMBUS_SMC_MLB_SDA	TRUE	27
FIREWIRE_FUNC_TEST	TRUE	
PPFW_SWITCH	TRUE	39
SLEEP_LED_FUNC_TEST	TRUE	
SYS_LED_ANODE	TRUE	35 46
SMC_FUNC_TEST	TRUE	
SMC_LID	TRUE	40 45 46 65
SMC_MANUAL_RST_L	TRUE	46
SMC_CPU_VSENSE	TRUE	45 48
Power Supply_FUNC_TEST	TRUE	
ALL_SYS_PWRGD	TRUE	26 45 63
PPVCORE_CPU_S0	TRUE	64
PP1V05_S0	TRUE	64
PP1V5_S0	TRUE	64
PP1V8_S0	TRUE	64
PP2V5_S0	TRUE	64
PP3V3_S0	TRUE	64
PP5V_S0	TRUE	64
PP1V2_S3	TRUE	64
PP1V8_S3	TRUE	64
PP2V5_S3	TRUE	64
PP3V3_S3	TRUE	64
PP5V_S3	TRUE	64
PP3V3_S5	TRUE	64
PP5V_S5	TRUE	64
PP3V42_G3H	TRUE	64
PPBUSA_G3H	TRUE	64
PPBUSB_G3H	TRUE	64
PP18V5_G3H	TRUE	64
PP0V9_S0	TRUE	64

Battery Digital Connector

FUNC_TEST	Value	Page
SMC_BS_ALRT_L	TRUE	45 46 65
SMBUS_BATT_SCL_F	TRUE	65
SMBUS_BATT_SDA_F	TRUE	65
BATT_IN	TRUE	
BATT_POS	TRUE	65
BATT_NEG	TRUE	65

Audio FUNC_TEST

FUNC_TEST	Value	Page
PP5V_S0_AUDIO_PWR	TRUE	
PP5V_S0_AUDIO	TRUE	
GND_AUDIO_PWR	TRUE	64
GND_AUDIO_CODEC	TRUE	64
ACZ_SDATAIN<0>	TRUE	21 64
ACZ_SDATAOUT	TRUE	21 64
ACZ_BITCLK	TRUE	21 64
ACZ_RST_L	TRUE	21 54 57
ACZ_SYNC	TRUE	21 64

Battery FUNC_TEST

FUNC_TEST	Value	Page
SMC_BATT_ISET	TRUE	45 66
SMC_BATT_CHG_EN	TRUE	45 46 66
SMC_BC_ACOK	TRUE	45 46 65 66
SMC_PS_ON	TRUE	39 45 46 65
SMC_BATT_TRICKLE_EN_L	TRUE	45 46 66
SYS_ONEWIRE	TRUE	45 46 65

USB FUNC_TEST

FUNC_TEST	Value	Page
TP_USBP_E	TRUE	6
TP_USBN_E	TRUE	6
TP_USBP_F	TRUE	6
TP_USBN_F	TRUE	6

DC-JACK FUNC_TEST

FUNC_TEST	Value	Page
ACIN_ENABLE_GATE	TRUE	65

Battery charger FUNC_TEST

FUNC_TEST	Value	Page
PPVBAT_G3H_CHGR_OUT	TRUE	66

INVERTER CONNECTOR FUNC_TEST

FUNC_TEST	Value	Page
PPBUS_ALL_INV_CONN	TRUE	67
INV_GND	TRUE	67
PP5V_INV_F	TRUE	67
INV_BKLIGHT_PWM_L	TRUE	67

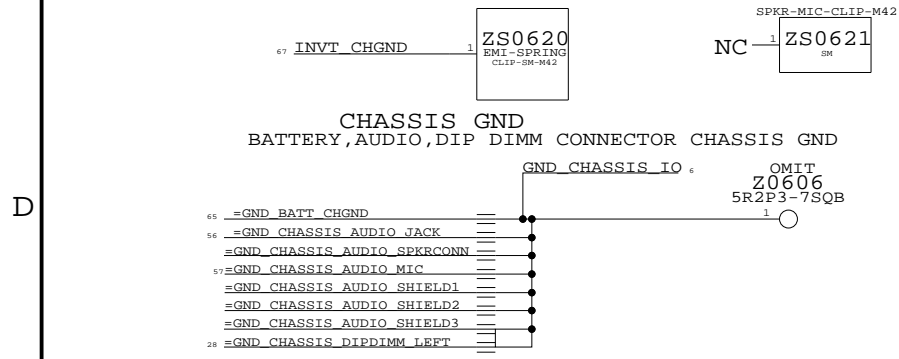
FUNC TEST 1 OF 2

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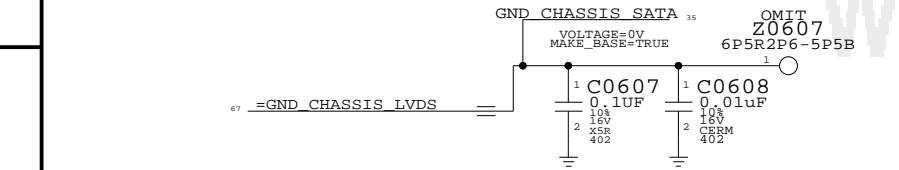
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	NONE	5	78	00000

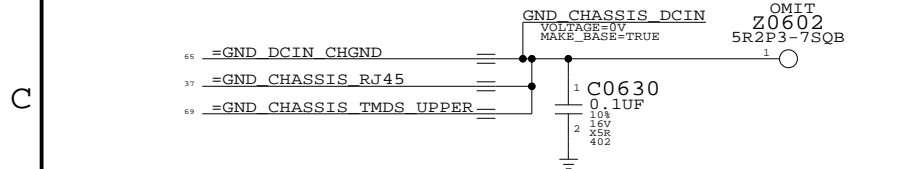
(EMI PAD FOR INVERTER CONNECTOR)



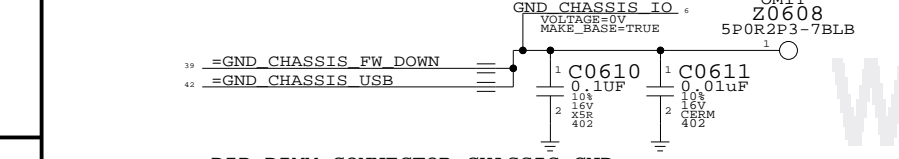
SATA, LVDS CONNECTOR CHASSIS GND



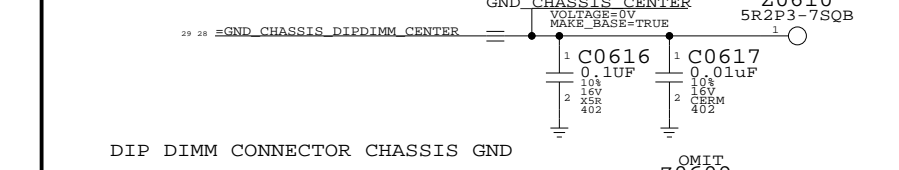
DCIN CONNECTOR CHASSIS GND



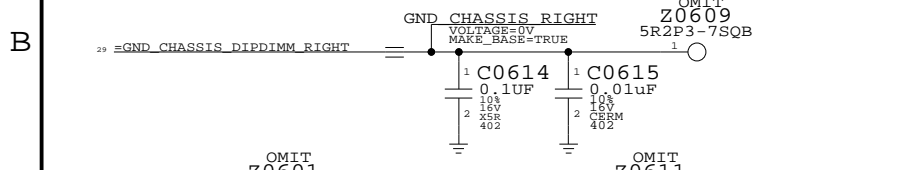
I/O CONNECTOR CHASSIS GND



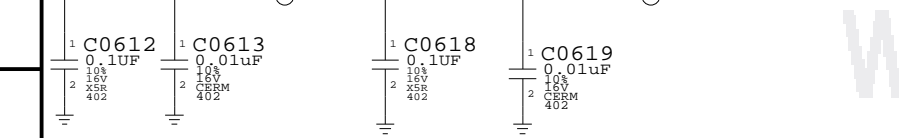
DIP DIMM CONNECTOR CHASSIS GND



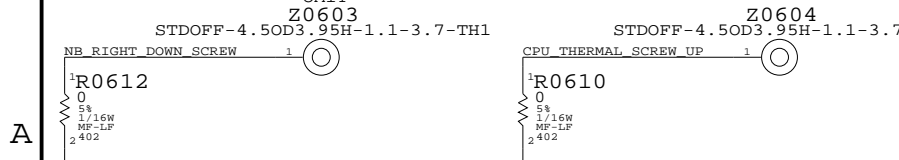
DIP DIMM CONNECTOR CHASSIS GND



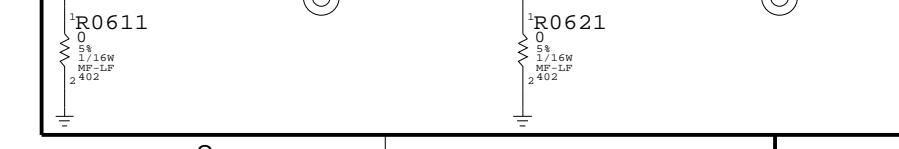
GND_CHASSIS_CPU



DIGITAL GND SCREW HOLE



CPU_THERMAL_SCREW_DOWN



LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

13	LVDS B CLK N	LVDS B CLK N SPN	MAKE_BASE=TRUE	5
13	LVDS B CLK P	LVDS B CLK P SPN	MAKE_BASE=TRUE	5
13	LVDS B DATA N<0>	LVDS B DATA N0 SPN	MAKE_BASE=TRUE	5
13	LVDS B DATA N<1>	LVDS B DATA N1 SPN	MAKE_BASE=TRUE	5
13	LVDS B DATA N<2>	LVDS B DATA N2 SPN	MAKE_BASE=TRUE	5
13	LVDS B DATA P<0>	LVDS B DATA P0 SPN	MAKE_BASE=TRUE	5
13	LVDS B DATA P<1>	LVDS B DATA P1 SPN	MAKE_BASE=TRUE	5
13	LVDS B DATA P<2>	LVDS B DATA P2 SPN	MAKE_BASE=TRUE	5

PCI EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

13	PEG D2R N<0>	PEG D2R N0 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<2>	PEG D2R N2 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<3>	PEG D2R N3 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<4>	PEG D2R N4 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<5>	PEG D2R N5 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<6>	PEG D2R N6 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<7>	PEG D2R N7 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<8>	PEG D2R N8 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<9>	PEG D2R N9 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<10>	PEG D2R N10 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<11>	PEG D2R N11 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<12>	PEG D2R N12 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<13>	PEG D2R N13 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<14>	PEG D2R N14 SPN	MAKE_BASE=TRUE	5
13	PEG D2R N<15>	PEG D2R N15 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<0>	PEG D2R P0 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<2>	PEG D2R P2 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<3>	PEG D2R P3 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<4>	PEG D2R P4 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<5>	PEG D2R P5 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<6>	PEG D2R P6 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<7>	PEG D2R P7 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<8>	PEG D2R P8 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<9>	PEG D2R P9 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<10>	PEG D2R P10 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<11>	PEG D2R P11 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<12>	PEG D2R P12 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<13>	PEG D2R P13 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<14>	PEG D2R P14 SPN	MAKE_BASE=TRUE	5
13	PEG D2R P<15>	PEG D2R P15 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<4>	PEG R2D C N4 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<5>	PEG R2D C N5 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<6>	PEG R2D C N6 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<7>	PEG R2D C N7 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<8>	PEG R2D C N8 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<9>	PEG R2D C N9 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<10>	PEG R2D C N10 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<11>	PEG R2D C N11 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<12>	PEG R2D C N12 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<13>	PEG R2D C N13 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<14>	PEG R2D C N14 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C N<15>	PEG R2D C N15 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<4>	PEG R2D C P4 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<5>	PEG R2D C P5 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<6>	PEG R2D C P6 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<7>	PEG R2D C P7 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<8>	PEG R2D C P8 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<9>	PEG R2D C P9 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<10>	PEG R2D C P10 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<11>	PEG R2D C P11 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<12>	PEG R2D C P12 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<13>	PEG R2D C P13 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<14>	PEG R2D C P14 SPN	MAKE_BASE=TRUE	5
13	PEG R2D C P<15>	PEG R2D C P15 SPN	MAKE_BASE=TRUE	5

NB CFG ALIASES

NO-CONNECT UNUSED CFG INTERFACE PORTS

14	NB_CFG<3>	TP_NB_CFG3	MAKE_BASE=TRUE	5
14	NB_CFG<4>	TP_NB_CFG4	MAKE_BASE=TRUE	5
14	NB_CFG<6>	TP_NB_CFG6	MAKE_BASE=TRUE	5
14	NB_CFG<8>	TP_NB_CFG8	MAKE_BASE=TRUE	5
14	NB_CFG<10>	TP_NB_CFG10	MAKE_BASE=TRUE	5
14	NB_CFG<11>	TP_NB_CFG11	MAKE_BASE=TRUE	5
14	NB_CFG<12>	TP_NB_CFG12	MAKE_BASE=TRUE	5
14	NB_CFG<13>	TP_NB_CFG13	MAKE_BASE=TRUE	5
14	NB_CFG<14>	TP_NB_CFG14	MAKE_BASE=TRUE	5
14	NB_CFG<15>	TP_NB_CFG15	MAKE_BASE=TRUE	5
14	NB_CFG<17>	TP_NB_CFG17	MAKE_BASE=TRUE	5

FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

38	FW_B_TPBIA5	FW_B_TPBIA5 SPN	MAKE_BASE=TRUE	5
38	FW_B_TPA_P	FW_B_TPA_P SPN	MAKE_BASE=TRUE	5
38	FW_B_TPA_N	FW_B_TPA_N SPN	MAKE_BASE=TRUE	5
38	FW_B_TPB_P	FW_B_TPB_P SPN	MAKE_BASE=TRUE	5
38	FW_B_TPB_N	FW_B_TPB_N SPN	MAKE_BASE=TRUE	5
38	FW_C_TPBIA5	FW_C_TPBIA5 SPN	MAKE_BASE=TRUE	5
38	FW_C_TPA_P	FW_C_TPA_P SPN	MAKE_BASE=TRUE	5
38	FW_C_TPA_N	FW_C_TPA_N SPN	MAKE_BASE=TRUE	5
38	FW_C_TPB_P	FW_C_TPB_P SPN	MAKE_BASE=TRUE	5
38	FW_C_TPB_N	FW_C_TPB_N SPN	MAKE_BASE=TRUE	5
39	FWPWR_PWRON	NC_FWPWR_PWRON	MAKE_TEST=TRUE MAKE_BASE=TRUE	5

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

21	SATA_A_D2R_N	SATA_A_D2R_N SPN	MAKE_BASE=TRUE	5
21	SATA_A_D2R_P	SATA_A_D2R_P SPN	MAKE_BASE=TRUE	5
21	SATA_A_R2D_C_N	SATA_A_R2D_C_N SPN	MAKE_BASE=TRUE	5
21	SATA_A_R2D_C_P	SATA_A_R2D_C_P SPN	MAKE_BASE=TRUE	5

PCI_EXP ALIASES

NO-CONNECT UNUSED PCI_EXP INTERFACE PORTS

22	PCIE_C_D2R_N	PCIE_C_D2R_N SPN	MAKE_BASE=TRUE	5
22	PCIE_C_D2R_P	PCIE_C_D2R_P SPN	MAKE_BASE=TRUE	5
22	PCIE_C_R2D_C_N	PCIE_C_R2D_C_N SPN	MAKE_BASE=TRUE	5
22	PCIE_C_R2D_C_P	PCIE_C_R2D_C_P SPN	MAKE_BASE=TRUE	5
22	PCIE_D_D2R_N	PCIE_D_D2R_N SPN	MAKE_BASE=TRUE	5
22	PCIE_D_D2R_P	PCIE_D_D2R_P SPN	MAKE_BASE=TRUE	5
22	PCIE_D_R2D_C_N	PCIE_D_R2D_C_N SPN	MAKE_BASE=TRUE	5
22	PCIE_D_R2D_C_P	PCIE_D_R2D_C_P SPN	MAKE_BASE=TRUE	5
22	PCIE_E_D2R_N	PCIE_E_D2R_N SPN	MAKE_BASE=TRUE	5
22	PCIE_E_D2R_P	PCIE_E_D2R_P SPN	MAKE_BASE=TRUE	5
22	PCIE_E_R2D_C_N	PCIE_E_R2D_C_N SPN	MAKE_BASE=TRUE	5
22	PCIE_E_R2D_C_P	PCIE_E_R2D_C_P SPN	MAKE_BASE=TRUE	5
22	PCIE_F_D2R_N	PCIE_F_D2R_N SPN	MAKE_BASE=TRUE	5
22	PCIE_F_D2R_P	PCIE_F_D2R_P SPN	MAKE_BASE=TRUE	5
22	PCIE_F_R2D_C_N	PCIE_F_R2D_C_N SPN	MAKE_BASE=TRUE	5
22	PCIE_F_R2D_C_P	PCIE_F_R2D_C_P SPN	MAKE_BASE=TRUE	5

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

32	CK410_SRC1_N	CK410_SRC1_N SPN	MAKE_BASE=TRUE	5
32	CK410_SRC1_P	CK410_SRC1_P SPN	MAKE_BASE=TRUE	5
32	CK410_SRC3_N	CK410_SRC3_N SPN	MAKE_BASE=TRUE	5
32	CK410_SRC3_P	CK410_SRC3_P SPN	MAKE_BASE=TRUE	5
32	CK410_SRC7_N	CK410_SRC7_N SPN	MAKE_BASE=TRUE	5
32	CK410_SRC7_P	CK410_SRC7_P SPN	MAKE_BASE=TRUE	5
32	CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L SPN	MAKE_BASE=TRUE	5
32	CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L SPN	MAKE_BASE=TRUE	5

SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

23	SUS_CLK_SB	SUS_CLK_SB SPN	MAKE_BASE=TRUE	5
----	------------	----------------	----------------	---

SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

28	MEM_A_A<15>	MEM_A_A15 SPN	MAKE_BASE=TRUE	5
28	MEM_A_A<14>	MEM_A_A14 SPN	MAKE_BASE=TRUE	5
29	MEM_B_A<15>	MEM_B_A15 SPN	MAKE_BASE=TRUE	5
29	MEM_B_A<14>	MEM_B_A14 SPN	MAKE_BASE=TRUE	5

Ethernet ALIASES

36	ENET_CTRL12	ENET_CTRL12 SPN	MAKE_BASE=TRUE	5
36	ENET_CTRL25	ENET_CTRL25 SPN	MAKE_BASE=TRUE	5

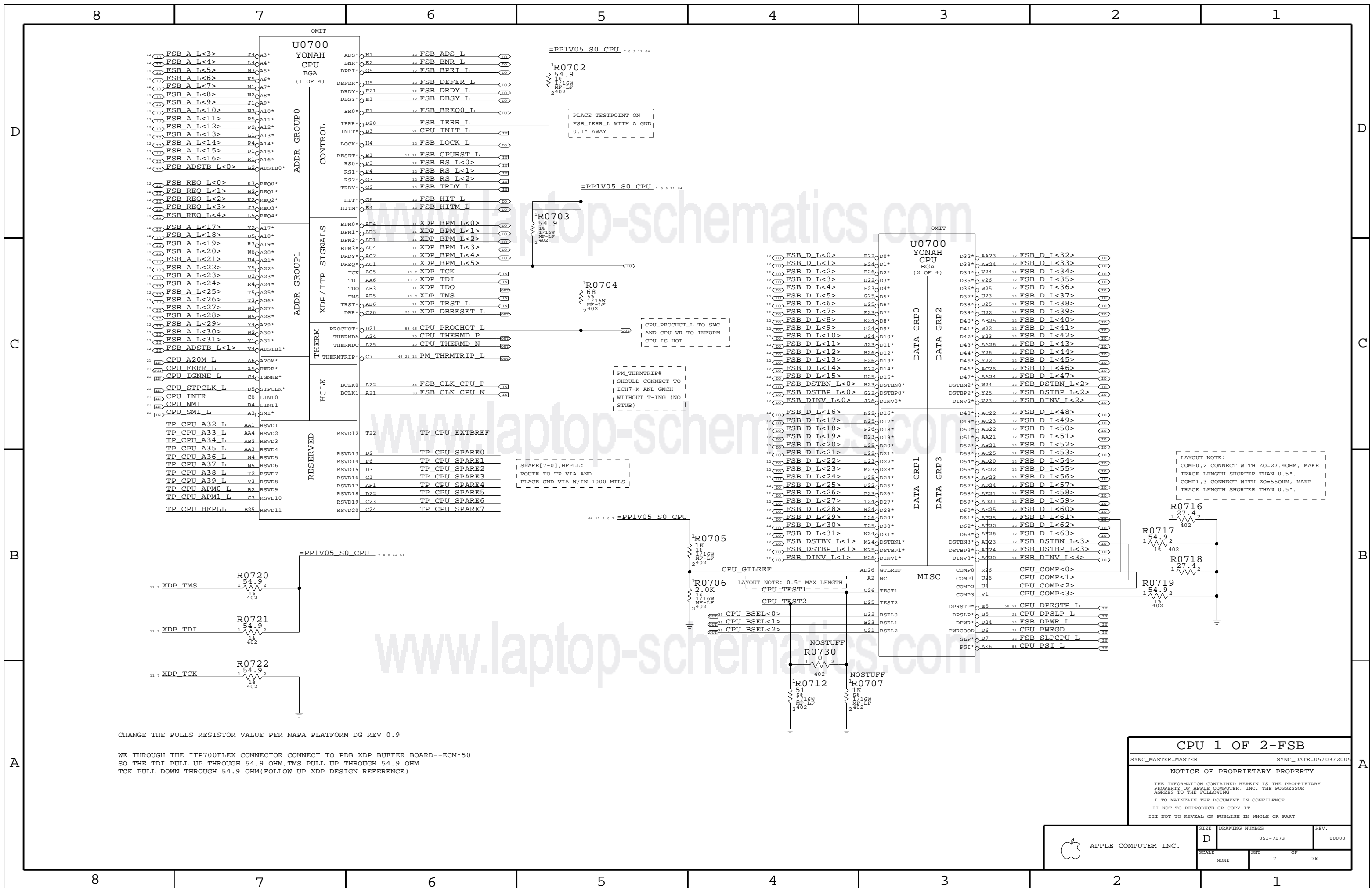
SIGNAL ALIAS /RESET

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0722	4	THERMAL STANDOFF	Z0603,Z0604,Z0605,Z0621	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0612	STANDOFF
860-0749	1	STANDOFF W/THERM HOLES,WIRELESS	Z0613	STANDOFF

APPLE COMPUTER INC.

SCALE	DRAWING NUMBER	REV.
NONE	D 051-7173	00000
SHT	6	OF 78



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50 SO THE TDI PULL UP THROUGH 54.9 OHM, TMS PULL UP THROUGH 54.9 OHM TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

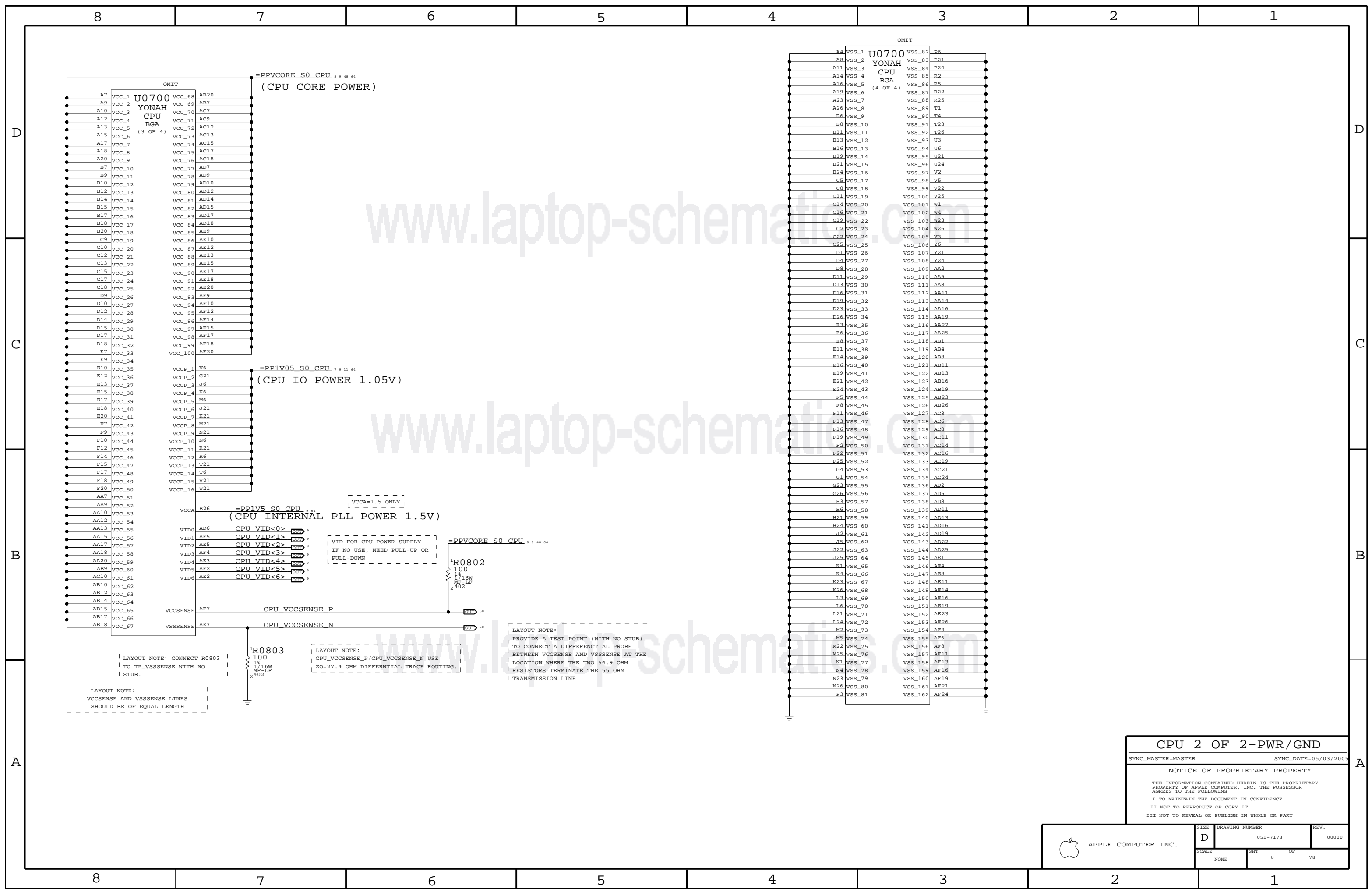
CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

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SCALE	NONE	SHT	7 OF 78



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

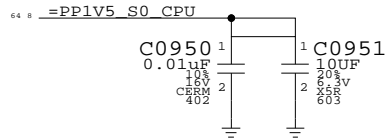
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SCALE	SHT		OF
NONE	8		78

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



CPU CORE VID<> SETTINGS

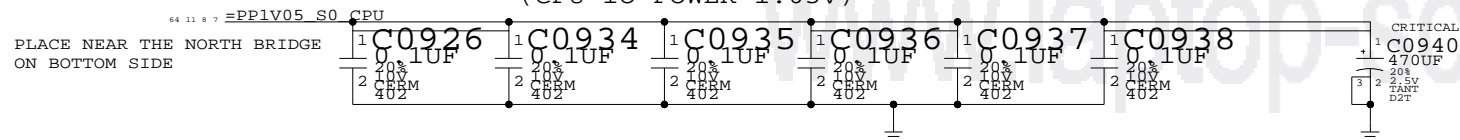
EN CPU VID<6>	R0921	1	0	MF-LP402	58 CPU VID R<6>
EN CPU VID<5>	R0922	1	0	MF-LP402	58 CPU VID R<5>
EN CPU VID<4>	R0923	1	0	MF-LP402	58 CPU VID R<4>
EN CPU VID<3>	R0924	1	0	MF-LP402	58 CPU VID R<3>
EN CPU VID<2>	R0925	1	0	MF-LP402	58 CPU VID R<2>
EN CPU VID<1>	R0926	1	0	MF-LP402	58 CPU VID R<1>
EN CPU VID<0>	R0927	1	0	MF-LP402	58 CPU VID R<0>

R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

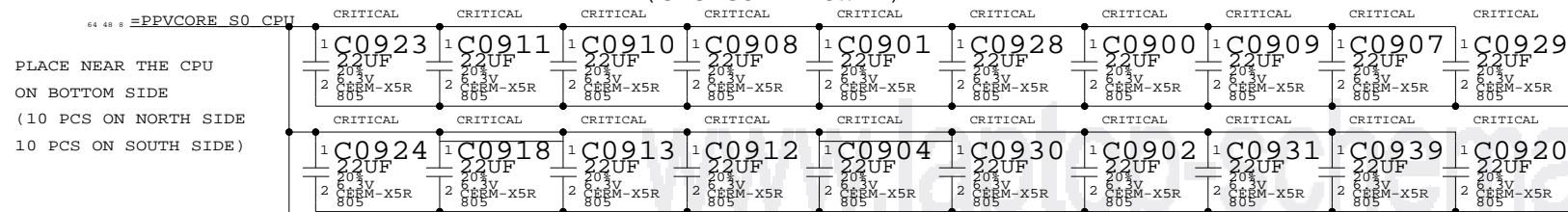
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

THIS 470UF FOR CPU, GMCH FSB BUS 1.05V



VCC CORE DECOUPLING
(CPU CORE POWER)



IF WE USE LOW ESL CAP, THEN WE CAN USE 20 PCS 22UF CAP

	MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM 1.1625		1.30
	VCCLFM TBD		TBD
SINGLE CORE SV CPU	VCCHFM 1.1625		1.30
	VCCLFM TBD		TBD
DUAL CORE LV CPU	VCCHFM 1.0		1.1625
	VCCLFM TBD		TBD
ULV CPU	VCCHFM TBD		TBD
	VCCLFM TBD		TBD

UNIT: V

- # ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
- # TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE (VCORE VOLTAGE)!
- # REFER TO YONAH PROCESSOR EMTS REV 1.0
- # VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
- # VCCLFM: VCORE AT LOWEST FREQUENCY MODE

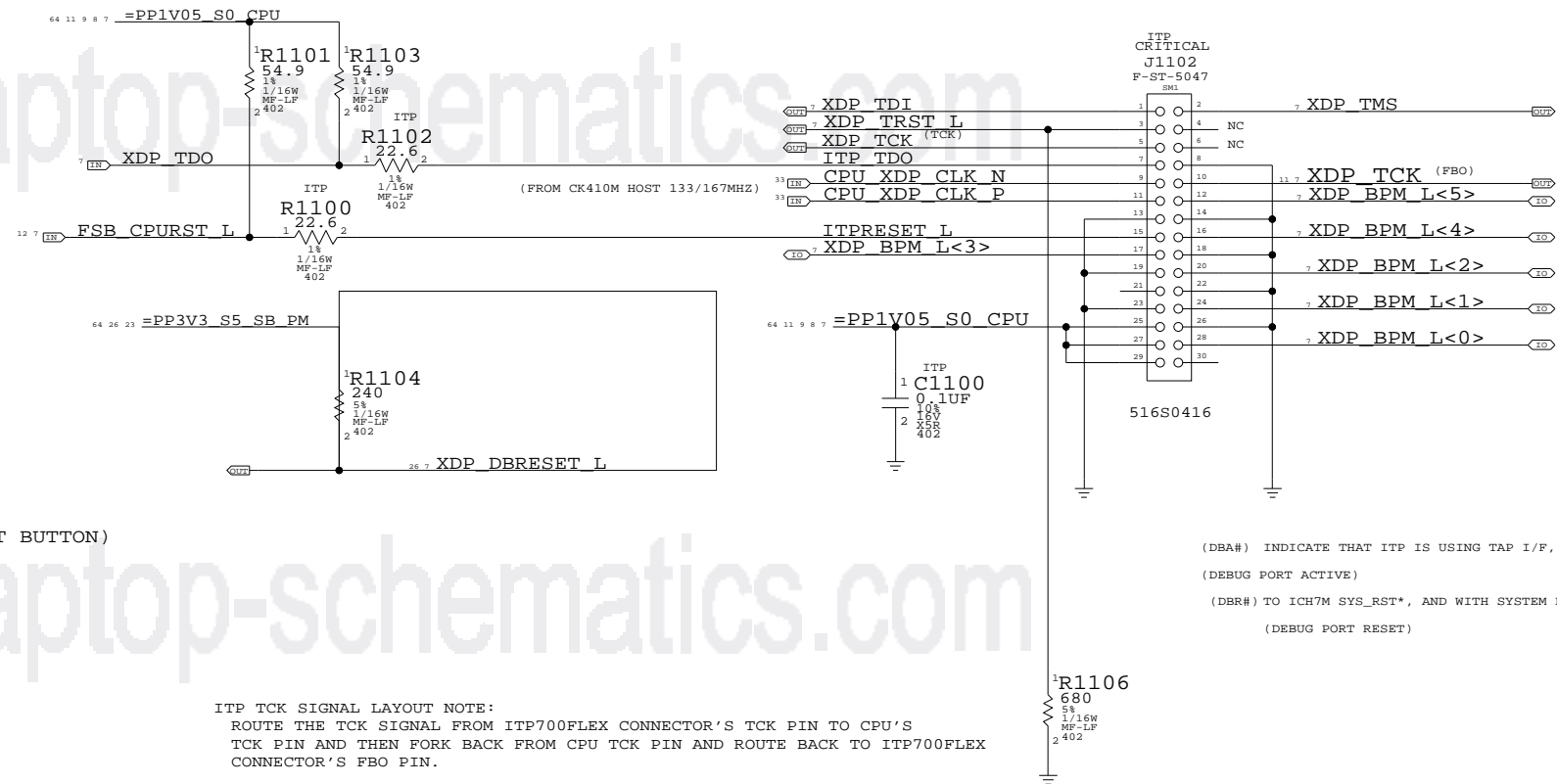
CPU DECAPS & VID<>

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CPU ITP700FLEX DEBUG SUPPORT



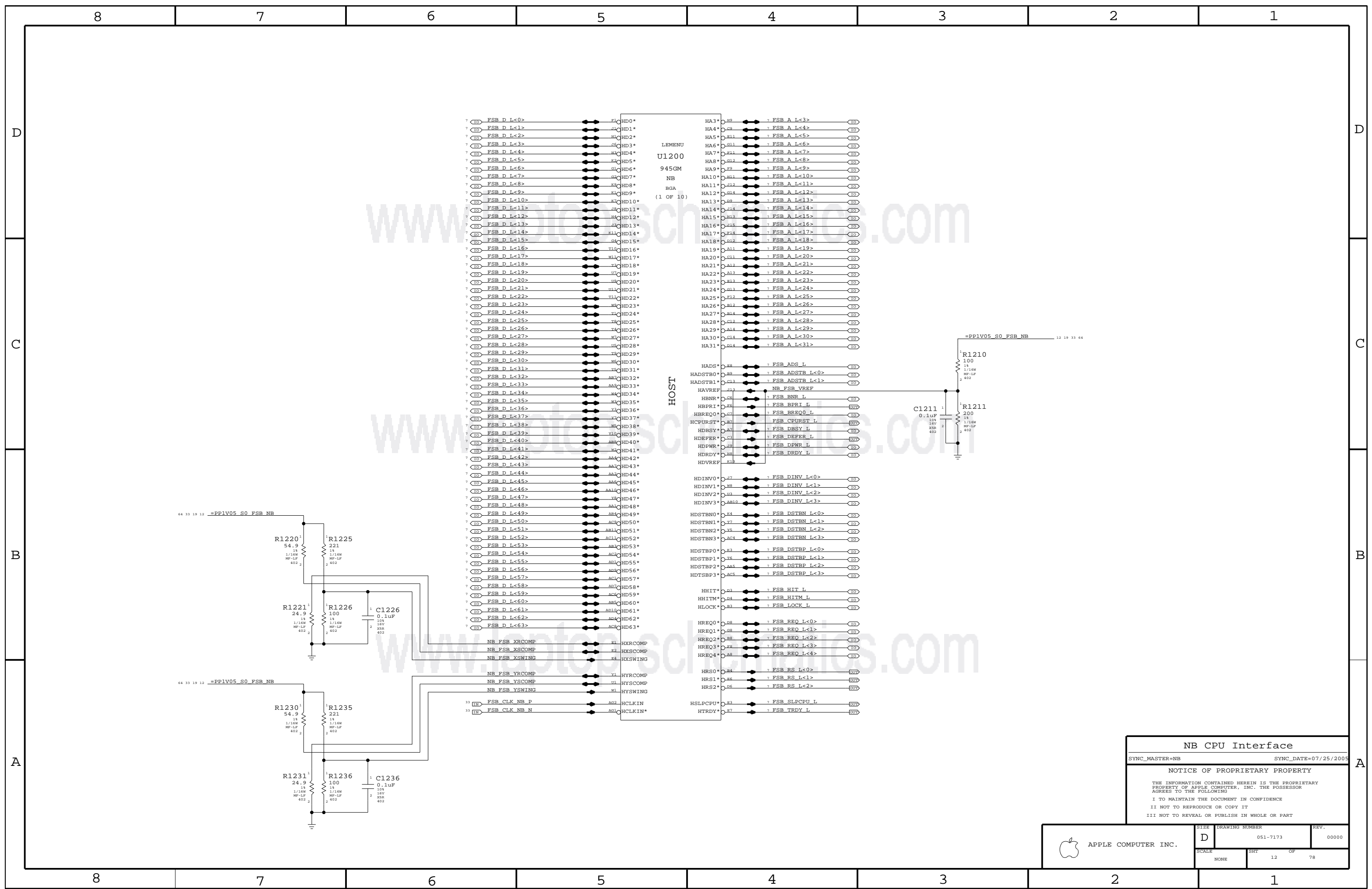
(AND WITH RESET BUTTON)

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)
(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX
CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG
SYNC_MASTER=MASTER SYNC_DATE=5/23/05
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NONE	11	78	



NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

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NONE	12		

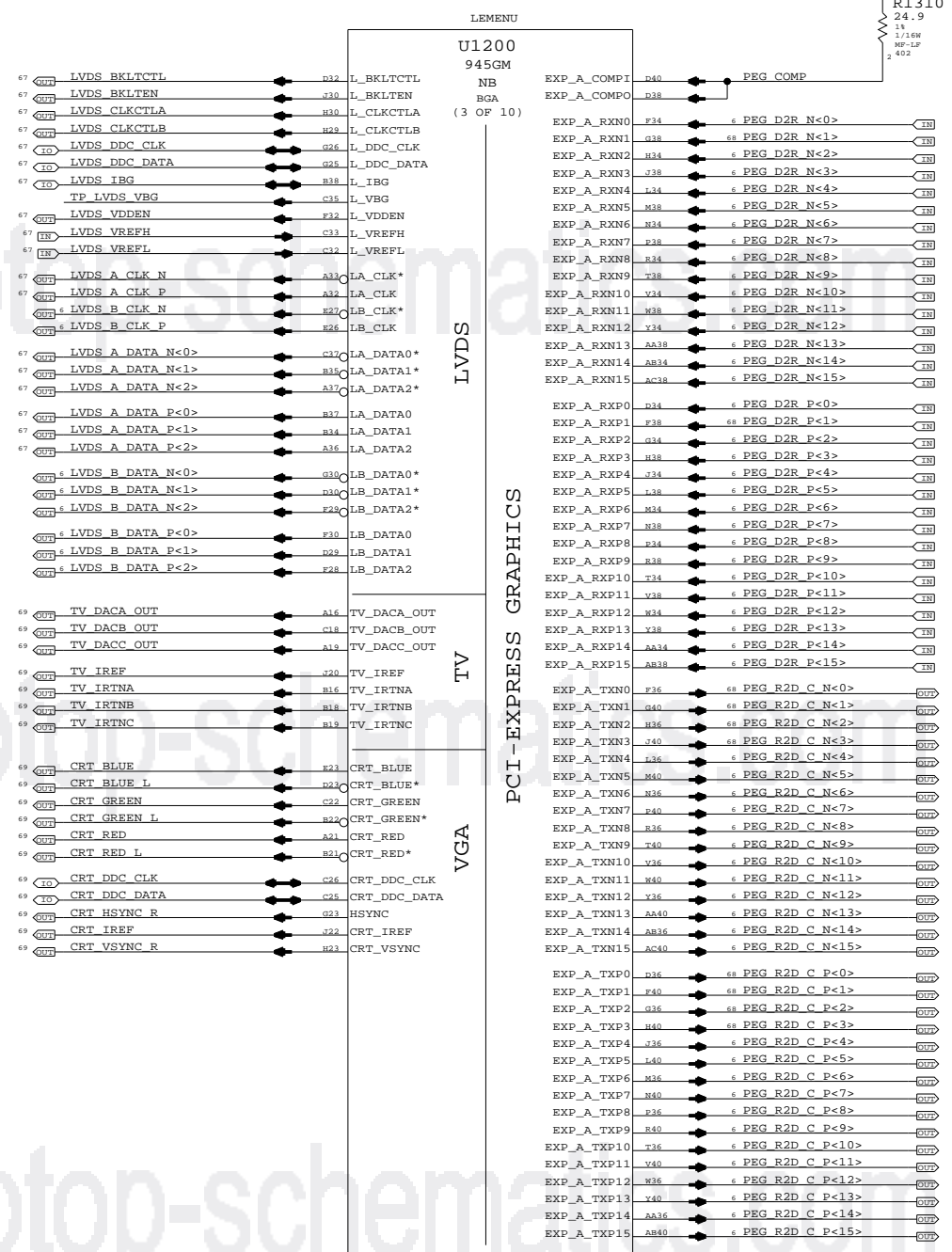
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

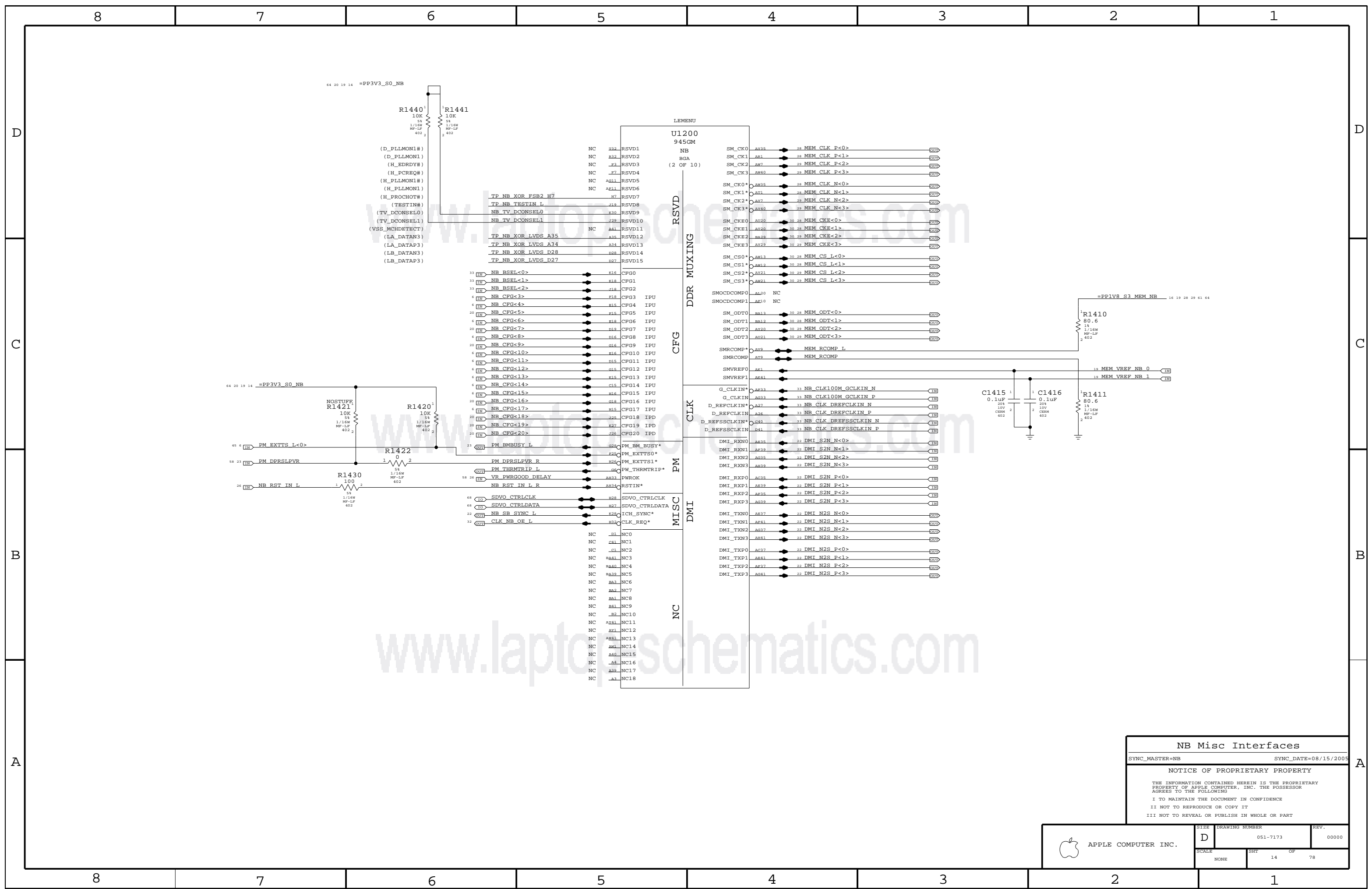
SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=NB SYNC_DATE=07/25/2005
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	D	051-7173	00000
SCALE	NONE	SHT	13 OF 78



NB Misc Interfaces

SYNC_MASTER=NB SYNC_DATE=08/15/2005

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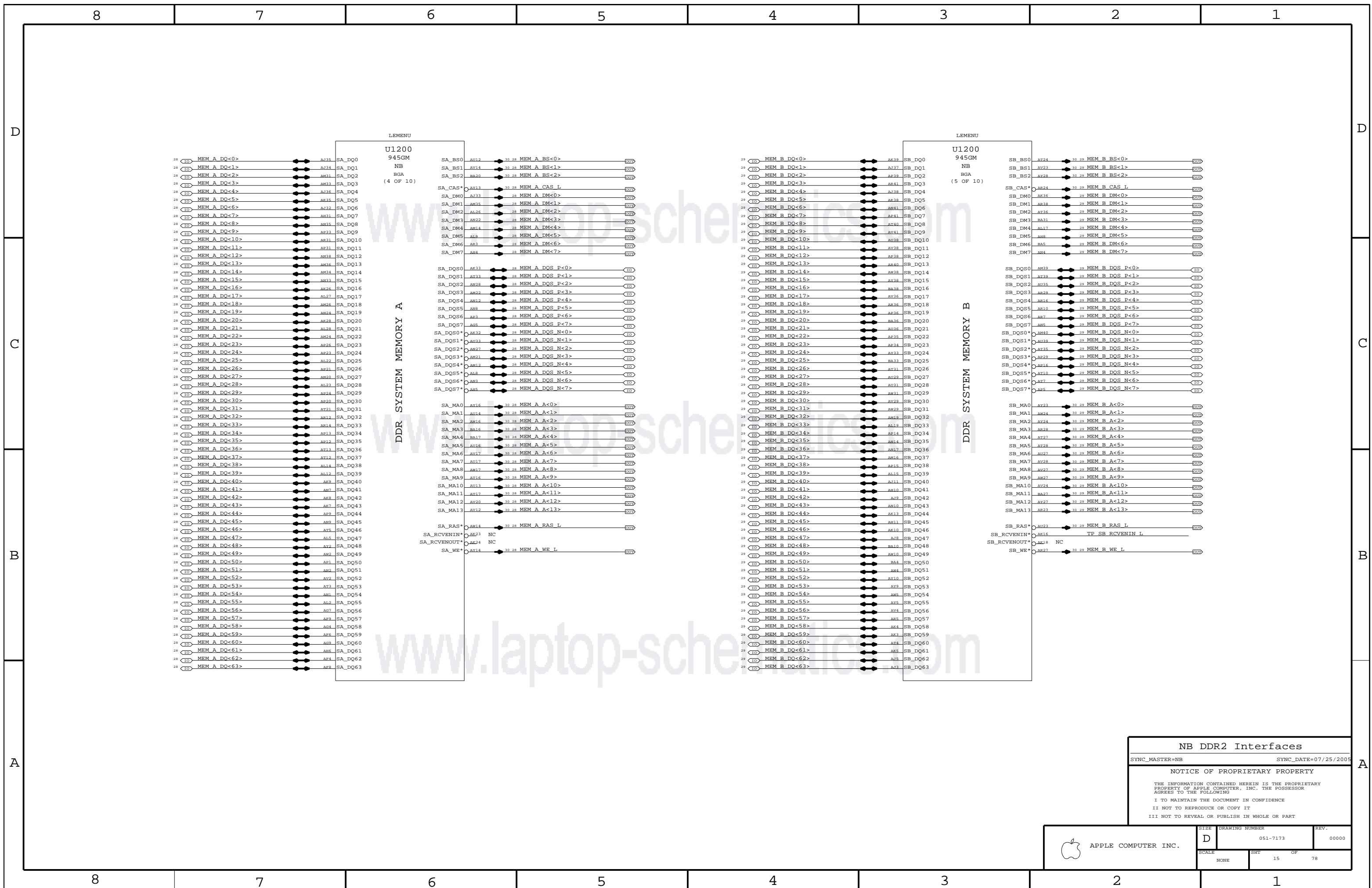
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	SCALE NONE	SHEET 14	OF 78



NB DDR2 Interfaces
 SYNC_MASTER=NB SYNC_DATE=07/25/2005
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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	15		

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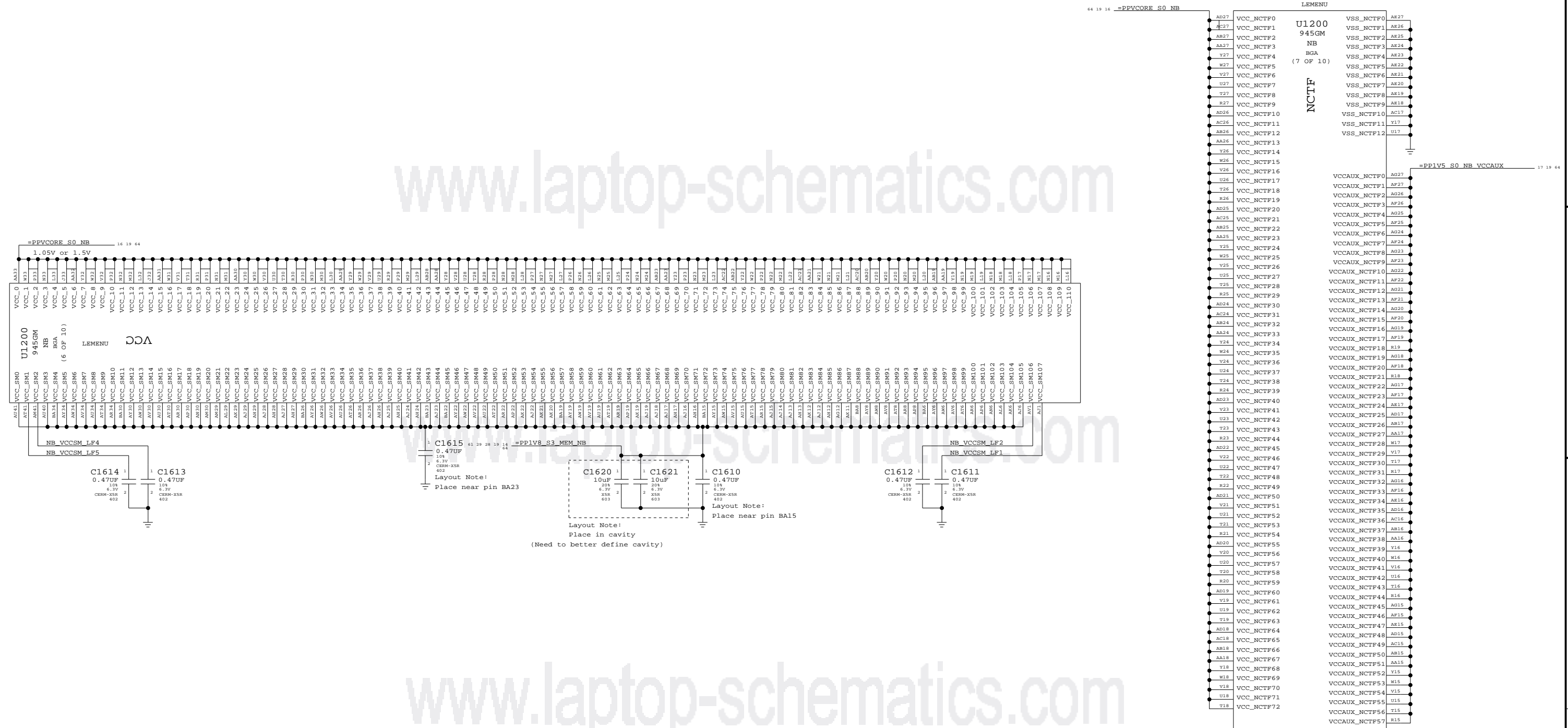
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NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

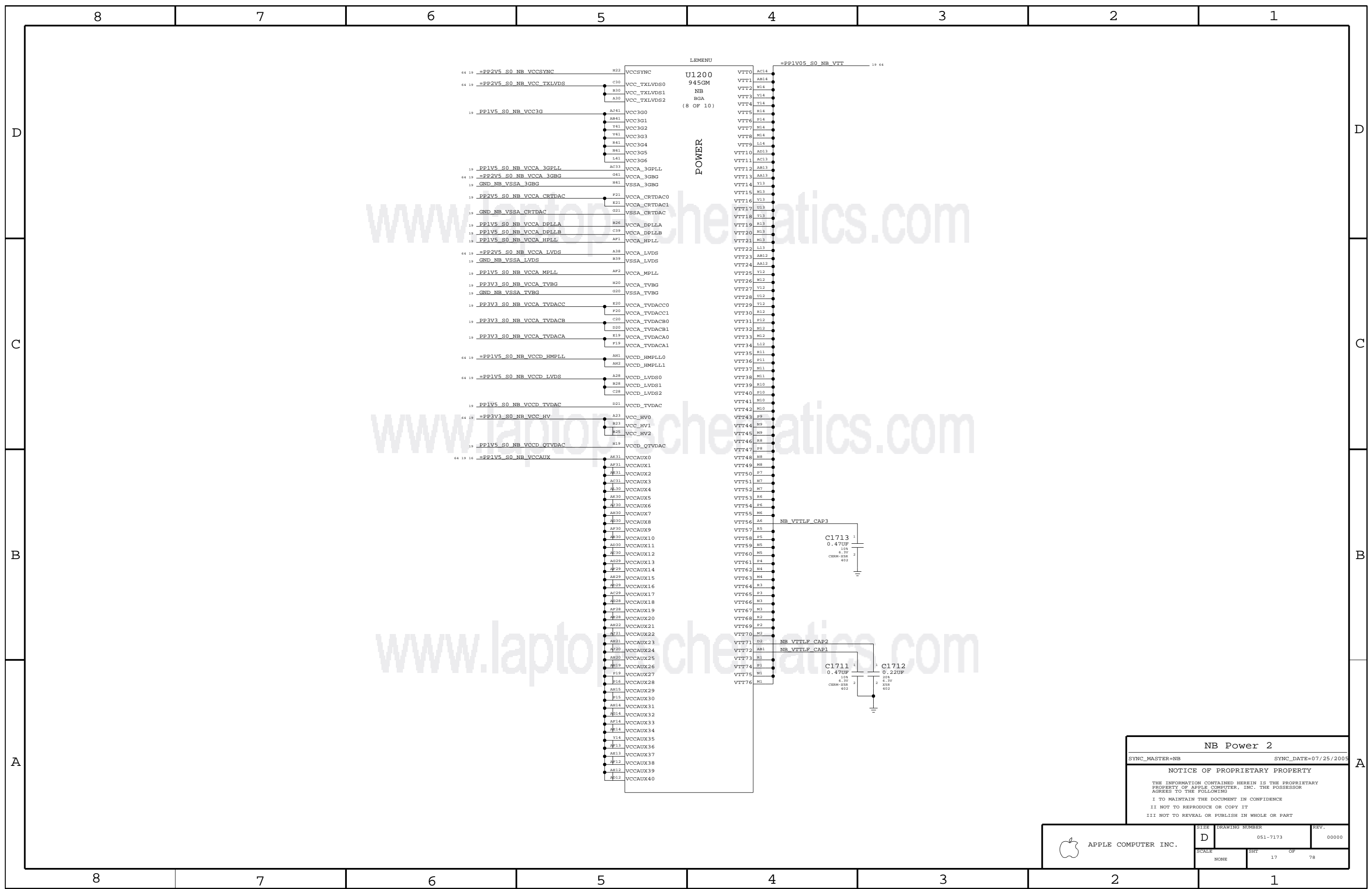
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NB Power 1
 SYNC_MASTER=NB SYNC_DATE=07/25/2005

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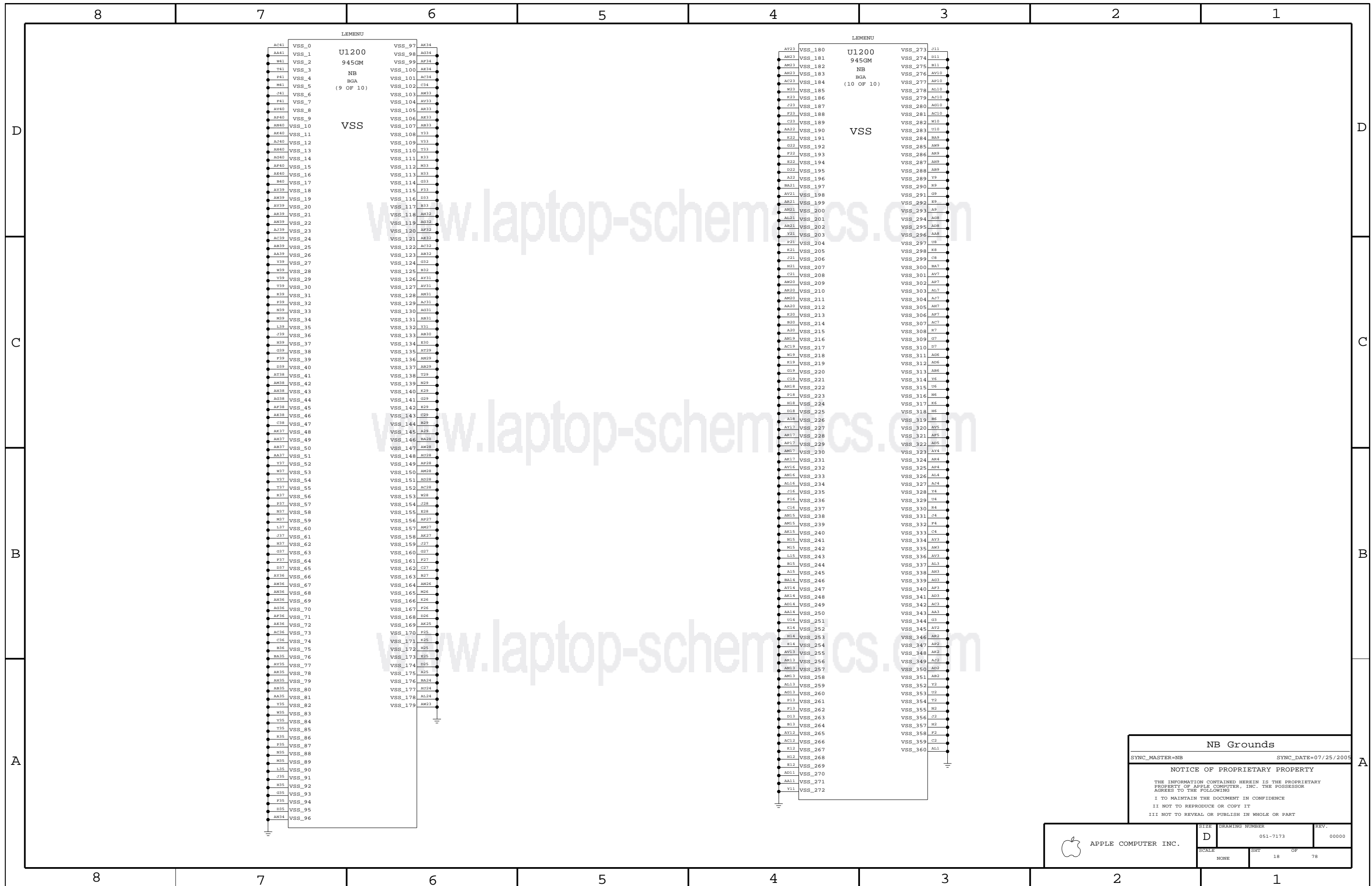
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	78
NONE	16		



NB Power 2
 SYNC_MASTER=NB SYNC_DATE=07/25/2005

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SCALE	SHT	OF	REV.
NONE	17	78	



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AC41	VSS_0	U1200	VSS_97	AK34
AA41	VSS_1	945GM	VSS_98	AP34
W41	VSS_2	NB	VSS_99	AE34
T41	VSS_3	BGA	VSS_100	AE34
P41	VSS_4	(9 OF 10)	VSS_101	AC34
M41	VSS_5		VSS_102	C34
J41	VSS_6		VSS_103	AM33
F41	VSS_7		VSS_104	AV33
AV40	VSS_8		VSS_105	AR33
AP40	VSS_9	VSS	VSS_106	AE33
AN40	VSS_10		VSS_107	AB33
AK40	VSS_11		VSS_108	F33
AL40	VSS_12		VSS_109	V33
AM40	VSS_13		VSS_110	F33
AG40	VSS_14		VSS_111	R33
AF40	VSS_15		VSS_112	M33
AE40	VSS_16		VSS_113	H33
AD40	VSS_17		VSS_114	G33
AC39	VSS_18		VSS_115	F33
AB39	VSS_19		VSS_116	D33
AA39	VSS_20		VSS_117	B33
Y39	VSS_21		VSS_118	ZH32
X39	VSS_22		VSS_119	AD32
W39	VSS_23		VSS_120	AP32
V39	VSS_24		VSS_121	AE32
U39	VSS_25		VSS_122	AC32
T39	VSS_26		VSS_123	AB32
S39	VSS_27		VSS_124	G32
R39	VSS_28		VSS_125	H32
Q39	VSS_29		VSS_126	AV31
P39	VSS_30		VSS_127	AV31
O39	VSS_31		VSS_128	AM31
N39	VSS_32		VSS_129	AL31
M39	VSS_33		VSS_130	AD31
L39	VSS_34		VSS_131	AB31
K39	VSS_35		VSS_132	Y31
J39	VSS_36		VSS_133	AB30
I39	VSS_37		VSS_134	E30
H39	VSS_38		VSS_135	AT29
G39	VSS_39		VSS_136	AN29
F39	VSS_40		VSS_137	AB29
E39	VSS_41		VSS_138	T29
D39	VSS_42		VSS_139	W29
C39	VSS_43		VSS_140	E29
B39	VSS_44		VSS_141	G29
A39	VSS_45		VSS_142	E29
Y39	VSS_46		VSS_143	C29
X39	VSS_47		VSS_144	S29
W39	VSS_48		VSS_145	A29
V39	VSS_49		VSS_146	WA28
U39	VSS_50		VSS_147	AW28
T39	VSS_51		VSS_148	AD28
S39	VSS_52		VSS_149	AP28
R39	VSS_53		VSS_150	AM28
Q39	VSS_54		VSS_151	AD28
P39	VSS_55		VSS_152	AC28
O39	VSS_56		VSS_153	W28
N39	VSS_57		VSS_154	J28
M39	VSS_58		VSS_155	E28
L39	VSS_59		VSS_156	AP27
K39	VSS_60		VSS_157	AM27
J39	VSS_61		VSS_158	AK27
I39	VSS_62		VSS_159	J27
H39	VSS_63		VSS_160	G27
G39	VSS_64		VSS_161	F27
F39	VSS_65		VSS_162	C27
E39	VSS_66		VSS_163	B27
D39	VSS_67		VSS_164	AN26
C39	VSS_68		VSS_165	M26
B39	VSS_69		VSS_166	K26
A39	VSS_70		VSS_167	F26
Y39	VSS_71		VSS_168	D26
X39	VSS_72		VSS_169	AK25
W39	VSS_73		VSS_170	F25
V39	VSS_74		VSS_171	K25
U39	VSS_75		VSS_172	H25
T39	VSS_76		VSS_173	E25
S39	VSS_77		VSS_174	D25
R39	VSS_78		VSS_175	A25
Q39	VSS_79		VSS_176	BA24
P39	VSS_80		VSS_177	AD24
O39	VSS_81		VSS_178	AL24
N39	VSS_82		VSS_179	AK23
M39	VSS_83			
L39	VSS_84			
K39	VSS_85			
J39	VSS_86			
I39	VSS_87			
H39	VSS_88			
G39	VSS_89			
F39	VSS_90			
E39	VSS_91			
D39	VSS_92			
C39	VSS_93			
B39	VSS_94			
A39	VSS_95			
Y39	VSS_96			

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AT23	VSS_180	U1200	VSS_273	J11
AM23	VSS_181	945GM	VSS_274	D11
AN23	VSS_182	NB	VSS_275	B11
AC23	VSS_183	BGA	VSS_276	AV10
AK23	VSS_184	(10 OF 10)	VSS_277	AP10
K23	VSS_185		VSS_278	AL10
J23	VSS_186		VSS_279	AL10
F23	VSS_187		VSS_280	AG10
C23	VSS_188		VSS_281	AC10
AA22	VSS_189	VSS	VSS_282	W10
K22	VSS_190		VSS_283	U10
G22	VSS_191		VSS_284	BA9
F22	VSS_192		VSS_285	AW9
E22	VSS_193		VSS_286	AK9
D22	VSS_194		VSS_287	AN9
A22	VSS_195		VSS_288	AM9
BA21	VSS_196		VSS_289	Y9
AV21	VSS_197		VSS_290	B9
AM21	VSS_198		VSS_291	G9
AN21	VSS_199		VSS_292	E9
AL21	VSS_200		VSS_293	A9
AB21	VSS_201		VSS_294	AD8
Y21	VSS_202		VSS_295	AD8
W21	VSS_203		VSS_296	AA8
P21	VSS_204		VSS_297	U8
K21	VSS_205		VSS_298	E8
J21	VSS_206		VSS_299	C8
H21	VSS_207		VSS_300	BA7
C21	VSS_208		VSS_301	AV7
AM20	VSS_209		VSS_302	AP7
AN20	VSS_210		VSS_303	AL7
AA20	VSS_211		VSS_304	AL7
K20	VSS_212		VSS_305	AM7
B20	VSS_213		VSS_306	AP7
A20	VSS_214		VSS_307	AC7
AM19	VSS_215		VSS_308	R7
AC19	VSS_216		VSS_309	G7
W19	VSS_217		VSS_310	D7
K19	VSS_218		VSS_311	AD6
G19	VSS_219		VSS_312	AD6
C19	VSS_220		VSS_313	AB6
AM18	VSS_221		VSS_314	Y6
P18	VSS_222		VSS_315	U6
H18	VSS_223		VSS_316	H6
D18	VSS_224		VSS_317	E6
A18	VSS_225		VSS_318	H6
AY17	VSS_226		VSS_319	B6
AP17	VSS_227		VSS_320	AV5
AM17	VSS_228		VSS_321	AP5
AL17	VSS_229		VSS_322	AD5
AV16	VSS_230		VSS_323	AL4
AM16	VSS_231		VSS_324	AB4
AL16	VSS_232		VSS_325	AP4
J16	VSS_233		VSS_326	AL4
F16	VSS_234		VSS_327	AL4
C16	VSS_235		VSS_328	V4
AM15	VSS_236		VSS_329	U4
AM15	VSS_237		VSS_330	R4
AM15	VSS_238		VSS_331	J4
AK15	VSS_239		VSS_332	F4
AM15	VSS_240		VSS_333	C4
M15	VSS_241		VSS_334	AP3
M15	VSS_242		VSS_335	AM3
L15	VSS_243		VSS_336	AV3
B15	VSS_244		VSS_337	AL3
A15	VSS_245		VSS_338	AM3
BA14	VSS_246		VSS_339	AG3
AT14	VSS_247		VSS_340	AP3
AK14	VSS_248		VSS_341	AD3
AD14	VSS_249		VSS_342	AC3
DA14	VSS_250		VSS_343	AA3
U14	VSS_251		VSS_344	G3
K14	VSS_252		VSS_345	AT2
H14	VSS_253		VSS_346	AM2
E14	VSS_254		VSS_347	AP2
AV13	VSS_255		VSS_348	AK2
AM13	VSS_256		VSS_349	AL2
AM13	VSS_257		VSS_350	AD2
AM13	VSS_258		VSS_351	AB2
AL13	VSS_259		VSS_352	Y2
AG13	VSS_260		VSS_353	U2
P13	VSS_261		VSS_354	T2
F13	VSS_262		VSS_355	H2
D13	VSS_263		VSS_356	J2
B13	VSS_264		VSS_357	H2
AY12	VSS_265		VSS_358	F2
AC12	VSS_266		VSS_359	C2
K12	VSS_267		VSS_360	AL1
H12	VSS_268			
E12	VSS_269			
AD11	VSS_270			
AA11	VSS_271			
Y11	VSS_272			

NB Grounds

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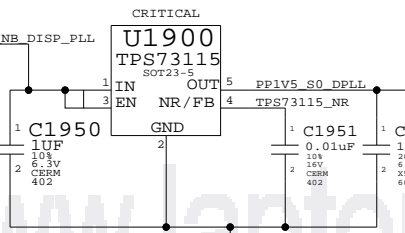
APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7173	00000
	SHT	OF	
	18	78	

Power Interface

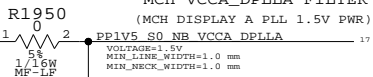
These are the power signals that leave the NB "block"

- =PP1V05_S0_FSB_NB
=PPVCORE_S0_NB
=PP1V05_S0_NB
=PP1V05_S0_NB_VTT
=PP1V5_S0_NB
=PP1V5_S0_NB_PCIE
=PP1V5_S0_NB_PLL
=PP1V5_S0_NB_TVDAC
=PP1V5_S0_NB_VCCD_HMPLL
=PP1V5_S0_NB_VCCD_LVDS
=PP1V5_S0_NB_VCCA_3GBG
=PP1V5_S0_NB_VCCA_LVDS
=PP1V8_S3_MEM_NB
=PP2V5_S0_NB_CRTDAC
=PP2V5_S0_NB_VCCSYNC
=PP2V5_S0_NB_VCC_TXLVDS
=PP2V5_S0_NB_VCCA_3GBG
=PP2V5_S0_NB_VCCA_LVDS
=PP3V3_S0_NB
=PP3V3_S0_NB_VCC_HV
=PP5V_S0_NB_TVDAC

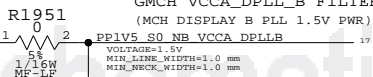
MCH DISPLAY PLL POWER LDO



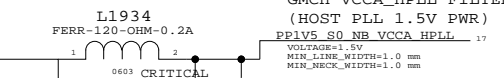
MCH VCCA_DPLL FILTER



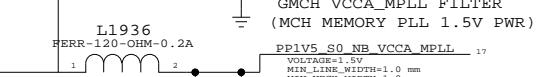
GMCH VCCA_DPLL_B FILTER



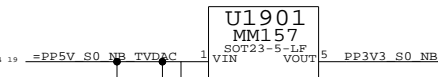
GMCH VCCA_HPLL FILTER



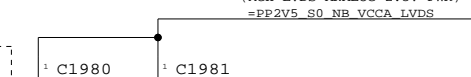
GMCH VCCA_MPLL FILTER



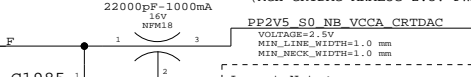
MCH VCCA_DPLL



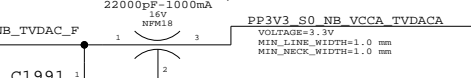
MCH VCCA_LVDS FILTER



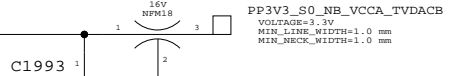
MCH VCCA_CRTDAC BYPASS



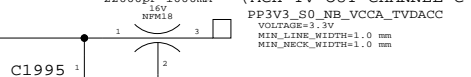
MCH VCCA_TVDACC FILTER



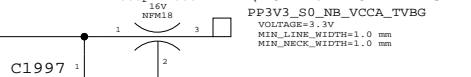
MCH VCCA_TVDACC FILTER



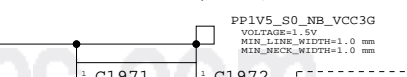
MCH VCCA_TVDACC FILTER



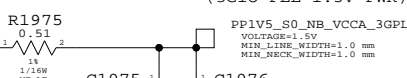
MCH VCCA_TVBG FILTER



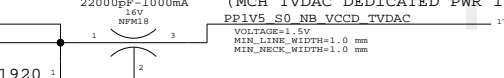
GMCH VCC3G FILTER



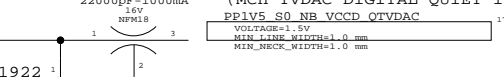
GMCH VCCA_3GPLL FILTER



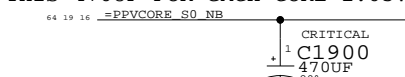
GMCH VCCD_TVDAC FILTER



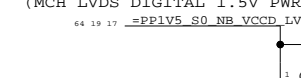
GMCH VCCD_QTVDAC FILTER



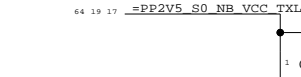
GMCH CORE PWR 1.05V BYPASS



GMCH VCCD_LVDS BYPASS



GMCH VCCD_3GBG BYPASS



GMCH VCCD_TVDAC



GMCH VCCD_QTVDAC



PLACE THOSE COMPONENT CLOSE TO GMCH

GMCH VCCD_LVDS BYPASS

GMCH VCCD_3GBG BYPASS

GMCH VCCD_TVDAC

GMCH VCCD_QTVDAC

Layout Note: Place in cavity

Layout Note: Place L and C close to MCH

Layout Note: This 0.1uF cap should be within 5 mm of NB edge

Layout Note: THESE 4 0.1uF CAPS SHOULD be within 5 mm of NB edge

Layout Note: These 2 caps should be within 6.35 mm of NB edge

Layout Note: These 8 caps should be within 6.35 mm of NB edge

Layout Note: 10uF caps should be close to MCH on opposite side.

Layout Note: These 4 caps should be within 6.35 mm of NB edge

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

Layout Note: Route to caps, then GND

Layout Note: Route to caps, then GND

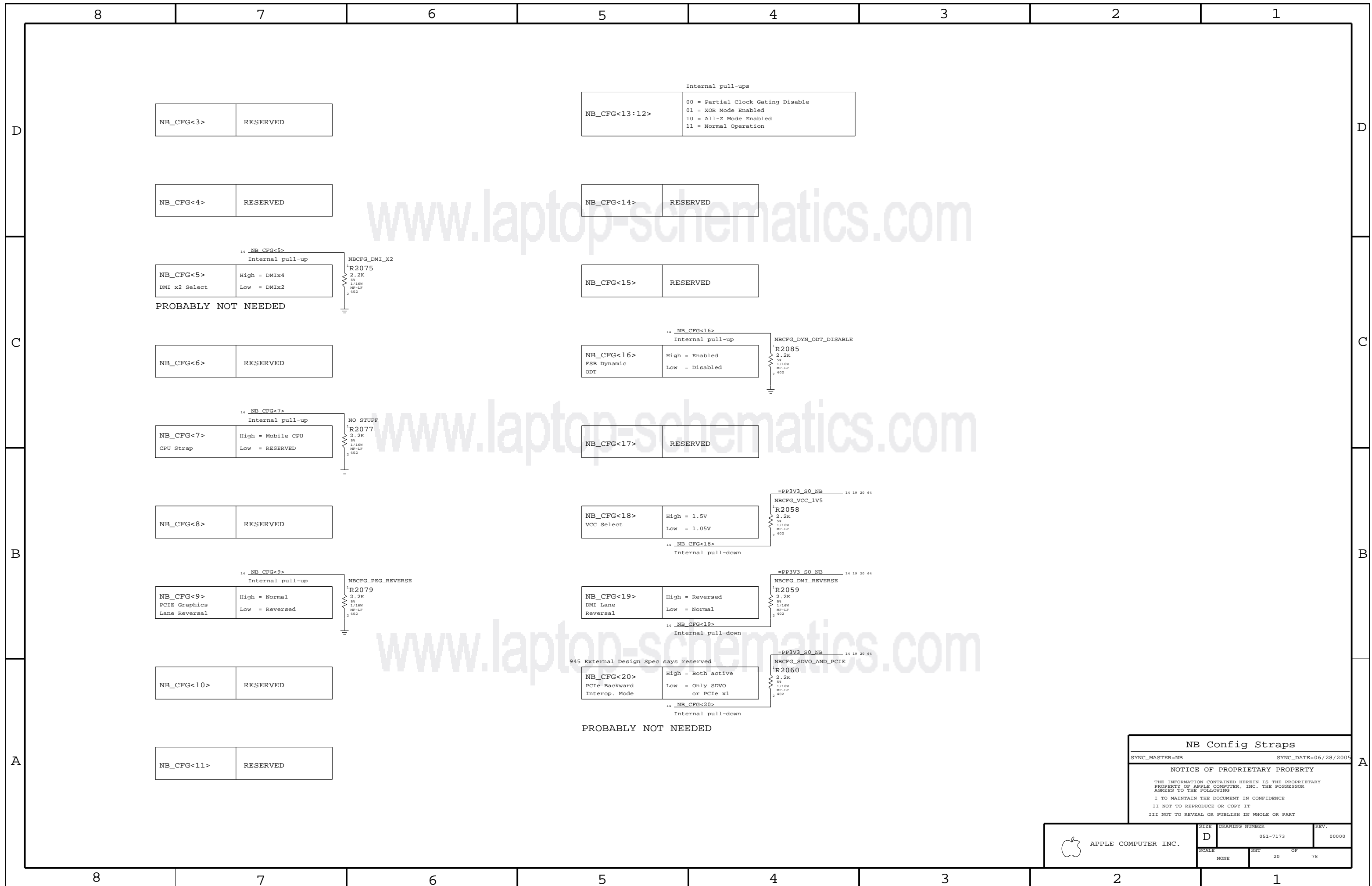
NB (GM) Decoupling

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Table with columns: DRAWING NUMBER (D), REV. (00000), SCALE (NONE), SHEET (19 OF 78), APPLE COMPUTER INC. logo.



NB Config Straps

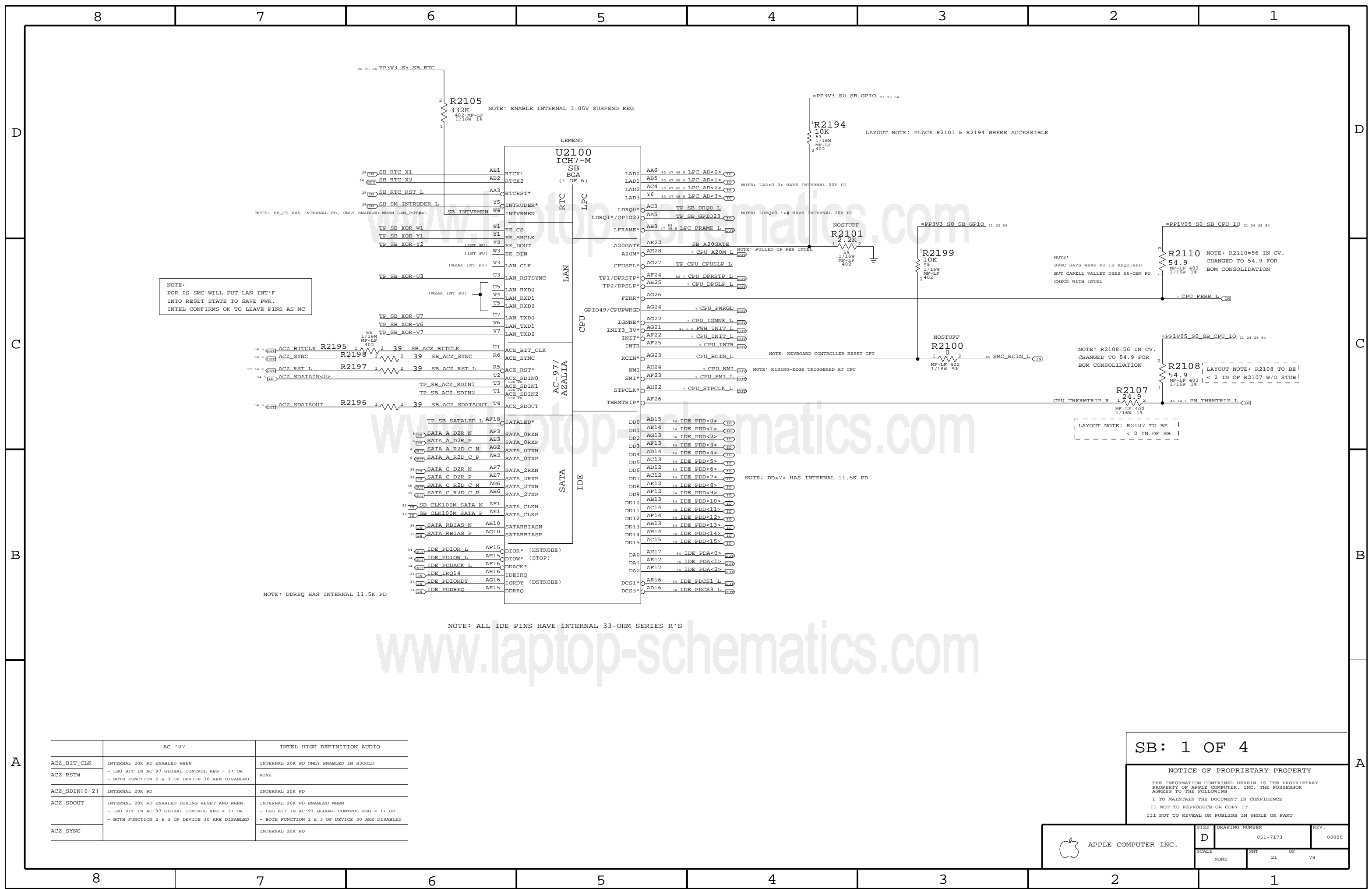
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NONE	20	78	



NOTE:
POR IS SMC WILL PUT LAN INTI'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: ER_CS HAS INTERNAL PD, ONLY ENABLED WHEN LAN_RST# = L

NOTE: LAD<0-3> HAVE INTERNAL 20K PU

NOTE: LDRQ<0-1> HAVE INTERNAL 20K PU

NOTE: PULLED UP PER INTEL

NOTE: KEYBOARD CONTROLLER RESET CPU

NOTE: RISING-EDGE TRIGGERED AT CPU

NOTE: DD<7> HAS INTERNAL 11.5K PD

NOTE:
SPEC SAYS WEAK PU IS REQUIRED
BUT CAPELL VALLEY USES 56-OHM PU
CHECK WITH INTEL

NOTE: R2108=56 IN CV.
CHANGED TO 54.9 FOR
BOM CONSOLIDATION

LAYOUT NOTE: R2107 TO BE
< 2 IN OF SB

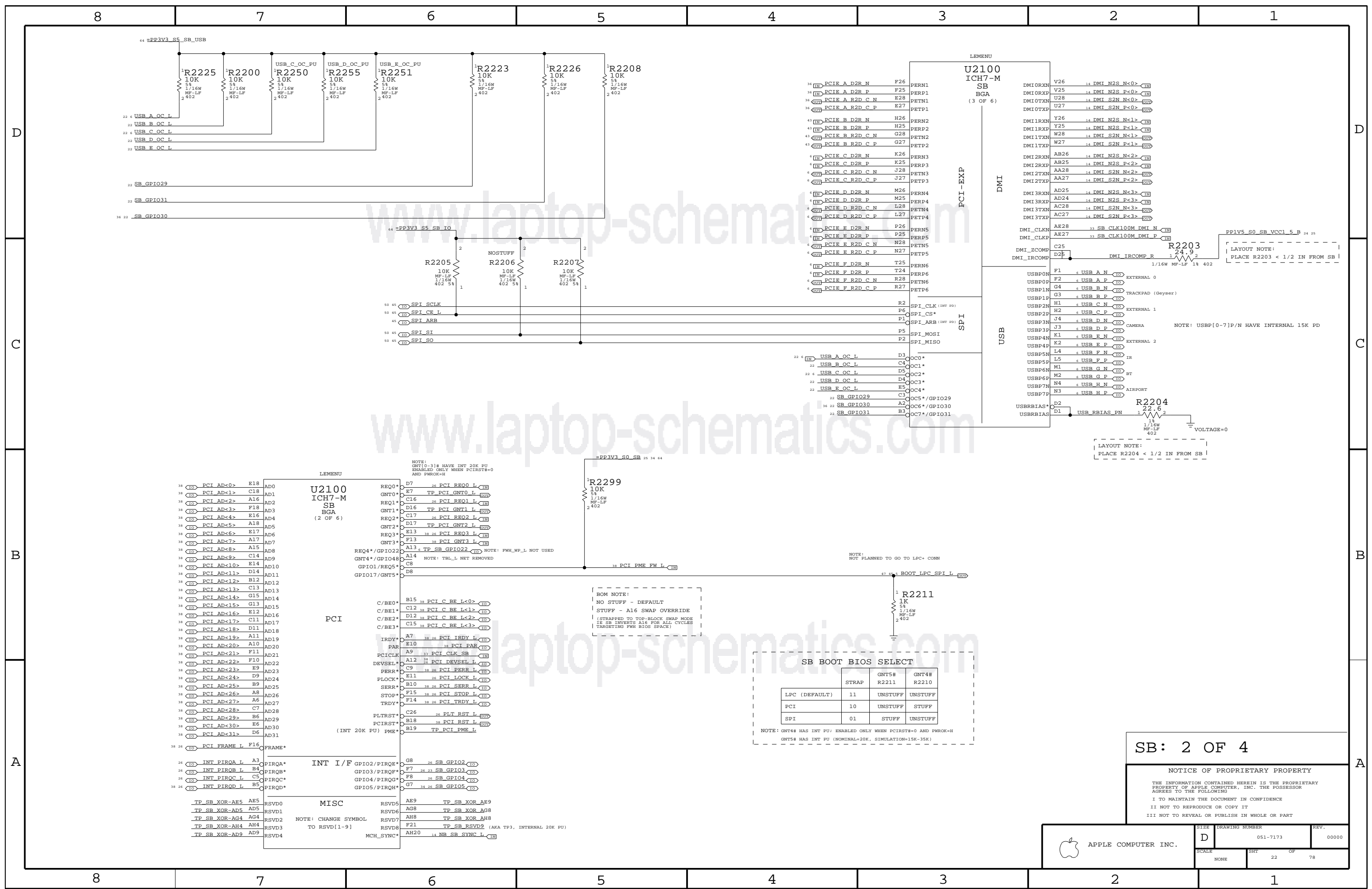
NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

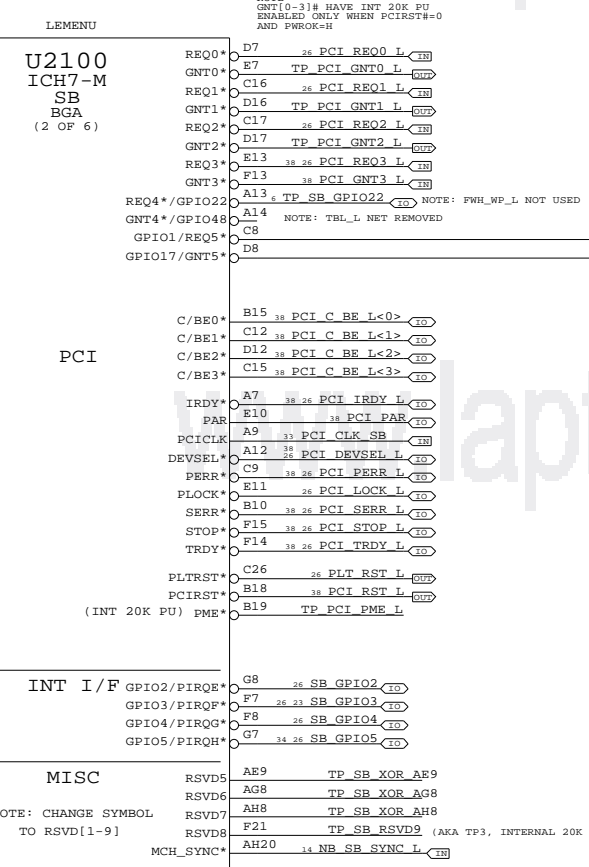
SB: 1 OF 4

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	D	051-7173	00000
SCALE	NONE	SHT	21 OF 78



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SB BOOT BIOS SELECT

	STRAP	GNT5#	GNT4#
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU: ENABLED ONLY WHEN PCIRST# = 0 AND FWRC# = H

NOTE: GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

SB: 2 OF 4

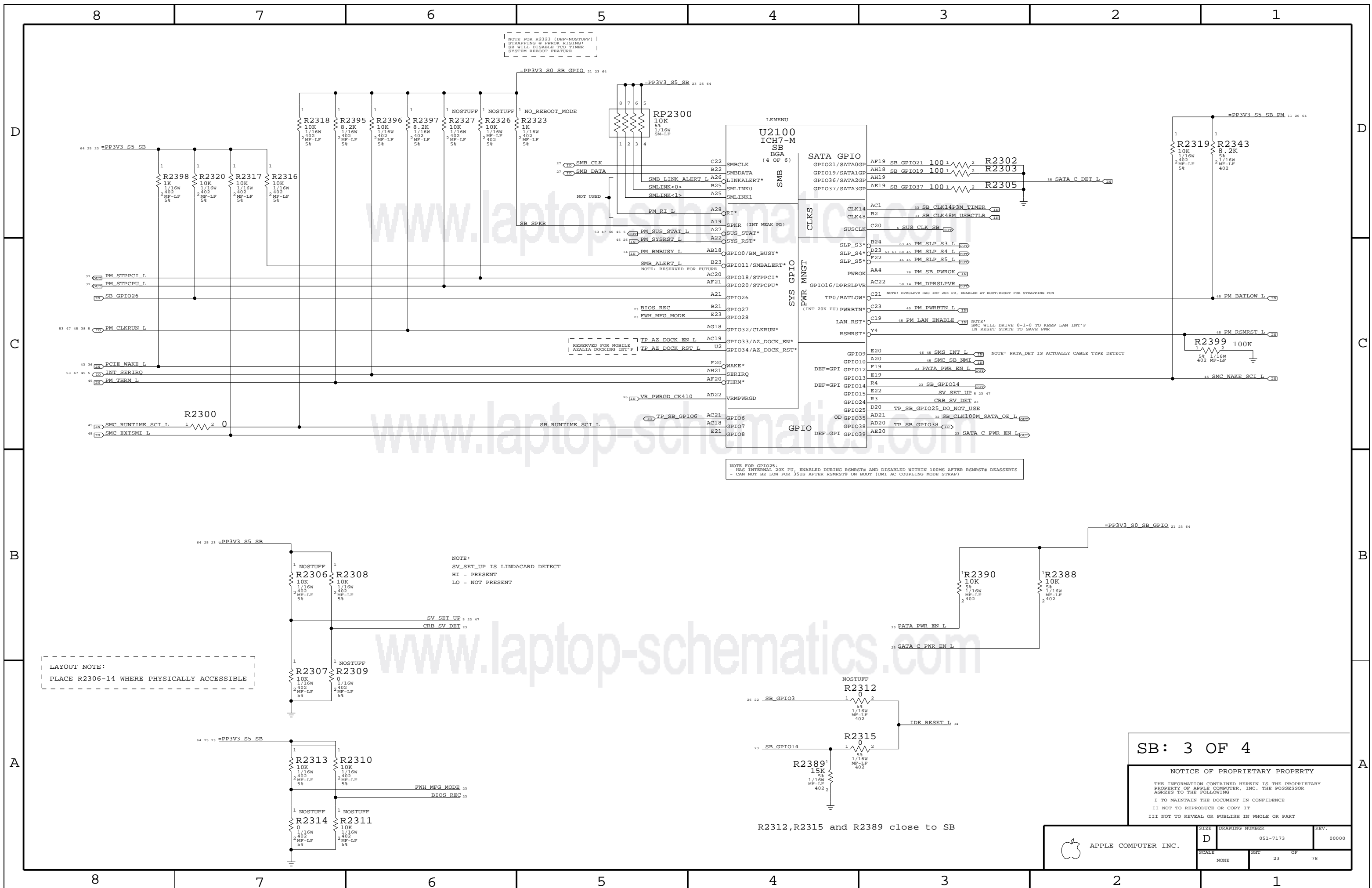
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NOTE FOR R2323 (DEF-NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

NOTE FOR R2323 (DEF-NOSTUFF) | STRAPPING & PWROK RISING: SB WILL DISABLE TOO TIMER SYSTEM REBOOT FEATURE

RESERVED FOR MOBILE | AHALIA DOCKING INT*P | TP_AZ DOCK EN L | TP_AZ DOCK RST L

NOTE FOR GPIO25:
 - HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 - CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (EMI AC COUPLING MODE STRAP)

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

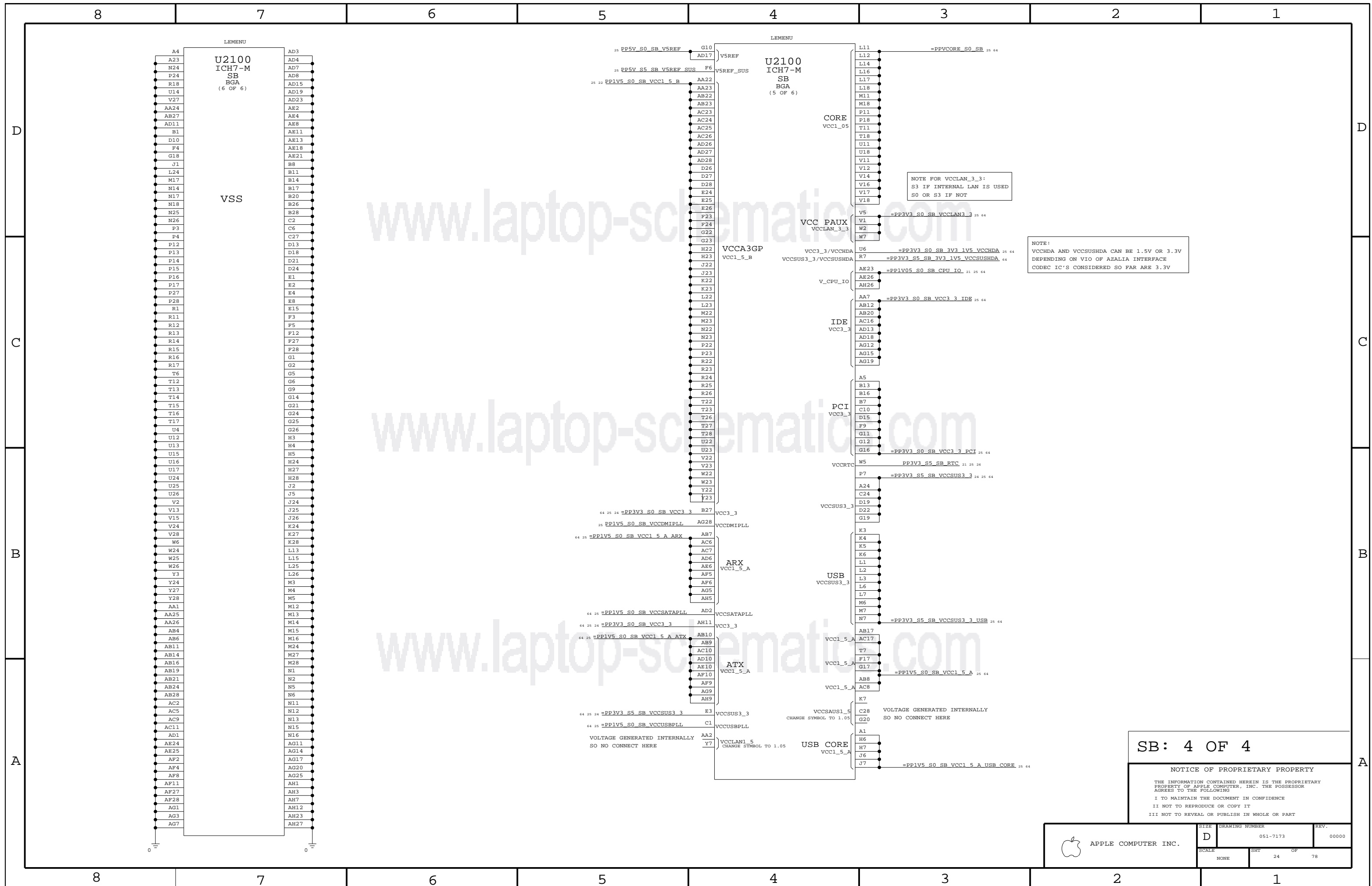
LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

SB: 3 OF 4

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R2312, R2315 and R2389 close to SB

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	D	051-7173	00000
SCALE	NONE	SHT	23 OF 78



NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

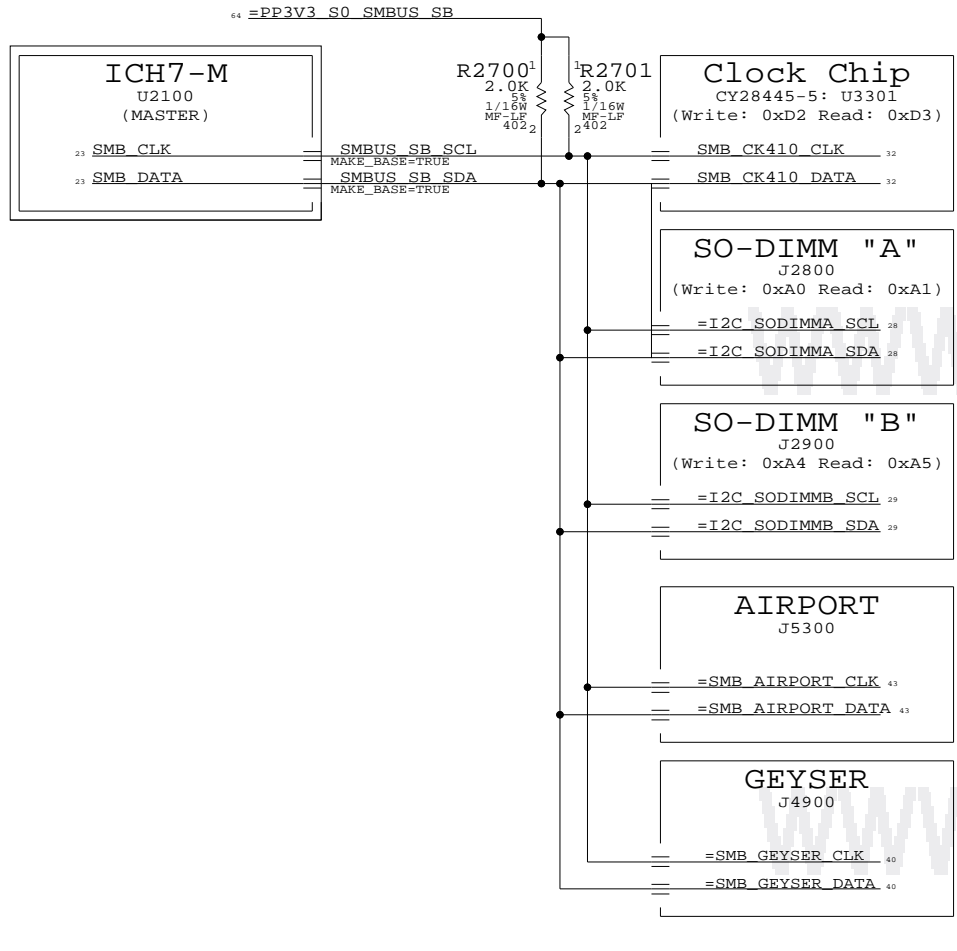
NOTE:
VCC3_3/VCC3_3_IDE AND VCC3_3/VCC3_3_PCI CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

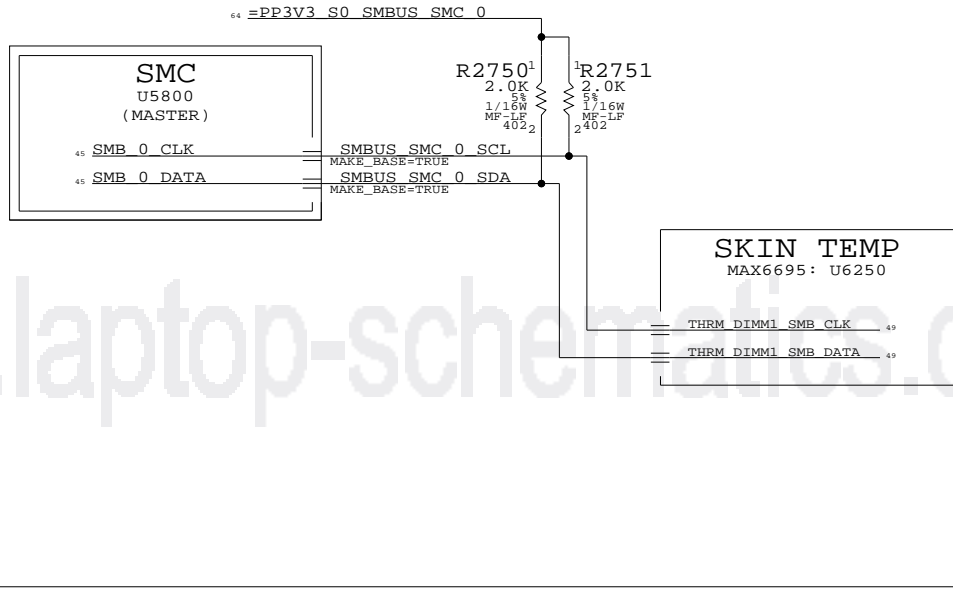
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	D	051-7173	00000
SCALE	SHT		OF
NONE	24		78

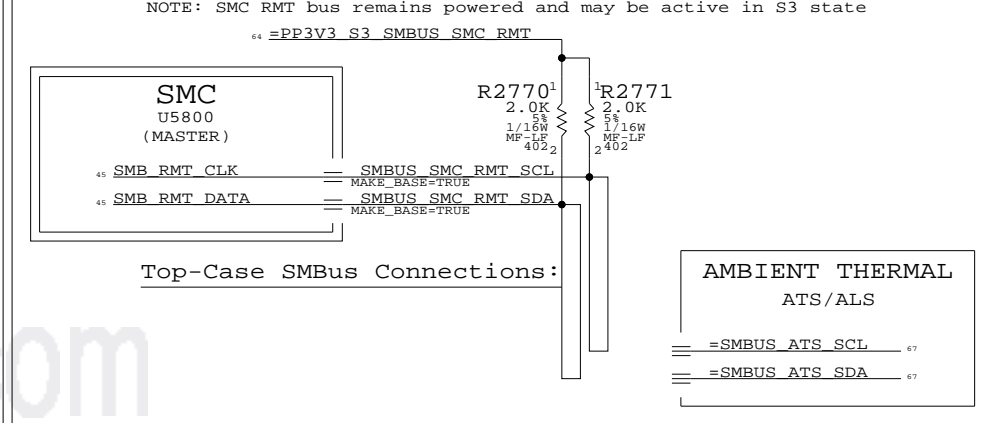
ICH7-M SMBus Connections



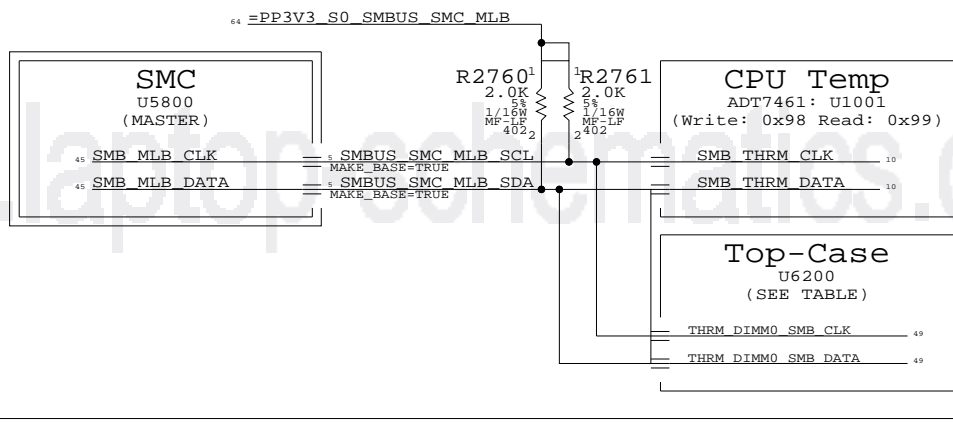
SMC "0" SMBus Connections



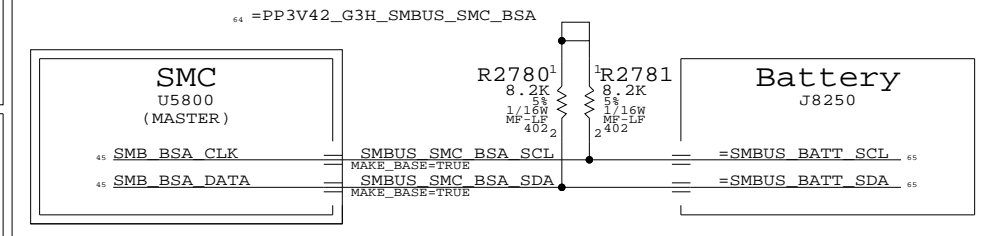
SMC "RMT" SMBus Connections



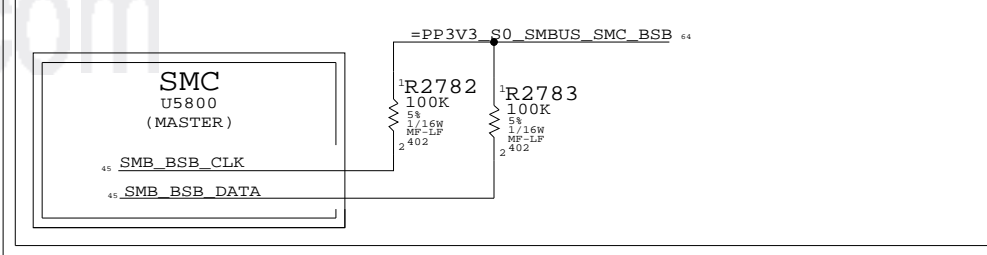
SMC "MLB" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



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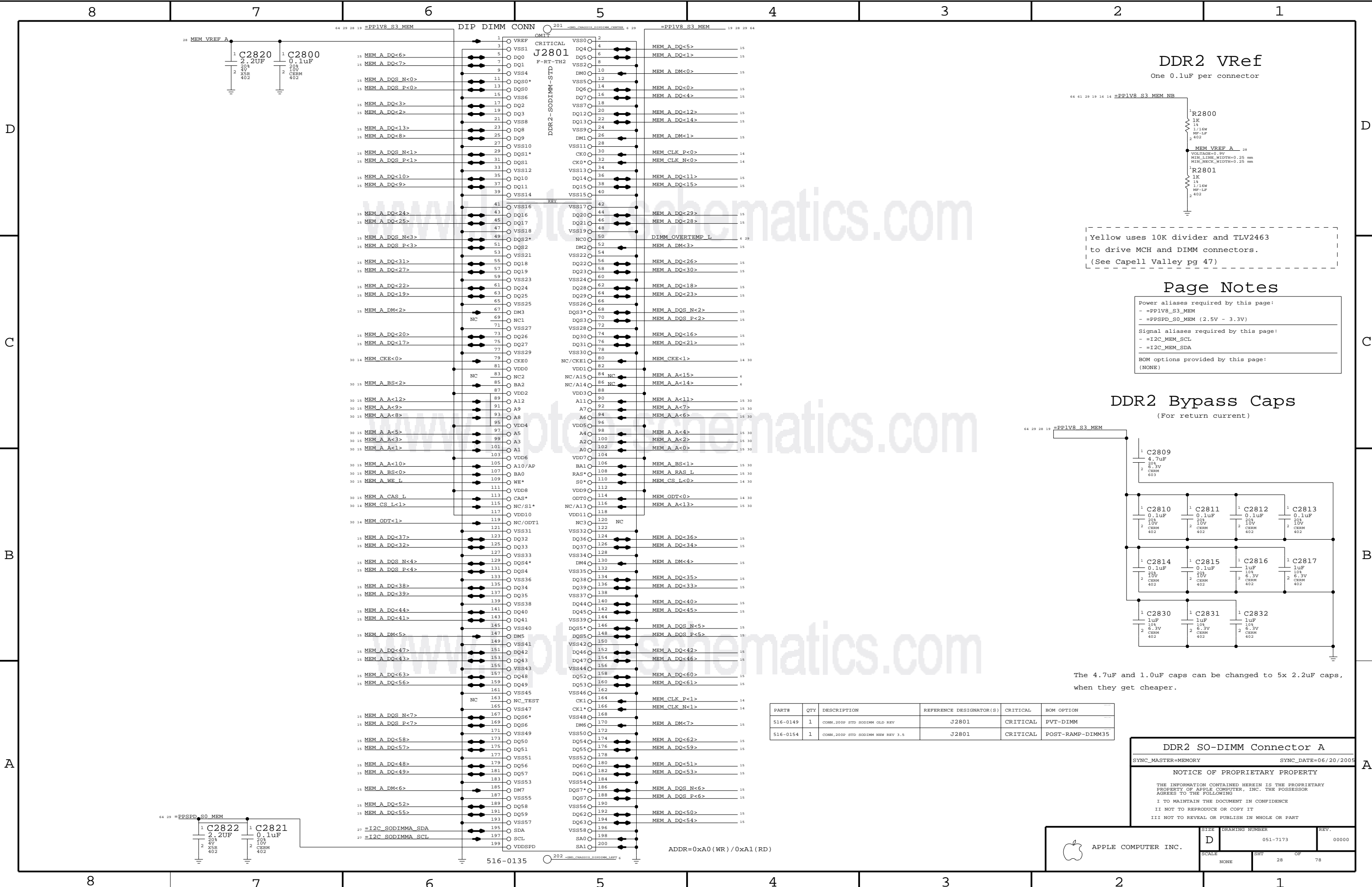
M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

NOTICE OF PROPRIETARY PROPERTY

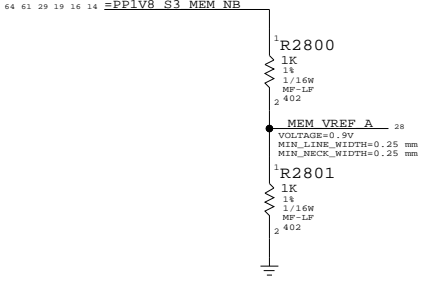
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	D	051-7173	00000
SCALE	NONE	SHT	27 OF 78



DDR2 VRef

One 0.1uF per connector



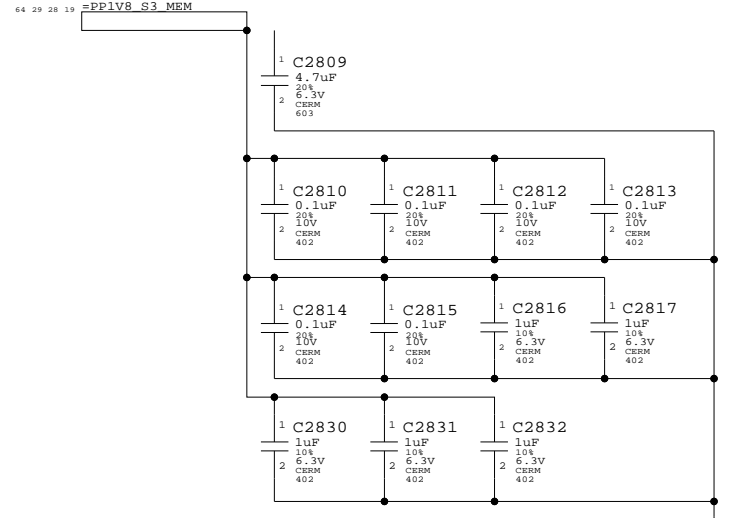
Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

Page Notes

- Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA
- BOM options provided by this page: (NONE)

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN.200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN.200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

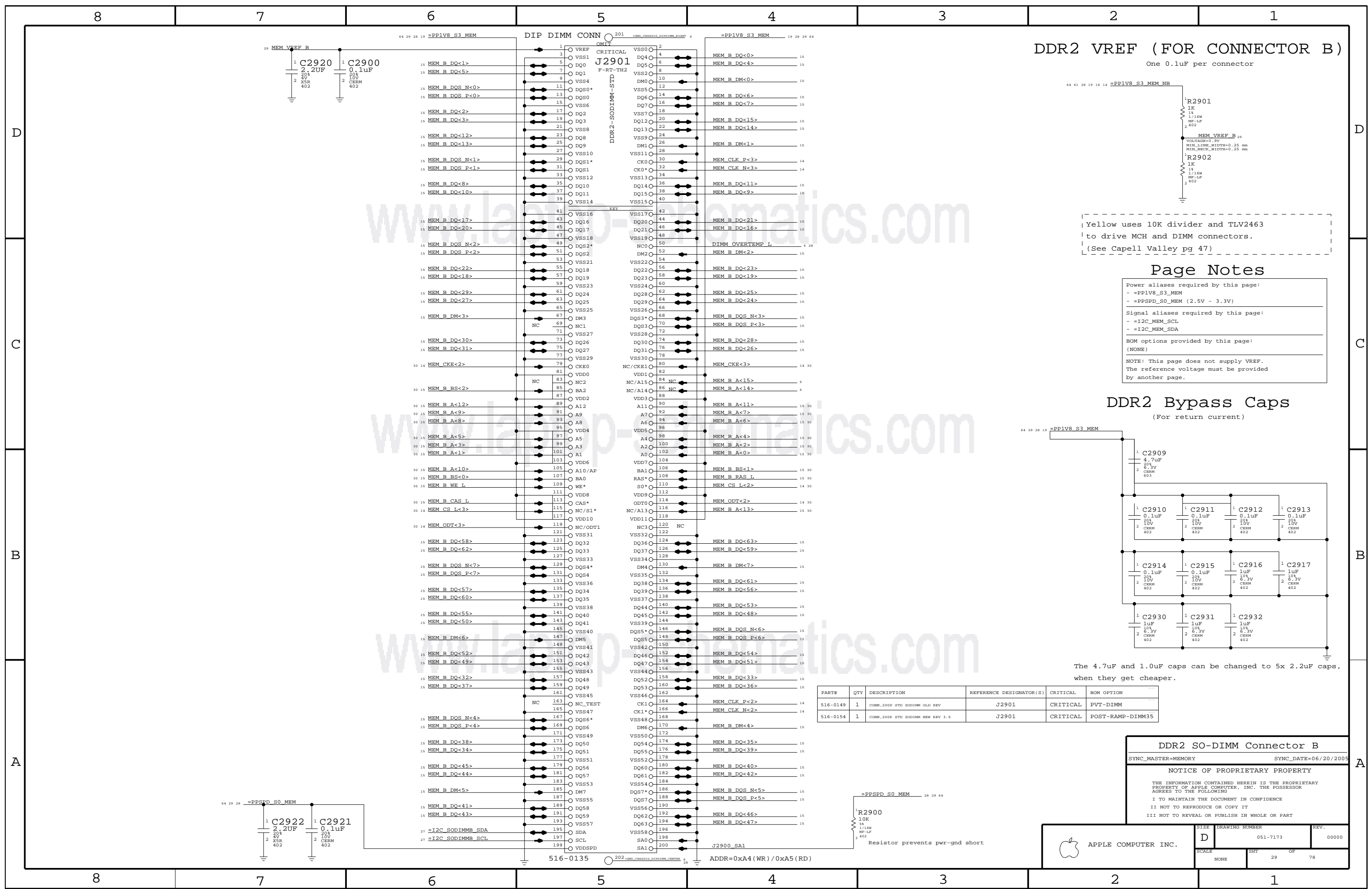
DDR2 SO-DIMM Connector A

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

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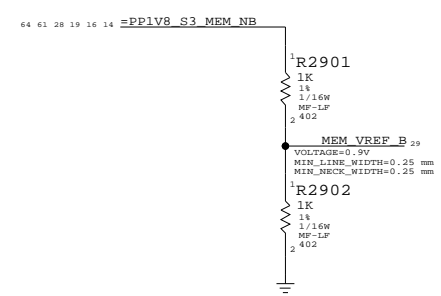
APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7173	00000
	SHT	OF	
	28	78	

ADDR=0xA0 (WR) / 0xA1 (RD)



DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector

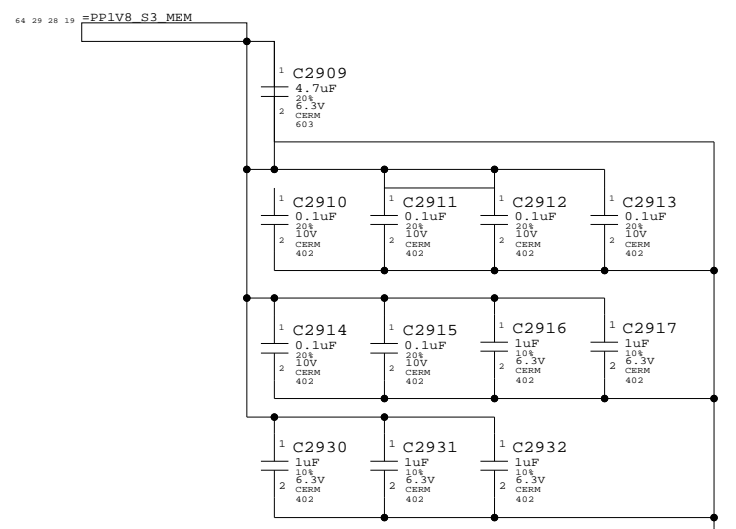


Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

- Power aliases required by this page:
- =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)
- Signal aliases required by this page:
- =I2C_MEM_SCL
 - =I2C_MEM_SDA
- BOM options provided by this page:
- (NONE)
- NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

DDR2 Bypass Caps (For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 1.5	J2901	CRITICAL	POST-RAMP-DIMM35

DDR2 SO-DIMM Connector B

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

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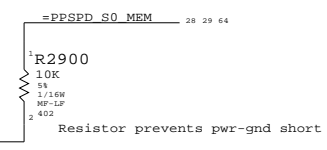
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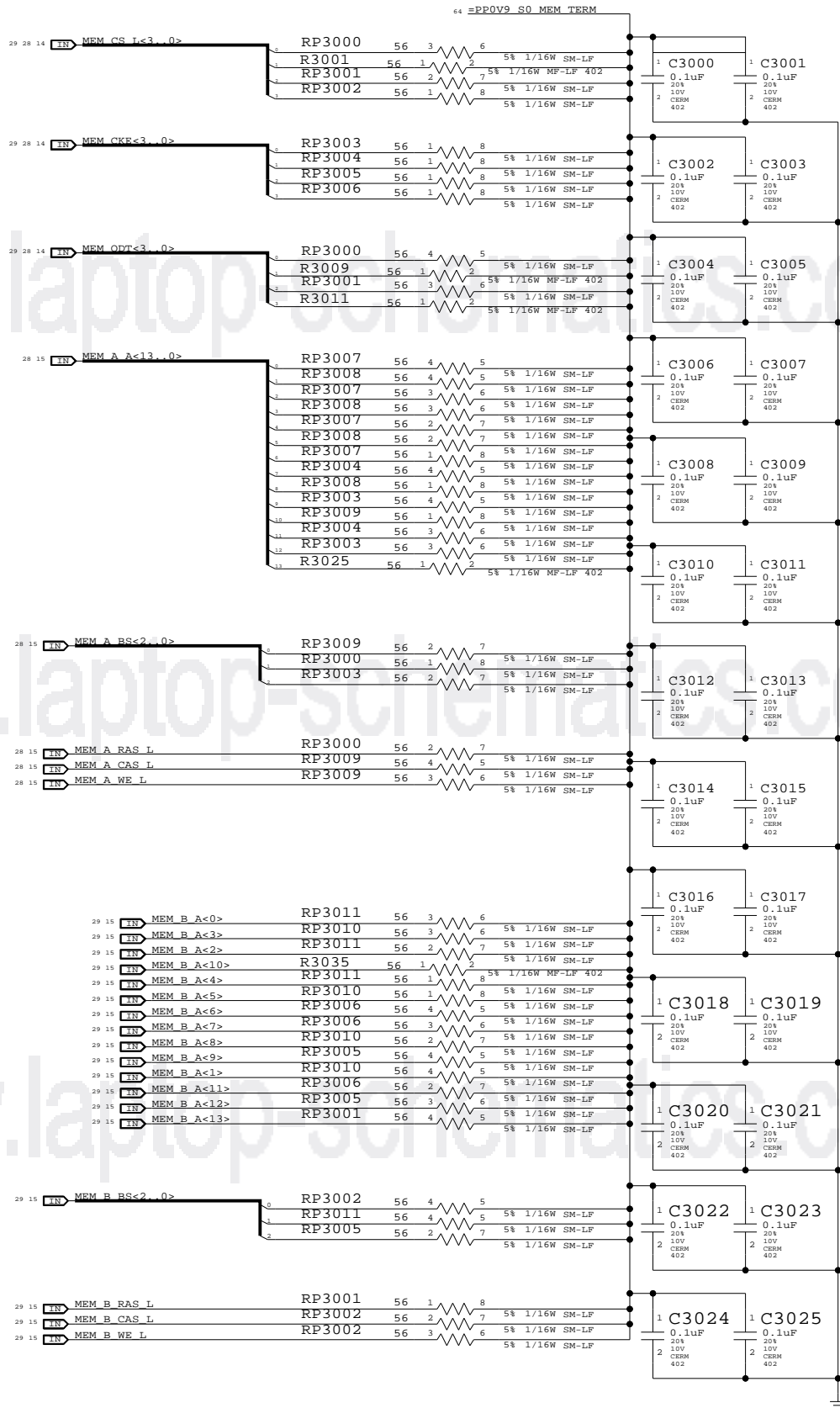
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	NONE	D 051-7173	00000
	SHT	OF	
	29	78	



One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE: PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

NOTICE OF PROPRIETARY PROPERTY

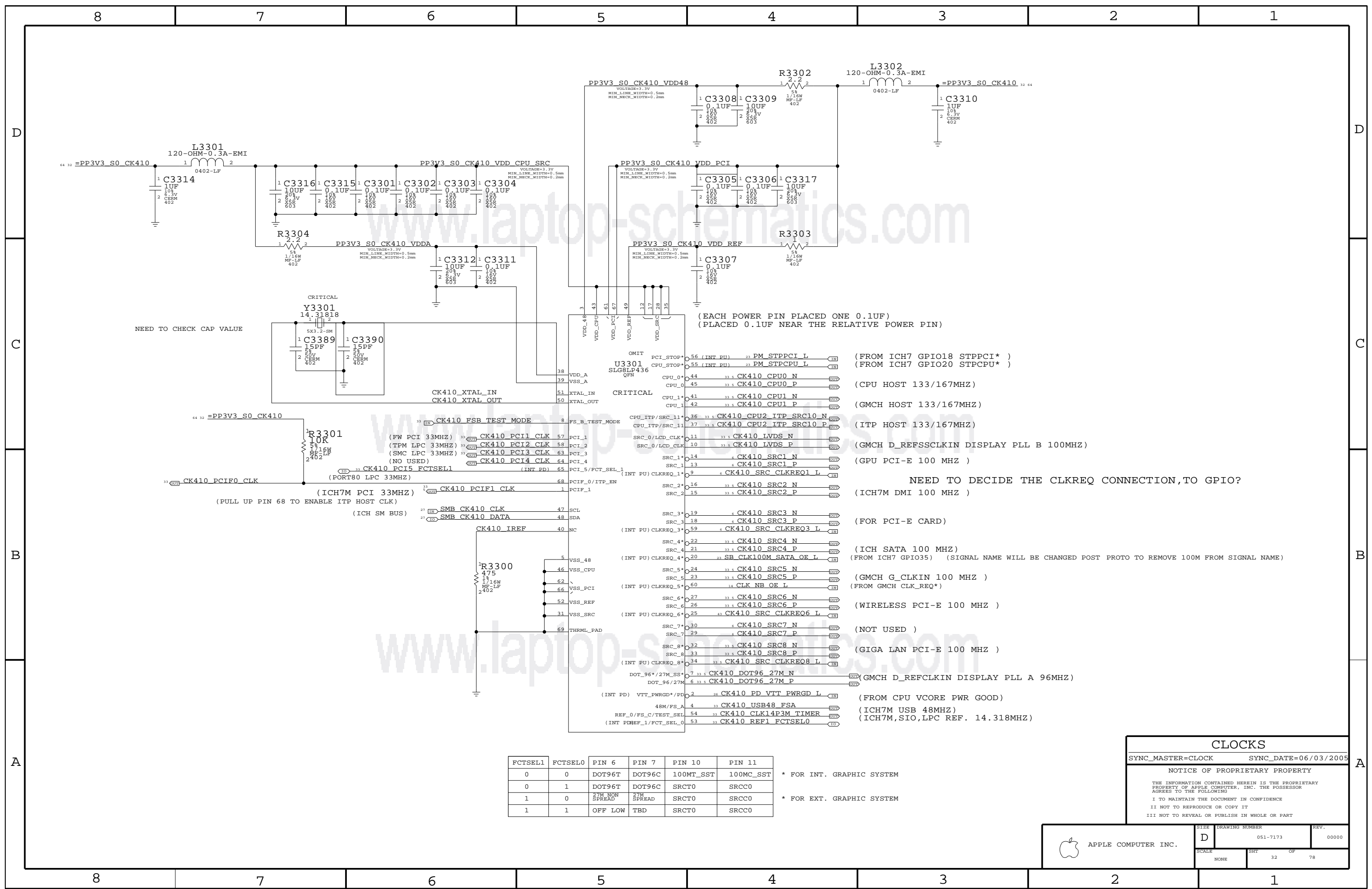
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	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	30	78	



- 56 (INT PU) 23 PM_STPPCI L (FROM ICH7 GPIO18 STPPCI*)
- 55 (INT PU) 23 PM_STPCPU L (FROM ICH7 GPIO20 STPCPU*)
- 44 33 CK410 CPU0 N (CPU HOST 133/167MHZ)
- 45 33 CK410 CPU0 P
- 41 33 CK410 CPU1 N (GMCH HOST 133/167MHZ)
- 42 33 CK410 CPU1 P
- 36 33 CK410 CPU2 ITP_SRC10_N (ITP HOST 133/167MHZ)
- 37 33 CK410 CPU2 ITP_SRC10_P
- 11 33 CK410 LVDS N (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 10 33 CK410 LVDS P
- 14 6 CK410 SRC1 N (GPU PCI-E 100 MHZ)
- 13 6 CK410 SRC1 P
- 9 6 CK410 SRC CLKREQ1 L (NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?)
- 16 33 CK410 SRC2 N (ICH7M DMI 100 MHZ)
- 15 33 CK410 SRC2 P
- 19 6 CK410 SRC3 N (FOR PCI-E CARD)
- 18 6 CK410 SRC3 P
- 59 6 CK410 SRC CLKREQ3 L (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 22 33 CK410 SRC4 N (ICH SATA 100 MHZ)
- 21 33 CK410 SRC4 P
- 20 33 SB_CLK100M_SATA_OE L (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 24 33 CK410 SRC5 N (GMCH G_CLKIN 100 MHZ)
- 23 33 CK410 SRC5 P (FROM GMCH CLK_REQ*)
- 60 14 CLK_NB_OE L (WIRELESS PCI-E 100 MHZ)
- 27 33 CK410 SRC6 N (NOT USED)
- 26 33 CK410 SRC6 P (GIGA LAN PCI-E 100 MHZ)
- 25 43 CK410 SRC CLKREQ6 L (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- 7 33 CK410 DOT96 27M N (FROM CPU VCORE PWR GOOD)
- 6 33 CK410 DOT96 27M P (ICH7M USB 48MHZ)
- 2 26 CK410 PD_VTT_PWRGD L (ICH7M, SIO, LPC REF. 14.318MHZ)
- 4 33 CK410 USB48_FSA
- 54 33 CK410_CLK14P3M_TIMER
- 53 33 CK410_REF1_FCTSEL0

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
 * FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

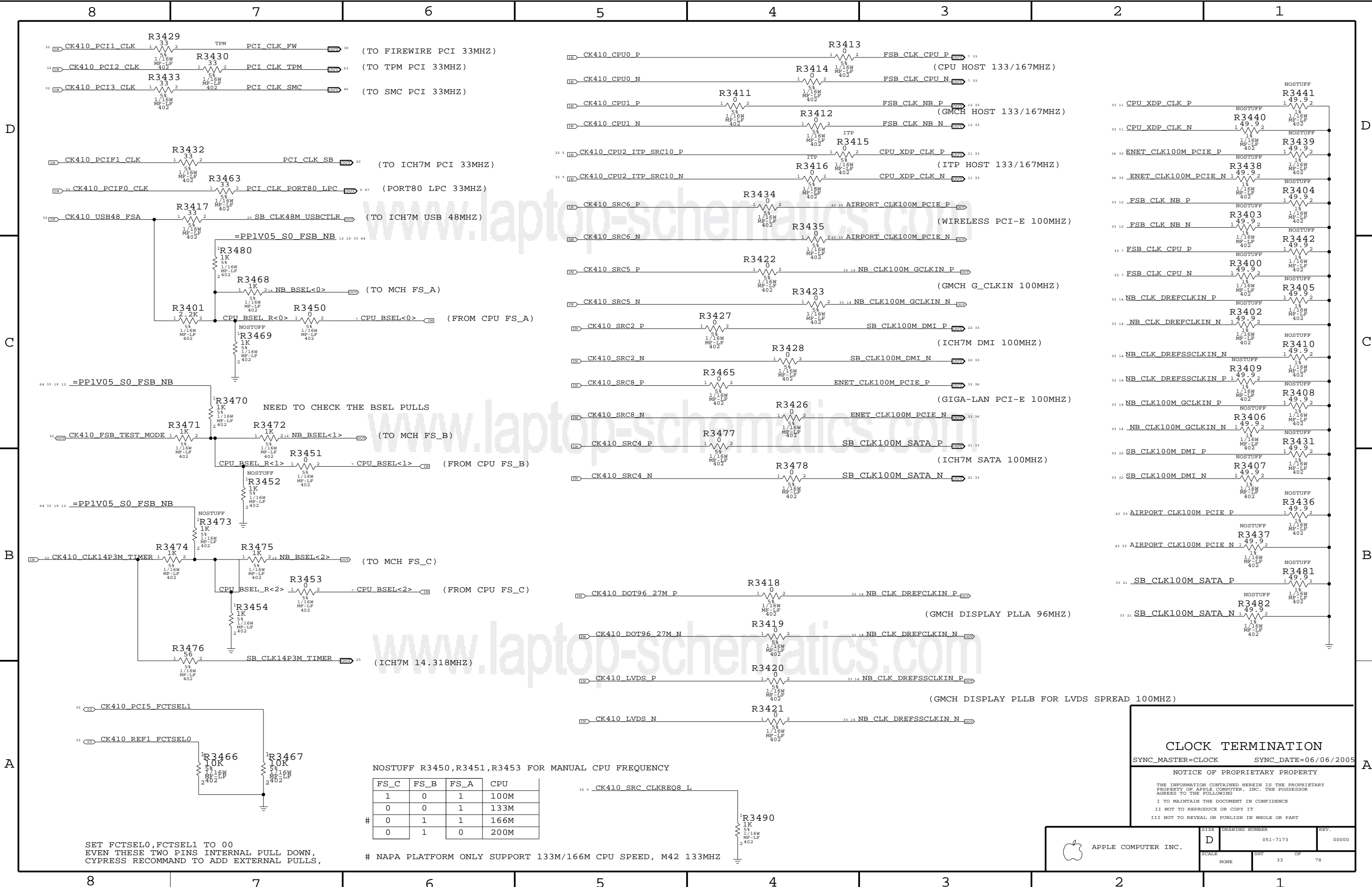
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D	051-7173	00000
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CLOCK TERMINATION
 SYNC_MASTER=CLOCK SYNC_DATE=06/06/2005
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NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

FS_C	FS_B	FS_A	CPU
1	0	1	100M
0	0	1	133M
0	1	1	166M
0	1	0	200M

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ

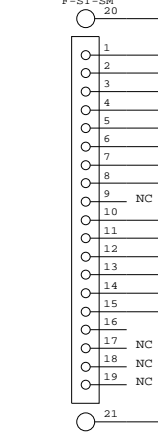
SET FCTSEL0,FCTSEL1 TO 00
 EVEN THESE TWO PINS INTERNAL PULL DOWN,
 CYPRESS RECOMMEND TO ADD EXTERNAL PULLS,

APPLE COMPUTER INC.	SCALE	DRAWING NUMBER	REV.
	NONE	D 051-7173	00000
	SHT	33	OF 78

SATA CONNECTOR

518S0390

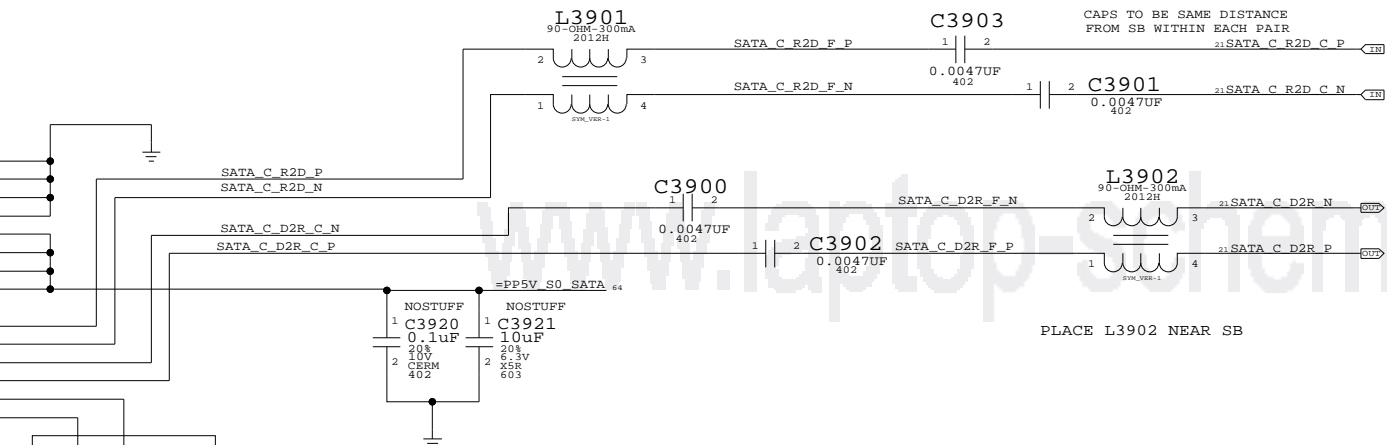
CRITICAL
J3901
20247-019E
F-ST-20



Place L3901 near J3901

VALUE=3900PF IN REFERENCE SCHEM

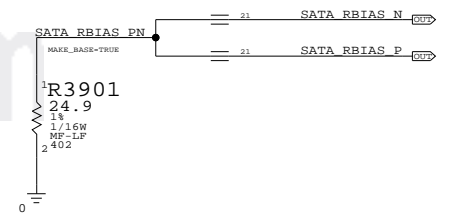
CAPS TO BE SAME DISTANCE FROM SB WITHIN EACH PAIR



R3900

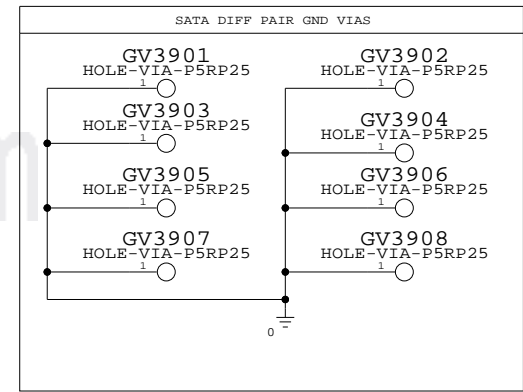
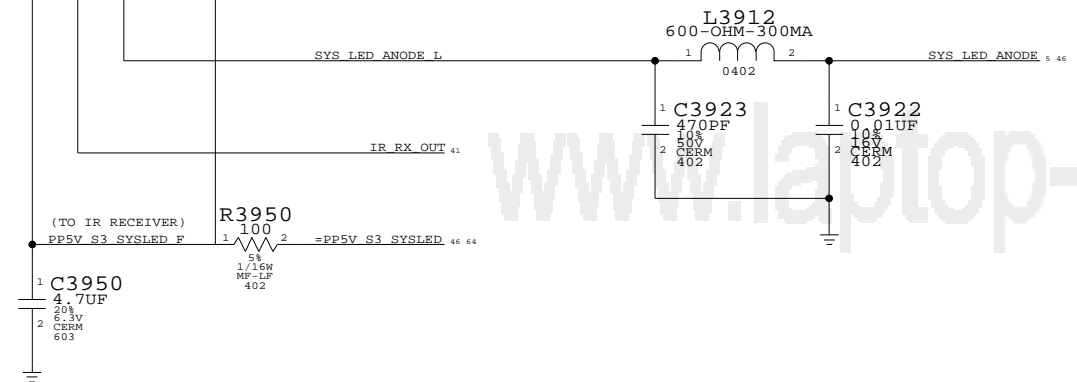


PLACE NEAR ICH7 PIN



PLACE L3902 NEAR SB

SYSTEM (SLEEP) LED FILTER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
155S0227	155S0164	?	L3901, L3902	KEEP MAG. LAYER IN BOM

SATA CONNECTOR

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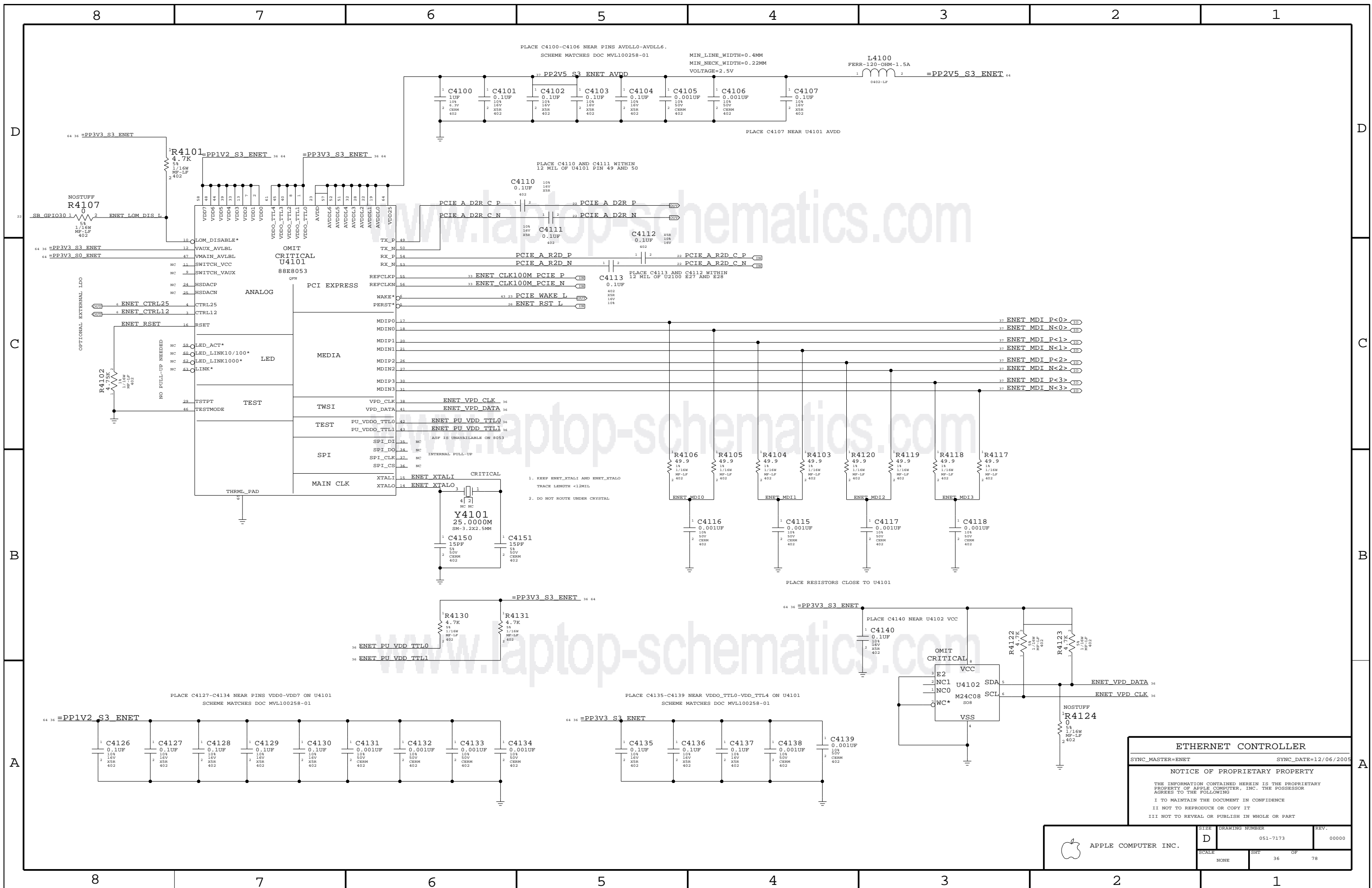
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SCALE	NONE	SHT	35 OF 78



ETHERNET CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=12/06/2005

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	D	051-7173	00000
SCALE		SHT	OF
NONE		36	78

D

D

C

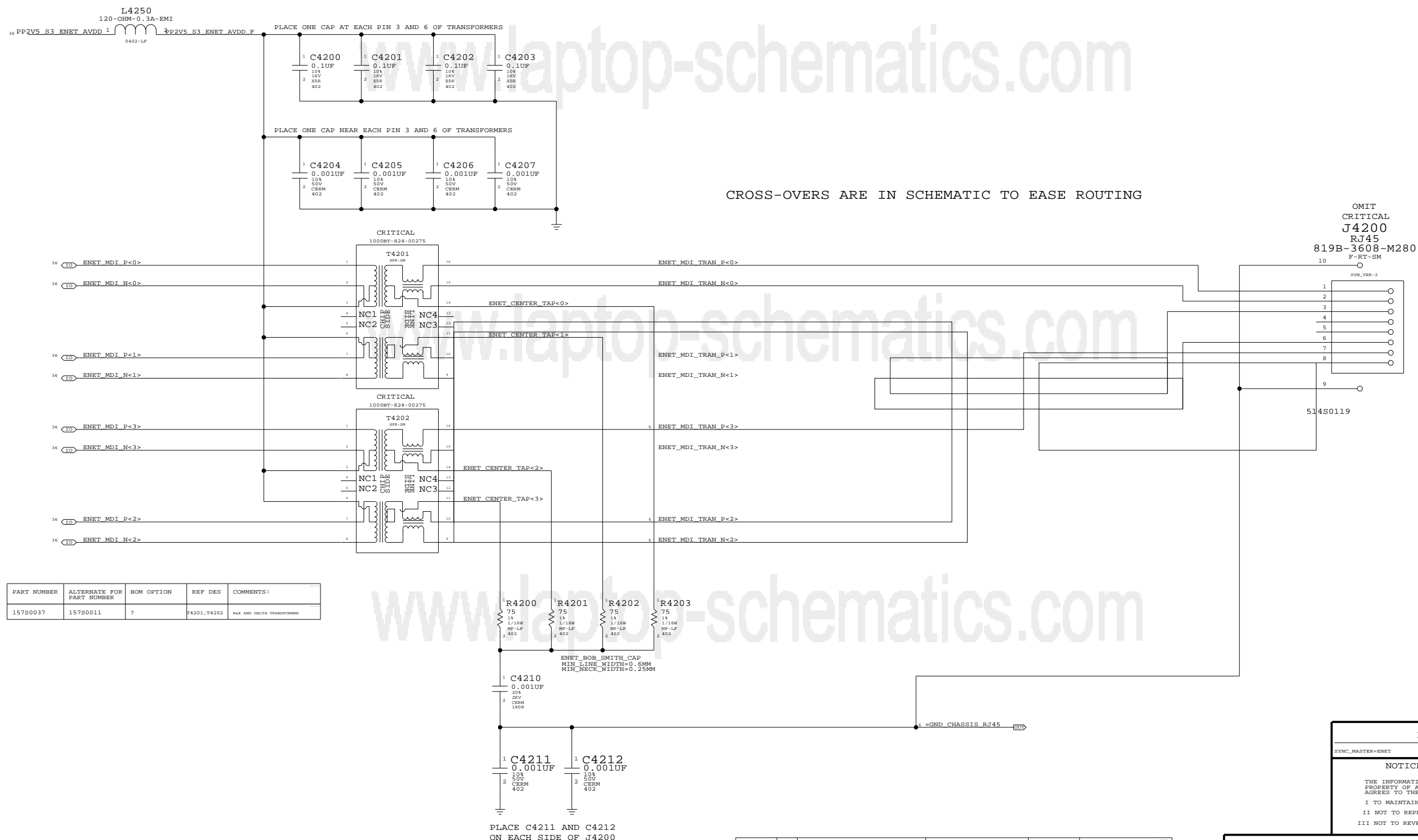
C

B

B

A

A



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
157S0037	157S0011	?	T4201, T4202	SEE AHD DELTA TRANSFORMER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN, SP RJ-45 JACK, MIDDLE PLANE, BK3, LP	J4200	CRITICAL	NORMAL
514S0144	1	CONN, SP RJ-45 JACK, MIDDLE PLANE, BLACK, LP	J4200	CRITICAL	FANCY

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 37	OF 78

ETHERNET CONNECTOR

SYNC_MASTER-ENET SYNC_DATE=11/14/2005

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PAGE NOTES

INPUT
=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

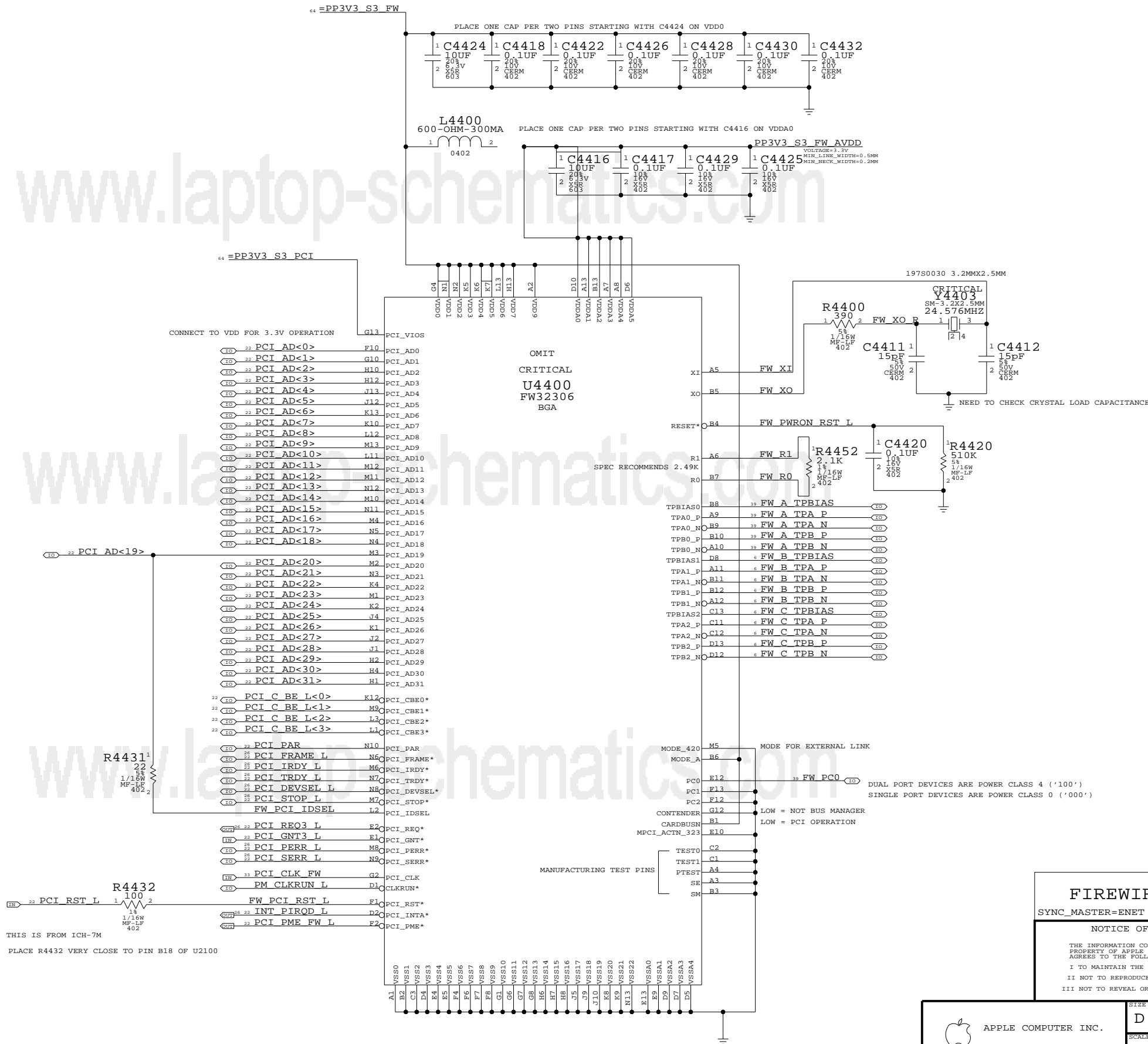
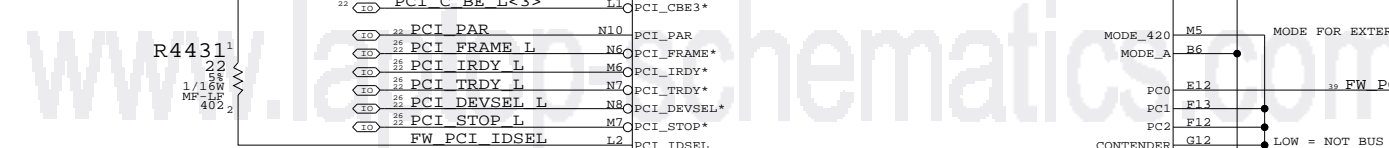
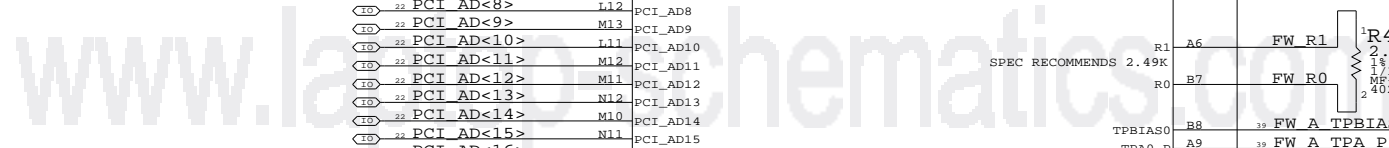
OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - CHANGED CLK_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP



THIS IS FROM ICH-7M
PLACE R4432 VERY CLOSE TO PIN B18 OF U2100

FIREWIRE CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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Table with columns for Drawing Number (D 051-7173), Scale (NONE), Sheet (38 OF 78), and Revision (00000). Includes Apple Computer Inc. logo.

Page Notes

INPUT:
 =PPBUS_S5_FW - PORT POWER
 =PP3V3_S5_FW - DIGITAL POWER
 =GND_CHASSIS_FW_PORT0 - CHASSIS GROUND
 =FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:
 FW_TPA0_P/N,FW_TPB0_P/N,FW_TPBIA0 - FIREWIRE DIFF PAIRS

OUTPUT:
 FW_PCO - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

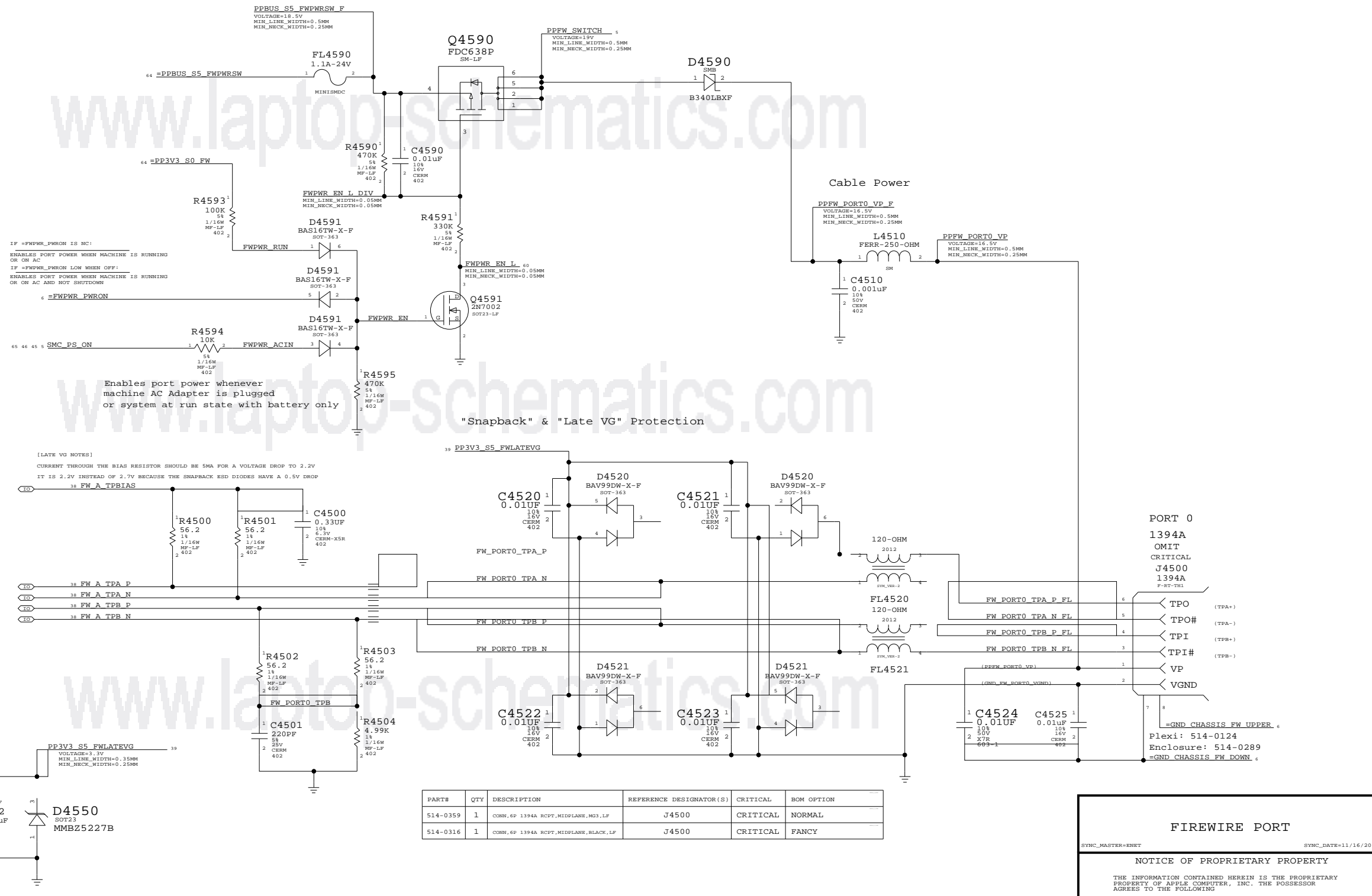
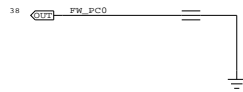
PAGE HISTORY

5/19/05 - INITIAL REVISION
 6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
 6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
 6/22/05 - CONNECTED FW_PCO FOR SINGLE PORT
 7/26/05 - UPDATED LATE-VG POWER BALL CIRCUIT FROM M1
 7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
 7/26/05 - SWITCHED TO 514-0124 FOR FIREWIRE CONNECTOR
 7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
 7/26/05 - CHANGED FL4590 TO 1.1A VERSION
 7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
 7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
 FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT
 1 FOR DUAL PORT



FIREWIRE PORT

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

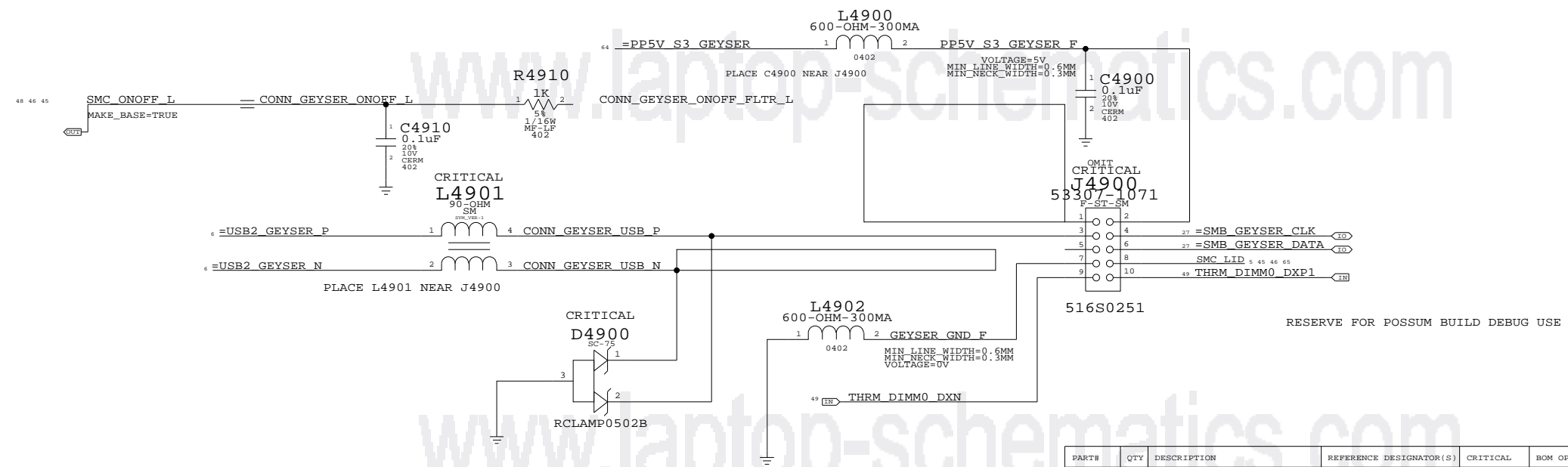
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	D	051-7173	00000
SCALE	SHT	OF	78
NONE		39	

GEYSER AND DIMMO REMOTE TEMP SENSORS

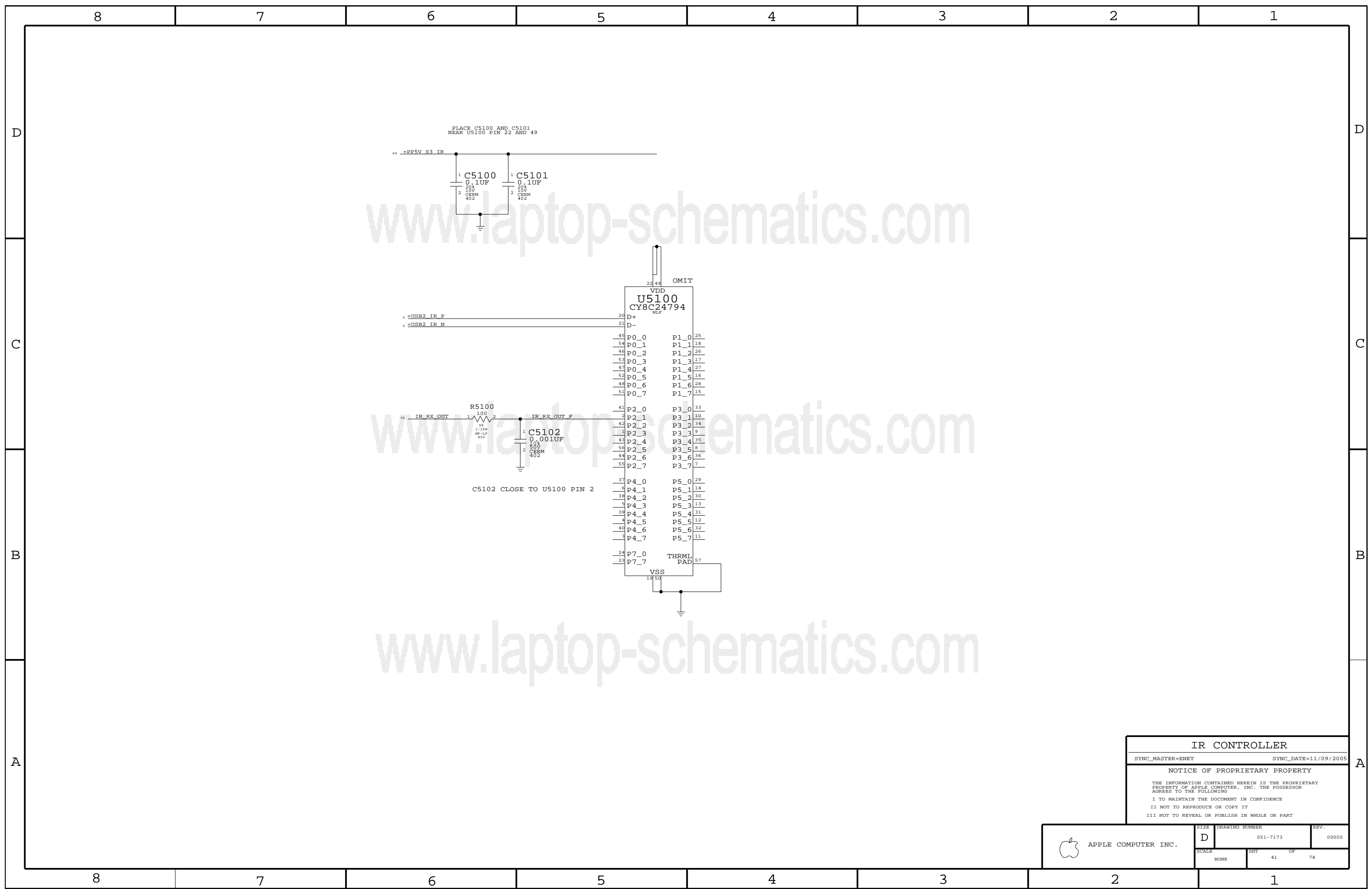


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY

CONNECTOR MISC
 SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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	SCALE: NONE	SHEET: 40	OF: 78



IR CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=11/09/2005

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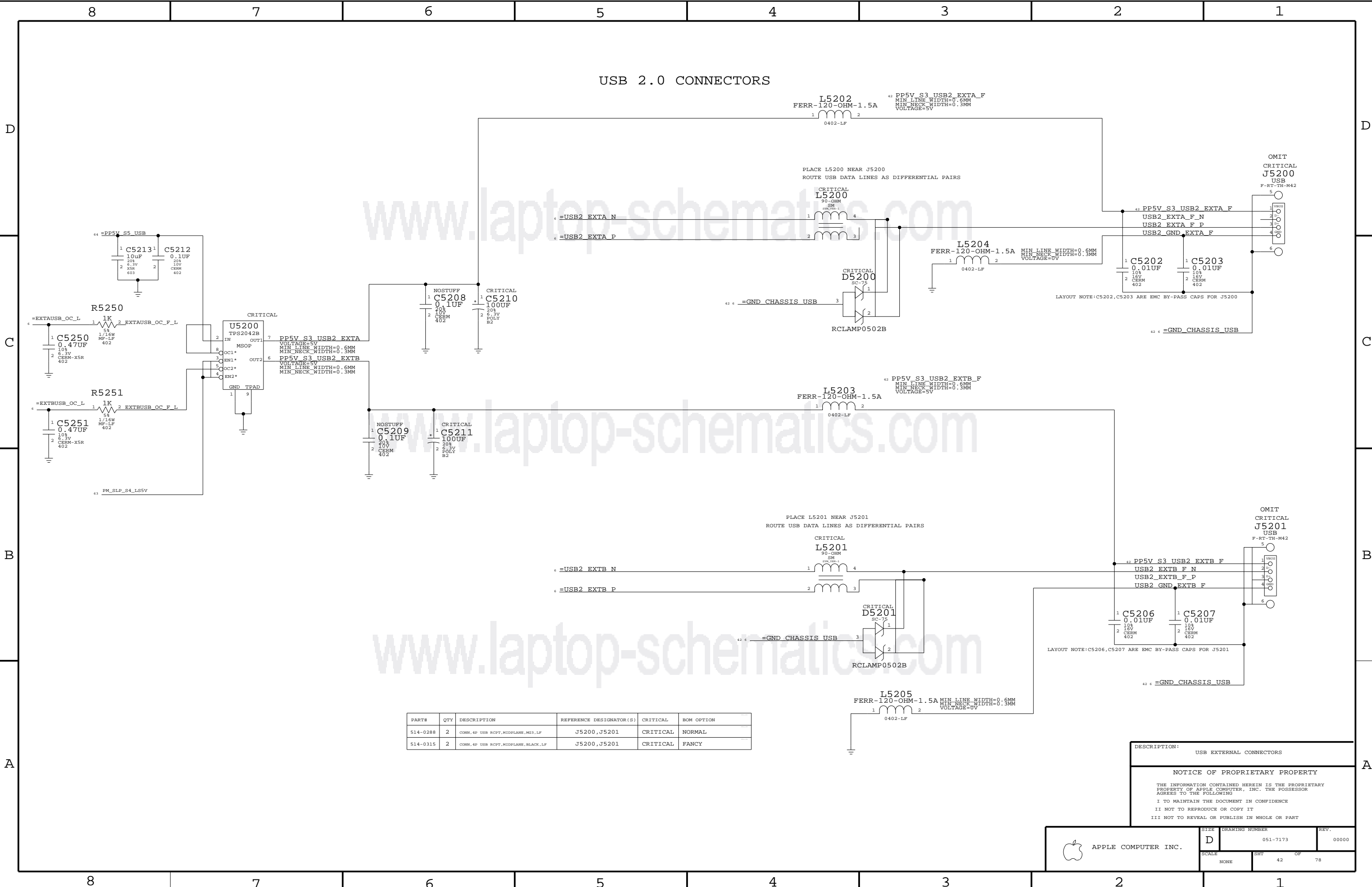
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 41	OF 78

USB 2.0 CONNECTORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN, 4P USB RCPT, MIDPLANE, W3, LF	J5200, J5201	CRITICAL	NORMAL
514-0315	2	CONN, 4P USB RCPT, MIDPLANE, BLACK, LF	J5200, J5201	CRITICAL	FANCY

DESCRIPTION:
USB EXTERNAL CONNECTORS

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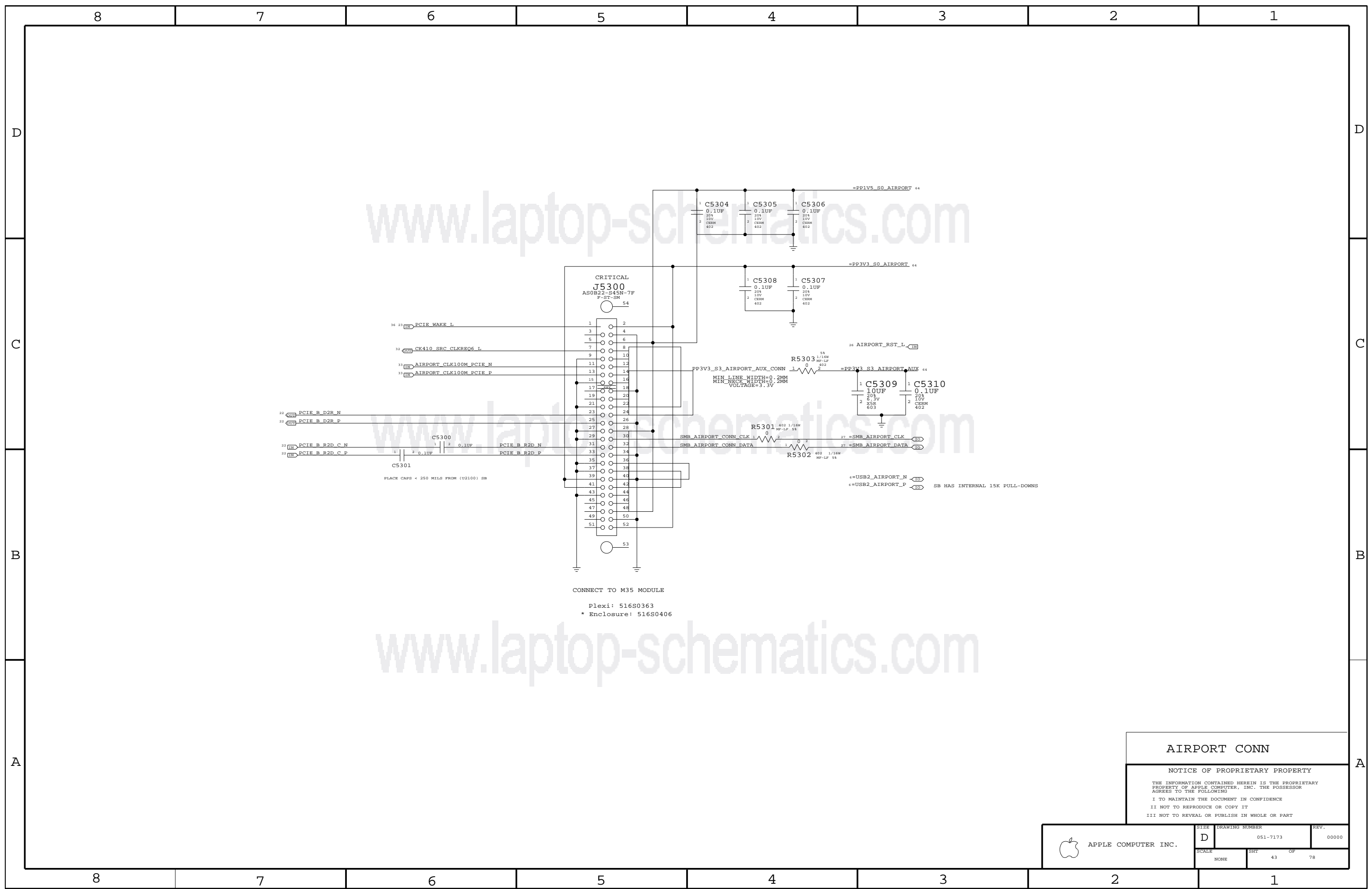
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APPLE COMPUTER INC.

SCALE	SHT	OF	REV.
NONE	42	78	00000



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AIRPORT CONN

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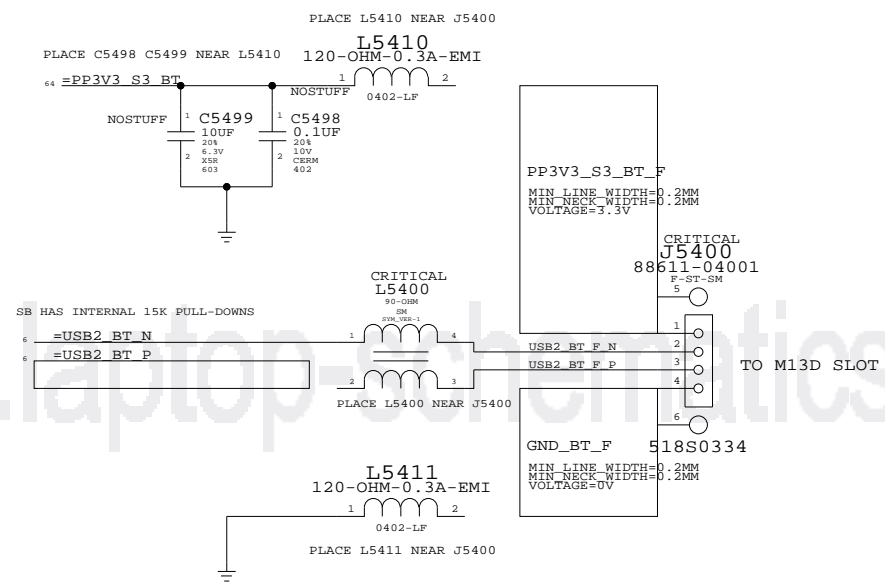
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 43	OF 78

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BLUETOOTH INTERFACE

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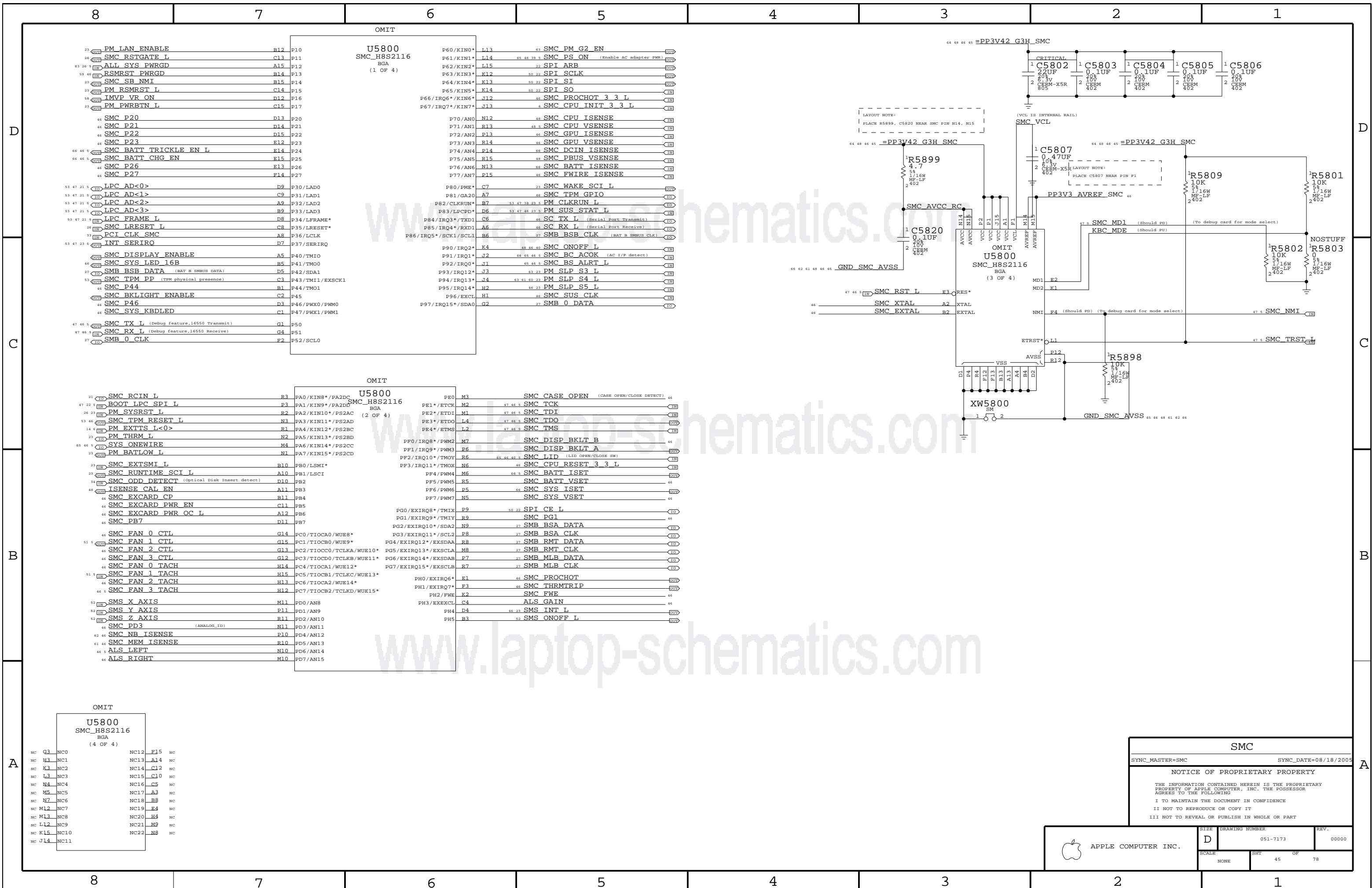
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	D	051-7173	00000
SCALE	SHT	OF	
NONE	44	78	



8 7 6 5 4 3 2 1

D

C

B

A

8 7 6 5 4 3 2 1

OMIT

U5800
SMC_H8S2116
BGA
(1 OF 4)

P60/KIN0*	L13	43	SMC PM G2 EN	OUT
P61/KIN1*	L14	65 46 39 8	SMC PS ON (Enable AC adapter PMR)	OUT
P62/KIN2*	L15	23	SPI ARB	OUT
P63/KIN3*	K12	50 22	SPI SCLK	OUT
P64/KIN4*	K13	50 22	SPI SI	OUT
P65/KIN5*	K14	50 22	SPI SO	OUT
P66/IRQ6*/KIN6*	J12	46	SMC PROCHOT 3 3 L	IN
P67/IRQ7*/KIN7*	J13	46	SMC CPU INIT 3 3 L	IN
P70/AN0	N12	46	SMC CPU ISENSE	IN
P71/AN1	R13	46 8	SMC CPU VSENSE	IN
P72/AN2	P13	46	SMC GPU ISENSE	IN
P73/AN3	R14	46	SMC GPU VSENSE	IN
P74/AN4	P14	46	SMC DCIN ISENSE	IN
P75/AN5	R15	46	SMC PBUS VSENSE	IN
P76/AN6	N13	46	SMC BATT ISENSE	IN
P77/AN7	P15	46	SMC FWIRE ISENSE	IN
P80/PME*	C7	23	SMC WAKE SCI L	OUT
P81/GA20	A7	46	SMC TPM GPIO	IO
P82/CLKRUN*	B7	53 47 38 23 8	PM CLRUN L	IO
P83/LPCPD*	D6	53 47 46 27 8	PM SUS STAT L	IO
P84/IRQ3*/TXD1	C6	46	SC TX L (Serial Port Transmit)	IO
P85/IRQ4*/RXD1	A6	46	SC RX L (Serial Port Receive)	IO
P86/IRQ5*/SCK1/SCL1	B6	27	SMB BSB CLK (BAT B SMBUS CLK)	IO
P90/IRQ2*	K4	46 46 46	SMC ONOFF L	IN
P91/IRQ1*	J2	66 65 46 8	SMC BC ACOK (AC I/P detect)	IN
P92/IRQ0*	J1	65 46 8	SMC BS ALRT L	IN
P93/IRQ12*	J3	63 21	PM SLP S3 L	IN
P94/IRQ13*	J4	63 61 60 21	PM SLP S4 L	IN
P95/IRQ14*	H2	46 21	PM SLP S5 L	IN
P96/EXCL	H1	46	SMC SUS CLK	IN
P97/IRQ15*/SDA0	G2	27	SMB 0 DATA	IO

OMIT

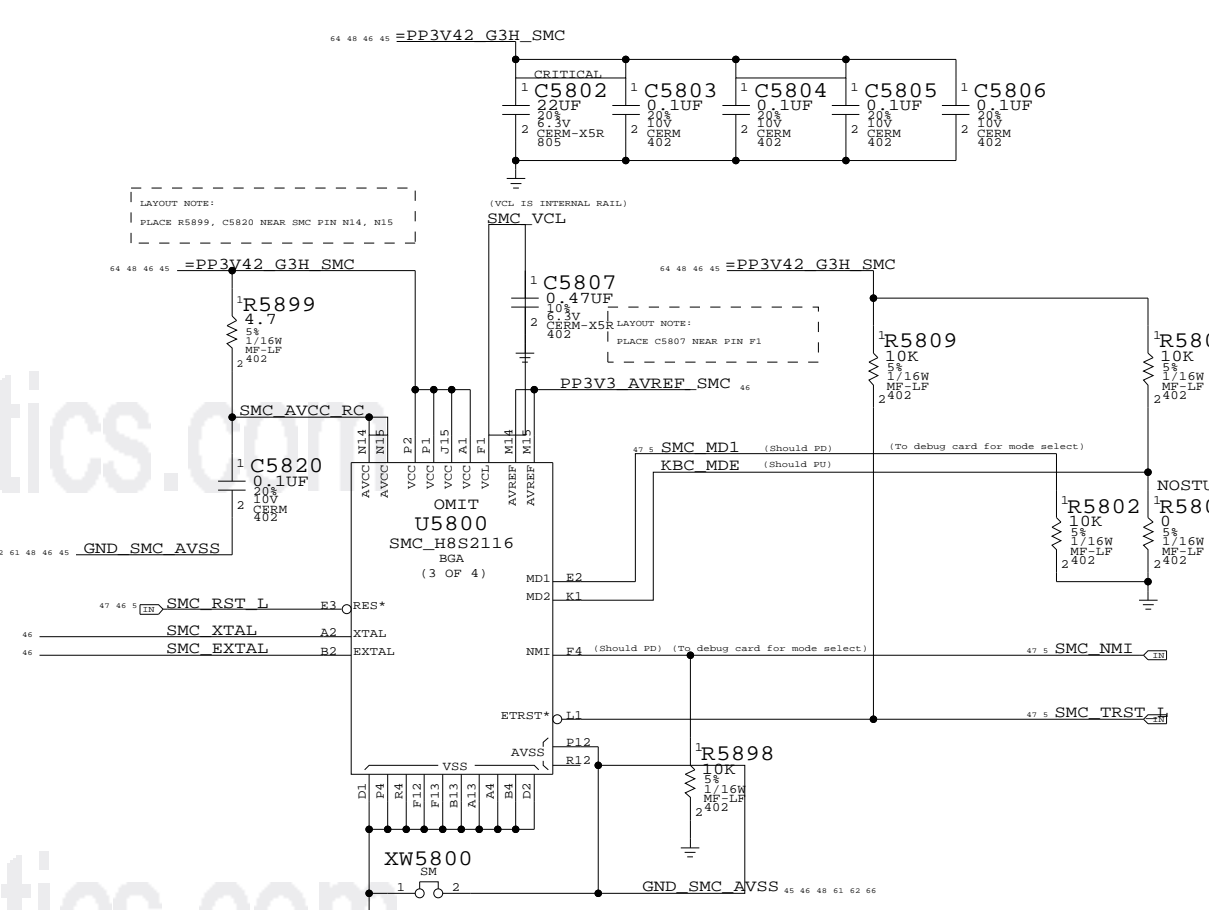
U5800
SMC_H8S2116
BGA
(2 OF 4)

PE0	M3	46	SMC CASE OPEN (CASE OPEN/CLOSE DETECT)	OUT
PE1*/ETCK	M2	47 46 5	SMC TCK	OUT
PE2*/ETDI	M1	47 46 5	SMC TDI	OUT
PE3*/ETDO	L4	47 46 5	SMC TDO	OUT
PE4*/ETMS	L2	47 46 5	SMC TMS	OUT
PF0/IRQ8*/PWM2	M7	46	SMC DISP BKLT B	OUT
PF1/IRQ9*/PWM3	P6	46	SMC DISP BKLT A	OUT
PF2/IRQ10*/TMOY	R6	65 46 40 5	SMC LID (LID OPEN/CLOSE SW)	OUT
PF3/IRQ11*/TMOX	N6	46	SMC CPU RESET 3 3 L	OUT
PF4/PWM4	M6	66 5	SMC BATT ISET	OUT
PF5/PWM5	R5	46	SMC BATT VSET	OUT
PF6/PWM6	P5	46	SMC SYS ISET	OUT
PF7/PWM7	N5	46	SMC SYS VSET	OUT
PG0/EXIRQ8*/TMIX	P9	50 22	SPI CE L	OUT
PG1/EXIRQ9*/TMIX	R9	46	SMC PG1	OUT
PG2/EXIRQ10*/SDA2	N9	27	SMB BSA DATA	IO
PG3/EXIRQ11*/SCL2	P8	27	SMB BSA CLK	IO
PG4/EXIRQ12*/EXSDAA	RR	27	SMB RMT DATA	IO
PG5/EXIRQ13*/EXSCLA	M8	27	SMB RMT CLK	IO
PG6/EXIRQ14*/EXSDAB	P7	27	SMB MLB DATA	IO
PG7/EXIRQ15*/EXSCLB	R7	27	SMB MLB CLK	IO
PH0/EXIRQ6*	E1	46	SMC PROCHOT	OUT
PH1/EXIRQ7*	F3	46	SMC THRMTRIP	OUT
PH2/FWE	K2	46	SMC FWE	OUT
PH3/EXEXCL	C4	46	ALS GAIN	OUT
PH4	D4	46 23	SMS INT L	OUT
PH5	B3	62	SMS ONOFF L	OUT

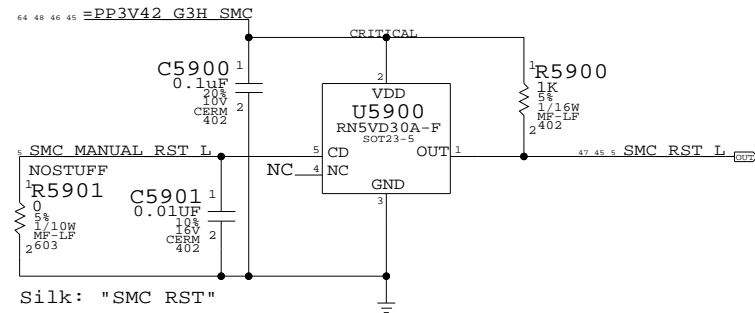
OMIT

U5800
SMC_H8S2116
BGA
(4 OF 4)

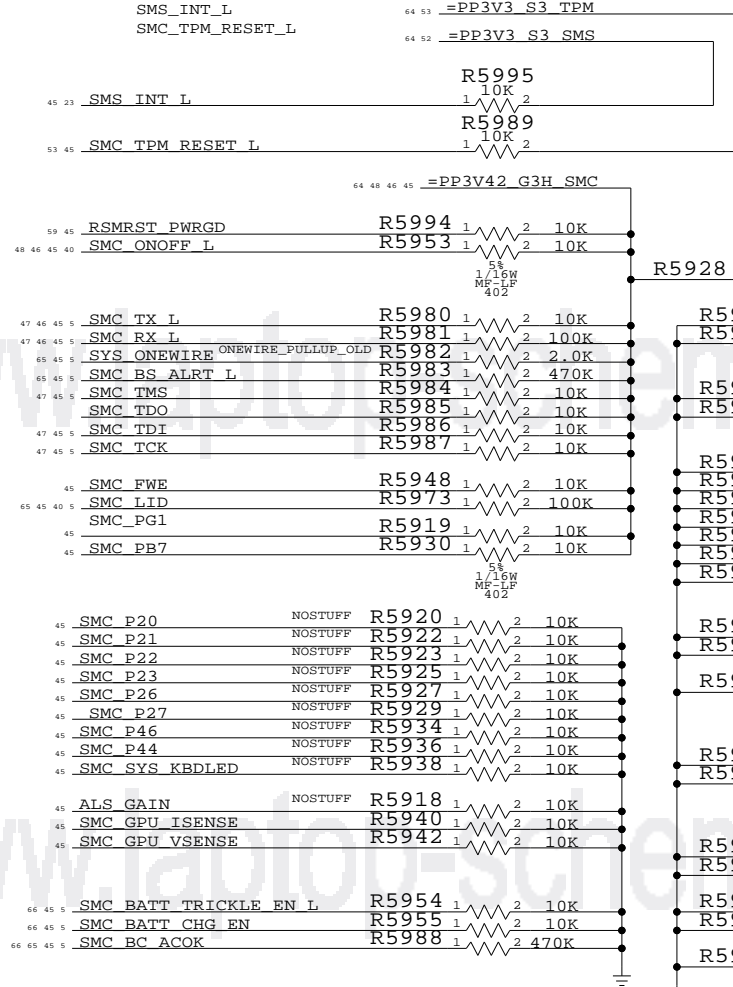
NC12	E15	NC
NC13	A14	NC
NC14	C12	NC
NC15	C10	NC
NC16	C5	NC
NC17	A3	NC
NC18	B8	NC
NC19	E4	NC
NC20	H4	NC
NC21	M9	NC
NC22	N8	NC



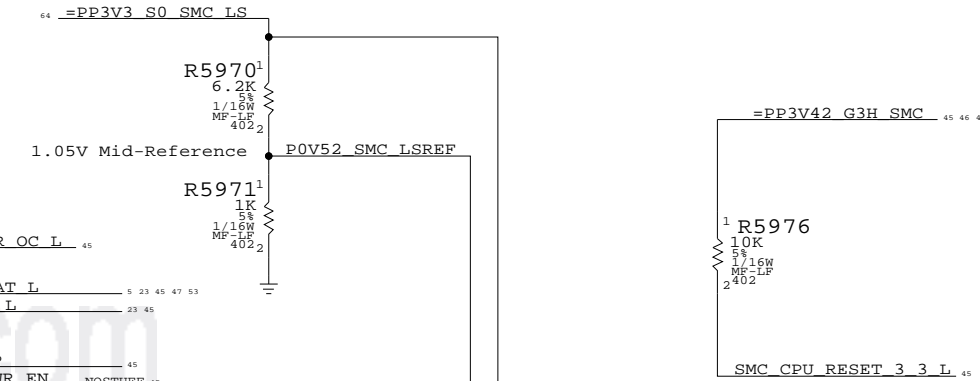
SMC Reset Button / Brownout Detect



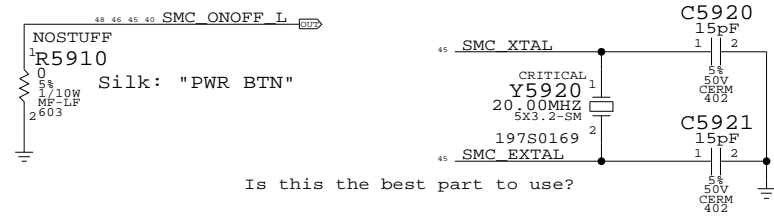
THESE NEED TO BE PULLED TO THE PROPER RAIL:



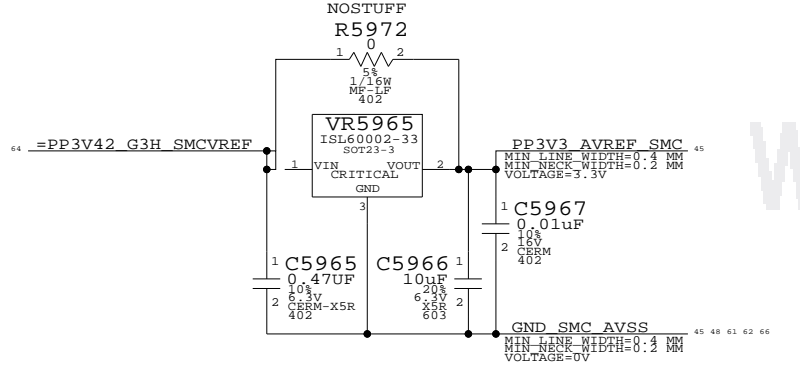
SMC 1.05V to 3.3V Level Shifting



Debug Power Button SMC Crystal Circuit

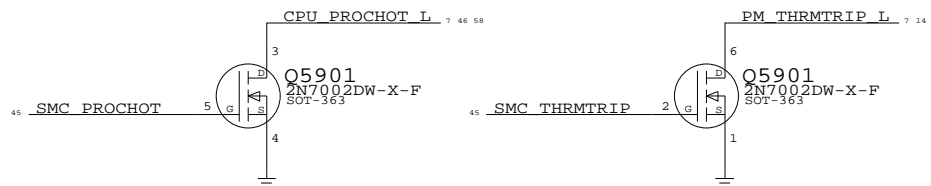


SMC AVREF Supply

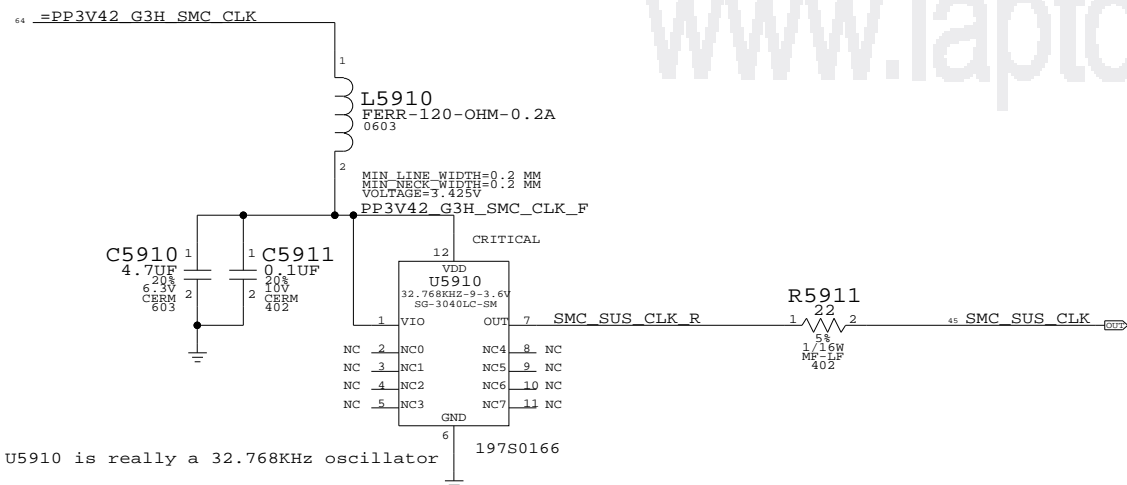


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

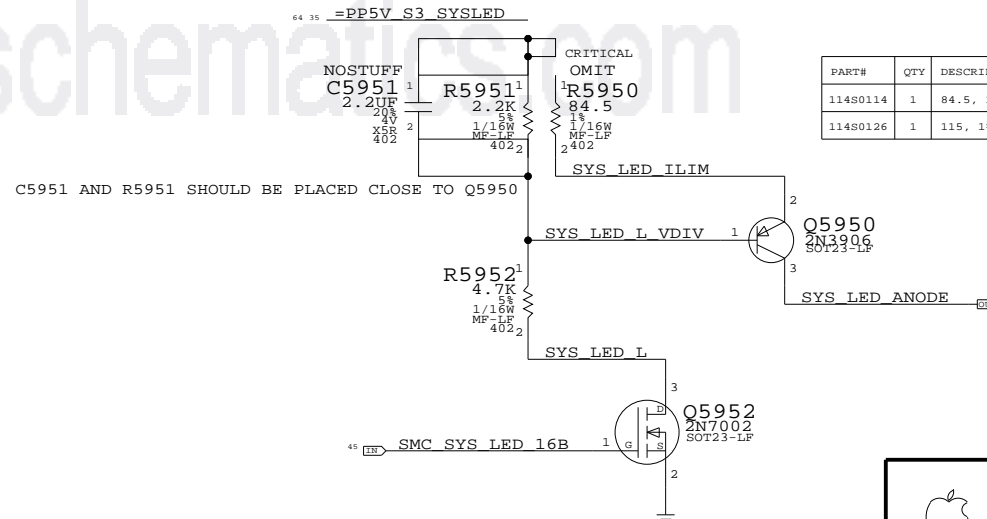
SMC 3.3V to 1.05V Level Shifting



SMC G3HOT OSCILLATOR



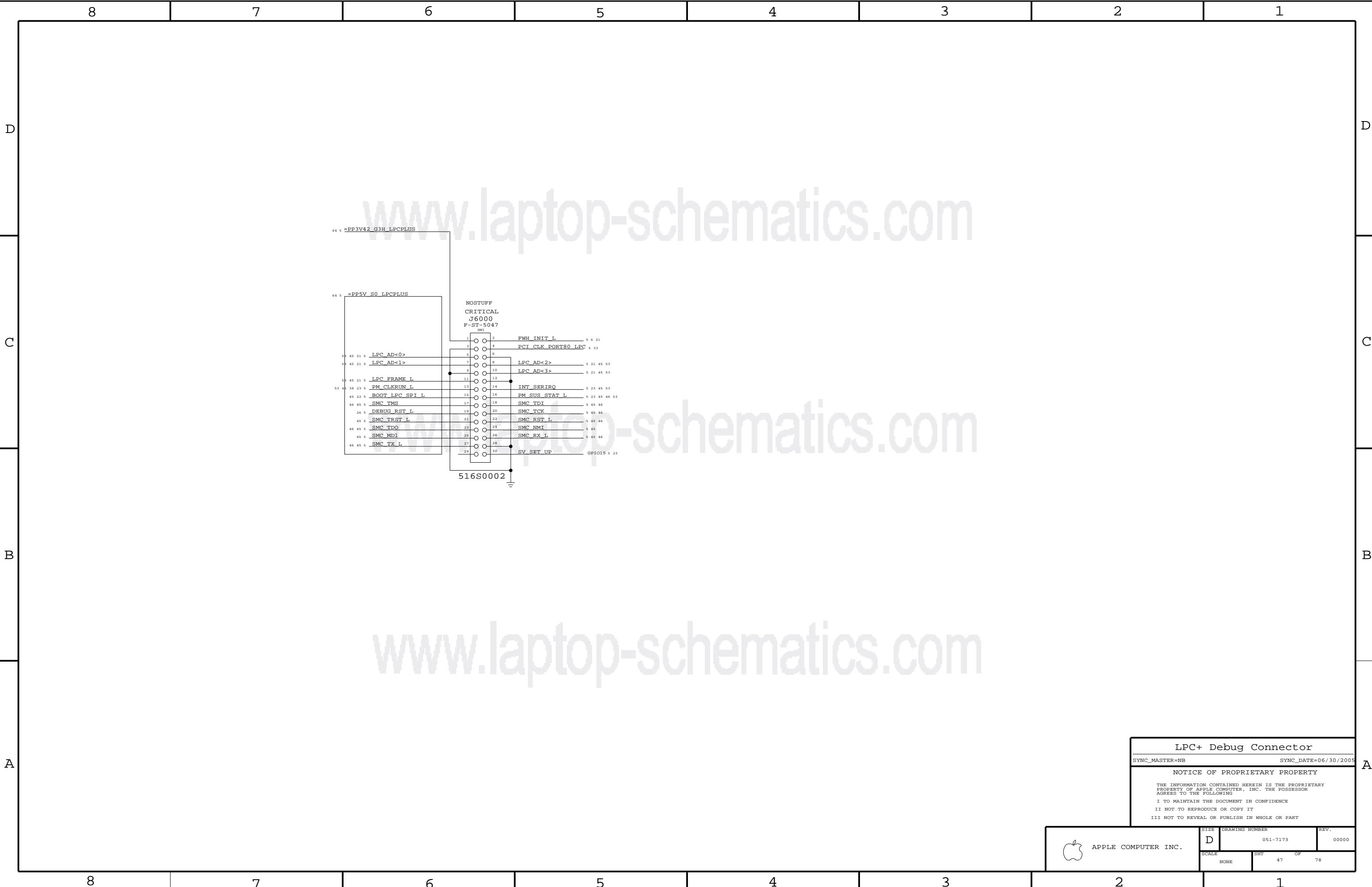
System (Sleep) LED Circuit



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480114	1	84.5, 18, 1/16W, MF-LF, 402	R5950	NORMAL
11480126	1	115, 18, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT
 SYNC_MASTER=SMC SYNC_DATE=08/23/2005
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 REV: 00000



LPC+ Debug Connector

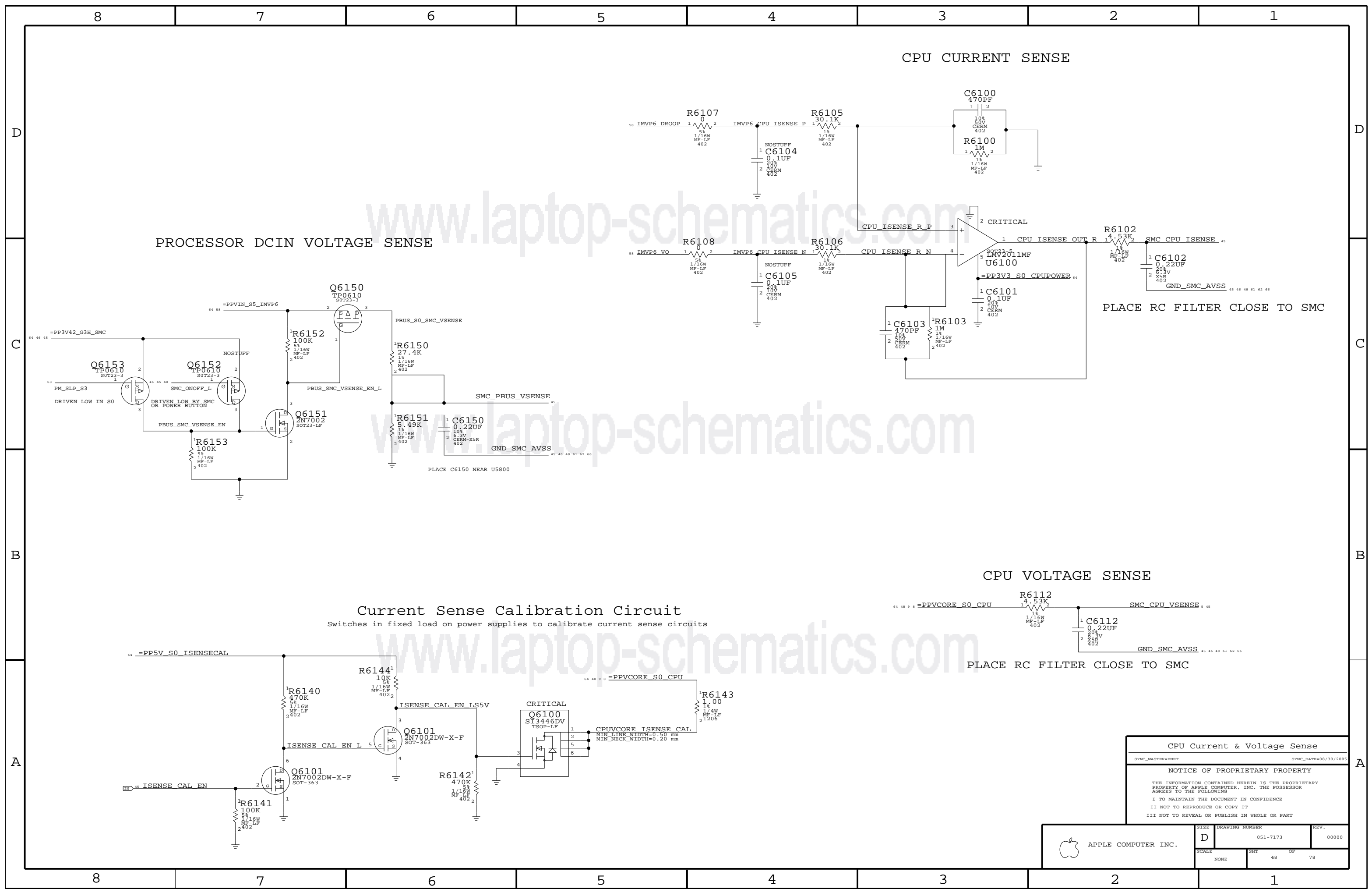
SYNC_MASTER=NB SYNC_DATE=06/30/2005

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	SCALE NONE	SHEET 47	OF 78



PROCESSOR DCIN VOLTAGE SENSE

CPU CURRENT SENSE

CPU VOLTAGE SENSE

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

PLACE RC FILTER CLOSE TO SMC

PLACE C6150 NEAR U5800

PLACE RC FILTER CLOSE TO SMC

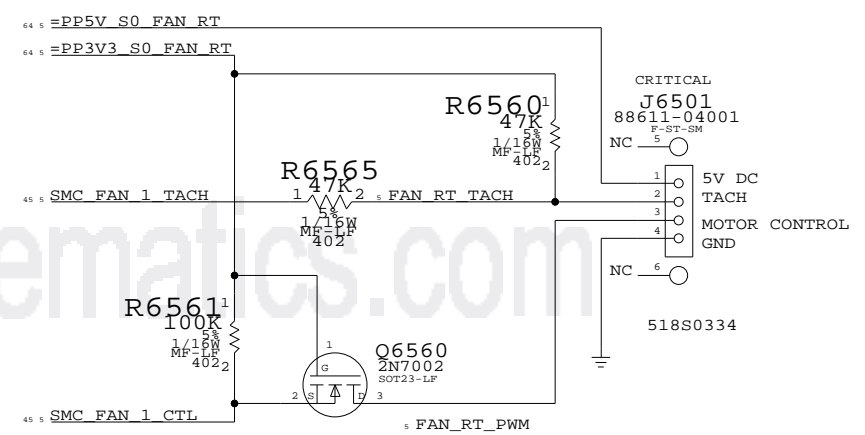
CPU Current & Voltage Sense
 SYNC_MASTER=EMBT SYNC_DATE=08/30/2005
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SCALE	SHT	OF	REV.
NONE	48	78	

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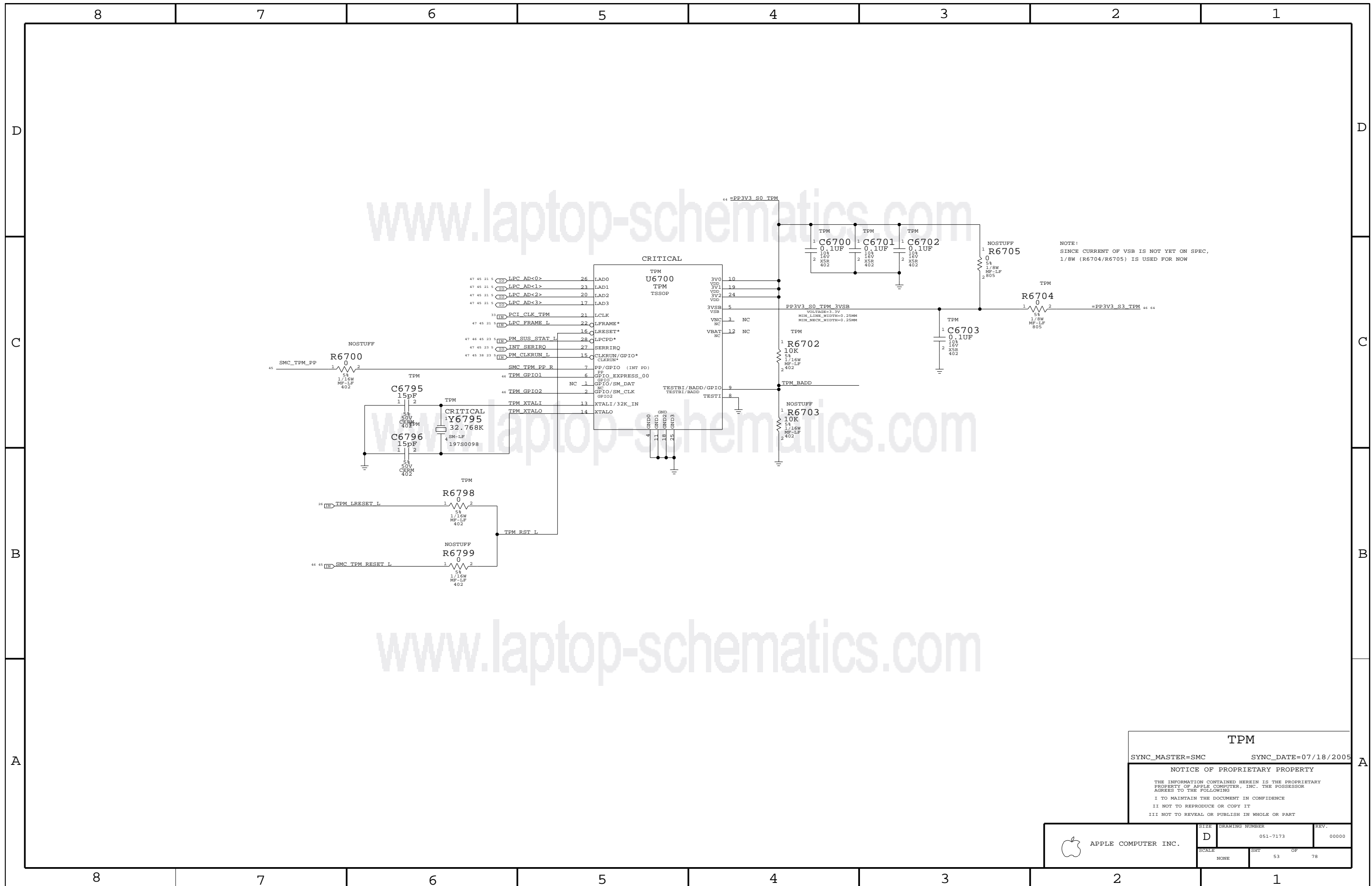
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Fan
SYNC_MASTER=ENET SYNC_DATE=11/10/2005
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NONE	51	78	



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NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

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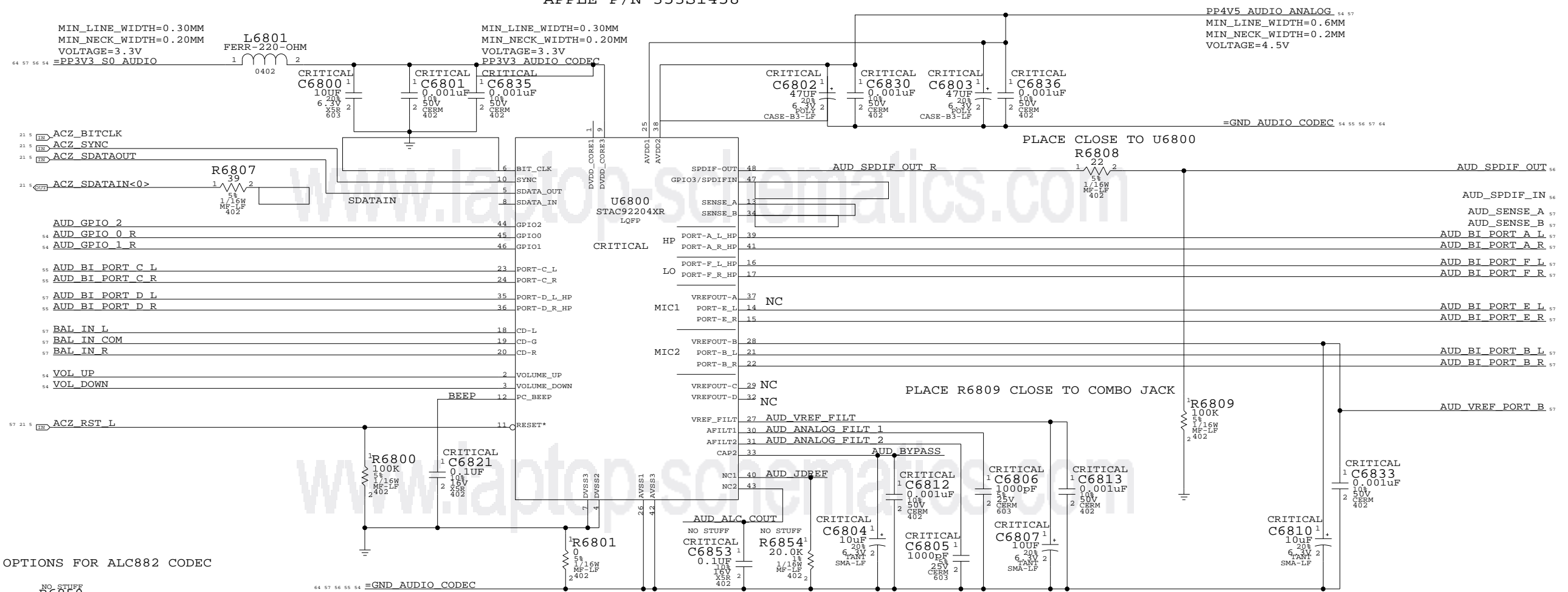
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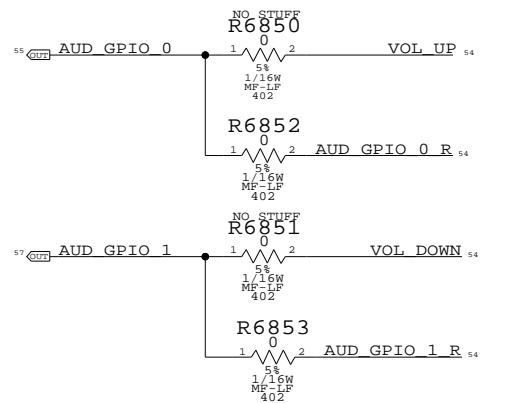
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7173	REV. 00000
	SCALE NONE	SHEET 53	OF 78

AUDIO CODEC

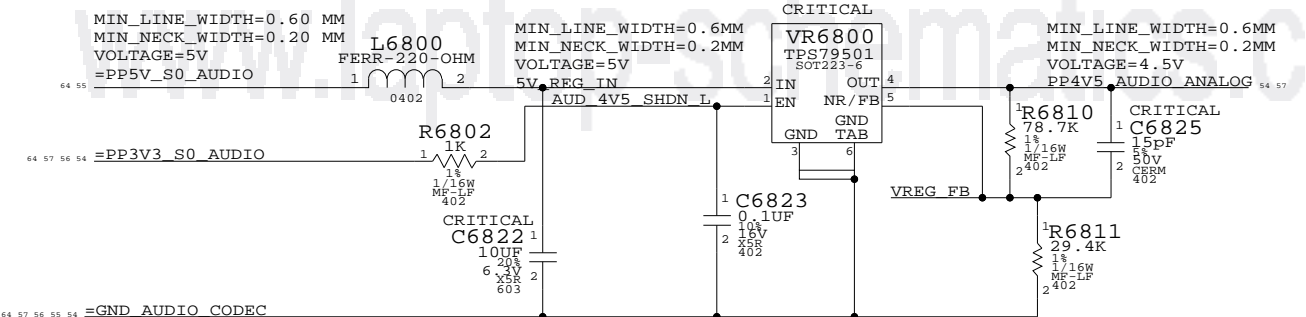
APPLE P/N 353S1458



STUFFING OPTIONS FOR ALC882 CODEC



64 57 56 55 54 =GND AUDIO CODEC
 MIN_LINE_WIDTH=0.30 MM
 MIN_NECK_WIDTH=0.20 MM
 VOLTAGE=0V



4.5V POWER SUPPLY FOR CODEC

USING DC OFFSET SCREENED PART AS PRIMARY OPTION

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
353S1345	353S1458	?	U6800	DC OFFSET SCREEN PRTS

AUDIO: CODEC

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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APPLE COMPUTER INC.

SCALE: NONE

SHT: 54 OF 78

SIZE: D

DRAWING NUMBER: 051-7173

REV.: 00000

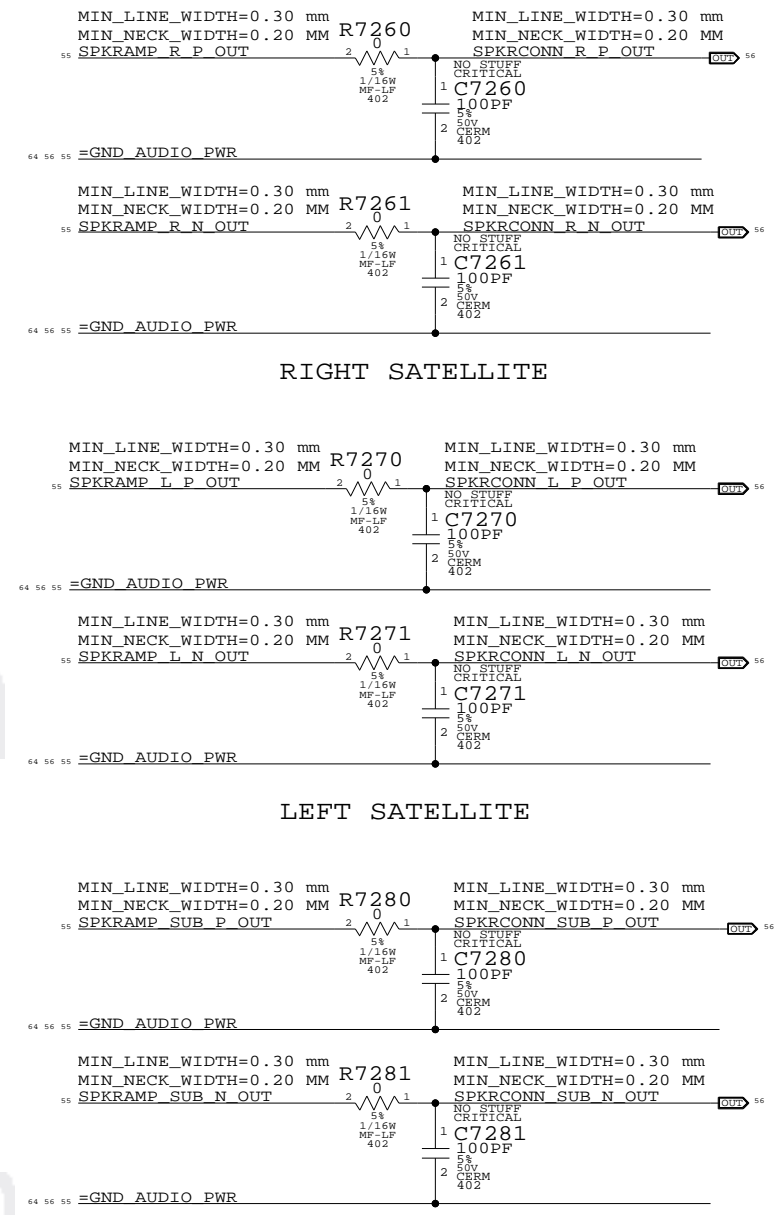
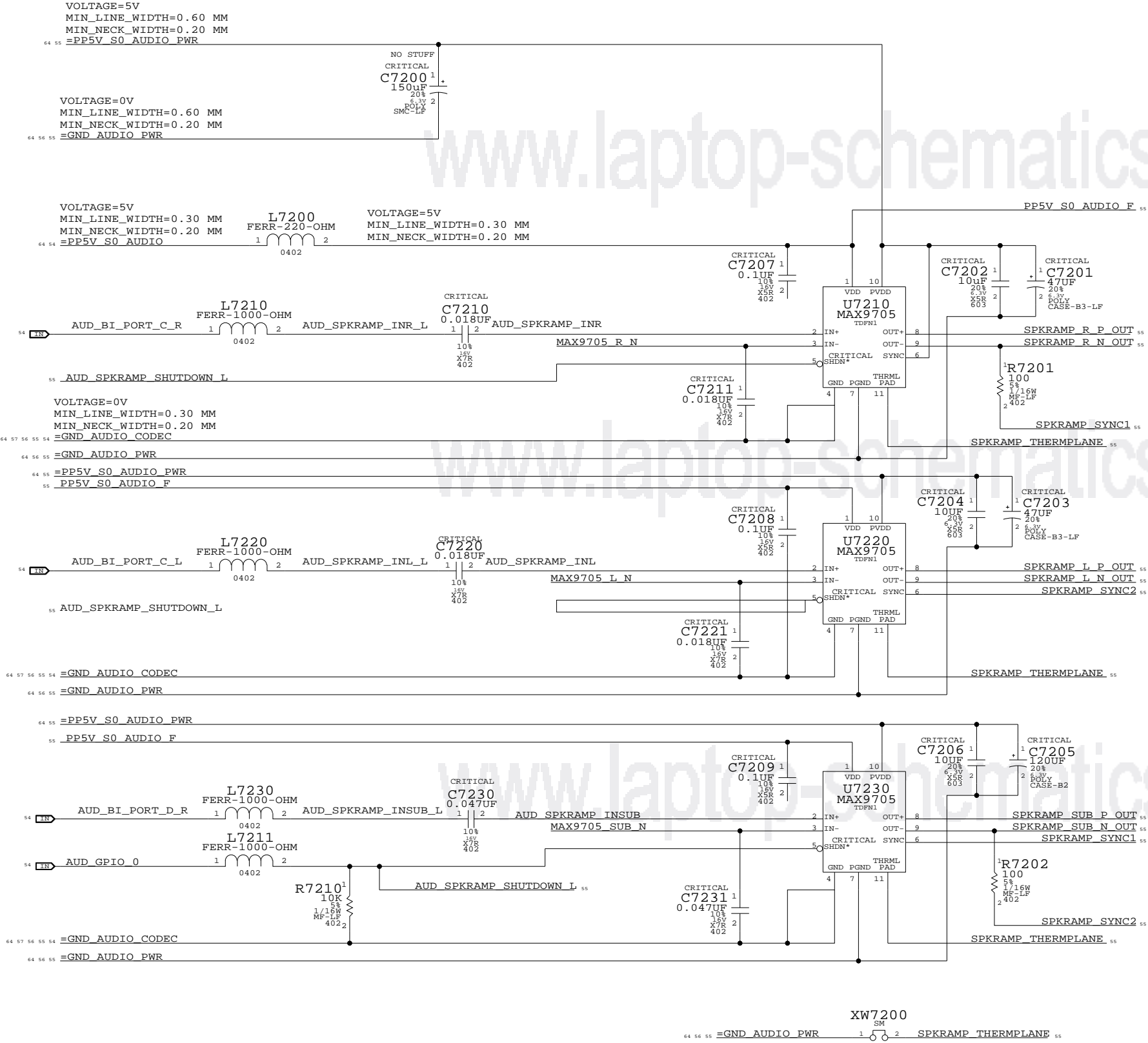
SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 442 Hz < FC < 736 Hz
 SUB 169 Hz < FC < 282 Hz

SPEAKER OUTPUT EMI FILTERS

D
C
B
A

D
C
B
A



AUDIO: SPEAKER AMP

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	55		

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AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

MIC CONNECTOR
APN:514S0392

CRITICAL
J7301
48227-0301
M-RT-SM1
4

MIC LO CONN
MIC HI CONN
MIC SHLD CONN

SPEAKER CONNECTOR
APN:518S0332

CRITICAL
J7302
88611-02001
F-ST-SM
3

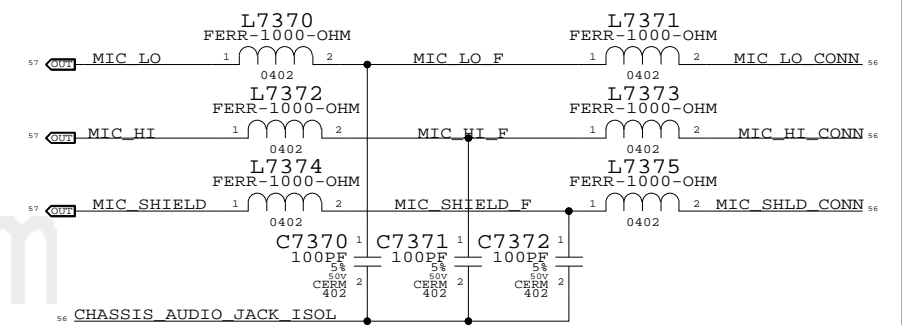
SPKRCONN L P OUT
SPKRCONN L N OUT
GND_AUDIO_PWR
SPKR_SHIELD
SPKRCONN SUB P OUT
SPKRCONN SUB N OUT
SPKRCONN R P OUT
SPKRCONN R N OUT

APN:518S0334

AUDIO SHIELD FILL

AUDIO_SHIELD_PLANE
CHASSIS_AUDIO_JACK_ISOL
CHASSIS_AUDIO_JACK_ISOL
CHASSIS_AUDIO_JACK_ISOL
CHASSIS_AUDIO_JACK_ISOL

MIC EMI FILTER



AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0290	1	CONN, 3.5MM COMBO AUDIO OUT, RA, MG3, LF	J7300	CRITICAL	NORMAL
514-0291	1	CONN, 3.5MM COMBO AUDIO IN, RA, MG3, LF	J7350	CRITICAL	NORMAL
514-0317	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J7300	CRITICAL	FANCY
514-0318	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J7350	CRITICAL	FANCY

AUDIO: JACK
 SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006
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APPLE COMPUTER INC.
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 SCALE: NONE SHEET 56 OF 78

D

D

C

C

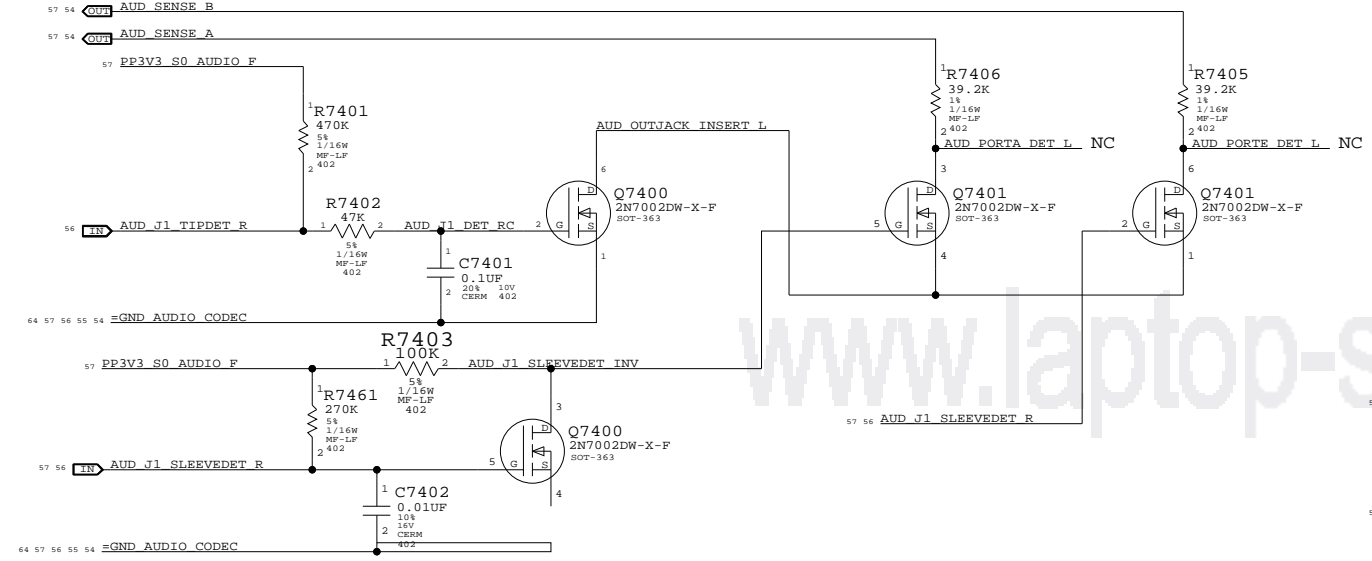
B

B

A

A

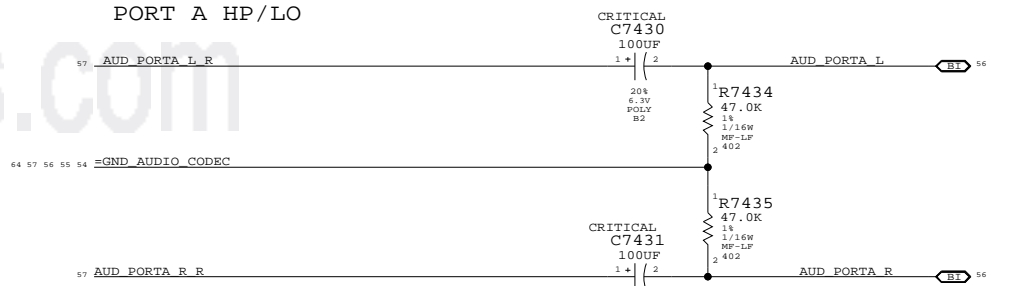
PORT A DETECT PORT E DETECT(E TELLS H TO TURN ON)



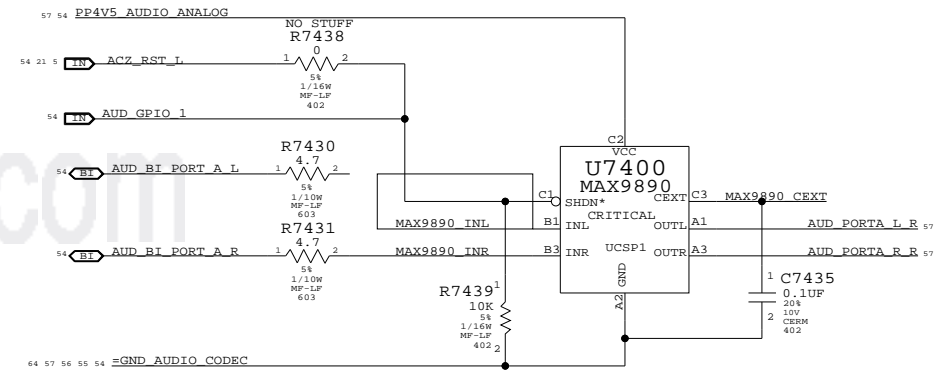
CODEC PORT ASSIGNMENTS

PORT A : HEADPHONE/LINE OUT
 PORT B : MICROPHONE ON BOTH CH (ADC 0)
 PORT C : SPEAKER AMP
 PORT D : UNUSED
 PORT E : SW USES TO TRIGGER DIGITAL OUT
 PORT F : LINE IN (ADC 1)
 CD INPUT : UNUSED

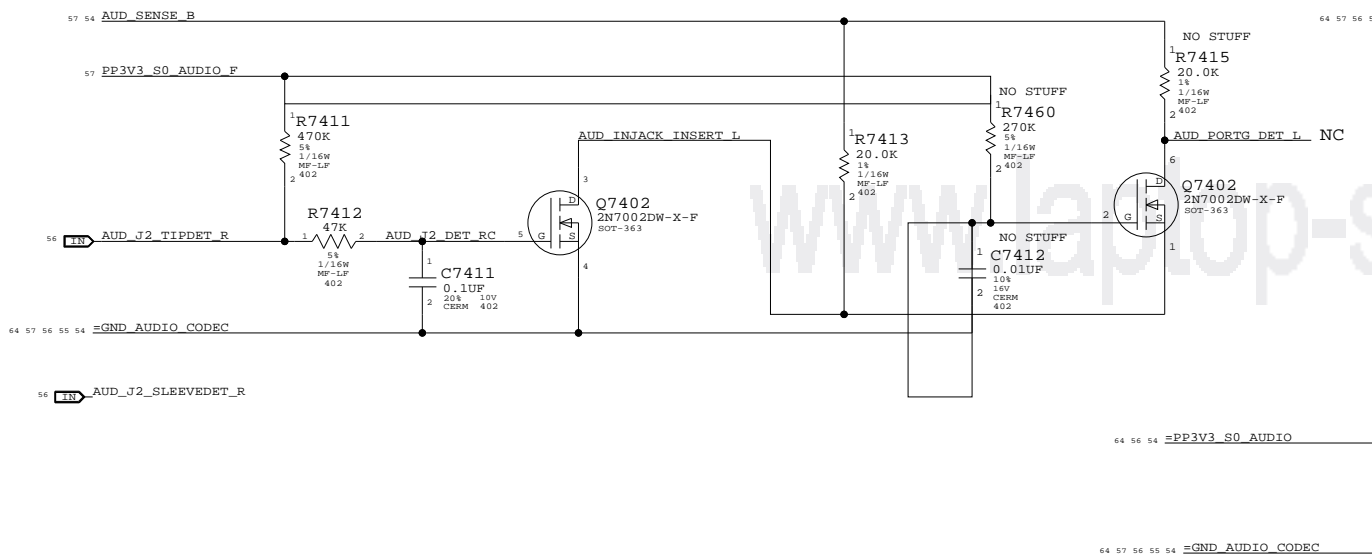
PORT A HP/LO



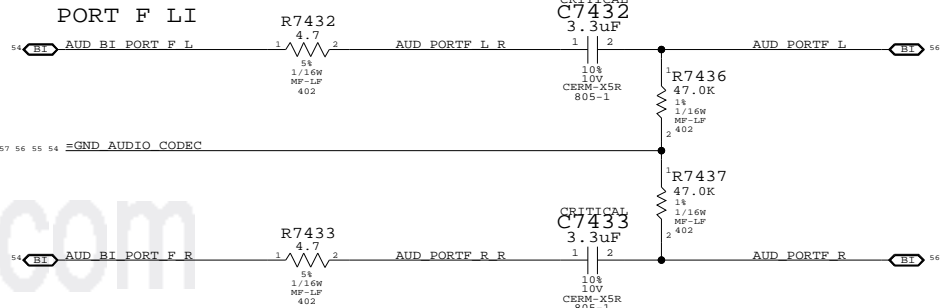
HP/LO DE-POP SWITCH APN: 353S1459



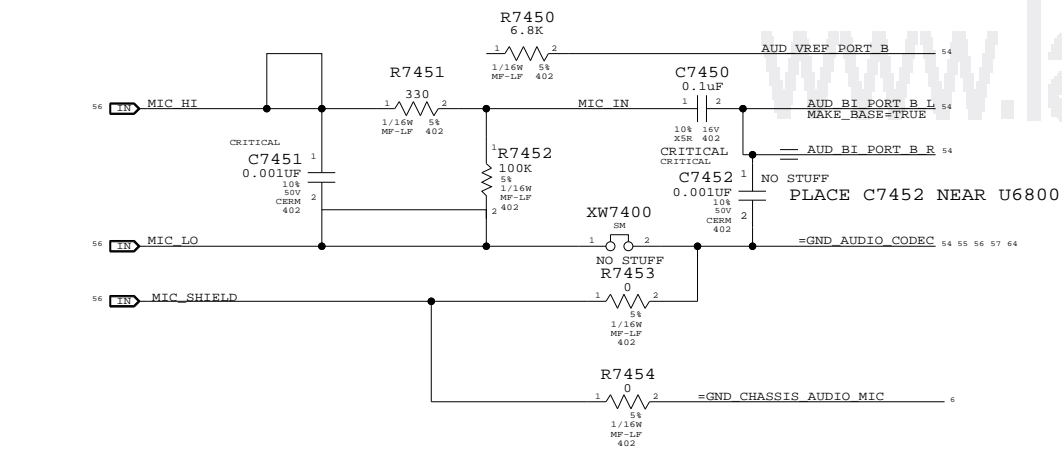
PORT F DETECT PORT G DETECT



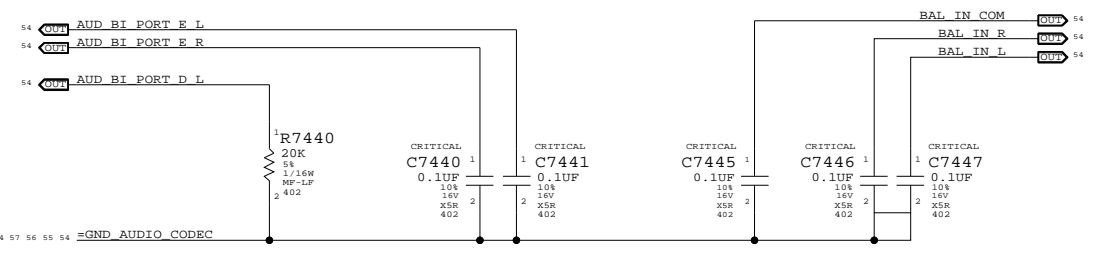
PORT F LI



MIC INPUT CIRCUITRY



UNUSED CODEC ANALOG PORT TERMINATIONS



AUDIO: JACK TRANSLATORS

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

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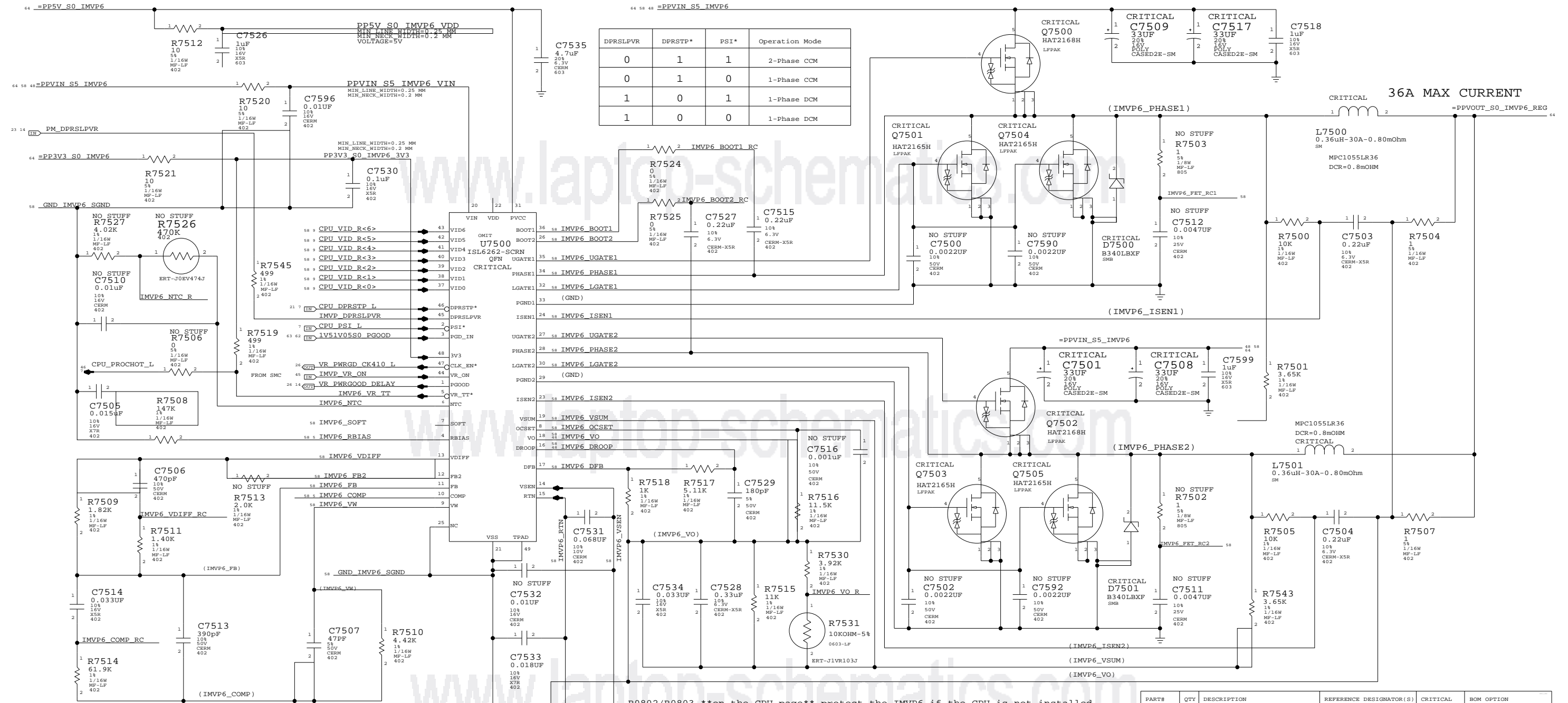
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
128S0093	128S0092	?	C7501_C7508	RENET T520V3300016AT0457650
128S0093	128S0092	?	C7509_C7517	RENET T520V3300016AT0457650

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM



Note 1: C7532, C7533 = 27.4 Ohm For Validating CPU Only.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500	353S1461	M42A

IMVP6 CPU VCore Regulator

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTIN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator

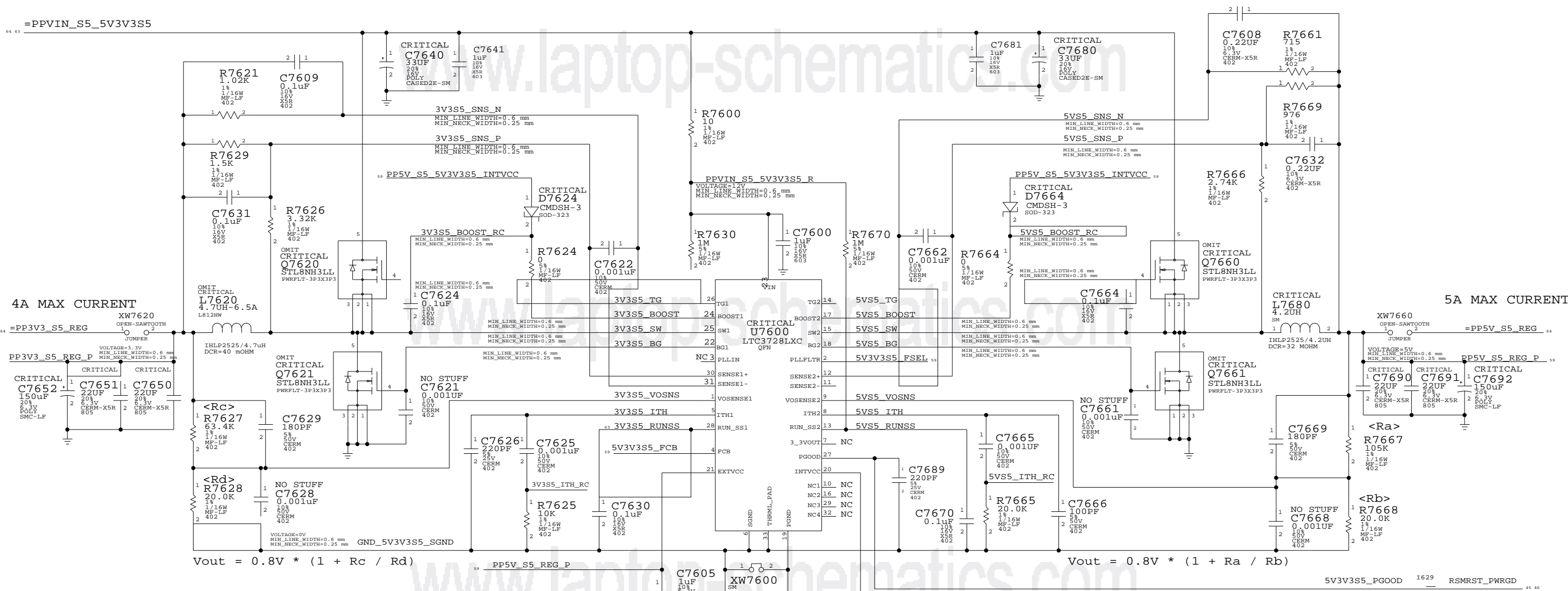
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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APPLE COMPUTER INC.	SCALE	SHEET	OF	REV.
	NONE	58	78	00000

5V / 3.3V POWER SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
15280133	1	4.7UH, +/-20%, 40mOHM, 3mm	L7620	3V3_IND_3MM
15280365	1	4.7UH, +/-20%, 40mOHM, 2.8mm	L7620	3V3_IND_2MM8
37680445	4	FAIRCHILD FDM6296	Q7620, Q7621, Q7660, Q7661	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
12880093	12880092	?	C7680, C7640	RENET VS20V330M16ATE0487650
37680448	37680445	?	Q7620, Q7621	VISHAY SI7806ADN
37680448	37680445	?	Q7660, Q7661	VISHAY SI7806ADN

5V / 3.3V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

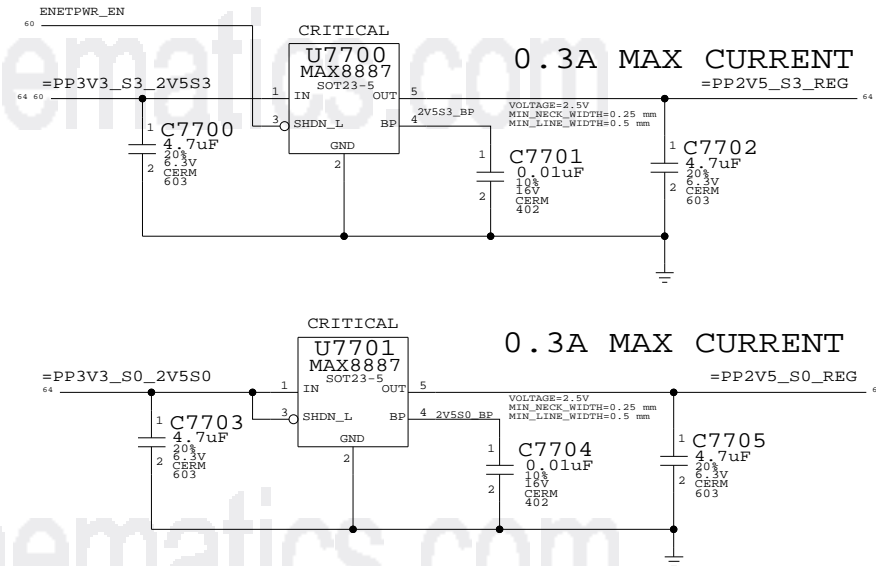
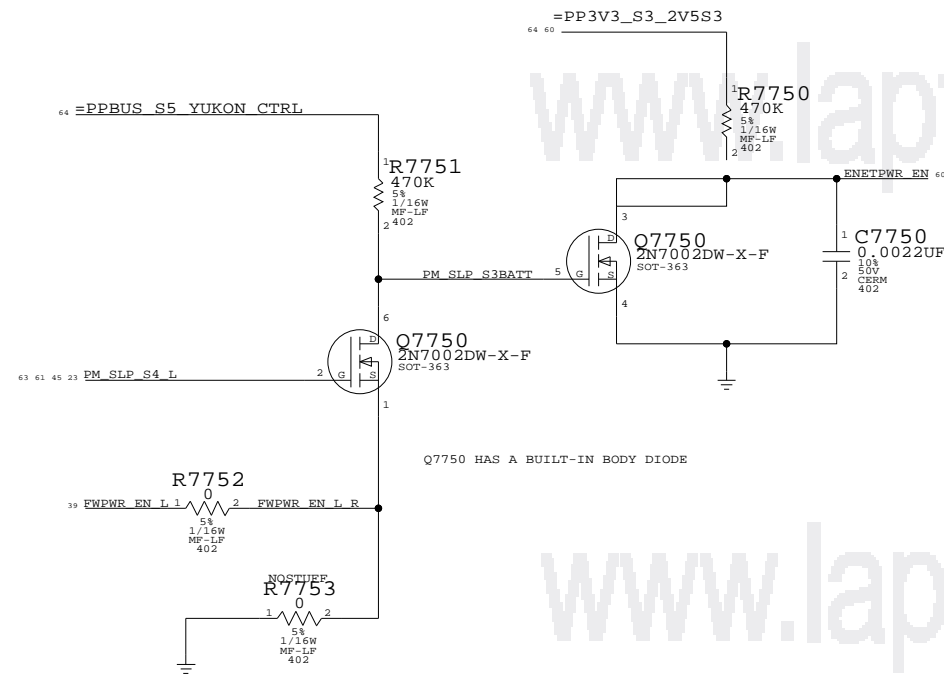
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APPLE COMPUTER INC.	SCALE	SHT	OF	REV.
	NONE	59	78	00000

YUKON POWER CONTROL

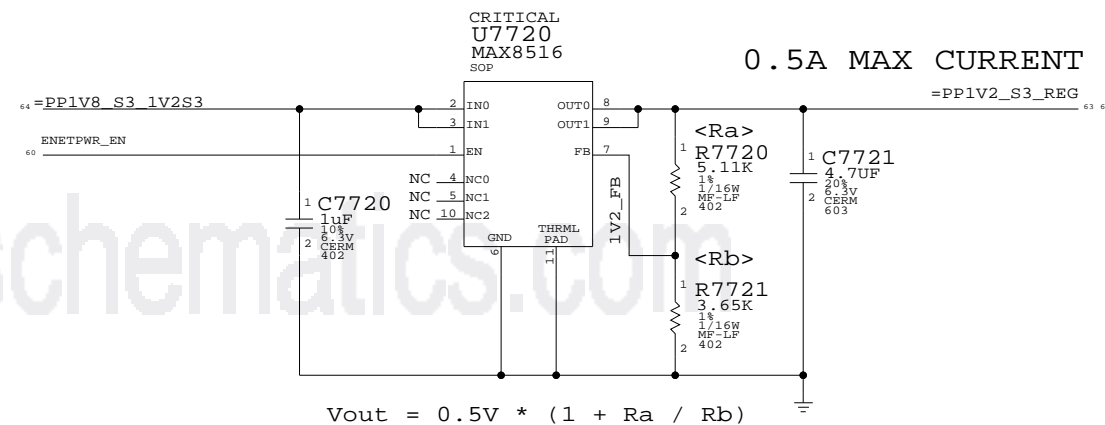
2.5V REGULATORS



1.2V REGULATOR

NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 S0	~S0 ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

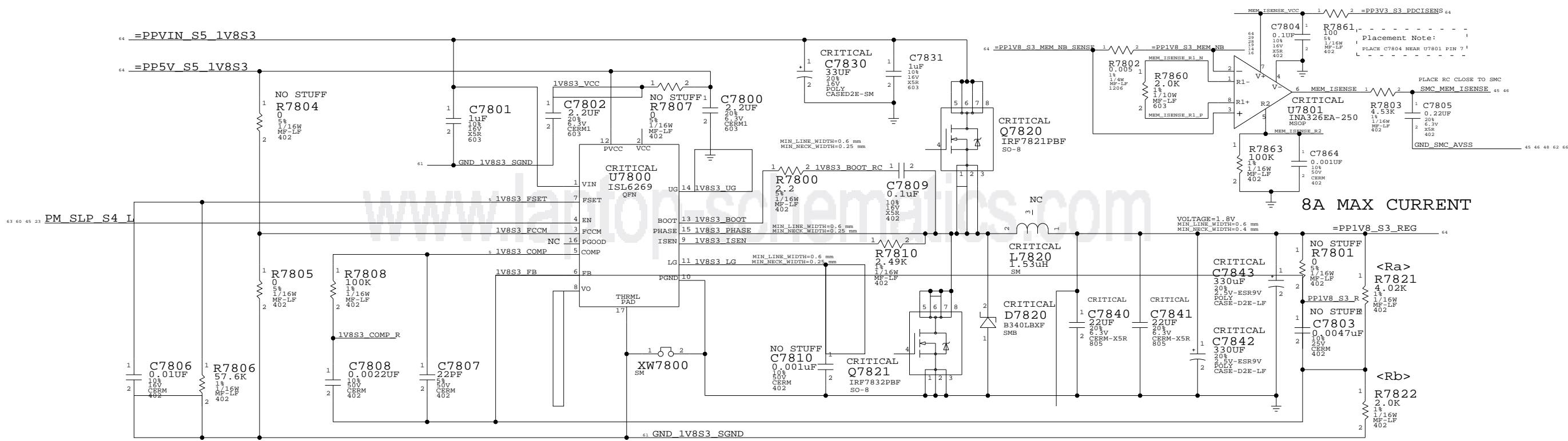
NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L



2.5V/1.2V Regulator
 SYNC_MASTER=ENET SYNC_DATE=12/06/2005
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	78
NONE		60	

1.8V POWER SUPPLY



$$V_{out} = 0.6V * (1 + R_a / R_b)$$

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	ERRY 0520V330MELR40457450

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842, C7843	PANASONIC KEF5X0D331ER
128S0095	128S0060	?	C7842, C7843	PANASONIC KEF5X0D331EK

1.8V Supply
 SYNC_MASTER=POWER SYNC_DATE=07/13/2005
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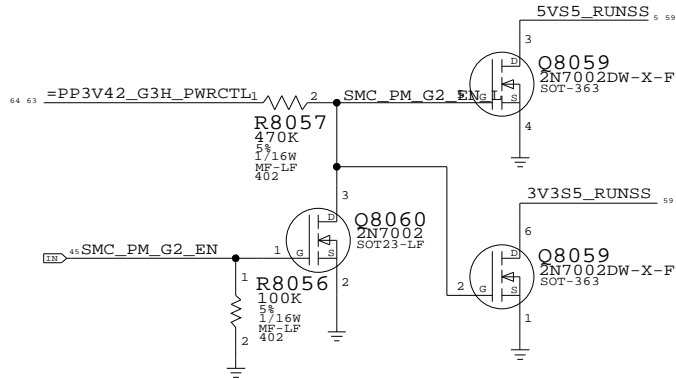
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	NONE	SHT	61 OF 78

POWER CONTROL SIGNALS

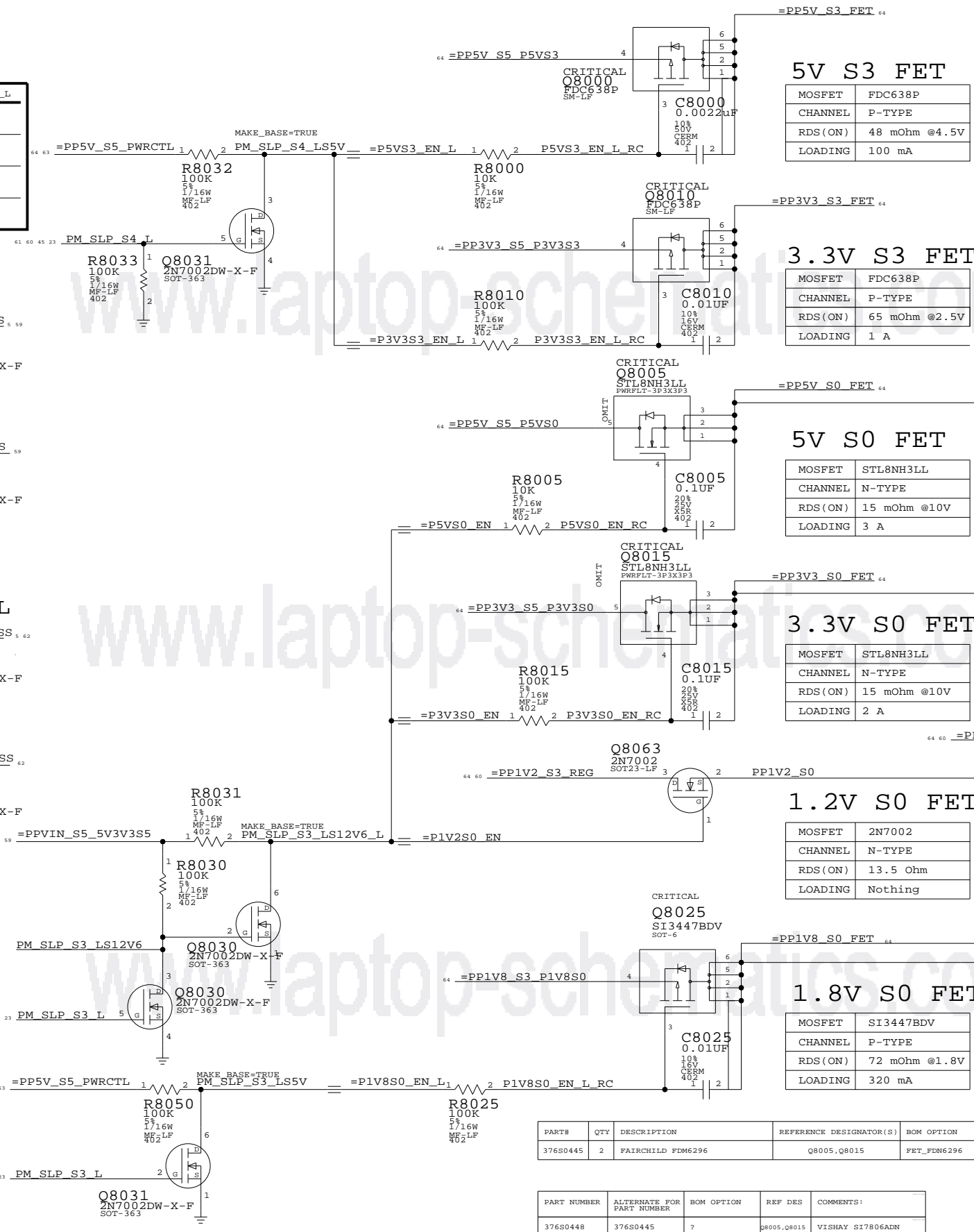
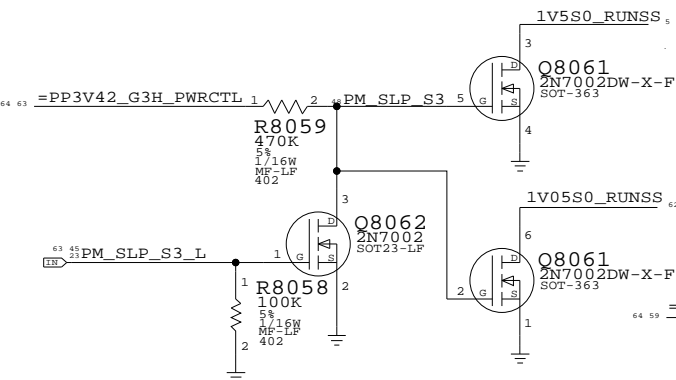
These rails are monitored by LTC2908

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V/3.3V S5 RUN/SS CONTROL

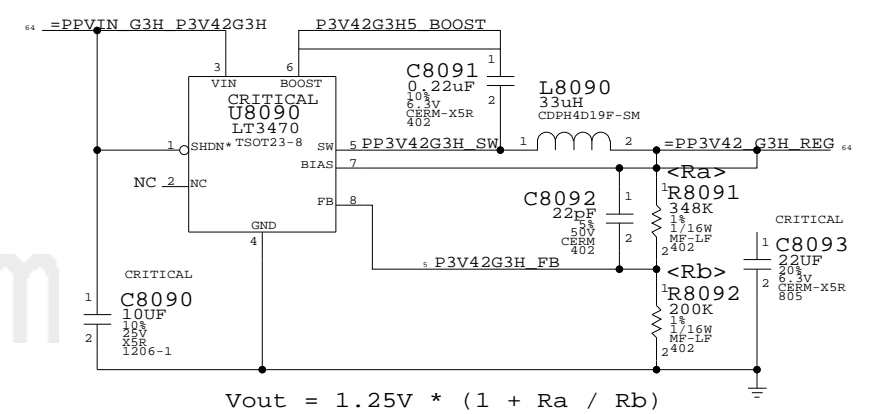


1.5V/1.05V S0 RUN/SS CONTROL



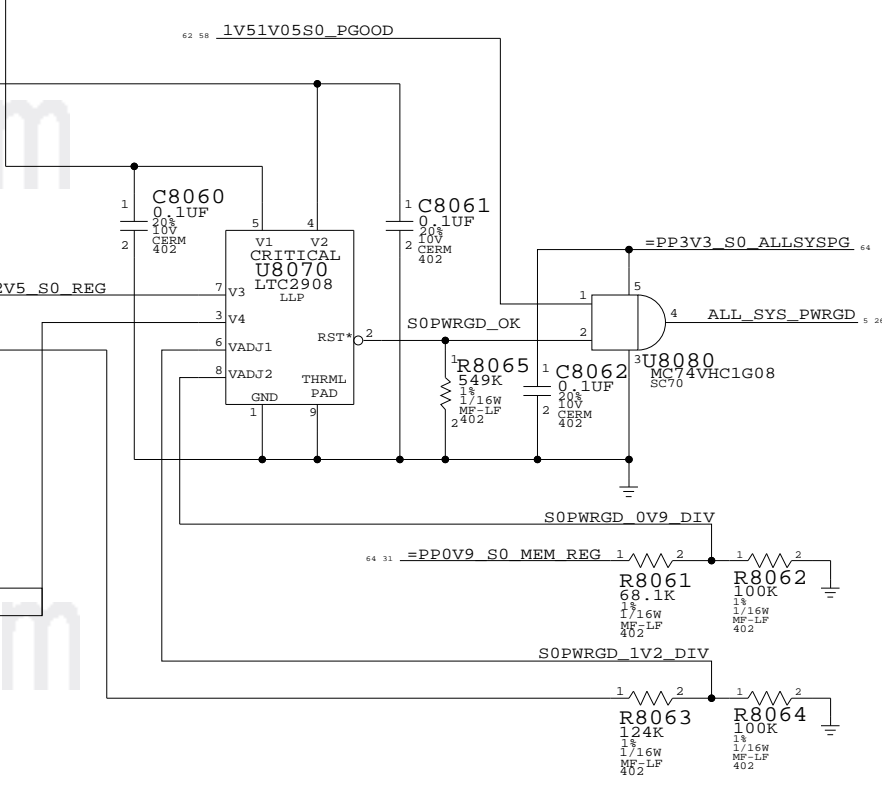
3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



$$V_{out} = 1.25V * (1 + R_a / R_b)$$

ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005,Q8015	FET_FDM6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	D8005,Q8015	VISHAY SI7806ADN

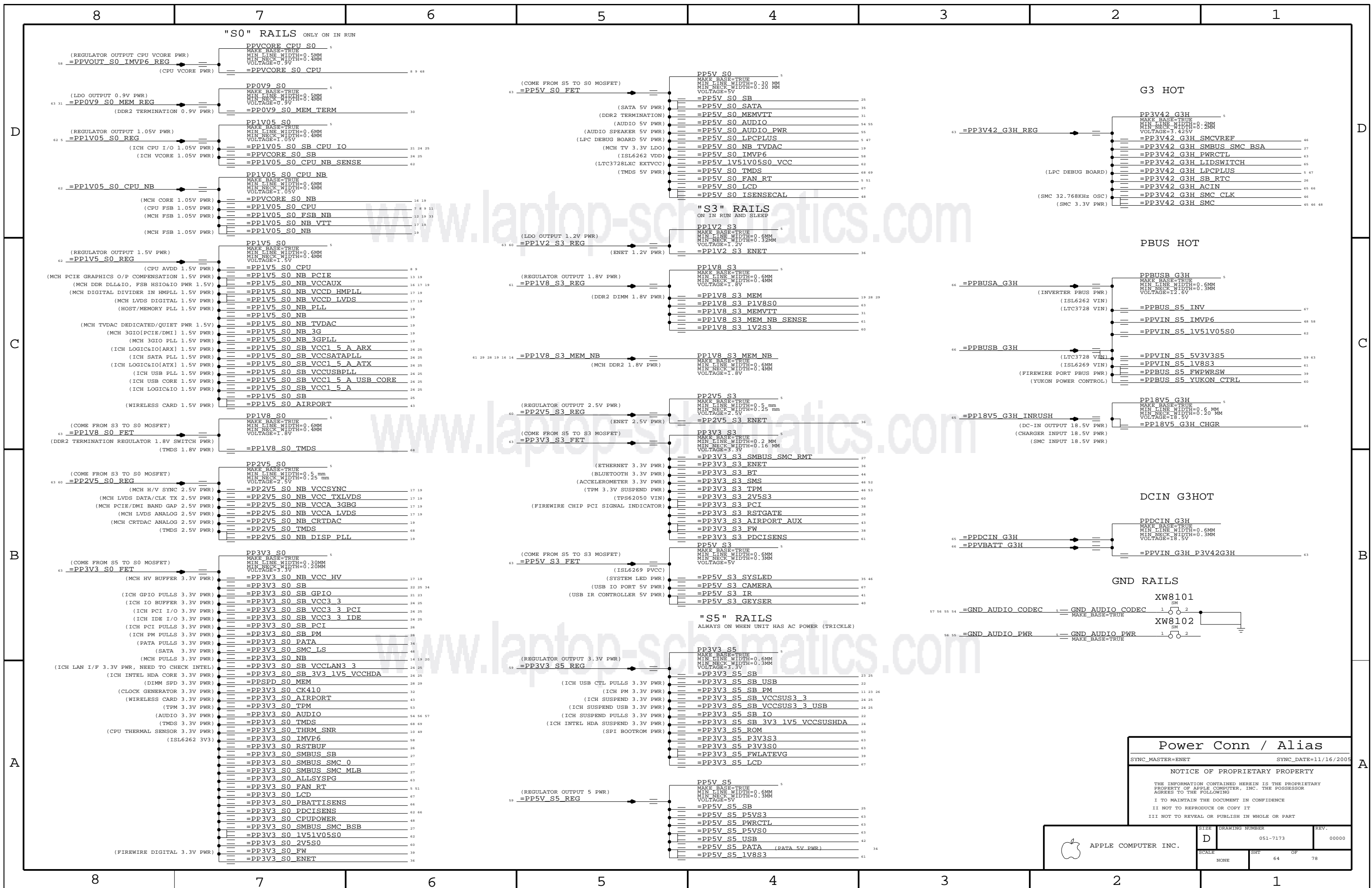
S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	63		



Power Conn / Alias

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

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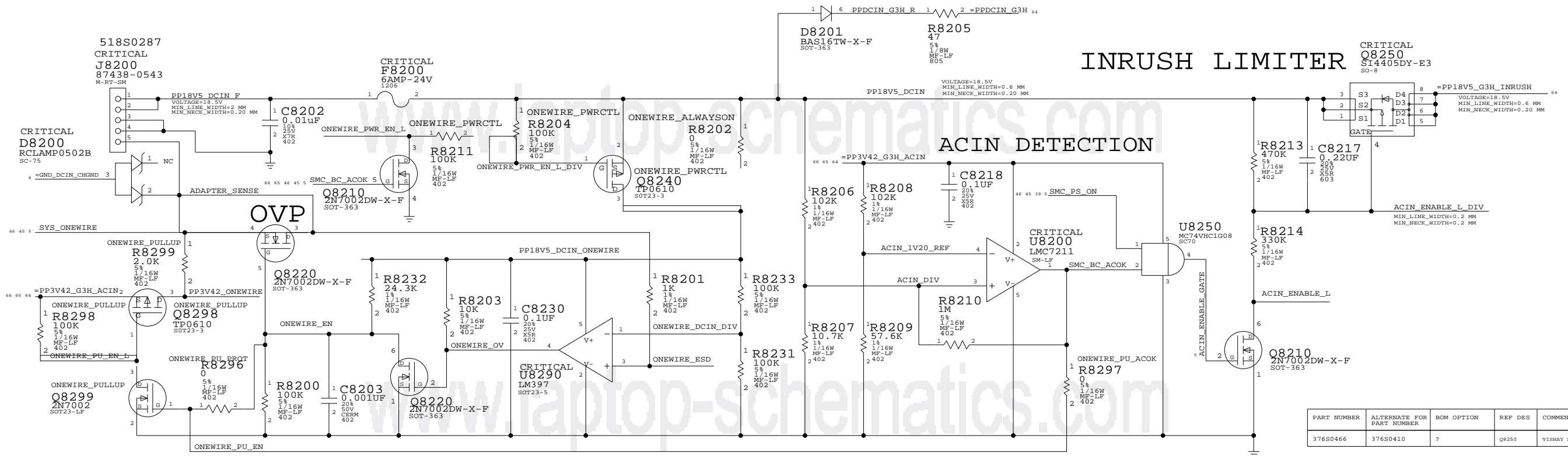
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	SCALE	SHT	OF	REV.
	NONE	64	78	00000

D	051-7173	00000
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DC-JACK INTERFACE

8 7 6 5 4 3 2 1



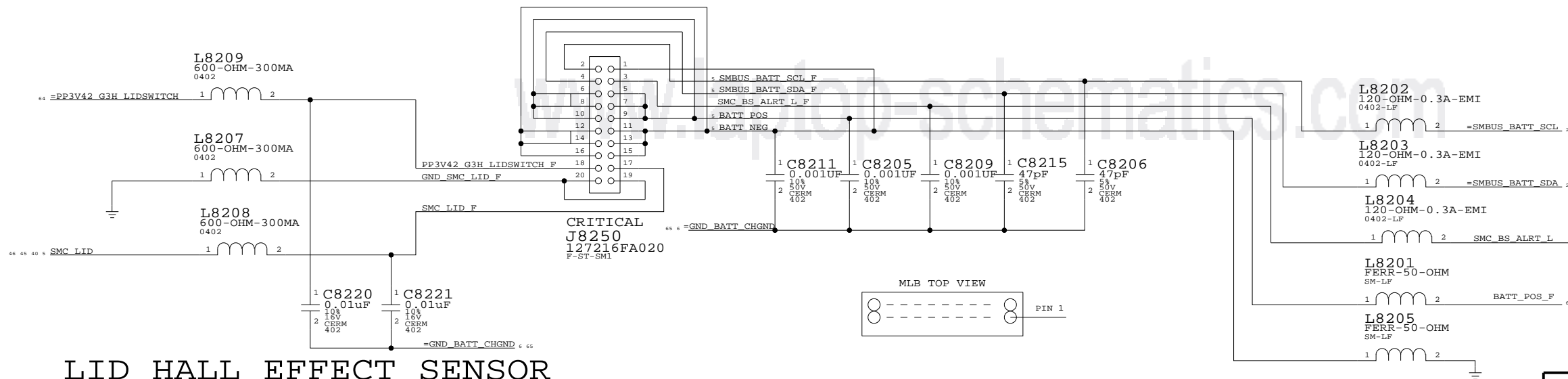
INRUSH LIMITER

ACIN DETECTION

OVP

BATTERY INTERFACE

8 7 6 5 4 3 2 1



LID HALL EFFECT SENSOR

DC-In & Battery Connectors

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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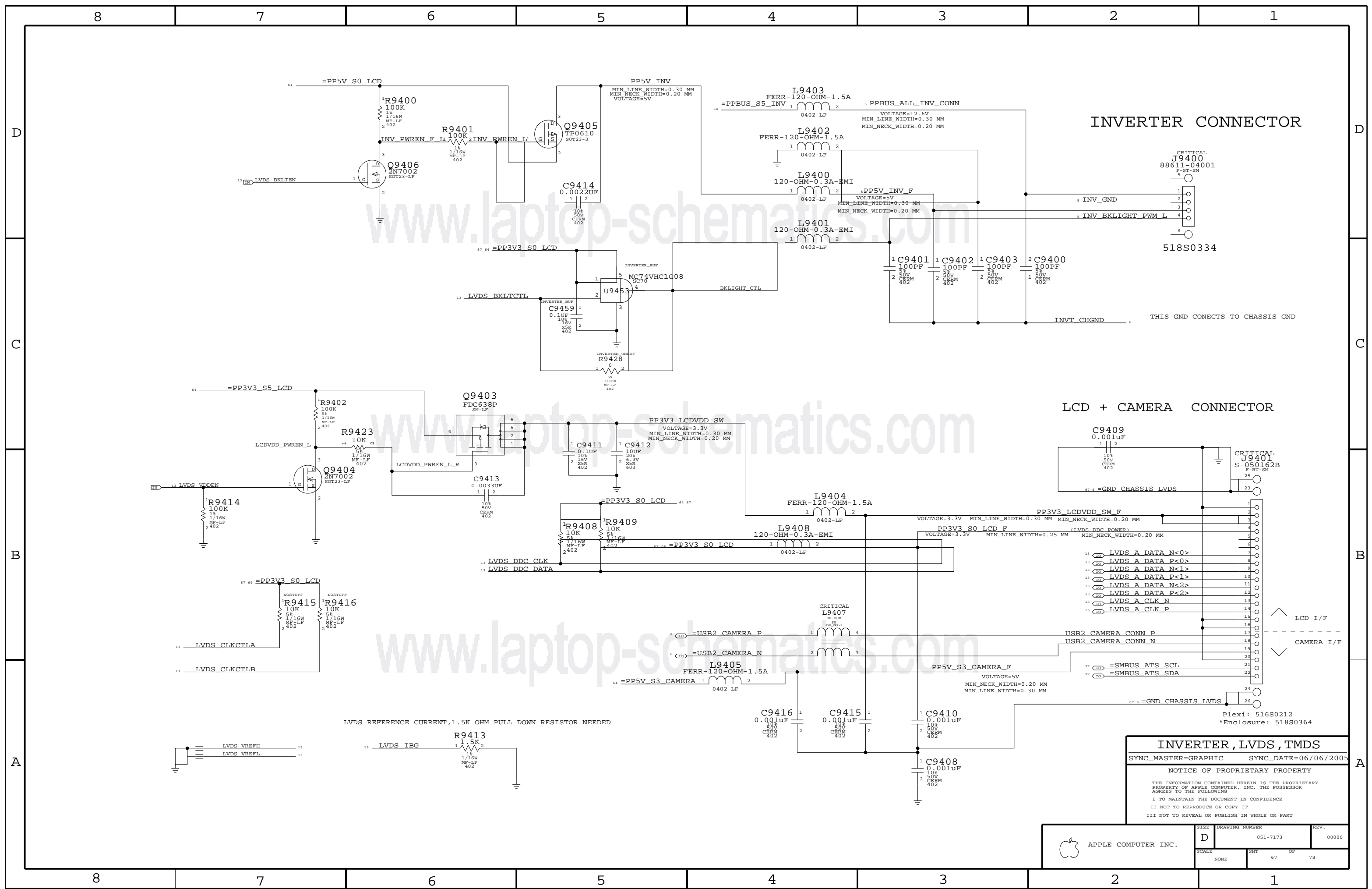
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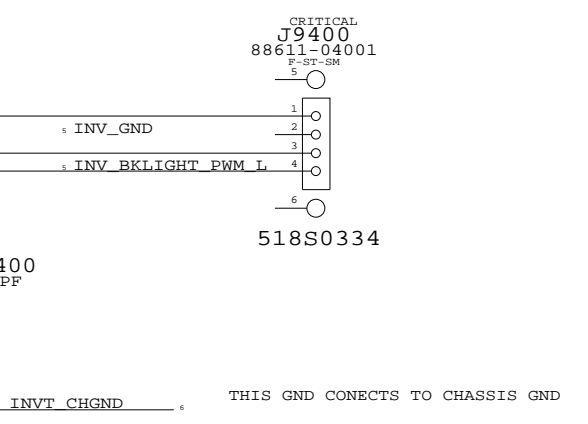
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7173	00000
SCALE	SHT	OF	REV.
NONE	65	78	

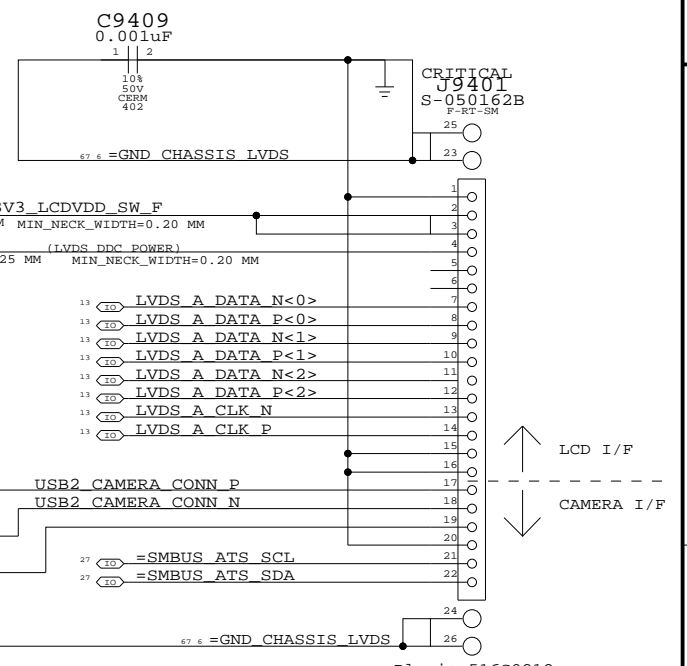
8 7 6 5 4 3 2 1



INVERTER CONNECTOR



LCD + CAMERA CONNECTOR



INVERTER, LVDS, TMDs

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

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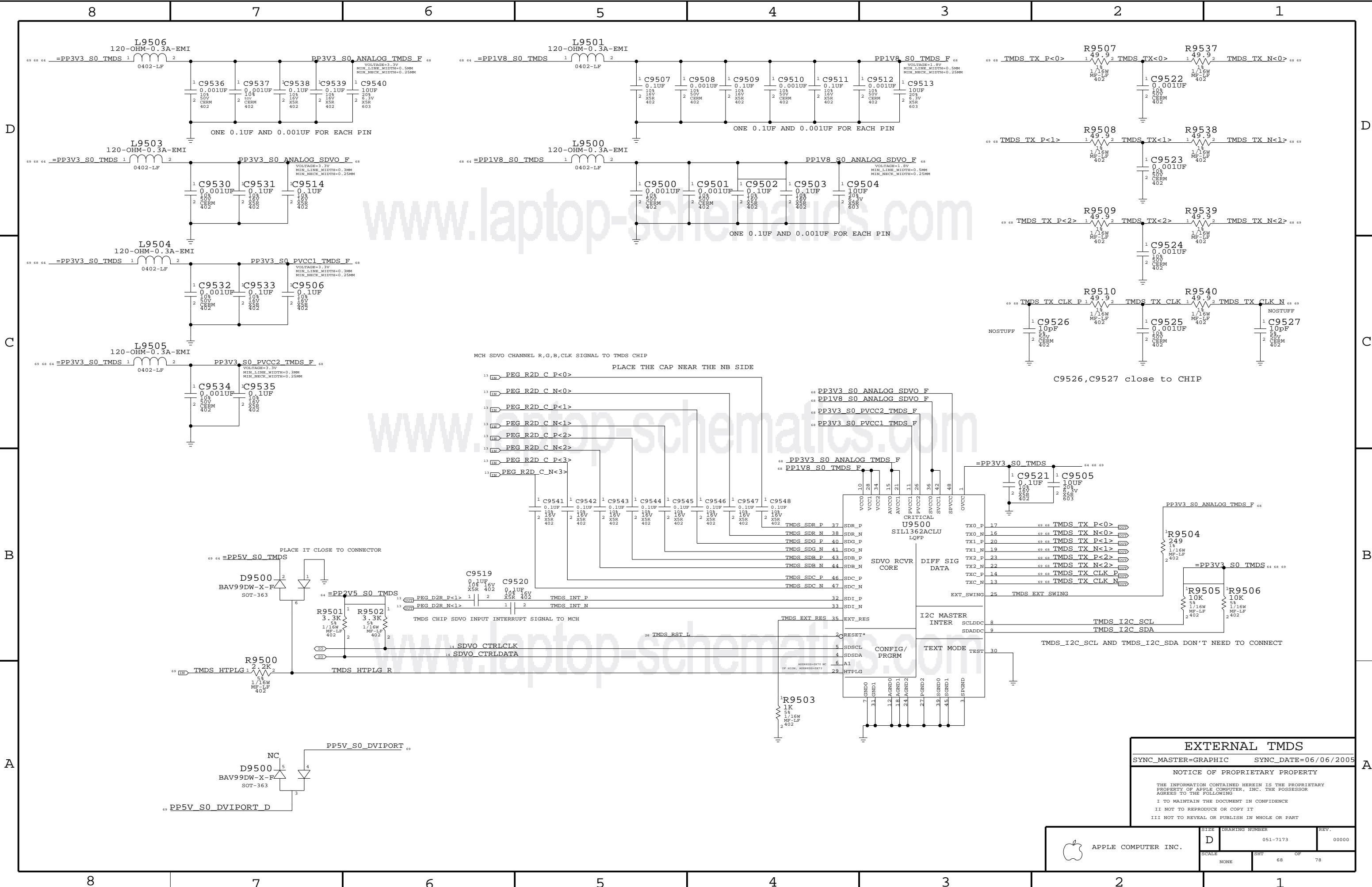
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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	67		



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EXTERNAL TMDs
 SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005
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	D	051-7173	00000
SCALE	SHT	OF	78
NONE	68		

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
15580227	15580164	?	REF: 15580164	KEEP MAG LAYER IN BOX

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

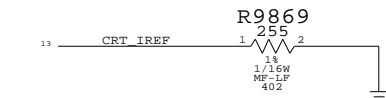
TMDS(MINI DVI) INTERFACE

Isolation required for DVI power switch

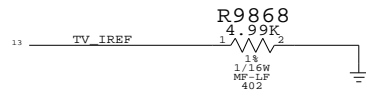
PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

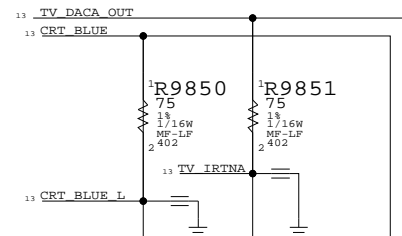
A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND



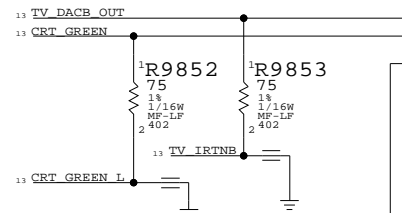
TV REFERENCE CURRENT, USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS



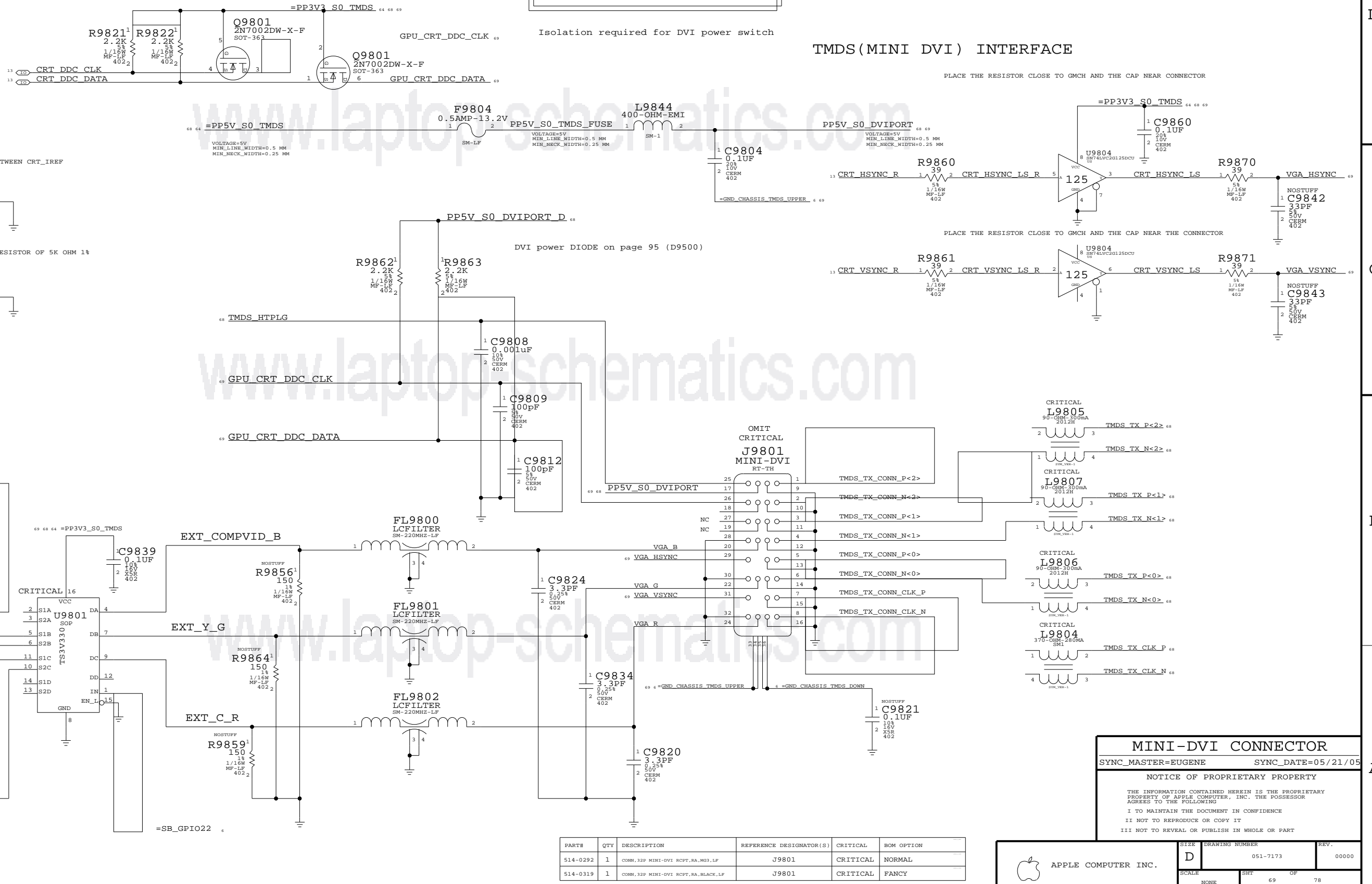
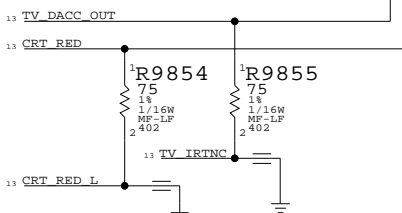
PLACE THE RESISTOR CLOSE TO GMCH



PLACE THE RESISTOR CLOSE TO GMCH



PLACE THE RESISTOR CLOSE TO GMCH



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN, 32P MINI-DVI RCP7, RA, MG3, LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN, 32P MINI-DVI RCP7, RA, BLACK, LF	J9801	CRITICAL	FANCY

MINI-DVI CONNECTOR
 SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

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SCALE: NONE SHEET: 69 OF 78

SIZE: D DRAWING NUMBER: 051-7173 REV.: 00000

8	7	6	5	4	3	2	1																																																																																																																																																																																																																																																																																																																																																																											
<p>Title: Basenet Report Design: m42a Date: Aug 5 16:01:17 2006</p> <p>Base nets and synonyms for m42a_lib.M42A(m42a_lib.m42a(sch.1))</p> <table border="1"> <thead> <tr> <th>Base Signal</th> <th>Synonyms</th> <th>Location((Zone) dir))</th> </tr> </thead> <tbody> <tr> <td>I_V2_FB</td> <td>I_V2_FB - @m42a_lib.M42A</td> <td>60A3</td> </tr> <tr> <td>I_V050_BG</td> <td>I_V050_BG - @m42a_lib.M42A</td> <td>62B4</td> </tr> <tr> <td>I_V050_BOOST</td> <td>I_V050_BOOST - @m42a_lib.M42A</td> <td>62B4</td> </tr> <tr> <td>I_V050_BOOST_RC</td> <td>I_V050_BOOST_RC - @m42a_lib.M42A</td> <td>62C3</td> </tr> <tr> <td>I_V050_COMP</td> <td>I_V050_COMP - @m42a_lib.M42A</td> <td>5D7</td> </tr> <tr> <td>I_V050_FSET</td> <td>I_V050_FSET - @m42a_lib.M42A</td> <td>5D7</td> </tr> <tr> <td>I_V050_ITH</td> <td>I_V050_ITH - @m42a_lib.M42A</td> <td>62B4</td> </tr> <tr> <td>I_V050_ITH_RC</td> <td>I_V050_ITH_RC - @m42a_lib.M42A</td> <td>62B4</td> </tr> <tr> <td>I_V050_RUNSS</td> <td>I_V050_RUNSS - @m42a_lib.M42A</td> <td>62B4 63B7</td> </tr> <tr> <td>I_V050_SNS_N</td> <td>I_V050_SNS_N - @m42a_lib.M42A</td> <td>62C3</td> </tr> <tr> <td>I_V050_SNS_P</td> <td>I_V050_SNS_P - @m42a_lib.M42A</td> <td>62C3</td> </tr> <tr> <td>I_V050_SW</td> <td>I_V050_SW - @m42a_lib.M42A</td> <td>62B4</td> </tr> <tr> <td>I_V050_TG</td> <td>I_V050_TG - @m42a_lib.M42A</td> <td>62C4</td> </tr> <tr> <td>I_V050_VOSSNS</td> <td>I_V050_VOSSNS - @m42a_lib.M42A</td> <td>62B4</td> </tr> <tr> <td>I_V500_BG</td> <td>I_V500_BG - @m42a_lib.M42A</td> <td>62B5</td> </tr> <tr> <td>I_V500_BOOST</td> <td>I_V500_BOOST - @m42a_lib.M42A</td> <td>62B5</td> </tr> <tr> <td>I_V500_BOOST_RC</td> <td>I_V500_BOOST_RC - @m42a_lib.M42A</td> <td>62C6</td> </tr> <tr> <td>I_V500_ITH</td> <td>I_V500_ITH - @m42a_lib.M42A</td> <td>62B5</td> </tr> <tr> <td>I_V500_ITH_RC</td> <td>I_V500_ITH_RC - @m42a_lib.M42A</td> <td>62B5</td> </tr> <tr> <td>I_V500_RUNSS</td> <td>I_V500_RUNSS - @m42a_lib.M42A</td> <td>5D7 62B5 63B7</td> </tr> <tr> <td>I_V500_SNS_N</td> <td>I_V500_SNS_N - @m42a_lib.M42A</td> <td>62C6</td> </tr> <tr> <td>I_V500_SNS_P</td> <td>I_V500_SNS_P - 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@m42a_lib.M42A</td> <td>6C2 42C8</td> </tr> <tr> <td>I_USB_C_OC_L</td> <td>I_USB_C_OC_L - @m42a_lib.M42A</td> <td>6C1 22C4 22D8</td> </tr> <tr> <td>I_EXTUSB_OC_L</td> <td>I_EXTUSB_OC_L - @m42a_lib.M42A</td> <td>6C2</td> </tr> <tr> <td>I_FWPWR_PWRON</td> <td>I_FWPWR_PWRON - @m42a_lib.M42A</td> <td>6D2 39C6</td> </tr> <tr> <td>I_NC_FWPWR_PWRON</td> <td>I_NC_FWPWR_PWRON - @m42a_lib.M42A</td> <td>6D1</td> </tr> <tr> <td>I_GND_BATT_CHGND</td> <td>I_GND_BATT_CHGND - @m42a_lib.M42A</td> <td>6D8 65A6 65A6</td> </tr> <tr> <td>I_GND_CHASSIS_AUDIO_JACK</td> <td>I_GND_CHASSIS_AUDIO_JACK - @m42a_lib.M42A</td> <td>6D8 5688</td> </tr> <tr> <td>I_GND_CHASSIS_AUDIO_MIC</td> <td>I_GND_CHASSIS_AUDIO_MIC - @m42a_lib.M42A</td> <td>6D8 57A6</td> </tr> <tr> <td>I_GND_CHASSIS_DIPDIMM_LEFT</td> <td>I_GND_CHASSIS_DIPDIMM_LEFT - @m42a_lib.M42A</td> <td>6D8 28A5</td> </tr> <tr> <td>I_GND_CHASSIS_DIPDIMM_RIGHT</td> <td>I_GND_CHASSIS_DIPDIMM_RIGHT - @m42a_lib.M42A</td> <td>6D8 28A5</td> </tr> <tr> <td>I_GND_CHASSIS_AUDIO_SPKRCONN</td> <td>I_GND_CHASSIS_AUDIO_SPKRCONN - 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@m42a_lib.M42A	62B4 63B7	I_V050_SNS_N	I_V050_SNS_N - @m42a_lib.M42A	62C3	I_V050_SNS_P	I_V050_SNS_P - @m42a_lib.M42A	62C3	I_V050_SW	I_V050_SW - @m42a_lib.M42A	62B4	I_V050_TG	I_V050_TG - @m42a_lib.M42A	62C4	I_V050_VOSSNS	I_V050_VOSSNS - @m42a_lib.M42A	62B4	I_V500_BG	I_V500_BG - @m42a_lib.M42A	62B5	I_V500_BOOST	I_V500_BOOST - @m42a_lib.M42A	62B5	I_V500_BOOST_RC	I_V500_BOOST_RC - @m42a_lib.M42A	62C6	I_V500_ITH	I_V500_ITH - @m42a_lib.M42A	62B5	I_V500_ITH_RC	I_V500_ITH_RC - @m42a_lib.M42A	62B5	I_V500_RUNSS	I_V500_RUNSS - @m42a_lib.M42A	5D7 62B5 63B7	I_V500_SNS_N	I_V500_SNS_N - @m42a_lib.M42A	62C6	I_V500_SNS_P	I_V500_SNS_P - @m42a_lib.M42A	62C6	I_V500_SW	I_V500_SW - @m42a_lib.M42A	62B5	I_V500_TG	I_V500_TG - @m42a_lib.M42A	62C5	I_V500_VOSSNS	I_V500_VOSSNS - @m42a_lib.M42A	62B5	I_V8S3_BOOT	I_V8S3_BOOT - @m42a_lib.M42A	61B5	I_V8S3_BOOT_RC	I_V8S3_BOOT_RC - @m42a_lib.M42A	61C4	I_V8S3_COMP	I_V8S3_COMP - @m42a_lib.M42A	5D7 61B6	I_V8S3_COMP_R	I_V8S3_COMP_R - @m42a_lib.M42A	61B6	I_V8S3_FB	I_V8S3_FB - @m42a_lib.M42A	61B6	I_V8S3_PCCM	I_V8S3_PCCM - @m42a_lib.M42A	61B6	I_V8S3_FSET	I_V8S3_FSET - @m42a_lib.M42A	5D7 61C6	I_V8S3_ISEN	I_V8S3_ISEN - @m42a_lib.M42A	61B5	I_V8S3_LG	I_V8S3_LG - @m42a_lib.M42A	61B5	I_V8S3_PHASE	I_V8S3_PHASE - @m42a_lib.M42A	61B5	I_V8S3_UG	I_V8S3_UG - @m42a_lib.M42A	61C5	I_V8S3_VCC	I_V8S3_VCC - @m42a_lib.M42A	61C6	I_V51V0500_FCB	I_V51V0500_FCB - @m42a_lib.M42A	62A3 62B5	I_V51V0500_FSEL	I_V51V0500_FSEL - @m42a_lib.M42A	62A2 62B4	I_V51V0500_POOD0	I_V51V0500_POOD0 - @m42a_lib.M42A	62A1 63C2	I_V2500_BP	I_V2500_BP - @m42a_lib.M42A	60C3	I_V25S3_BP	I_V25S3_BP - @m42a_lib.M42A	60C3	I_V3V35_BG	I_V3V35_BG - @m42a_lib.M42A	59B5	I_V3V35_BOOST	I_V3V35_BOOST - @m42a_lib.M42A	59B5	I_V3V35_BOOST_RC	I_V3V35_BOOST_RC - @m42a_lib.M42A	59C6	I_V3V35_COMP	I_V3V35_COMP - @m42a_lib.M42A	5D7	I_V3V35_FSET	I_V3V35_FSET - @m42a_lib.M42A	5D7	I_V3V35_ITH	I_V3V35_ITH - @m42a_lib.M42A	59B5	I_V3V35_ITH_RC	I_V3V35_ITH_RC - @m42a_lib.M42A	59B5	I_V3V35_RUNSS	I_V3V35_RUNSS - @m42a_lib.M42A	59B5 63C7	I_V3V35_SNS_N	I_V3V35_SNS_N - @m42a_lib.M42A	59C6	I_V3V35_SNS_P	I_V3V35_SNS_P - @m42a_lib.M42A	59C6	I_V3V35_SW	I_V3V35_SW - @m42a_lib.M42A	59B5	I_V3V35_TG	I_V3V35_TG - @m42a_lib.M42A	59C5	I_V3V35_VOSSNS	I_V3V35_VOSSNS - @m42a_lib.M42A	59B5	I_V3V35_FCB	I_V3V35_FCB - @m42a_lib.M42A	59A3 59B5	I_V3V35_FSEL	I_V3V35_FSEL - @m42a_lib.M42A	59A2 59B4	I_V585_BG	I_V585_BG - @m42a_lib.M42A	59B4	I_V585_BOOST	I_V585_BOOST - @m42a_lib.M42A	59B4	I_V585_BOOST_RC	I_V585_BOOST_RC - @m42a_lib.M42A	59C3	I_V585_ITH	I_V585_ITH - @m42a_lib.M42A	59B4	I_V585_ITH_RC	I_V585_ITH_RC - @m42a_lib.M42A	59B3	I_V585_RUNSS	I_V585_RUNSS - @m42a_lib.M42A	5D7 59B4 63C7	I_V585_SNS_N	I_V585_SNS_N - @m42a_lib.M42A	59C3	I_V585_SNS_P	I_V585_SNS_P - @m42a_lib.M42A	59C3	I_V585_SW	I_V585_SW - @m42a_lib.M42A	59B4	I_V585_TG	I_V585_TG - @m42a_lib.M42A	59C4	I_V585_VOSSNS	I_V585_VOSSNS - @m42a_lib.M42A	59B4	I_V5_REG_IN	I_V5_REG_IN - @m42a_lib.M42A	54A5	I_EXTUSB_OC_L	I_EXTUSB_OC_L - @m42a_lib.M42A	6C2 42C8	I_USB_C_OC_L	I_USB_C_OC_L - @m42a_lib.M42A	6C1 22C4 22D8	I_EXTUSB_OC_L	I_EXTUSB_OC_L - @m42a_lib.M42A	6C2	I_FWPWR_PWRON	I_FWPWR_PWRON - @m42a_lib.M42A	6D2 39C6	I_NC_FWPWR_PWRON	I_NC_FWPWR_PWRON - @m42a_lib.M42A	6D1	I_GND_BATT_CHGND	I_GND_BATT_CHGND - @m42a_lib.M42A	6D8 65A6 65A6	I_GND_CHASSIS_AUDIO_JACK	I_GND_CHASSIS_AUDIO_JACK - @m42a_lib.M42A	6D8 5688	I_GND_CHASSIS_AUDIO_MIC	I_GND_CHASSIS_AUDIO_MIC - @m42a_lib.M42A	6D8 57A6	I_GND_CHASSIS_DIPDIMM_LEFT	I_GND_CHASSIS_DIPDIMM_LEFT - @m42a_lib.M42A	6D8 28A5	I_GND_CHASSIS_DIPDIMM_RIGHT	I_GND_CHASSIS_DIPDIMM_RIGHT - @m42a_lib.M42A	6D8 28A5	I_GND_CHASSIS_AUDIO_SPKRCONN	I_GND_CHASSIS_AUDIO_SPKRCONN - @m42a_lib.M42A	6D8	I_GND_CHASSIS_AUDIO_SHIELD3	I_GND_CHASSIS_AUDIO_SHIELD3 - @m42a_lib.M42A	6D8	I_GND_CHASSIS_AUDIO_SHIELD2	I_GND_CHASSIS_AUDIO_SHIELD2 - @m42a_lib.M42A	6D8	I_GND_CHASSIS_AUDIO_SHIELD1	I_GND_CHASSIS_AUDIO_SHIELD1 - @m42a_lib.M42A	6D8	I_GND_CHASSIS_AUDIO_MIC	I_GND_CHASSIS_AUDIO_MIC - @m42a_lib.M42A	6D8 57A6	I_GND_CHASSIS_AUDIO_JACK	I_GND_CHASSIS_AUDIO_JACK - @m42a_lib.M42A	6D8 5688	I_GND_CHASSIS_DIPDIMM_CENTER	I_GND_CHASSIS_DIPDIMM_CENTER - @m42a_lib.M42A	6B8 28D5 29A5	I_GND_CHASSIS_DIPDIMM_CENTER	I_GND_CHASSIS_DIPDIMM_CENTER - @m42a_lib.M42A	6B7	I_GND_CHASSIS_DIPDIMM_RIGHT	I_GND_CHASSIS_DIPDIMM_RIGHT - @m42a_lib.M42A	6B8 29D4	I_GND_CHASSIS_DIPDIMM_LEFT	I_GND_CHASSIS_DIPDIMM_LEFT - @m42a_lib.M42A	6B7	I_GND_CHASSIS_FW_UPPER	I_GND_CHASSIS_FW_UPPER - @m42a_lib.M42A	6A6 39A1	I_GND_CHASSIS_TMSD_DOWN	I_GND_CHASSIS_TMSD_DOWN - @m42a_lib.M42A	6A6 69A3	I_GND_CHASSIS_I01	I_GND_CHASSIS_I01 - @m42a_lib.M42A	6A5	I_GND_CHASSIS_TMSD_DOWN	I_GND_CHASSIS_TMSD_DOWN - @m42a_lib.M42A	6A6 69A3	I_GND_CHASSIS_LVDS	I_GND_CHASSIS_LVDS - @m42a_lib.M42A	6C8 67A2 67B2																																																																														
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I_V5_REG_IN	I_V5_REG_IN - @m42a_lib.M42A	54A5																																																																																																																																																																																																																																																																																																																																																																																
I_EXTUSB_OC_L	I_EXTUSB_OC_L - @m42a_lib.M42A	6C2 42C8																																																																																																																																																																																																																																																																																																																																																																																
I_USB_C_OC_L	I_USB_C_OC_L - @m42a_lib.M42A	6C1 22C4 22D8																																																																																																																																																																																																																																																																																																																																																																																
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I_FWPWR_PWRON	I_FWPWR_PWRON - @m42a_lib.M42A	6D2 39C6																																																																																																																																																																																																																																																																																																																																																																																
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I_GND_BATT_CHGND	I_GND_BATT_CHGND - @m42a_lib.M42A	6D8 65A6 65A6																																																																																																																																																																																																																																																																																																																																																																																
I_GND_CHASSIS_AUDIO_JACK	I_GND_CHASSIS_AUDIO_JACK - @m42a_lib.M42A	6D8 5688																																																																																																																																																																																																																																																																																																																																																																																
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@m42a_lib.M42A	19D1 19D7 64C6		=P1V05_S0_CPU_NB - @m42a_lib.M42A	62A6 64D8		=P1V05_S0_NB_VTT - @m42a_lib.M42A	17D3 19B5 19D7 64C6		=P1V05_S0_CPU - @m42a_lib.M42A	7B5 7B6 7D5 7D5 8C7 9C8		11B3 11C5 64D6			=PVPVORE_S0_NB - @m42a_lib.M42A	16C8 16D3 19C8 19D7 64D6		P1V05_S0_CPU_NB - @m42a_lib.M42A	64D7		=PVPVORE_S0_NB - @m42a_lib.M42A	16C8 16D3 19C8 19D7 64D6		=P1V05_S0_NB_VTT - @m42a_lib.M42A	17D3 19B5 19D7 64C6		=P1V05_S0_NB - @m42a_lib.M42A	19D1 19D7 64C6		=P1V05_S0_CPU_NB - @m42a_lib.M42A	62A6 64D8		=P1V05_S0_CPU - @m42a_lib.M42A	7B5 7B6 7D5 7D5 8C7 9C8		11B3 11C5 64D6		=P1V05_S0_REG	=P1V05_S0_REG - @m42a_lib.M42A	5B2 62B1 64D8		=P1V05_S0_CPU_NB_SENSE - @m42a_lib.M42A	62A8 64D6		=P1V05_S0_SB_CFU_IO - @m42a_lib.M42A	21C1 21C1 24C3 25C4 64D6		=PVPVORE_S0_SB - @m42a_lib.M42A	24D3 25D3 64D6		P1V05_S0 - @m42a_lib.M42A	5B2 64D7		=PVPVORE_S0_SB - @m42a_lib.M42A	24D3 25D3 64D6		=P1V05_S0_SB_CFU_IO - @m42a_lib.M42A	21C1 21C1 24C3 25C4 64D6		=P1V05_S0_CPU_NB_SENSE - @m42a_lib.M42A	62A8 64D6	=P1V5_S0_NB	=P1V5_S0_NB - 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A							A
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CAP_402 m42a[62B3]	C7962 CAP_402 m42a[62C4]	C7964 CAP_402 m42a[62C3]	C7965 CAP_402 m42a[62B3]	C7966 CAP_402 m42a[62B3]	C7968 CAP_402 m42a[62B2]	C7969 CAP_402 m42a[62B2]	C7970 CAP_402 m42a[62B4]	C7980 CAP_P_CASED2E-SM m42a[62C4]	C7981 CAP_603 m42a[62C4]	C7989 CAP_402 m42a[62B4]	C7990 CAP_805 m42a[62A7]	C7991 CAP_805 m42a[62A7]	C7992 CAP_P_CASE-D2E-LF m42a[62B1]	C7999 CAP_402 m42a[62A6]	C8000 CAP_402 m42a[63D4]	C8005 CAP_402 m42a[63C4]	C8010 CAP_402 m42a[63C4]	C8015 CAP_402 m42a[63B4]	C8025 CAP_402 m42a[63A4]	C8060 CAP_402 m42a[63B3]	C8061 CAP_402 m42a[63B2]	C8062 CAP_402 m42a[63B2]	C8090 CAP_1206-1 m42a[63C3]	C8091 CAP_402 m42a[63D2]	C8092 CAP_402 m42a[63D1]	C8093 CAP_805 m42a[63D1]	C8202 CAP_402 m42a[65D7]	C8203 CAP_402 m42a[65C7]	C8205 CAP_402 m42a[65A5]	C8206 CAP_402 m42a[65A4]	C8209 CAP_402 m42a[65A5]	C8211 CAP_402 m42a[65A5]	C8215 CAP_402 m42a[65A4]	C8217 CAP_603 m42a[65C2]	C8218 CAP_402 m42a[65C4]	C8220 CAP_402 m42a[65A7]	C8221 CAP_402 m42a[65A7]	C8230 CAP_402 m42a[65C6]	C8300 CAP_402 m42a[66C7]	C8301 CAP_402 m42a[66C7]	C8302 CAP_402 m42a[66C7]	C8303 CAP_402 m42a[66C4]	C8304 CAP_402 m42a[66C5]	C8305 CAP_1206-1 m42a[66C4]	C8306 CAP_1206-1 m42a[66C3]	C8307 CAP_1206-1 m42a[66C3]	C8308 CAP_P_CASED2E-SM m42a[66B4]	C8309 CAP_P_6_3X5_5SM1 m42a[66B3]	C8310 CAP_P_CASED2E-SM m42a[66B3]	C8311 CAP_402 m42a[66C7]	C8312 CAP_402 m42a[66C5]	C8313 CAP_402 m42a[66C6]	C8316 CAP_402 m42a[66B4]	C8317 CAP_402 m42a[66B5]	C8318 CAP_402 m42a[66B4]	C8320 CAP_402 m42a[66B5]	C8321 CAP_402 m42a[66B5]	C8322 CAP_402 m42a[66B4]	C8323 CAP_402 m42a[66A5]	C8324 CAP_402 m42a[66A4]	C8325 CAP_402 m42a[66C7]	C8326 CAP_402 m42a[66C7]	C8327 CAP_402 m42a[66D7]	C8328 CAP_402 m42a[66B6]	C8340 CAP_402 m42a[66C7]	C8341 CAP_402 m42a[66B8]	C8370 CAP_402 m42a[66C3]	C8371 CAP_402 m42a[66C2]	C8372 CAP_402 m42a[66B1]	C8375 CAP_402 m42a[66B3]	C8381 CAP_603 m42a[66B3]	C8400 CAP_402 m42a[67C3]	C9401 CAP_402 m42a[67C3]	C9402 CAP_402 m42a[67C3]	C9403 CAP_402 m42a[67C3]	C9408 CAP_402 m42a[67A3]	C9409 CAP_402 m42a[67B2]	C9410 CAP_402 m42a[67A3]	C9411 CAP_402 m42a[67B5]	C9412 CAP_603 m42a[67B5]	C9413 CAP_402 m42a[67B6]	C9414 CAP_402 m42a[67D5]	C9415 CAP_402 m42a[67A3]	C9416 CAP_402 m42a[67A4]	C9459 CAP_402 m42a[68D5]	C9500 CAP_402 m42a[68D5]	C9501 CAP_402 m42a[68D4]	C9502 CAP_402 m42a[68D4]	C9503 CAP_402 m42a[68D4]	C9504 CAP_603 m42a[68D4]	C9505 CAP_603 m42a[68B2]	C9506 CAP_402 m42a[68C7]	C9507 CAP_402 m42a[68D5]	C9508 CAP_402 m42a[61C4]	C9509 CAP_402 m42a[68D4]	C9510 CAP_402 m42a[68D4]	C9511 CAP_402 m42a[68D4]	C9512 CAP_402 m42a[68D3]	C9513 CAP_603 m42a[68D3]	C9514 CAP_402 m42a[68D7]	C9519 CAP_402 m42a[68B6]	C9520 CAP_402 m42a[68B6]	C9521 CAP_402 m42a[68B3]	C9522 CAP_402 m42a[68B2]	C9523 CAP_402 m42a[68D2]	C9524 CAP_402 m42a[68C2]	C9525 CAP_402 m42a[68C2]	C9526 CAP_402 m42a[68C3]	C9527 CAP_402 m42a[68C1]	C9530 CAP_402 m42a[68D7]	C9531 CAP_402 m42a[68D7]	C9532 CAP_402 m42a[68C7]	C9533 CAP_402 m42a[68C7]	C9534 CAP_402 m42a[68C7]	C9535 CAP_402 m42a[68C7]	C9536 CAP_402 m42a[68D7]	C9537 CAP_402 m42a[68D7]	C9538 CAP_402 m42a[68D7]	C9539 CAP_402 m42a[68D7]	C9540 CAP_603 m42a[68D6]	C9541 CAP_402 m42a[68B5]	C9542 CAP_402 m42a[68B5]	C9543 CAP_402 m42a[68B5]	C9544 CAP_402 m42a[68B5]	C9545 CAP_402 m42a[68B5]	C9546 CAP_402 m42a[68B4]	C9547 CAP_402 m42a[68B4]	C9548 CAP_402 m42a[68B4]	C9804 CAP_402 m42a[69C4]	C9808 CAP_402 m42a[69C5]	C9809 CAP_402 m42a[69B5]	C9812 CAP_402 m42a[69B5]	C9820 CAP_402 m42a[69A4]	C9821 CAP_402 m42a[69A3]	C9824 CAP_402 m42a[69B5]	C9834 CAP_402 m42a[69A4]	C9839 CAP_402 m42a[69B7]	C9842 CAP_402 m42a[69C1]	C9843 CAP_402 m42a[69C1]	C9860 CAP_402 m42a[69C2]	D1986 DIODE_SCHOT_6PB_SOT-363 m42a[19C2 19D2]	D2502 DIODE_SCHOT_6PB_SOT-363 m42a[25C8 25D8]	D2600 DIODE_SCHOT_6PB_SOT-363 m42a[26D5 26D5]	D4520 DIODE_DUAL_6P_SOT-36 m42a[39B4 39B3]	D4521 DIODE_DUAL_6P_SOT-36 m42a[39A4 39A3]	D4550 ZENER_SOT23 m42a[39A6]	D4590 DIODE_SCHOT_SMB m42a[39D4]	D4591 DPAK3P_SOT-363 m42a[39C5 39C5]	D4900 DIODE_SCHOT_3P_A_SC-75 m42a[40C6]	D5200 DIODE_SCHOT_3P_A_SC-75 m42a[42C3]	D5201 DIODE_SCHOT_3P_A_SC-75 m42a[42A3]	D7500 DIODE_SCHOT_SMB m42a[58C3]	D7501 DIODE_SCHOT_SMB m42a[58B3]	D7624 DIODE_SCHOT_SOD-323 m42a[59C6]	D7664 DIODE_SCHOT_SOD-323 m42a[59C3]	D7820 DIODE_SCHOT_SMB m42a[61B4]	D7921 DIODE_SMB m42a[62B7]	D7924 DIODE_SCHOT_SOD-323 m42a[62C6]	D7961 DIODE_SMB m42a[62B2]	D7964 DIODE_SCHOT_SOD-323 m42a[62C3]	D8200 DIODE_SCHOT_3P_A_SC-75 m42a[65C7]	D8201 DPAK3P_SOT-363 m42a[65D4]	D8201 DPAK3P_SOT-363 m42a[66B3]	D8300 DIODE_SCHOT_SOD-123 m42a[66C5]	D8322 DPAK3P_SOT-363 m42a[66C8 66A5 66A6]	D9500 DIODE_DUAL_6P_SOT-36 m42a[68A7 68B7]	D27300 SUPPR_TRANSIENT_4P1-0405 m42a[56C6]	D27301 SUPPR_TRANSIENT_4P1-0405 m42a[56C6]	D27350 SUPPR_TRANSIENT_4P1-0405 m42a[56A6]	D27351 SUPPR_TRANSIENT_4P1-0405 m42a[56A6]	F8200 FUSE_1206 m42a[65D6]	F8300 FUSE_1206 m42a[66C3]	F9804 FUSE_SM-LF m42a[69C5]	FL4520 FILTER_4P_2012 m42a[39B3]	FL4521 FILTER_4P_2012 m42a[39B3]	FL4590 FUSE_MINISMD m42a[39D5]	FL9800 FILTER_IC_SM-220MHZ-LF m42a[69A5]	FL9801 FILTER_IC_SM-220MHZ-LF m42a[69A5]	FL9802 FILTER_IC_SM-220MHZ-LF m42a[69A5]	GV3901 HOLE_VIA m42a[35C2]	GV3902 HOLE_VIA m42a[35C2]	GV3903 HOLE_VIA m42a[35C2]	GV3904 HOLE_VIA m42a[35C2]	GV3905 HOLE_VIA m42a[35B2]	GV3906 HOLE_VIA m42a[35B2]	GV3907 HOLE_VIA m42a[35B2]	GV3908 HOLE_VIA m42a[35B2]	J1102 CON_F30STSM_5047_SML m42a[11B2]	J2600 CON_F2RT_S2MT_SM_F-R m42a[26D6]	J2801 CON_F200RT_DDR2DIMM m42a[28D6]	J2901 TH1_F-RT-TH2 m42a[29D5]	J3801 CON_M50ST_D2MT_SM_M-ST m42a[34C4]	J3901 CON_F19ST_S2MT_SM_F-ST m42a[35D8]	J4200 CON_RJ45_8RT_S2MT_SM m42a[37C2]	J4500 CON_F8RT_S2MT_TH_F-R m42a[39B2]	J4900 CON_F10ST_D_SMA_F-ST m42a[40C4]	J5200 CON_F4RT_USB_S2MT_TH m42a[42D1]	J5201 CON_F4RT_USB_S2MT_TH m42a[42B1]	J5300 CON_F52RT_D2MT_SM_F-S m42a[43C5]	J5400 CON_F4ST_S2MT_SM_F-S m42a[44C4]	J6000 CON_F30STSM_5047_SML m42a[47C6]	J6250 CON_F2ST_S2MT_SM_F-S m42a[49C6]	J6251 CON_F2ST_S2MT_SM_F-S m42a[49A6]	J6501 CON_F4ST_S2MT_SM_F-S m42a[51C3]	J7300 CON_F8RT_2MT_AUDIOIO m42a[56C8]	J7301 T_TH1_F-RT-TH2 m42a[56D1]	J7302 CON_F2ST_S2MT_SM_F-S m42a[56D1]	J7303 CON_F4ST_S2MT_SM_F-S m42a[56C1]	J7350 CON_F8RT_2MT_AUDIOIO m42a[56B8]	J8200 CON_M5RT_S_SM_M-RT-S m42a[65D7]	J8250 CON_F20ST_D_SM_F-ST-SM1 m42a[65B6]	J9400 CON_F4ST_S2MT_SM_F-S m42a[67D2]	J9401 CON_F22RT_S4MT_SM_F-RT-SM m42a[67B1]	J9801 CON_DVI_30RT_Q4MT_TH1_RT-TH m42a[69B4]	L1922 IND_0603 m42a[19A7]	L1934 IND_0603 m42a[19C5]	L1936 IND_0603 m42a[19C5]	L1970 IND_1210 m42a[19B4]	L1975 IND_0805 m42a[19A4]	L1985 IND_0603 m42a[19D3]	L1990 IND_0603 m42a[19C3]	L2500 IND_SM-3 m42a[25B8]	L2507 IND_1206 m42a[25A7]	L3301 IND_0402-LF m42a[32D7]	L3302 IND_0402-LF m42a[32D3]	L3901 FILTER_4P_2012H m42a[35D6]	L3902 FILTER_4P_2012H m42a[35D5]	L3912 IND_0402 m42a[35C6]	L4100 IND_0402-LF m42a[36D3]	L4250 IND_0402-LF m42a[37D7]	L4400 IND_0402 m42a[38D4]	L4510 IND_SM m42a[39C3]	L4550 IND_SM-1 m42a[39A7]	L4900 IND_0402 m42a[40D5]	L4901 FILTER_4P_SM m42a[40C6]	L4902 IND_0402 m42a[40C5]	L5200 FILTER_4P_SM m42a[42C4]	L5201 FILTER_4P_SM m42a[42B4]	L5202 IND_0402-LF m42a[42D4]	L5203 IND_0402-LF m42a[42C4]	L5204 IND_0402-LF m42a[42C3]	L5205 IND_0402-LF m42a[42B3]	L5400 FILTER_4P_SM m42a[44B5]	L5410 IND_0402-LF m42a[44C5]	L5411 IND_0402-LF m42a[44B5]	L5910 IND_0603 m42a[46A7]	L6800 IND_0402 m42a[54A5]	L6801 IND_0402 m42a[54D6]	L7200 IND_0402 m42a[55C7]	L7210 IND_0402 m42a[55A7]	L7220 IND_0402 m42a[55B7]	L7230 IND_0402 m42a[55A7]	L7300 IND_0402-LF m42a[56D6]	L7301 IND_0402-LF m42a[56D4]	L7302 IND_0402 m42a[56D6]	L7303 IND_0402 m42a[56C6]	L7304 IND_0402 m42a[56C4]	L7305 IND_0402 m42a[56C6]	L7306 IND_0402 m42a[56C4]	L7307 IND_0402 m42a[56D6]	L7350 IND_0402 m42a[56B6]	L7351 IND_0402 m42a[56B4]	L7352 IND_0402 m42a[56B6]	L7353 IND_0402 m42a[56B6]	L7354 IND_0402 m42a[56B4]	L7355 IND_0402 m42a[56B6]	L7356 IND_0402 m42a[56B4]	L7357 IND_0402 m42a[56A6]	L7370 IND_0402 m42a[56B2]	L7371 IND_0402 m42a[56B1]	L7372 IND_0402 m42a[56B2]	L7373 IND_0402 m42a[56B1]	L7374 IND_0402 m42a[56B2]	L7375 IND_0402 m42a[56B1]	L7390 IND_0402 m42a[56D8]	L7400 IND_0402 m42a[57B4]	L7500 IND_SM m42a[58D2]	L7501 IND_SM m42a[58B2]	L7620 IND_0402-LF m42a[59B7]	L7680 IND_SM m42a[59B2]	L7820 IND_3P_SM m42a[61B3]	L7920 IND_SM m42a[62B7]	L7960 IND_3P_SM m42a[62B2]	L8090 IND_CDPH4D19F-SM m42a[63D1]	L8201 IND_SM-LF m42a[65A3]	L8202 IND_0402-LF m42a[65A3]	L8203 IND_0402-LF m42a[65A3]	L8204 IND_0402-LF m42a[65A3]	L8205 IND_SM-LF m42a[65A3]	L8207 IND_0402 m42a[65A7]	L8208 IND_0402 m42a[65A7]	L8209 IND_0402 m42a[65A7]	L8300 IND_3P_SM m42a[66C4]	L9400 IND_0402-LF m42a[67D4]	L9401 IND_0402-LF m42a[67C4]	L9402 IND_0402-LF m42a[67D4]	L9403 IND_0402-LF m42a[67D4]	L9404 IND_0402-LF m42a[67B4]	L9405 IND_0402-LF m42a[67A4]	L9407 FILTER_4P_SM m42a[67A4]	L9408 IND_0402-LF m42a[67B4]	L9500 IND_0402-LF m42a[68D5]	L9501 IND_0402-LF m42a[68D5]	L9503 IND_0402-LF m42a[68D8]	L9504 IND_0402-LF m42a[68C8]	L9505 IND_0402-LF m42a[68C8]	L9506 IND_0402-LF m42a[68D8]	L9804 FILTER_4P_SM m42a[69A2]	L9805 FILTER_4P_2012H m42a[69B2]	L9806 FILTER_4P_2012H m42a[69B2]	L9807 FILTER_4P_2012H m42a[69B2]	L9844 IND_SM-1 m42a[69C4]	Q2680 TRA_SINGLE_MOSFET_NC m42a[26A3]	Q3810 TRA_FDC638P_SM-LF m42a[34C5]	Q3875 TRA_2N7002DW_SOT-363 m42a[34C6 34C7]	Q4590 TRA_FDC638P_SM-LF m42a[39D5]	Q5291 TRA_2N7002_SOT23-LF m42a[39C5]	Q5901 TRA_2N7002DW_SOT-363 m42a[46B4 46B5]	Q5950 TRA_2N3906_SOT23-LF m42a[46A3]	Q5952 TRA_2N7002_SOT23-LF m42a[46A3]	Q6100 TRA_S13446DV_TSOP-LF m42a[48A5]	Q6101 TRA_2N7002DW_SOT-363 m42a[48A6 48A7]	Q6150 TRA_TP0610_SOT23-3 m42a[48C6]	Q6151 TRA_2N7002_SOT23-LF m42a[48C7]	Q6152 TRA_TP0610_SOT23-3 m42a[48C7]	Q6153 TRA_TP0610_SOT23-3 m42a[48C8]	Q6200 TRA_B0846M3T5G_NFN_SOT732-3 m42a[49B6]	Q6560 TRA_2N7002_SOT23-LF m42a[51B3]	Q6650 TRA_2N7002_SOT23-LF m42a[52B6]	Q6651 TRA_TP0610_SOT23-3 m42a[52B6]	Q7400 TRA_2N7002DW_SOT-363 m42a[57C7 57D7]	Q7401 TRA_2N7002DW_SOT-363 m42a[57D5 57D6]	Q7402 TRA_2N7002DW_SOT-363 m42a[57B7 57C5]	Q7500 TRA_HAT2168H_LFPAK m42a[58D3]	Q7501 TRA_HAT2165H_LFPAK m42a[58D4]

	8	7	6	5	4	3	2	1
	Q7502 TRA_HAT216RH_LFFPAK m42a[58C3]		R2079 RES_402 m42a[20B7]		R3404 RES_402 m42a[33D1]		R5905 RES_402 m42a[46D4]	
	Q7503 TRA_HAT2165H_LFFPAK m42a[58B4]		R2085 RES_402 m42a[20C4]		R3405 RES_402 m42a[33C1]		R5906 RES_402 m42a[46D4]	
	Q7504 TRA_HAT2165H_LFFPAK m42a[58D3]		R2100 RES_402 m42a[21C3]		R3406 RES_402 m42a[33B1]		R5910 RES_603 m42a[46C8]	
	Q7505 TRA_HAT2165H_LFFPAK m42a[58B3]		R2101 RES_402 m42a[21C4]		R3407 RES_402 m42a[33B1]		R5911 RES_402 m42a[46A6]	
	Q7620 TRA_STL8NH31L_COMBO m42a[59C7]		R2105 RES_402 m42a[21D6]		R3408 RES_402 m42a[33C1]		R5918 RES_402 m42a[46C5]	
	Q7621 TRA_STL8NH31L_COMBO m42a[59B7]		R2107 RES_402 m42a[21C2]		R3409 RES_402 m42a[33C1]		R5919 RES_402 m42a[46C5]	
	Q7660 TRA_STL8NH31L_COMBO m42a[59C3]		R2108 RES_402 m42a[21C2]		R3410 RES_402 m42a[33C1]		R5920 RES_402 m42a[46C5]	
	Q7661 TRA_STL8NH31L_COMBO m42a[59B3]		R2110 RES_402 m42a[21C2]		R3411 RES_402 m42a[33D4]		R5922 RES_402 m42a[46C5]	
	Q7750 TRA_2N7002DW_SOT-363 m42a[60C6 60C7]		R2194 RES_402 m42a[21D4]		R3412 RES_402 m42a[33D4]		R5923 RES_402 m42a[46C5]	
	Q7820 TRA_IRF7821_SO-8 m42a[61C4]		R2195 RES_402 m42a[21C6]		R3413 RES_402 m42a[33D4]		R5924 RES_402 m42a[46C5]	
	Q7821 TRA_IRF7821_SO-8 m42a[61B4]		R2196 RES_402 m42a[21C6]		R3414 RES_402 m42a[33D4]		R5925 RES_402 m42a[46C5]	
	Q7920 TRA_IRF7821_SO-8 m42a[62C6]		R2197 RES_402 m42a[21C6]		R3415 RES_402 m42a[33D4]		R5926 RES_402 m42a[46C4]	
	Q7921 TRA_IRF7821_SO-8 m42a[62B6]		R2198 RES_402 m42a[21C6]		R3416 RES_402 m42a[33D4]		R5927 RES_402 m42a[46C5]	
	Q7960 TRA_IRF7821_SO-8 m42a[62C3]		R2199 RES_402 m42a[21C3]		R3417 RES_402 m42a[33C7]		R5928 RES_402 m42a[46D4]	
	Q7961 TRA_IRF7821_SO-8 m42a[62B3]		R2200 RES_402 m42a[22D7]		R3418 RES_402 m42a[33B4]		R5929 RES_402 m42a[46C5]	
	Q8000 TRA_FDC638P_SM-LF m42a[63D4]		R2203 RES_402 m42a[22C2]		R3419 RES_402 m42a[33B4]		R5930 RES_402 m42a[46C5]	
	Q8005 TRA_STL8NH31L_COMBO m42a[63C4]		R2204 RES_402 m42a[22C2]		R3420 RES_402 m42a[33A4]		R5931 RES_402 m42a[46C4]	
	Q8010 TRA_FDC638P_SM-LF m42a[63D4]		R2205 RES_402 m42a[22C6]		R3421 RES_402 m42a[33C4]		R5932 RES_402 m42a[46C4]	
	Q8015 TRA_STL8NH31L_COMBO m42a[63C4]		R2206 RES_402 m42a[22C5]		R3422 RES_402 m42a[33C4]		R5933 RES_402 m42a[46C4]	
	Q8025 TRA_S13447BDV_SOT-6 m42a[63A4]		R2207 RES_402 m42a[22C5]		R3423 RES_402 m42a[33C4]		R5934 RES_402 m42a[46C5]	
	Q8030 TRA_2N7002DW_SOT-363 m42a[63A6 63B6]		R2208 RES_402 m42a[22D5]		R3426 RES_402 m42a[33C4]		R5935 RES_402 m42a[46C4]	
	Q8031 TRA_2N7002DW_SOT-363 m42a[63D6 63A6]		R2211 RES_402 m42a[22B3]		R3427 RES_402 m42a[33C4]		R5936 RES_402 m42a[46C5]	
	Q8059 TRA_2N7002DW_SOT-363 m42a[63C7 63C7]		R2223 RES_402 m42a[22D6]		R3428 RES_402 m42a[33C4]		R5937 RES_402 m42a[46C4]	
	Q8060 TRA_2N7002_SOT23-LF m42a[63C8]		R2225 RES_402 m42a[22D7]		R3429 RES_402 m42a[33D8]		R5938 RES_402 m42a[46C5]	
	Q8061 TRA_2N7002DW_SOT-363 m42a[63B7 63B7]		R2226 RES_402 m42a[22D5]		R3430 RES_402 m42a[33D7]		R5939 RES_402 m42a[46C4]	
	Q8062 TRA_2N7002_SOT23-LF m42a[63B8]		R2250 RES_402 m42a[22D7]		R3431 RES_402 m42a[33B1]		R5940 RES_402 m42a[46C5]	
	Q8063 TRA_2N7002_SOT23-LF m42a[63B4]		R2251 RES_402 m42a[22D6]		R3432 RES_402 m42a[33D7]		R5941 RES_402 m42a[46C4]	
	Q8210 TRA_2N7002DW_SOT-363 m42a[65C6 65C3]		R2255 RES_402 m42a[22D7]		R3433 RES_402 m42a[33B8]		R5942 RES_402 m42a[46C5]	
	Q8220 TRA_2N7002DW_SOT-363 m42a[65C7 65C6]		R2299 RES_402 m42a[22B5]		R3434 RES_402 m42a[33D4]		R5943 RES_402 m42a[46B4]	
	Q8240 TRA_TP0610_SOT23-3 m42a[65C5]		R2300 RES_402 m42a[23C7]		R3435 RES_402 m42a[33C4]		R5944 RES_402 m42a[46B4]	
	Q8250 TRA_S14405DY_SO-8 m42a[66C9]		R2302 RES_402 m42a[23D3]		R3436 RES_402 m42a[33B1]		R5945 RES_402 m42a[46C4]	
	Q8298 TRA_TP0610_SOT23-3 m42a[65C7]		R2303 RES_402 m42a[23D3]		R3437 RES_402 m42a[33B1]		R5946 RES_402 m42a[46C4]	
	Q8299 TRA_2N7002_SOT23-LF m42a[65C7]		R2305 RES_402 m42a[23D3]		R3438 RES_402 m42a[33D1]		R5947 RES_402 m42a[46B4]	
	Q8300 TRA_S14405DY_SO-8 m42a[66D5]		R2306 RES_402 m42a[23B7]		R3439 RES_402 m42a[33D1]		R5948 RES_402 m42a[46C5]	
	Q8301 TRA_HAT2168H_LFFPAK m42a[66C4]		R2307 RES_402 m42a[23A7]		R3440 RES_402 m42a[33D1]		R5949 RES_402 m42a[46C4]	
	Q8302 TRA_HAT2165H_LFFPAK m42a[66B4]		R2308 RES_402 m42a[23B7]		R3441 RES_402 m42a[33D1]		R5950 RES_402 m42a[46A3]	
	Q8320 TRA_S14405DY_SO-8 m42a[66B3]		R2309 RES_402 m42a[23A7]		R3442 RES_402 m42a[33C1]		R5951 RES_402 m42a[46A3]	
	Q8321 TRA_S14405DY_SO-8 m42a[66B3]		R2310 RES_402 m42a[23A7]		R3443 RES_402 m42a[33C7]		R5952 RES_402 m42a[46A3]	
	Q8322 TRA_2N7002DW_SOT-363 m42a[66A4 66A4]		R2311 RES_402 m42a[23A7]		R3451 RES_402 m42a[33B7]		R5953 RES_402 m42a[46D5]	
	Q8324 TRA_2N7002DW_SOT-363 m42a[66A3 66A4]		R2312 RES_402 m42a[23A3]		R3452 RES_402 m42a[33B7]		R5954 RES_402 m42a[46B5]	
	Q8340 TRA_REL5203_SM m42a[66A9]		R2313 RES_402 m42a[23A7]		R3453 RES_402 m42a[33B7]		R5955 RES_402 m42a[46B5]	
	Q8350 TRA_2N7002_SOT23-LF m42a[66A6]		R2314 RES_402 m42a[23A7]		R3454 RES_402 m42a[33B7]		R5970 RES_402 m42a[46D3]	
	Q9403 TRA_FDC638P_SM-LF m42a[67B6]		R2315 RES_402 m42a[23A3]		R3463 RES_402 m42a[33D7]		R5971 RES_402 m42a[46D3]	
	Q9404 TRA_2N7002_SOT23-LF m42a[67B7]		R2316 RES_402 m42a[23D7]		R3465 RES_402 m42a[33C4]		R5972 RES_402 m42a[46C7]	
	Q9405 TRA_TP0610_SOT23-3 m42a[67D5]		R2317 RES_402 m42a[23D7]		R3466 RES_402 m42a[33A7]		R5973 RES_402 m42a[46C5]	
	Q9406 TRA_2N7002_SOT23-LF m42a[67D6]		R2318 RES_402 m42a[23D7]		R3467 RES_402 m42a[33A7]		R5976 RES_402 m42a[46D1]	
	Q9801 TRA_2N7002DW_SOT-363 m42a[69D6 69D6]		R2319 RES_402 m42a[23D2]		R3468 RES_402 m42a[33C7]		R5980 RES_402 m42a[46D5]	
	R0610 RES_402 m42a[6A7]		R2320 RES_402 m42a[23D7]		R3469 RES_402 m42a[33C7]		R5981 RES_402 m42a[46D5]	
	R0611 RES_402 m42a[6A8]		R2323 RES_402 m42a[23D5]		R3470 RES_402 m42a[33C7]		R5982 RES_402 m42a[46D5]	
	R0612 RES_402 m42a[6A8]		R2326 RES_402 m42a[23D6]		R3471 RES_402 m42a[33B7]		R5983 RES_402 m42a[46C5]	
	R0621 RES_402 m42a[6A7]		R2327 RES_402 m42a[23D6]		R3472 RES_402 m42a[33B7]		R5984 RES_402 m42a[46C5]	
	R0702 RES_402 m42a[7D5]		R2343 RES_402 m42a[23D1]		R3473 RES_402 m42a[33B7]		R5985 RES_402 m42a[46C5]	
	R0703 RES_402 m42a[7C5]		R2388 RES_402 m42a[23B2]		R3474 RES_402 m42a[33B8]		R5986 RES_402 m42a[46C5]	
	R0704 RES_402 m42a[7C5]		R2389 RES_402 m42a[23A4]		R3475 RES_402 m42a[33B7]		R5987 RES_402 m42a[46C5]	
	R0705 RES_402 m42a[7B4]		R2390 RES_402 m42a[23B3]		R3476 RES_402 m42a[33A7]		R5988 RES_402 m42a[46B5]	
	R0706 RES_402 m42a[7B4]		R2395 RES_402 m42a[23D7]		R3477 RES_402 m42a[33B4]		R5989 RES_402 m42a[46D5]	
	R0707 RES_402 m42a[7A4]		R2396 RES_402 m42a[23D6]		R3478 RES_402 m42a[33A4]		R5990 RES_402 m42a[46B2]	
	R0712 RES_402 m42a[7A4]		R2397 RES_402 m42a[23D6]		R3480 RES_402 m42a[33C7]		R5991 RES_402 m42a[46B2]	
	R0716 RES_402 m42a[7B2]		R2398 RES_402 m42a[23D8]		R3481 RES_402 m42a[33B1]		R5992 RES_402 m42a[46B2]	
	R0717 RES_402 m42a[7B2]		R2399 RES_402 m42a[23C1]		R3482 RES_402 m42a[33B1]		R5993 RES_402 m42a[46B2]	
	R0718 RES_402 m42a[7B2]		R2500 RES_603 m42a[25A8]		R3490 RES_402 m42a[33A4]		R5994 RES_402 m42a[46D5]	
	R0719 RES_402 m42a[7B2]		R2501 RES_402 m42a[25C8]		R3824 RES_402 m42a[34C4]		R5995 RES_402 m42a[46D5]	
	R0720 RES_402 m42a[7B7]		R2502 RES_402 m42a[25D8]		R3825 RES_402 m42a[34C5]		R5996 RES_402 m42a[46B4]	
	R0721 RES_402 m42a[7B7]		R2600 RES_402 m42a[26D4]		R3851 RES_402 m42a[34C4]		R5997 RES_402 m42a[46B4]	
	R0722 RES_402 m42a[7A7]		R2606 RES_402 m42a[26D5]		R3853 RES_402 m42a[34C3]		R5998 RES_402 m42a[46B4]	
	R0730 RES_402 m42a[7A4]		R2607 RES_402 m42a[26D5]		R3858 RES_402 m42a[34B5]		R5999 RES_402 m42a[46C1]	
	R0802 RES_402 m42a[8B6]		R2609 RES_402 m42a[26C7]		R3859 RES_402 m42a[34B4]		R6100 RES_402 m42a[48D3]	
	R0803 RES_402 m42a[8A7]		R2610 RES_402 m42a[26C7]		R3865 RES_402 m42a[34C6]		R6101 RES_402 m42a[48C2]	
	R0921 RES_402 m42a[9D2]		R2611 RES_402 m42a[26B5]		R3876 RES_402 m42a[34C7]		R6102 RES_402 m42a[48C3]	
	R0922 RES_402 m42a[9D2]		R2612 RES_402 m42a[26A5]		R3877 RES_402 m42a[34C6]		R6103 RES_402 m42a[48C3]	
	R0923 RES_402 m42a[9C2]		R2622 RES_402 m42a[26A5]		R3900 RES_402 m42a[35D3]		R6105 RES_402 m42a[48D4]	
	R0924 RES_402 m42a[9C2]		R2636 RES_402 m42a[26C2]		R3901 RES_402 m42a[35C3]		R6106 RES_402 m42a[48C4]	
	R0925 RES_402 m42a[9C2]		R2637 RES_402 m42a[26C2]		R3950 RES_402 m42a[35B7]		R6107 RES_402 m42a[48D4]	
	R0926 RES_402 m42a[9C2]		R2638 RES_402 m42a[26C2]		R4101 RES_402 m42a[36D8]		R6108 RES_402 m42a[48C4]	
	R1001 RES_402 m42a[10B6]		R2639 RES_402 m42a[26C2]		R4102 RES_402 m42a[36C8]		R6112 RES_402 m42a[48B2]	
	R1002 RES_402 m42a[10B6]		R2640 RES_402 m42a[26C2]		R4103 RES_402 m42a[36A4]		R6140 RES_402 m42a[48A7]	
	R1005 RES_402 m42a[10C4]		R2641 RES_402 m42a[26C2]		R4104 RES_402 m42a[36B4]		R6141 RES_402 m42a[48A7]	
	R1106 RES_402 m42a[10C3]		R2642 RES_402 m42a[26C2]		R4105 RES_402 m42a[36B4]		R6142 RES_402 m42a[48A6]	
	R1107 RES_402 m42a[10C4]		R2643 RES_402 m42a[26C2]		R4106 RES_402 m42a[36B5]		R6143 RES_1206 m42a[48A4]	
	R1108 RES_402 m42a[10C4]		R2680 RES_402 m42a[26B3]		R4107 RES_402 m42a[36D8]		R6144 RES_402 m42a[48A6]	
	R1109 RES_402 m42a[10C3]		R2681 RES_402 m42a[26B2]		R4117 RES_402 m42a[36B3]		R6150 RES_402 m42a[48C6]	
	R1110 RES_402 m42a[11B4]		R2682 RES_402 m42a[26A2]		R4118 RES_402 m42a[36B3]		R6151 RES_402 m42a[48B6]	
	R1101 RES_402 m42a[11C5]		R2683 RES_402 m42a[26B2]		R4119 RES_402 m42a[36B3]		R6152 RES_402 m42a[48C7]	
	R1102 RES_402 m42a[11B4]		R2684 RES_402 m42a[26B2]		R4120 RES_402 m42a[36B4]		R6153 RES_402 m42a[48B7]	
	R1103 RES_402 m42a[11C5]		R2685 RES_402 m42a[26B2]		R4122 RES_402 m42a[36A3]		R6200 RES_402 m42a[49C5]	
	R1104 RES_402 m42a[11B5]		R2687 RES_402 m42a[26A2]		R4123 RES_402 m42a[36A2]		R6201 RES_402 m42a[49D3]	
	R1106 RES_402 m42a[11A3]		R2688 RES_402 m42a[26A3]		R4124 RES_402 m42a[36A2]		R6203 RES_402 m42a[49D3]	
	R1210 RES_402 m42a[12C3]		R2689 RES_402 m42a[26A2]		R4130 RES_402 m42a[36B6]		R6251 RES_402 m42a[49A5]	
	R1211 RES_402 m42a[12C3]		R2696 RES_402 m42a[26C6]		R4131 RES_402 m42a[36B6]		R6252 RES_402 m42a[49B3]	
	R1220 RES_402 m42a[12B7]		R2697 RES_402 m42a[26C5]		R4200 RES_402 m42a[37A6]		R6253 RES_402 m42a[50D4]	
	R1221 RES_402 m42a[12B7]		R2700 RES_402 m42a[27D7]		R4201 RES_402 m42a[37A5]		R6302 RES_402 m42a[50D4]	
	R1225 RES_402 m42a[12B7]		R2701 RES_402 m42a[27D7]		R4202 RES_402 m42a[37A5]		R6303 RES_402 m42a[50C3]	
	R1226 RES_402 m42a[12B7]		R2750 RES_402 m42a[27D4]		R4203 RES_402 m42a[37A5]			

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D	R7210 RES_402 m42a[55A7]	R7260 RES_402 m42a[55D2]	R7261 RES_402 m42a[55C2]	R7270 RES_402 m42a[55C2]	R7271 RES_402 m42a[55C2]	R7280 RES_402 m42a[55B2]	R7281 RES_402 m42a[55B2]	R7300 RES_402 m42a[56C4]	R7301 RES_402 m42a[56C4]	R7320 RES_402 m42a[56B5]	R7321 RES_402 m42a[56D7]	R7322 RES_402 m42a[56B7]	R7349 RES_402 m42a[56B7]	R7350 RES_402 m42a[56A4]	R7351 RES_402 m42a[56A4]	R7380 RES_402 m42a[56C2]	R7382 RES_402 m42a[56B2]	R7391 RES_402 m42a[56C7]	R7401 RES_402 m42a[57D8]	R7402 RES_402 m42a[57D7]	R7403 RES_402 m42a[57C7]	R7404 RES_402 m42a[57C4]	R7405 RES_402 m42a[57D5]	R7406 RES_402 m42a[57D6]	R7411 RES_402 m42a[57C8]	R7412 RES_402 m42a[57B7]	R7413 RES_402 m42a[57C6]	R7414 RES_402 m42a[57C4]	R7415 RES_402 m42a[57C5]	R7430 RES_603 m42a[57C3]	R7431 RES_603 m42a[57B3]	R7432 RES_402 m42a[57B3]	R7433 RES_402 m42a[57A3]	R7434 RES_402 m42a[57C2]	R7435 RES_402 m42a[57C2]	R7436 RES_402 m42a[57B2]	R7437 RES_402 m42a[57B2]	R7438 RES_402 m42a[57C2]	R7439 RES_402 m42a[57B2]	R7440 RES_402 m42a[57A5]	R7450 RES_402 m42a[57A7]	R7451 RES_402 m42a[57A7]	R7452 RES_402 m42a[57A7]	R7453 RES_402 m42a[57A7]	R7454 RES_402 m42a[57A7]	R7460 RES_402 m42a[57C6]	R7461 RES_402 m42a[57C7]	R7500 RES_402 m42a[58C2]	R7501 RES_402 m42a[58C2]	R7502 RES_805 m42a[58B3]	R7503 RES_805 m42a[58D3]	R7504 RES_402 m42a[58C1]	R7505 RES_402 m42a[58B2]	R7506 RES_402 m42a[58C7]	R7507 RES_402 m42a[58B1]	R7508 RES_402 m42a[58B8]	R7509 RES_402 m42a[58B8]	R7510 RES_402 m42a[58B6]	R7511 RES_402 m42a[58B8]	R7512 RES_402 m42a[58D7]	R7513 RES_402 m42a[58B7]	R7514 RES_402 m42a[58B8]	R7515 RES_402 m42a[58B5]	R7516 RES_402 m42a[58B4]	R7517 RES_402 m42a[58B5]	R7518 RES_402 m42a[58B5]	R7519 RES_402 m42a[58C7]	R7520 RES_402 m42a[58D7]	R7521 RES_402 m42a[58D8]	R7522 RES_402 m42a[58A5]	R7523 RES_402 m42a[58A6]	R7524 RES_402 m42a[58D5]	R7525 RES_402 m42a[58C5]	R7526 THERMIST_402 m42a[58C7]	R7527 RES_402 m42a[58C8]	R7530 RES_402 m42a[58B4]	R7531 THERMIST_0603-LF m42a[58B4]	R7543 RES_402 m42a[58B2]	R7545 RES_402 m42a[58C7]	R7600 RES_402 m42a[59C5]	R7603 RES_402 m42a[59A3]	R7604 RES_402 m42a[59A3]	R7606 RES_402 m42a[59A3]	R7607 RES_402 m42a[59A3]	R7621 RES_402 m42a[59C7]	R7624 RES_402 m42a[59C5]	R7625 RES_402 m42a[59B6]	R7626 RES_402 m42a[59C7]	R7627 RES_402 m42a[59B7]	R7628 RES_402 m42a[59B7]	R7629 RES_402 m42a[59C7]	R7630 RES_402 m42a[59C5]	R7661 RES_402 m42a[59C2]	R7664 RES_402 m42a[59C3]	R7665 RES_402 m42a[59B4]	R7666 RES_402 m42a[59C2]	R7667 RES_402 m42a[59B2]	R7668 RES_402 m42a[59B2]	R7669 RES_402 m42a[59C2]	R7670 RES_402 m42a[59C4]	R7720 RES_402 m42a[60B3]	R7721 RES_402 m42a[60A3]	R7750 RES_402 m42a[60C6]	R7751 RES_402 m42a[60C7]	R7752 RES_402 m42a[60C7]	R7753 RES_402 m42a[60B7]	R7800 RES_402 m42a[61C4]	R7801 RES_402 m42a[61B2]	R7802 RES_1206 m42a[61C3]	R7803 RES_402 m42a[61C2]	R7804 RES_402 m42a[61C7]	R7805 RES_402 m42a[61B7]	R7806 RES_402 m42a[61B7]	R7807 RES_402 m42a[61C5]	R7808 RES_402 m42a[61B6]	R7810 RES_402 m42a[61B4]	R7821 RES_402 m42a[61B2]	R7822 RES_402 m42a[61B2]	R7860 RES_603 m42a[61C3]	R7861 RES_402 m42a[61C2]	R7863 RES_402 m42a[61C2]	R7900 RES_402 m42a[62C5]	R7901 RES_402 m42a[62B1]	R7902 RES_1206 m42a[62A7]	R7903 RES_402 m42a[62A3]	R7904 RES_402 m42a[62A3]	R7905 RES_402 m42a[62A6]	R7906 RES_402 m42a[62A3]	R7907 RES_402 m42a[62A3]	R7921 RES_402 m42a[62C7]	R7924 RES_402 m42a[62C6]	R7925 RES_402 m42a[62B6]	R7926 RES_402 m42a[62C7]	R7927 RES_402 m42a[62B8]	R7928 RES_402 m42a[62B8]	R7929 RES_402 m42a[62C7]	R7930 RES_402 m42a[62C5]	R7961 RES_402 m42a[62C2]	R7964 RES_402 m42a[62C3]	R7965 RES_402 m42a[62B3]	R7966 RES_402 m42a[62C2]	R7967 RES_402 m42a[62B2]	R7968 RES_402 m42a[62C7]	R7969 RES_402 m42a[62C2]	R7970 RES_402 m42a[62C4]	R7990 RES_402 m42a[62A6]	R7991 RES_402 m42a[62A6]	R7992 RES_603 m42a[62A7]	R8000 RES_402 m42a[63D5]	R8005 RES_402 m42a[63C5]	R8010 RES_402 m42a[63C5]	R8015 RES_402 m42a[63B5]	R8025 RES_402 m42a[63A5]	R8030 RES_402 m42a[63B6]	R8031 RES_402 m42a[63B6]	R8032 RES_402 m42a[63D6]	R8033 RES_402 m42a[63D6]	R8050 RES_402 m42a[63A6]	R8056 RES_402 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m42a[66B6]	R8310 RES_402 m42a[66C5]	R8311 RES_402 m42a[66B7]	R8312 RES_402 m42a[66C7]	R8320 RES_2525 m42a[66B3]	R8322 RES_402 m42a[66A3]	R8323 RES_402 m42a[66A3]	R8324 RES_402 m42a[66A4]	R8325 RES_402 m42a[66A5]	R8330 RES_402 m42a[66B4]	R8331 RES_402 m42a[66A4]	R8332 RES_402 m42a[66C4]	R8341 RES_402 m42a[66B8]	R8342 RES_402 m42a[66C8]	R8343 RES_402 m42a[66B8]	R8344 RES_402 m42a[66B8]	R8350 RES_402 m42a[66B5]	R8351 RES_402 m42a[66B6]	R8352 RES_402 m42a[66B5]	R8360 RES_402 m42a[66D7]	R8361 RES_402 m42a[66C7]	R8362 RES_402 m42a[66B7]	R8363 RES_402 m42a[66B6]	R8364 RES_402 m42a[66B6]	R8365 RES_402 m42a[66B6]	R8367 RES_402 m42a[66C6]	R8370 RES_402 m42a[66C2]	R8371 RES_402 m42a[66B2]	R8381 RES_603 m42a[66B4]	R8397 RES_0612 m42a[66C4]	R8400 RES_402 m42a[67D6]	R9401 RES_402 m42a[67D6]	R9402 RES_402 m42a[67C7]	R9408 RES_402 m42a[67B5]	R9409 RES_402 m42a[67B5]	R9413 RES_402 m42a[67A6]	R9414 RES_402 m42a[67B7]	R9415 RES_402 m42a[67B7]	R9416 RES_402 m42a[67B7]	R9423 RES_402 m42a[67B6]	R9428 RES_402 m42a[67C5]	R9500 RES_402 m42a[68A7]	R9501 RES_402 m42a[68B6]	R9502 RES_402 m42a[68B6]	R9503 RES_402 m42a[68A4]	R9504 RES_402 m42a[68B2]	R9505 RES_402 m42a[68B2]	R9506 RES_402 m42a[68B1]	R9507 RES_402 m42a[68D2]	R9508 RES_402 m42a[68D2]	R9509 RES_402 m42a[68C2]	R9510 RES_402 m42a[68C2]	R9537 RES_402 m42a[68D1]	R9538 RES_402 m42a[68D1]	R9539 RES_402 m42a[68C1]	R9540 RES_402 m42a[68C1]	R9821 RES_402 m42a[69D7]	R9822 RES_402 m42a[69D6]	R9850 RES_402 m42a[69B8]	R9851 RES_402 m42a[69B8]	R9852 RES_402 m42a[69A8]	R9853 RES_402 m42a[69A8]	R9854 RES_402 m42a[69A8]	R9855 RES_402 m42a[69A8]	R9856 RES_402 m42a[69B6]	R9859 RES_402 m42a[69A6]	R9860 RES_402 m42a[69C3]	R9861 RES_402 m42a[69C3]	R9862 RES_402 m42a[69C5]	R9863 RES_402 m42a[69C5]	R9864 RES_402 m42a[69A6]	R9868 RES_402 m42a[69C8]	R9869 RES_402 m42a[69C8]	R9870 RES_402 m42a[69C1]	R9871 RES_402 m42a[69C1]	RP2300 RPAK4F_SM-LF m42a[23D5]	RP2600 RPAK4F_SM-LF m42a[26D2]	RP2601 RPAK4F_SM-LF m42a[26C2]	RP2602 RPAK4F_SM-LF m42a[26C2]	RP3000 RPAK4F_SM-LF m42a[30B4 30C4 30D4 30D4]	RP3001 RPAK4F_SM-LF m42a[30C4 30A4 30A4 30D4]	RP3002 RPAK4F_SM-LF m42a[30A4 30A4 30A4 30D4]	RP3003 RPAK4F_SM-LF m42a[30C4 30C4 30C4 30D4]	RP3004 RPAK4F_SM-LF m42a[30C4 30C4 30D4]	RP3005 RPAK4F_SM-LF m42a[30B4 30A4 30A4 30D4]	RP3006 RPAK4F_SM-LF m42a[30B4 30B4 30A4 30D4]	RP3007 RPAK4F_SM-LF m42a[30C4 30C4 30C4 30C4]	RP3008 RPAK4F_SM-LF m42a[30C4 30C4 30C4 30C4]	RP3009 RPAK4F_SM-LF m42a[30B4 30B4 30C4 30C4]	RP3010 RPAK4F_SM-LF m42a[30B4 30B4 30B4 30B4]	RP3011 RPAK4F_SM-LF m42a[30B4 30A4 30B4 30B4]	T4201 XFR_1000BT_82400275_ m42a[37C6]	XFR-SM	T4202 XFR_1000BT_82400275_ m42a[37B6]	XFR-SM	U0700 CPU_YONAH_BGA m42a[7C3 7D7]	U0700 CPU_YONAH_BGA m42a[8D8 8D4]	U1001 APT7461_MSOP m42a[10C5]	U1200 NB_945GM_BGA m42a[12D5]	U1200 NB_945GM_BGA m42a[13D4]	U1200 NB_945GM_BGA m42a[14D5]	U1200 NB_945GM_BGA m42a[15D3 15D7]	U1200 NB_945GM_BGA m42a[16D2 16C8]	U1200 NB_945GM_BGA m42a[17D5]	U1200 NB_945GM_BGA m42a[18D4 18D7]	U1900 LREG_TPS73115_SOT23-5 m42a[19D6]	U1901 M157_SOT23-5-LF m42a[19C4]	U2100 SB_1CH7M_BGA m42a[21D6]	U2100 SB_1CH7M_BGA m42a[22B7 22D3]	U2100 SB_1CH7M_BGA m42a[23D4]	U2100 SB_1CH7M_BGA m42a[24D4 24D7]	U2601 MC74VHC1G08_SCT0 m42a[26A5]	U2603 MC74VHC1G08_SCT0-5 m42a[26A7]	U2680 MC74VHC1G08_SCT0 m42a[26B3]	U3100 LREG_BD3533FVM_MSOP m42a[31C4]	U3301 CLK_SVN_SLG81P436_QF m42a[32C5]	N	U4101 88E8053_QFN m42a[36D6]	U4102 EEPROM_M24C08_S08 m42a[36A3]	U4400 FW32306_BGA_BGA m42a[38C5]	U5100 CY8C24794_MLF m42a[41C5]	U5200 SWI_TPS2042B_MSOP m42a[42C7]	U5800 SMC_H8S2116_BGA m42a[45A8 45C3 45C7 45D7]	U5900 VDET_RSG_VD_SOT23-5 m42a[46D7]	U5910 OBC_12P_SM-3040LC-SM m42a[46A7]	U5977 COMPARATOR_LMC7211_S m42a[46C2]	M-LF	U6100 OPAMP_LMV2011_SOT23-5 m42a[48C3]	U6200 MAX6695_UMAX m42a[49D4]	U6250 MAX6695_UMAX m42a[49B4]	U6301 FLASH_SST25VF016B_SO m42a[50D3]	I_S01	U6620 K3MS2_QFN m42a[52C5]	U6650 L193L02AL_LGA m42a[52B5]	U6700 TPM_TSSOP m42a[53C5]	U6800 AUDIO_STAC92204XR_LQ m42a[54D5]	FP	U7210 MAX9705_TDFN1 m42a[55C5]	U7220 MAX9705_TDFN1 m42a[55B5]	U7230 MAX9705_TDFN1 m42a[55A5]	U7400 MAX9890_UCSP1 m42a[57C2]	U7500 ISL6262_QFN m42a[58C6]	U7600 LTC3728L_QFN m42a[59C5]	U7700 MAX8887_SOT23-5 m42a[60D4]	U7701 MAX8887_SOT23-5 m42a[60C4]	U7720 LREG_MAX8516_SOP m42a[60B3]	U7800 ISL6269_QFN m42a[61C5]	U7801 AMP_INA326_MSOP m42a[61C2]	U7900 LTC3728L_QFN m42a[62C5]	U7901 AMP_INA326_MSOP m42a[62A6]	U8070 LTC2908_LLP m42a[63B2]	U8080 MC74VHC1G08_SCT0 m42a[63B1]	U8090 LT3470_TSOT23-8 m42a[63D3]	U8200 COMPARATOR_LMC7211_S m42a[65C4]	M-LF	U8250 MC74VHC1G08_SCT0 m42a[65C3]	U8290 COMPARATOR_LM397_SOT m42a[65C5]	23-5	U8300 ISL6255_QFN m42a[66C6]	U8370 INA193_SOT23-5 m42a[66C3]	U8375 INA193_SOT23-5 m42a[66B2]	U9453 MC74VHC1G08_SCT0 m42a[67C5]	U9500 ST11362_LQFP m42a[68B4]	U9801 VIDEO_TS3V330_SOP m42a[69B7]	U9804 SN74LVC2G125_US m42a[69C2 69C2]	VR5965 VREF_ISL6000233_SOT2 m42a[46C7]	3-3	VR6800 LREG_TPS79501_SOT223 m42a[54A5]	-6	XW5800 SHORT_SM m42a[45C3]	XW7200 SHORT_SM m42a[55A5]	XW7300 SHORT_SM m42a[56C4]	XW7301 SHORT_SM m42a[56B4]	XW7302 SHORT_SM m42a[56C2]	XW7303 SHORT_SM m42a[56C2]	XW7304 SHORT_SM m42a[56B2]	XW7305 SHORT_SM m42a[56B7]	XW7400 SHORT_SM m42a[57A7]	XW7500 SHORT_SM m42a[58A6]	XW7600 SHORT_SM m42a[59A5]	XW7620 JUMPER_OPEN-SAWTOOTH m42a[59B8]	XW7660 JUMPER_OPEN-SAWTOOTH m42a[59B1]	XW7800 SHORT_SM m42a[61B5]	XW7900 SHORT_SM m42a[62A5]	XW7920 JUMPER_OPEN-SAWTOOTH m42a[62B8]	XW8101 SHORT_SM m42a[64B2]	XW8102 SHORT_SM m42a[64B2]	XW8300 SHORT_SM m42a[66B4]	Y2600 CRYSTAL_4PIN_SM-LF m42a[26C7]	Y3301 CRYSTAL_5X3.2-SM m42a[32C7]	Y4101 CRYSTAL_4PIN_SM-3.2X 2.5MM m42a[36B6]	Y4403 CRYSTAL_4PIN_SM-3.2X 2.5MM m42a[38C2]	Y5920 CRYSTAL_5X3.2-SM m42a[46C7]	Y6795 CRYSTAL_4PIN_SM-LF m42a[53B6]	Z0601 MTHOLE m42a[68B]	Z0602 MTHOLE m42a[68B]	Z0603 PCB_STANDOFF m42a[68B]	Z0604 PCB_STANDOFF m42a[68A]	Z0605 PCB_STANDOFF m42a[68A]	Z0606 MTHOLE m42a[68D]	Z0607 MTHOLE m42a[68C]	Z0608 MTHOLE m42a[68C]	Z0609 MTHOLE m42a[68B]	Z0610 MTHOLE m42a[68B]	Z0611 MTHOLE m42a[68B]	Z0612 PCB_STANDOFF m42a[68A]	Z0613 PCB_STANDOFF m42a[68A]	Z0621 PCB_STANDOFF m42a[68A]	ZS0620 SPRING_CLIP_LP_RMI_C m42a[60D7]	LIP-SM-M42	ZS0621 CLIP_SM m42a[68D]
A	8	7	6	5	4	3	2	1																																																																																																																																																																																																																																																																																																																																																																																																																	