051-7173 MLB , M42C

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EE DRIS:
RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINKELHOFFER
LT-LAWRENCE TAN
ES-ERIC SMITH
LD-LINDA DUNN

Schematic / PCB #’s

Apple Computer Inc.
### Power Supply NO_TESTS

<table>
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<tr>
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### CLOCK NO_TESTS

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### FIREWARE NO_TESTS

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### ETHERNET NO_TESTS

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### Fan Connectors

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### LPC+ Debug Connector

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<tbody>
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<td>NO_TEST</td>
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### Other Func Test Points

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</thead>
<tbody>
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<td>NO_TEST</td>
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</tbody>
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**battery Legacy**

---

**Enthusiastic Battery**

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**www.laptop-schematics.com**
CPU ITP700FLEX DEBUG SUPPORT

XDP_DBRESET_L
XDP_TDI
XDP_TDO
XDP_TRST_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TMS
CPU_XDP_CLK_P
CPU_XDP_CLK_N
XDP_BPM_L<7>
FSB_CPURST_L
XDP_BPM_L<10>
XDP_BPM_L<11>
XDP_BPM_L<12>
XDP_BPM_L<13>
XDP_BPM_L<14>
XDP_BPM_L<15>
XDP_BPM_L<16>
XDP_BPM_L<17>
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XDP_BPM_L<22>
XDP_BPM_L<23>
XDP_BPM_L<24>
XDP_BPM_L<25>
XDP_BPM_L<26>
XDP_BPM_L<27>
XDP_BPM_L<28>
XDP_BPM_L<29>
XDP_BPM_L<30>
XDP_BPM_L<31>
CPU ITP700FLEX DEBUG SUPPORT

NOTE ON TCK SIGNAL LAYOUT:
- ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU's TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PRO PIN.
- CONNECTOR'S FBO PIN.
- (AND WITH RESET BUTTON)

SCH Expr. No.
- XDP_TDI
- XDP_TDO
- XDP_TRST_L
- XDP_BPM_L<0>
- XDP_BPM_L<1>
- XDP_BPM_L<2>
- XDP_BPM_L<3>
- XDP_BPM_L<4>
- XDP_BPM_L<5>
- XDP_BPM_L<6>
- XDP_BPM_L<7>
- XDP_BPM_L<8>
- XDP_BPM_L<9>
- XDP_BPM_L<10>
- XDP_BPM_L<11>
- XDP_BPM_L<12>
- XDP_BPM_L<13>
- XDP_BPM_L<14>
- XDP_BPM_L<15>
- XDP_BPM_L<16>
- XDP_BPM_L<17>
- XDP_BPM_L<18>
- XDP_BPM_L<19>
- XDP_BPM_L<20>
- XDP_BPM_L<21>
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- XDP_BPM_L<23>
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- XDP_BPM_L<25>
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- XDP_BPM_L<27>
- XDP_BPM_L<28>
- XDP_BPM_L<29>
- XDP_BPM_L<30>
- XDP_BPM_L<31>

- CPU ITP700FLEX DEBUG SUPPORT

NOTE ON TCK SIGNAL LAYOUT:
- ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU's TCK PIN AND THEN FUSE BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PRO PIN.
- CONNECTOR'S FBO PIN.
- (AND WITH RESET BUTTON)
Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.

Unused DAC outputs should be disconnected.

TV-Out Disable

Component: DACA, DACB & DACC

Otherwise, tie VCCD_LVDS to GND also.

Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and associated components. Unused DAC outputs should be disconnected.

TVSYNC:   DACB & DACC only

HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core

VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.
Platform Reset Connections

Unbuffered

Buffered

Gated

Initial resistor values are based on CRB, but may change after characterization.

SB Misc
The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, (See Capell Valley pg 47) Yellow uses 10K divider and TLV2463

Page Notes

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Page Notes

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DDR2 Bypass Caps

(For return current.)

The 4.7uF and 1.0uF caps can be changed to 2.2uF caps, when they get cheaper.

<table>
<thead>
<tr>
<th>Cap</th>
<th>Type</th>
<th>Value</th>
<th>Note</th>
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</thead>
<tbody>
<tr>
<td>C2810</td>
<td>0.1uF</td>
<td>4.7uF</td>
<td></td>
</tr>
<tr>
<td>C2811</td>
<td>0.1uF</td>
<td>1.0uF</td>
<td></td>
</tr>
<tr>
<td>C2812</td>
<td>0.1uF</td>
<td>2.2uF</td>
<td></td>
</tr>
<tr>
<td>C2813</td>
<td>0.1uF</td>
<td>2.2uF</td>
<td></td>
</tr>
<tr>
<td>C2814</td>
<td>0.1uF</td>
<td>2.2uF</td>
<td></td>
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<tr>
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<td>2.2uF</td>
<td></td>
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<tr>
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<tr>
<td>C2823</td>
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<td>2.2uF</td>
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<td>C2824</td>
<td>0.1uF</td>
<td>2.2uF</td>
<td></td>
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<tr>
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<tr>
<td>C2826</td>
<td>0.1uF</td>
<td>2.2uF</td>
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<tr>
<td>C2827</td>
<td>0.1uF</td>
<td>2.2uF</td>
<td></td>
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<tr>
<td>C2828</td>
<td>0.1uF</td>
<td>2.2uF</td>
<td></td>
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</tbody>
</table>

---

DDR2 SO-DIMM Connector A

---

The diagram shows the connection points for the DDR2 SO-DIMM connector. The key points include:

- **Pin 1** (bottom left)
- **Pin 32** (bottom right)
- **Pin 64** (upper right)
- **Pin 96** (upper left)

The BOM options are as follows:

- **PP1V8_S3_MEM**
- **PP1V8_S3_MEM_NB**

For more details, please refer to the Capell Valley page 47.
If power inputs are not S0, MEMVTT_EN must be used to disable MEMVTT in S0 mode.
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SATA CONNECTOR

PLACE NEAR ICH7 PIN

PLACE NEAR ICH7 PIN
C5102 close to U5100 PIN 2

PLACE C5100 AND C5101 NEAR U5100 PIN 22 AND 49

C5100

0.1 UF

10V

CERM 20%

C5101

0.1 UF

10V

CERM 20%

C5102

0.01 UF

CERM 20%

U5100 CY8C274744

OMIT 22 49

REV. A

APPLE COMPUTER INC.

SYNC_MASTER=ENET

SYNC_DATE=11/09/2005

IR CONTROLLER

IR CONTROLLER = USB2_IR_N

IR_RX_OUT = PP5V_S3_IR

IR_RX_OUT_F = USB2_IR_P
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REV.
APPLE COMPUTER INC.
SCALE
SYNC_DATE=06/30/2005
SYNC_MASTER=NB
LPC+ Debug Connector

GPIO15
51000002

INT_SERIRQ
PM_CLKRUN_L
PM_SUS_STAT_L
LPC_FRAME_L
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_TDO
LPC_TMS
LPC_TCK
SMC_MD1
SMC_TX_L
SMC_TRST_L
SMC_RST_L
SMC_RX_L
SMC_NMI
SMC_TDI
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
F-WH_INIT_L
PCI_CLK_PORT80_L
SV_SET_UP
PCI_CLK_PORT80_L
F-WH_INIT_L
LPC_FRAME_L
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
LPC_TDO
LPC_TMS
LPC_TCK
SMC_MD1
SMC_TX_L
SMC_TRST_L
SMC_RST_L
SMC_RX_L
SMC_NMI
SMC_TDI
LPC_AD<0>
LPC_AD<1>
LPC_AD<2>
LPC_AD<3>
F-WH_INIT_L
PCI_CLK_PORT80_L
SV_SET_UP
PCI_CLK_PORT80_L
F-WH_INIT_L
Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits.
**DIMM0 TEMPERATURE ZONE**

**DIMM1 TEMPERATURE ZONE**

**NOTE:** REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452 AND THEN 518S0487.
AFTER THIS CHANGE, THE SCHEMATIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.

**TEMPERATURE SENSE**

**NOTE:** REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0452 AND 518S0487.
AFTER THIS CHANGE, THE SCHEMATIC DOES NOT MATCH THE PCB ON THESE TWO LOCATIONS.
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA (LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM
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REV.

SCALE

NONE

NC

TACH

5V DC

MOTOR CONTROL

GND

SOT23-LF

FAN_RT

SMC_FAN_1_CTL

SMC_FAN_1_TACH

FAN_RT_PWM

FAN_RT_TACH

PP3V3_S0_FAN_RT

PP5V_S0_FAN_RT

J6501

CRITICAL

F-ST-SM

100K

5%

MF-LF 402

1/16W

R6560

1 2

88609-04001

4 3 2 1

6 5

865S

1 2

R6561

1 2

821 MF-LF 402

47K

1/16W

R6565

2

518S0486

47K

1/16W5%

402MF-LF1/16W5%

821

SMC_FAN_1_CTL FAN_RT_PWM

SMC_FAN_1_TACH FAN_RT_TACH

PP3V3_S0_FAN_RT

PP5V_S0_FAN_RT

Fan

SYNC_MASTER=ENET

SYNC_DATE=11/10/2005
POWER CONTROL SIGNALS

These rails are monitored by LTC2308

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<tr>
<th>Mode</th>
<th>1V2</th>
<th>1V0</th>
<th>1V5</th>
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<tbody>
<tr>
<td>Battery Off</td>
<td>0</td>
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<td>0</td>
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5V/3.3V S5 RUN/SS CONTROL

1.5V/1.05V S0 RUN/SS CONTROL

3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.425V delivered to SMU PWM generator

5V S3 FET

5V S0 FET

3.3V S3 FET

3.3V S0 FET

1.2V S0 FET

1.8V S0 FET

ALL SYSTEM PWRGD CIRCUIT

S3/S0 FETS, G3H SUPPLY

APPLE COMPUTER INC.
CHLIM circuit (R8362, R8363, C8328) subject to change pending M1 resolution (100mW offset, radar 4221420)
INVERTER CONNECTOR

LCD + CAMERA CONNECTOR

INVERTER, LVDS, TMDS

APPLE COMPUTER INC.

*Enclosure: 518S0364
Plexi: 516S0212

REV.

SYNC_DATE=06/06/2005

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MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 MM

BRITISH-120-OHM-1.5A