1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

M42B MLB SCHEMATIC

10/2/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		536501	PRODUCTION RELEASED	10/02/07	?

Schematic / PCB #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-7370	1	SCHEM,M42B,MLB	SCH	
820-2213	1	PCBF,M42B,MLB	PCB	

EE DRIS:

RX-RAYMOND XU
DK-DINESH KUMAR
RC-RAY CHANG
MK-MARC KLINGELHOFER
LT-LAWRENCE TAN
LD-LINDA DUNN

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK | ENG APPD | MFG APPD | QA APPD | DESIGNER | RELEASE | SCALE: NONE

MATERIAL/FINISH NOTED AS APPLICABLE

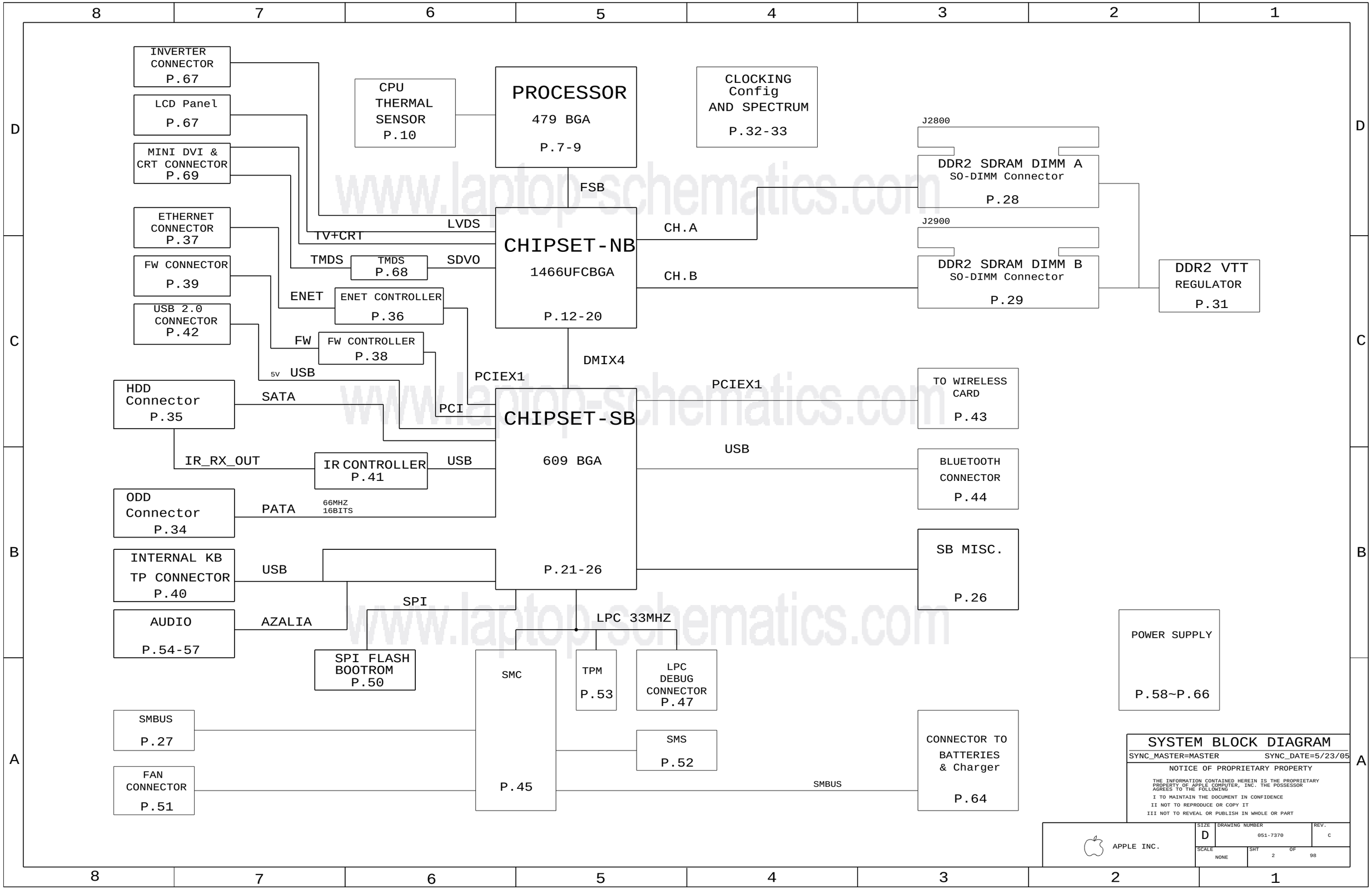
SIZE: D

APPLE INC.

TITLE: SCHEM,MLB,M42B

DRAWING NUMBER: 051-7370 REV. C

SHT 1 OF 98



SYSTEM BLOCK DIAGRAM

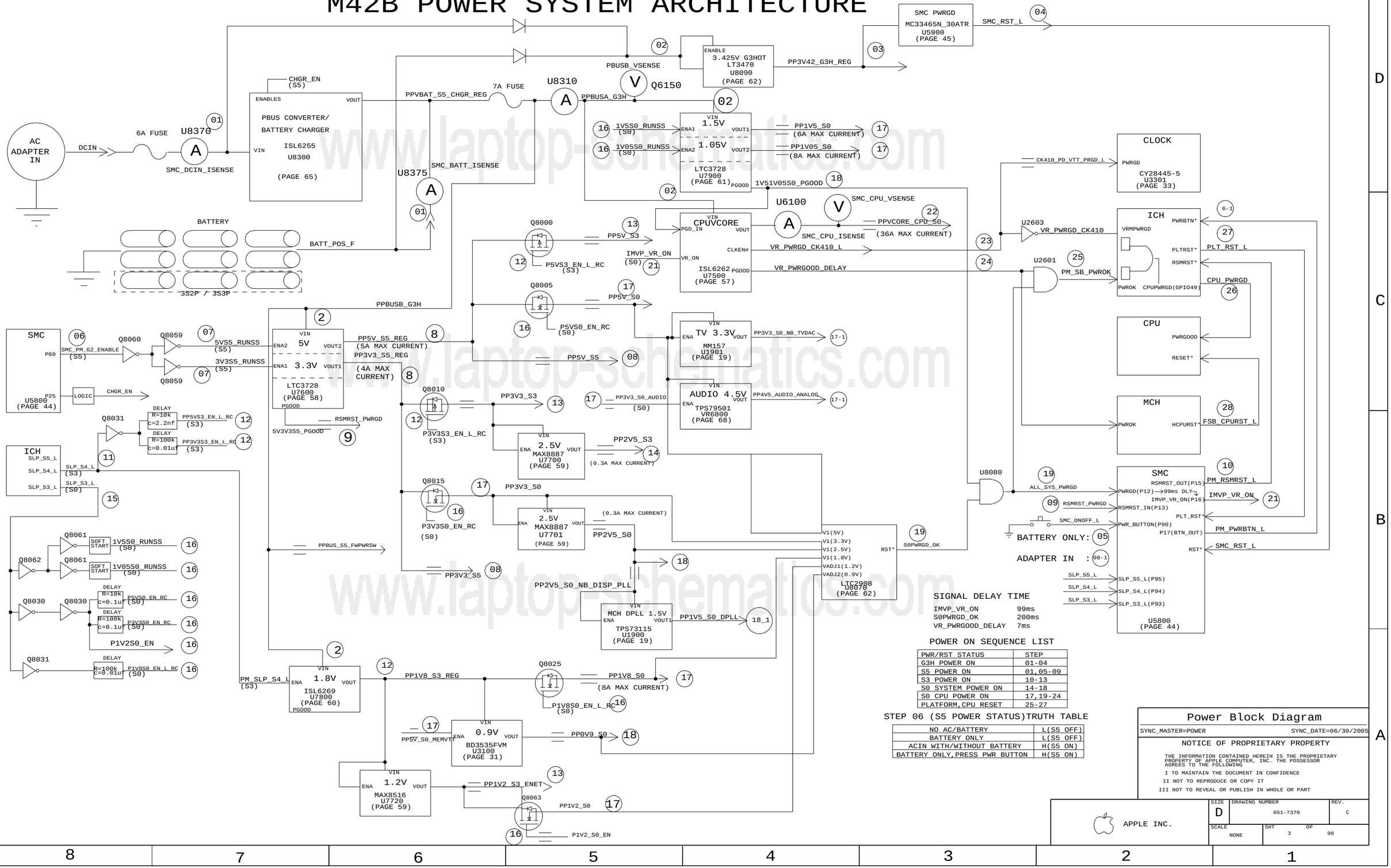
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	2	98

M42B POWER SYSTEM ARCHITECTURE



BOARD STACK-UP AND CONSTRUCTION

Top		SIGNAL
2		GROUND
3		SIGNAL(High Speed)
4		SIGNAL(High Speed)
5		GROUND
6		POWER
7		POWER
8		GROUND
9		SIGNAL(High Speed)
10		SIGNAL(High Speed)
11		GROUND
BOTTOM		SIGNAL

MLB STACKUP

LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S3389	1	IC,MEROM,CPU 2.0GHZ,479 PGA	U0700	GOOD
337S3391	1	IC,MEROM,CPU 2.16GHZ,479 PGA	U0700	BETTER
337S3391	1	IC,MEROM,CPU 2.16GHZ,479 PGA	U0700	BEST

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	LEMENU
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	LEMENU
359S0109	1	IC,SLG8LP436,CLOCK GEN,68PIN QFN	U3301	LEMENU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S2132	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6301	M42A_PGM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	M42A_PGM
341S2133	1	IC,SMC,176P BGA,HSB/2116	U5800	M42A_PGM
341S1890	1	IC,PSOC+W/USB,56P,MLF,CY8C24794	U5100	M42A_PGM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCN	CRITICAL	BEST-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCM	CRITICAL	BETTER-KIONIX
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:YCL	CRITICAL	GOOD-KIONIX

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 4 OF 98	

Functional Test Points

Power Supply NO_TESTs

NO_TEST

I93		IMVP6_RBIAS	58A4 58B7
I94		IMVP6_COMP	58A4 58B7
I95		5VS5_RUNSS	59B4 63C7
I96		1V5S0_RUNSS	62B5 63B7
I101		1V8S3_COMP	61B6
I102		1V8S3_FSET	61C6
I103	TRUE	3V3S5_COMP	
I104	TRUE	3V3S5_FSET	
I106	TRUE	1V05S0_COMP	
I105	TRUE	1V05S0_FSET	
I107	TRUE	P3V42G3H_FB	63D2

CLOCK NO_TESTS

NO_TEST

I111	TRUE	CK410_CPU0_N	32C4 33D5
I112	TRUE	CK410_CPU0_P	32C4 33D5
I113	TRUE	CK410_CPU1_N	32C4 33D5
I114	TRUE	CK410_CPU1_P	32C4 33D5
I115	TRUE	CK410_CPU2_ITP_SRC10_N	32C4 33D5
I116	TRUE	CK410_CPU2_ITP_SRC10_P	32C4 33D5
I117	TRUE	CK410_DOT96_27M_N	32A4 33B5
I118	TRUE	CK410_DOT96_27M_P	32A4 33B5
I119	TRUE	CK410_LVDS_N	32B4 33A5
I120	TRUE	CK410_LVDS_P	32B4 33A5
I122	TRUE	CK410_PCI4_CLK_SPN	
I122	TRUE	CK410_PCIF1_CLK	32B6 33D8
I123	TRUE	CK410_SRC1_N_SPN	6B3
I122	TRUE	CK410_SRC1_P_SPN	6B3
I123	TRUE	CK410_SRC2_N	32B4 33C5
I183	TRUE	CK410_SRC2_P	32B4 33C5
I184	TRUE	CK410_SRC3_N_SPN	6B3
I185	TRUE	CK410_SRC3_P_SPN	6B3
I186	TRUE	CK410_SRC4_N	32B4 33B5
I187	TRUE	CK410_SRC4_P	32B4 33B5
I188	TRUE	CK410_SRC5_N	32B4 33C5
I189	TRUE	CK410_SRC5_P	32B4 33C5
I190	TRUE	CK410_SRC6_N	32B4 33C5
I191	TRUE	CK410_SRC6_P	32B4 33D5
I192	TRUE	CK410_SRC7_N_SPN	6B3
I193	TRUE	CK410_SRC7_P_SPN	6B3
I194	TRUE	CK410_SRC8_N	32A4 33C5
I195	TRUE	CK410_SRC8_P	32A4 33C5
I196	TRUE	CK410_SRC_CLKREQ1_L_SPN	6B3
I197	TRUE	CK410_SRC_CLKREQ3_L_SPN	6B3
I198	TRUE	CK410_SRC_CLKREQ8_L	32A4 33A5

FIREWARE NO_TESTS

NO_TEST

I199	TRUE	FW_B_TPA_N_SPN	6D1
I200	TRUE	FW_B_TPA_P_SPN	6D1
I201	TRUE	FW_B_TPBIAS_SPN	6D1
I202	TRUE	FW_B_TPB_N_SPN	6D1
I203	TRUE	FW_B_TPB_P_SPN	6D1
I204	TRUE	FW_C_TPA_N_SPN	6D1
I205	TRUE	FW_C_TPA_P_SPN	6D1
I206	TRUE	FW_C_TPBIAS_SPN	6D1
I207	TRUE	FW_C_TPB_N_SPN	6D1
I208	TRUE	FW_C_TPB_P_SPN	6D1

LVDS NO_TESTS

NO_TEST

I209	TRUE	LVDS_B_CLK_N_SPN	6D5
I210	TRUE	LVDS_B_CLK_P_SPN	6D5
I211	TRUE	LVDS_B_DATA_N0_SPN	6D5
I212	TRUE	LVDS_B_DATA_N1_SPN	6D5
I213	TRUE	LVDS_B_DATA_N2_SPN	6D5
I214	TRUE	LVDS_B_DATA_P1_SPN	6D5
I215	TRUE	LVDS_B_DATA_P2_SPN	6D5

ETHERNET NO_TESTS

NO_TEST

I216	TRUE	ENET_MDI_TRAN_P<2>	37B5
I217	TRUE	ENET_MDI_TRAN_N<2>	37B5
I218	TRUE	ENET_MDI_TRAN_P<3>	37B5

NO_TEST

I219	TRUE	SMC_FAN_3_TACH	45B8 46C3
I220	TRUE	ALS_LEFT	45A8 46C3

Fan Connectors

FUNC_TEST

I12	TRUE	=PP5V_S0_FAN_RT	51C4 64D3
I15	TRUE	FAN_RT_PWM	51B3
I16	TRUE	FAN_RT_TACH	51C3
I157	TRUE	=PP3V3_S0_FAN_RT	51C4 64A6
I158	TRUE	SMC_FAN_1_CTL	45B8 51B4
I159	TRUE	SMC_FAN_1_TACH	45B8 51C4

LPC+ Debug Connector

FUNC_TEST

I20	TRUE	=PP3V42_G3H_LPCPLUS	47C6 64D1
I19	TRUE	=PP5V_S0_LPCPLUS	47C6 64D3
I18	TRUE	LPC_AD<0>	21D4 45D8 47C6 53C6
I17	TRUE	LPC_AD<1>	21D4 45D8 47C6 53C6
I71	TRUE	LPC_FRAME_L	21C5 45C8 47C6 53C6
I72	TRUE	PM_CLKRUN_L	23C8 38A5 45D5 47C6 53C6
I73	TRUE	BOOT_LPC_SPI_L	22B3 45C8 47C6
I74	TRUE	SMC_TMS	45B5 46C6 47C6
I75	TRUE	DEBUG_RST_L	26B1 47C6
I76	TRUE	SMC_TRST_L	45C1 47C6
I77	TRUE	SMC_TDO	45C5 46C6 47B6
I78	TRUE	SMC_MD1	45C2 47B6
I79	TRUE	SMC_TX_L	45C8 46B2 46D6 47B6
I80	TRUE	FWH_INIT_L	6B2 21C4 47C5
I81	TRUE	PCI_CLK_PORT80_LPC	33D6 47C5
I82	TRUE	LPC_AD<2>	21D4 45D8 47C5 53C6
I83	TRUE	LPC_AD<3>	21D4 45D8 47C5 53C6
I84	TRUE	INT_SERIRQ	23C8 45C8 47C5 53C6
I85	TRUE	PM_SUS_STAT_L	23C5 45D5 46D3 47C5 53C6
I86	TRUE	SMC_TDI	45C5 46C6 47C5
I87	TRUE	SMC_TCK	45C5 46C6 47C5
I88	TRUE	SMC_RST_L	45C3 46D7 47C5
I89	TRUE	SMC_NMI	45C1 47B5
I91	TRUE	SMC_RX_L	45C8 46B2 46D6 47B5
I90	TRUE	SV_SET_UP	23B6 23C3 47B5

Other Func Test Points

FUNC_TEST

I62	TRUE	=PP1V05_S0_REG	62B1 64D8

SMBus FUNC_TEST

I182

	TRUE	SMBUS_SMC_MLB_SCL	27C5
I183	TRUE	SMBUS_SMC_MLB_SDA	27B5

FIREWIRE FUNC_TEST

I152	TRUE	PPFW_SWITCH	39D4

SLEEP LED FUNC_TEST

I155	TRUE	SYS_LED_ANODE	35C5 46A3

SMC FUNC_TEST

I145	TRUE	SMC_LID	40C4 45B5 46C6 65A8
I146	TRUE	SMC_MANUAL_RST_L	46D8
I156	TRUE	SMC_CPU_VSENSE	45D5 48B1

Power Supply FUNC_TEST

I160	TRUE	ALL_SYS_PWRGD	26A5 45D8 63B1
I161	TRUE	PPVCORE_CPU_S0	64D7
I162	TRUE	PP1V05_S0	64D7
I140	TRUE	PP1V5_S0	64C7
I142	TRUE	PP1V8_S0	64C7
I163	TRUE	PP2V5_S0	64B7
I165	TRUE	PP3V3_S0	64B7
I166	TRUE	PP5V_S0	64D4
I167	TRUE	PP1V2_S3	64C4
I168	TRUE	PP1V8_S3	64C4
I170	TRUE	PP2V5_S3	64C4
I172	TRUE	PP3V3_S3	64B4
I171	TRUE	PP5V_S3	64B4
I177	TRUE	PP3V3_S5	64A4
I178	TRUE	PP5V_S5	64A4
I176	TRUE	PP3V42_G3H	64D1
I174	TRUE	PPBUSA_G3H	
I175	TRUE	PPBUSB_G3H	64C1
I179	TRUE	PP18V5_G3H	64C1
I181	TRUE	PP0V9_S0	64D7

Battery Digital Connector

FUNC_TEST

I1	TRUE	SMC_BS_ALRT_L	45C5 46C6 65A2
I3	TRUE	SMBUS_BATT_SCL_F	65B6
I4	TRUE	SMBUS_BATT_SDA_F	65A6
I2	TRUE	BATT_IN	
I177	TRUE	BATT_POS	65A6
I160	TRUE	BATT_NEG	65A6

Audio FUNC_TEST

I9	TRUE	PP5V_S0_AUDIO_PWR	
I11	TRUE	PP5V_S0_AUDIO	
I10	TRUE	GND_AUDIO_PWR	64B2
I21	TRUE	GND_AUDIO_CODEC	64B2
I22	TRUE	ACZ_SDATAIN<0>	21C7 54D7
I24	TRUE	ACZ_SDATAOUT	21C7 54D7
I23	TRUE	ACZ_BITCLK	21C7 54D7
I25	TRUE	ACZ_RST_L	21C7 54C7 57C3
I45	TRUE	ACZ_SYNC	21C7 54D7

Battery FUNC_TEST

I29	TRUE	SMC_BATT_ISET	45B5 66B7
I32	TRUE	SMC_BATT_CHG_EN	45D8 46B6 66A4
I31	TRUE	SMC_BC_ACOK	45C5 46B6 65C3 65C7 66A5
I33	TRUE	SMC_PS_ON	39C6 45D5 46B3 65C3
I36	TRUE	SMC_BATT_TRICKLE_EN_L	45D8 46B6 66A3
I38	TRUE	SYS_ONEWIRE	45B8 46D6 65C8

USB FUNC_TEST

I44	TRUE	TP_USBP_E	6C2
I47	TRUE	TP_USBN_E	6C2
I46	TRUE	TP_USBP_F	
I48	TRUE	TP_USBN_F	

DC-JACK FUNC_TEST

I57	TRUE	ACIN_ENABLE_GATE	65C3

Battery charger FUNC_TEST

I58	TRUE	PPVBAT_G3H_CHGR_OUT	66B5 66C2

INVERTER CONNECTOR FUNC_TEST

I60	TRUE	PPBUS_ALL_INV_CONN	67D3
I59	TRUE	INV_GND	67D2
I61	TRUE	PP5V_INV_F	67D3
I63	TRUE	INV_BKLIGHT_PWM_L	67D2

FUNC TEST 1 OF 2

APPLE INC.	SIZE D	DRAWING NUMBER 051-7370	REV. C
	SCALE NONE	SHT 5 OF 98	

(EMI PAD FOR INVERTER GONNECTOR)

67C2 INVT_CHGND — 1 — ZS0620 EMI-SPRING CLIP-SM-M42

SPKR-MIC-CLIP-M42

NC — 1 — ZS0621 SM

CHASSIS GND

BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_IO 6C7 — OMIT Z0606 5R2P3-7SQB 1

65A6 =GND_BATT_CHGND
56B8 =GND_CHASSIS_AUDIO_JACK
=GND_CHASSIS_AUDIO_SPKRCONN
57A6 =GND_CHASSIS_AUDIO_MIC
=GND_CHASSIS_AUDIO_SHIELD1
=GND_CHASSIS_AUDIO_SHIELD2
=GND_CHASSIS_AUDIO_SHIELD3
28A5 =GND_CHASSIS_DIPDIMM_LEFT

SATA,LVDS CONNECTOR CHASSIS GND

GND_CHASSIS_SATA 35C8 — OMIT Z0607 6P5R2P6-5P5B 1

VOLTAGE=0V MAKE_BASE=TRUE

67B2 67A2 =GND_CHASSIS_LVDS

C0607 0.1UF 10% 16V X5R 402

C0608 0.01UF 10% 16V CERM 402

DCIN CONNECTOR CHASSIS GND

GND_CHASSIS_DCIN — OMIT Z0602 5R2P3-7SQB 1

VOLTAGE=0V MAKE_BASE=TRUE

65C8 =GND_DCIN_CHGND
37A4 =GND_CHASSIS_RJ45
69C3 69A4 =GND_CHASSIS_TMDS_UPPER

C0630 0.1UF 10% 16V X5R 402

I/O CONNECTOR CHASSIS GND

GND_CHASSIS_IO 607 — OMIT Z0608 5P0R2P3-7BLB 1

VOLTAGE=0V MAKE_BASE=TRUE

39A1 =GND_CHASSIS_FW_DOWN
42C4 42C2 42A4 42A2 =GND_CHASSIS_USB

C0610 0.1UF 10% 16V X5R 402

C0611 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_CENTER — OMIT Z0610 5R2P3-7SQB 1

VOLTAGE=0V MAKE_BASE=TRUE

29A5 28D5 =GND_CHASSIS_DIPDIMM_CENTER

C0616 0.1UF 10% 16V X5R 402

C0617 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_RIGHT — OMIT Z0609 5R2P3-7SQB 1

VOLTAGE=0V MAKE_BASE=TRUE

29D4 =GND_CHASSIS_DIPDIMM_RIGHT

C0614 0.1UF 10% 16V X5R 402

C0615 0.01UF 10% 16V CERM 402

OMIT Z0601 5R2P3-7SQB — GND_CHASSIS_CPU 1

C0612 0.1UF 10% 16V X5R 402

C0613 0.01UF 10% 16V CERM 402

OMIT Z0611 5R2P3-7B — GND_CHASSIS_FANSCREW 1

C0618 0.1UF 10% 16V X5R 402

C0619 0.01UF 10% 16V CERM 402

DIGITAL GND SCREW HOLE OMIT

OMIT Z0603 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — NB_RIGHT_DOWN_SCREW 1

R0612 0 5% 1/16W MF-LF 402

OMIT Z0604 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — CPU_THERMAL_SCREW_UP 1

R0610 0 5% 1/16W MF-LF 402

OMIT Z0605 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — CPU_THERMAL_SCREW_DOWN 1

R0611 0 5% 1/16W MF-LF 402

OMIT Z0621 STDOFF-4.5OD3.95H-1.1-3.7-TH1 — CPU_THERMAL_SCREW_RIGHT 1

R0621 0 5% 1/16W MF-LF 402

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

13C5	LVDS_B_CLK_N	LVDS_B_CLK_N_SPN	5A7
13C5	LVDS_B_CLK_P	LVDS_B_CLK_P_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<0>	LVDS_B_DATA_N0_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<1>	LVDS_B_DATA_N1_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_N<2>	LVDS_B_DATA_N2_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<0>	LVDS_B_DATA_P0_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<1>	LVDS_B_DATA_P1_SPN	MAKE_BASE=TRUE 5A7
13C5	LVDS_B_DATA_P<2>	LVDS_B_DATA_P2_SPN	MAKE_BASE=TRUE 5A7 MAKE_BASE=TRUE

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

13D3	PEG_D2R_N<0>	PEG_D2R_N0_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<2>	PEG_D2R_N2_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<3>	PEG_D2R_N3_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<4>	PEG_D2R_N4_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<5>	PEG_D2R_N5_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<6>	PEG_D2R_N6_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<7>	PEG_D2R_N7_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<8>	PEG_D2R_N8_SPN	MAKE_BASE=TRUE
13D3	PEG_D2R_N<9>	PEG_D2R_N9_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<10>	PEG_D2R_N10_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<11>	PEG_D2R_N11_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<12>	PEG_D2R_N12_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<13>	PEG_D2R_N13_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<14>	PEG_D2R_N14_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_N<15>	PEG_D2R_N15_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<0>	PEG_D2R_P0_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<2>	PEG_D2R_P2_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<3>	PEG_D2R_P3_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<4>	PEG_D2R_P4_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<5>	PEG_D2R_P5_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<6>	PEG_D2R_P6_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<7>	PEG_D2R_P7_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<8>	PEG_D2R_P8_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<9>	PEG_D2R_P9_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<10>	PEG_D2R_P10_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<11>	PEG_D2R_P11_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<12>	PEG_D2R_P12_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<13>	PEG_D2R_P13_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<14>	PEG_D2R_P14_SPN	MAKE_BASE=TRUE
13C3	PEG_D2R_P<15>	PEG_D2R_P15_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<4>	PEG_R2D_C_N4_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<5>	PEG_R2D_C_N5_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<6>	PEG_R2D_C_N6_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<7>	PEG_R2D_C_N7_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<8>	PEG_R2D_C_N8_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<9>	PEG_R2D_C_N9_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<10>	PEG_R2D_C_N10_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<11>	PEG_R2D_C_N11_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<12>	PEG_R2D_C_N12_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<13>	PEG_R2D_C_N13_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<14>	PEG_R2D_C_N14_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_N<15>	PEG_R2D_C_N15_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<4>	PEG_R2D_C_P4_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<5>	PEG_R2D_C_P5_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<6>	PEG_R2D_C_P6_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<7>	PEG_R2D_C_P7_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<8>	PEG_R2D_C_P8_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<9>	PEG_R2D_C_P9_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<10>	PEG_R2D_C_P10_SPN	MAKE_BASE=TRUE
13B3	PEG_R2D_C_P<11>	PEG_R2D_C_P11_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<12>	PEG_R2D_C_P12_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<13>	PEG_R2D_C_P13_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<14>	PEG_R2D_C_P14_SPN	MAKE_BASE=TRUE
13A3	PEG_R2D_C_P<15>	PEG_R2D_C_P15_SPN	MAKE_BASE=TRUE

69A3 =GND_CHASSIS_TMDS_DOWN
39A1 =GND_CHASSIS_FW_UPPER

GND_CHASSIS_IO1 — VOLTAGE=0V MAKE_BASE=TRUE — I393

OMIT Z0612 STDOFF-4.2OD2.15H-1.2-TH — NC 1

OMIT Z0613 STDOFF-4.2OD2.15H-1.2-TH — NC 1

NB CFG ALIASES

NO-CONNECT UNUSED CFG INTERFACE PORTS

14C6	NB_CFG<3>	TP_NB_CFG3	
14C6	NB_CFG<4>	TP_NB_CFG4	MAKE_BASE=TRUE
14C6	NB_CFG<6>	TP_NB_CFG6	MAKE_BASE=TRUE
14C6	NB_CFG<8>	TP_NB_CFG8	MAKE_BASE=TRUE
14C6	NB_CFG<10>	TP_NB_CFG10	MAKE_BASE=TRUE
14C6	NB_CFG<11>	TP_NB_CFG11	MAKE_BASE=TRUE
14C6	NB_CFG<12>	TP_NB_CFG12	MAKE_BASE=TRUE
14C6	NB_CFG<13>	TP_NB_CFG13	MAKE_BASE=TRUE
14C6	NB_CFG<14>	TP_NB_CFG14	MAKE_BASE=TRUE
14C6	NB_CFG<15>	TP_NB_CFG15	MAKE_BASE=TRUE
14C6	NB_CFG<17>	TP_NB_CFG17	MAKE_BASE=TRUE MAKE_BASE=TRUE

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

21B6	SATA_A_D2R_N	SATA_A_D2R_N_SPN	
21B6	SATA_A_D2R_P	SATA_A_D2R_P_SPN	MAKE_BASE=TRUE
21B6	SATA_A_R2D_C_N	SATA_A_R2D_C_N_SPN	MAKE_BASE=TRUE
21B6	SATA_A_R2D_C_P	SATA_A_R2D_C_P_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

PCI_EXP ALIASES

NO-CONNECT UNUSED PCI_EXP INTERFACE PORTS

22D4	PCIE_C_D2R_N	PCIE_C_D2R_N_SPN	
22D4	PCIE_C_D2R_P	PCIE_C_D2R_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_C_R2D_C_N	PCIE_C_R2D_C_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_C_R2D_C_P	PCIE_C_R2D_C_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_D2R_N	PCIE_D_D2R_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_D2R_P	PCIE_D_D2R_P_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_R2D_C_N	PCIE_D_R2D_C_N_SPN	MAKE_BASE=TRUE
22D4	PCIE_D_R2D_C_P	PCIE_D_R2D_C_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_D2R_N	PCIE_E_D2R_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_D2R_P	PCIE_E_D2R_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_R2D_C_N	PCIE_E_R2D_C_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_E_R2D_C_P	PCIE_E_R2D_C_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_D2R_N	PCIE_F_D2R_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_D2R_P	PCIE_F_D2R_P_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_R2D_C_N	PCIE_F_R2D_C_N_SPN	MAKE_BASE=TRUE
22C4	PCIE_F_R2D_C_P	PCIE_F_R2D_C_P_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

32B4	CK410_SRC1_N	CK410_SRC1_N_SPN	5C7
32B4	CK410_SRC1_P	CK410_SRC1_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC3_N	CK410_SRC3_N_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC3_P	CK410_SRC3_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC7_N	CK410_SRC7_N_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC7_P	CK410_SRC7_P_SPN	MAKE_BASE=TRUE 5C7
32B4	CK410_SRC_CLKREQ1_L	CK410_SRC_CLKREQ1_L_SPN	MAKE_BASE=TRUE 5B7
32B4	CK410_SRC_CLKREQ3_L	CK410_SRC_CLKREQ3_L_SPN	MAKE_BASE=TRUE 5B7 MAKE_BASE=TRUE

SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

23C3	SUS_CLK_SB	SUS_CLK_SB_SPN	MAKE_BASE=TRUE

SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

28C4	MEM_A_A<15>	MEM_A_A15_SPN	
28C4	MEM_A_A<14>	MEM_A_A14_SPN	MAKE_BASE=TRUE
29C4	MEM_B_A<15>	MEM_B_A15_SPN	MAKE_BASE=TRUE
29C4	MEM_B_A<14>	MEM_B_A14_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

Ethernet ALIASES

36C8	ENET_CTRL12	ENET_CTRL12_SPN	
36C8	ENET_CTRL25	ENET_CTRL25_SPN	MAKE_BASE=TRUE MAKE_BASE=TRUE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0722	4	THERMAL STANDOFF	Z0603,Z0604,Z0605,Z0621	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0612	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0613	STANDOFF

FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

38B3	FW_B_TPBIAS	FW_B_TPBIAS_SPN	5B7
38B3	FW_B_TPA_P	FW_B_TPA_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPA_N	FW_B_TPA_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPB_P	FW_B_TPB_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_B_TPB_N	FW_B_TPB_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPBIAS	FW_C_TPBIAS_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPA_P	FW_C_TPA_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPA_N	FW_C_TPA_N_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPB_P	FW_C_TPB_P_SPN	MAKE_BASE=TRUE 5B7
38B3	FW_C_TPB_N	FW_C_TPB_N_SPN	MAKE_BASE=TRUE 5B7 MAKE_BASE=TRUE

39C6 =FWPWR_PWRON — NC_FWPWR_PWRON — NO_TEST=TRUE MAKE_BASE=TRUE

USB PORT A = External USB2.0 Port

42C5 =USB2_EXTA_P — USB2_EXTA_P — MAKE_BASE=TRUE — USB_A_P 22C2
42C5 =USB2_EXTA_N — USB2_EXTA_N — MAKE_BASE=TRUE — USB_A_N 22C2
42C8 =EXTAUSB_OC_L — EXTAUSB_OC_L — MAKE_BASE=TRUE — USB_A_OC_L 22C4 22D8

USB PORT B = Trackpad(Geyser)

40C7 =USB2_GEYSER_P — USB2_GEYSER_P — MAKE_BASE=TRUE — USB_B_P 22C2
40C7 =USB2_GEYSER_N — USB2_GEYSER_N — MAKE_BASE=TRUE — USB_B_N 22C2

USB PORT C = External USB2.0 Port B

42B5 =USB2_EXTB_P — USB2_EXTB_P — MAKE_BASE=TRUE — USB_C_P 22C2
42B5 =USB2_EXTB_N — USB2_EXTB_N — MAKE_BASE=TRUE — USB_C_N 22C2
42C8 =EXTBUSB_OC_L — EXTBUSB_OC_L — MAKE_BASE=TRUE — USB_C_OC_L 22C4 22D8

USB PORT D = CAMERA

67B4 =USB2_CAMERA_P — USB2_CAMERA_P — MAKE_BASE=TRUE — USB_D_P 22C2
67A4 =USB2_CAMERA_N — USB2_CAMERA_N — MAKE_BASE=TRUE — USB_D_N 22C2

USB PORT "E" = Unused

5C1 TP_USBP_E — MAKE_BASE=TRUE — USB_E_P 22C2
5C1 TP_USBN_E — MAKE_BASE=TRUE — USB_E_N 22C2

USB PORT "F" = IR CONTROLLER

41C6 =USB2_IR_P — USB_IR_P — USB_F_P 22C2
41C6 =USB2_IR_N — USB_IR_N — MAKE_BASE=TRUE — USB_F_N 22C2 MAKE_BASE=TRUE

USB PORT "G" = BLUETOOTH

44C6 =USB2_BT_P — USB_BT_P — MAKE_BASE=TRUE — USB_G_P 22C2
44C6 =USB2_BT_N — USB_BT_N — MAKE_BASE=TRUE — USB_G_N 22C2

USB PORT "H" = PCI-E Mini Card

43B4 =USB2_AIRPORT_P — USB2_AIRPORT_P — MAKE_BASE=TRUE — USB_H_P 22C2
43B4 =USB2_AIRPORT_N — USB2_AIRPORT_N — MAKE_BASE=TRUE — USB_H_N 22C2

ANALOG SWITCH GPIO

69A6 =SB_GPIO22 — SB_GPIO22 — MAKE_BASE=TRUE — TP_SB_GPIO22 22B6

45B8 14B7 PM_EXTTS_L<0> — MAKE_BASE=TRUE — DIMM_OVERTEMP_L 28C4 29C4

47C5 21C4 5C2 FWH_INIT_L — MAKE_BASE=TRUE — SMC_CPU_INIT_3_3_L 45D5

SIGNAL ALIAS /RESET

SYNC_MASTER=ENET — SYNC_DATE=08/19/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

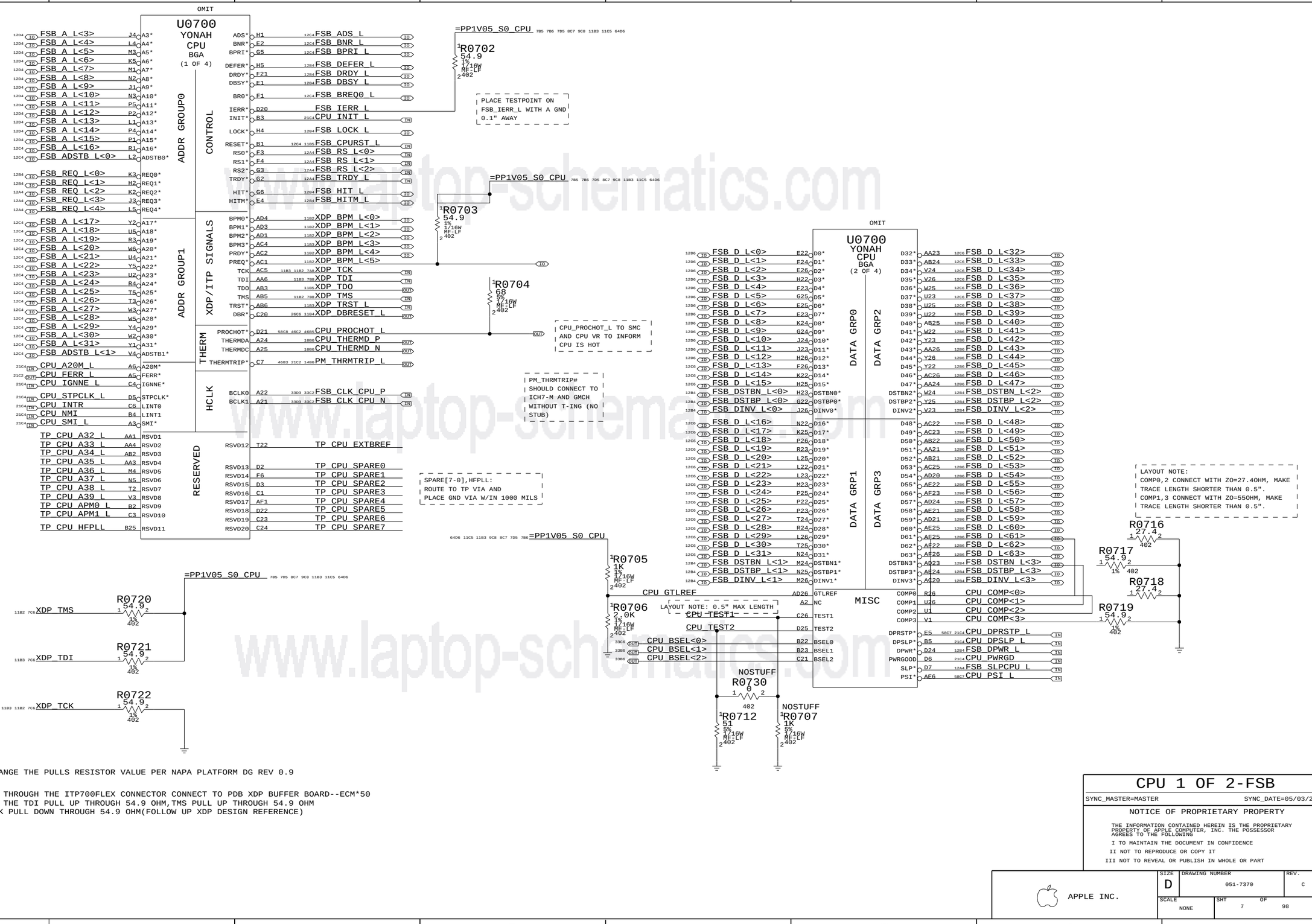
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 6 OF 98	



CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

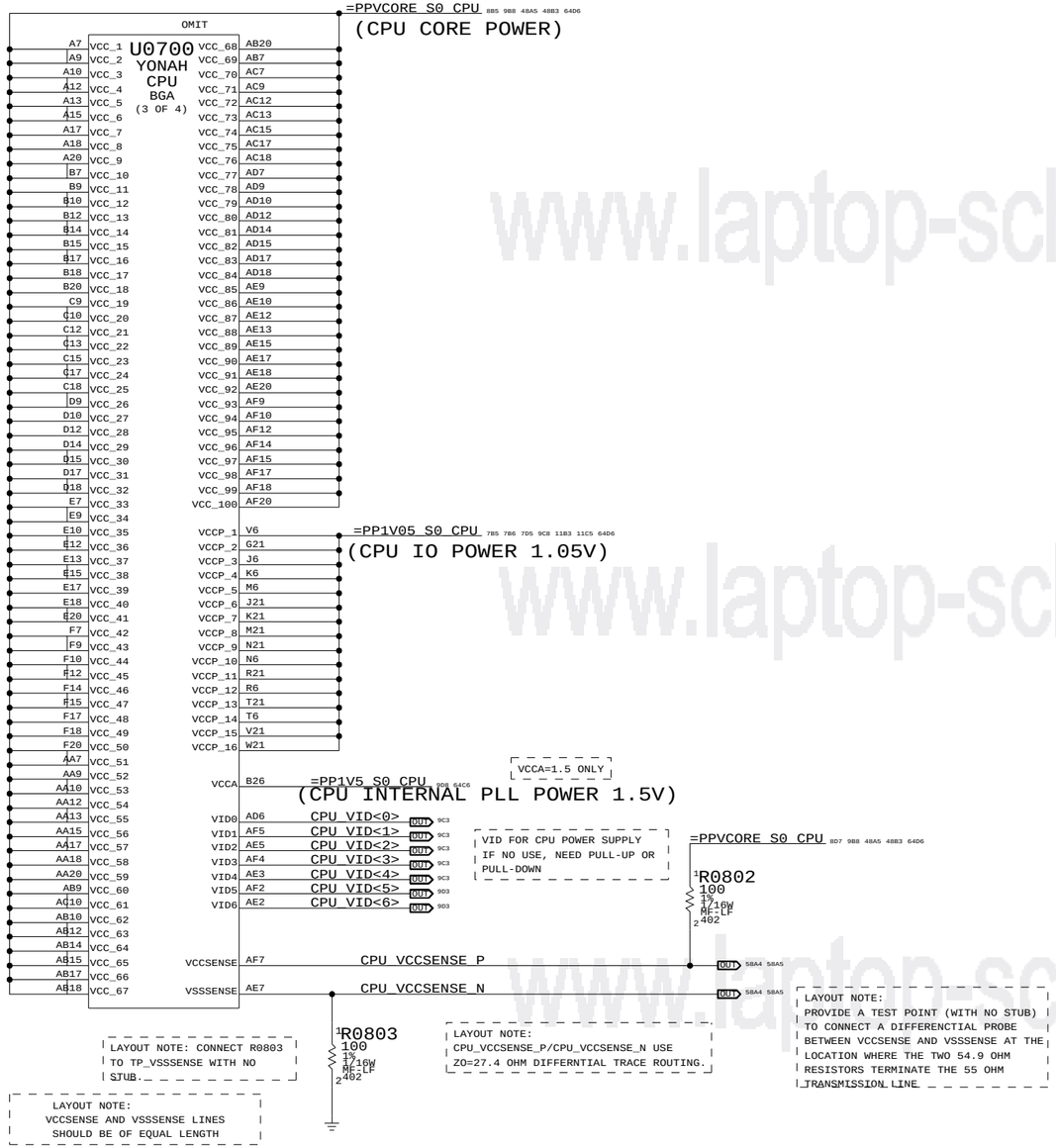
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

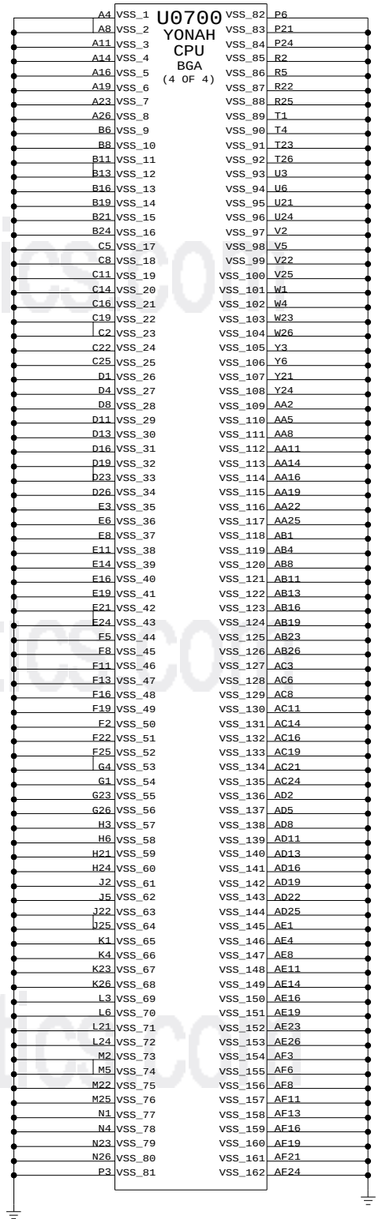
CPU 1 OF 2-FSB

SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 7 OF 98	





CPU 2 OF 2-PWR/GND

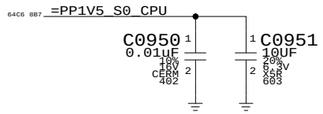
SYNC_MASTER=MASTER SYNC_DATE=05/03/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

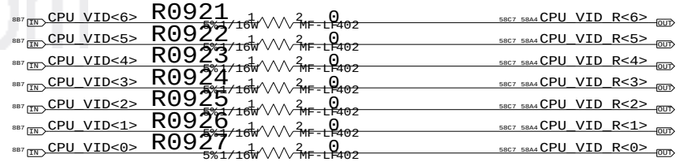
SCALE	SHT	OF
NONE	8	98

VCCA DECOUPLING
(CPU INTERNAL PLL POWER 1.5V)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602	?	ALL	USE SAMSUNG AND MURATA ONLY
138S0606	138S0602	?	ALL	USE TAIYO

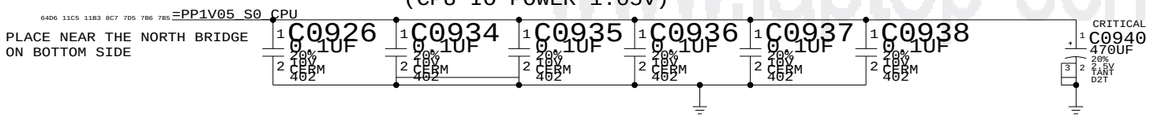
CPU CORE VID<> SETTINGS



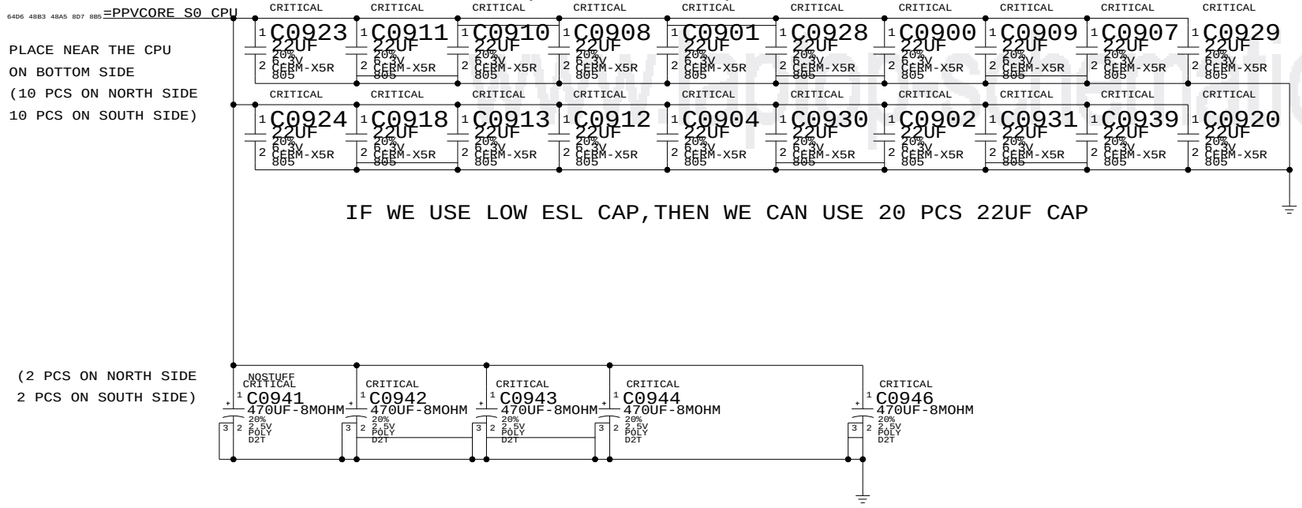
R0921~R0927 FOR CPU VOLTAGE MANUAL SETTING

VCCP CORE DECOUPLING
(CPU IO POWER 1.05V)

THIS 470UF FOR CPU,GMCH FSB BUS 1.05V



VCC CORE DECOUPLING
(CPU CORE POWER)



IF WE USE LOW ESL CAP,THEN WE CAN USE 20 PCS 22UF CAP

		MIN	TYP	MAX
DUAL CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM	TBD		TBD
SINGLE CORE SV CPU	VCCHFM	1.1625		1.30
	VCCLFM		TBD	
DUAL CORE LV CPU	VCCHFM	1.0		1.1625
	VCCLFM		TBD	
ULV CPU	VCCHFM	TBD		TBD
	VCCLFM		TBD	

UNIT: V

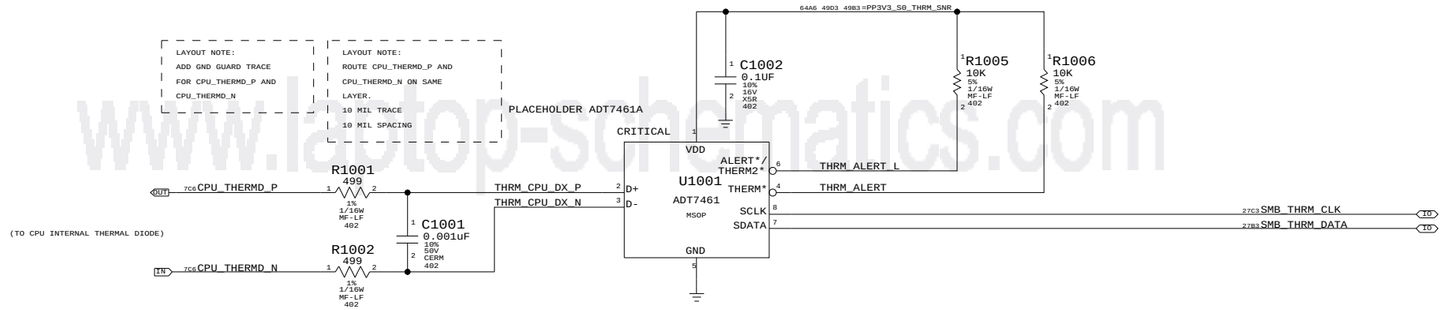
ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V
TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE(VCORE VOLTAGE)!
REFER TO YONAH PROCESSOR EMTS REV 1.0
VCCHFM: VCORE AT HIGHEST FREQUENCY MODE
VCCLFM: VCORE AT LOWEST FREQUENCY MODE

CPU DECAPS & VID<>

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 9 OF 98	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

SYNC_MASTER=ENET SYNC_DATE=08/19/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 10 OF 98	

CPU ITP700FLEX DEBUG SUPPORT

64D6 11B3 9C8 8C7 7D5 7B6 7B5 =PP1V05_S0_CPU

R1101 54.9 1% 1/16W MF-LF 402

R1103 54.9 1% 1/16W MF-LF 402

ITP R1102 22.6 1% 1/16W MF-LF 402

7C6 IN XDP_TDO

ITP R1100 22.6 1% 1/16W MF-LF 402

12C4 7D6 IN FSB_CPURST_L

64A3 26C5 23D1 =PP3V3_S5_SB_PM

R1104 240 5% 1/16W MF-LF 402

OUT 26C6 7C6 XDP_DBRESET_L

(AND WITH RESET BUTTON)

ITP CRITICAL J1102 F-ST-5047 SM1

7C6 7B8 OUT XDP_TDI	1	2	XDP_TMS 7C6 7B8 OUT
7C6 OUT XDP_TRST_L	3	4	NC
11B2 7C6 7A8 OUT XDP_TCK (TCK)	5	6	NC
ITP_TDO	7	8	
33D3 33D2 IN CPU_XDP_CLK_N	9	10	XDP_TCK (FBO)
33D3 33D2 IN CPU_XDP_CLK_P	11	12	7C6 XDP_BPM_L<5> IO
	13	14	7C6 XDP_BPM_L<4> IO
ITPRESET_L	15	16	
7C6 IO XDP_BPM_L<3>	17	18	7C6 XDP_BPM_L<2> IO
	19	20	7C6 XDP_BPM_L<1> IO
	21	22	7C6 XDP_BPM_L<0> IO
	23	24	
	25	26	
	27	28	
	29	30	

516S0416

(FROM CK410M HOST 133/167MHZ)

9C8 8C7 7D5 7B6 7B5 6A06 11C6 =PP1V05_S0_CPU

ITP C1100 0.1UF 10% 16V X5R 402

R1106 680 5% 1/16W MF-LF 402

(DBA#) INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.

(DEBUG PORT ACTIVE)

(DBR#) TO ICH7M SYS_RST*, AND WITH SYSTEM RESET LOGIC

(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 11 OF 98	

NB CPU Interface

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 12 OF 98	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

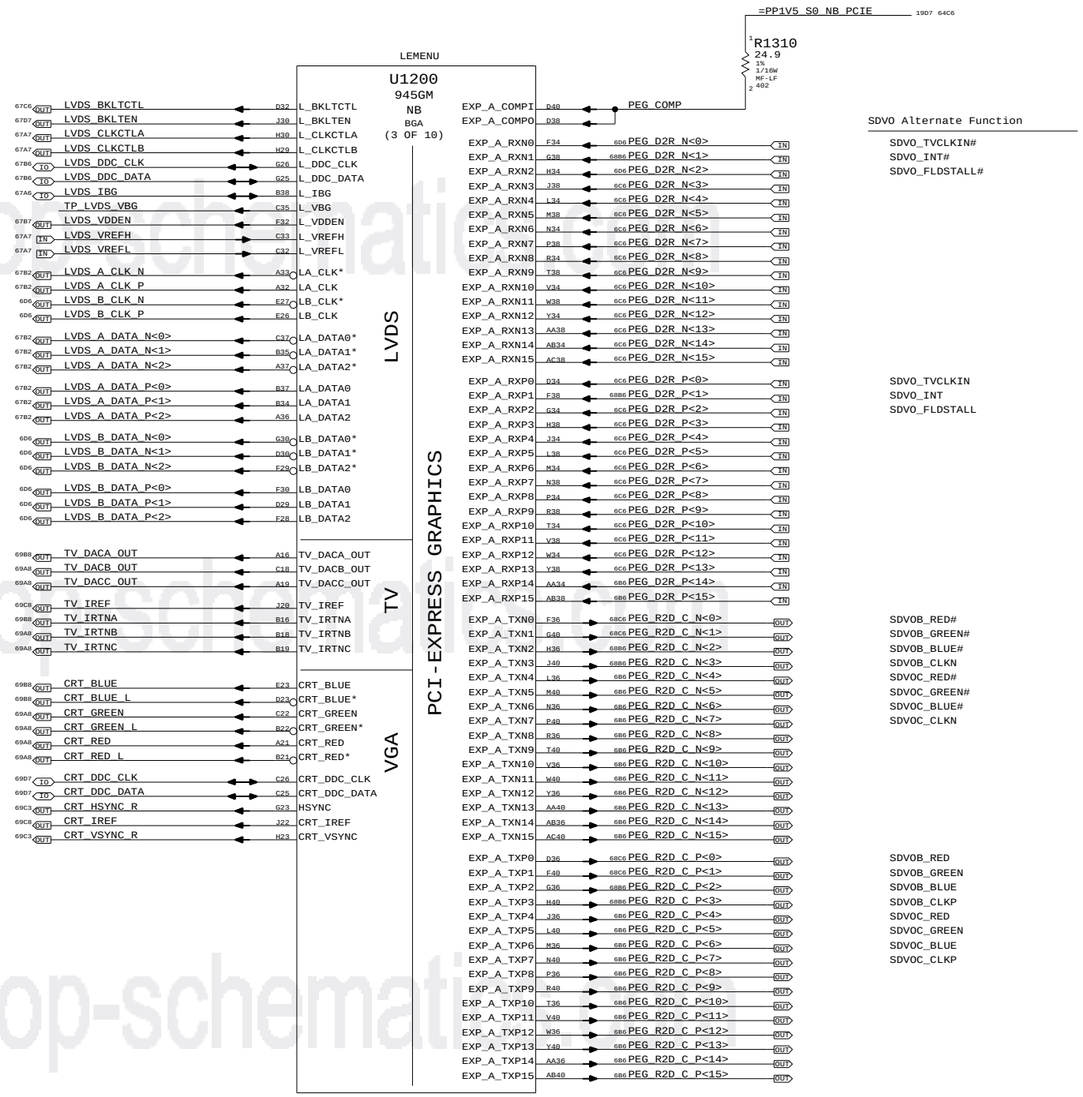
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

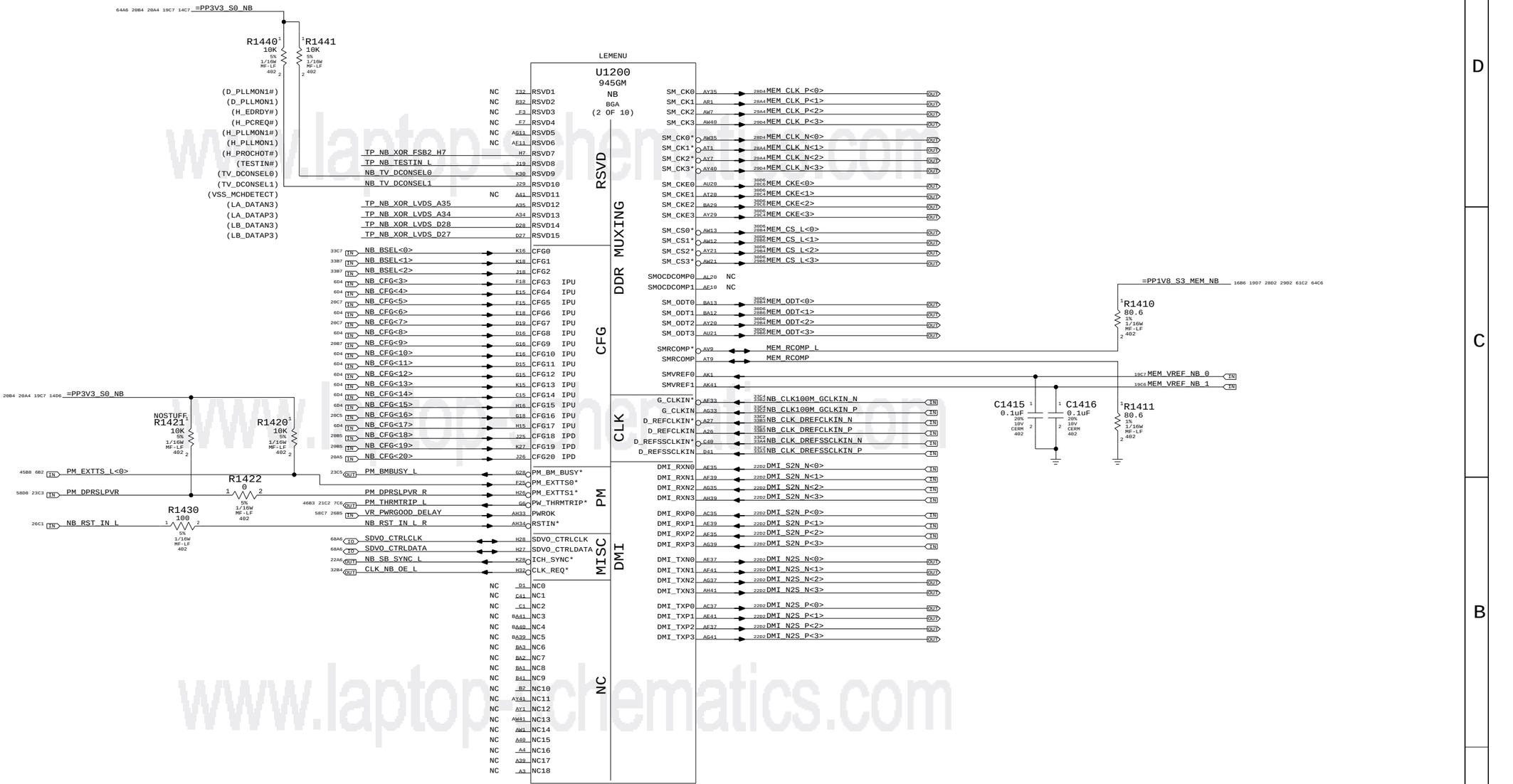


NB PEG / Video Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 13 OF 98	

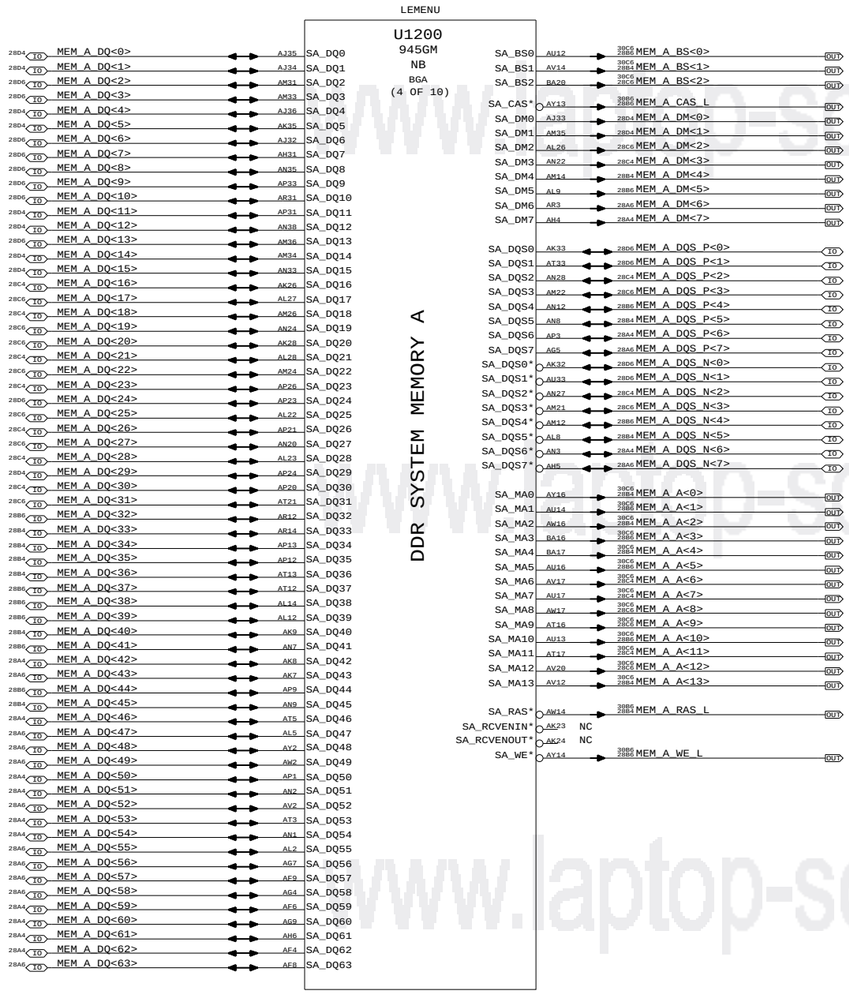


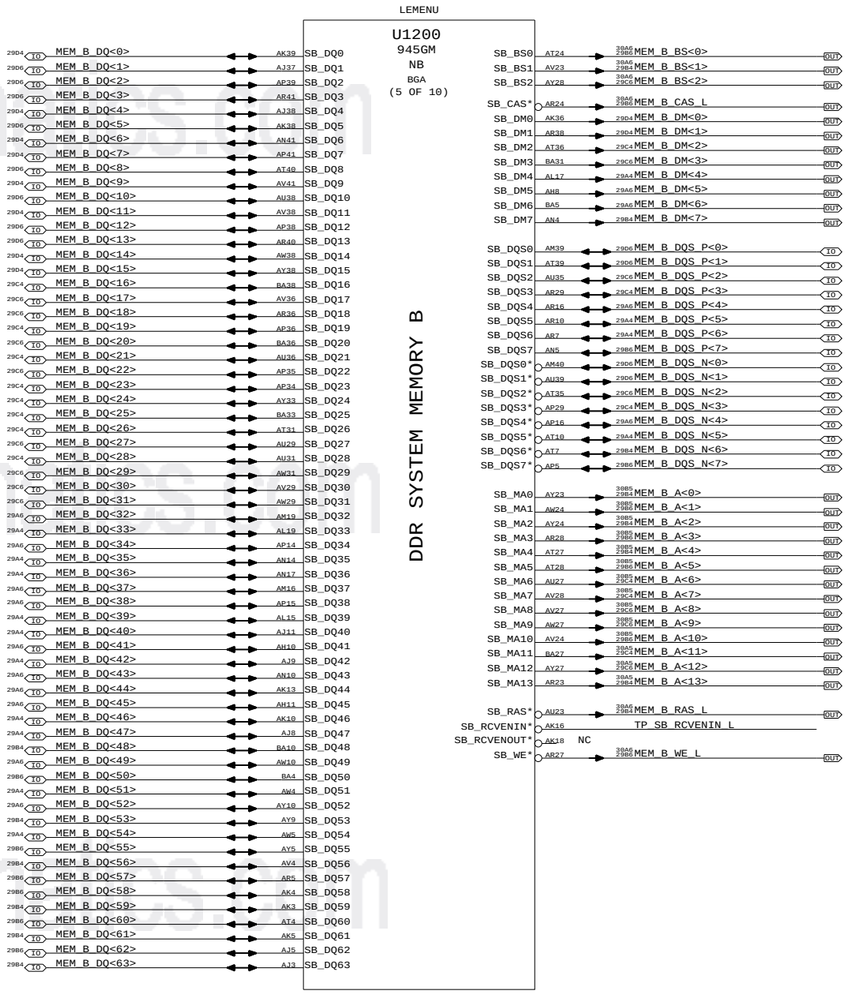
NB Misc Interfaces

SYNC_MASTER=NB SYNC_DATE=08/15/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 14 OF 98	



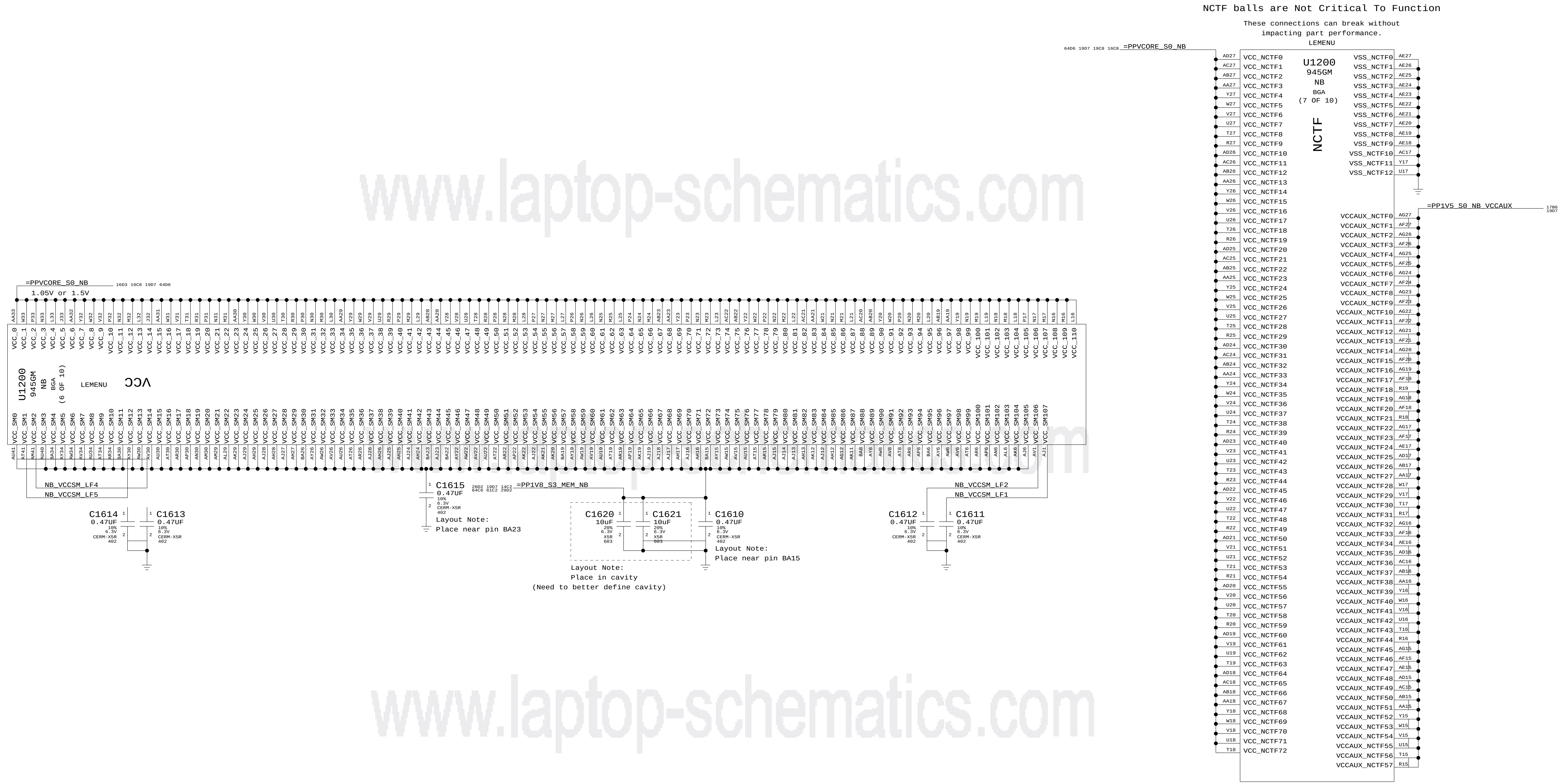


NB DDR2 Interfaces

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 15 OF 98	



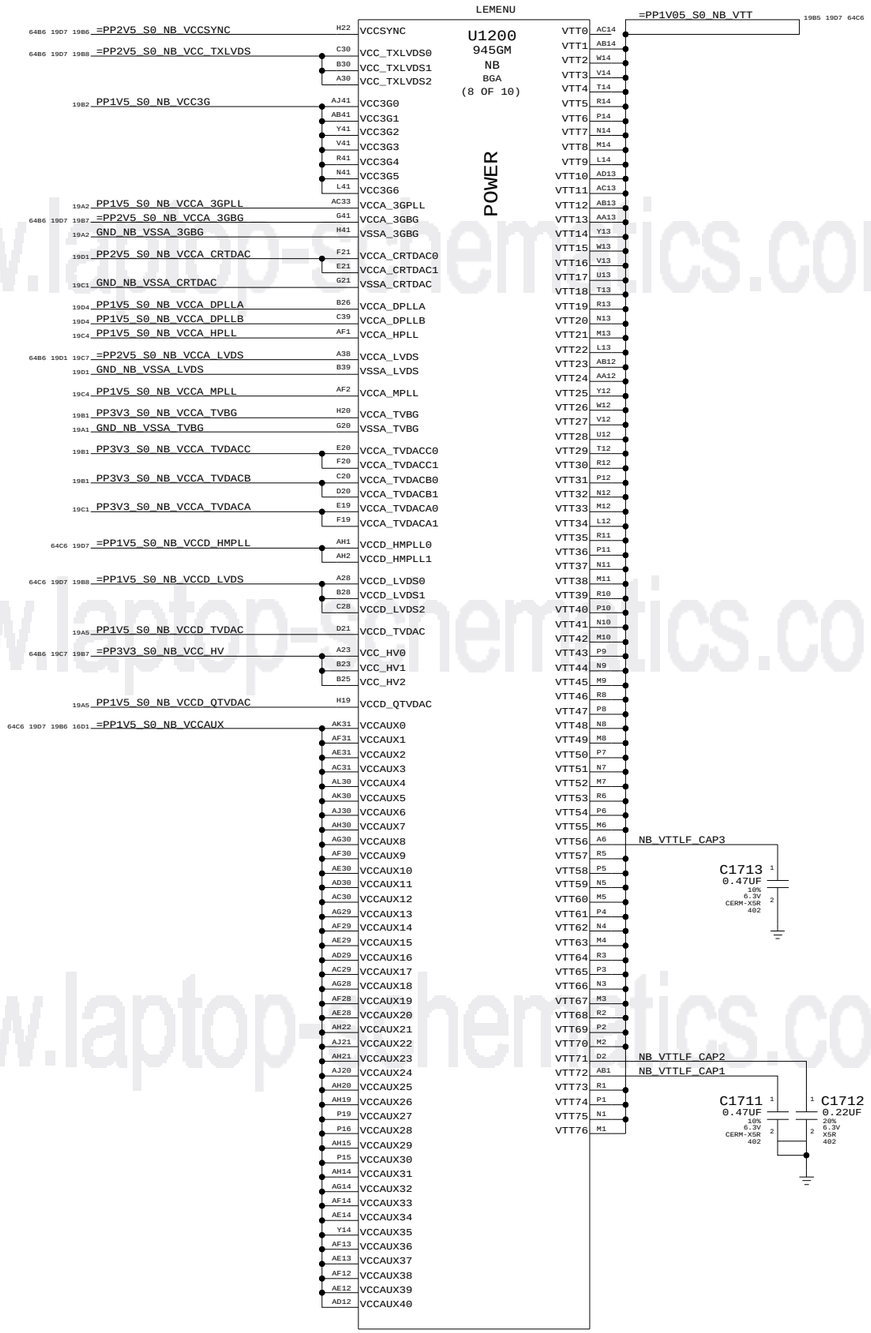
NB Power 1

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	16	98

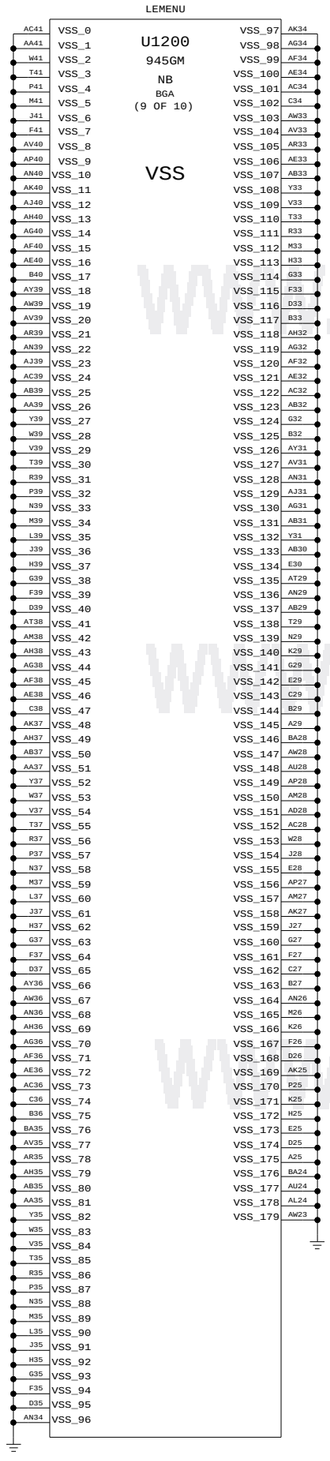


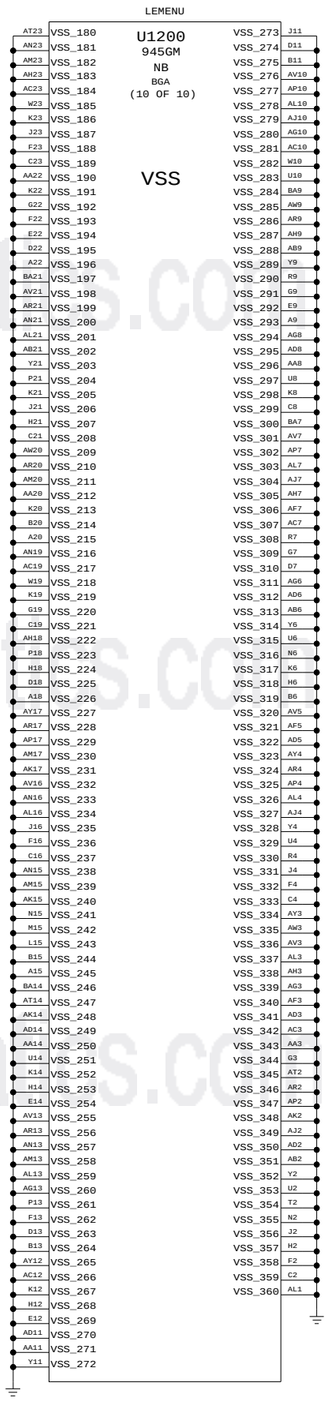
NB Power 2

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 17 OF 98	





NB Grounds

SYNC_MASTER=NB SYNC_DATE=07/25/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 18 OF 98	

Power Interface

These are the power signals that leave the NB "block"

IN =PP1V05_S0_FSB_NB 12A7 12B7 12C2 33B8 33C7 33C8 64D6
IN =PPVCORE_S0_NB 16C8 16D3 19C8 64D6
IN =PP1V05_S0_NB 19D1 64C6
IN =PP1V05_S0_NB_VTT 17D3 19B5 64C6

IN =PP1V5_S0_NB 19C1 64C6
IN =PP1V5_S0_NB_PCIE 13D2 64C6
IN =PP1V5_S0_NB_PLL 19C6 64C6
IN =PP1V5_S0_NB_TVDAC 19A8 64C6
IN =PP1V5_S0_NB_VCCD_HMPLL 17C6 64C6
IN =PP1V5_S0_NB_VCCD_LVDS 17C6 19B8 64C6
IN =PP1V5_S0_NB_VCCAUX 16D1 17B6 19B6 64C6
IN =PP1V8_S3_MEM_NB 14C2 16B6 28D2 29D2 61C2 64C6

IN =PP2V5_S0_NB_CRTDAC 19D4 64B6

IN =PP2V5_S0_NB_VCCSYNC 17D6 19B6 64B6
IN =PP2V5_S0_NB_VCC_TXLVDS 17D6 19B8 64B6
IN =PP2V5_S0_NB_VCCA_3GBG 17D6 19B7 64B6
IN =PP2V5_S0_NB_VCCA_LVDS 17C6 19D1 64B6

IN =PP3V3_S0_NB 14C7 14D6 28A4 28B4 64A6
IN =PP3V3_S0_NB_VCC_HV 17C6 19B7 64B6

IN =PP5V_S0_NB_TVDAC 19C4 64D3

MCH DISPLAY PLL POWER LDO

64B6 =PP2V5_S0_NB_DISP_PLL
CRITICAL
U1900 TPS73115 SOT23-5
IN OUT 5 PP1V5_S0_DPLL
EN NR/FB 4 TPS73115_NR
GND 2
C1950 1UF 10% 6.3V CERM 402
C1951 0.01uF 20% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603

R1950 0 5% 1/16W MF-LF 402
MCH VCCA_DPLLA FILTER
(MCH DISPLAY A PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLA 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1953 0.1uF 20% 10V CERM 402

R1951 0 5% 1/16W MF-LF 402
GMCH VCCA_DPLL_B FILTER
(MCH DISPLAY B PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_DPLLB 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1954 0.1uF 20% 10V CERM 402

Layout Note:
THESE 4 0.1UF CAPS SHOULD
be within 5 mm of NB edge

MCH VCCA_LVDS FILTER

(MCH LVDS ANALOG 2.5V PWR)
=PP2V5_S0_NB_VCCA_LVDS 17C6 19C7 64B6
C1980 0.1uF 20% 10V CERM 402
C1981 0.01uF 10% 16V CERM 402
GND_NB_VSSA_LVDS 17C6

Layout Note:
This 0.1uF cap should
be within 5 mm of NB edge

Layout Note: Route to caps, then GND

64B6 19D7 =PP2V5_S0_NB_CRTDAC
R1985 10 1% 1/16W MF-LF 402
PP2V5_S0_NB_CRTDAC_FOLLOW
VOLTAGE=2.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363
=PP1V05_S0_NB 19D7 64C6
L1985 180-OHM-1.5A 0603
PP2V5_S0_NB_CRTDAC_F
C1986 22000pF-1000mA 16V NFM18

MCH VCCA_CRTDAC BYPASS
(MCH CRTDAC ANALOG 2.5V PWR)
PP2V5_S0_NB_VCCA_CRTDAC 17D6
VOLTAGE=2.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1985 0.1uF 20% 10V CERM 402

Layout Note:
These 2 caps should be
within 6.35 mm of NB edge

GND_NB_VSSA_CRTDAC 17D6
Layout Note: Route to caps, then GND

GMCH VCCA_HPLL FILTER

(HOST PLL 1.5V PWR)
64C6 19D7 =PP1V5_S0_NB_PLL
L1934 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_HPLL 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
CRITICAL
C1934 22UF 20% 6.3V CERM-X5R 805
C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER

(MCH MEMORY PLL 1.5V PWR)
L1936 FERR-120-OHM-0.2A 0603
PP1V5_S0_NB_VCCA_MPLL 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
CRITICAL
C1936 22UF 20% 6.3V CERM-X5R 805
C1937 0.1uF 20% 10V CERM 402

64C3 29D6 29D4 29B2 28D6 28D4 28B2 19C8 64C3 29D6 29D4 =PP1V8_S3_MEM
PLACE THOSE COMPONENT
CLOSE TO GMCH
R1988 1K 1% 1/16W MF-LF 402
MEM_VREF_NB_0 14C2
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
R1989 1K 1% 1/16W MF-LF 402
R1986 1K 1% 1/16W MF-LF 402
MEM_VREF_NB_1 14C2
R1987 1K 1% 1/16W MF-LF 402

GMCH CORE PWR 1.05V BYPASS
THIS 470UF FOR GMCH CORE 1.05V

19D7 16D3 16C8 64D6 =PPVCORE_S0_NB
CRITICAL
C1900 470UF 20% 2.5V TANT D2T
C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1UF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)
64C6 19D7 17C6 =PP1V5_S0_NB_VCCD_LVDS
C1910 10uF 20% 6.3V X5R 603
C1911 0.1uF 20% 10V CERM 402

MCH VCC_HV BYPASS

(MCH HV BUFFER 3.3V PWR)
64B6 19C7 17C6 =PP3V3_S0_NB_VCC_HV
C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

MCH VCCSYNC BYPASS

(MCH H/V SYNC 2.5V PWR)
19D7 17D6 64B6 =PP2V5_S0_NB_VCCSYNC
C1917 0.1uF 20% 10V CERM 402

945 EDS: 5 mOhm, 1nH (1210?)

GMCH VCCTX_LVDS BYPASS

(MCH LVDS DATA/CLK TX 2.5V PWR)
64B6 19D7 17D6 =PP2V5_S0_NB_VCC_TXLVDS
C1912 4.7uF 20% 6.3V CERM 603
C1913 0.1uF 20% 10V CERM 402
945 EDS: 1210?

MCH VCCA_3GBG BYPASS

(MCH PCIE/DMI BAND GAP 2.5V PWR)
64B6 19D7 17D6 =PP2V5_S0_NB_VCCA_3GBG
C1916 0.1uF 20% 10V CERM 402

GMCH VCCAUX FILTER

(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
64C6 19D7 17B6 16D1 =PP1V5_S0_NB_VCCAUX
C1918 0.1uF 20% 10V CERM 402

MCH VTT BYPASS

(MCH FSB 1.05V PWR) (SHARE C0940 470UF)
64C6 19D7 17D3 =PP1V05_S0_NB_VTT
C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603
Layout Note:
Place in cavity
C1967 0.22uF 20% 6.3V X5R 402
Layout Note:
Place on the edge

64C6 19D7 =PP1V5_S0_NB_TVDAC
C1921 22000pF-1000mA 16V NFM18
GMCH VCCD_TVDAC FILTER
(MCH TVDAC DEDICATED PWR 1.5V)
PP1V5_S0_NB_VCCD_TVDAC 17C6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1920 0.1uF 20% 10V CERM 402

Layout Note:
These 4 caps should be
within 6.35 mm of NB edge

L1922 180-OHM-1.5A 0603
PP1V5_S0_NB_QTVDAC
C1923 22000pF-1000mA 16V NFM18

GMCH VCCD_QTVDAC FILTER
(MCH TVDAC DIGITAL QUIET 1.5V PWR)
PP1V5_S0_NB_VCCD_QTVDAC 17B6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1922 0.1uF 20% 10V CERM 402

91NH, 20%, 20MOHM, 1.5A (1210 TYP)
CRITICAL
L1970 91nH 1210
64C6 =PP1V5_S0_NB_3G
CRITICAL
C1970 220UF 20% 2.5V POLY CASE-B2

Layout Note:
Place L and C
close to MCH

GMCH VCC3G FILTER

(PCI-E/DMI ANALOG 1.5V PWR)
PP1V5_S0_NB_VCC3G 17D6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603

Layout Note:
10uF caps should
be close to MCH
on opposite side.

1uH, 20%
64C6 =PP1V5_S0_NB_3GPLL
L1975 1.0UH-220MA-0.12-OHM 0805
PP1V5_S0_NB_3GPLL_F
R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER

(3GIO PLL 1.5V PWR)
PP1V5_S0_NB_VCCA_3GPLL 17D6
VOLTAGE=1.5V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402

Layout Note:
3GPLL 10uF cap should
be placed in cavity

GND_NB_VSSA_3GBG 17D6
Layout Note: Route to caps, then GND

64C3 29D6 29D4 29B2 28D6 28D4 28B2 19C8 64C3 29D6 29D4 =PP1V8_S3_MEM
R1990 10 1% 1/16W MF-LF 402
PP3V3_S0_NB_TVDAC_FOLLOW
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
D1986 BAT54DW SOT-363
=PP1V5_S0_NB 19D7 64C6
L1990 180-OHM-1.5A 0603
PP3V3_S0_NB_TVDAC_F
C1990 10uF 20% 6.3V X5R 603
C1991 0.1uF 20% 10V CERM 402
C1992 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL A 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACA 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1994 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL B 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACB 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1993 0.1uF 20% 10V CERM 402

Layout Note:
These 8 caps should be
within 6.35 mm of NB edge

C1996 22000pF-1000mA 16V NFM18

MCH VCCA_TVDACC FILTER
(MCH TV OUT CHANNEL C 3.3V PWR)
PP3V3_S0_NB_VCCA_TVDACC 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1995 0.1uF 20% 10V CERM 402

C1998 22000pF-1000mA 16V NFM18

MCH VCCA_TVBG FILTER
(MCH TV DAC BAND GAP 3.3V PWR)
PP3V3_S0_NB_VCCA_TVBG 17C6
VOLTAGE=3.3V
MIN_LINE_WIDTH=1.0 mm
MIN_NECK_WIDTH=1.0 mm
C1997 0.1uF 20% 10V CERM 402

GND_NB_VSSA_TVBG 17C6
Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=NB SYNC_DATE=06/22/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 19 OF 98	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 64A6
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 64A6
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14C7 14D6 19C7 20B4 64A6
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

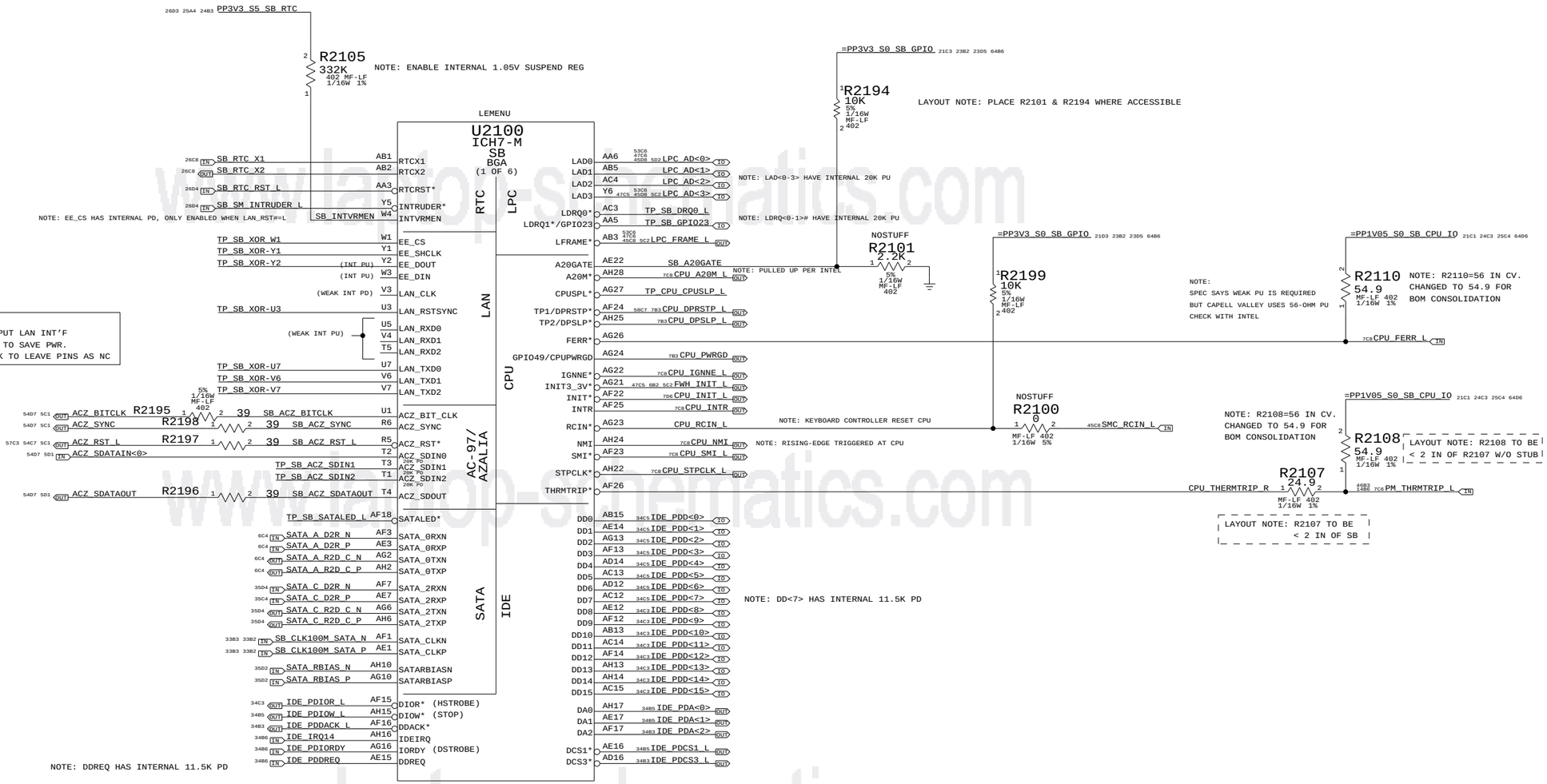
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=NB SYNC_DATE=06/28/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 20 OF 98	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

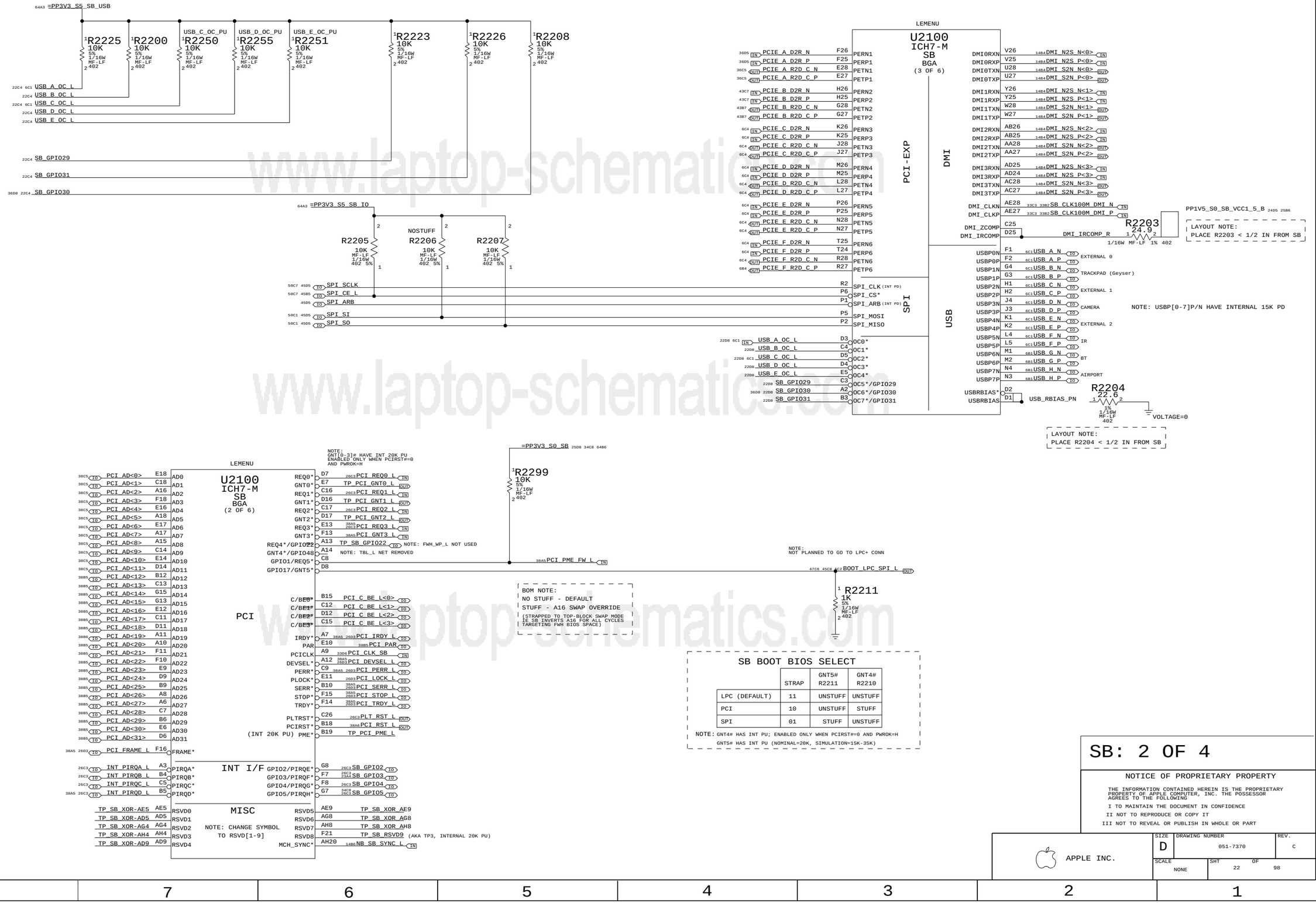
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 21 OF 98	


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
USB_C_OC_PU
R2250 10K 5% 1/16W MF-LF 402
USB_D_OC_PU
R2255 10K 5% 1/16W MF-LF 402
USB_E_OC_PU
R2251 10K 5% 1/16W MF-LF 402
R2223 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
R2208 10K 5% 1/16W MF-LF 402
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO31
SB_GPIO30
=PP3V3_S5_SB_IO
R2205 10K MF-LF 1/16W 402 5%
NOSTUFF
R2206 10K MF-LF 1/16W 402 5%
R2207 10K MF-LF 1/16W 402 5%
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
LEMENU
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCIE_A_D2R_N
PCIE_A_D2R_P
PCIE_A_R2D_C_N
PCIE_A_R2D_C_P
PCIE_B_D2R_N
PCIE_B_D2R_P
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_C_D2R_N
PCIE_C_D2R_P
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_D_D2R_N
PCIE_D_D2R_P
PCIE_D_R2D_C_N
PCIE_D_R2D_C_P
PCIE_E_D2R_N
PCIE_E_D2R_P
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_F_D2R_N
PCIE_F_D2R_P
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
PCI-EXP
SPI_CLK (INT PD)
SPI_CS*
SPI_ARB (INT PD)
SPI_MOSI
SPI_MISO
SPI
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
USB
DMI
DMI0RXN
DMI0RXP
DMI0TXN
DMI0TXP
DMI1RXN
DMI1RXP
DMI1TXN
DMI1TXP
DMI2RXN
DMI2RXP
DMI2TXN
DMI2TXP
DMI3RXN
DMI3RXP
DMI3TXN
DMI3TXP
DMI_CLKN
DMI_CLKP
DMI_ZCOMP
DMI_IRCOMP
DMI_IRCOMP_R
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE: PLACE R2203 < 1/2 IN FROM SB
USBP0N
USBP0P
USBP1N
USBP1P
USBP2N
USBP2P
USBP3N
USBP3P
USBP4N
USBP4P
USBP5N
USBP5P
USBP6N
USBP6P
USBP7N
USBP7P
USBRBIAS*
USBRBIAS
USB_RBIAS_PN
R2204 22.6 1% 1/16W MF-LF 402
VOLTAGE=0
LAYOUT NOTE: PLACE R2204 < 1/2 IN FROM SB
EXTERNAL 0
TRACKPAD (Geyser)
EXTERNAL 1
CAMERA
EXTERNAL 2
IR
BT
AIRPORT
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
NOTE: GNT[0-3]# HAVE INT 20K PU ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
=PP3V3_S0_SB
R2299 10K 5% 1/16W MF-LF 402
PCI_AD<0>
PCI_AD<1>
PCI_AD<2>
PCI_AD<3>
PCI_AD<4>
PCI_AD<5>
PCI_AD<6>
PCI_AD<7>
PCI_AD<8>
PCI_AD<9>
PCI_AD<10>
PCI_AD<11>
PCI_AD<12>
PCI_AD<13>
PCI_AD<14>
PCI_AD<15>
PCI_AD<16>
PCI_AD<17>
PCI_AD<18>
PCI_AD<19>
PCI_AD<20>
PCI_AD<21>
PCI_AD<22>
PCI_AD<23>
PCI_AD<24>
PCI_AD<25>
PCI_AD<26>
PCI_AD<27>
PCI_AD<28>
PCI_AD<29>
PCI_AD<30>
PCI_AD<31>
PCI_FRAME_L
PCI
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
FRAME*
REQ0*
GNT0*
REQ1*
GNT1*
REQ2*
GNT2*
REQ3*
GNT3*
REQ4*/GPIO22
GNT4*/GPIO48
GPIO1/REQ5*
GPIO17/GNT5*
PCI_REQ0_L
TP_PCI_GNT0_L
PCI_REQ1_L
TP_PCI_GNT1_L
PCI_REQ2_L
TP_PCI_GNT2_L
PCI_REQ3_L
PCI_GNT3_L
TP_SB_GPIO22
NOTE: FWH_WP_L NOT USED
NOTE: TBL_L NET REMOVED
PCI_PME_FW_L
C/BE0*
C/BE1*
C/BE2*
C/BE3*
PCI_C_BE_L<0>
PCI_C_BE_L<1>
PCI_C_BE_L<2>
PCI_C_BE_L<3>
IRDY*
PAR
PCICLK
DEVSEL*
PERR*
PLOCK*
SERR*
STOP*
TRDY*
PCI_IRDY_L
PCI_PAR
PCI_CLK_SB
PCI_DEVSEL_L
PCI_PERR_L
PCI_LOCK_L
PCI_SERR_L
PCI_STOP_L
PCI_TRDY_L
PLTRST*
PCIRST*
(INT 20K PU) PME*
PLT_RST_L
PCI_RST_L
TP_PCI_PME_L
INT I/F
PIRQA*
PIRQB*
PIRQC*
PIRQD*
INT_PIRQA_L
INT_PIRQB_L
INT_PIRQC_L
INT_PIRQD_L
GPIO2/PIRQE*
GPIO3/PIRQF*
GPIO4/PIRQG*
GPIO5/PIRQH*
SB_GPIO2
SB_GPIO3
SB_GPIO4
SB_GPIO5
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
RSVD5
RSVD6
RSVD7
RSVD8
MCH_SYNC*
TP_SB_XOR-AE5
TP_SB_XOR-AD5
TP_SB_XOR-AG4
TP_SB_XOR-AH4
TP_SB_XOR-AD9
TP_SB_XOR_AE9
TP_SB_XOR_AG8
TP_SB_XOR_AH8
TP_SB_RSVD9 (AKA TP3, INTERNAL 20K PU)
NB_SB_SYNC_L
BOM NOTE:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE IF SB INVERTS A16 FOR ALL CYCLES TARGETING FWH BIOS SPACE)
NOTE: NOT PLANNED TO GO TO LPC+ CONN
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
SB BOOT BIOS SELECT
STRAP
GNT5# R2211
GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
SB: 2 OF 4
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7370
REV. C
SCALE NONE
SHT 22 OF 98

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21C3 21D3 23B2 64B6

=PP3V3_S5_SB 23A7 23B7 23D8 25C8 64A3

64A3 25C8 23D4 23B7 23A7 =PP3V3_S5_SB

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 10K 1/16W 402 MF-LF 5% NOSTUFF
R2326 10K 1/16W 402 MF-LF 5% NOSTUFF
R2323 1K 1/16W 402 MF-LF 5% NO_REBOOT_MODE

RP2300 10K 5% 1/16W SM-LF

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

LEMENU

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27D8 TO SMB_CLK	C22	SMBCLK
27D8 TO SMB_DATA	B22	SMBDATA
SMB_LINK_ALERT_L	A26	LINKALERT*
SMLINK<0>	B25	SMLINK0
NOT USED SMLINK<1>	A25	SMLINK1
PM_RI_L	A28	RI*

SB_SPKR — A19 SPKR (INT WEAK PD)

53C6 47C5 46D3 45D5 5C2 OUT PM_SUS_STAT_L	A27	SUS_STAT*
45C8 26C5 IN PM_SYSRST_L	A22	SYS_RST*
14B6 IN PM_BMBUSY_L	AB18	GPIO0/BM_BUSY*
SMB_ALERT_L NOTE: RESERVED FOR FUTURE	B23	GPIO11/SMBALERT*
32C4 OUT PM_STPPCI_L	AC20	GPIO18/STPPCI*
32C4 OUT PM_STPCPU_L	AF21	GPIO20/STPCPU*
IN SB_GPIO26	A21	GPIO26
23A6 BIOS_REC	B21	GPIO27
23A6 FWH_MFG_MODE	E23	GPIO28
53C6 47C6 45D5 38A5 5C2 TO PM_CLKRUN_L	AG18	GPIO32/CLKRUN*
RESERVED FOR MOBILE AZALIA DOCKING INT'F — TP_AZ_DOCK_EN_L	AC19	GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L	U2	GPIO34/AZ_DOCK_RST*
43C6 36C6 IN PCIE_WAKE_L	F20	WAKE*
53C6 47C5 45C8 5C2 TO INT_SERIRQ	AH21	SERIRQ
45B8 IN PM_THRM_L	AF20	THRM*
26A8 IN VR_PWRGD_CK410	AD22	VRMPWRGD
TO TP_SB_GPIO6	AC21	GPIO6
SB_RUNTIME_SCI_L	AC18	GPIO7
	E21	GPIO8

SYS GPIO / PWR MNGT

SATA GPIO

GPIO21/SATA0GP	AF19	SB_GPIO21 — 100 — R2302
GPIO19/SATA1GP	AH18	SB_GPIO19 — 100 — R2303
GPIO36/SATA2GP	AH19	
GPIO37/SATA3GP	AE19	SB_GPIO37 — 100 — R2305

35D2 SATA_C_DET_L IN

CLKS

CLK14	AC1	33A6 SB_CLK14P3M_TIMER IN
CLK48	B2	33C7 SB_CLK48M_USBCTLR IN
SUSCLK	C20	68A4 SUS_CLK_SB OUT

SLP_S3*	B24	63A7 63B8 45C5 PM_SLP_S3_L OUT
SLP_S4*	D23	63D6 61B8 60C8 45C5 PM_SLP_S4_L OUT
SLP_S5*	F22	46D3 45C5 PM_SLP_S5_L OUT
PWROK	AA4	26A6 PM_SB_PWROK IN
GPIO16/DPRSLPVR	AC22	58D8 14B7 PM_DPRSLPVR OUT
TP0/BATLOW*	C21	NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN*	C23	45D8 PM_PWRBTN_L IN
LAN_RST*	C19	45D8 PM_LAN_ENABLE IN
RSMRST*	Y4	

NOTE:
SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F
IN RESET STATE TO SAVE PWR

GPIO9	E20	46D6 45B5 SMS_INT_L IN
GPIO10	A20	45D8 SMC_SB_NMI IN
DEF=GPI GPIO12	F19	23B3 PATA_PWR_EN_L OUT
GPIO13	E19	
DEF=GPI GPIO14	R4	23A4 SB_GPIO14 OUT
GPIO15	E22	SV_SET_UP 5C2 23B6 47B5
GPIO24	R3	CRB_SV_DET 23B6
GPIO25	D20	TP_SB_GPIO25_DO_NOT_USE
OD GPIO35	AD21	32B4 SB_CLK100M_SATA_OE_L OUT
GPIO38	AD20	TP_SB_GPIO38 TO
DEF=GPI GPIO39	AE20	23A3 SATA_C_PWR_EN_L OUT

NOTE: PATA_DET IS ACTUALLY CABLE TYPE DETECT

GPIO

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB_PM 11B5 26C5 64A3

R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

45B8 PM_BATLOW_L IN

45D8 PM_RSMRST_L IN

R2399 100K 5% 1/16W 402 MF-LF

45D5 SMC_WAKE_SCI_L IN

R2300 0

45B8 IN SMC_RUNTIME_SCI_L
45B8 IN SMC_EXTSMI_L

SB_RUNTIME_SCI_L

64A3 25C8 23D8 23D4 23A7 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

SV_SET_UP 5C2 23C3 47B5
CRB_SV_DET 23C3

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

64A3 25C8 23D8 23D4 23B7 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23C5
BIOS_REC 23C5

=PP3V3_S0_SB_GPIO 21C3 21D3 23D5 64B6

R2390 10K 5% 1/16W MF-LF 402
R2388 10K 5% 1/16W MF-LF 402

23C3 PATA_PWR_EN_L
23B3 SATA_C_PWR_EN_L

NOSTUFF R2312 0 5% 1/16W MF-LF 402
26C3 22A6 SB_GPIO3

IDE_RESET_L 34C5

R2315 0 5% 1/16W MF-LF 402
23C3 SB_GPIO14

R2389 15K 5% 1/10W MF-LF 402

R2312,R2315 and R2389 close to SB

SB: 3 OF 4

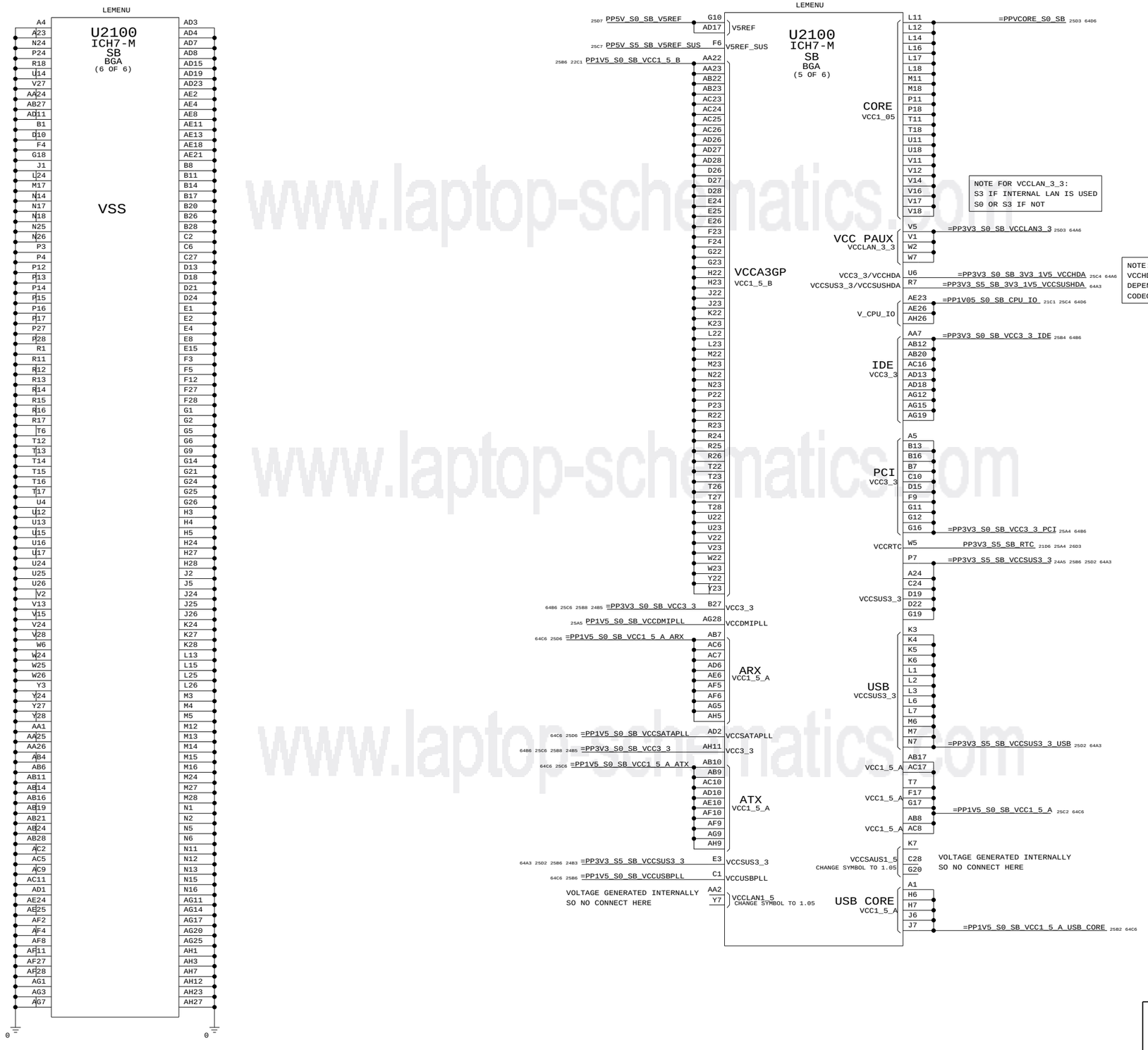
NOTICE OF PROPRIETARY PROPERTY

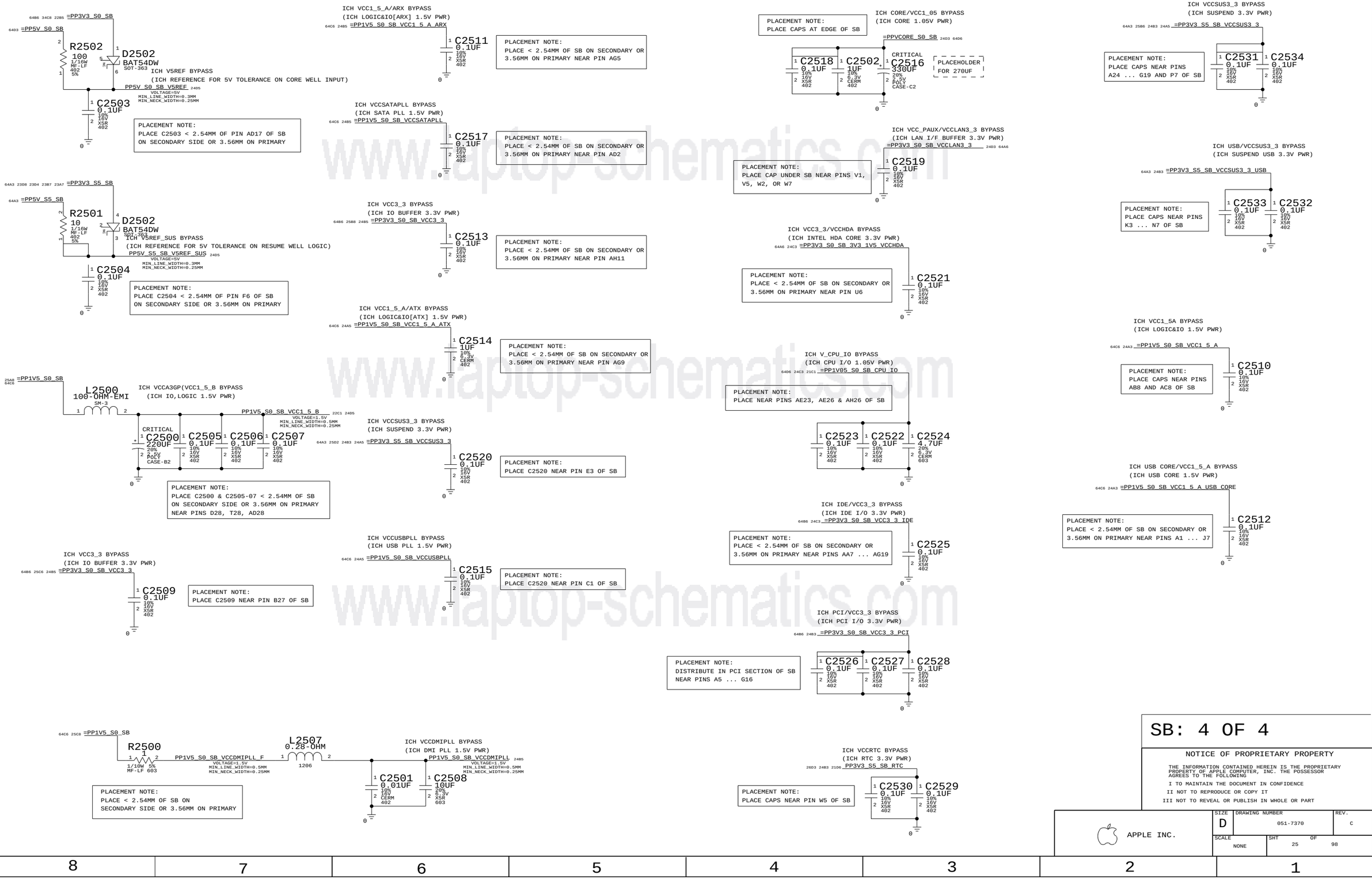
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

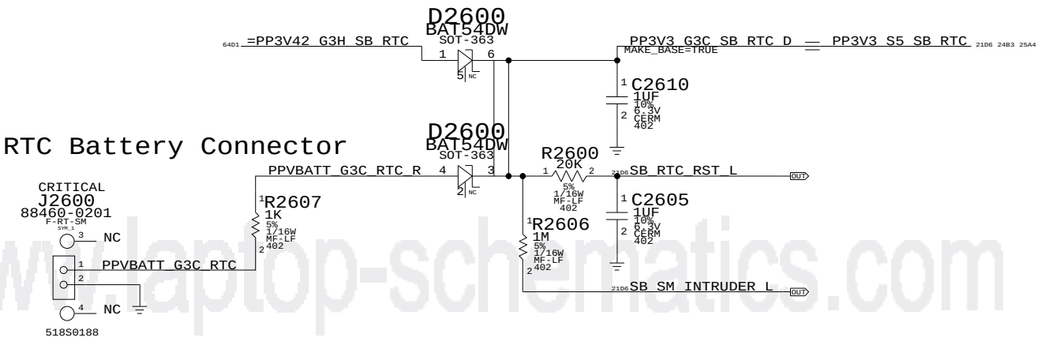
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 23 OF 98	

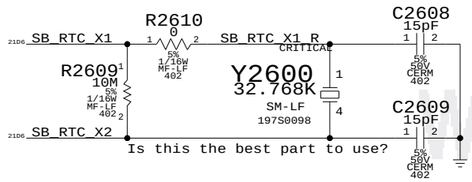


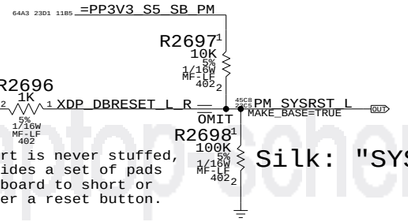

ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V1,
V5, W2, OR W7
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7 ... AG19
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... J7
CRITICAL
PLACEHOLDER FOR 270UF
SB: 4 OF 4
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7370
REV. C
SCALE NONE
SHT 25 OF 98

RTC Battery Connector



SB RTC Crystal Circuit

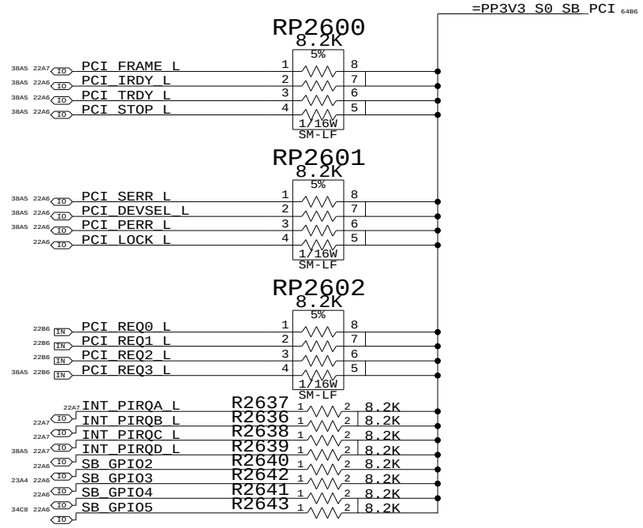




This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

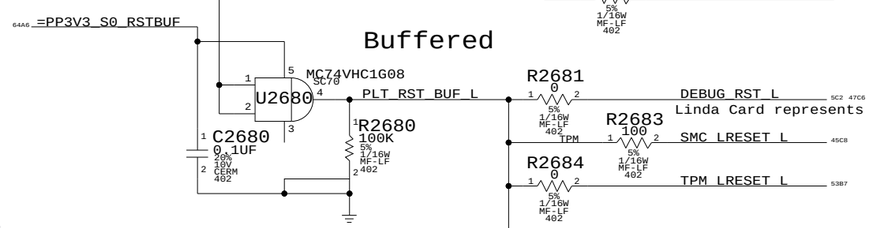
RP2600 / RP2601 / RP2602



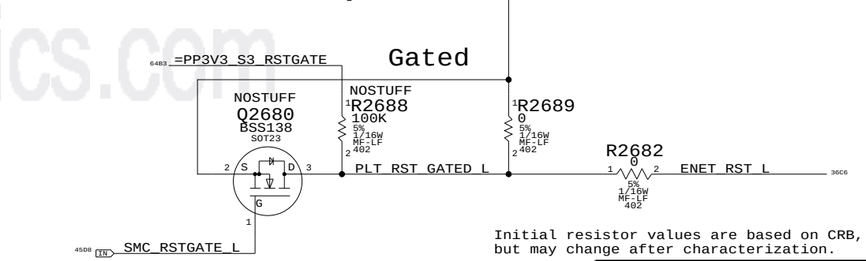
Platform Reset Connections

Unbuffered

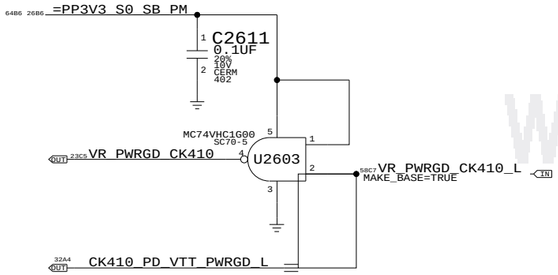
Buffered

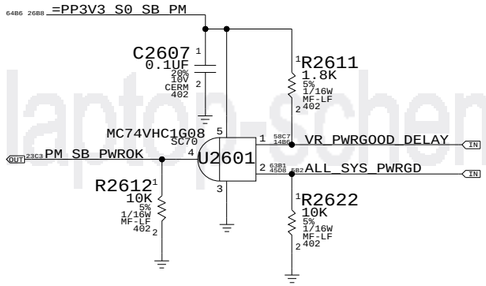


Gated



Initial resistor values are based on CRB, but may change after characterization.





SB Misc

SYNC_MASTER=NB SYNC_DATE=07/26/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 26 OF 98	

ICH7-M SMBus Connections

64A6 =PP3V3_S0_SMBUS_SB

ICH7-M
U2100
(MASTER)

23D5 SMB_CLK — SMBUS_SB_SCL (MAKE_BASE=TRUE)
23D5 SMB_DATA — SMBUS_SB_SDA (MAKE_BASE=TRUE)

R2700 2.0K 5% 1/16W MF-LF 402 — R2701 2.0K 5% 1/16W MF-LF 402

Clock Chip
CY28445-5: U3301
(Write: 0xD2 Read: 0xD3)

SMB_CK410_CLK 32B6
SMB_CK410_DATA 32B6

SO-DIMM "A"
J2800
(Write: 0xA0 Read: 0xA1)

=I2C_SODIMMA_SCL 28A6
=I2C_SODIMMA_SDA 28A6

SO-DIMM "B"
J2900
(Write: 0xA4 Read: 0xA5)

=I2C_SODIMMB_SCL 29A6
=I2C_SODIMMB_SDA 29A6

AIRPORT
J5300

=SMB_AIRPORT_CLK 43B4
=SMB_AIRPORT_DATA 43B4

GEYSER
J4900

=SMB_GEYSER_CLK 40C4
=SMB_GEYSER_DATA 40C4

SMC "0" SMBus Connections

64A6 =PP3V3_S0_SMBUS_SMC_0

SMC
U5800
(MASTER)

45C8 SMB_0_CLK — SMBUS_SMC_0_SCL (MAKE_BASE=TRUE)
45C5 SMB_0_DATA — SMBUS_SMC_0_SDA (MAKE_BASE=TRUE)

R2750 2.0K 5% 1/16W MF-LF 402 — R2751 2.0K 5% 1/16W MF-LF 402

SKIN TEMP
MAX6695: U6250

THRM_DIMM1_SMB_CLK 49B4
THRM_DIMM1_SMB_DATA 49B4

SMC "MLB" SMBus Connections

64A6 =PP3V3_S0_SMBUS_SMC_MLB

SMC
U5800
(MASTER)

45B5 SMB_MLB_CLK — 5B2 SMBUS_SMC_MLB_SCL (MAKE_BASE=TRUE)
45B5 SMB_MLB_DATA — 5B2 SMBUS_SMC_MLB_SDA (MAKE_BASE=TRUE)

R2760 2.0K 5% 1/16W MF-LF 402 — R2761 2.0K 5% 1/16W MF-LF 402

CPU Temp
ADT7461: U1001
(Write: 0x98 Read: 0x99)

SMB_THRM_CLK 10B3
SMB_THRM_DATA 10B3

Top-Case
U6200
(SEE TABLE)

THRM_DIMM0_SMB_CLK 49C4
THRM_DIMM0_SMB_DATA 49C4

SMC "RMT" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

64B3 =PP3V3_S3_SMBUS_SMC_RMT

SMC
U5800
(MASTER)

45B9 SMB_RMT_CLK — SMBUS_SMC_RMT_SCL (MAKE_BASE=TRUE)
45B9 SMB_RMT_DATA — SMBUS_SMC_RMT_SDA (MAKE_BASE=TRUE)

R2770 2.0K 5% 1/16W MF-LF 402 — R2771 2.0K 5% 1/16W MF-LF 402

Top-Case SMBus Connections:

AMBIENT THERMAL
ATS/ALS

=SMBUS_ATS_SCL 67A2
=SMBUS_ATS_SDA 67A2

SMC "Battery A" SMBus Connections

64D1 =PP3V42_G3H_SMBUS_SMC_BSA

SMC
U5800
(MASTER)

45B9 SMB_BSA_CLK — SMBUS_SMC_BSA_SCL (MAKE_BASE=TRUE)
45B9 SMB_BSA_DATA — SMBUS_SMC_BSA_SDA (MAKE_BASE=TRUE)

R2780 8.2K 5% 1/16W MF-LF 402 — R2781 8.2K 5% 1/16W MF-LF 402

Battery
J8250

=SMBUS_BATT_SCL 65A2
=SMBUS_BATT_SDA 65A2

SMC "Battery B" SMBus Connections

=PP3V3_S0_SMBUS_SMC_BSB 64A6

SMC
U5800
(MASTER)

45C5 SMB_BSB_CLK
45C8 SMB_BSB_DATA

R2782 100K 5% 1/16W MF-LF 402 — R2783 100K 5% 1/16W MF-LF 402

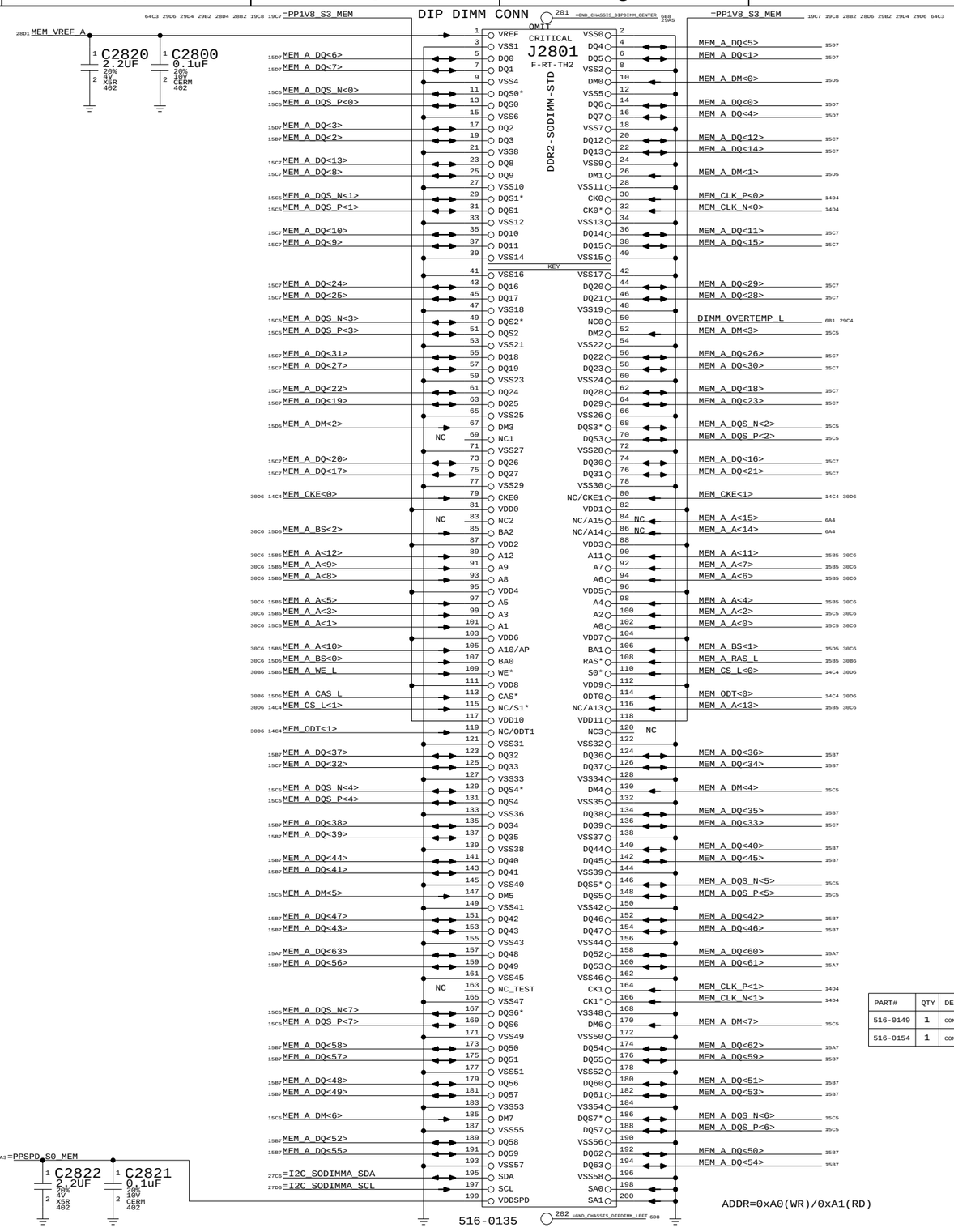
M42 SMBUS CONNECTIONS

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE INC.

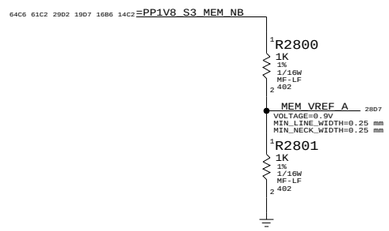
SIZE D | DRAWING NUMBER 051-7370 | REV. C

SCALE NONE | SHT 27 OF 98



DDR2 VRef

One 0.1uF per connector



Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

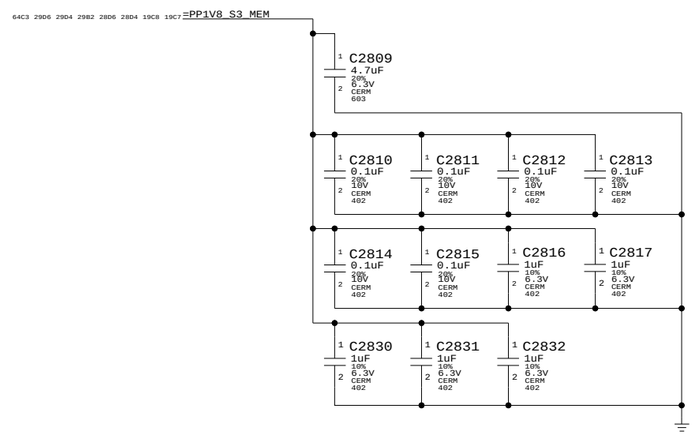
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

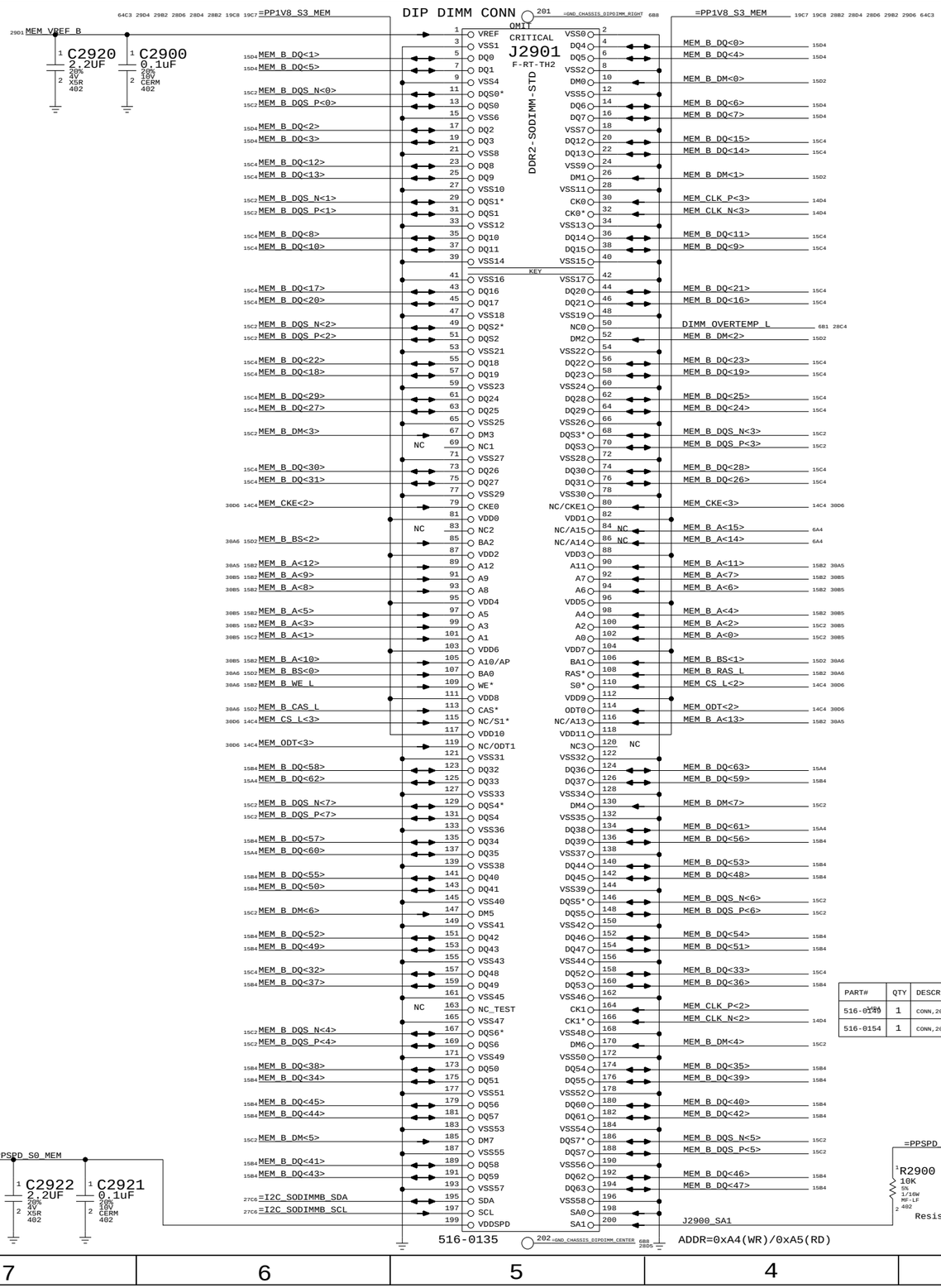
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2801	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2801	CRITICAL	POST-RAMP-DIMM35

DDR2 SO-DIMM Connector A

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

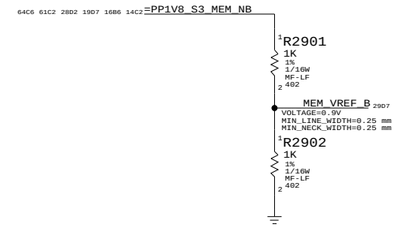
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 28 OF 98	



DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector



Yellow uses 10K divider and TLV2463
to drive MCH and DIMM connectors.
(See Capell Valley pg 47)

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

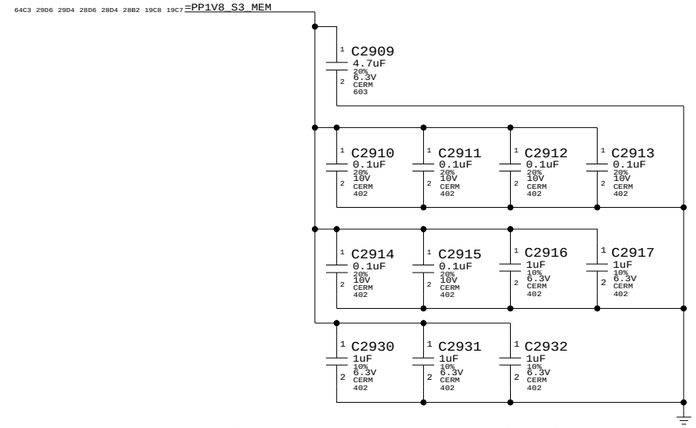
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

DDR2 Bypass Caps

(For return current)



The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps,
when they get cheaper.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0149	1	CONN,200P STD SODIMM OLD REV	J2901	CRITICAL	PVT-DIMM
516-0154	1	CONN,200P STD SODIMM NEW REV 3.5	J2901	CRITICAL	POST-RAMP-DIMM35

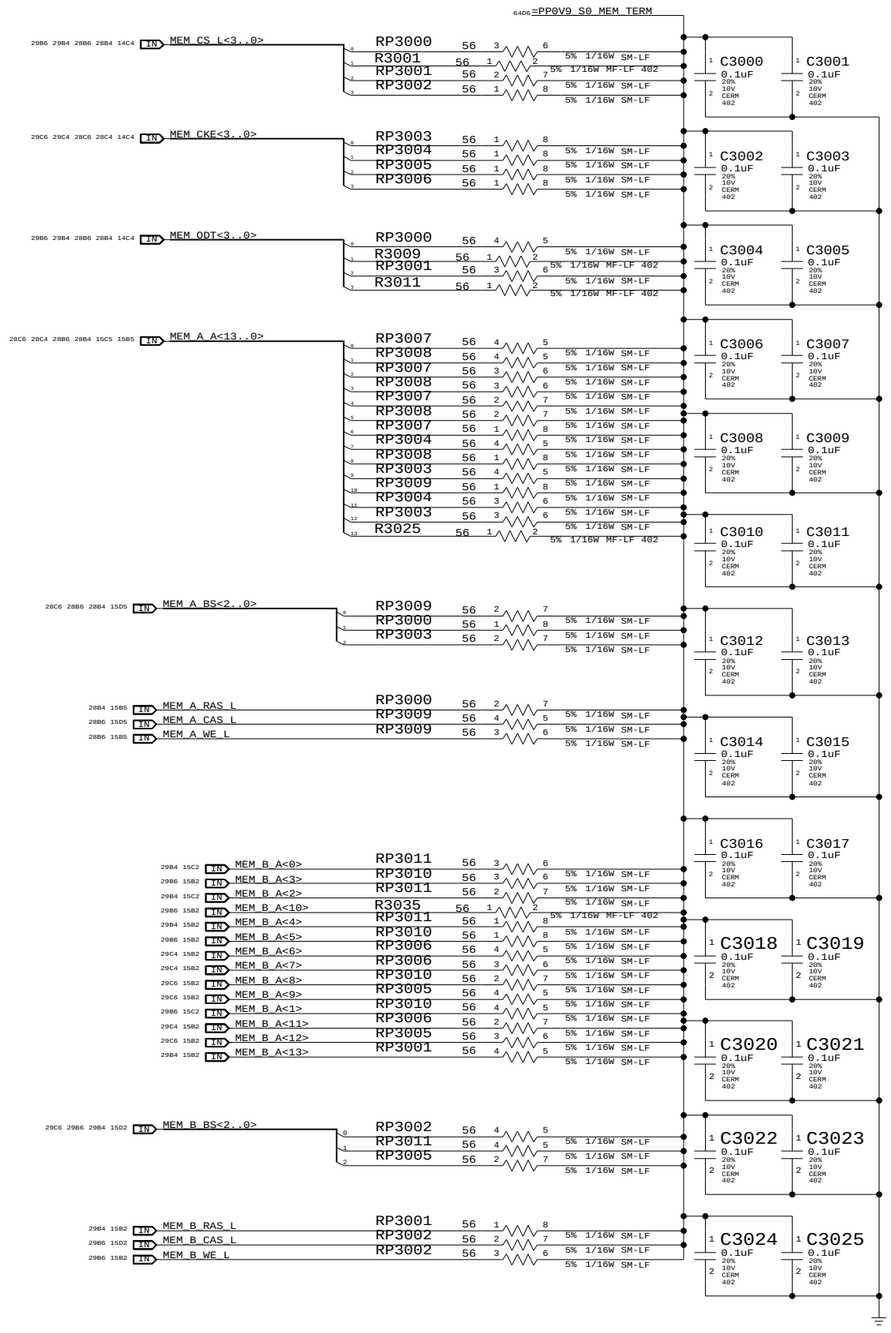
DDR2 SO-DIMM Connector B

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 29 OF 98	

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	30	98

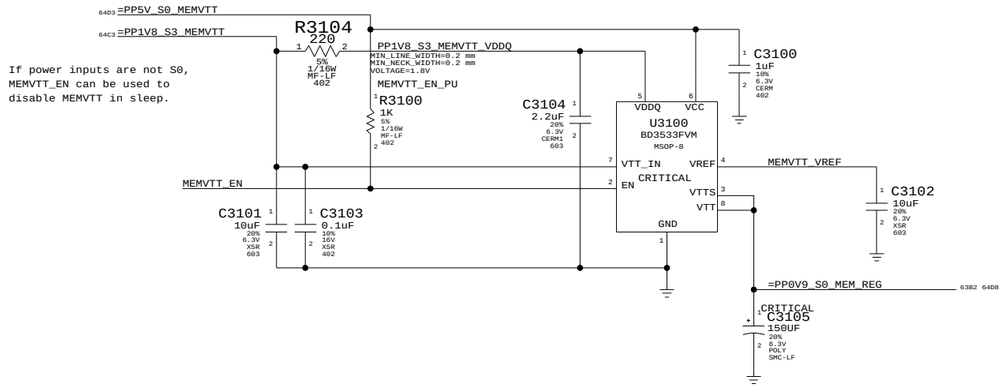
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



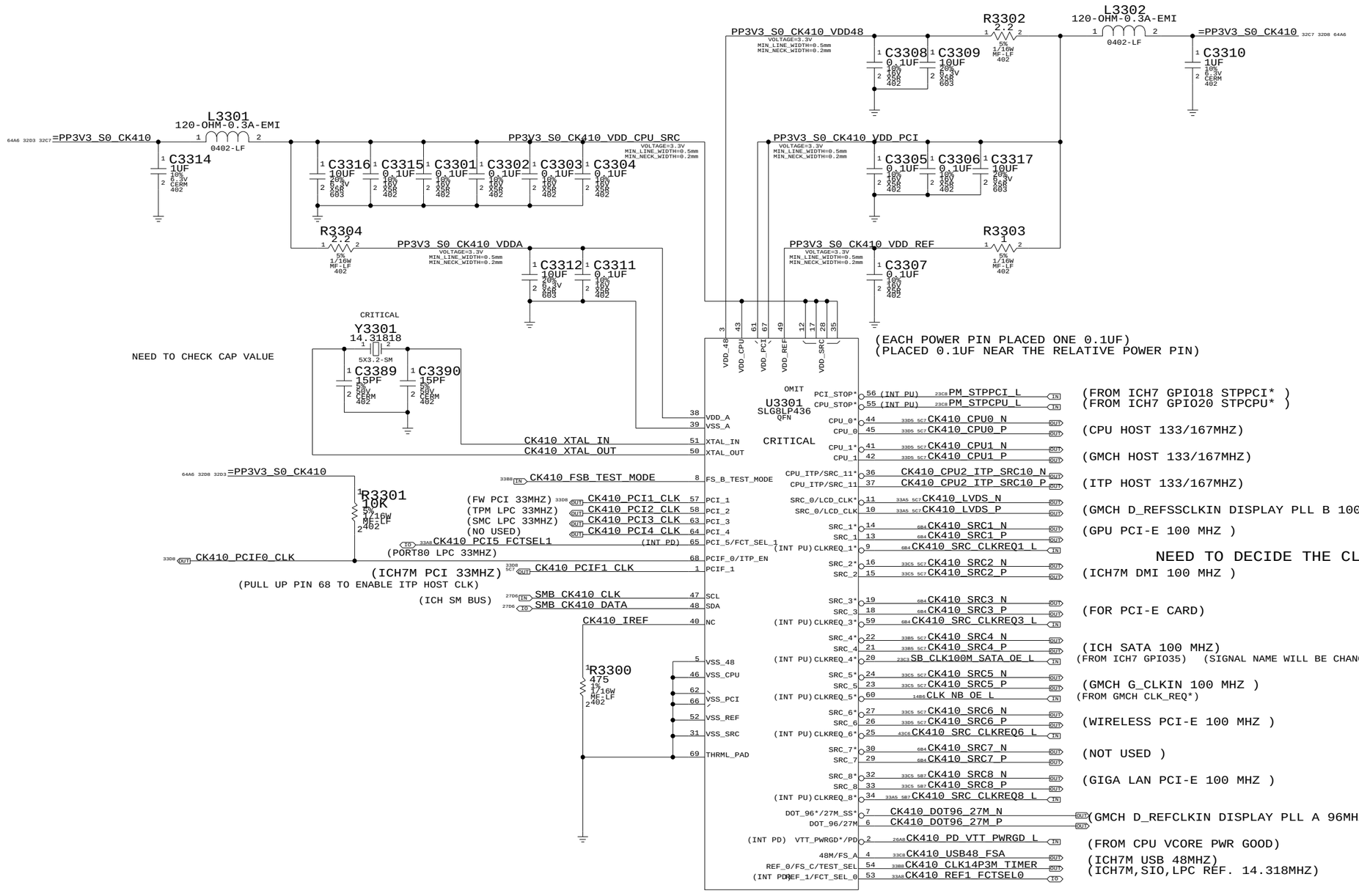
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	31	98



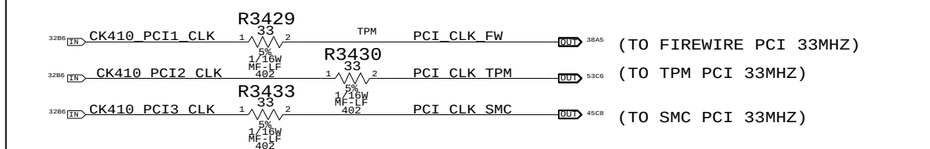
FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

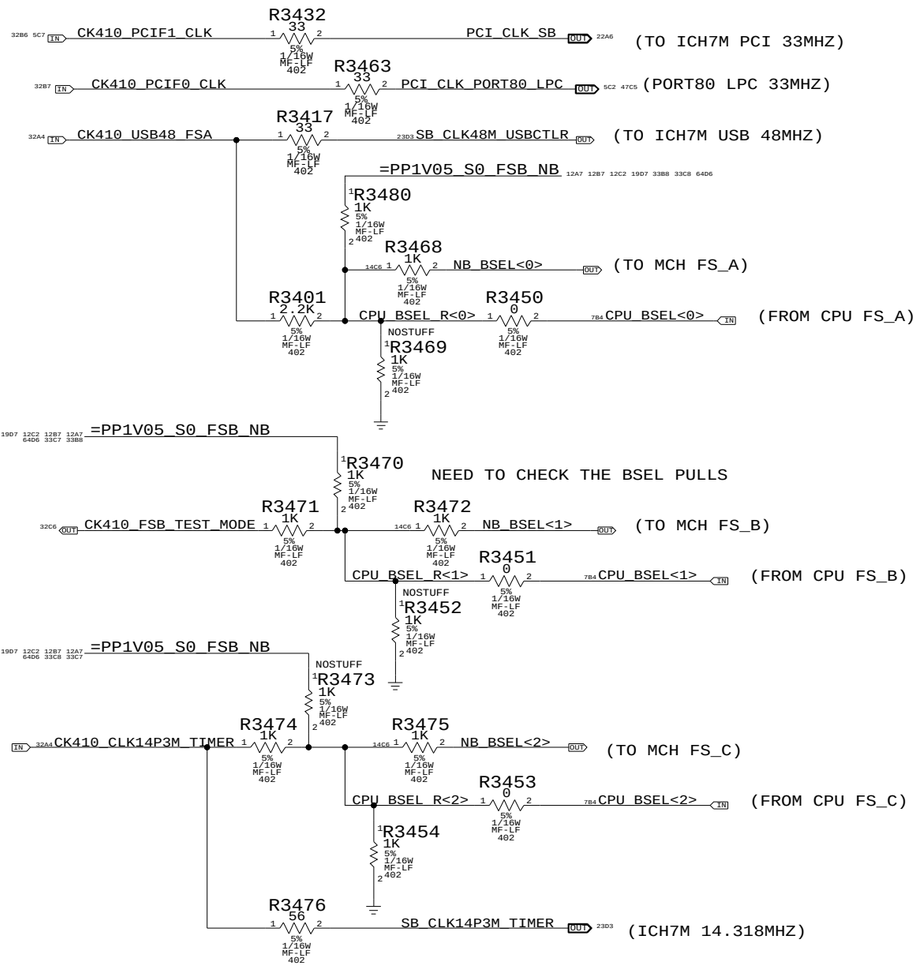
CLOCKS

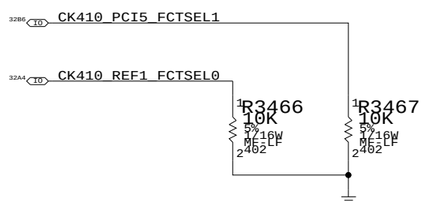
SYNC_MASTER=CLOCK SYNC_DATE=06/03/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 33 OF 98	





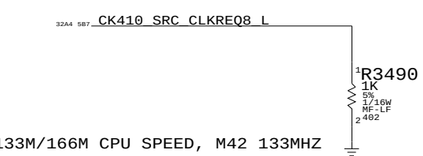


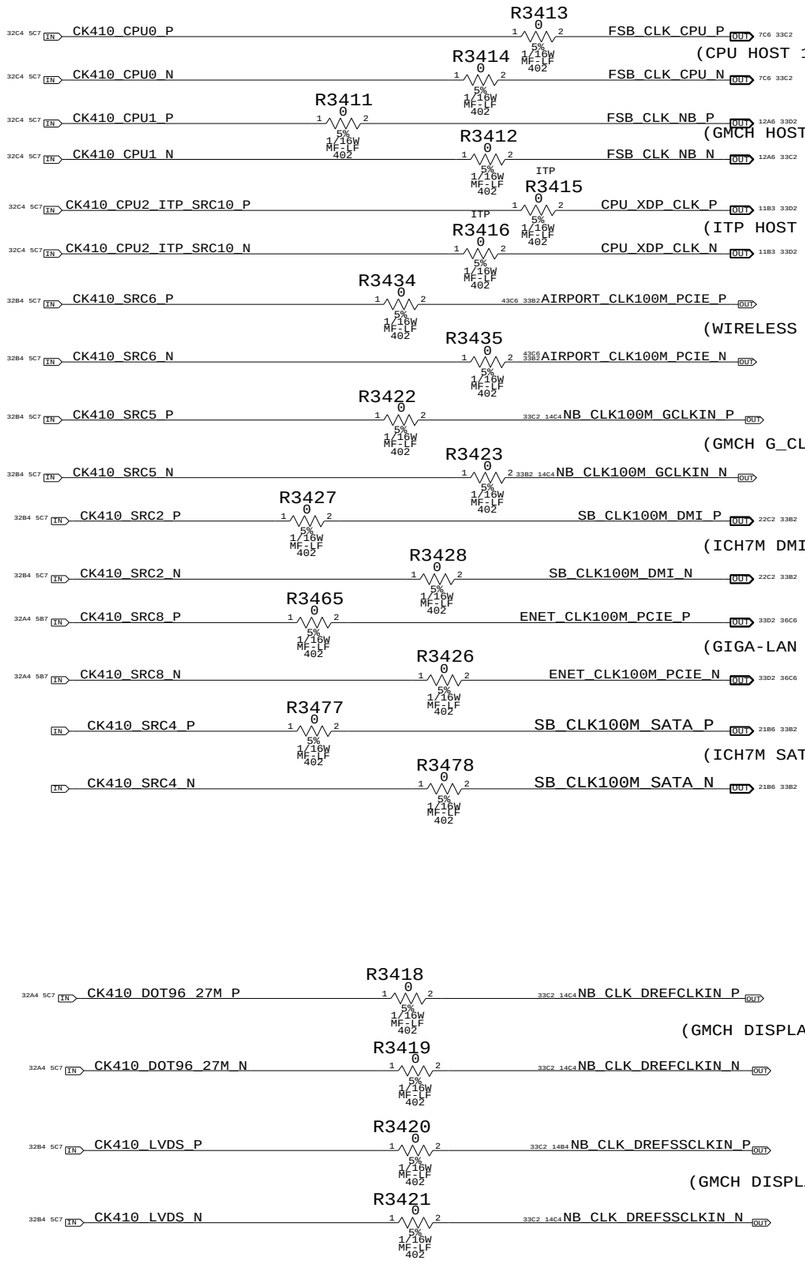
SET FCTSEL0,FCTSEL1 TO 00
EVEN THESE TWO PINS INTERNAL PULL DOWN,
CYPRESS RECOMMAND TO ADD EXTERNAL PULLS,

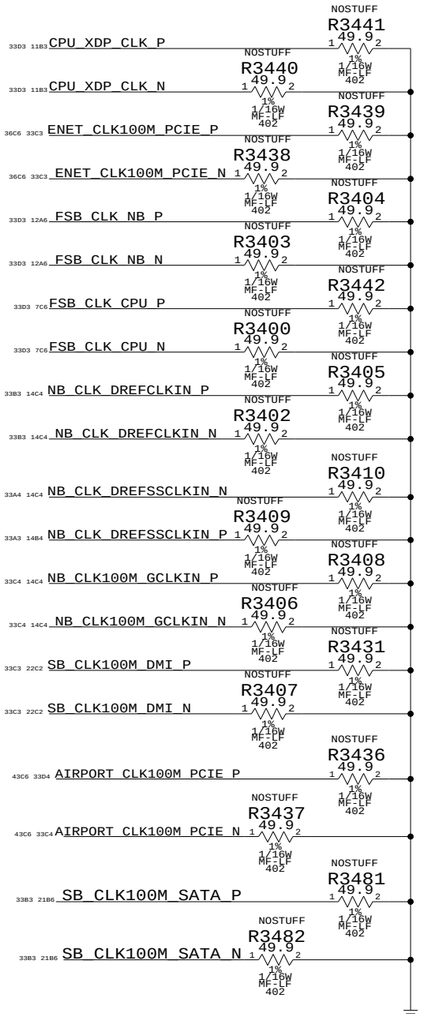
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	1	0	1	100M
	0	0	1	133M
#	0	1	1	166M
	0	1	0	200M

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED, M42 133MHZ







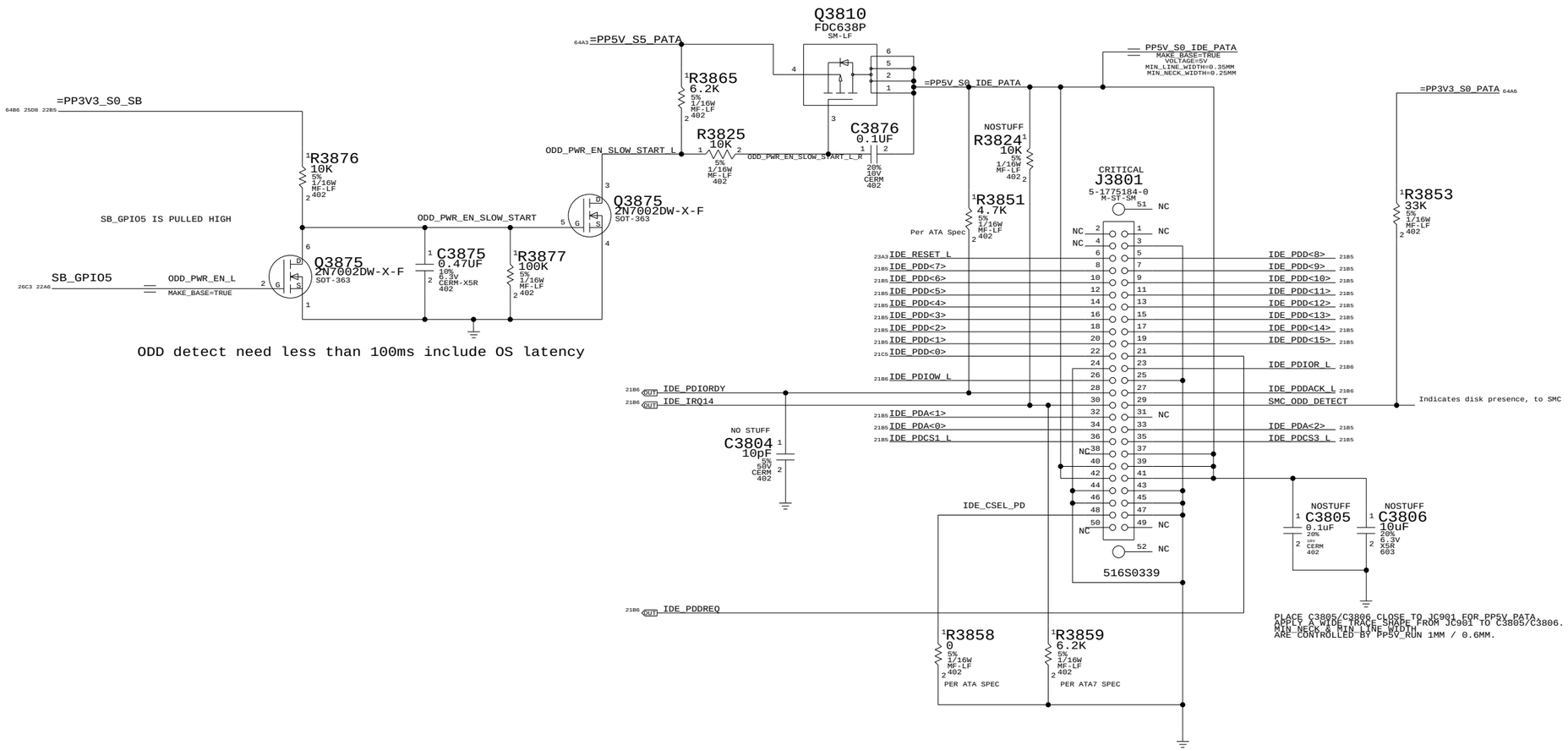
CLOCK TERMINATION

SYNC_MASTER=CLOCK SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	34	98

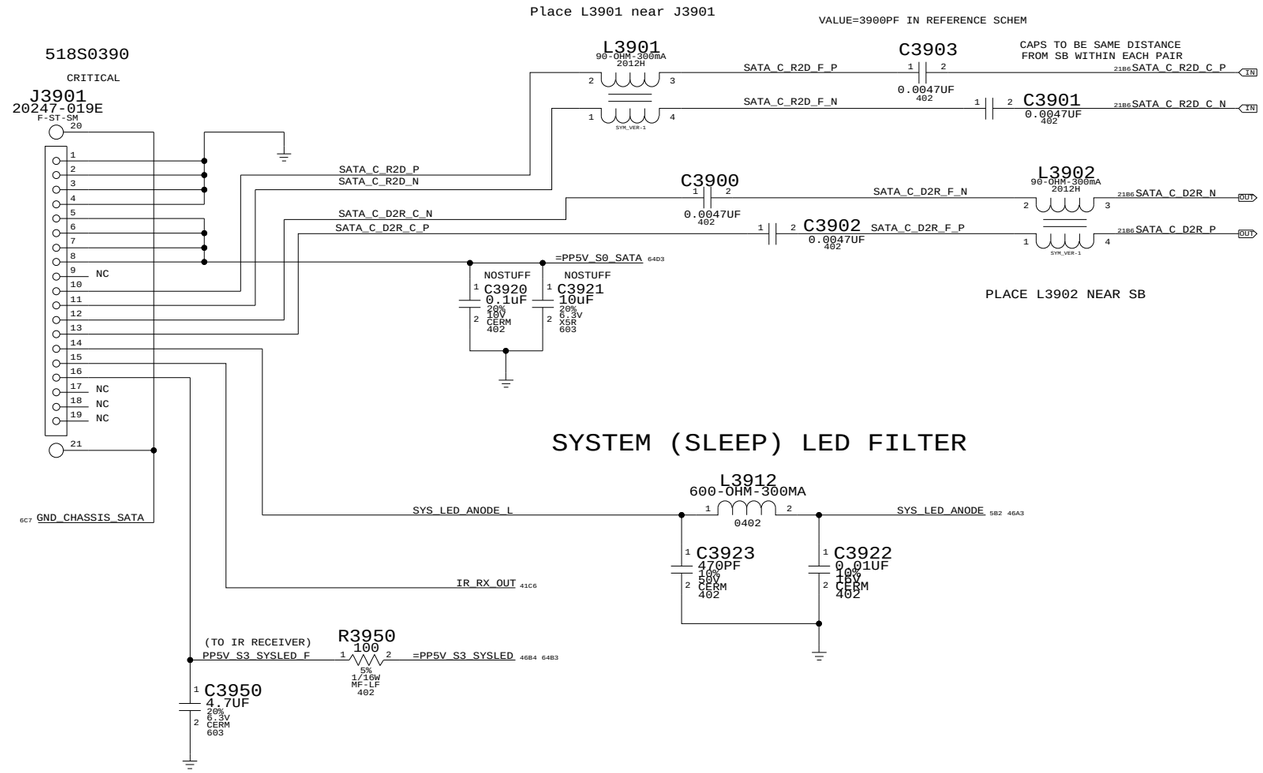


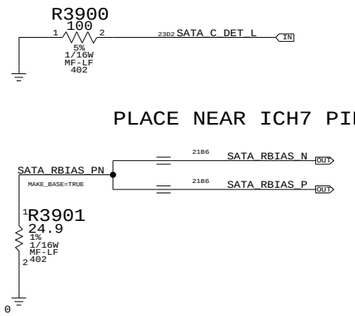
PATA CONNECTOR

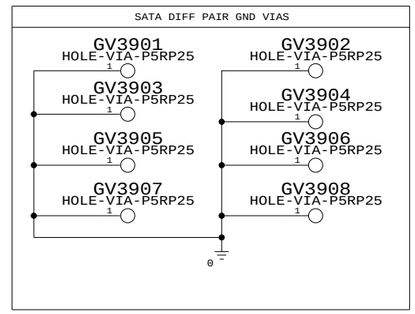
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 38 OF 98	

SATA CONNECTOR







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L3901,L3902	KEEP MAG.LAYER IN BOM

SATA CONNECTOR

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 39 OF 98	

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

37D8 PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402-LF
=PP2V5_S3_ENET 64C3

PLACE C4107 NEAR U4101 AVDD

36C8 36B5 36B4 36A5 64B3 36D6 =PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402
=PP1V2_S3_ENET 36A8 64C3
=PP3V3_S3_ENET 36D8 64B3 36A5 36B4 36B5 36C8

NOSTUFF R4107 0 5% 1/16W MF-LF 402
22C4 22D8 SB_GPIO30
ENET_LOM_DIS_L

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF X5R 10% 16V 402
C4113 0.1UF 402 X5R 16V 10%

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

PCIE_A_D2R_C_P
PCIE_A_D2R_C_N
22D4 PCIE_A_D2R_P OUT
22D4 PCIE_A_D2R_N OUT

PCIE_A_R2D_P
PCIE_A_R2D_N
22D4 PCIE_A_R2D_C_P IN
22D4 PCIE_A_R2D_C_N IN

OMIT
CRITICAL
U4101
88E8053
QFN

VDD7	58		
VDD6	48		
VDD5	44		
VDD4	39		
VDD3	33		
VDD2	13		
VDD1	7		
VDD0	2		
VDDO_TTL4	61		
VDDO_TTL3	45		
VDDO_TTL2	40		
VDDO_TTL1	8		
VDDO_TTL0	1		
AVDD	23		
AVDDL6	57		
AVDDL5	52		
AVDDL4	51		
AVDDL3	32		
AVDDL2	28		
AVDDL1	22		
AVDDL0	19		
VDD25	64		
LOM_DISABLE*	10		
VAUX_AVLBL	12		
VMAIN_AVLBL	47		
SWITCH_VCC	11	NC	
SWITCH_VAUX	9	NC	
HSDACP	24	NC	
HSDACN	25	NC	
CTRL25	4		ENET_CTRL25 6A4 OUT
CTRL12	3		ENET_CTRL12 6A4 OUT
RSET	16		ENET_RSET
LED_ACT*	59	NC	
LED_LINK10/100*	60	NC	
LED_LINK1000*	62	NC	
LINK*	63	NC	
TSTPT	29		
TESTMODE	46		
TX_P	49		
TX_N	50		
RX_P	54		
RX_N	53		
REFCLKP	55		33D2 33C3 ENET_CLK100M_PCIE_P IN
REFCLKN	56		33D2 33C3 ENET_CLK100M_PCIE_N IN
WAKE*	6		43C6 23C8 PCIE_WAKE_L OUT
PERST*	5		26A1 ENET_RST_L IN
MDIP0	17		
MDIN0	18		
MDIP1	20		
MDIN1	21		
MDIP2	26		
MDIN2	27		
MDIP3	30		
MDIN3	31		
VPD_CLK	38		ENET_VPD_CLK 36A2
VPD_DATA	41		ENET_VPD_DATA 36A2
PU_VDDO_TTL0	42		ENET_PU_VDD_TTL0 36A6
PU_VDDO_TTL1	43		ENET_PU_VDD_TTL1 36A6
SPI_DI	35	NC	
SPI_DO	34	NC	
SPI_CLK	37	NC	
SPI_CS	36	NC	
XTALI	15		ENET_XTALI
XTALO	14		ENET_XTALO
THRML_PAD	65		

ANALOG
PCI EXPRESS
LED
MEDIA
TEST
TWSI
TEST
SPI
MAIN CLK

OPTIONAL EXTERNAL LDO
NO PULL-UP NEEDED

R4102 4.75K 1% 1/16W MF-LF 402

ASF IS UNAVAILABLE ON 80S3
INTERNAL PULL-UP

CRITICAL
Y4101 25.0000M SM-3.2X2.5MM
NC NC
C4150 15PF 5% 50V CERM 402
C4151 15PF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

R4106 49.9 1% 1/16W MF-LF 402 ENET_MDI0
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402 ENET_MDI1
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402 ENET_MDI2
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402 ENET_MDI3
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI_P<0> 37C8 IO
ENET_MDI_N<0> 37C8 IO
ENET_MDI_P<1> 37B8 IO
ENET_MDI_N<1> 37B8 IO
ENET_MDI_P<2> 37B8 IO
ENET_MDI_N<2> 37B8 IO
ENET_MDI_P<3> 37B8 IO
ENET_MDI_N<3> 37B8 IO

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

64B3 36D8 36D6 36C8 36B5 36A5 =PP3V3_S3_ENET

PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL
U4102
M24C08 SO8

E2	3	
NC1	2	
NC0	1	
WC*	7	
VCC	8	
SDA	5	ENET_VPD_DATA 36C6
SCL	6	ENET_VPD_CLK 36C6
VSS	4	

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

NOSTUFF R4124 0 5% 1/16W MF-LF 402

=PP3V3_S3_ENET 36A5 36B4 36C8 36D6 36D8 64B3

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

36C6 ENET_PU_VDD_TTL0
36B6 ENET_PU_VDD_TTL1

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

64C3 36D7 =PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

64B3 36D8 36D6 36C8 36B5 36B4 =PP3V3_S3_ENET

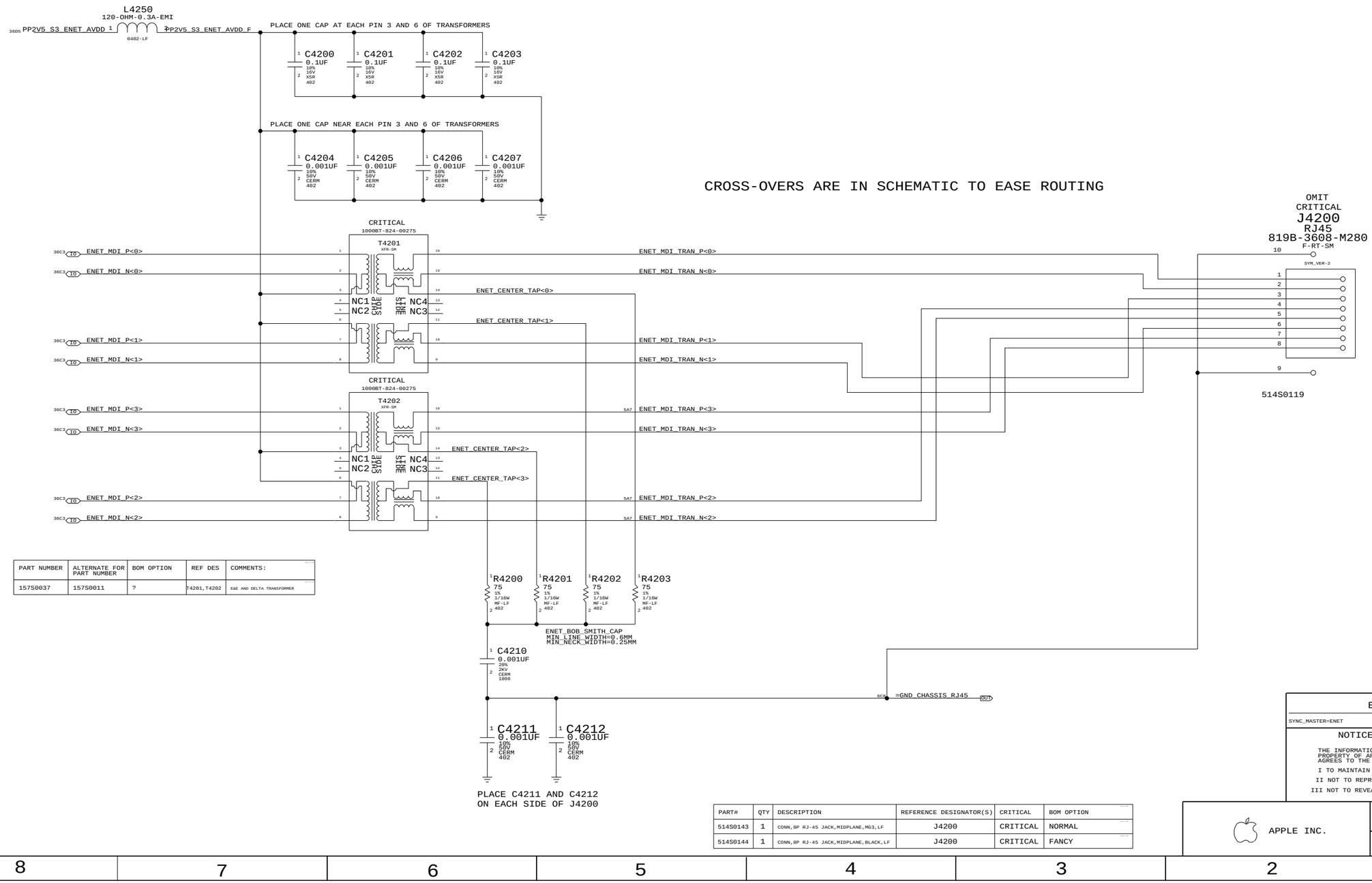
C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=ENET
SYNC_DATE=12/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	41	98



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0037	157S0011	?	T4201,T4202	E&E AND DELTA TRANSFORMER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0143	1	CONN,8P RJ-45 JACK,MIDPLANE,MG3,LF	J4200	CRITICAL	NORMAL
514S0144	1	CONN,8P RJ-45 JACK,MIDPLANE,BLACK,LF	J4200	CRITICAL	FANCY

ETHERNET CONNECTOR

SYNC_MASTER=ENET SYNC_DATE=11/14/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 42 OF 98	

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD19 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510R PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME_DIFF_PAIR NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PCB CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

64B3 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 10V CERM 402
C4422 0.1UF 10% 10V CERM 402
C4426 0.1UF 10% 10V CERM 402
C4428 0.1UF 10% 10V CERM 402
C4430 0.1UF 10% 10V CERM 402
C4432 0.1UF 10% 10V CERM 402

L4400 600-OHM-300MA 0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 10V X5R 402
C4429 0.1UF 10% 10V X5R 402
C4425 0.1UF 10% 10V X5R 402

64B3 =PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

OMIT
CRITICAL
U4400
FW32306
BGA

G4	VDD0		
M1	VDD1		
M2	VDD2		
K5	VDD3		
K6	VDD4		
K7	VDD5		
L13	VDD6		
H13	VDD7		
A2	VDD9		
D10	VDDA0		
A13	VDDA1		
B13	VDDA2		
A7	VDDA3		
A8	VDDA4		
D6	VDDA5		
G13	PCI_VIOS		
F10	PCI_AD0	22B7	PCI_AD<0>
G10	PCI_AD1	22B7	PCI_AD<1>
H10	PCI_AD2	22B7	PCI_AD<2>
H12	PCI_AD3	22B7	PCI_AD<3>
J13	PCI_AD4	22B7	PCI_AD<4>
J12	PCI_AD5	22B7	PCI_AD<5>
K13	PCI_AD6	22B7	PCI_AD<6>
K10	PCI_AD7	22B7	PCI_AD<7>
L12	PCI_AD8	22B7	PCI_AD<8>
M13	PCI_AD9	22B7	PCI_AD<9>
L11	PCI_AD10	22B7	PCI_AD<10>
M12	PCI_AD11	22B7	PCI_AD<11>
M11	PCI_AD12	22B7	PCI_AD<12>
N12	PCI_AD13	22B7	PCI_AD<13>
M10	PCI_AD14	22B7	PCI_AD<14>
N11	PCI_AD15	22B7	PCI_AD<15>
M4	PCI_AD16	22B7	PCI_AD<16>
N5	PCI_AD17	22B7	PCI_AD<17>
N4	PCI_AD18	22B7	PCI_AD<18>
M3	PCI_AD19	22A7	PCI_AD<19>
M2	PCI_AD20	22A7	PCI_AD<20>
N3	PCI_AD21	22A7	PCI_AD<21>
K4	PCI_AD22	22A7	PCI_AD<22>
M1	PCI_AD23	22A7	PCI_AD<23>
K2	PCI_AD24	22A7	PCI_AD<24>
J4	PCI_AD25	22A7	PCI_AD<25>
K1	PCI_AD26	22A7	PCI_AD<26>
J2	PCI_AD27	22A7	PCI_AD<27>
J1	PCI_AD28	22A7	PCI_AD<28>
H2	PCI_AD29	22A7	PCI_AD<29>
H4	PCI_AD30	22A7	PCI_AD<30>
H1	PCI_AD31	22A7	PCI_AD<31>
K12	PCI_CBE0*	22B6	PCI_C_BE_L<0>
M9	PCI_CBE1*	22B6	PCI_C_BE_L<1>
L3	PCI_CBE2*	22B6	PCI_C_BE_L<2>
L1	PCI_CBE3*	22B6	PCI_C_BE_L<3>
N10	PCI_PAR	22A6	PCI_PAR
N6	PCI_FRAME*	26C3 22A7	PCI_FRAME_L
M6	PCI_IRDY*	26C3 22A6	PCI_IRDY_L
N7	PCI_TRDY*	26C3 22A6	PCI_TRDY_L
N8	PCI_DEVSEL*	26C3 22A6	PCI_DEVSEL_L
M7	PCI_STOP*	26C3 22A6	PCI_STOP_L
L2	PCI_IDSEL		FW_PCI_IDSEL
E2	PCI_REQ*	26C3 22B6	PCI_REQ3_L
E1	PCI_GNT*	22B6	PCI_GNT3_L
M8	PCI_PERR*	26C3 22A6	PCI_PERR_L
N9	PCI_SERR*	26C3 22A6	PCI_SERR_L
G2	PCI_CLK	33D6	PCI_CLK_FW
D1	CLKRUN*		PM_CLKRUN_L
F1	PCI_RST*		FW_PCI_RST_L
D2	PCI_INTA*	26C3	INT_PIRQD_L
F2	PCI_PME*	22B6	PCI_PME_FW_L

R4431 22 5% 1/16W MF-LF 402

R4432 100 1% 1/16W MF-LF 402

THIS IS FROM ICH-7M

PLACE R4432 VERY CLOSE TO PIN B18 OF U2100

197S0030 3.2MMX2.5MM
CRITICAL
Y4403 SM-3.2X2.5MM 24.576MHZ

R4400 390 5% 1/16W MF-LF 402
C4411 15PF 5% 50V C0G 402
C4412 15PF 5% 50V C0G 402

NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5		FW_XI
XO	B5		FW_XO
RESET*	B4		FW_PWRON_RST_L
R1	A6		FW_R1
R0	B7		FW_R0
TPBIAS0	B8	39B4	FW_A_TPBIAS
TPA0_P	A9	39B4	FW_A_TPA_P
TPA0_N	B9	39B4	FW_A_TPA_N
TPB0_P	B10	39B4	FW_A_TPB_P
TPB0_N	A10	39B4	FW_A_TPB_N
TPBIAS1	D8	6D2	FW_B_TPBIAS
TPA1_P	A11	6D2	FW_B_TPA_P
TPA1_N	B11	6D2	FW_B_TPA_N
TPB1_P	B12	6D2	FW_B_TPB_P
TPB1_N	A12	6D2	FW_B_TPB_N
TPBIAS2	C13	6D2	FW_C_TPBIAS
TPA2_P	C11	6D2	FW_C_TPA_P
TPA2_N	C12	6D2	FW_C_TPA_N
TPB2_P	D13	6D2	FW_C_TPB_P
TPB2_N	D12	6D2	FW_C_TPB_N

R4452 2.1K 1% 1/16W MF-LF 402
C4420 0.1UF 10% 10V X5R 402
R4420 510K 5% 1/10W MF-LF 402

SPEC RECOMMENDS 2.49K

MODE_420	M5		MODE FOR EXTERNAL LINK
MODE_A	B6		
PC0	E12	39C4	FW_PC0
PC1	F13		
PC2	F12		
CONTENDER	G12		LOW = NOT BUS MANAGER
CARDBUSN	B1		LOW = PCI OPERATION
MPCI_ACTN_323	E10		

DUAL PORT DEVICES ARE POWER CLASS 4 (’100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (’000’)

TEST0	C2	
TEST1	C1	
PTEST	A4	
SE	A3	
SM	B3	

MANUFACTURING TEST PINS

VSS0	A1		
VSS1	B2		
VSS2	C3		
VSS3	D4		
VSS4	E4		
VSS5	E5		
VSS6	F4		
VSS7	F6		
VSS8	F7		
VSS9	F8		
VSS10	G1		
VSS11	G6		
VSS12	G7		
VSS13	G8		
VSS14	H6		
VSS15	H7		
VSS16	H8		
VSS17	J5		
VSS18	J9		
VSS19	J10		
VSS20	K8		
VSS21	K9		
VSS22	N13		
VSSA0	E13		
VSSA1	E9		
VSSA2	D9		
VSSA3	D7		
VSSA4	D5		

FIREWIRE CONTROLLER

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 44 OF 98	

Page Notes

INPUT:

=PPBUS_FW - PORT POWER

=PP3V3_S5_FW - DIGITAL POWER

=GND_CHASSIS_FW_PORT0 - CHASSIS GROUND

=FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:

FW_TPA0_P/N,FW_TPB0_P/N,FW_TPBIAS0 - FIREWIRE DIFF PAIRS

OUTPUT:

FW_PC0 - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

PAGE HISTORY

5/19/05 - INITIAL REVISION
6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
6/22/05 - CONNECTED FW_PC0 FOR SINGLE PORT
7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1
7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
7/26/05 - SWITCHED TO 514-0124 FOR PRE-PROTO CONNECTOR
7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
7/26/05 - CHANGED FL4590 TO 1.1A VERSION
7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple
FireWire Design Guide (FWDG 0.6, 5/14/03)

PORT POWER CLASS

0 FOR SINGLE PORT
1 FOR DUAL PORT

38A3 OUT FW_PC0

PPBUS_S5_FWPWRSW_F
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

64C1 =PPBUS_S5_FWPWRSW

FL4590
1.1A-24V
MINISMDC

Q4590
FDC638P
SM-LF

PPFW_SWITCH 58Z
VOLTAGE=18V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

D4590
SMB
B340LBXF

64A6 =PP3V3_S0_FW

R4590 470K 5% 1/16W MF-LF 402
C4590 0.01uF 10% 16V CERM 402

FWPWR_EN_L_DIV
MIN_LINE_WIDTH=0.05MM
MIN_NECK_WIDTH=0.05MM

R4593 100K 5% 1/16W MF-LF 402

R4591 330K 5% 1/16W MF-LF 402

IF =FWPWR_PWRON IS NC:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC
IF =FWPWR_PWRON LOW WHEN OFF:
ENABLES PORT POWER WHEN MACHINE IS RUNNING OR ON AC AND NOT SHUTDOWN

D4591 BAS16TW-X-F SOT-363

FWPWR_RUN

6D2 =FWPWR_PWRON

FWPWR_EN_L 60C8
MIN_LINE_WIDTH=0.05MM
MIN_NECK_WIDTH=0.05MM

Q4591
2N7002
SOT23-LF

FWPWR_EN

R4594 10K 5% 1/16W MF-LF 402

65C3 46B3 45D5 5C1 SMC_PS_ON

FWPWR_ACIN

R4595 470K 5% 1/16W MF-LF 402

Enables port power whenever
machine AC Adapter is plugged
or system at run state with battery only

Cable Power

PPFW_PORT0_VP_F
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

L4510
FERR-250-OHM
SM

PPFW_PORT0_VP
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C4510 0.001uF 10% 50V CERM 402

"Snapback" & "Late VG" Protection

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A 0.5V DROP

39A6 PP3V3_S5_FWLATEVG

3883 FW_A_TPBIAS

R4500 56.2 1% 1/16W MF-LF 402
R4501 56.2 1% 1/16W MF-LF 402
C4500 0.33UF 10% 6.3V CERM-X5R 402

3883 FW_A_TPA_P
3883 FW_A_TPA_N
3883 FW_A_TPB_P
3883 FW_A_TPB_N

R4502 56.2 1% 1/16W MF-LF 402
R4503 56.2 1% 1/16W MF-LF 402

FW_PORT0_TPB

C4501 220PF 5% 25V CERM 402

R4504 4.99K 1% 1/16W MF-LF 402

D4520 BAV99DW-X-F SOT-363
C4520 0.01UF 10% 16V CERM 402
C4521 0.01UF 10% 16V CERM 402

FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N

120-OHM 2012 SYM_VER-2
FL4520
FL4521

FW_PORT0_TPA_P_FL
FW_PORT0_TPA_N_FL
FW_PORT0_TPB_P_FL
FW_PORT0_TPB_N_FL

D4521 BAV99DW-X-F SOT-363
C4522 0.01UF 10% 16V CERM 402
C4523 0.01UF 10% 16V CERM 402

C4524 0.01uF 10% 50V X7R 603-1
C4525 0.01uF 10% 16V CERM 402

PORT 0
1394A
OMIT
CRITICAL
J4500
1394A
F-RT-TH1

TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP (PPFW_PORT0_VP)
VGND (GND_FW_PORT0_VGND)

=GND_CHASSIS_FW_UPPER 6A6
Plexi: 514-0124
Enclosure: 514-0289
=GND_CHASSIS_FW_DOWN 6C8

LATE-VG PROTECTION POWER

64A3 =PP3V3_S5_FWLATEVG

R4550 330 5% 1/16W MF-LF 402

PP3V3_S5_FWLATEVG_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM

L4550
400-OHM-EMI
SM-1

PP3V3_S5_FWLATEVG 39B5
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM

NO STUFF
C4551 0.1uF 20% 16V CERM 402

NO STUFF
C4552 0.001uF 10% 50V CERM 402

D4550
SOT23
MMBZ5227B

CAPS MAY NOT BE NECESSARY.
NO STUFF FOR NOW THOUGH

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0359	1	CONN,6P 1394A RCPT,MIDPLANE,MG3,LF	J4500	CRITICAL	NORMAL
514-0316	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK,LF	J4500	CRITICAL	FANCY

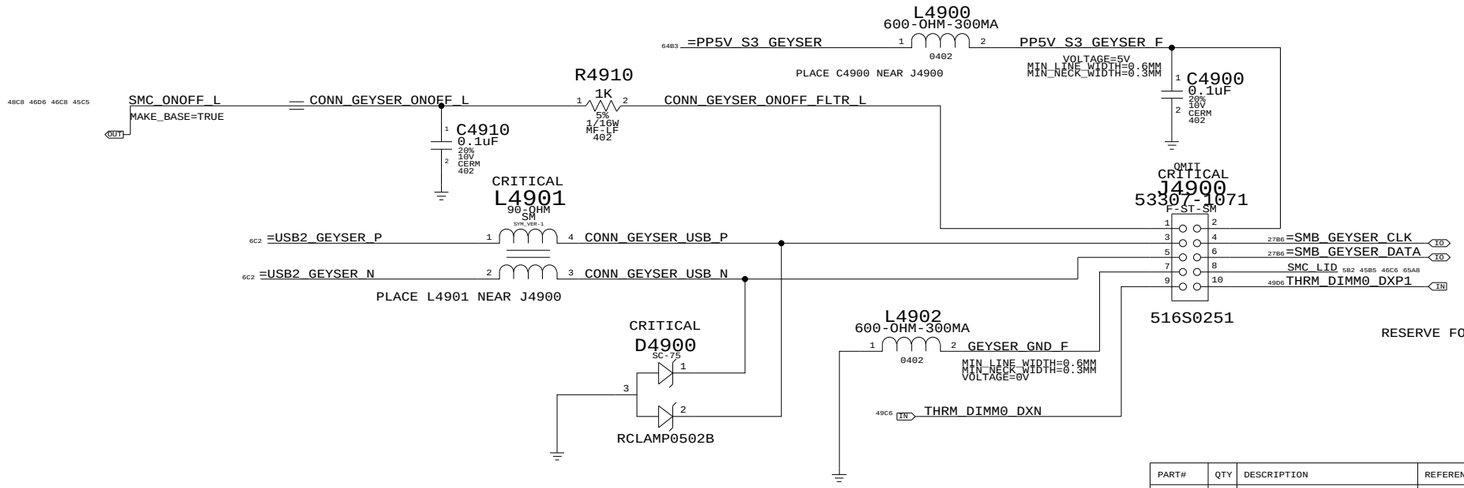
FIREWIRE PORT

SYNC_MASTER=ENET
SYNC_DATE=11/16/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 45 OF 98	

GEYSER AND DIMM0 REMOTE TEMP SENSORS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	NORMAL
516S0482	1	ACES 88646-1071-NS	J4900	CRITICAL	FANCY

CONNECTOR MISC

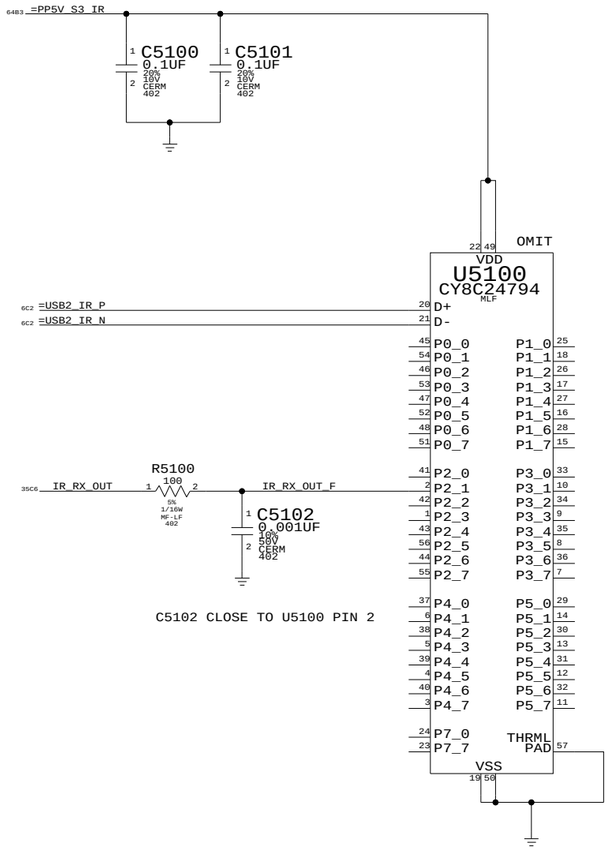
SYNC_MASTER=ENET SYNC_DATE=11/16/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	49	98

PLACE C5100 AND C5101
NEAR U5100 PIN 22 AND 49



C5102 CLOSE TO U5100 PIN 2

IR CONTROLLER

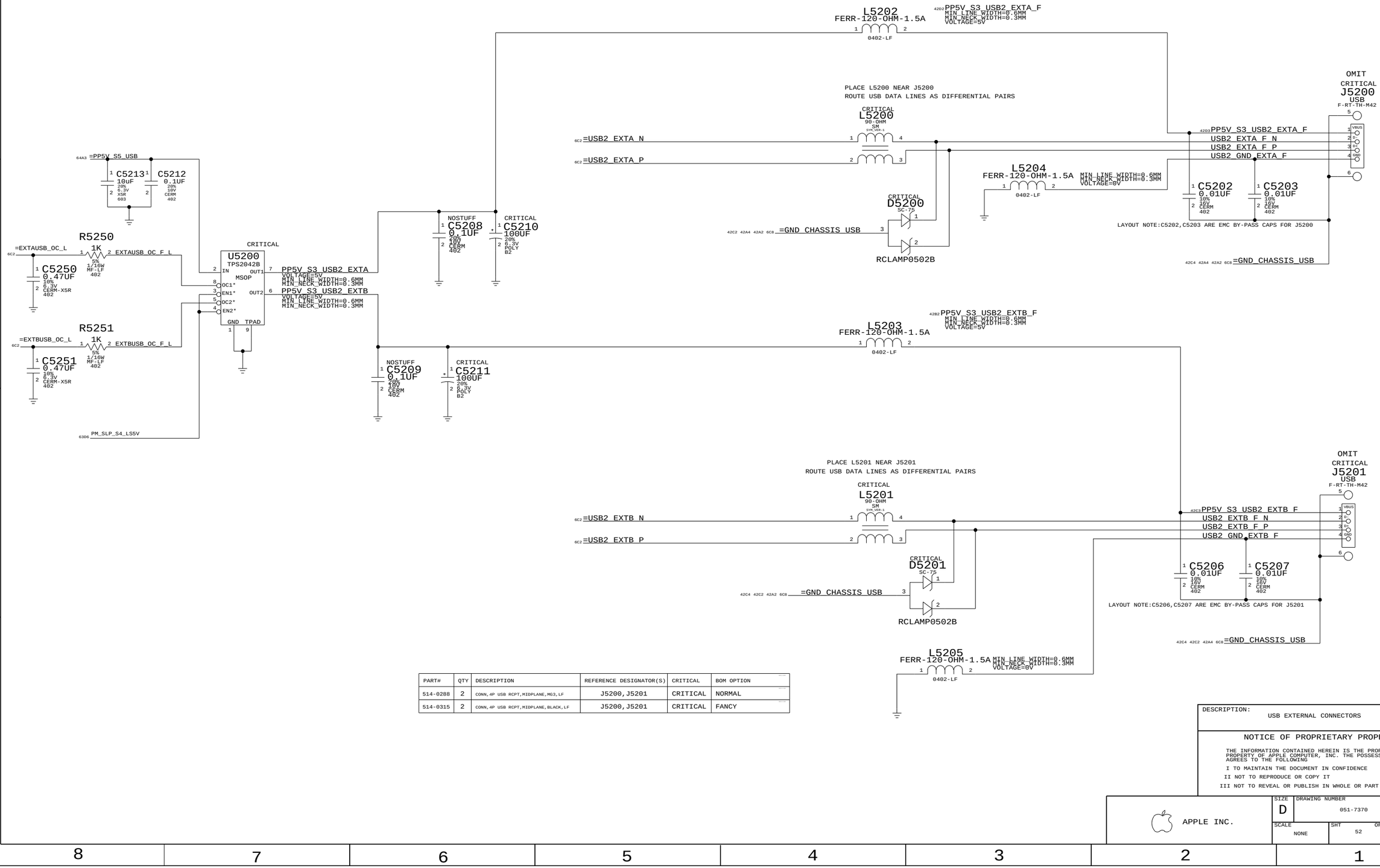
SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	51	98

USB 2.0 CONNECTORS

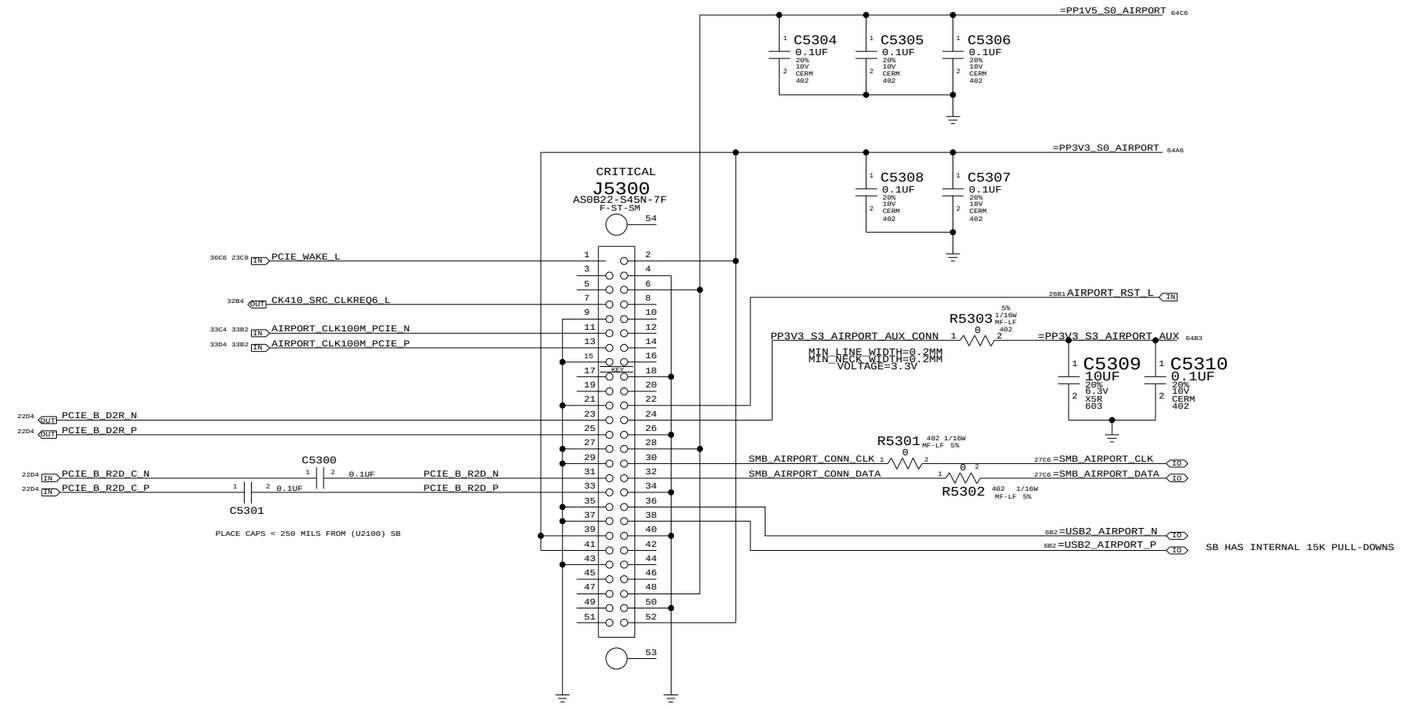


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0288	2	CONN,4P USB RCPT,MIDPLANE,MG3,LF	J5200,J5201	CRITICAL	NORMAL
514-0315	2	CONN,4P USB RCPT,MIDPLANE,BLACK,LF	J5200,J5201	CRITICAL	FANCY

DESCRIPTION:
USB EXTERNAL CONNECTORS

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 52 OF 98	



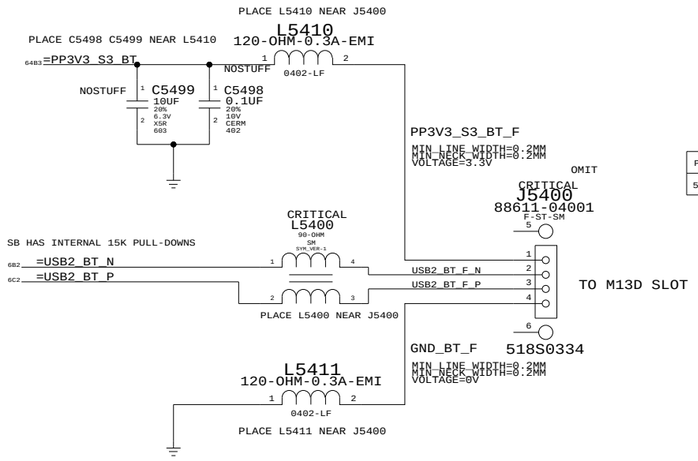
CONNECT TO M35 MODULE

Plexi: 516S0363
* Enclosure: 516S0406

AIRPORT CONN

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 53 OF 98	

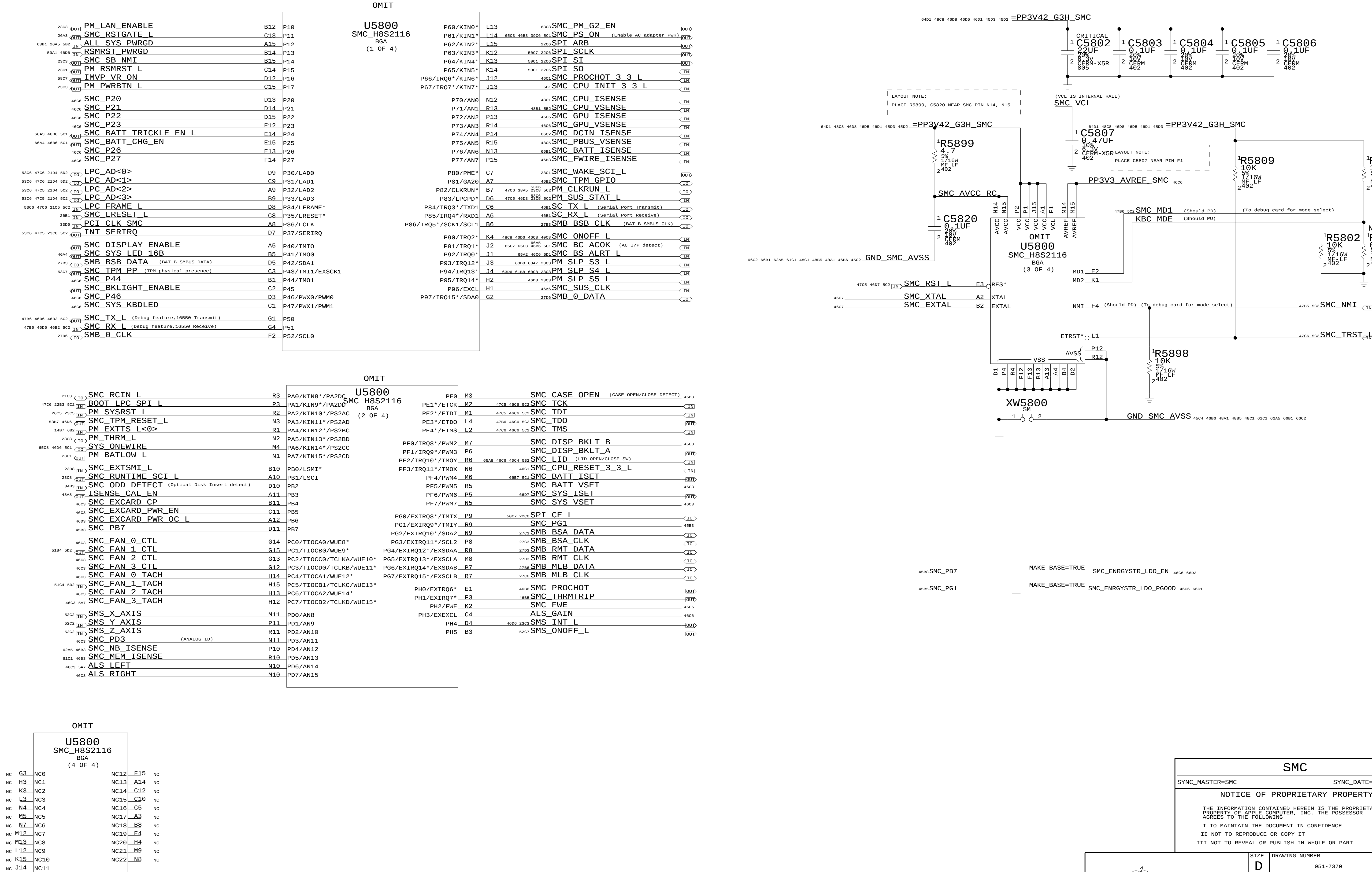


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J5400	CRITICAL	M42B

BLUETOOTH INTERFACE

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 54 OF 98	



SMC

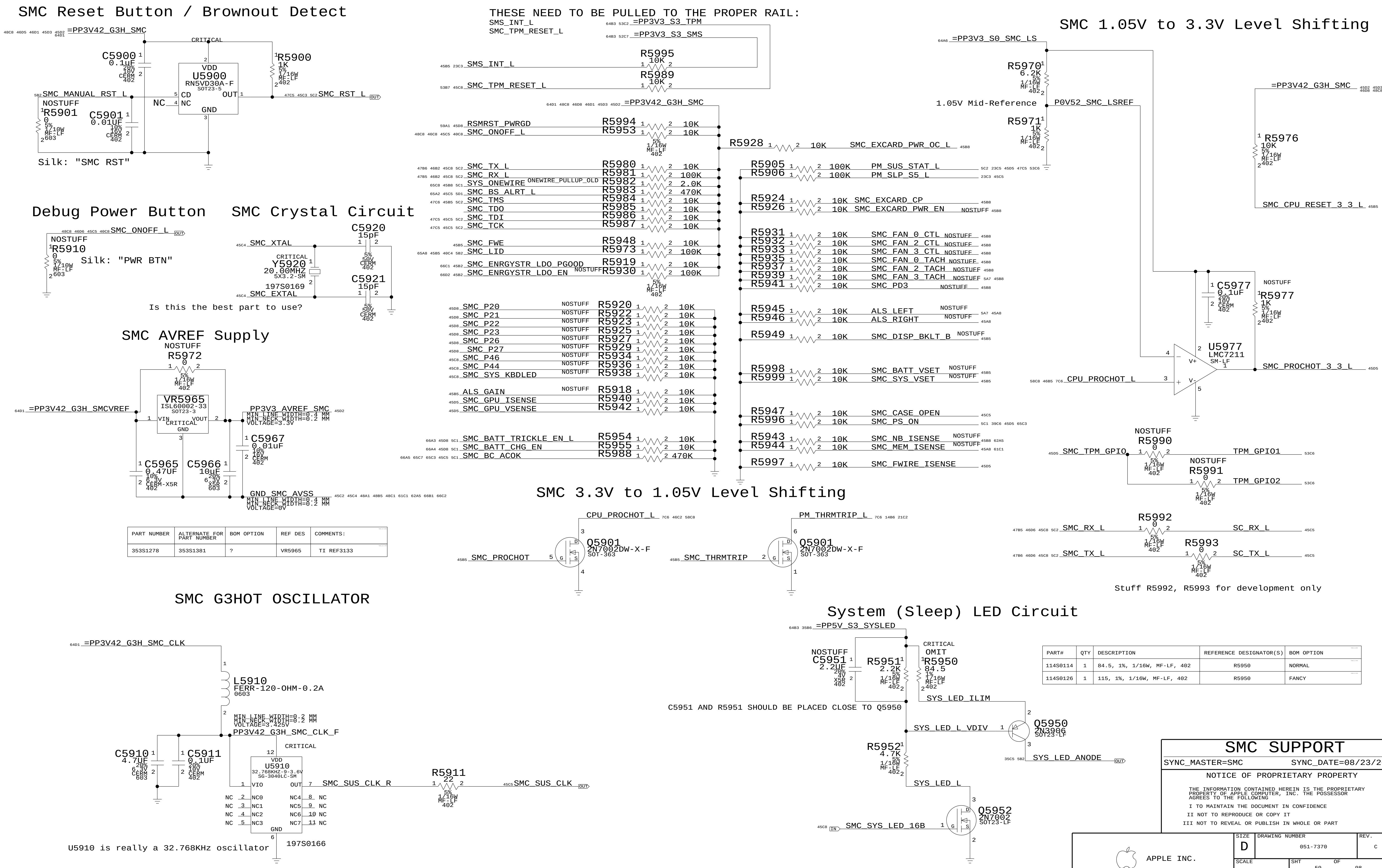
SYNC_MASTER=SMC SYNC_DATE=08/18/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	58	98


SMC Reset Button / Brownout Detect
=PP3V42_G3H_SMC
CRITICAL
C5900 0.1uF 20% 10V CERM 402
U5900 RN5VD30A-F SOT23-5
VDD CD NC OUT GND
R5900 1K 5% 1/16W MF-LF 402
SMC_MANUAL_RST_L
SMC_RST_L
NOSTUFF
R5901 0 5% 1/10W MF-LF 603
C5901 0.01UF 10% 16V CERM 402
NC
Silk: "SMC RST"
Debug Power Button
SMC_ONOFF_L
NOSTUFF
R5910 0 5% 1/10W MF-LF 603
Silk: "PWR BTN"
SMC Crystal Circuit
SMC_XTAL
SMC_EXTAL
C5920 15pF 5% 50V CERM 402
C5921 15pF 5% 50V CERM 402
CRITICAL
Y5920 20.00MHZ 5X3.2-SM
197S0169
Is this the best part to use?
SMC AVREF Supply
NOSTUFF
R5972 0 5% 1/16W MF-LF 402
=PP3V42_G3H_SMCVREF
VR5965 ISL60002-33 SOT23-3
VIN VOUT CRITICAL GND
PP3V3_AVREF_SMC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C5967 0.01uF 10% 16V CERM 402
C5965 0.47UF 10% 6.3V CERM-X5R 402
C5966 10uF 20% 6.3V X5R 603
GND_SMC_AVSS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0V
THESE NEED TO BE PULLED TO THE PROPER RAIL:
SMS_INT_L
SMC_TPM_RESET_L
=PP3V3_S3_TPM
=PP3V3_S3_SMS
R5995 10K
R5989 10K
=PP3V42_G3H_SMC
RSMRST_PWRGD R5994 10K
SMC_ONOFF_L R5953 10K
5% 1/16W MF-LF 402
R5928 10K SMC_EXCARD_PWR_OC_L
SMC_TX_L R5980 10K
SMC_RX_L R5981 100K
SYS_ONEWIRE ONEWIRE_PULLUP_OLD R5982 2.0K
SMC_BS_ALRT_L R5983 470K
SMC_TMS R5984 10K
SMC_TDO R5985 10K
SMC_TDI R5986 10K
SMC_TCK R5987 10K
SMC_FWE R5948 10K
SMC_LID R5973 100K
SMC_ENRGYSTR_LDO_PGOOD R5919 10K
SMC_ENRGYSTR_LDO_EN NOSTUFF R5930 100K
SMC_P20 NOSTUFF R5920 10K
SMC_P21 NOSTUFF R5922 10K
SMC_P22 NOSTUFF R5923 10K
SMC_P23 NOSTUFF R5925 10K
SMC_P26 NOSTUFF R5927 10K
SMC_P27 NOSTUFF R5929 10K
SMC_P46 NOSTUFF R5934 10K
SMC_P44 NOSTUFF R5936 10K
SMC_SYS_KBDLED NOSTUFF R5938 10K
ALS_GAIN NOSTUFF R5918 10K
SMC_GPU_ISENSE R5940 10K
SMC_GPU_VSENSE R5942 10K
SMC_BATT_TRICKLE_EN_L R5954 10K
SMC_BATT_CHG_EN R5955 10K
SMC_BC_ACOK R5988 470K
R5905 100K PM_SUS_STAT_L
R5906 100K PM_SLP_S5_L
R5924 10K SMC_EXCARD_CP
R5926 10K SMC_EXCARD_PWR_EN NOSTUFF
R5931 10K SMC_FAN_0_CTL NOSTUFF
R5932 10K SMC_FAN_2_CTL NOSTUFF
R5933 10K SMC_FAN_3_CTL NOSTUFF
R5935 10K SMC_FAN_0_TACH NOSTUFF
R5937 10K SMC_FAN_2_TACH NOSTUFF
R5939 10K SMC_FAN_3_TACH NOSTUFF
R5941 10K SMC_PD3 NOSTUFF
R5945 10K ALS_LEFT NOSTUFF
R5946 10K ALS_RIGHT NOSTUFF
R5949 10K SMC_DISP_BKLT_B NOSTUFF
R5998 10K SMC_BATT_VSET NOSTUFF
R5999 10K SMC_SYS_VSET NOSTUFF
R5947 10K SMC_CASE_OPEN
R5996 10K SMC_PS_ON
R5943 10K SMC_NB_ISENSE NOSTUFF
R5944 10K SMC_MEM_ISENSE NOSTUFF
R5997 10K SMC_FWIRE_ISENSE
SMC 1.05V to 3.3V Level Shifting
=PP3V3_S0_SMC_LS
R5970 6.2K 5% 1/16W MF-LF 402
1.05V Mid-Reference
P0V52_SMC_LSREF
R5971 1K 5% 1/16W MF-LF 402
=PP3V42_G3H_SMC
R5976 10K 5% 1/16W MF-LF 402
SMC_CPU_RESET_3_3_L
C5977 0.1uF 20% 10V CERM 402
NOSTUFF
R5977 1K 5% 1/16W MF-LF 402
U5977 LMC7211 SM-LF
V+ V-
SMC_PROCHOT_3_3_L
CPU_PROCHOT_L
NOSTUFF
R5990 0 5% 1/16W MF-LF 402
SMC_TPM_GPIO
TPM_GPIO1
NOSTUFF
R5991 0 5% 1/16W MF-LF 402
TPM_GPIO2
R5992 0 5% 1/16W MF-LF 402
SMC_RX_L
SC_RX_L
R5993 0 5% 1/16W MF-LF 402
SMC_TX_L
SC_TX_L
Stuff R5992, R5993 for development only
SMC 3.3V to 1.05V Level Shifting
CPU_PROCHOT_L
Q5901 2N7002DW-X-F SOT-363
SMC_PROCHOT
PM_THRMTRIP_L
Q5901 2N7002DW-X-F SOT-363
SMC_THRMTRIP
SMC G3HOT OSCILLATOR
=PP3V42_G3H_SMC_CLK
L5910 FERR-120-OHM-0.2A 0603
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.425V
PP3V42_G3H_SMC_CLK_F
CRITICAL
C5910 4.7UF 20% 6.3V CERM 603
C5911 0.1UF 20% 10V CERM 402
U5910 32.768KHZ-9-3.6V SG-3040LC-SM
VDD VIO OUT NC0 NC1 NC2 NC3 NC4 NC5 NC6 NC7 GND
SMC_SUS_CLK_R
R5911 22 5% 1/16W MF-LF 402
SMC_SUS_CLK
197S0166
U5910 is really a 32.768KHz oscillator
System (Sleep) LED Circuit
=PP5V_S3_SYSLED
NOSTUFF
C5951 2.2UF 20% 4V X5R 402
R5951 2.2K 5% 1/16W MF-LF 402
CRITICAL
OMIT
R5950 84.5 1% 1/16W MF-LF 402
SYS_LED_ILIM
C5951 AND R5951 SHOULD BE PLACED CLOSE TO Q5950
SYS_LED_L_VDIV
Q5950 2N3906 SOT23-LF
SYS_LED_ANODE
R5952 4.7K 5% 1/16W MF-LF 402
SYS_LED_L
Q5952 2N7002 SOT23-LF
SMC_SYS_LED_16B

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5965	TI REF3133

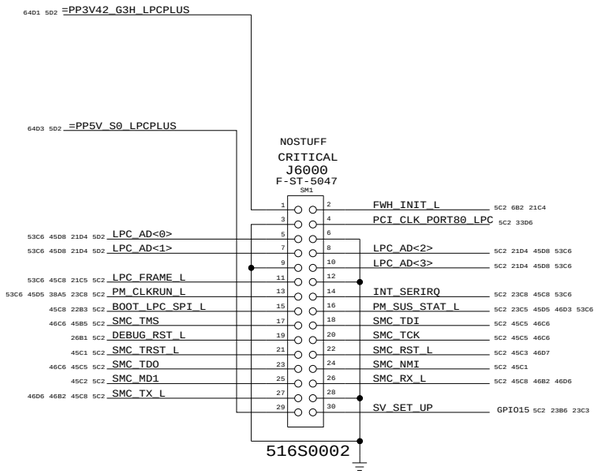
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0114	1	84.5, 1%, 1/16W, MF-LF, 402	R5950	NORMAL
114S0126	1	115, 1%, 1/16W, MF-LF, 402	R5950	FANCY

SMC SUPPORT

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

APPLE INC.

SIZE D | DRAWING NUMBER 051-7370 | REV. C | SCALE NONE | SHT 59 OF 98



LPC+ Debug Connector

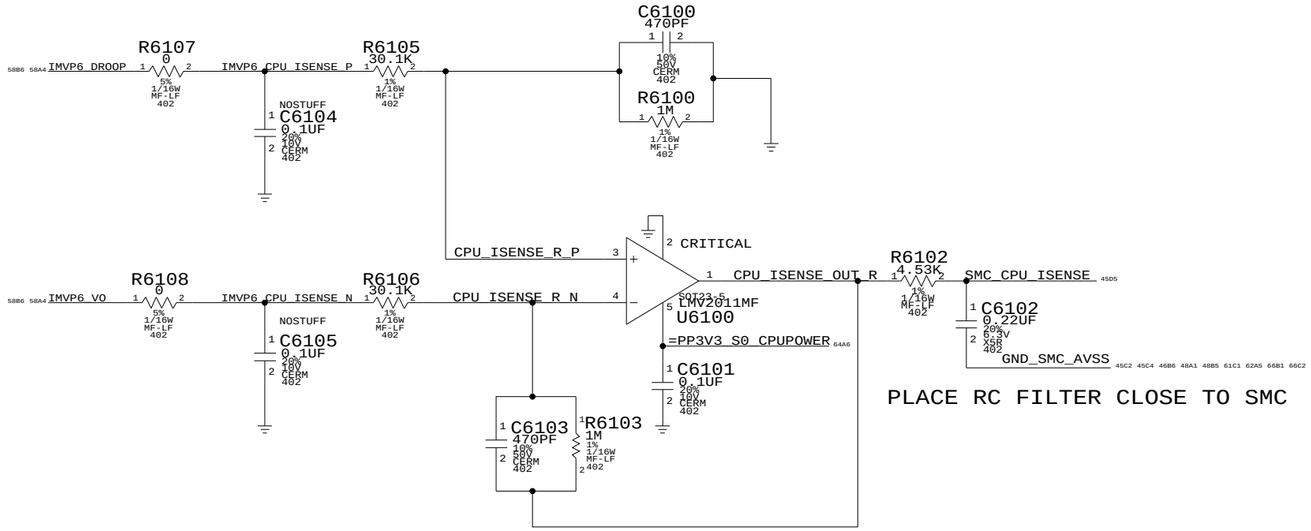
SYNC_MASTER=NB SYNC_DATE=06/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

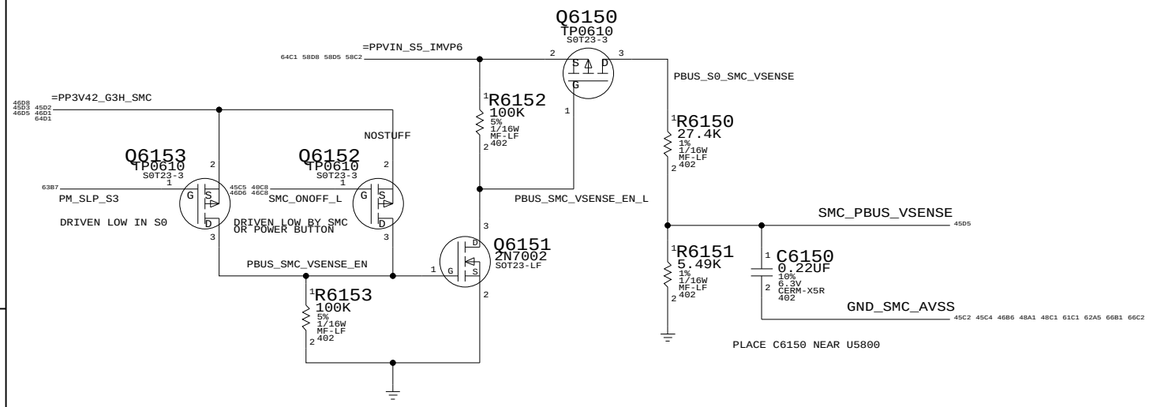
SCALE	SHT	OF
NONE	60	98

CPU CURRENT SENSE



PLACE RC FILTER CLOSE TO SMC

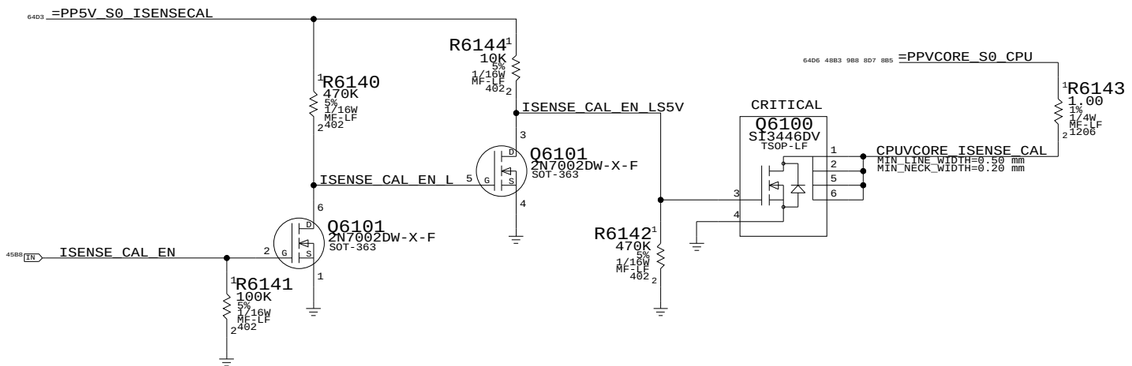
PROCESSOR DCIN VOLTAGE SENSE



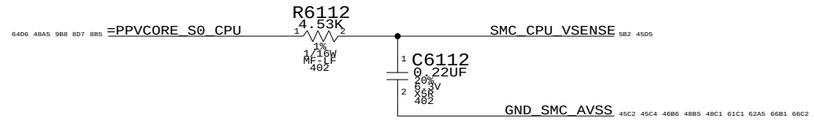
PLACE C6150 NEAR U5800

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



CPU VOLTAGE SENSE



PLACE RC FILTER CLOSE TO SMC

CPU Current & Voltage Sense

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

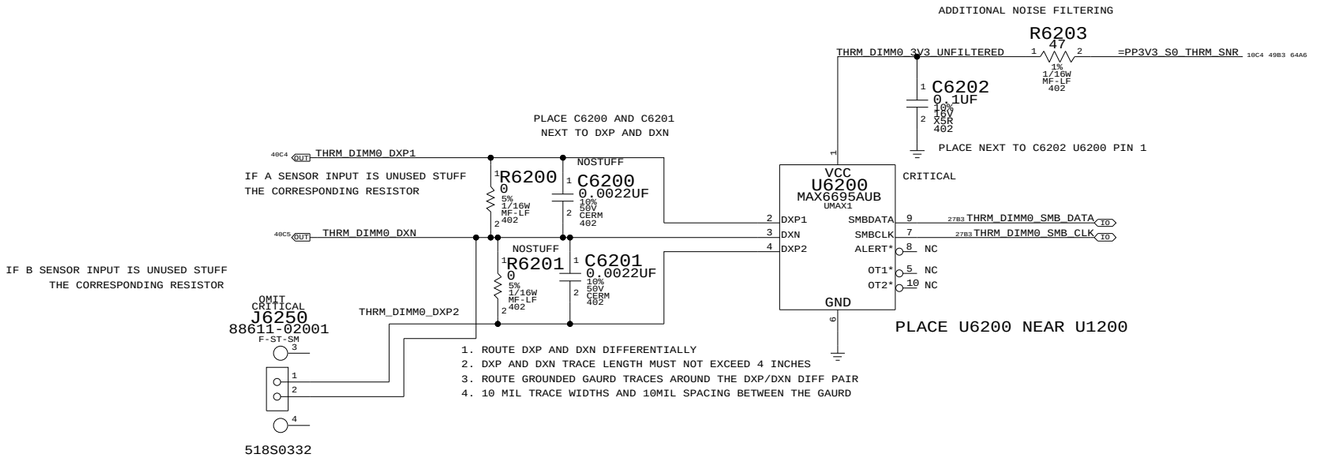
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

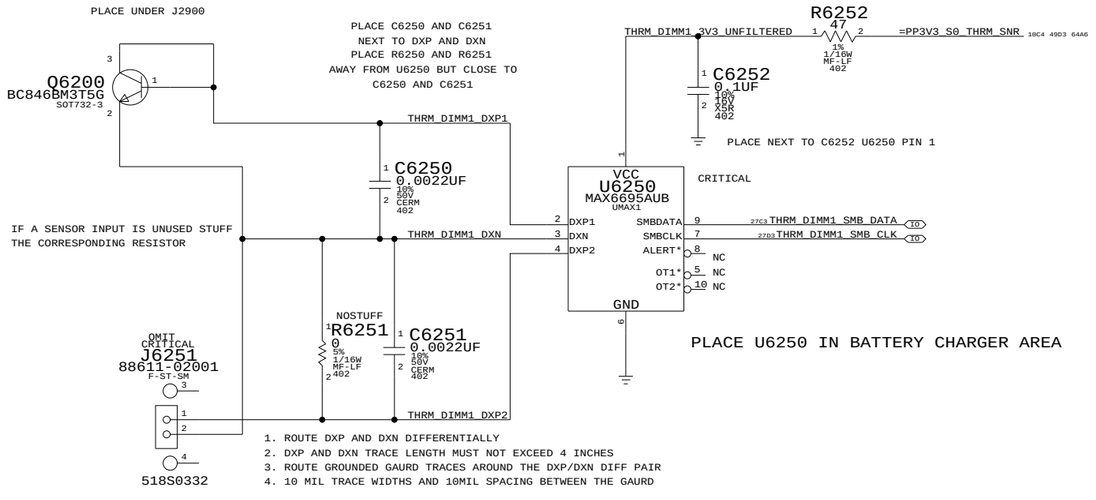
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 61 OF 98	

DIMM0 TEMPERATURE ZONE



NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

DIMM1 TEMPERATURE ZONE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
518S0487	2	JST 2-PIN CONNECTOR	J6250,J6251	M42B

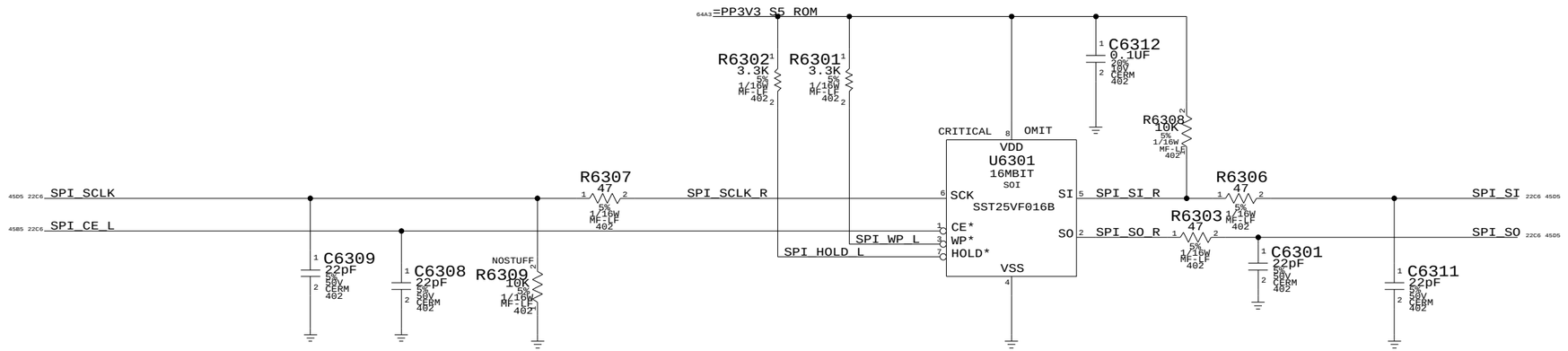
NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART

TEMPERATURE SENSE

SYNC_MASTER=ENET SYNC_DATE=11/09/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 62 OF 98	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

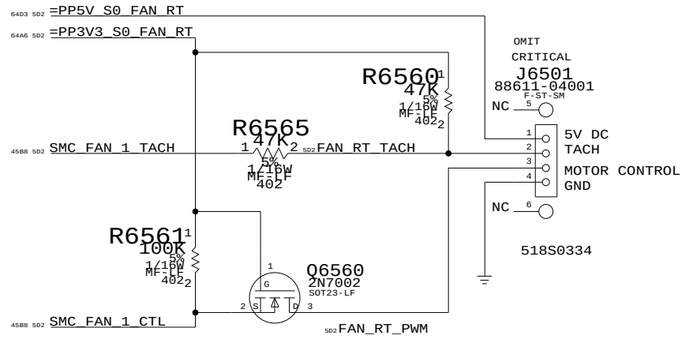
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 63 OF 98	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J6501	CRITICAL	M42B

Fan

SYNC_MASTER=ENET SYNC_DATE=11/10/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 65 OF 98	

PAGE NOTES

INPUT

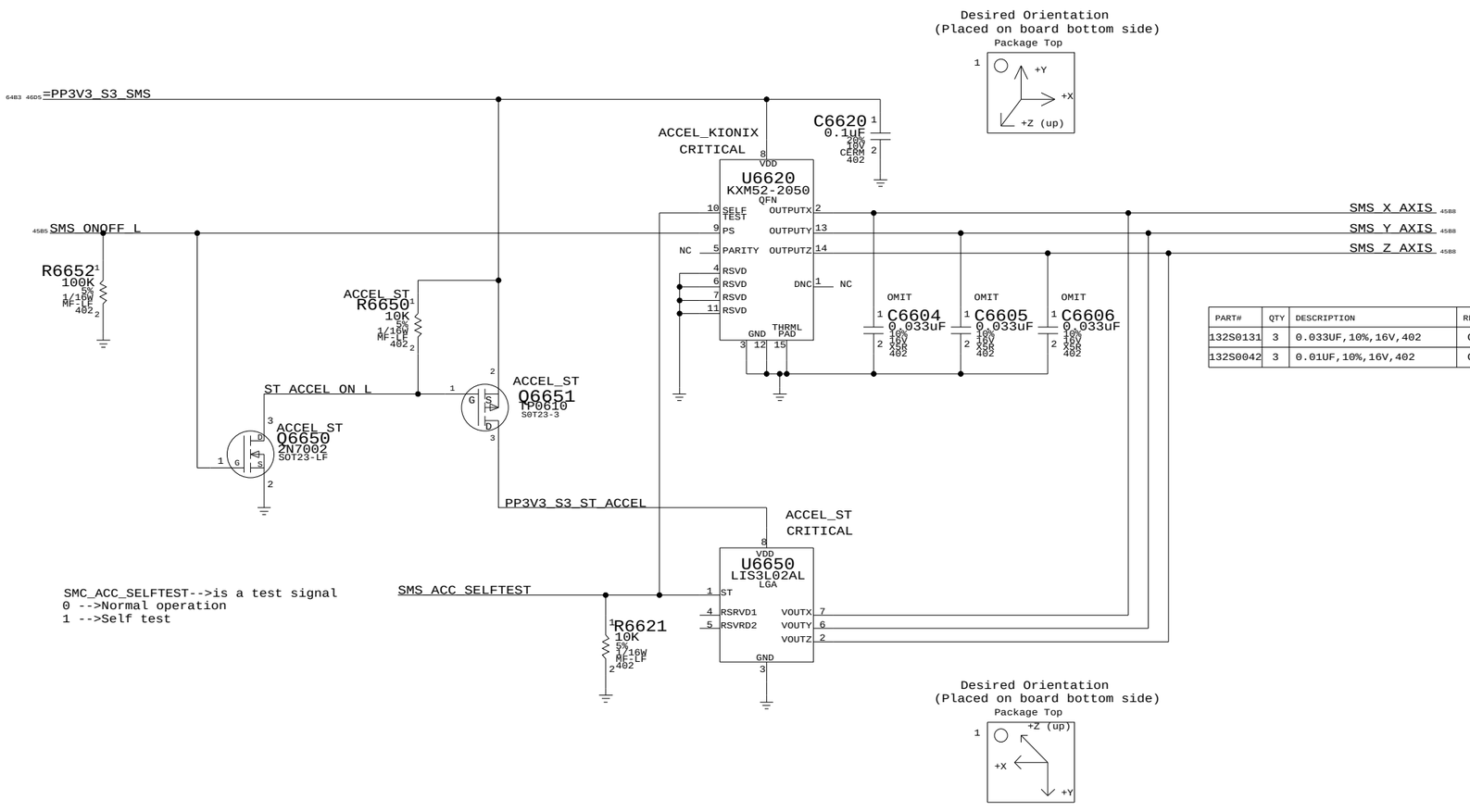
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



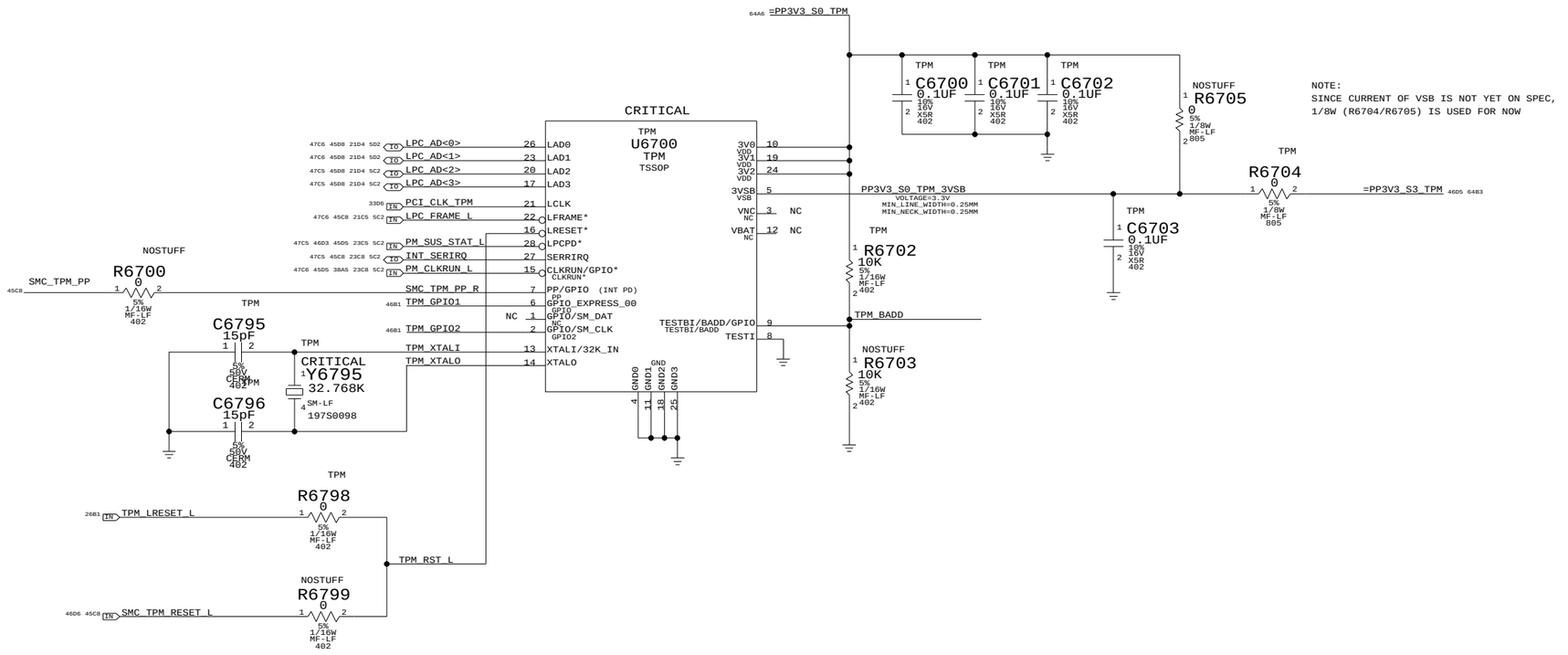
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0131	3	0.033UF,10%,16V,402	C6604,C6605,C6606		ACCEL_KIONIX
132S0042	3	0.01UF,10%,16V,402	C6604,C6605,C6606		ACCEL_ST

SMS

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 66 OF 98	



TPM

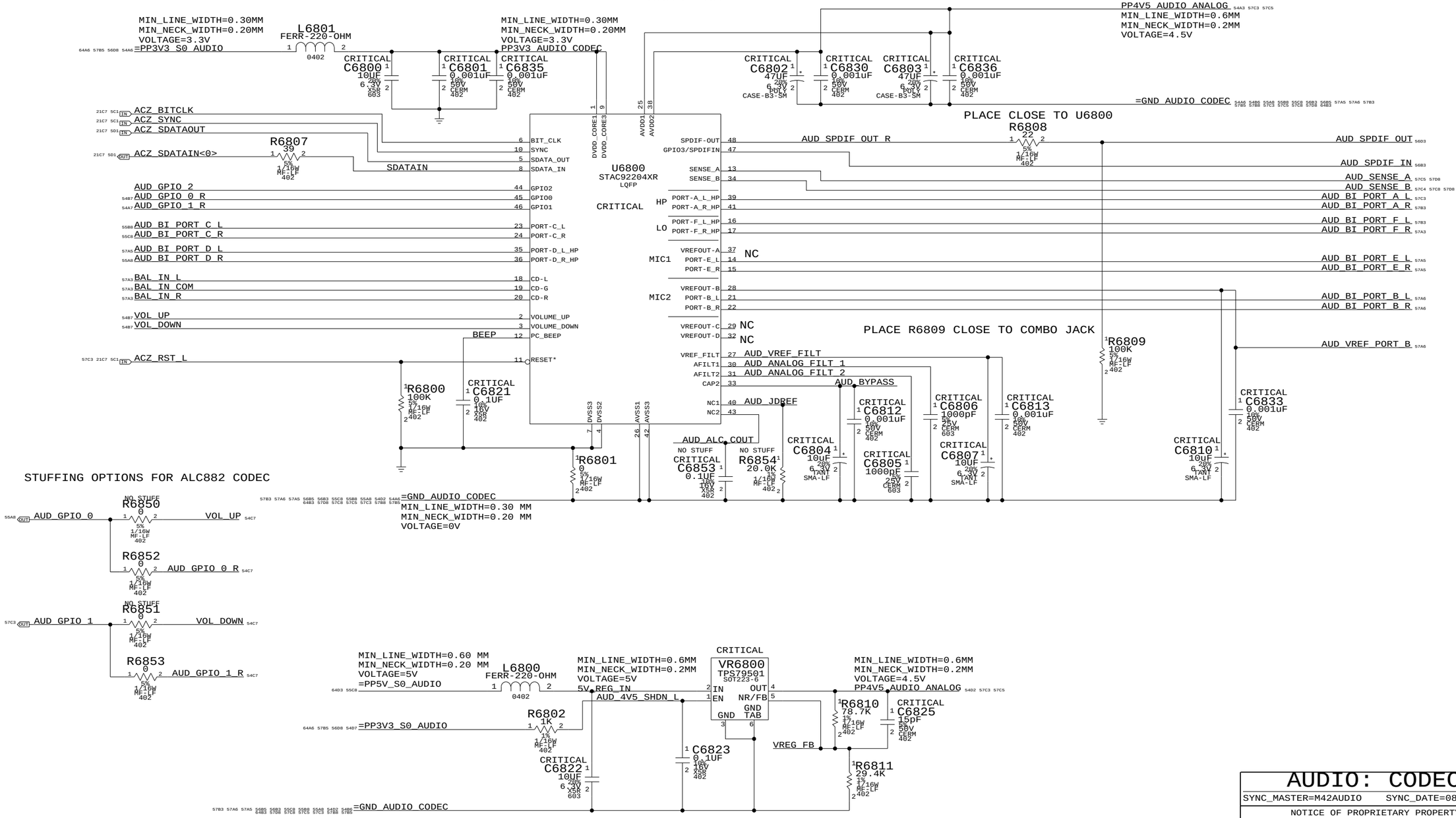
SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 67 OF 98	

AUDIO CODEC

APPLE P/N 353S1458



STUFFING OPTIONS FOR ALC882 CODEC

4.5V POWER SUPPLY FOR CODEC

AUDIO: CODEC

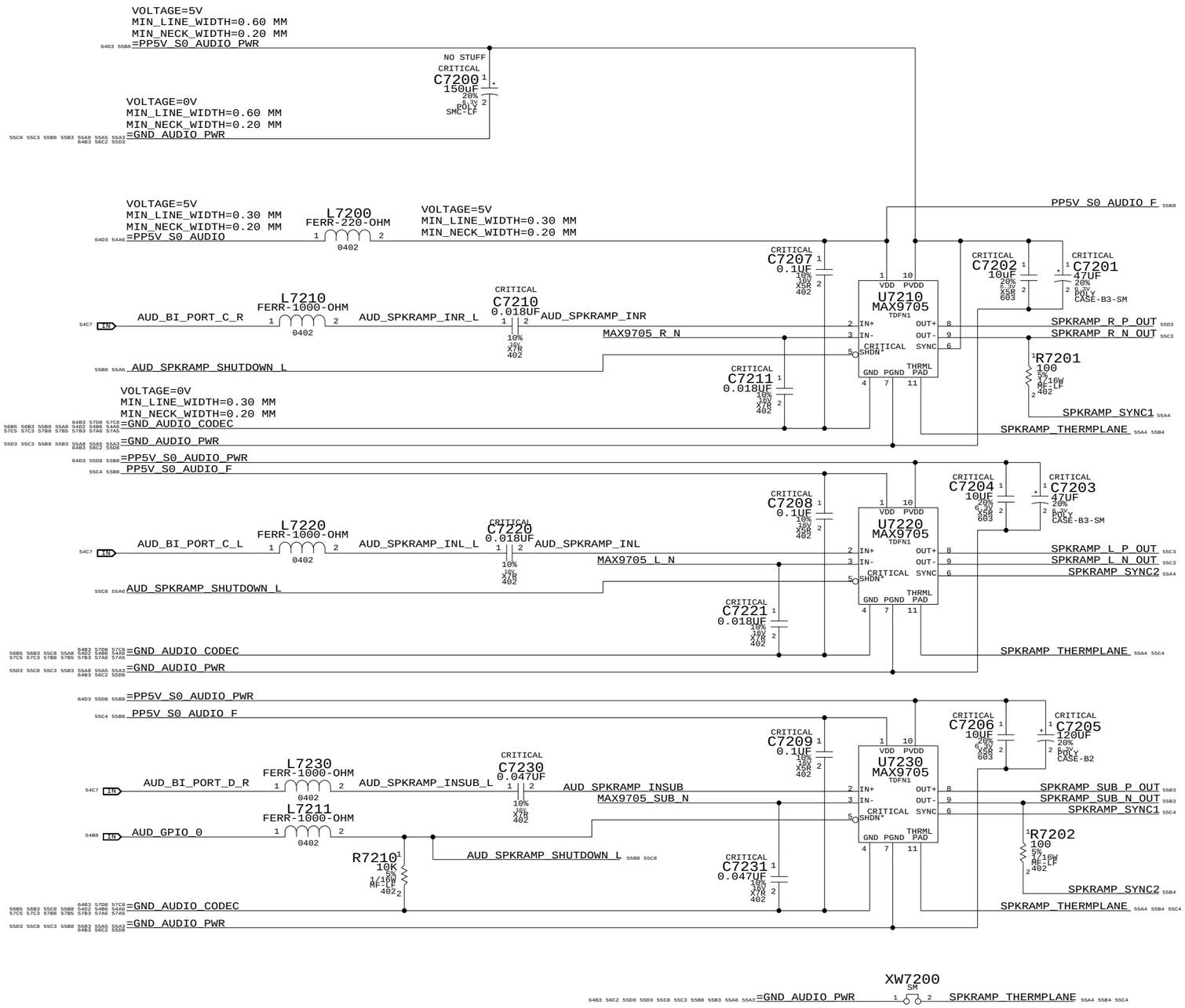
SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

APPLE INC.

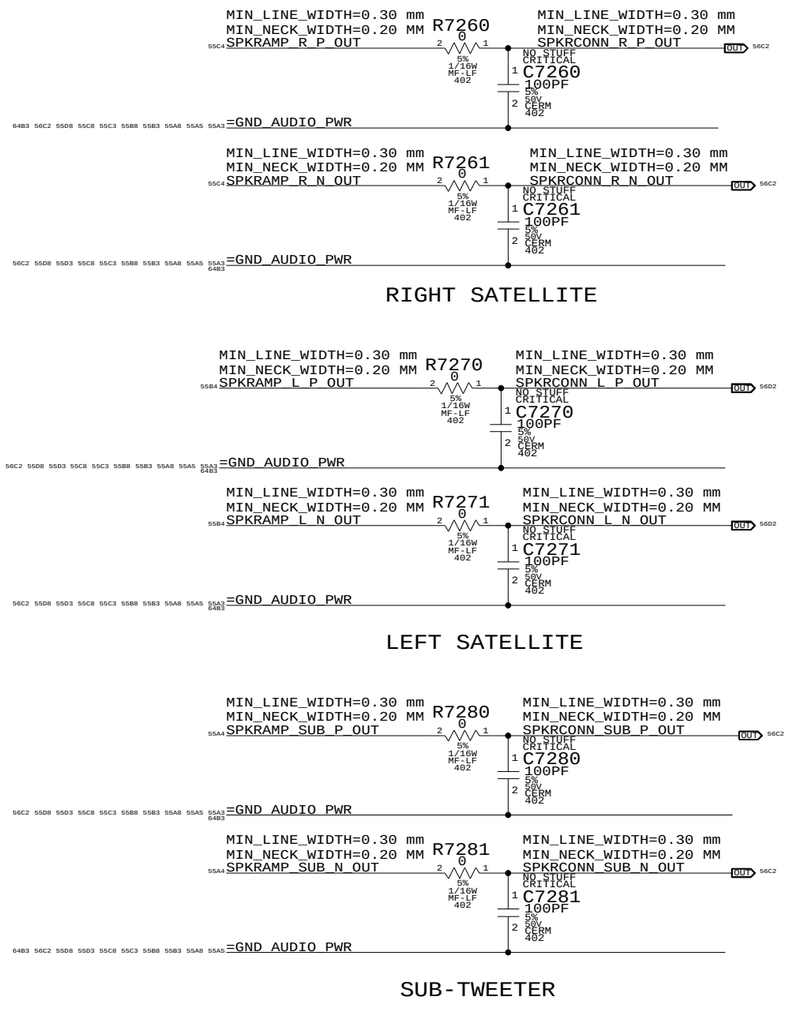
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 68 OF 98	

SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE 442 Hz < FC < 736 Hz
SUB 169 Hz < FC < 282 Hz



SPEAKER OUTPUT EMI FILTERS



AUDIO: SPEAKER AMP

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	72	98

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
518S0491	518S0332	?	J7302	IMPROVED TWO PIN CONNECTOR

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

L7390 FERR-220-OHM 0402 =PP3V3_S0_AUDIO
PP3V3_S0_AUDIO_SPDIF
APN:514-0290 APN:514-0317 OMIT CRITICAL J7300 AUDIO-OUT F-RT-TH
VCC GND VIN
SHLD_PIN SHLD_PIN
NO STUFF C7306 100PF 5% 50V CERM 402
C7300 1UF 10% 6.3V CERM 402
GND_AUDIO_SPDIF_DGND
R7391 0 5% 1/16W MF-LF 402
CHASSIS_AUDIO_JACK_ISOL
XW7305 SM =GND_CHASSIS_AUDIO_JACK CHASSIS_AUDIO_JACK_ISOL
NO STUFF R7320 0 5% 1/16W MF-LF 402 CHASSIS_AUDIO_JACK_ISOL =GND_AUDIO_CODEC
AUD_CONNJ1_SLEEVE NO STUFF R7321 0 5% 1/16W MF-LF 402
AUD_CONNJ1_TIPDET
AUD_CONNJ1_RING
AUD_CONNJ1_TIP
AUD_CONNJ1_SLEEVEDET
C7307 0.047uF 10% 10V X7R 402
C7308 0.047uF 10% 10V X7R 402
CRITICAL DZ7300 5.6V-15A 0405
CRITICAL DZ7301 5.6V-15A 0405
L7300 FERR-120-OHM-1.5A 0402-LF
L7302 FERR-1000-OHM 0402
L7303 FERR-1000-OHM 0402
L7305 FERR-1000-OHM 0402
L7307 FERR-1000-OHM 0402
AUD_CONNJ1_SLEEVE_F
AUD_CONNJ1_TIPDET_F
AUD_CONNJ1_RING_F
AUD_CONNJ1_TIP_F
AUD_CONNJ1_SLEEVEDET_F
C7302 100PF 5% 50V CERM 402
C7303 0.001uF 10% 50V CERM 402
C7305 100PF 5% 50V CERM 402
C7301 100PF 5% 50V CERM 402
L7301 FERR-120-OHM-1.5A 0402-LF
L7304 FERR-1000-OHM 0402
L7306 FERR-1000-OHM 0402
R7300 10K 5% 1/16W MF-LF 402
R7301 4.7 5% 1/16W MF-LF 402
AUD_SPDIF_OUT
AUD_PORTA_R
AUD_PORTA_L
AUD_J1_SLEEVEDET_R
AUD_J1_TIPDET_R
XW7300 SM AUD_J1_COM
XW7301 SM AUD_J2_COM =GND_AUDIO_CODEC

SPEAKER CONNECTOR

APN:518S0332

SPKRCONN_L_P_OUT
SPKRCONN_L_N_OUT
NO STUFF R7380 0 5% 1/16W MF-LF 402 =GND_AUDIO_PWR SPKR_SHIELD
SPKRCONN_SUB_P_OUT
SPKRCONN_SUB_N_OUT
SPKRCONN_R_P_OUT
SPKRCONN_R_N_OUT

APN:518S0334

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J7303	CRITICAL	M42B

MIC CONNECTOR

APN:514S0392

CRITICAL J7301 48227-0301 M-RT-SM1
MIC_LO_CONN
MIC_HI_CONN
MIC_SHLD_CONN

CRITICAL J7302 88611-02001 F-ST-SM

CRITICAL J7303 88611-04001 F-ST-SM

AUDIO SHIELD FILL

XW7302 SM AUDIO_SHIELD_PLANE CHASSIS_AUDIO_JACK_ISOL
XW7303 SM CHASSIS_AUDIO_JACK_ISOL
XW7304 SM CHASSIS_AUDIO_JACK_ISOL
NO STUFF R7382 0 5% 1/16W MF-LF 402

AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX

PP3V3_S0_AUDIO_SPDIF
APN:514-0291 APN:514-0318 OMIT CRITICAL J7350 AUDIO-IN F-RT-TH
VCC GND VOUT
SHLD_PIN SHLD_PIN
NO STUFF C7357 100PF 5% 50V CERM 402
C7350 1UF 10% 6.3V CERM 402
C7351 10uF 20% 6.3V X5R 603
GND_AUDIO_SPDIF_DGND
CHASSIS_AUDIO_JACK_ISOL
R7349 10 5% 1/16W MF-LF 402 AUD_J2_OPT_OUT
NO STUFF R7322 0 5% 1/16W MF-LF 402
AUD_CONNJ2_SLEEVE
AUD_CONNJ2_TIP
AUD_CONNJ2_TIPDET
AUD_CONNJ2_RING
AUD_CONNJ2_SLEEVEDET
CRITICAL DZ7350 5.6V-15A 0405
CRITICAL DZ7351 5.6V-15A 0405
L7350 FERR-220-OHM 0402
L7352 FERR-1000-OHM 0402
L7353 FERR-1000-OHM 0402
L7355 FERR-1000-OHM 0402
L7357 FERR-1000-OHM 0402
AUD_CONNJ2_SLEEVE_F
AUD_CONNJ2_TIPDET_F
AUD_CONNJ2_RING_F
AUD_CONNJ2_TIP_F
AUD_CONNJ2_SLEEVEDET_F
C7353 100PF 5% 50V CERM 402
C7354 0.001uF 10% 50V CERM 402
C7356 100PF 5% 50V CERM 402
C7352 100PF 5% 50V CERM 402
L7351 FERR-220-OHM 0402
L7354 FERR-1000-OHM 0402
L7356 FERR-1000-OHM 0402
R7350 10K 5% 1/16W MF-LF 402
R7351 4.7 5% 1/16W MF-LF 402
AUD_SPDIF_IN
AUD_PORTF_R
AUD_PORTF_L
AUD_J2_SLEEVEDET_R
AUD_J2_TIPDET_R

MIC EMI FILTER

L7370 FERR-1000-OHM 0402 MIC_LO
L7371 FERR-1000-OHM 0402 MIC_LO_F MIC_LO_CONN
L7372 FERR-1000-OHM 0402 MIC_HI
L7373 FERR-1000-OHM 0402 MIC_HI_F MIC_HI_CONN
L7374 FERR-1000-OHM 0402 MIC_SHIELD
L7375 FERR-1000-OHM 0402 MIC_SHIELD_F MIC_SHLD_CONN
C7370 100PF 5% 50V CERM 402
C7371 100PF 5% 50V CERM 402
C7372 100PF 5% 50V CERM 402
CHASSIS_AUDIO_JACK_ISOL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0409	1	CONN,3.5MM COMBO AUDIO OUT,RA,MG3,LF	J7300	CRITICAL	NORMAL
514-0408	1	CONN,3.5MM COMBO AUDIO IN,RA,MG3,LF	J7350	CRITICAL	NORMAL
514-0411	1	CONN,3.5MM COMBO AUDIO OUT,RA,BLACK,LF	J7300	CRITICAL	FANCY
514-0410	1	CONN,3.5MM COMBO AUDIO IN,RA,BLACK,LF	J7350	CRITICAL	FANCY

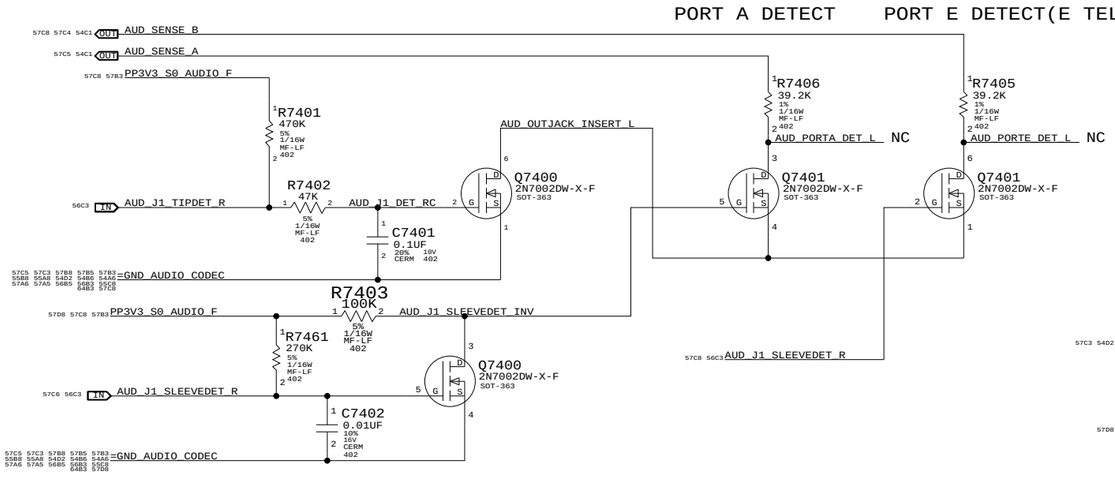
AUDIO: JACK

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

APPLE INC.

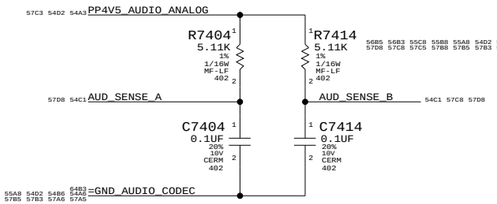
SIZE	DRAWING NUMBER	REV.
D	051-7370	C

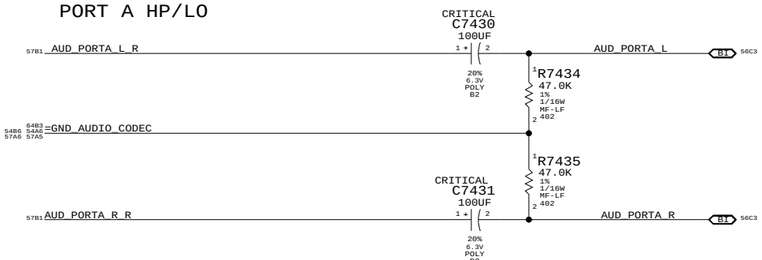
SCALE: NONE SHT 73 OF 98

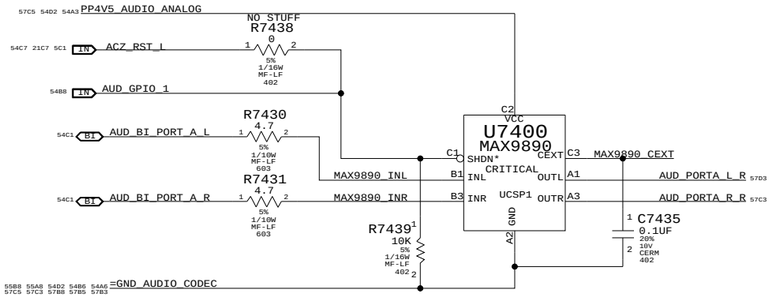


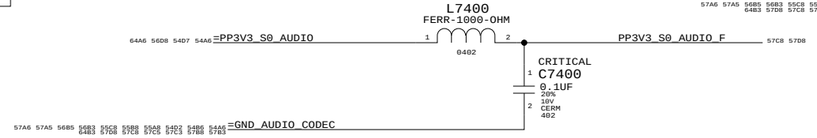
CODEC PORT ASSIGNMENTS

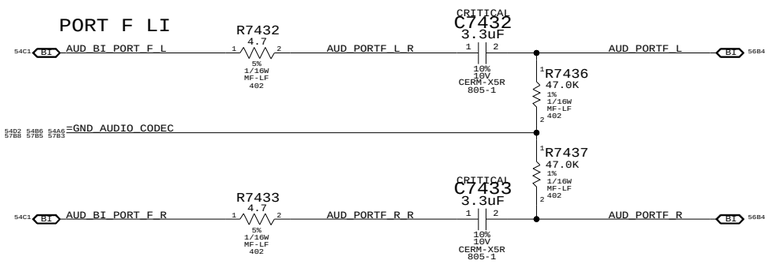
PORT A :HEADPHONE/LINE OUT
PORT B :MICROPHONE ON BOTH CH (ADC 0)
PORT C :SPEAKER AMP
PORT D :UNUSED
PORT E :SW USES TO TRIGGER DIGITAL OUT
PORT F :LINE IN (ADC 1)
CD INPUT :UNUSED

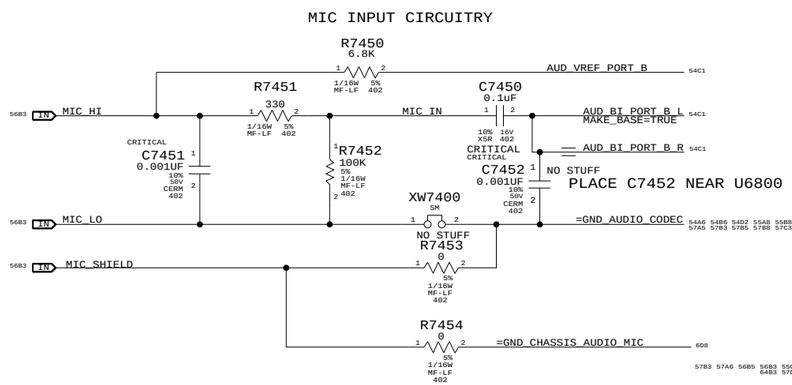


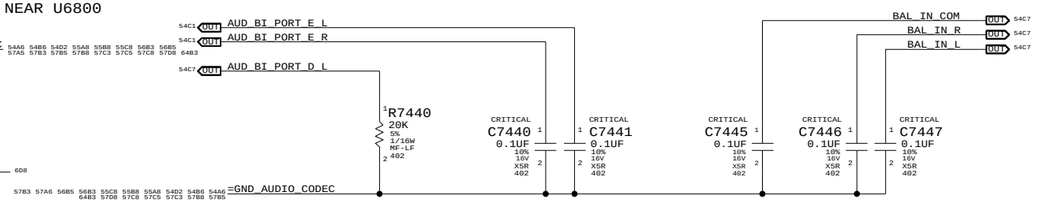












AUDIO: JACK TRANSLATORS

SYNC_MASTER=M42AUDIO SYNC_DATE=08/05/2006

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE	SHT	OF
NONE	74	98

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7501,C7508	KEMET T520V336M016ATE045?650
128S0093	128S0092	?	C7509,C7517	KEMET T520V336M016ATE045?650

DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Note 1: C7532,C7533 = 27.4 Ohm For Validating CPU Only.

R0802/R0803 **on the CPU page** protect the IMVP6 if the CPU is not installed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1465	1	ISL6262	U7500		M42
353S1461	1	ISL9504	U7500		M42A

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM
IMVP6_FET_RC1	0.25 MM	0.25 MM
IMVP6_VSUM_R1	0.25 MM	0.25 MM
IMVP6_VO_R1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM
IMVP6_FET_RC2	0.25 MM	0.25 MM
IMVP6_VSUM_R2	0.25 MM	0.25 MM
IMVP6_VO_R2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
CPU_VID_R<0..6>	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCORE REGULATOR

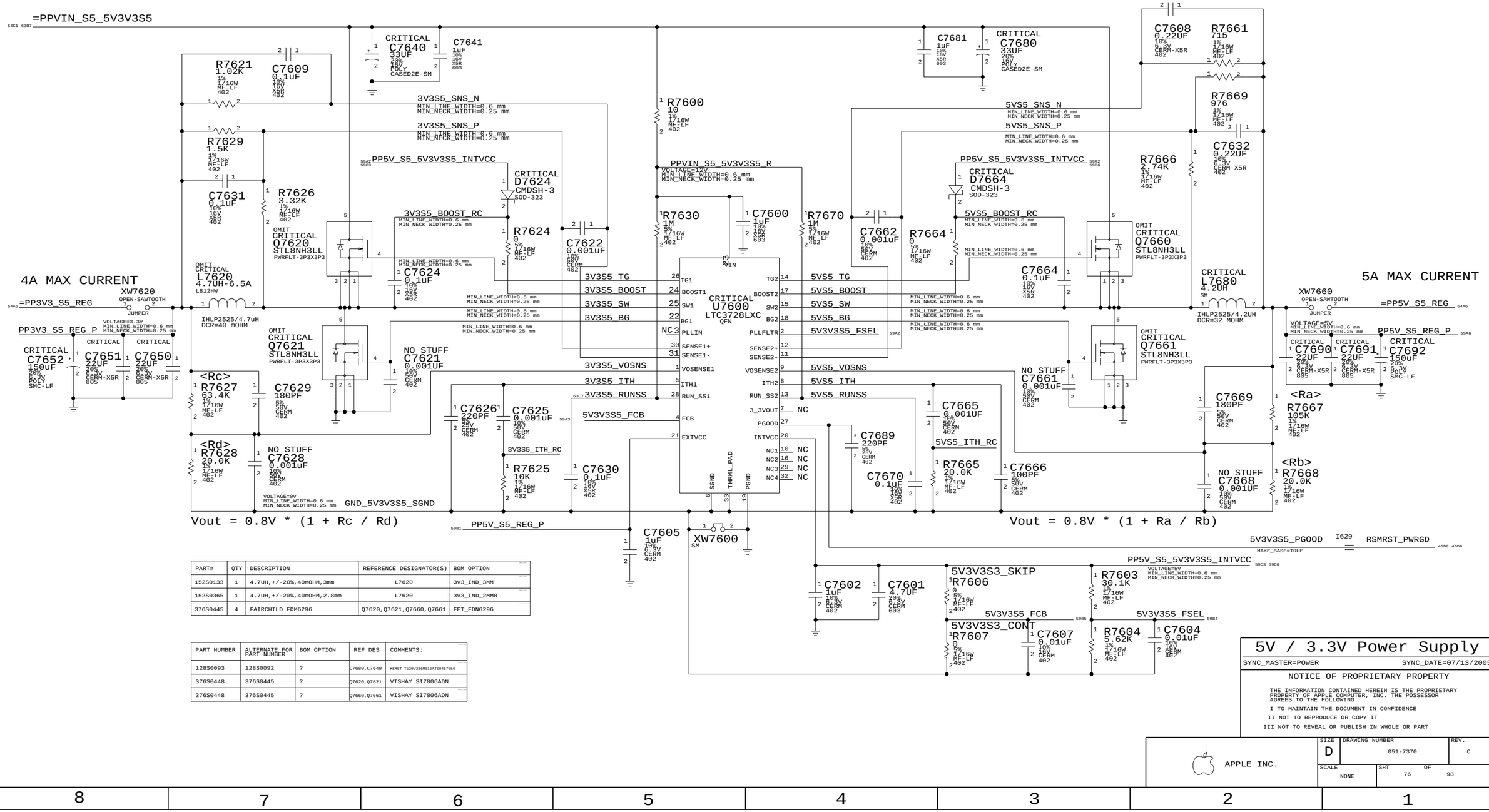
IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 75 OF 98	

5V/3.3V POWER SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S0133	1	4.7UH,+/-20%,40mOHM,3mm	L7620	3V3_IND_3MM
152S0365	1	4.7UH,+/-20%,40mOHM,2.8mm	L7620	3V3_IND_2MM8
376S0445	4	FAIRCHILD FDM6296	Q7620,Q7621,Q7660,Q7661	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7680,C7640	KEMET T520V336M016ATE045?650
376S0448	376S0445	?	Q7620,Q7621	VISHAY SI7806ADN
376S0448	376S0445	?	Q7660,Q7661	VISHAY SI7806ADN

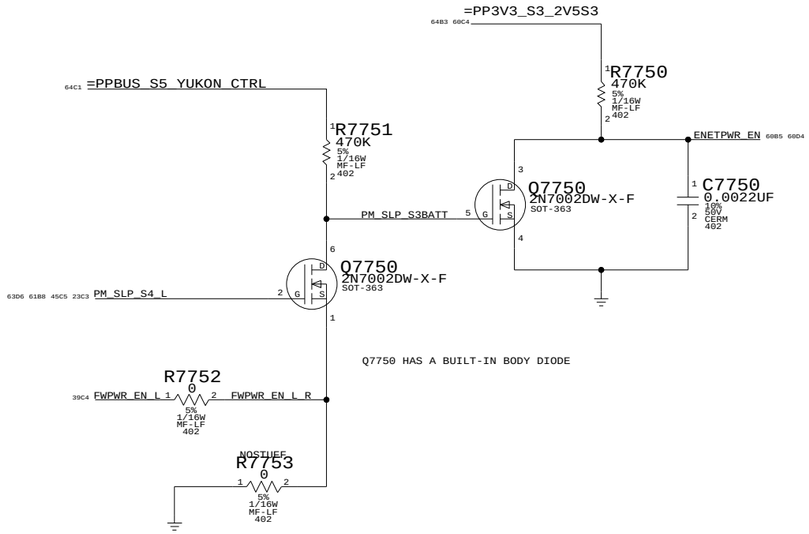
5V / 3.3V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 76 OF 98	

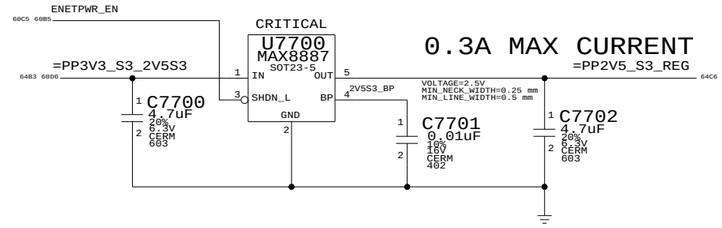
YUKON POWER CONTROL

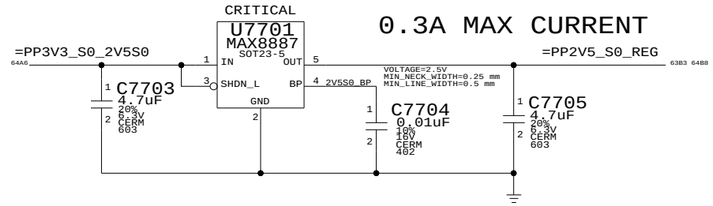


NAME	PM_SLP_S4_L	FWPWR_EN_L	PM_SLP_S3BATT	ENETPWR_EN
LOGIC	S3 | S0	~S0 | ~SMC_PS_ON		POWER YUKON
S3 ON BATTERY	TRUE (3.3V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S0 OR S3 ON AC	TRUE (3.3V)	FALSE (0V)	FALSE (0V)	TRUE (3.3V)
S5 ON AC	FALSE (0V)	TRUE (PBUS 12.6V)	TRUE (PBUS 12.6V)	FALSE (0V)
S5 ON BATT	FALSE (0V)	FALSE (0V)	TRUE (PBUS 12.6V)	FALSE (0V)

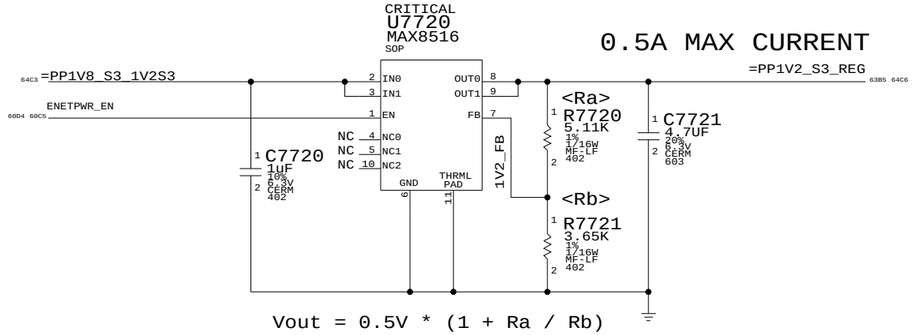
NOTE: IF CHANGE TO STUFFING R7753 THEN ENETPWR_EN IS BUFFERED PM_SLP_S4_L

2.5V REGULATORS





1.2V REGULATOR



Vout = 0.5V * (1 + Ra / Rb)

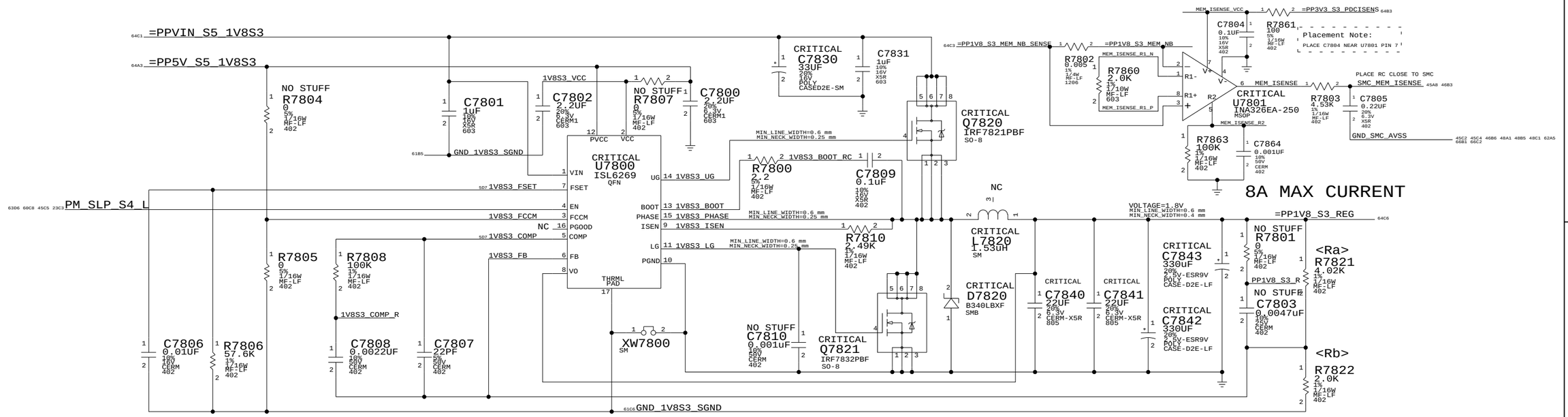
2.5V/1.2V Regulator

SYNC_MASTER=ENET SYNC_DATE=12/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 77 OF 98	

1.8V POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7830	KEMET T520V336M016ATE045760

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331ER
128S0095	128S0060	?	C7842,C7843	PANASONIC EEFSX0D331XE

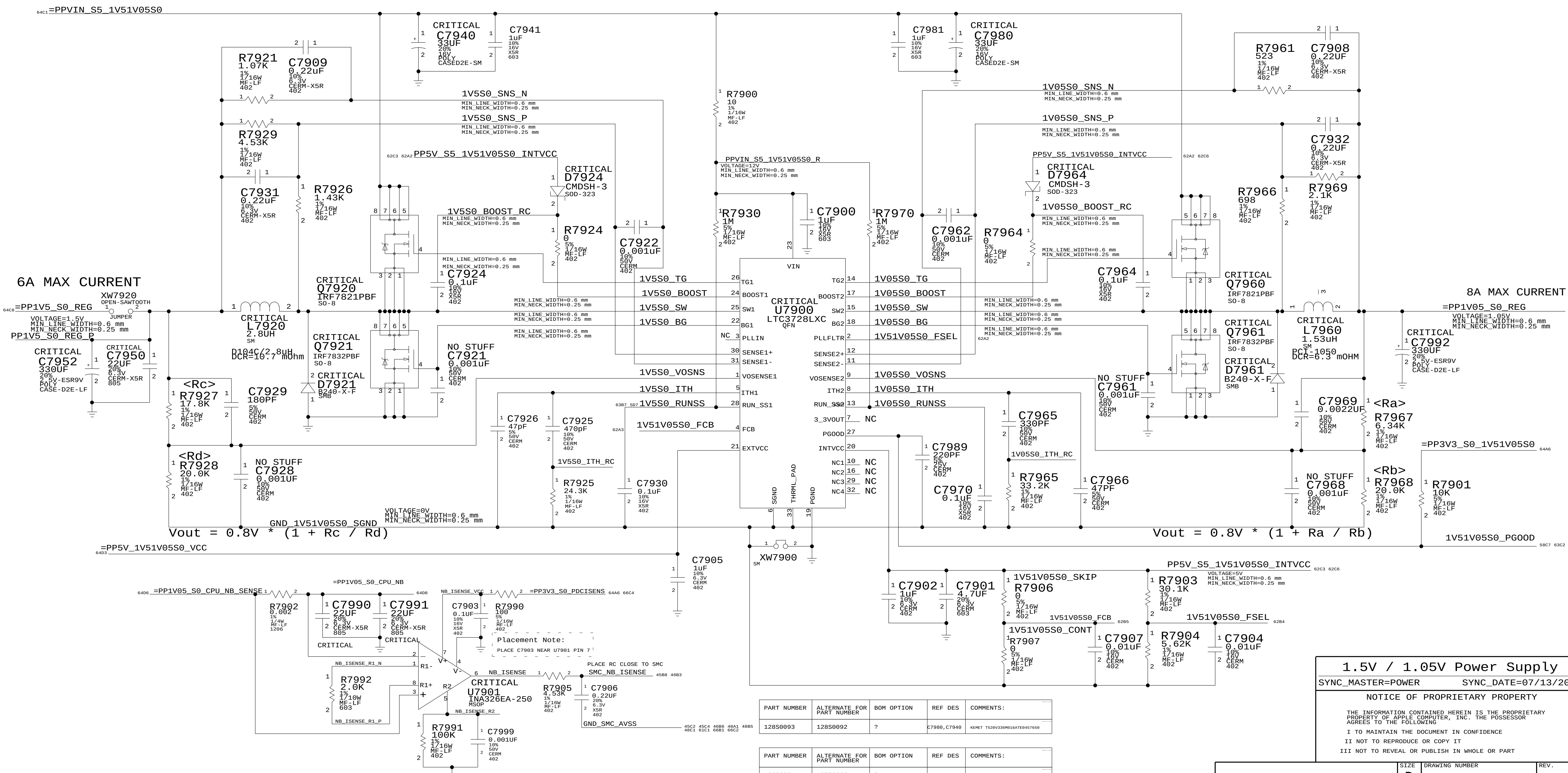
1.8V Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 78 OF 98	

1.5V/1.05V POWER SUPPLY



=PPVIN_S5_1V51V05S0
6A MAX CURRENT
=PP1V5_S0_REG
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
PP1V5_S0_REG_P
XW7920 OPEN-SAWTOOTH JUMPER
CRITICAL C7952 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C7950 22UF 20% 6.3V CERM-X5R 805
R7921 1.07K 1% 1/16W MF-LF 402
C7909 0.22uF 10% 6.3V CERM-X5R 402
R7929 4.53K 1% 1/16W MF-LF 402
C7931 0.22uF 10% 6.3V CERM-X5R 402
R7926 1.43K 1% 1/16W MF-LF 402
CRITICAL L7920 2.8UH SM
D104C/2.8uH DCR=10.7 mOhm
CRITICAL Q7920 IRF7821PBF SO-8
CRITICAL Q7921 IRF7832PBF SO-8
CRITICAL D7921 B240-X-F SMB
CRITICAL C7940 33UF 20% 16V POLY CASED2E-SM
C7941 1uF 10% 16V X5R 603
1V5S0_SNS_N
1V5S0_SNS_P
PP5V_S5_1V51V05S0_INTVCC
CRITICAL D7924 CMDSH-3 SOD-323
1V5S0_BOOST_RC
R7924 0 5% 1/16W MF-LF 402
C7922 0.001uF 10% 50V CERM 402
C7924 0.1uF 10% 16V X5R 402
NO STUFF C7921 0.001uF 10% 50V CERM 402
<Rc> R7927 17.8K 1% 1/16W MF-LF 402
C7929 180PF 5% 50V CERM 402
<Rd> R7928 20.0K 1% 1/16W MF-LF 402
NO STUFF C7928 0.001UF 10% 50V CERM 402
GND_1V51V05S0_SGND
VOLTAGE=0V
Vout = 0.8V * (1 + Rc / Rd)
=PP5V_1V51V05S0_VCC
C7926 47pF 5% 50V CERM 402
C7925 470pF 10% 50V CERM 402
1V5S0_ITH_RC
R7925 24.3K 1% 1/16W MF-LF 402
C7930 0.1uF 10% 16V X5R 402
R7900 10 1% 1/16W MF-LF 402
PPVIN_S5_1V51V05S0_R
VOLTAGE=12V
R7930 1M 5% 1/16W MF-LF 402
C7900 1uF 10% 16V X5R 603
R7970 1M 5% 1/16W MF-LF 402
CRITICAL U7900 LTC3728LXC QFN
VIN
TG1 BOOST1 SW1 BG1 PLLIN SENSE1+ SENSE1- VOSENSE1 ITH1 RUN_SS1 FCB EXTVCC
TG2 BOOST2 SW2 BG2 PLLFLTR SENSE2+ SENSE2- VOSENSE2 ITH2 RUN_SS2 3_3VOUT PGOOD INTVCC NC1 NC2 NC3 NC4
SGND THRML_PAD PGND
1V5S0_TG
1V5S0_BOOST
1V5S0_SW
1V5S0_BG
1V5S0_VOSNS
1V5S0_ITH
1V5S0_RUNSS
1V51V05S0_FCB
1V05S0_TG
1V05S0_BOOST
1V05S0_SW
1V05S0_BG
1V51V05S0_FSEL
1V05S0_VOSNS
1V05S0_ITH
1V05S0_RUNSS
NC
C7905 1uF 10% 6.3V CERM 402
XW7900 SM
C7981 1uF 10% 16V X5R 603
CRITICAL C7980 33UF 20% 16V POLY CASED2E-SM
1V05S0_SNS_N
1V05S0_SNS_P
CRITICAL D7964 CMDSH-3 SOD-323
1V05S0_BOOST_RC
C7962 0.001uF 10% 50V CERM 402
R7964 0 5% 1/16W MF-LF 402
C7964 0.1uF 10% 16V X5R 402
C7965 330PF 10% 50V CERM 402
1V05S0_ITH_RC
R7965 33.2K 1% 1/16W MF-LF 402
C7966 47PF 5% 50V CERM 402
C7989 220PF 5% 25V CERM 402
C7970 0.1uF 10% 16V X5R 402
R7961 523 1% 1/16W MF-LF 402
C7908 0.22UF 10% 6.3V CERM-X5R 402
C7932 0.22UF 10% 6.3V CERM-X5R 402
R7966 698 1% 1/16W MF-LF 402
R7969 2.1K 1% 1/16W MF-LF 402
CRITICAL Q7960 IRF7821PBF SO-8
CRITICAL Q7961 IRF7832PBF SO-8
CRITICAL D7961 B240-X-F SMB
NO STUFF C7961 0.001uF 10% 50V CERM 402
CRITICAL L7960 1.53uH SM
PCI-1050 DCR=6.3 mOHM
8A MAX CURRENT
=PP1V05_S0_REG
VOLTAGE=1.05V
CRITICAL C7992 330UF 20% 2.5V-ESR9V POLY CASE-D2E-LF
C7969 0.0022UF 10% 50V CERM 402
<Ra> R7967 6.34K 1% 1/16W MF-LF 402
NO STUFF C7968 0.001uF 10% 50V CERM 402
<Rb> R7968 20.0K 1% 1/16W MF-LF 402
=PP3V3_S0_1V51V05S0
R7901 10K 5% 1/16W MF-LF 402
Vout = 0.8V * (1 + Ra / Rb)
1V51V05S0_PGOOD
C7902 1uF 10% 6.3V CERM 402
C7901 4.7UF 20% 6.3V CERM 603
1V51V05S0_SKIP
R7906 0 5% 1/16W MF-LF 402
1V51V05S0_CONT
R7907 0 5% 1/16W MF-LF 402
C7907 0.01uF 10% 16V CERM 402
PP5V_S5_1V51V05S0_INTVCC
VOLTAGE=5V
R7903 30.1K 1% 1/16W MF-LF 402
R7904 5.62K 1% 1/16W MF-LF 402
C7904 0.01uF 10% 16V CERM 402
=PP1V05_S0_CPU_NB_SENSE
R7902 0.002 1% 1/4W MF-LF 1206
=PP1V05_S0_CPU_NB
CRITICAL C7990 22UF 20% 6.3V CERM-X5R 805
CRITICAL C7991 22UF 20% 6.3V CERM-X5R 805
NB_ISENSE_VCC
=PP3V3_S0_PDCISENS
C7903 0.1UF 10% 16V X5R 402
R7990 100 5% 1/16W MF-LF 402
Placement Note:
PLACE C7903 NEAR U7901 PIN 7
NB_ISENSE_R1_N
NB_ISENSE_R1_P
R7992 2.0K 1% 1/10W MF-LF 603
CRITICAL U7901 INA326EA-250 MSOP
NB_ISENSE
NB_ISENSE_R2
PLACE RC CLOSE TO SMC
SMC_NB_ISENSE
R7905 4.53K 1% 1/16W MF-LF 402
C7906 0.22UF 20% 6.3V X5R 402
GND_SMC_AVSS
R7991 100K 1% 1/16W MF-LF 402
C7999 0.001UF 10% 50V CERM 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7980,C7940	KEMET T520V336M016ATE0457650

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060	?	C7952,C7992	PANASONIC EEFSX0D331ER
128S0095	128S0060	?	C7952,C7992	PANASONIC EEFSX0D331XE

1.5V / 1.05V Power Supply

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

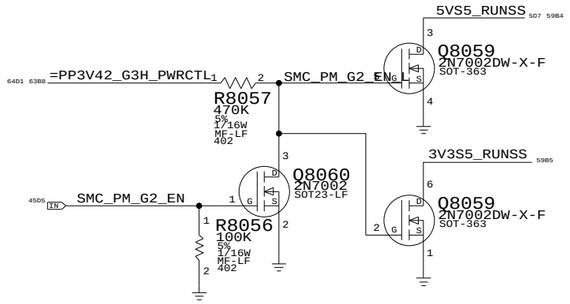
SCALE	SHT	OF
NONE	79	98

POWER CONTROL SIGNALS

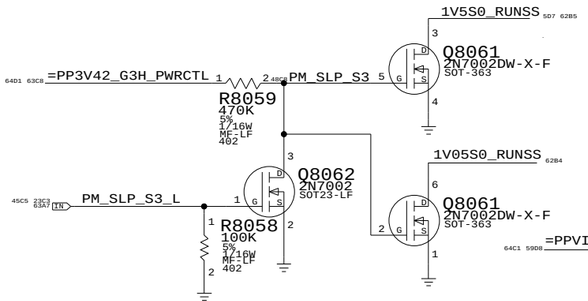
These rails are monitored by LTC2908

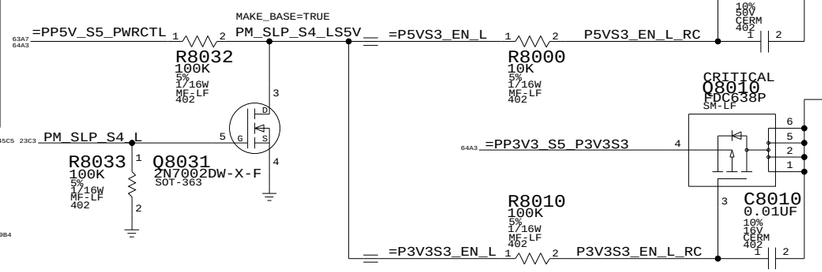
State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

5V/3.3V S5 RUN/SS CONTROL



1.5V/1.05V S0 RUN/SS CONTROL



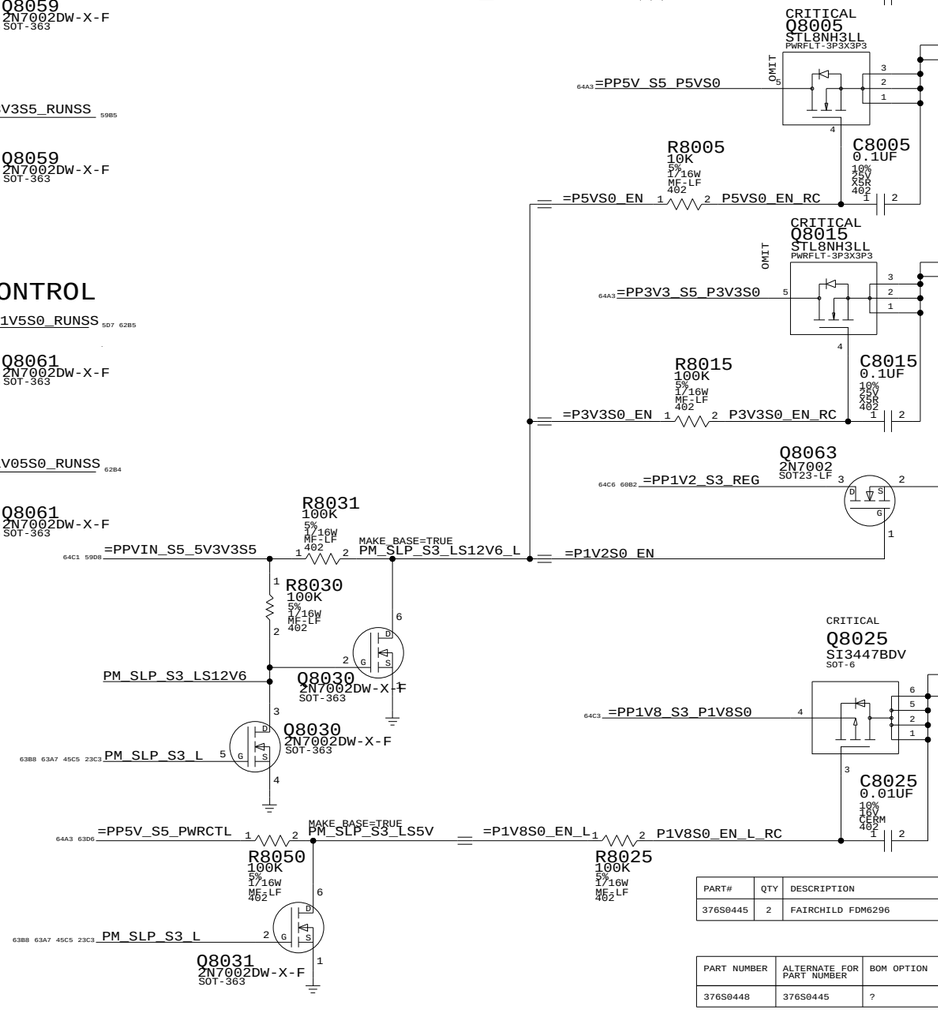


5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	100 mA

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	1 A



5V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	3 A

3.3V S0 FET

MOSFET	STL8NH3LL
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @10V
LOADING	2 A

1.2V S0 FET

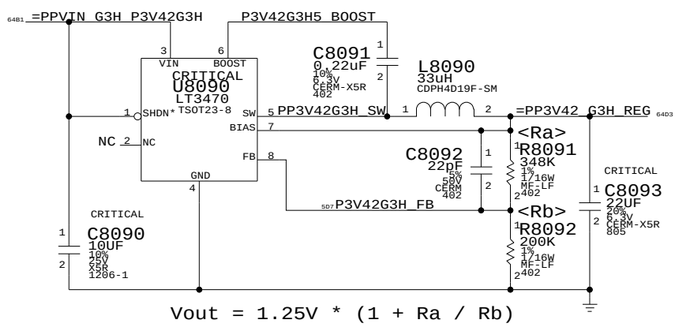
MOSFET	2N7002
CHANNEL	N-TYPE
RDS(ON)	13.5 Ohm
LOADING	Nothing

1.8V S0 FET

MOSFET	SI3447BDV
CHANNEL	P-TYPE
RDS(ON)	72 mOhm @1.8V
LOADING	320 mA

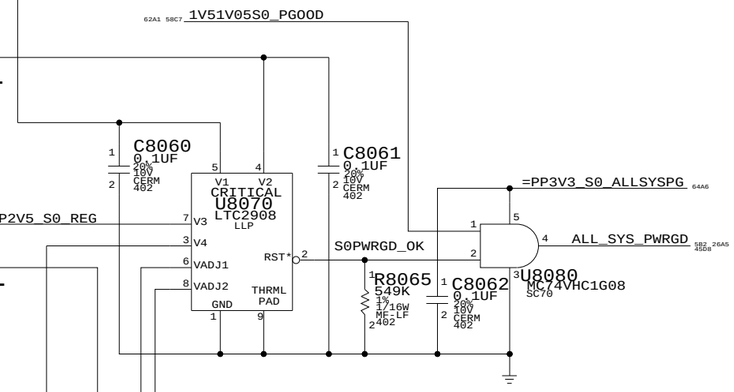
3.425V "G3Hot" SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Vout = 1.25V * (1 + Ra / Rb)

ALL SYSTEM PWRGD CIRCUIT



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0445	2	FAIRCHILD FDM6296	Q8005,Q8015	FET_FDN6296

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q8005,Q8015	VISHAY SI7806ADN

S3/S0 FETS, G3H SUPPLY

SYNC_MASTER=ENET SYNC_DATE=08/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE: NONE SHT 80 OF 98

"S0" RAILS ONLY ON IN RUN

PPVCORE_CPU_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(REGULATOR OUTPUT CPU VCORE PWR) =PPVOUT_S0_IMVP6_REG (58D1)
(CPU VCORE PWR) =PPVCORE_S0_CPU — 8B5 8D7 9B8 48A5 48B3

PP0V9_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=0.9V

(LDO OUTPUT 0.9V PWR) =PP0V9_S0_MEM_REG (63B2 31B3)
(DDR2 TERMINATION 0.9V PWR) =PP0V9_S0_MEM_TERM — 30D4

PP1V05_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V

(REGULATOR OUTPUT 1.05V PWR) =PP1V05_S0_REG (62B1 5B2)
(ICH CPU I/O 1.05V PWR) =PP1V05_S0_SB_CPU_IO — 21C1 24C3 25C4
(ICH VCORE 1.05V PWR) =PPVCORE_S0_SB — 24D3 25D3
=PP1V05_S0_CPU_NB_SENSE — 62A8

PP1V05_S0_CPU_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.05V

=PP1V05_S0_CPU_NB (62A6)
(MCH CORE 1.05V PWR) =PPVCORE_S0_NB — 16C8 16D3 19C8 19D7
(CPU FSB 1.05V PWR) =PP1V05_S0_CPU — 7B5 7B6 7D5 8C7 9C8 11B3 11C5
(MCH FSB 1.05V PWR) =PP1V05_S0_FSB_NB — 12A7 12B7 12C2 19D7 33B8 33C7 33C8
=PP1V05_S0_NB_VTT — 17D3 19B5 19D7
(MCH FSB 1.05V PWR) =PP1V05_S0_NB — 19D1 19D7

PP1V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.5V

(REGULATOR OUTPUT 1.5V PWR) =PP1V5_S0_REG (62B8)
(CPU AVDD 1.5V PWR) =PP1V5_S0_CPU — 8B7 9D8
(MCH PCIE GRAPHICS O/P COMPENSATION 1.5V PWR) =PP1V5_S0_NB_PCIE — 13D2 19D7
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V) =PP1V5_S0_NB_VCCAUX — 16D1 17B6 19B6 19D7
(MCH DIGITAL DIVIDER IN HMPLL 1.5V PWR) =PP1V5_S0_NB_VCCD_HMPLL — 17C6 19D7
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS — 17C6 19B8 19D7
(HOST/MEMORY PLL 1.5V PWR) =PP1V5_S0_NB_PLL — 19C6 19D7
=PP1V5_S0_NB — 19C1 19D7
(MCH TVDAC DEDICATED/QUIET PWR 1.5V) =PP1V5_S0_NB_TVDAC — 19A8 19D7
(MCH 3GIO[PCIE/DMI] 1.5V PWR) =PP1V5_S0_NB_3G — 19B5
(MCH 3GIO PLL 1.5V PWR) =PP1V5_S0_NB_3GPLL — 19A5
(ICH LOGIC&IO[ARX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ARX — 24B5 25D6
(ICH SATA PLL 1.5V PWR) =PP1V5_S0_SB_VCCSATAPLL — 24B5 25D6
(ICH LOGIC&IO[ATX] 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_ATX — 24A5 25C6
(ICH USB PLL 1.5V PWR) =PP1V5_S0_SB_VCCUSBPLL — 24A5 25B6
(ICH USB CORE 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A_USB_CORE — 24A3 25B2
(ICH LOGIC&IO 1.5V PWR) =PP1V5_S0_SB_VCC1_5_A — 24A3 25C2
=PP1V5_S0_SB — 25A8 25C8
(WIRELESS CARD 1.5V PWR) =PP1V5_S0_AIRPORT — 43D3

PP1V8_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

(COME FROM S3 TO S0 MOSFET) =PP1V8_S0_FET (63B3)
(DDR2 TERMINATION REGULATOR 1.8V SWITCH PWR) =PP1V8_S0_TMDS — 68D6

PP2V5_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(COME FROM S3 TO S0 MOSFET) =PP2V5_S0_REG (63B3 60C2)
(MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC — 17D6 19B6 19D7
(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS — 17D6 19B8 19D7
(MCH PCIE/DMI BAND GAP 2.5V PWR) =PP2V5_S0_NB_VCCA_3GBG — 17D6 19B7 19D7
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS — 17C6 19C7 19D1
(MCH CRTDAC ANALOG 2.5V PWR) =PP2V5_S0_NB_CRTDAC — 19D4 19D7
(TMDS 2.5V PWR) =PP2V5_S0_TMDS — 68B7
=PP2V5_S0_NB_DISP_PLL — 19D6

PP3V3_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

(COME FROM S5 TO S0 MOSFET) =PP3V3_S0_FET (63C3)
(MCH HV BUFFER 3.3V PWR) =PP3V3_S0_NB_VCC_HV — 17C6 19B7 19C7
=PP3V3_S0_SB — 22B5 25D8 34C8
(ICH GPIO PULLS 3.3V PWR) =PP3V3_S0_SB_GPIO — 21C3 21D3 23B2 23D5
(ICH IO BUFFER 3.3V PWR) =PP3V3_S0_SB_VCC3_3 — 24B5 25B8 25C6
(ICH PCI I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_PCI — 24B3 25A4
(ICH IDE I/O 3.3V PWR) =PP3V3_S0_SB_VCC3_3_IDE — 24C3 25B4
(ICH PCI PULLS 3.3V PWR) =PP3V3_S0_SB_PCI — 26D1
(ICH PM PULLS 3.3V PWR) =PP3V3_S0_SB_PM — 26B6 26B8
(PATA PULLS 3.3V PWR) =PP3V3_S0_PATA — 34C2
(SATA 3.3V PWR) =PP3V3_S0_SMC_LS — 46D3
(MCH PULLS 3.3V PWR) =PP3V3_S0_NB — 14C7 14D6 19C7 20A4 20B4
(ICH LAN I/F 3.3V PWR, NEED TO CHECK INTEL) =PP3V3_S0_SB_VCCLAN3_3 — 24D3 25D3
(ICH INTEL HDA CORE 3.3V PWR) =PP3V3_S0_SB_3V3_1V5_VCCHDA — 24C3 25C4
(DIMM SPD 3.3V PWR) =PPSPD_S0_MEM — 28A7 29A3 29A7
(CLOCK GENERATOR 3.3V PWR) =PP3V3_S0_CK410 — 32C7 32D3 32D8
(WIRELESS CARD 3.3V PWR) =PP3V3_S0_AIRPORT — 43C3
(TPM 3.3V PWR) =PP3V3_S0_TPM — 53D4
(AUDIO 3.3V PWR) =PP3V3_S0_AUDIO — 54A6 54D7 56D8 57B5
(TMDS 3.3V PWR) =PP3V3_S0_TMDS — 68B1 68B2 68C8 68D8 69B7 69D1 69D5
(CPU THERMAL SENSOR 3.3V PWR) =PP3V3_S0_THRM_SNR — 10C4 49B3 49D3
(ISL6262 3V3) =PP3V3_S0_IMVP6 — 58D8
=PP3V3_S0_RSTBUF — 26B4
=PP3V3_S0_SMBUS_SB — 27D8
=PP3V3_S0_SMBUS_SMC_0 — 27D5
=PP3V3_S0_SMBUS_SMC_MLB — 27C5
=PP3V3_S0_ALLSYSPG — 63B1
=PP3V3_S0_FAN_RT — 5D2 51C4
=PP3V3_S0_LCD — 67B5 67B7 67C6
=PP3V3_S0_PBATTISENS — 66B3
=PP3V3_S0_PDCISENS — 62A5 66C4
=PP3V3_S0_CPUPOWER — 48C2
=PP3V3_S0_SMBUS_SMC_BSB — 27B1
=PP3V3_S0_1V51V05S0 — 62B1
=PP3V3_S0_2V5S0 — 60C4
=PP3V3_S0_FW — 39C6
(FIREWIRE DIGITAL 3.3V PWR) =PP3V3_S0_ENET — 36C8

PP5V_S0
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V

(COME FROM S5 TO S0 MOSFET) =PP5V_S0_FET (63C3)
=PP5V_S0_SB — 25D8
(SATA 5V PWR) =PP5V_S0_SATA — 35C6
(DDR2 TERMINATION) =PP5V_S0_MEMVTT — 31C6
(AUDIO 5V PWR) =PP5V_S0_AUDIO — 54A6 55C8
(AUDIO SPEAKER 5V PWR) =PP5V_S0_AUDIO_PWR — 55B8 55D8
(LPC DEBUG BOARD 5V PWR) =PP5V_S0_LPCPLUS — 5D2 47C6
(MCH TV 3.3V LDO) =PP5V_S0_NB_TVDAC — 19C4 19C7
(ISL6262 VDD) =PP5V_S0_IMVP6 — 58D8
(LTC3728LXC EXTVCC) =PP5V_1V51V05S0_VCC — 62A8
(TMDS 5V PWR) =PP5V_S0_TMDS — 68B7 69C6
=PP5V_S0_FAN_RT — 5D2 51C4
=PP5V_S0_LCD — 67D7
=PP5V_S0_ISENSECAL — 48A8

"S3" RAILS
ON IN RUN AND SLEEP

PP1V2_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.32MM
VOLTAGE=1.2V

(LDO OUTPUT 1.2V PWR) =PP1V2_S3_REG (63B5 60B2)
(ENET 1.2V PWR) =PP1V2_S3_ENET — 36A8 36D7

PP1V8_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.8V

(REGULATOR OUTPUT 1.8V PWR) =PP1V8_S3_REG (61B1)
(DDR2 DIMM 1.8V PWR) =PP1V8_S3_MEM — 19C7 19C8 28B2 28D4 28D6 29B2 29D4 29D6
=PP1V8_S3_P1V8S0 — 63A5
=PP1V8_S3_MEMVTT — 31C6
=PP1V8_S3_MEM_NB_SENSE — 61C4
=PP1V8_S3_1V2S3 — 60B5

PP1V8_S3_MEM_NB
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=1.8V

=PP1V8_S3_MEM_NB (61C2 29D2 28D2 19D7 16B6 14C2)
(MCH DDR2 1.8V PWR)

PP2V5_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V

(REGULATOR OUTPUT 2.5V PWR) =PP2V5_S3_REG (60C2)
(ENET 2.5V PWR) =PP2V5_S3_ENET — 36D3

PP3V3_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.16 MM
VOLTAGE=3.3V

(COME FROM S5 TO S3 MOSFET) =PP3V3_S3_FET (63D3)
=PP3V3_S3_SMBUS_SMC_RMT — 27D3
(ETHERNET 3.3V PWR) =PP3V3_S3_ENET — 36A5 36B4 36B5 36C8 36D6 36D8
(BLUETOOTH 3.3V PWR) =PP3V3_S3_BT — 44C6
(ACCELEROMETER 3.3V PWR) =PP3V3_S3_SMS — 46D5 52C7
(TPM 3.3V SUSPEND PWR) =PP3V3_S3_TPM — 46D5 53C2
(TPS62050 VIN) =PP3V3_S3_2V5S3 — 60C4 60D6
(FIREWIRE CHIP PCI SIGNAL INDICATOR) =PP3V3_S3_PCI — 38C5
=PP3V3_S3_RSTGATE — 26B3
=PP3V3_S3_AIRPORT_AUX — 43C3
=PP3V3_S3_FW — 38D5
=PP3V3_S3_PDCISENS — 61C1

PP5V_S3
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(COME FROM S5 TO S3 MOSFET) =PP5V_S3_FET (63D3)
(ISL6269 PVCC)
(SYSTEM LED PWR) =PP5V_S3_SYSLED — 35B6 46B4
(USB IO PORT 5V PWR) =PP5V_S3_CAMERA — 67A5
(USB IR CONTROLLER 5V PWR) =PP5V_S3_IR — 41D6
=PP5V_S3_GEYSER — 40D6

"S5" RAILS
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP3V3_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=3.3V

(REGULATOR OUTPUT 3.3V PWR) =PP3V3_S5_REG (59B8)
=PP3V3_S5_SB — 23A7 23B7 23D4 23D8 25C8
(ICH USB CTL PULLS 3.3V PWR) =PP3V3_S5_SB_USB — 22D8
(ICH PM 3.3V PWR) =PP3V3_S5_SB_PM — 11B5 23D1 26C5
(ICH SUSPEND 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3 — 24A5 24B3 25B6 25D2
(ICH SUSPEND USB 3.3V PWR) =PP3V3_S5_SB_VCCSUS3_3_USB — 24B3 25D2
(ICH SUSPEND PULLS 3.3V PWR) =PP3V3_S5_SB_IO — 22C6
(ICH INTEL HDA SUSPEND 3.3V PWR) =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA — 24C3
(SPI BOOTROM PWR) =PP3V3_S5_ROM — 50D4
=PP3V3_S5_P3V3S3 — 63D5
=PP3V3_S5_P3V3S0 — 63C5
=PP3V3_S5_FWLATEVG — 39A8
=PP3V3_S5_LCD — 67C7

PP5V_S5
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=5V

(REGULATOR OUTPUT 5 PWR) =PP5V_S5_REG (59B1)
=PP5V_S5_SB — 25C8
=PP5V_S5_P5VS3 — 63D5
=PP5V_S5_PWRCTL — 63A7 63D6
=PP5V_S5_P5VS0 — 63C5
=PP5V_S5_USB — 42C8
=PP5V_S5_PATA (PATA 5V PWR) — 34D6
=PP5V_S5_1V8S3 — 61C7

G3 HOT

PP3V42_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.425V

=PP3V42_G3H_REG (63D1)
=PP3V42_G3H_SMCVREF — 46C8
=PP3V42_G3H_SMBUS_SMC_BSA — 27C3
=PP3V42_G3H_PWRCTL — 63B8 63C8
=PP3V42_G3H_LIDSWITCH — 65A8
(LPC DEBUG BOARD) =PP3V42_G3H_LPCPLUS — 5D2 47C6
=PP3V42_G3H_SB_RTC — 26D6
=PP3V42_G3H_ACIN — 65C4 65C8 66A5
(SMC 32.768KHz OSC) =PP3V42_G3H_SMC_CLK — 46A8
(SMC 3.3V PWR) =PP3V42_G3H_SMC — 45D2 45D3 46D1 46D5 46D8 48C8

PBUS HOT

PPBUSB_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=12.6V

=PPBUSA_G3H (66C2)
(INVERTER PBUS PWR)
(ISL6262 VIN)
(LTC3728 VIN) =PPBUS_S5_INV — 67D4
=PPVIN_S5_IMVP6 — 48C7 58C2 58D5 58D8
=PPVIN_S5_1V51V05S0 — 62D8

=PPBUSB_G3H (66C2)
(LTC3728 VIN) =PPVIN_S5_5V3V3S5 — 59D8 63B7
(ISL6269 VIN) =PPVIN_S5_1V8S3 — 61C7
(FIREWIRE PORT PBUS PWR) =PPBUS_S5_FWPWRSW — 39D6
(YUKON POWER CONTROL) =PPBUS_S5_YUKON_CTRL — 60C8

PP18V5_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.5V

=PP18V5_G3H_INRUSH (65D1)
(DC-IN OUTPUT 18.5V PWR)
(CHARGER INPUT 18.5V PWR)
(SMC INPUT 18.5V PWR) =PP18V5_G3H_CHGR — 66D8

DCIN G3HOT

PPDCIN_G3H
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.3MM
VOLTAGE=18.5V

=PPDCIN_G3H (65D3)
=PPVBATT_G3H (66B2)
=PPVIN_G3H_P3V42G3H — 63D3

GND RAILS

XW8101
SM
=GND_AUDIO_CODEC (5D1) — GND_AUDIO_CODEC — MAKE_BASE=TRUE
57A6 57A5 56B5 56B3 55C8 55B8 55A8 54D2 54B6 54A5 57D8 57C8 57C5 57C3 57B8 57B5 57B3

XW8102
SM
=GND_AUDIO_PWR (5D1) — GND_AUDIO_PWR — MAKE_BASE=TRUE
56C2 55D8 55D3 55C8 55C3 55B8 55B3 55A8 55A5 55A3

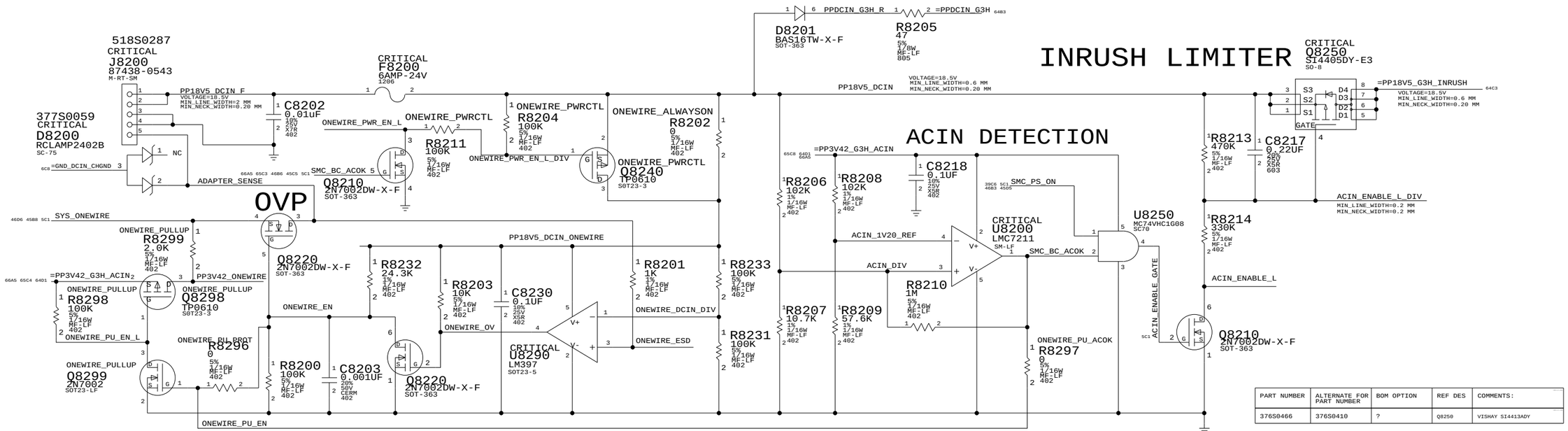
Power Conn / Alias

SYNC_MASTER=ENET SYNC_DATE=11/16/2005

APPLE INC.

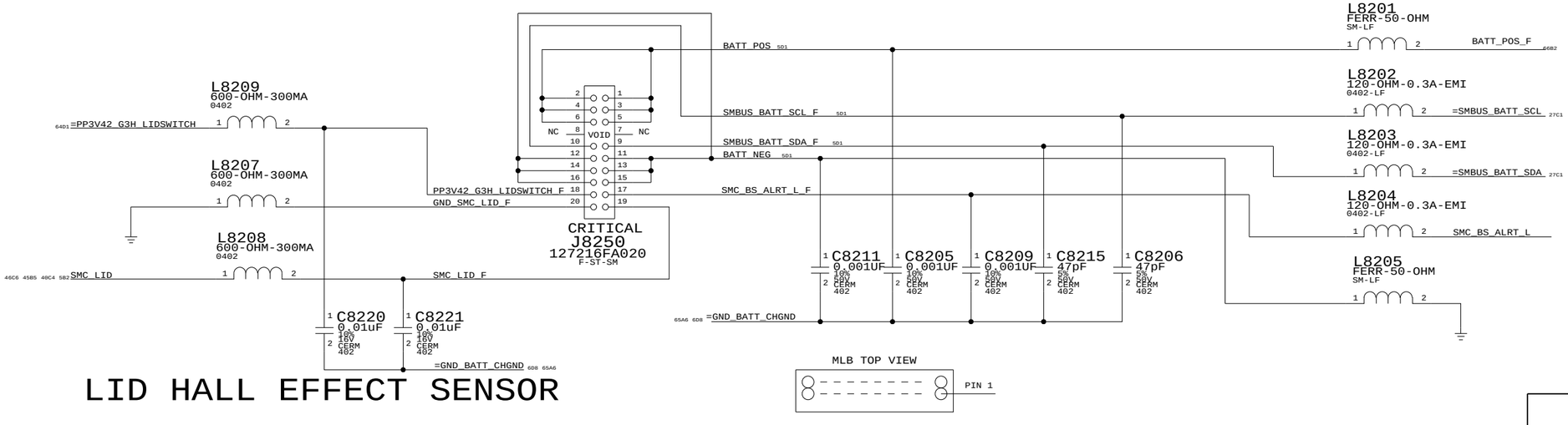
SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 81 OF 98	

DC-JACK INTERFACE



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0466	376S0410	?	Q8250	VISHAY SI4413ADY

BATTERY INTERFACE



LID HALL EFFECT SENSOR

DC-In & Battery Connectors

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C

SCALE	SHT	OF
NONE	82	98

PBUS SUPPLY / BATTERY CHARGER

CHLIM circuit (R8362, R8363, C8328) subject to change pending M1 resolution (100mV offset, radar 4221420)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C8308,C8310	KEMET T520V336M016ATE045/650
376S0466	376S0410	?	Q8300,Q8320	VISHAY SI4413ADY
376S0466	376S0410	?	Q8321	VISHAY SI4413ADY

PBUS Supply/Battery Charger

SYNC_MASTER=SMC SYNC_DATE=08/19/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 83 OF 98	

INVERTER CONNECTOR

=PP5V_S0_LCD — R9400 100K 1% 1/16W MF-LF 402 — R9401 100K 1% 1/16W MF-LF 402 — INV_PWREN_F_L — INV_PWREN_L — Q9405 TP0610 SOT23-3 — PP5V_INV (MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM, VOLTAGE=5V)

LVDS_BKLTEN — Q9406 2N7002 SOT23-LF

C9414 0.0022UF 10% 50V CERM 402

L9403 FERR-120-OHM-1.5A 0402-LF — =PPBUS_S5_INV — PPBUS_ALL_INV_CONN (VOLTAGE=12.6V, MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM)

L9402 FERR-120-OHM-1.5A 0402-LF

L9400 120-OHM-0.3A-EMI 0402-LF — PP5V_INV_F (VOLTAGE=5V, MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM)

L9401 120-OHM-0.3A-EMI 0402-LF

C9401 100PF 5% 50V CERM 402 — C9402 100PF 5% 50V CERM 402 — C9403 100PF 5% 50V CERM 402 — C9400 100PF 5% 50V CERM 402

OMIT
CRITICAL
J9400 88611-04001 F-ST-SM
INV_GND
INV_BKLIGHT_PWM_L
518S0334

=PP3V3_S0_LCD — INVERTER_BUF — U9453 MC74VHC1G08 SC70 — LVDS_BKLTCTL — BKLIGHT_CTL

C9459 0.1UF 10% 16V X5R 402

INVERTER_UNBUF — R9428 0 5% 1/10W MF-LF 402

INVT_CHGND — THIS GND CONECTS TO CHASSIS GND

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518S0486	1	IMPROVED ACES CONNECTOR	J9400	CRITICAL	M42B

LCD + CAMERA CONNECTOR

=PP3V3_S5_LCD — R9402 100K 5% 1/16W MF-LF 402 — R9423 10K 5% 1/16W MF-LF 402 — LCDVDD_PWREN_L — LCDVDD_PWREN_L_R

LVDS_VDDEN — Q9404 2N7002 SOT23-LF

R9414 100K 1% 1/16W MF-LF 402

Q9403 FDC638P SM-LF

C9413 0.0033UF 10% 50V CERM 402

C9411 0.1UF 10% 16V X5R 402 — C9412 10UF 20% 6.3V X5R 603

PP3V3_LCDVDD_SW (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM)

L9404 FERR-120-OHM-1.5A 0402-LF — PP3V3_LCDVDD_SW_F (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.30 MM, MIN_NECK_WIDTH=0.20 MM)

=PP3V3_S0_LCD — R9408 10K 5% 1/16W MF-LF 402 — R9409 10K 5% 1/16W MF-LF 402

L9408 120-OHM-0.3A-EMI 0402-LF — PP3V3_S0_LCD_F (LVDS_DDC_POWER) (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.20 MM)

LVDS_DDC_CLK
LVDS_DDC_DATA

LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
LVDS_A_DATA_N<2>
LVDS_A_DATA_P<2>
LVDS_A_CLK_N
LVDS_A_CLK_P

=PP3V3_S0_LCD — NOSTUFF R9415 10K 5% 1/16W MF-LF 402 — NOSTUFF R9416 10K 5% 1/16W MF-LF 402

LVDS_CLKCTLA
LVDS_CLKCTLB

CRITICAL L9407 90-OHM SM SYM_VER-1

=USB2_CAMERA_P — USB2_CAMERA_CONN_P
=USB2_CAMERA_N — USB2_CAMERA_CONN_N

L9405 FERR-120-OHM-1.5A 0402-LF — =PP5V_S3_CAMERA — PP5V_S3_CAMERA_F (VOLTAGE=5V, MIN_NECK_WIDTH=0.20 MM, MIN_LINE_WIDTH=0.30 MM)

=SMBUS_ATS_SCL
=SMBUS_ATS_SDA

C9409 0.001uF 10% 50V CERM 402

CRITICAL J9401 S-050162B F-RT-SM
=GND_CHASSIS_LVDS

LCD I/F
CAMERA I/F

C9416 0.001uF 10% 50V CERM 402 — C9415 0.001uF 10% 50V CERM 402 — C9410 0.001uF 10% 50V CERM 402 — C9408 0.001uF 10% 50V CERM 402

Plexi: 516S0212
*Enclosure: 518S0364

LVDS REFERENCE CURRENT,1.5K OHM PULL DOWN RESISTOR NEEDED

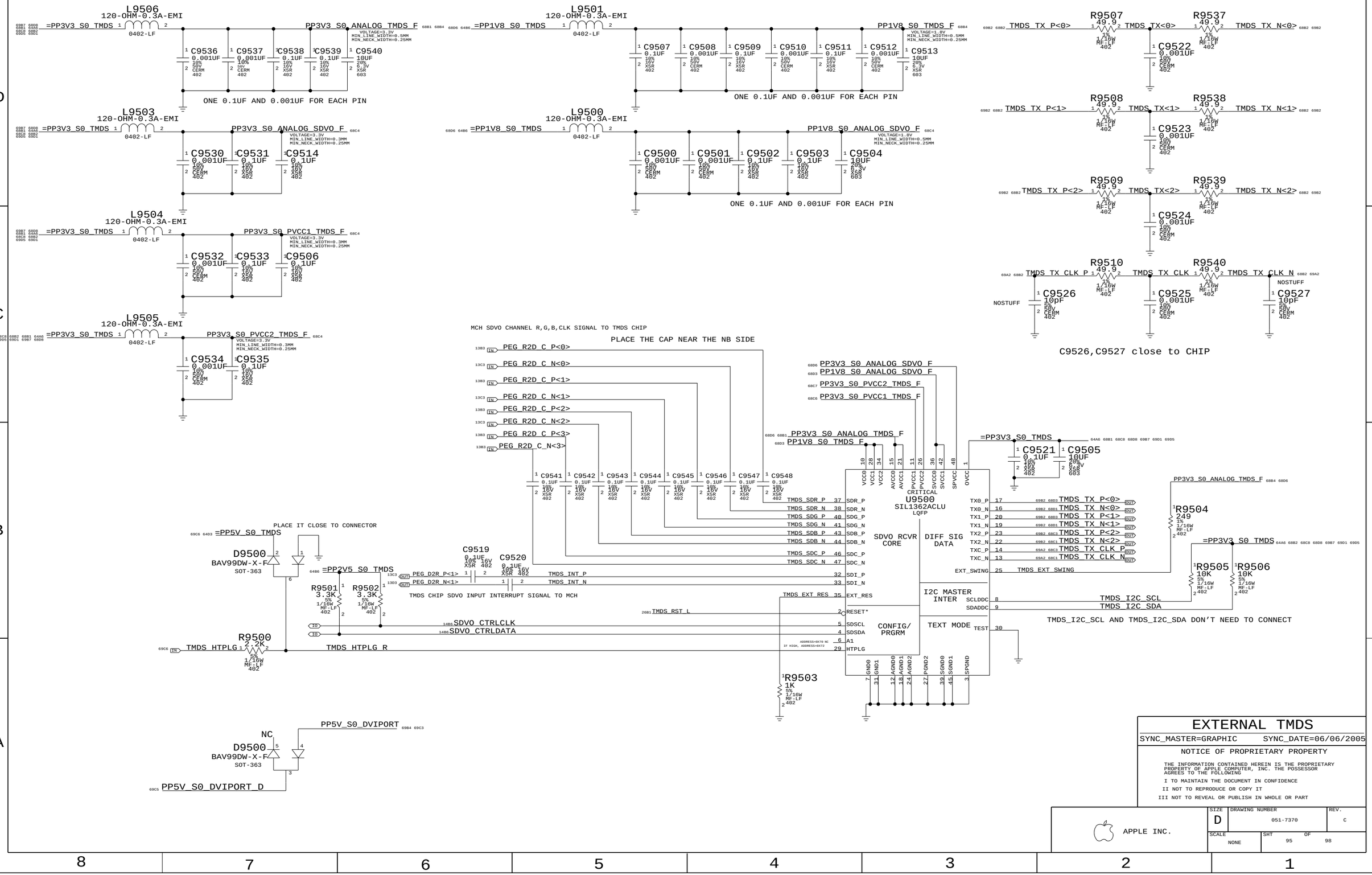
LVDS_VREFH
LVDS_VREFL
LVDS_IBG — R9413 1.5K 1% 1/16W MF-LF 402

INVERTER,LVDS,TMDS

SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 94 OF 98	


L9506
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
0402-LF
PP3V3_S0_ANALOG_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9536 0.001UF 10% 50V CERM 402
C9537 0.001UF 10% 50V CERM 402
C9538 0.1UF 10% 16V X5R 402
C9539 0.1UF 10% 16V X5R 402
C9540 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN
L9503
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
PP3V3_S0_ANALOG_SDVO_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9530 0.001UF 10% 50V CERM 402
C9531 0.1UF 10% 16V X5R 402
C9514 0.1UF 10% 16V X5R 402
L9504
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
PP3V3_S0_PVCC1_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9532 0.001UF 10% 50V CERM 402
C9533 0.1UF 10% 16V X5R 402
C9506 0.1UF 10% 16V X5R 402
L9505
120-OHM-0.3A-EMI
=PP3V3_S0_TMDS
PP3V3_S0_PVCC2_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9534 0.001UF 10% 50V CERM 402
C9535 0.1UF 10% 16V X5R 402
L9501
120-OHM-0.3A-EMI
=PP1V8_S0_TMDS
PP1V8_S0_TMDS_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9507 0.1UF 10% 16V X5R 402
C9508 0.001UF 10% 50V CERM 402
C9509 0.1UF 10% 16V X5R 402
C9510 0.001UF 10% 50V CERM 402
C9511 0.1UF 10% 16V X5R 402
C9512 0.001UF 10% 50V CERM 402
C9513 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN
L9500
120-OHM-0.3A-EMI
=PP1V8_S0_TMDS
PP1V8_S0_ANALOG_SDVO_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9500 0.001UF 10% 50V CERM 402
C9501 0.001UF 10% 50V CERM 402
C9502 0.1UF 10% 16V X5R 402
C9503 0.1UF 10% 16V X5R 402
C9504 10UF 20% 6.3V X5R 603
ONE 0.1UF AND 0.001UF FOR EACH PIN
R9507 49.9 1% 1/10W MF-LF 402
R9537 49.9 1% 1/10W MF-LF 402
TMDS_TX_P<0>
TMDS_TX<0>
TMDS_TX_N<0>
C9522 0.001UF 10% 50V CERM 402
R9508 49.9 1% 1/10W MF-LF 402
R9538 49.9 1% 1/10W MF-LF 402
TMDS_TX_P<1>
TMDS_TX<1>
TMDS_TX_N<1>
C9523 0.001UF 10% 50V CERM 402
R9509 49.9 1% 1/10W MF-LF 402
R9539 49.9 1% 1/10W MF-LF 402
TMDS_TX_P<2>
TMDS_TX<2>
TMDS_TX_N<2>
C9524 0.001UF 10% 50V CERM 402
R9510 49.9 1% 1/10W MF-LF 402
R9540 49.9 1% 1/10W MF-LF 402
TMDS_TX_CLK_P
TMDS_TX_CLK
TMDS_TX_CLK_N
NOSTUFF
C9526 10pF 5% 50V CERM 402
C9525 0.001UF 10% 50V CERM 402
NOSTUFF
C9527 10pF 5% 50V CERM 402
C9526,C9527 close to CHIP
MCH SDVO CHANNEL R,G,B,CLK SIGNAL TO TMDS CHIP
PLACE THE CAP NEAR THE NB SIDE
PEG_R2D_C_P<0>
PEG_R2D_C_N<0>
PEG_R2D_C_P<1>
PEG_R2D_C_N<1>
PEG_R2D_C_P<2>
PEG_R2D_C_N<2>
PEG_R2D_C_P<3>
PEG_R2D_C_N<3>
C9541 0.1UF 10% 16V X5R 402
C9542 0.1UF 10% 16V X5R 402
C9543 0.1UF 10% 16V X5R 402
C9544 0.1UF 10% 16V X5R 402
C9545 0.1UF 10% 16V X5R 402
C9546 0.1UF 10% 16V X5R 402
C9547 0.1UF 10% 16V X5R 402
C9548 0.1UF 10% 16V X5R 402
PP3V3_S0_ANALOG_SDVO_F
PP1V8_S0_ANALOG_SDVO_F
PP3V3_S0_PVCC2_TMDS_F
PP3V3_S0_PVCC1_TMDS_F
PP3V3_S0_ANALOG_TMDS_F
PP1V8_S0_TMDS_F
=PP3V3_S0_TMDS
C9521 0.1UF 10% 16V X5R 402
C9505 10UF 20% 6.3V X5R 603
U9500
SIL1362ACLU
LQFP
CRITICAL
SDVO RCVR CORE
DIFF SIG DATA
I2C MASTER INTER
CONFIG/ PRGRM
TEXT MODE
TMDS_SDR_P
TMDS_SDR_N
TMDS_SDG_P
TMDS_SDG_N
TMDS_SDB_P
TMDS_SDB_N
TMDS_SDC_P
TMDS_SDC_N
TMDS_INT_P
TMDS_INT_N
TMDS_EXT_RES
TMDS_RST_L
SDVO_CTRLCLK
SDVO_CTRLDATA
TMDS_HTPLG_R
TX0_P
TX0_N
TX1_P
TX1_N
TX2_P
TX2_N
TXC_P
TXC_N
EXT_SWING
TMDS_EXT_SWING
SCLDDC
SDADDC
TMDS_I2C_SCL
TMDS_I2C_SDA
TEST
PEG_D2R_P<1>
PEG_D2R_N<1>
C9519 0.1UF 10% 16V X5R 402
C9520 0.1UF 10% 16V X5R 402
TMDS CHIP SDVO INPUT INTERRUPT SIGNAL TO MCH
PLACE IT CLOSE TO CONNECTOR
=PP5V_S0_TMDS
D9500
BAV99DW-X-F
SOT-363
=PP2V5_S0_TMDS
R9501 3.3K 5% 1/16W MF-LF 402
R9502 3.3K 5% 1/16W MF-LF 402
R9500 2.2K 5% 1/16W MF-LF 402
TMDS_HTPLG
R9503 1K 5% 1/16W MF-LF 402
PP3V3_S0_ANALOG_TMDS_F
R9504 249 1% 1/16W MF-LF 402
=PP3V3_S0_TMDS
R9505 10K 5% 1/16W MF-LF 402
R9506 10K 5% 1/16W MF-LF 402
TMDS_I2C_SCL AND TMDS_I2C_SDA DON'T NEED TO CONNECT
NC
D9500
BAV99DW-X-F
SOT-363
PP5V_S0_DVIPORT
PP5V_S0_DVIPORT_D
EXTERNAL TMDS
SYNC_MASTER=GRAPHIC
SYNC_DATE=06/06/2005
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE INC.
SIZE D
DRAWING NUMBER 051-7370
REV. C
SCALE NONE
SHT 95 OF 98

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0227	155S0164	?	L9805,L9806,L9807	KEEP MAG.LAYER IN BOM

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

=PP3V3_S0_TMDS 64A6 68B1 68B2 68C8 68D8 69B7 69D1

Q9801 2N7002DW-X-F SOT-363

R9821 2.2K 5% 1/16W MF-LF 402

R9822 2.2K 5% 1/16W MF-LF 402

GPU_CRT_DDC_CLK 69B6

GPU_CRT_DDC_DATA 69B6

13B5 CRT_DDC_CLK

13B5 CRT_DDC_DATA

Q9801 2N7002DW-X-F SOT-363

TMDS(MINI DVI) INTERFACE

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

=PP3V3_S0_TMDS 64A6 68B1 68B2 68C8 68D8 69B7 69D5

C9860 0.1UF 20% 10V CERM 402

U9804 SN74LVC2G125DCU

13B5 CRT_HSYNC_R

R9860 39 5% 1/16W MF-LF 402

CRT_HSYNC_LS_R

CRT_HSYNC_LS

R9870 39 5% 1/16W MF-LF 402

VGA_HSYNC 69B4

NOSTUFF C9842 33PF 5% 50V CERM 402

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

U9804 SN74LVC2G125DCU

13B5 CRT_VSYNC_R

R9861 39 5% 1/16W MF-LF 402

CRT_VSYNC_LS_R

CRT_VSYNC_LS

R9871 39 5% 1/16W MF-LF 402

VGA_VSYNC 69B4

NOSTUFF C9843 33PF 5% 50V CERM 402

F9804 0.5AMP-13.2V SM-LF

68B7 64D3 =PP5V_S0_TMDS

VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

PP5V_S0_TMDS_FUSE

L9844 400-OHM-EMI SM-1

VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

PP5V_S0_DVIPORT 68A6 69B4

C9804 0.1UF 20% 10V CERM 402

=GND_CHASSIS_TMDS_UPPER 6C8 69A4

A 255 OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

13B5 CRT_IREF

R9869 255 1% 1/16W MF-LF 402

TV REFERENCE CURRENT,USES AN EXTERNAL RESISTOR OF 5K OHM 1% TO SET INTERNAL VOLTAGE LEVELS

13C5 TV_IREF

R9868 4.99K 1% 1/16W MF-LF 402

PP5V_S0_DVIPORT_D 68A8

DVI power DIODE on page 95 (D9500)

R9862 2.2K 5% 1/16W MF-LF 402

R9863 2.2K 5% 1/16W MF-LF 402

68A7 TMDS_HTPLG

C9808 0.001uF 10% 50V CERM 402

69D5 GPU_CRT_DDC_CLK

C9809 100pF 5% 50V CERM 402

69D5 GPU_CRT_DDC_DATA

C9812 100pF 5% 50V CERM 402

OMIT CRITICAL

J9801 MINI-DVI RT-TH

PP5V_S0_DVIPORT 68A6 69C3

TMDS_TX_CONN_P<2>

TMDS_TX_CONN_N<2>

TMDS_TX_CONN_P<1>

TMDS_TX_CONN_N<1>

TMDS_TX_CONN_P<0>

TMDS_TX_CONN_N<0>

TMDS_TX_CONN_CLK_P

TMDS_TX_CONN_CLK_N

NC NC

VGA_B 69C1 VGA_HSYNC

VGA_G 69C1 VGA_VSYNC

VGA_R

=GND_CHASSIS_TMDS_UPPER 6C8 69C3

=GND_CHASSIS_TMDS_DOWN 6A6

CRITICAL L9805 90-OHM-300MA 2012H

TMDS_TX_P<2> 68B2 68C3

TMDS_TX_N<2> 68B2 68C1

CRITICAL L9807 90-OHM-300MA 2012H

TMDS_TX_P<1> 68B2 68D3

TMDS_TX_N<1> 68B2 68D1

CRITICAL L9806 90-OHM-300MA 2012H

TMDS_TX_P<0> 68B2 68D3

TMDS_TX_N<0> 68B2 68D1

CRITICAL L9804 370-OHM-280MA SM1

TMDS_TX_CLK_P 68B2 68C3

TMDS_TX_CLK_N 68B2 68C1

C9834 3.3PF 0.25% 50V CERM 402

C9824 3.3PF 0.25% 50V CERM 402

C9820 3.3PF 0.25% 50V CERM 402

NOSTUFF C9821 0.1UF 10% 16V X5R 402

PLACE THE RESISTOR CLOSE TO GMCH

13C5 TV_DACA_OUT

13B5 CRT_BLUE

R9850 75 1% 1/16W MF-LF 402

R9851 75 1% 1/16W MF-LF 402

13C5 TV_IRTNA

13B5 CRT_BLUE_L

PLACE THE RESISTOR CLOSE TO GMCH

13C5 TV_DACB_OUT

13B5 CRT_GREEN

R9852 75 1% 1/16W MF-LF 402

R9853 75 1% 1/16W MF-LF 402

13C5 TV_IRTNB

13B5 CRT_GREEN_L

PLACE THE RESISTOR CLOSE TO GMCH

13C5 TV_DACC_OUT

13B5 CRT_RED

R9854 75 1% 1/16W MF-LF 402

R9855 75 1% 1/16W MF-LF 402

13C5 TV_IRTNC

13B5 CRT_RED_L

68B2 68B1 69D5 64A6 68D1 68C8 =PP3V3_S0_TMDS

C9839 0.1UF 10% 16V X5R 402

CRITICAL U9801 TS3V330 SOP

VCC 16

S1A 2 S2A 3 S1B 5 S2B 6 S1C 11 S2C 10 S1D 14 S2D 13

DA 4 DB 7 DC 9 DD 12 IN 1 EN_L 15

GND 8

EXT_COMPVID_B

EXT_Y_G

EXT_C_R

FL9800 LCFILTER SM-220MHZ-LF

FL9801 LCFILTER SM-220MHZ-LF

FL9802 LCFILTER SM-220MHZ-LF

NOSTUFF R9856 150 1% 1/16W MF-LF 402

NOSTUFF R9864 150 1% 1/16W MF-LF 402

NOSTUFF R9859 150 1% 1/16W MF-LF 402

=SB_GPIO22 6B2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0292	1	CONN,32P MINI-DVI RCPT,RA,MG3,LF	J9801	CRITICAL	NORMAL
514-0319	1	CONN,32P MINI-DVI RCPT,RA,BLACK,LF	J9801	CRITICAL	FANCY

MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7370	C
SCALE: NONE	SHT 98 OF 98	