

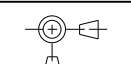
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
D		412039	PRODUCTION RELEASED	11/29/05	?

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table Of Contents	N/A	N/A
2	2	Board Information	N/A	N/A
3	3	System Block Diagram	N/A	N/A
4	4	Power Block Diagram	N/A	N/A
5	5	Revision History	N/A	N/A
6	6	Q16C Pin Swaps	N/A	N/A
7	7	Functional Test Points	N/A	N/A
8	8	I2C Connections	N/A	N/A
9	9	JTAG Connections	N/A	N/A
10	10	Power Synonyms	N/A	N/A
11	11	Signal Synonyms	N/A	N/A
12	12	Power Inputs	N/A	N/A
13	13	Battery Charger	N/A	N/A
14	14	12.8V PBUS/PMU Supplies	N/A	N/A
15	15	5V/3.3V Supplies	N/A	N/A
16	16	1.8V/1.5V Supplies	N/A	N/A
17	17	2.5V Supply	N/A	N/A
18	19	Vesta Power & Misc	N/A	N/A
19	21	I2 Power	N/A	N/A
20	22	I2 Power Supplies	N/A	N/A
21	23	I2 Supplemental	N/A	N/A
22	24	I2 Miscellaneous	N/A	N/A
23	25	PCI Clock Buffer	N/A	N/A
24	26	LEDs/Reset/Debug	N/A	N/A
25	27	Power Management Unit (PMU05)	N/A	N/A
26	29	Power Sequencing	N/A	N/A
27	30	Fan Controller	N/A	N/A
28	31	ALS Support	N/A	N/A
29	32	Sudden Motion Sensor	N/A	N/A
30	33	Q16C Internal I/O I	N/A	N/A
31	34	Q16C Internal I/O II	N/A	N/A
32	35	I2 Processor Interface	N/A	N/A
33	36	A8 MaxBus (CPU0)	MULLET	08/02/2005
34	37	A8 Configuration Straps	MULLET	08/02/2005
35	38	A8 Power (CPU0)	MULLET	08/02/2005
36	39	CPU VCore Supply	N/A	N/A
37	46	CPU AVDD Supply	N/A	N/A
38	47	I2 Memory Interface	N/A	N/A
39	48	Memory Series Termination	N/A	N/A
40	50	DDR2 SO-DIMM Slot A	N/A	N/A

PDF	CSA	CONTENTS	SYNC MASTER	DATE
41	52	DDR2 SO-DIMM Slot B	N/A	N/A
42	55	M11 Frame Buffer Constraints	N/A	N/A
43	56	I2 AGP Interface	N/A	N/A
44	57	GPU (M11) AGP Interface	N/A	N/A
45	58	GPU VCore Supply	N/A	N/A
46	59	GPU (M11) Core Power	N/A	N/A
47	60	GPU (M11) I/O Power	N/A	N/A
48	61	GPU (M11) Frame Buffer I/F	N/A	N/A
49	62	GPU Frame Buffer A	N/A	N/A
50	63	GPU Frame Buffer B	N/A	N/A
51	64	GPU (M11) GPIOs/Straps	N/A	N/A
52	65	GPU (M11) Clocks/Misc	N/A	N/A
53	66	GPU (M11) DVI/DAC Outputs	N/A	N/A
54	67	Lower TMDS Transmitter	N/A	N/A
55	68	Upper TMDS Transmitter	N/A	N/A
56	69	Internal Display Conns	N/A	N/A
57	70	External Display Conns	N/A	N/A
58	71	BootROM	N/A	N/A
59	72	I2 PCI Interface	N/A	N/A
60	73	Q85 Airport/BT Connector	N/A	N/A
61	74	Cardbus	N/A	N/A
62	75	NEC USB2	N/A	N/A
63	81	I2 UATA Interface	N/A	N/A
64	82	HDD/ODD Connectors	N/A	N/A
65	84	I2 Ethernet Interface	N/A	N/A
66	85	Vesta Ethernet PHY	N/A	N/A
67	86	Ethernet Connector	N/A	N/A
68	88	I2 FireWire Interface	N/A	N/A
69	89	Vesta FireWire PHY	N/A	N/A
70	90	FireWire Ports	N/A	N/A
71	91	FireWire Series Term	N/A	N/A
72	92	I2 USB Interface	N/A	N/A
73	93	NEC USB2 Interface	N/A	N/A
74	100	Audio Board Connector	N/A	N/A
75	110	Spacing & Physical Constraints	N/A	N/A
76	111	Spacing & Physical Constraints 2	N/A	N/A
77	112	Cross Reference Page		
78	113	Cross Reference Page		
79	114	Cross Reference Page		
80	115	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7001	1	SCHEM,MLB,Q16C	SCH1	CRITICAL	
820-1940	1	PCBF,MLB,Q16C	PCB1	CRITICAL	
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:UEB]	CRITICAL	EEE_UEB
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:UEC]	CRITICAL	EEE_UEC
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USK]	CRITICAL	EEE_USK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6MM	[EEE:USL]	CRITICAL	EEE_USL

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7001	REV. D
				SHT 1 OF 115	

D

D

C

C

B

B

A

A

Design-Specific Rules

TABLE_SPACING_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	BGA_P1MM	10	0.10 MM	1.25 MM	0.1 MM	12.5 MM
TABLE_SPACING_RULE	BGA_P2MM	20	0.20 MM	1.25 MM	0.1 MM	12.5 MM
TABLE_SPACING_RULE	DEFAULT	*	0.1 MM	2.5 MM	0.15 MM	10.0 MM

"1MM" area defined around BGAs to reduce DRCs caused by fan-out.
 "BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

TABLE_PHYSICAL_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_PHYSICAL_RULE	STANDARD	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_PHYSICAL_RULE	DEFAULT	*	Y	0.100 MM	0.100 mm
TABLE_PHYSICAL_RULE	DEFAULT	*	Y	0.100 MM	1.25 MM

Layer-specific rules for 90-ohm differential impedance

TABLE_SPACING_RULE	90_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.200 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	90_OHM_DIFF	*	2.5 MM	0.200 MM	2.5 MM	1.0 MM

Layer-specific rules for 100-ohm differential impedance

TABLE_PHYSICAL_RULE	90_OHM_DIFF	TOP,BOTTOM	Y	0.118 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	90_OHM_DIFF	*	Y	0.125 MM	0.1 MM	5 MM

Layer-specific rules for 110-ohm differential impedance

TABLE_SPACING_RULE	110_OHM_DIFF	TOP,BOTTOM	2.5 MM	0.330 MM	2.5 MM	1.0 MM
TABLE_SPACING_RULE	110_OHM_DIFF	*	2.5 MM	0.330 MM	2.5 MM	1.0 MM

Layer-specific rules for 60-ohm single-ended impedance

TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE
TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM <td>=50_OHM_SE</td> <td>=50_OHM_SE</td>	=50_OHM_SE	=50_OHM_SE

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM <td>0.100 MM <td>1.25 MM</td> </td>	0.100 MM <td>1.25 MM</td>	1.25 MM

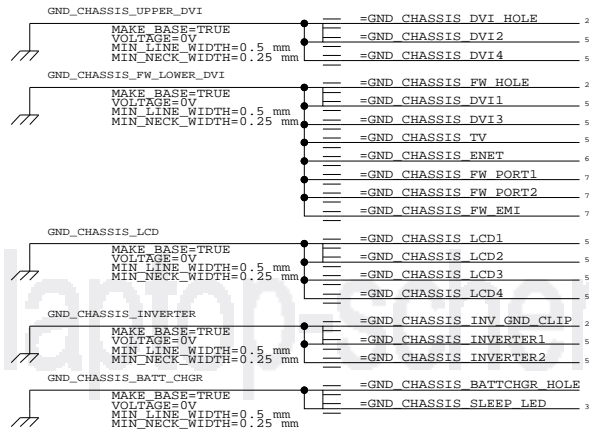
Layer-specific rules for 110-ohm differential impedance

TABLE_PHYSICAL_RULE	110_OHM_DIFF	TOP,BOTTOM	Y	0.080 MM	0.1 MM	5 MM
TABLE_PHYSICAL_RULE	110_OHM_DIFF	*	Y	0.085 MM <td>0.1 MM <td>5 MM</td> </td>	0.1 MM <td>5 MM</td>	5 MM

Portable-specific Override Rules

TABLE_SPACING_RULE	AGP	201	*	0.2 MM			
TABLE_SPACING_RULE	AGP	201	*	0.2 MM			
TABLE_SPACING_RULE	AGP_STB	251	*	0.25 MM			
TABLE_SPACING_RULE	VGA	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_SPACING_RULE	TV	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT
TABLE_PHYSICAL_RULE	VGA	*		=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE
TABLE_PHYSICAL_RULE	TV	*		=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE

CHASSIS GND CONNECTIONS



Layer-specific rules for 60-ohm single-ended impedance

TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE
TABLE_PHYSICAL_RULE	60_OHM_SE	*	Y	0.076 MM <td>=50_OHM_SE</td> <td>=50_OHM_SE</td>	=50_OHM_SE	=50_OHM_SE

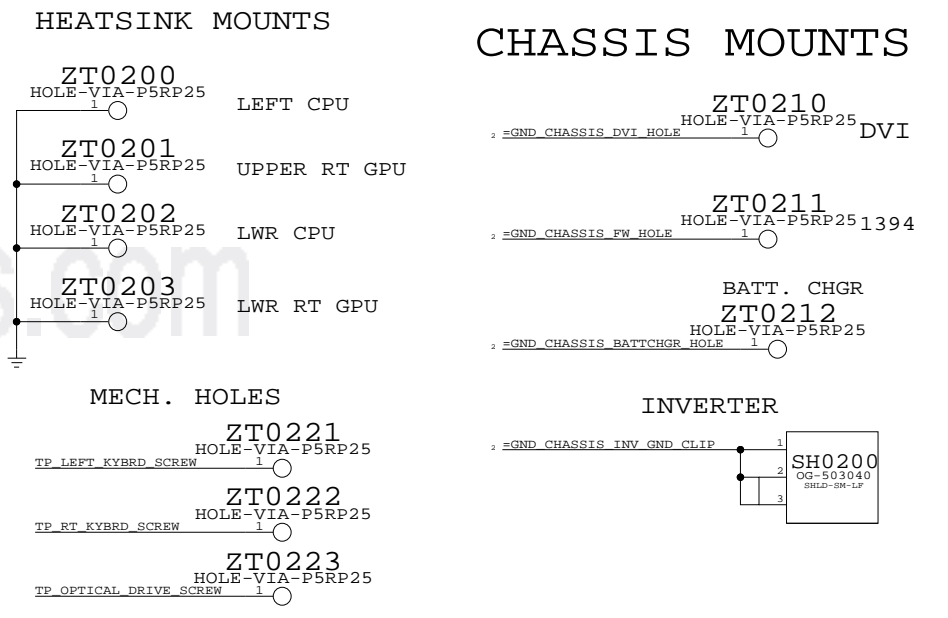
Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM
TABLE_SPACING_RULE	50_OHM_SE	*	Y	0.100 MM <td>0.100 MM <td>1.25 MM</td> </td>	0.100 MM <td>1.25 MM</td>	1.25 MM

NO_TEST Properties

1778_ITH_RC	45	NO_TEST=TRUE	TP_VESTA_DNC_E9	18	NO_TEST=TRUE
1778_VRNG	45	NO_TEST=TRUE	TP_VESTA_F1000	66	NO_TEST=TRUE
GPU_DVOD_R<18>	6 53	NO_TEST=TRUE	TP_VESTA_PHYA<0>	66	NO_TEST=TRUE
LTC3412_RUNSS	17	NO_TEST=TRUE	TP_VESTA_REGSEN2	18	NO_TEST=TRUE
TMDS_CONN_CLKP	57	NO_TEST=TRUE	TP_VESTA_SPD0	66	NO_TEST=TRUE
TP_NEC_SMC	62	NO_TEST=TRUE	USB_NEC_BT_N	6 31	NO_TEST=TRUE
TP_NEC_SMI_L	62	NO_TEST=TRUE	USB_NEC_N<1>	73	NO_TEST=TRUE
TP_NEC_SRCLK	62	NO_TEST=TRUE	USB_NEC_N<2>	73	NO_TEST=TRUE
TP_USB2_PWREN<0>	73	NO_TEST=TRUE	USB_NEC_N<3>	73	NO_TEST=TRUE
TP_USB2_PWREN<2>	73	NO_TEST=TRUE	USB_NEC_P<0>	73	NO_TEST=TRUE
TP_USB2_PWREN<3>	73	NO_TEST=TRUE	USB_NEC_P<1>	73	NO_TEST=TRUE
UATA_DD_R<0>	6 43	NO_TEST=TRUE	SI_TMDS_DN<5>	55	NO_TEST=TRUE
UATA_DD_R<8>	6 43	NO_TEST=TRUE	SI_TMDS_DN<4>	55	NO_TEST=TRUE
UATA_DD_R<10>	6 43	NO_TEST=TRUE	SI_TMDS_DP<3>	55	NO_TEST=TRUE
UATA_DA_R<0>	6 43	NO_TEST=TRUE	SI_TMDS_DN<2>	54	NO_TEST=TRUE
UATA_DA_R<1>	6 43	NO_TEST=TRUE	SI_TMDS_DN<1>	54	NO_TEST=TRUE
UATA_DA_R<1>	6 43	NO_TEST=TRUE	SI_TMDS_DN<0>	54	NO_TEST=TRUE
			SI_TMDS_CLKP	54	NO_TEST=TRUE

BOARD HOLES



BOARD STACK-UP AND CONSTRUCTION

SEE BOARD FILE FOR DETAILED INFORMATION
 CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA

Layer	Material	Thickness
1	SIGNAL (1/2 OZ + COPPER PLATING)	
2	PREPREG	
3	GROUND (1/2 OZ)	
4	CORE	
5	SIGNAL (1/2 OZ)	
6	PREPREG	
7	GROUND (1/2 OZ)	
8	CUT POWER PLANE (1 OZ)	
9	CORE	
10	SIGNAL (1/2 OZ)	
11	PREPREG	
12	GROUND (1/2 OZ)	
13	SIGNAL (1/2 OZ + COPPER PLATING)	

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7338	PCBA, MLB, BESTMHZ, 1.67, VRAM_S, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_USB, GPU_LF, VRAM_SAMSUNG, gCommon
630-7339	PCBA, MLB, BESTMHZ, 1.67, VRAM_H, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_UC, GPU_LF, VRAM_HYNIX, gCommon
630-7445	PCBA, MLB, BESTMHZ, GPU_EUT, VRAM_S, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_USK, GPU_EUTECTIC, VRAM_SAMSUNG, gCommon
630-7446	PCBA, MLB, BESTMHZ, GPU_EUT, VRAM_H, PB15	COMMON, ALTERNATE, gQ16C, gQ16C_BST, EEE_USL, GPU_EUTECTIC, VRAM_HYNIX, gCommon

BOM GROUP	BOM OPTIONS
gCommon	5V_HD_LOGIC, BACKUP_BATT, CPU_A7PM, I2_FW_BETA, I2_MAXBUS_50OHM, MAXBUS_1V8, gCommon1
gCommon1	MMM_ACCEL_KIONIX, GPU_PWRPLAY, GPU_SS, GPU_LVDDR_2V8, GPU_MEMIO_1V8, gCommon2
gCommon2	I2_REV1_NOT, I2_MAXBUS_FBCLK_MATCHED, I2_AGP_FBCLK_MATCHED, I2_PCI_FBCLK_MATCHED, gCommon3
gCommon3	CPU_VCORE_2STATES, I2_MAXBUS_166MHZ, I2VCORE_1V5, I2VCORE_BURST, gCommon4
gCommon4	VESTA_PORT2_DISABLE, DVO_1V8, TMDS_DUAL, VCORE_OFFSET, VCORE_OFFSET_SW, gUSB
gUSB	USB2_NEC, USB1P1_NEC, TPAD_SEQ_PMU
gQ16C	Q16C_PARTS, BOOTROM_PROG, PMU_PROG, MAXBUS_TBEN_SYNC

gQ16C_BST	A7PM_1P67_LGA, CPU0_BUSRATIO_10.0X, CPU0_VCORE_1V28, CPU0_AVDD_1V28, Q16BST
gQ16C_BST	A7PM_1P67_LGA, CPU0_BUSRATIO_10.0X, CPU0_VCORE_1V28, CPU0_AVDD_1V28, Q16BST

Module Components

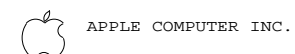
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0383	1	IC, ASIC, I2, REV1.2, NB/SB, 974 BGA	U2100	CRITICAL	
337S3135	1	IC, PMU05, BLANK, QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC, PMU05, V1, QFP	U2700	CRITICAL	PMU_PROG
337S3276	1	IC, A7PM, R1.6, 1.67GHZ, LGA, 1.28V, 23W, 85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3077	1	IC, A8, xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC, GPU, M11P	U5700	CRITICAL	GPU_LF
338S0299	1	IC, GPU, M11P, EUTECTIC	U5700	CRITICAL	GPU_EUTECTIC
335S0088	1	BOOTROM, BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1736	1	IC, BOOTROM, B, Q16C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC, ASIC, VESTA, V1.3, LF	U8500	CRITICAL	
333S0317	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC, GDDR SDRAM, 2MX32X4, 300MHZ, LF FBGA144	U6200, U6250, U6300, U6350	CRITICAL	VRAM_HYNIX

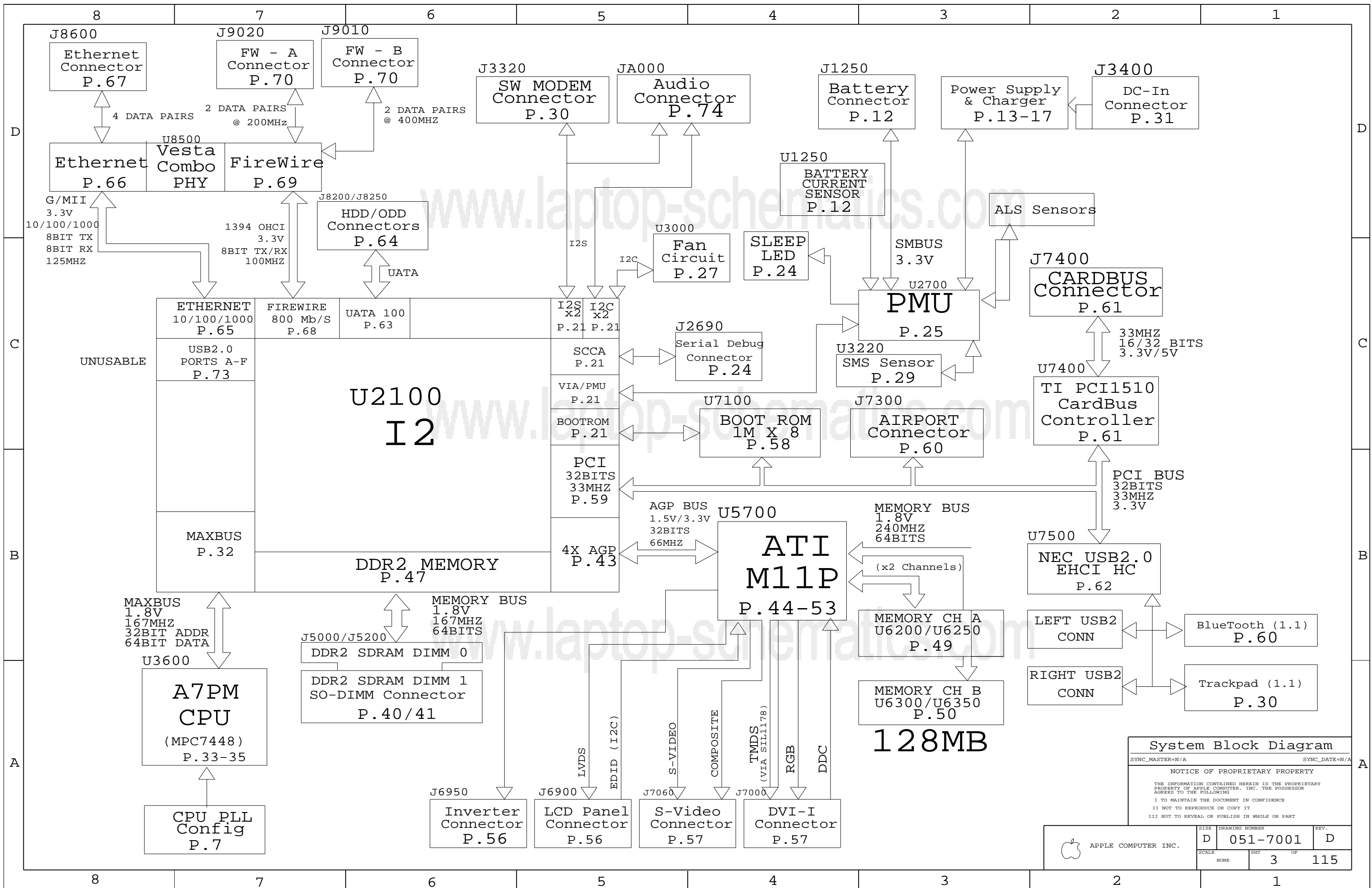
PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0388	343S0356		U8500	v1.4 is alt to v1.3
337S3162	337S3276	A7PM_1P67_LGA	U3600	v1.5 is alt to v1.6

Board Information

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SIZE	DRAWING NUMBER	REV.
D	051-7001	D
SCALE	SHT	OF
NONE	2	115





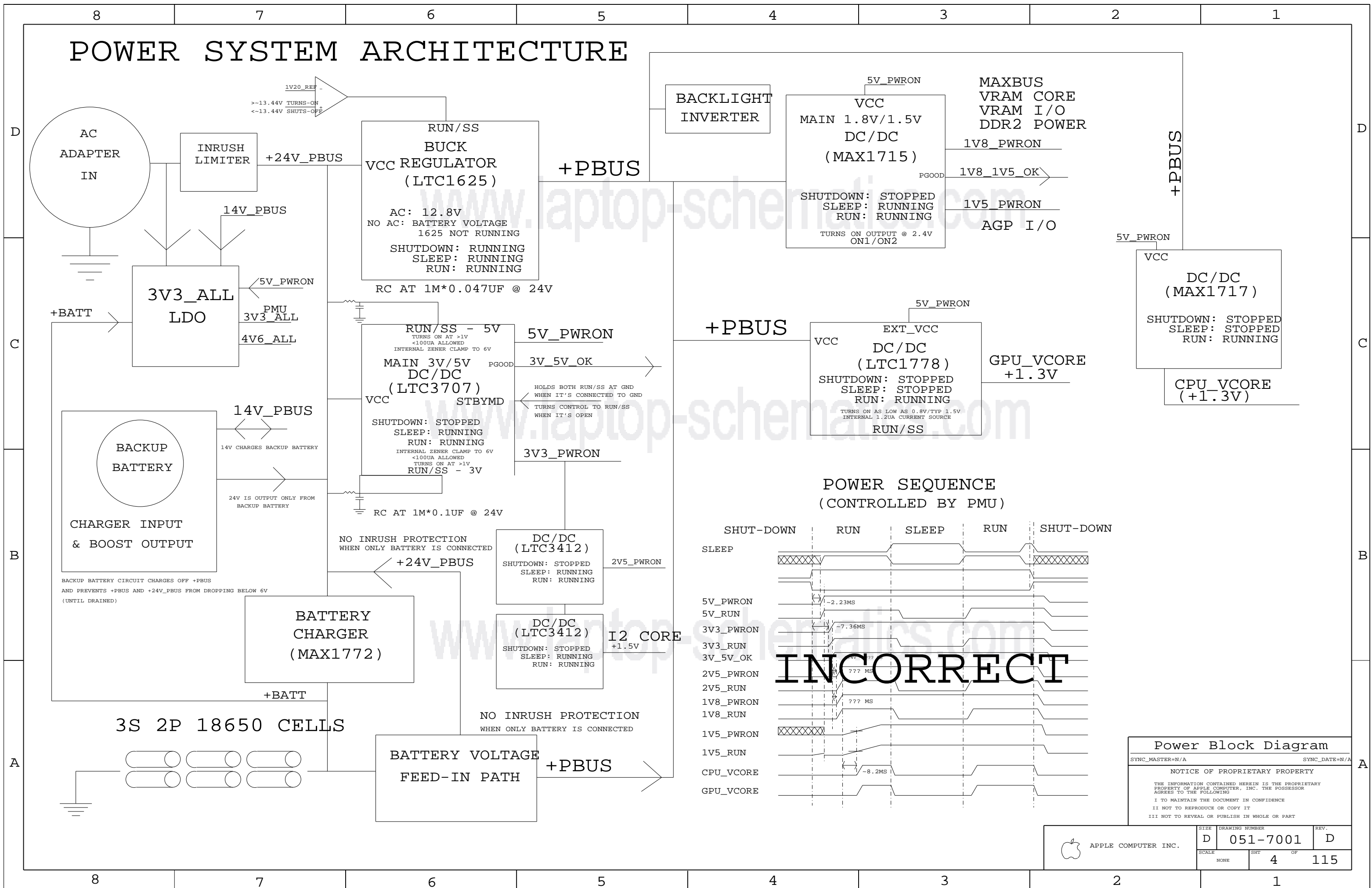
System Block Diagram

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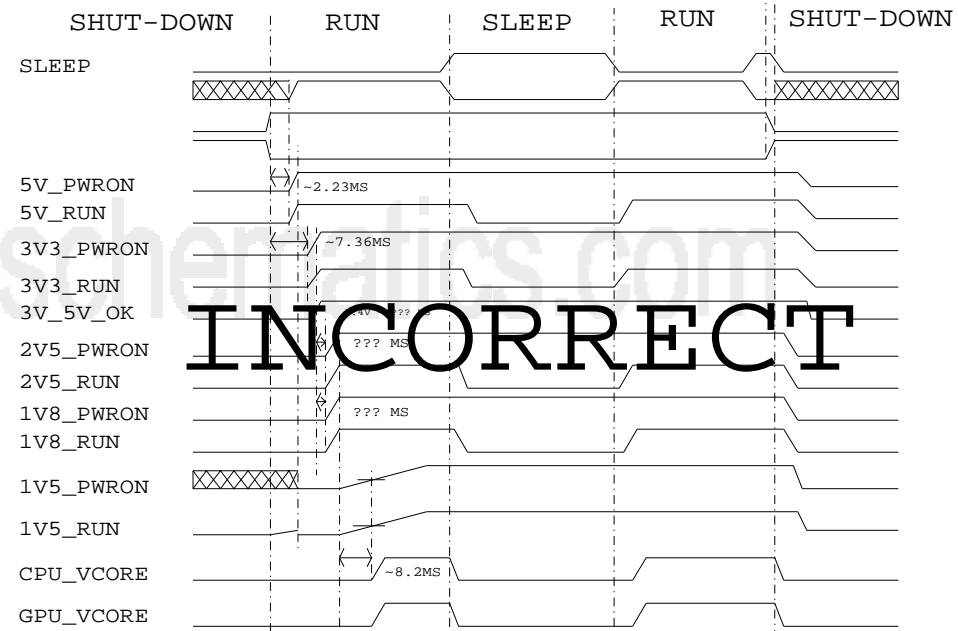
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	D	051-7001	D
SCALE	SHT OF		REV.
NONE	3 OF		115

POWER SYSTEM ARCHITECTURE



POWER SEQUENCE (CONTROLLED BY PMU)



Power Block Diagram
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHT OF		REV.
NONE	4 OF		115

REVISION HISTORY

EVT

- 04/04/2005 - Beginning revision history
- 04/06/2005 - Made DDR2 and FB pin swaps as requested by CM
- 04/06/2005 - Modem connector moved to non-shared page
- 04/06/2005 - Changed R2941 to level shift/pass FET to correct GPU VCore and CPU Vcore power sequencing
- 04/06/2005 - Made additional FB pin swaps
- 04/11/2005 - Changed DDR2 CS/CKE RPAKs to RPAK2P (added RP4871, RP4876)
- 04/11/2005 - Implemented more DDR2 pin swaps
- 04/11/2005 - Implemented FireWire pin swaps
- 04/11/2005 - Added remaining spacing and physical rule tables
- 04/11/2005 - Added upper LVDS channel to function0 test page
- 04/11/2005 - Changed battery sense resistor to 0.006 ohm (R1250)
- 04/11/2005 - Stuffed R2903 to disable FW port power when off on AC
- 04/12/2005 - Changed audio test to XSR (CA035, CA050, CA051)
- 04/12/2005 - Corrected MIN LINE WIDTH properties on P3V3_PWRON
- 04/12/2005 - Corrected TMS DIFFERENTIAL PAIR properties at DVI connector
- 04/12/2005 - Reduced MIN NECK WIDTH property on GPU to 0.2 mm for TMS parts
- 04/12/2005 - Corrected line and neck width properties
- 04/12/2005 - Added high/low swing BOMPTIONS for DVO on SI TMS parts
- 04/13/2005 - Added 1.5V DVO option to GPU
- 04/13/2005 - Removed series R isolating VG from digital ground on FW ports (per design guide)
- 04/15/2005 - Moved FB series R to page 61
- 04/18/2005 - Added VREF inputs and decoupling on GPU
- 04/18/2005 - Corrected system problems on PMU port usage
- 04/19/2005 - Added NO_RST core properties
- 04/19/2005 - Corrected ENER power rail to PWRON from RUN (for Wake-on-LAN)
- 04/20/2005 - Added page 2 and modified pages 11, 35, 81 for design specific pin swaps
- 04/20/2005 - Changed R5880 to 6.34k to take GPU Vcore to 1.3V/1.05V
- 04/21/2005 - Corrected STOP_AGP_L net name (hooked to I2 now) and removed redundant pullup
- 04/22/2005 - Added external pullups to replace missing internal I2 pullups
- 04/22/2005 - Added ADC caps at PMU
- 04/22/2005 - Corrected logic change for Vesta FireWire crystal (to 18pf)
- 04/22/2005 - Disconnected FW_POWERDOWN from Vesta LPWR_1394 pin
- 04/22/2005 - Corrected pull-down resistor value for 0.006 ohm battery current sense
- 05/03/2005 - Added 22uF CPU Vcore caps to 330 uF caps
- 05/03/2005 - Changed GPU FB MYREFs into separate dividers
- 05/03/2005 - Rinswapped UATA I/F, DVO I/F, USB pull-downs
- 05/04/2005 - Added extra cap at input to I2 USBVDD
- 05/05/2005 - Added pull-downs to unused HSD and QDD connectors
- 05/05/2005 - Added PDIAS signal between HSD and QDD connectors
- 05/10/2005 - Various Pb-free component replacements
- 05/13/2005 - Various Pb-free component replacements
- 05/13/2005 - Rinswaps for I2 RPAKs to match up with Q41C style layout
- 05/16/2005 - Various Pb-free component replacements
- 05/19/2005 - Added Hynix VRAM option and P3As
- 05/19/2005 - Various Pb-free component replacements
- 05/20/2005 - Added HSDN sync circuit
- 05/21/2005 - Various Pb-free component replacements
- 05/21/2005 - Added DSP signal between HSD and QDD connectors
- 05/21/2005 - Corrected AGP_INT_L connection between I2 and GPU
- 05/23/2005 - Corrected VSA sync connections at GPU
- 05/23/2005 - Released as REV 01 for Pre-EVT/EVT
- 08/25/2005 - Added USB controller
- 08/25/2005 - Added ZDB clock buffer for PCI clocks
- 08/25/2005 - Various Pb-free component replacements
- 08/25/2005 - Removed SMC PIC microcontroller
- 08/25/2005 - Added 2 0.1uF caps to GPU Vcore regulator output
- 08/25/2005 - Corrected USB diff pair and spacing/physical rules on port connections
- 06/01/2005 - Corrected FireWire VP caps to 50V
- 06/01/2005 - Various Pb-free replacements
- 06/02/2005 - Released as REV 02 for EVT
- 06/03/2005 - Changed CPU clock series Rs to 0 ohms
- 06/03/2005 - Released as REV 03 for EVT
- 06/07/2005 - Updated BOM options on CPU Vcore and AVDD for 1.22, 1.30, and 1.33V
- 06/07/2005 - Corrected alternate errors and a leaded table item
- 06/07/2005 - Released as REV 04 for EVT

DVT

- 06/28/2005 - Added 10K pullup to VIA_REQ_L
- 06/28/2005 - Changed R2941 to level shift/pass FET to correct GPU VCore and CPU Vcore power sequencing
- 06/28/2005 - Moved R2943 to SVS_PWRSEN_L_L to correct trackpad power state in sleep
- 06/28/2005 - Moved R2943 to SW to correct pumpup problem in sleep
- 07/06/2005 - Changed to USB1P_NP_BOMPTION
- 07/06/2005 - Various Pb-free replacements
- 07/06/2005 - Changed TMS drive strength resistors to 301 ohm, which was built at EVT
- 07/08/2005 - Added FET to allow PMU control of trackpad power sequencing
- 07/09/2005 - Added resistor mux for I2's MAXBUS I/O rail (PWRON vs RUN)
- 07/09/2005 - Changed CPU Vcore to 2-states only (no MUX)
- 07/09/2005 - Removed I2's connection to TSEN (leakage path)
- 07/09/2005 - Removed 1.5GHz config
- 07/14/2005 - Changed 75MHz crystal to new APN specifying 1uW drive parts
- 07/14/2005 - Added line width constraints to LFC1625 and CPU Vcore gate nodes
- 07/18/2005 - Added external 10K pullups in parallel with all I2 internal pullups
- 07/18/2005 - Changed R1702 series R value to 19.2 ohm
- 07/18/2005 - Added 150 ohm pull-downs to FW_CTL lines at Vesta
- 07/19/2005 - Changed TMS transmitter ferrites to part with higher current rating (1.5A)
- 07/19/2005 - Added BOMPTIONS for and stuffed CPU Vcore at 1.28V and 1.30V
- 07/19/2005 - Added audio mute sequencing FETs
- 07/19/2005 - Moved UATA_DSTR0BE cap to other side of series resistor
- 07/22/2005 - Released as REV 06 for DVT
- 07/22/2005 - Changed all external I2 GPIO pullups to 10K
- 07/25/2005 - Stuffed R2942, R2942, R2942 to correct I2 2.5V pullup problem
- 07/25/2005 - Replaced 371S0299 with 371S0300
- 07/25/2005 - Swapped I2_MAXBUS 130HM and I2_MAXBUS 500HM BOMPTIONS
- 07/26/2005 - Changed to Vesta v1.4 as primary, U850U Vesta v1.3 as alternate
- 07/26/2005 - Changed PCI_ZDB output series term 5002 ohms
- 07/29/2005 - Swapped locations of C2500 and C2501
- 07/29/2005 - Released as REV 07 for DVT

Pre-PVT

- 08/02/2005 - Added R0985 10K pull down on JTAG_CPU0_TCK
- 08/02/2005 - Added R3773 10K pull down on CPU0_EXT_QUAL on Mullet and sync'd
- 08/05/2005 - Changed R4947 to NO series for R0P
- 08/05/2005 - Changed C1730 and C2205 to 2200pF
- 08/05/2005 - Changed C1730 to 5.6uF
- 08/05/2005 - Changed C1700 and C1701 and C2215 and C2216 to 47uF
- 08/05/2005 - Changed R1720 and R2205 to 7.5k
- 08/05/2005 - Changed C3940-C3947 to 1206 ceramic caps
- 08/17/2005 - Changed power supply jumpers to shorts
- 08/17/2005 - Added five ceramic caps to Vcore supply
- 08/17/2005 - Changed to 60 schotky to reduce reverse leakage
- 08/18/2005 - Changed R2958 to 10K for improved power sequencing timing
- 08/22/2005 - Added FETs to reduce leakage onto Vesta rails
- 08/24/2005 - Changed C6600-P6601 to 1uF due to insertion of FET
- 08/24/2005 - Changed R5822 to 100K for power sequence improvement
- 08/24/2005 - No stuffed R2959 for power sequence improvement
- 08/24/2005 - Released as REV 08 for Pre-PVT

PVT

- 08/29/2005 - (051-6929) Released as REV A for PVT
- 08/31/2005 - Stuffed R8429 with 10K 5% to ensure MDIO logic levels
- 08/31/2005 - Changed R8429 to unused level 109H
- 09/02/2005 - Changed ML to 820-1940 which corrects tolerance on DIMM conn holes
- 09/09/2005 - Changed C1804-C2006 to 0.033uF for SWS filtering improvements
- 09/09/2005 - (051-7001) Released as REV A for Production

D

SYNC_MASTER=N/A SYNC_DATE=N/A


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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	
NONE	5	115	

8

7

6

5

4

3

2

1

I2S Series Rs

MAKE_BASE=TRUE	22	I2S0_SB_TO_DEV.DTO_R	==	=RP1150P1	11	11	=RP1150P8	I2S0_SB_TO_DEV.DTO	7	74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_BITCLK_R	==	=RP1150P2	11	11	=RP1150P7	I2S0_BITCLK	7	74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_MCLK_R	==	=RP1150P3	11	11	=RP1150P6	I2S0_MCLK	7	74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_SYNC_R	==	=RP1150P4	11	11	=RP1150P5	I2S0_SYNC	7	74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SB_TO_DEV.DTO_R	==	=RP1151P1	11	11	=RP1151P8	I2S1_SB_TO_DEV.DTO	30		MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SYNC_R	==	=RP1151P2	11	11	=RP1151P7	I2S1_SYNC	30		MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_MCLK_R	==	=RP1151P3	11	11	=RP1151P6	I2S1_MCLK	30		MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_BITCLK_R	==	=RP1151P4	11	11	=RP1151P5	I2S1_BITCLK	30		MAKE_BASE=TRUE

Lower DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<16>	==	=RP6720P1	54	54	=RP6720P8	GPU_DVOD<16>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<4>	==	=RP6720P2	54	54	=RP6720P7	GPU_DVOD<4>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<7>	==	=RP6720P3	54	54	=RP6720P6	GPU_DVOD<7>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<6>	==	=RP6720P4	54	54	=RP6720P5	GPU_DVOD<6>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<11>	==	=RP6721P1	54	54	=RP6721P8	GPU_DVOD<11>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<9>	==	=RP6721P2	54	54	=RP6721P7	GPU_DVOD<9>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<10>	==	=RP6721P3	54	54	=RP6721P6	GPU_DVOD<10>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_HSYNC_R	==	=RP6721P4	54	54	=RP6721P5	GPU_DVO_HSYNC	54	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<3>	==	=RP6722P1	54	54	=RP6722P8	GPU_DVOD<3>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<5>	==	=RP6722P2	54	54	=RP6722P7	GPU_DVOD<5>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<13>	==	=RP6722P3	54	54	=RP6722P6	GPU_DVOD<13>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<12>	==	=RP6722P4	54	54	=RP6722P5	GPU_DVOD<12>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<2>	==	=RP6723P1	54	54	=RP6723P8	GPU_DVOD<2>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<1>	==	=RP6723P2	54	54	=RP6723P7	GPU_DVOD<1>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<0>	==	=RP6723P3	54	54	=RP6723P6	GPU_DVOD<0>	54		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<14>	==	=RP6723P4	54	54	=RP6723P5	GPU_DVOD<14>	55		MAKE_BASE=TRUE

UATA Series Rs

MAKE_BASE=TRUE	63	UATA_DD_R<12>	==	=RP8150P1	63	63	=RP8150P8	UATA_DD<12>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_CS0_L	==	=RP8150P2	63	63	=RP8150P7	UATA_CS0_L	7	63	64	MAKE_BASE=TRUE (IDE_CS1FX_L)
MAKE_BASE=TRUE	63	UATA_DD_R<14>	==	=RP8150P3	63	63	=RP8150P6	UATA_DD<14>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<11>	==	=RP8150P4	63	63	=RP8150P5	UATA_DD<11>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<7>	==	=RP8151P1	63	63	=RP8151P8	UATA_DD<7>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<2>	==	=RP8151P2	63	63	=RP8151P7	UATA_DD<2>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<3>	==	=RP8151P3	63	63	=RP8151P6	UATA_DD<3>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<15>	==	=RP8151P4	63	63	=RP8151P5	UATA_DD<15>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<9>	==	=RP8152P1	63	63	=RP8152P8	UATA_DD<9>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<4>	==	=RP8152P2	63	63	=RP8152P7	UATA_DD<4>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<6>	==	=RP8152P3	63	63	=RP8152P6	UATA_DD<6>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<5>	==	=RP8152P4	63	63	=RP8152P5	UATA_DD<5>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DA_R<2>	==	=RP8153P1	63	63	=RP8153P8	UATA_DA<2>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<8>	==	=RP8153P2	63	63	=RP8153P7	UATA_DD<8>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<10>	==	=RP8153P3	63	63	=RP8153P6	UATA_DD<10>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DA_R<0>	==	=RP8153P4	63	63	=RP8153P5	UATA_DA<0>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<13>	==	=RP8154P1	63	63	=RP8154P8	UATA_DD<13>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<0>	==	=RP8154P2	63	63	=RP8154P7	UATA_DD<0>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<1>	==	=RP8154P3	63	63	=RP8154P6	UATA_DD<1>	7	63	64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DA_R<1>	==	=RP8154P4	63	63	=RP8154P5	UATA_DA<1>	7	63	64	MAKE_BASE=TRUE

Upper DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVO_DE_R	==	=RP6821P1	55	55	=RP6821P8	GPU_DVO_DE	54	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_VSYNC_R	==	=RP6821P2	55	55	=RP6821P7	GPU_DVO_VSYNC	54	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_CLKP_R	==	=RP6821P3	55	55	=RP6821P6	GPU_DVO_CLKP	54	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<8>	==	=RP6821P4	55	55	=RP6821P5	GPU_DVOD<8>	54	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<21>	==	=RP6822P1	55	55	=RP6822P8	GPU_DVOD<21>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<19>	==	=RP6822P2	55	55	=RP6822P7	GPU_DVOD<19>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<17>	==	=RP6822P3	55	55	=RP6822P6	GPU_DVOD<17>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<15>	==	=RP6822P4	55	55	=RP6822P5	GPU_DVOD<15>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<20>	==	=RP6823P1	55	55	=RP6823P8	GPU_DVOD<20>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<22>	==	=RP6823P2	55	55	=RP6823P7	GPU_DVOD<22>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<23>	==	=RP6823P3	55	55	=RP6823P6	GPU_DVOD<23>	55		MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<18>	==	=RP6823P4	55	55	=RP6823P5	GPU_DVOD<18>	55		MAKE_BASE=TRUE

MAXBUS Pullups

MAKE_BASE=TRUE	33	MAXBUS_TS_L	==	=RP3510P1	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BG_L	==	=RP3510P2	32							
MAKE_BASE=TRUE	33	MAXBUS_CPU0_DBG_L	==	=RP3510P3	32							
MAKE_BASE=TRUE	32	NC_MAXBUS_I2_TBNEN NO_TEST=YES	==	=RP3510P4	32							
MAKE_BASE=TRUE	33	MAXBUS_CPU0_BG_L	==	=RP3511P1	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_HIT_L	==	=RP3511P2	32							
MAKE_BASE=TRUE	33	MAXBUS_CPU0_HIT_L	==	=RP3511P3	32							
MAKE_BASE=TRUE	33	MAXBUS_CPU0_BR_L	==	=RP3511P4	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BR_L	==	=RP3512P1	32							
MAKE_BASE=TRUE	33	MAXBUS_TA_L	==	=RP3512P2	32							
MAKE_BASE=TRUE	34	MAXBUS_CPU0_INT_L	==	=RP3512P3	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_INT_L	==	=RP3512P4	32							
MAKE_BASE=TRUE	33	MAXBUS_CPU0_DRDY_L	==	=RP3513P2	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DRDY_L	==	=RP3513P3	32							
MAKE_BASE=TRUE	33	MAXBUS_AACK_L	==	=RP3513P4	32							
MAKE_BASE=TRUE	33	MAXBUS_ARTRY_L	==	=RP3514P1	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DBG_L	==	=RP3514P2	32							
MAKE_BASE=TRUE	33	MAXBUS_TEAL_L	==	=RP3514P3	32							

AGP Pullups

MAKE_BASE=TRUE	44	AGP_TRDY_L	==	=RP5610P1	43							
MAKE_BASE=TRUE	44	AGP_IRDY_L	==	=RP5610P2	43							
MAKE_BASE=TRUE	44	AGP_REQ_L	==	=RP5610P3	43							
MAKE_BASE=TRUE	44	AGP_RBF_L	==	=RP5610P4	43							
MAKE_BASE=TRUE	44	AGP_FRAME_L	==	=RP5611P1	43							
MAKE_BASE=TRUE	44	AGP_DEVSEL_L	==	=RP5611P2	43							
MAKE_BASE=TRUE	44	AGP_STOP_L	==	=RP5611P3	43							
MAKE_BASE=TRUE	44	AGP_GNT_L	==	=RP5611P4	43							

USB Pulldowns

MAKE_BASE=TRUE	72	USB_I2_BT_P	==	=RP9210P8	11							
MAKE_BASE=TRUE	72	USB_I2_BT_N	==	=RP9210P7	11							
MAKE_BASE=TRUE	72	USB2_I2_RIGHT_PORT_N	==	=RP9210P6	11							
MAKE_BASE=TRUE	72	USB2_I2_RIGHT_PORT_P	==	=RP9210P5	11							
MAKE_BASE=TRUE	72	USB2_I2_P<1>	==	=RP9211P8	72							
MAKE_BASE=TRUE	72	USB2_I2_N<1>	==	=RP9211P7	72							
MAKE_BASE=TRUE	72	USB2_I2_N<3>	==	=RP9211P6	72							
MAKE_BASE=TRUE	72	USB2_I2_P<3>	==	=RP9211P5	72							
MAKE_BASE=TRUE	72	USB_I2_TPAD_N	==	=RP9212P8	11							
MAKE_BASE=TRUE	72	USB_I2_TPAD_P	==	=RP9212P7	11							
MAKE_BASE=TRUE	72	USB2_I2_LEFT_PORT_P	==	=RP9212P6	11							
MAKE_BASE=TRUE	72	USB2_I2_LEFT_PORT_N	==	=RP9212P5	11							
MAKE_BASE=TRUE	71	USB2_NEC_LEFT_PORT_P	==	=RP9300P8	11							
MAKE_BASE=TRUE	71	USB2_NEC_LEFT_PORT_N	==	=RP9300P7	11							
MAKE_BASE=TRUE	71	USB2_NEC_RIGHT_PORT_N	==	=RP9300P6	11							
MAKE_BASE=TRUE	71	USB2_NEC_RIGHT_PORT_P	==	=RP9300P5	11							
MAKE_BASE=TRUE	71	USB_NEC_BT_P	==	=RP9301P8	11							
MAKE_BASE=TRUE	71	USB_NEC_BT_N	==	=RP9301P7	11							
MAKE_BASE=TRUE	71	USB_NEC_TPAD_N	==	=RP9301P6	11							
MAKE_BASE=TRUE	71	USB_NEC_TPAD_P	==	=RP9301P5	11							

PCI Pullups

MAKE_BASE=TRUE	59	PCI_AIRPORT_GNT_L	==	=RP7250P1	59							
MAKE_BASE=TRUE	59	PCI_TRDY_L	==	=RP7250P2	59							
MAKE_BASE=TRUE	59	PCI_IRDY_L	==	=RP7250P3	59							
MAKE_BASE=TRUE	59	PCI_STOP_L	==	=RP7250P4	59							
MAKE_BASE=TRUE	59	PCI_CBUS_REQ_L	==	=RP7251P1	59							
MAKE_BASE=TRUE	59	PCI_AIRPORT_REQ_L	==	=RP7251P2	59							
MAKE_BASE=TRUE	59	PCI_CBUS_GNT_L	==	=RP7251P3	59							
MAKE_BASE=TRUE	59	PCI_FRAME_L	==	=RP7251P4	59							

FW Series Rs

MAKE_BASE=TRUE	68	FW_D_R<7>	==	=RP9100P1	71	71	=RP9100P8	FW_D<7>	9	69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68	FW_D_R<3>	==	=RP9100P2	71	71	=RP9100P7	FW_D<3>	9	69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68	FW_D_R<4>	==	=RP9100P3	71	71	=RP9100P6	FW_D<4>	9	69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68	FW_D_R<2>	==	=RP9100P4	71	71					

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
PP24V_ADAPTER	10	PP24V_ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector.
PP24V_ALL_PBUSA	10	PP24V_ALL_PBUSA	10	FUNC_TEST=YES	
PP12V8_ALL_PBUSB	10	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES	
PPVCORE_RUN_GPU	10	PPVCORE_RUN_GPU	10	FUNC_TEST=YES	
PPVCORE_RUN_CPU	10	PPVCORE_RUN_CPU	10	FUNC_TEST=YES	
PP1V8_PWRON	10	PP1V8_PWRON	10	FUNC_TEST=YES	Place within 50 mm of power supply.
PP2V5_PWRON	10	PP2V5_PWRON	10	FUNC_TEST=YES	
PP5V_PWRON	10	PP5V_PWRON	10	FUNC_TEST=YES	
PP3V3_PWRON	10	PP3V3_PWRON	10	FUNC_TEST=YES	
PP5V_RUN	10	PP5V_RUN	10	FUNC_TEST=YES	
PP3V3_ALL	10	PP3V3_ALL	10	FUNC_TEST=YES	
=FTP_GND	7 10	=FTP_GND	7 10	FUNC_TEST=YES	Place 5-10 GND TPs.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
LVDS_U0_P	53 56	LVDS_U0_P	53 56	FUNC_TEST=YES	
LVDS_U0_N	53 56	LVDS_U0_N	53 56	FUNC_TEST=YES	
LVDS_U1_P	53 56	LVDS_U1_P	53 56	FUNC_TEST=YES	
LVDS_U1_N	53 56	LVDS_U1_N	53 56	FUNC_TEST=YES	
LVDS_U2_P	53 56	LVDS_U2_P	53 56	FUNC_TEST=YES	
LVDS_U2_N	53 56	LVDS_U2_N	53 56	FUNC_TEST=YES	
CLKLVDS_U_P	53 56	CLKLVDS_U_P	53 56	FUNC_TEST=YES	
CLKLVDS_U_N	53 56	CLKLVDS_U_N	53 56	FUNC_TEST=YES	
LVDS_L0_P	53 56	LVDS_L0_P	53 56	FUNC_TEST=YES	
LVDS_L0_N	53 56	LVDS_L0_N	53 56	FUNC_TEST=YES	
LVDS_L1_P	53 56	LVDS_L1_P	53 56	FUNC_TEST=YES	
LVDS_L1_N	53 56	LVDS_L1_N	53 56	FUNC_TEST=YES	
LVDS_L2_P	53 56	LVDS_L2_P	53 56	FUNC_TEST=YES	
LVDS_L2_N	53 56	LVDS_L2_N	53 56	FUNC_TEST=YES	
CLKLVDS_L_P	53 56	CLKLVDS_L_P	53 56	FUNC_TEST=YES	
CLKLVDS_L_N	53 56	CLKLVDS_L_N	53 56	FUNC_TEST=YES	
LVDS_DDC_CLK	51 56	LVDS_DDC_CLK	51 56	FUNC_TEST=YES	
LVDS_DDC_DATA	51 56	LVDS_DDC_DATA	51 56	FUNC_TEST=YES	
=PP3V3_DDC_LCD	10 56	=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES	
PP3V3_LCD_CONN	56	PP3V3_LCD_CONN	56	FUNC_TEST=YES	

Place within 25 mm of LVDS connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
PPBUS_INVERTER	56	PPBUS_INVERTER	56	FUNC_TEST=YES	
PP5V_INV_SW	56	PP5V_INV_SW	56	FUNC_TEST=YES	
BRIGHT_PWM	56	BRIGHT_PWM	56	FUNC_TEST=YES	
GND_INVERTER	56	GND_INVERTER	56	FUNC_TEST=YES	

Place within 25 mm of inverter connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
=PP5V_RUN_ODD	10 64	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES	
=PP5V_RUN_HDD	10 64	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES	
PP3V3R5V_RUN_HDD_LOGIC	64	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES	
UATA_DD<15..0>	6 63 64	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES	
UATA_DMAR0	63 64	UATA_DMAR0	63 64	FUNC_TEST=YES	
UATA_DSTROBE	63 64	UATA_DSTROBE	63 64	FUNC_TEST=YES	
UATA_DMACK_L	63 64	UATA_DMACK_L	63 64	FUNC_TEST=YES	
UATA_DA<2..0>	6 63 64	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES	
UATA_CS0_L	6 63 64	UATA_CS0_L	6 63 64	FUNC_TEST=YES	
UATA_CS1_L	63 64	UATA_CS1_L	63 64	FUNC_TEST=YES	
UATA_RESET_L	63 64	UATA_RESET_L	63 64	FUNC_TEST=YES	
UATA_HSTROBE	63 64	UATA_HSTROBE	63 64	FUNC_TEST=YES	
UATA_STOP	63 64	UATA_STOP	63 64	FUNC_TEST=YES	
UATA_INTRO	63 64	UATA_INTRO	63 64	FUNC_TEST=YES	

Place within 50 mm of ODD/HDD connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
PP5V_PWRON_AUDIO_PVDD	74	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES	
PP5V_PWRON_AUDIO_AVDD	74	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
PP3V3_PWRON_AUDIO_AVDD	74	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
=PP3V3_RUN_AUDIO	10 74	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES	
=I2C_AUDIO_SCL	8 74	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES	
=I2C_AUDIO_SDA	8 74	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES	
I2S0_MCLK	6 74	I2S0_MCLK	6 74	FUNC_TEST=YES	
I2S0_BITCLK	6 74	I2S0_BITCLK	6 74	FUNC_TEST=YES	
I2S0_SYNC	6 74	I2S0_SYNC	6 74	FUNC_TEST=YES	
I2S0_SB_TO_DEV_DTO	6 74	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES	
I2S0_DEV_TO_SB_DTI	22 74	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES	
AUDIO_LO_MUTE_L	22 74	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES	
AUDIO_SPKR_MUTE_L	22 74	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES	
AUDIO_CODEC_RESET_L	22 74	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES	
AUDIO_SPDIFRX_RESET_L	22 74	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES	
AUDIO_LO_DET_L	22 74	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES	
AUDIO_LI_DET_L	22 74	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES	
AUDIO_LO_OPTICAL_PLUG_L	22 74	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES	
AUDIO_LI_OPTICAL_PLUG_L	22 74	AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES	
AUDIO_I2S_DTIB_SEL	22 74	AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES	
AUDIO_EXT_MCLK_SEL	22 74	AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES	
AUDIO_GPIO_11	22 74	AUDIO_GPIO_11	22 74	FUNC_TEST=YES	
GND_AUDIO_AGND	74	GND_AUDIO_AGND	74	FUNC_TEST=YES	
GND_AUDIO_PGND	74	GND_AUDIO_PGND	74	FUNC_TEST=YES	

Place within 25 mm of audio connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
PP5V_TPAD_F	10 30	PP5V_TPAD_F	10 30	FUNC_TEST=YES	
USB_TPAD_P	11 30	USB_TPAD_P	11 30	FUNC_TEST=YES	
USB_TPAD_N	11 30	USB_TPAD_N	11 30	FUNC_TEST=YES	
PP3V3_PWRON_DS1775_R	10 30	PP3V3_PWRON_DS1775_R	10 30	FUNC_TEST=YES	
SYS_OVERTEMP_L	11 25 30	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
PP3V3_ALL_HALL_EFFECT_R	10 30	PP3V3_ALL_HALL_EFFECT_R	10 30	FUNC_TEST=YES	
SYS_LID_OPEN_F	10 30	SYS_LID_OPEN_F	10 30	FUNC_TEST=YES	
SYS_POWER_BUTTON_L_F	10 30	SYS_POWER_BUTTON_L_F	10 30	FUNC_TEST=YES	
=FTP_SLEEP_LED	10 30	=FTP_SLEEP_LED	10 30	FUNC_TEST=YES	
SYS_CHARGE_LED_L	24 74	SYS_CHARGE_LED_L	24 74	FUNC_TEST=YES	
SYS_ADAPTER_ANALOG_AC_DET	12 74	SYS_ADAPTER_ANALOG_AC_DET	12 74	FUNC_TEST=YES	
KBDDLED_ANODE	28 30	KBDDLED_ANODE	28 30	FUNC_TEST=YES	
KBDDLED_RETURN	28 30	KBDDLED_RETURN	28 30	FUNC_TEST=YES	
=I2C_DS1775_SDA	8 30	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES	
=I2C_DS1775_SCL	8 30	=I2C_DS1775_SCL	8 30	FUNC_TEST=YES	

Place within 25 mm of TPAD connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
=PP5V_FAN1_PWR	10 31	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	
FAN1_TACH	27 31	FAN1_TACH	27 31	FUNC_TEST=YES	
FAN1_PWM	27 31	FAN1_PWM	27 31	FUNC_TEST=YES	
=FTP_GND	7 10	=FTP_GND	7 10	FUNC_TEST=YES	

Place within 25 mm of fan connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
=PP5V_FAN2_PWR	10 31	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	
FAN2_TACH	27 31	FAN2_TACH	27 31	FUNC_TEST=YES	
FAN2_PWM	27 31	FAN2_PWM	27 31	FUNC_TEST=YES	
=FTP_GND	7 10	=FTP_GND	7 10	FUNC_TEST=YES	

Place within 25 mm of fan connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
=PP3V3_PWRON_LEFT_ALS	10 31	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	
ALS_0_OUT	25 31	ALS_0_OUT	25 31	FUNC_TEST=YES	
ALS_GAIN_BOOST	25 28 31	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	

Place within 25 mm of ALS connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
SCCA_RXD	22 24	SCCA_RXD	22 24	FUNC_TEST=YES	
SCCA_TXD_L	22 24	SCCA_TXD_L	22 24	FUNC_TEST=YES	

Place within 25 mm of debug connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
=PPVIO_BU_BATT	10 31	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	
=PPVOUT_BU_BATT	10 31	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	

Place within 25 mm of battery connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
=PP5V_PWRON_RIGHT_USB	10 31	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	
USB2_RIGHT_PORT_P	11 31	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	
USB2_RIGHT_PORT_N	11 31	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	

Place within 25 mm of right USB connector.

TEST POINT	LOC	TEST POINT	LOC	FUNC_TEST	NOTE
=PP5V_PWRON_LEFT_USB	10 74	=PP5V_PWRON_LEFT_USB	10 74	FUNC_TEST=YES	
USB2_LEFT_PORT_P	11 74	USB2_LEFT_PORT_P	11 74	FUNC_TEST=YES	
USB2_LEFT_PORT_N	11 74	USB2_LEFT_PORT_N	11 74	FUNC_TEST=YES	

Place within 25 mm of left USB connector.

Functional Test Points

SYNC_MASTER=N/A SYNC_DATE=N/A

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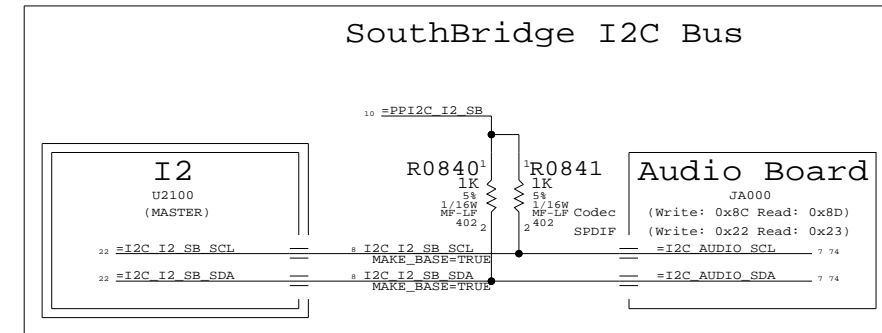
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SIZE	DRAWING NUMBER	REV.
D	051-7001	D
SCALE	SHT	OF
NONE	7	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
I2C_PMU_SMB_SCL	I2C	I2C		I2C_PMU_SMB_SCL
I2C_PMU_SMB_SDA	I2C	I2C		I2C_PMU_SMB_SDA
I2C_PMU_SCL	I2C	I2C		I2C_PMU_SCL
I2C_PMU_SDA	I2C	I2C		I2C_PMU_SDA
I2C_NB	I2C	I2C		I2C_I2_NB_SCL
I2C_NB	I2C	I2C		I2C_I2_NB_SDA
	I2C	I2C		I2C_I2_SB_SCL
	I2C	I2C		I2C_I2_SB_SDA
	I2C	I2C		I2C_GPU_TMDS_SCL
	I2C	I2C		I2C_GPU_TMDS_SDA



Page Notes

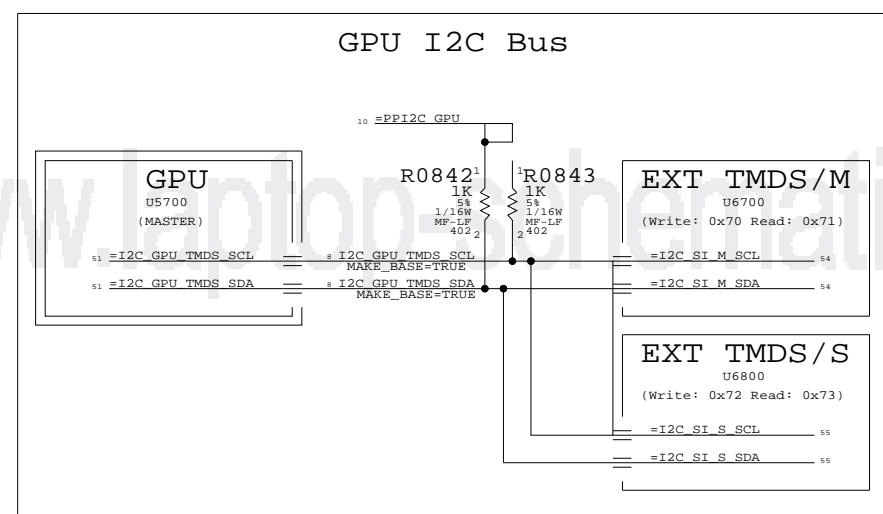
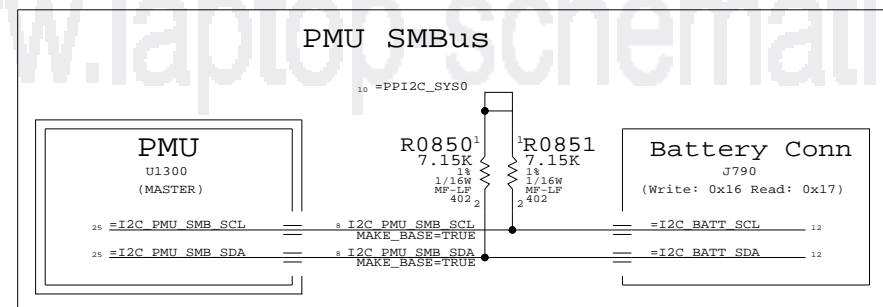
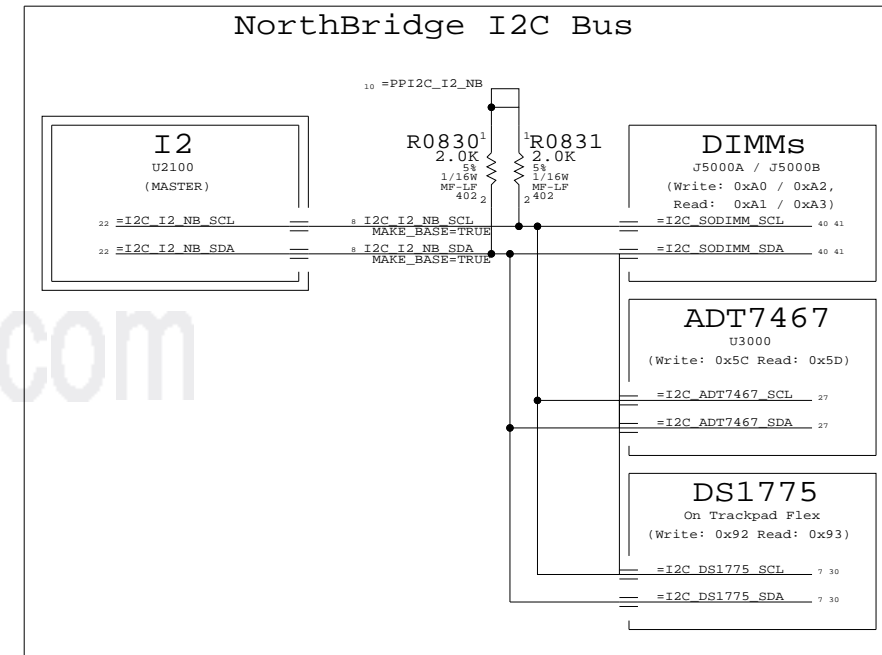
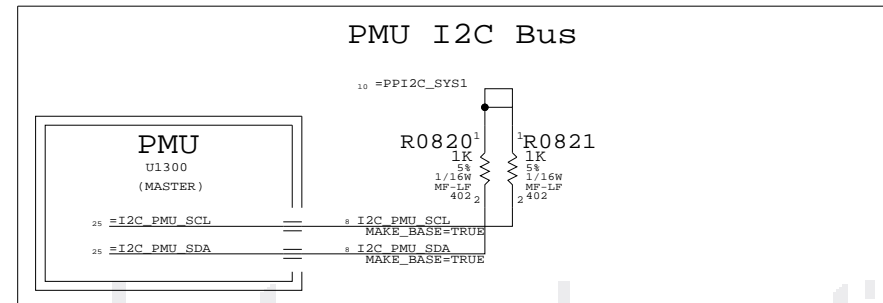
Power aliases required by this page: (NONE)

Signal aliases required by this page: (NONE)

BOM options provided by this page:

- GOV_I2C / GOV_I2C_BYPASS
Allows bypassing Governor I2C bus. Most devices are connected directly to PMU instead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown. NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.

www.laptop-schematics.com



I2C Connections

SYNC_MASTER=N/A SYNC_DATE=N/A

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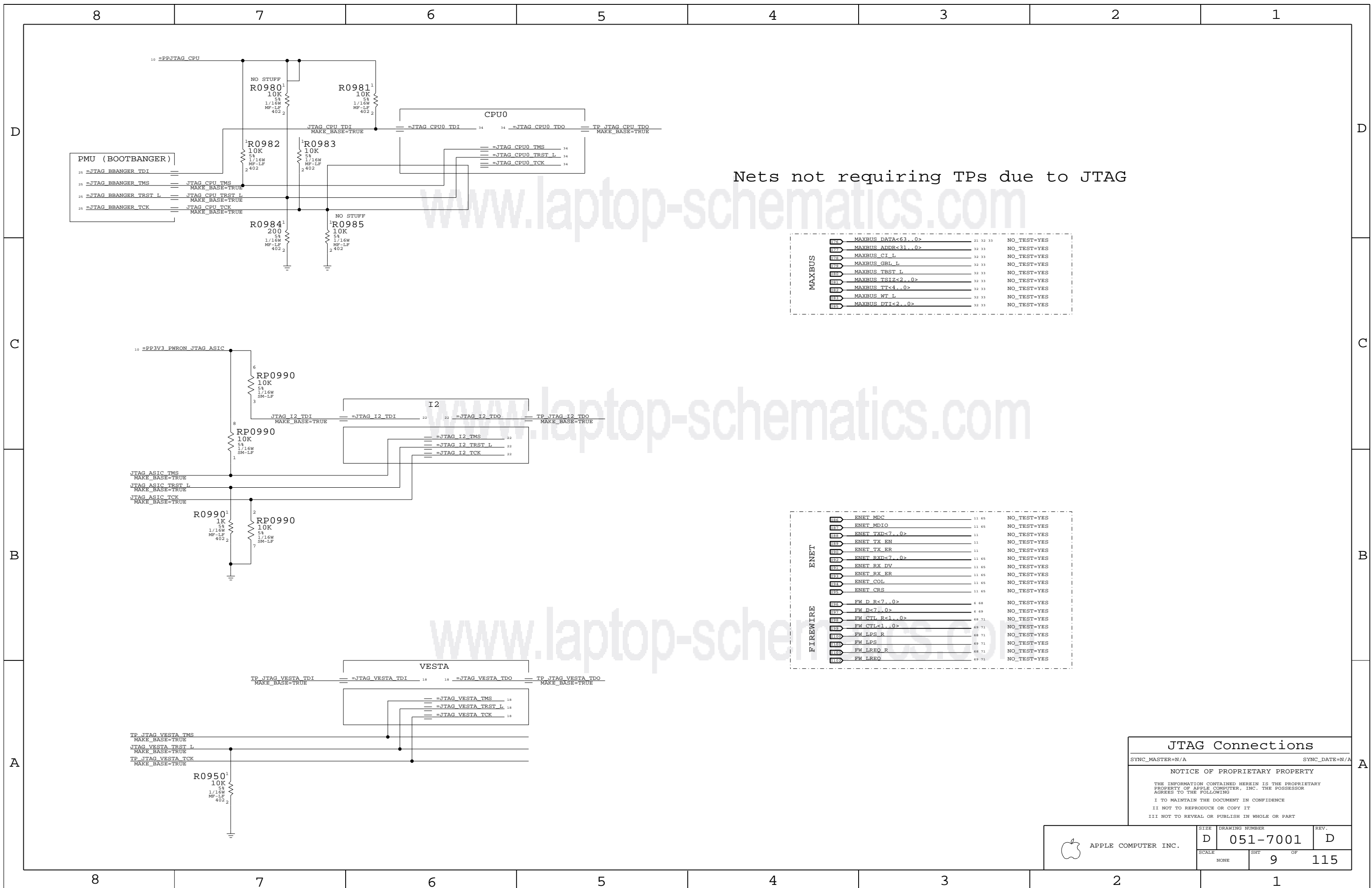
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	D	051-7001	D
SCALE	SHEET		OF
NONE	8		115



Nets not requiring TPs due to JTAG

MAXBUS		
RES	MAXBUS_DATA<63..0>	21 32 33 NO_TEST=YES
RES	MAXBUS_ADDR<31..0>	32 33 NO_TEST=YES
RES	MAXBUS_CE_L	32 33 NO_TEST=YES
RES	MAXBUS_GBL_L	32 33 NO_TEST=YES
RES	MAXBUS_TRST_L	32 33 NO_TEST=YES
RES	MAXBUS_TSIZ<2..0>	32 33 NO_TEST=YES
RES	MAXBUS_TT<4..0>	32 33 NO_TEST=YES
RES	MAXBUS_WT_L	32 33 NO_TEST=YES
RES	MAXBUS_DTI<2..0>	32 33 NO_TEST=YES

ENET		
RES	ENET_MDC	11 68 NO_TEST=YES
RES	ENET_MDIO	11 68 NO_TEST=YES
RES	ENET_TXD<7..0>	11 NO_TEST=YES
RES	ENET_TX_EN	11 NO_TEST=YES
RES	ENET_TX_ER	11 NO_TEST=YES
RES	ENET_RXD<7..0>	11 68 NO_TEST=YES
RES	ENET_RX_DV	11 68 NO_TEST=YES
RES	ENET_RX_ER	11 68 NO_TEST=YES
RES	ENET_COL	11 68 NO_TEST=YES
RES	ENET_CRD	11 68 NO_TEST=YES
FIREWIRE		
RES	FW_D_R<7..0>	6 68 NO_TEST=YES
RES	FW_D<7..0>	6 68 NO_TEST=YES
RES	FW_CTL_R<1..0>	68 71 NO_TEST=YES
RES	FW_CTL<1..0>	68 71 NO_TEST=YES
RES	FW_LPS_R	68 71 NO_TEST=YES
RES	FW_LPS	68 71 NO_TEST=YES
RES	FW_LREQ_R	68 71 NO_TEST=YES
RES	FW_LREQ	68 71 NO_TEST=YES

JTAG Connections

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT	OF	
NONE	9	115	



Power Synonyms		
SYNC_MASTER=N/A		SYNC_DATE=N/A

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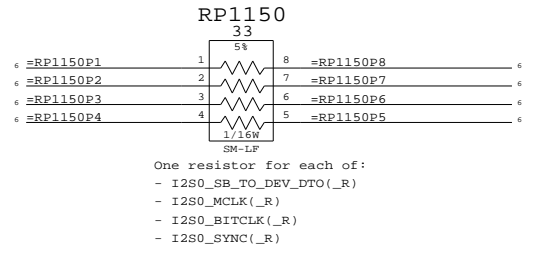
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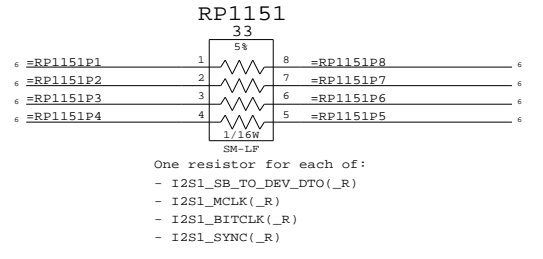
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	
NONE	10	115	

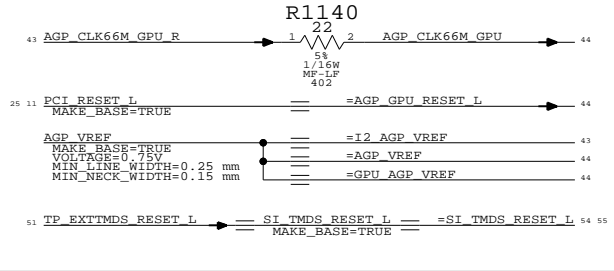
I2S0 Series Rs



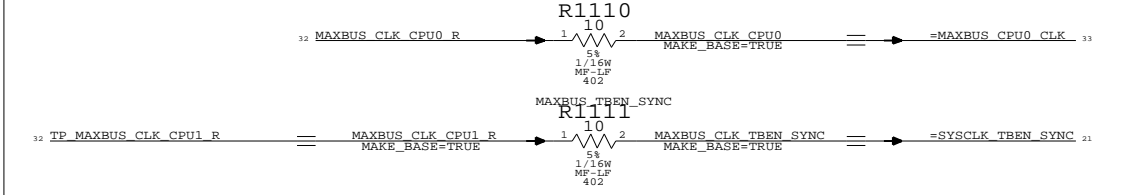
I2S1 Series Rs



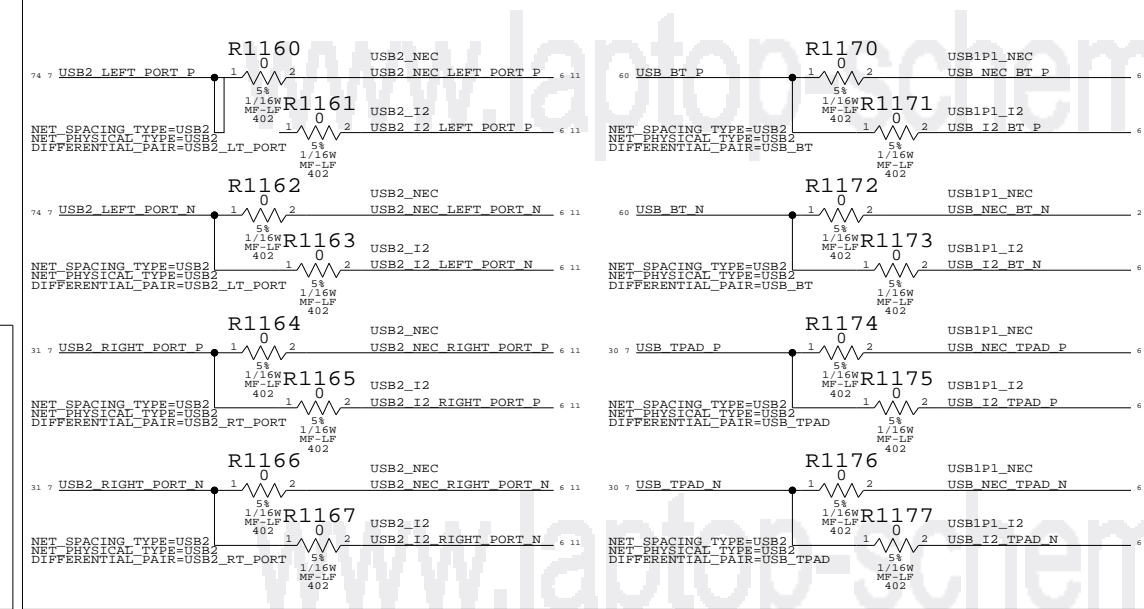
GPU



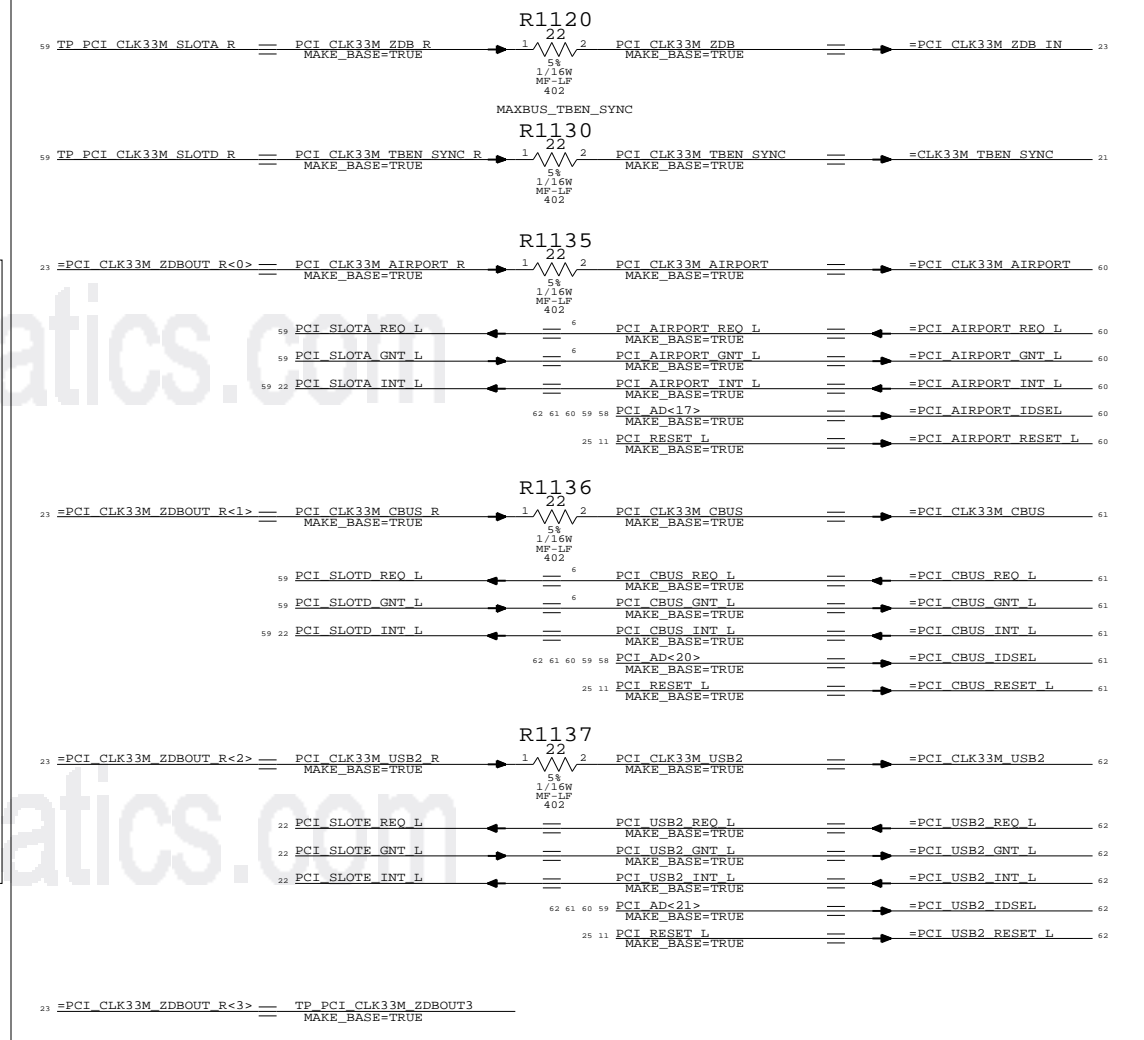
CPU Clocks



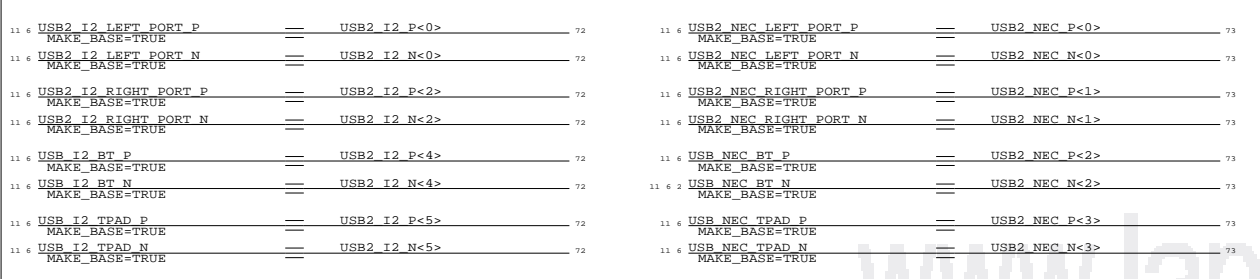
USB Controller Mux



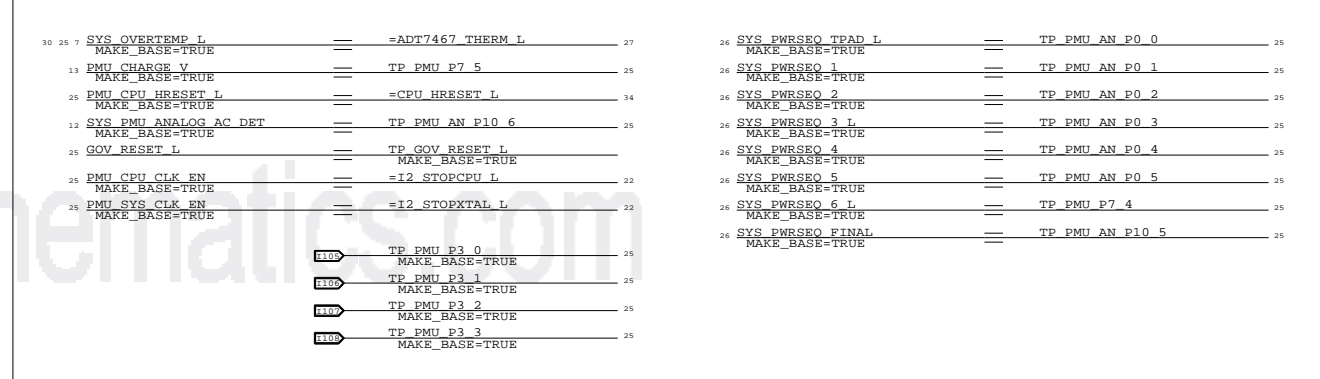
PCI



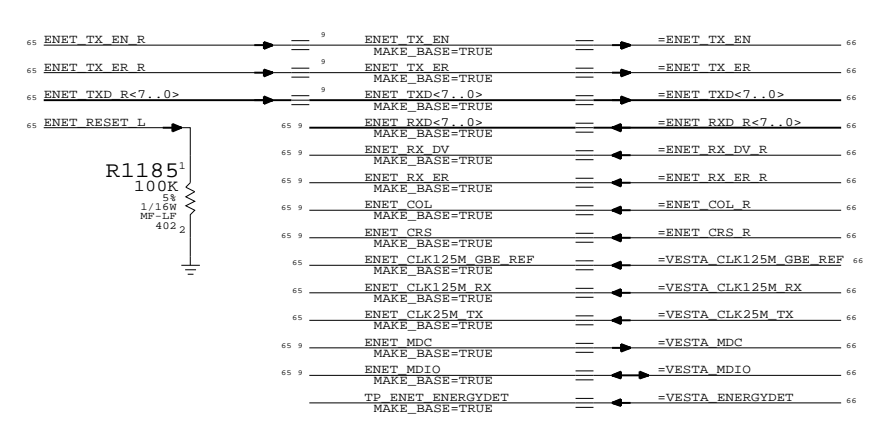
USB Port Assignments



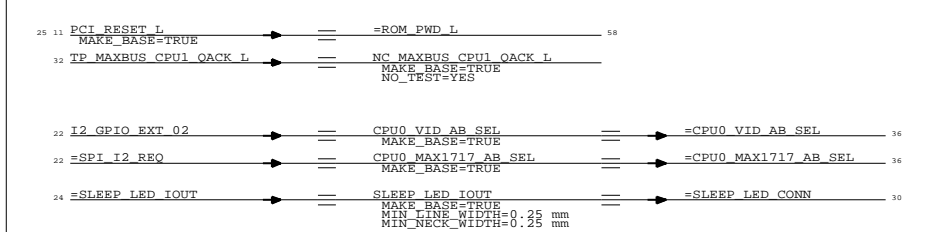
PMU Connections



Vesta Ethernet



MISC



Signal Synonyms

SYNC_MASTER=N/A SYNC_DATE=N/A

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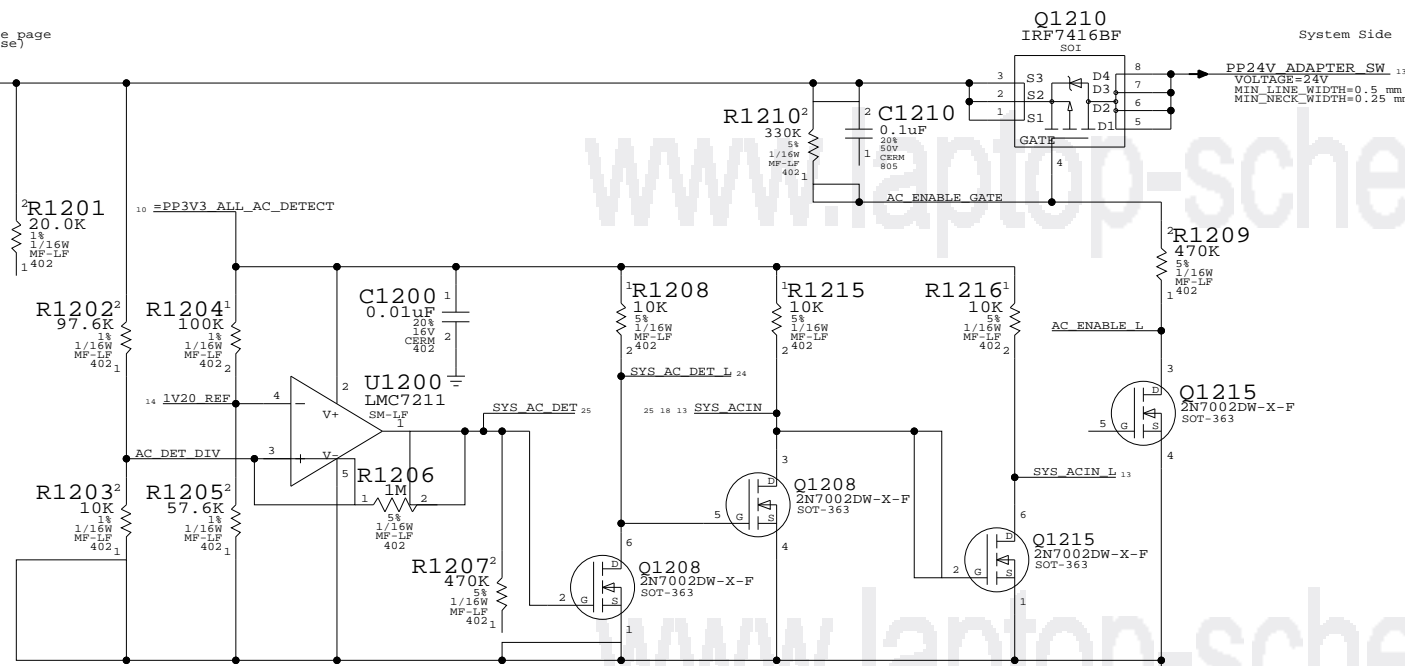
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ELECTRICAL_CONSTRAINT_SET		NET_TYPE		DIFFERENTIAL_PAIR	
NET	TYPE	SPACING	PHYSICAL	PHYSICAL	PHYSICAL
PP24V	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINP	12
PP24V	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINN	12

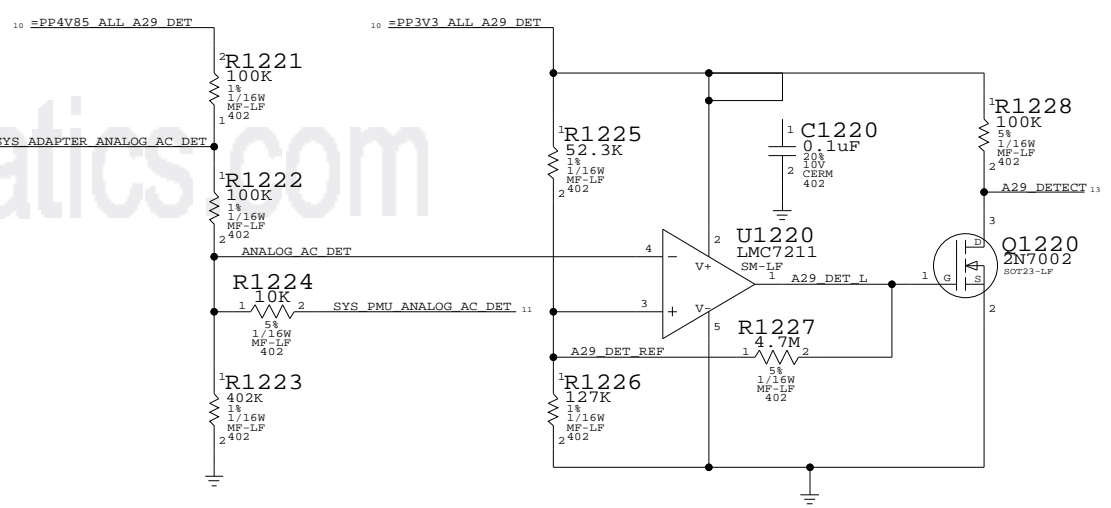
ADAPTER INPUT/INRUSH LIMITER

Adapter Connector Side
(Connector is on separate page to facilitate design reuse)



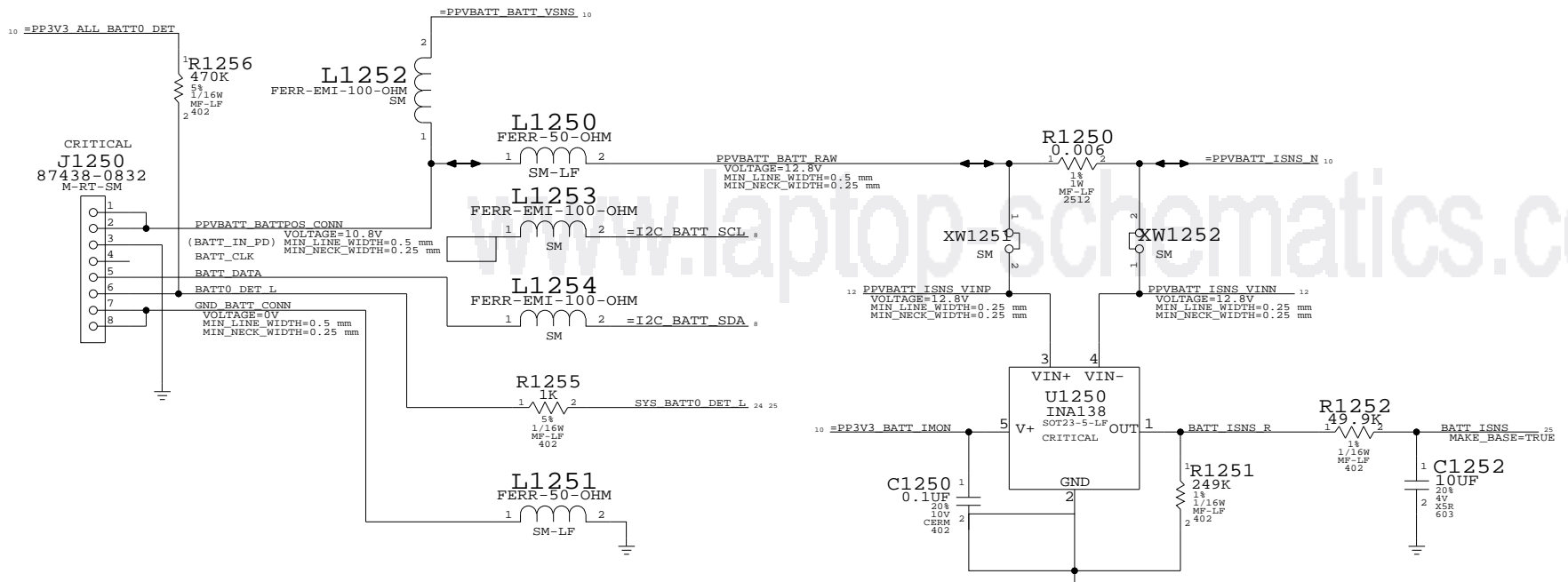
GREATER THAN 13.1V DETECT
SYS AC_DET indicates adapter presence. SYS ACIN is code controlled signal to enable use of AC in system. Q1205 ensures SYS ACIN goes low as soon as SYS AC_DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



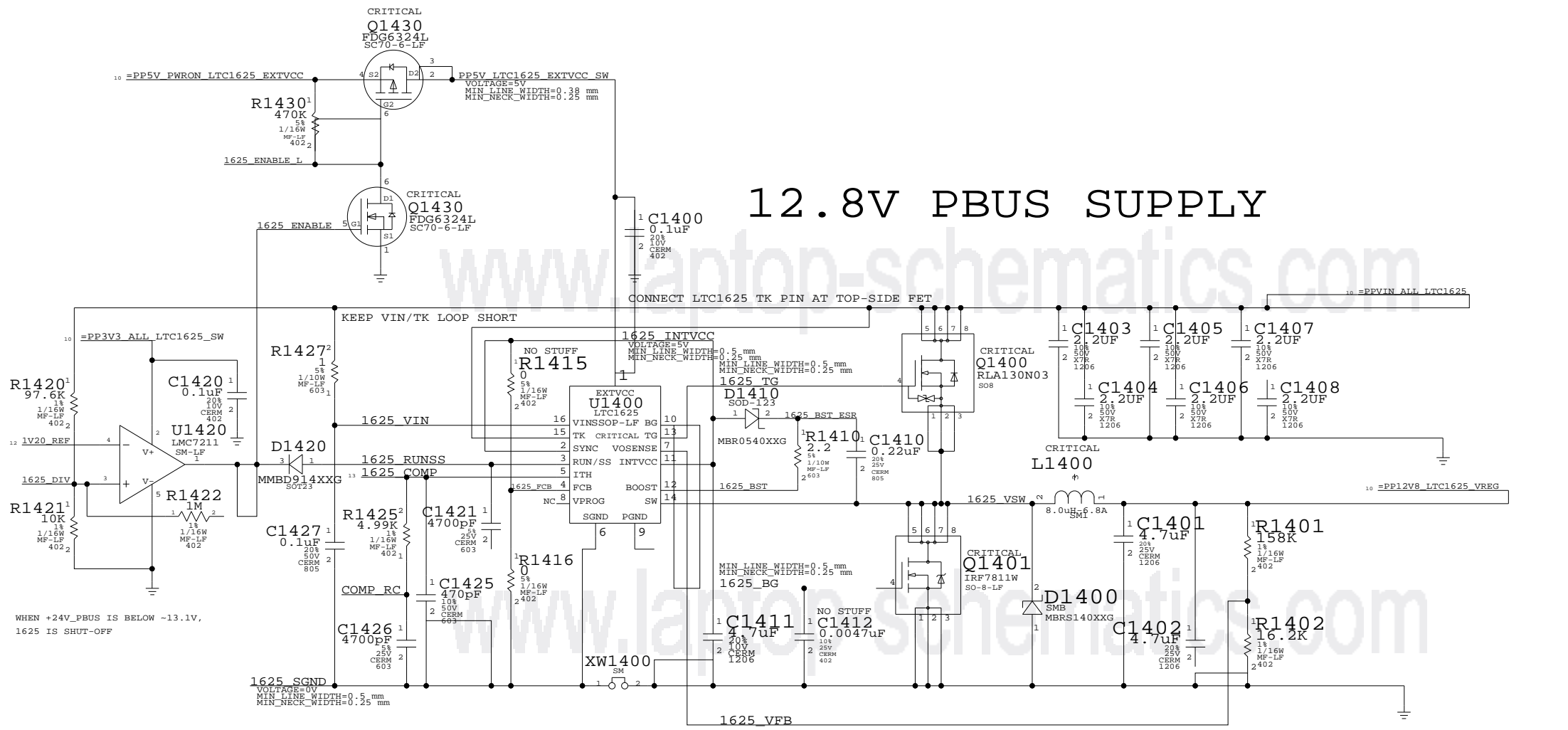
ADAPTER IDS		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



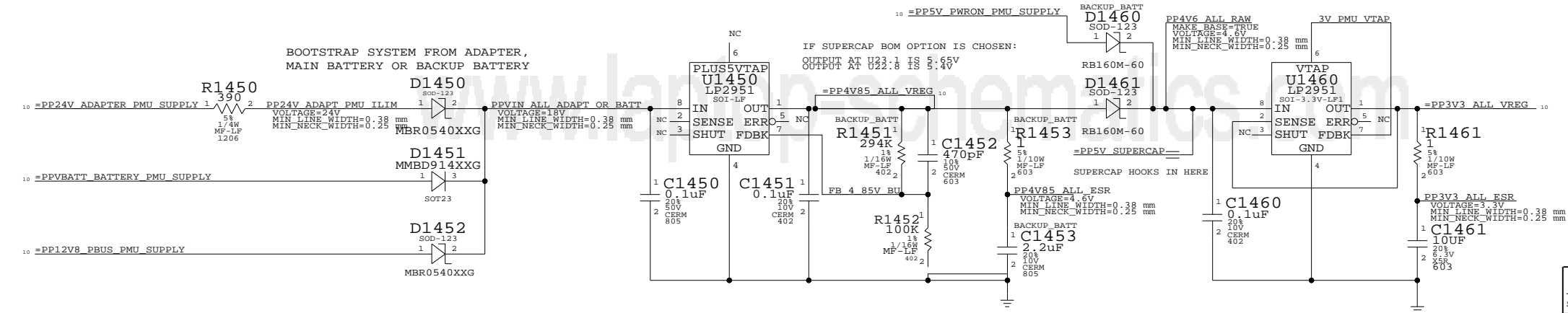
Power Inputs
 SYNC_MASTER=N/A SYNC_DATE=N/A
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SCALE	SHT	OF	REV.
NONE	12	115	



12.8V PBUS SUPPLY

PMU SUPPLY



12.8V PBUS/PMU Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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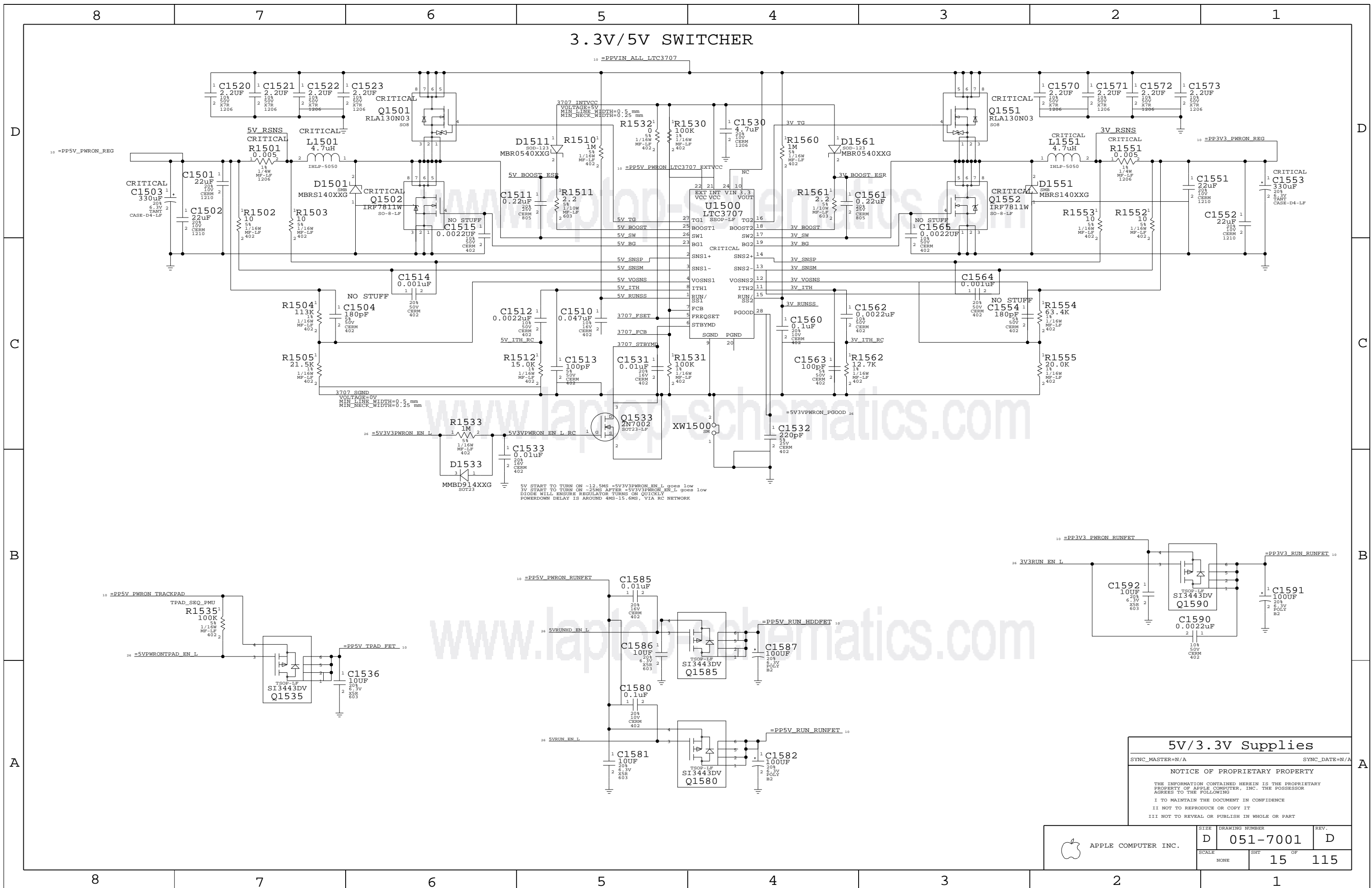
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0465	1	RES,MP-LP,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7001	D
SCALE	SHT	OF
NONE	14	115

3.3V/5V SWITCHER



5V/3.3V Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

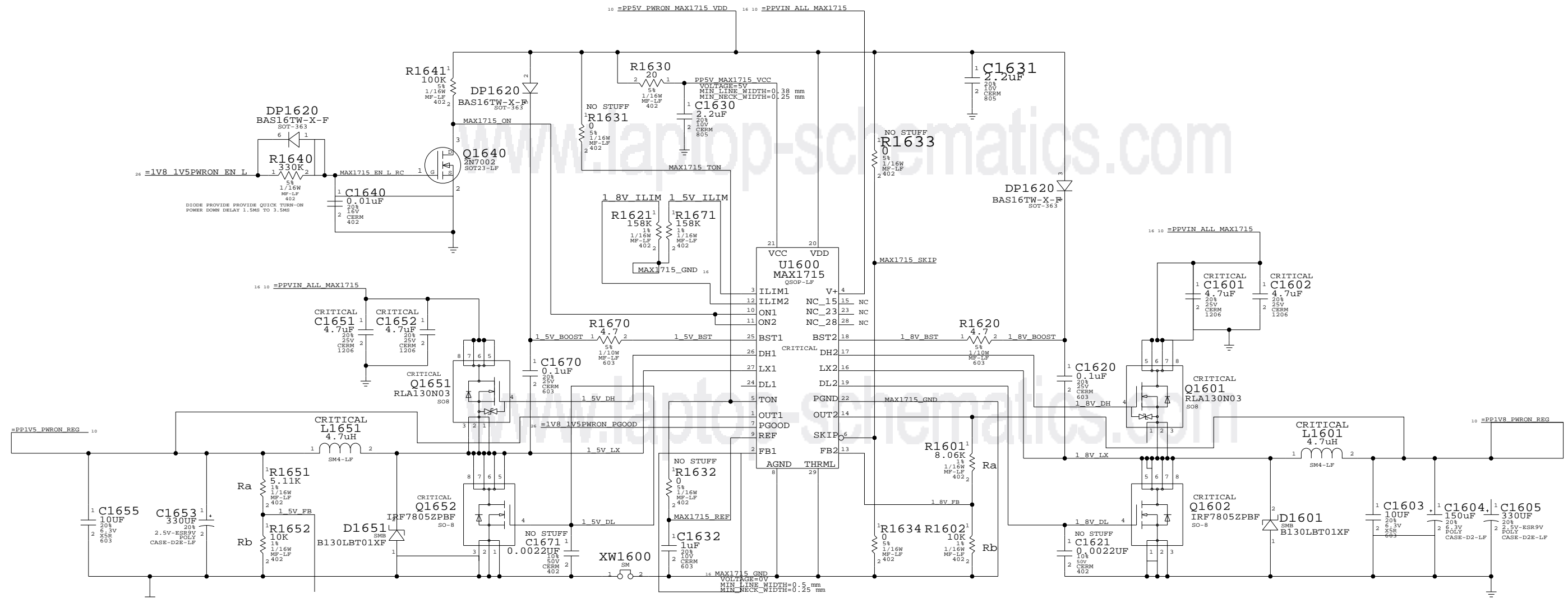
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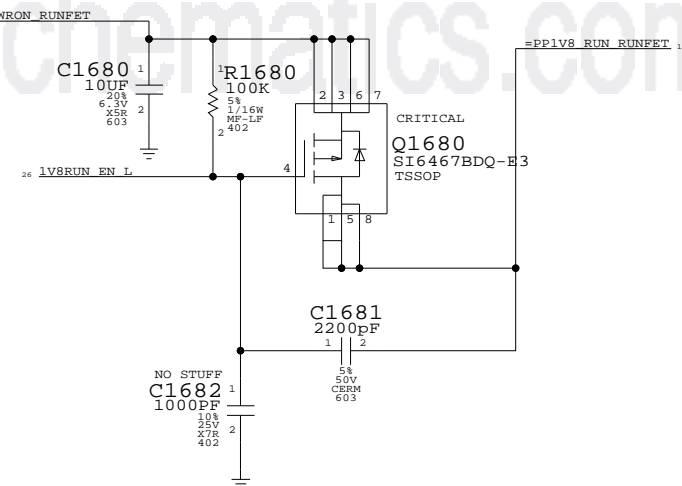
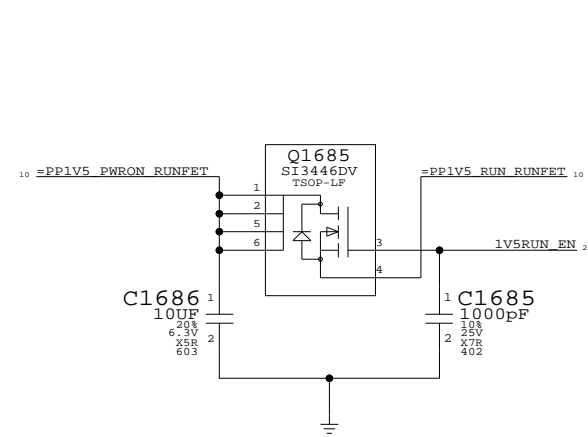
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SCALE	SHT	OF	
NONE	15	115	

1.5V/1.8V SWITCHER



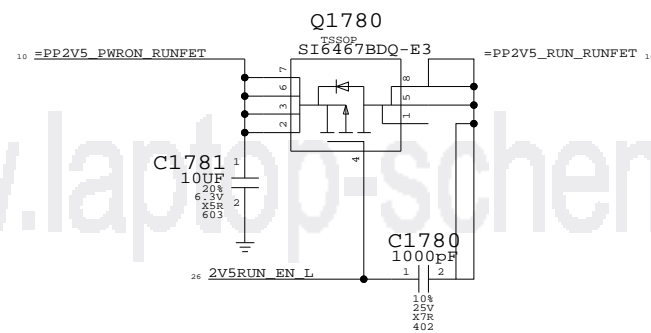
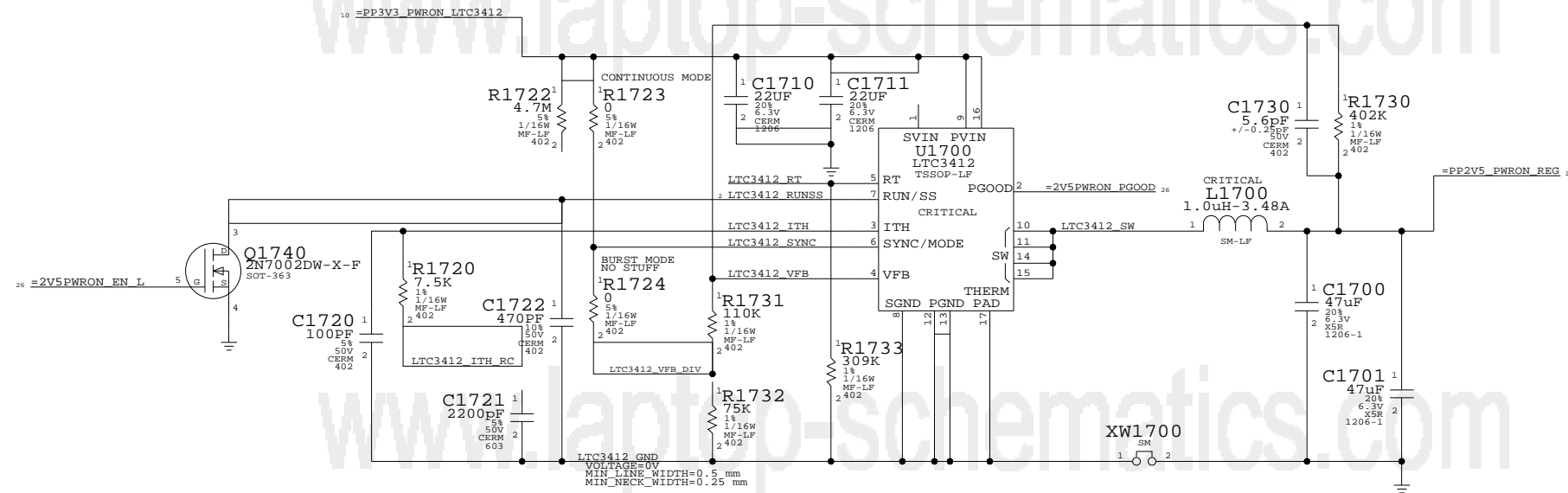
$$V_{out} = 1.0V * (1 + R_a/R_b)$$



1.8V/1.5V Supplies
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHT	OF	
NONE	16	115	

2.5V SWITCHER



2.5V Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT OF	17 OF 115

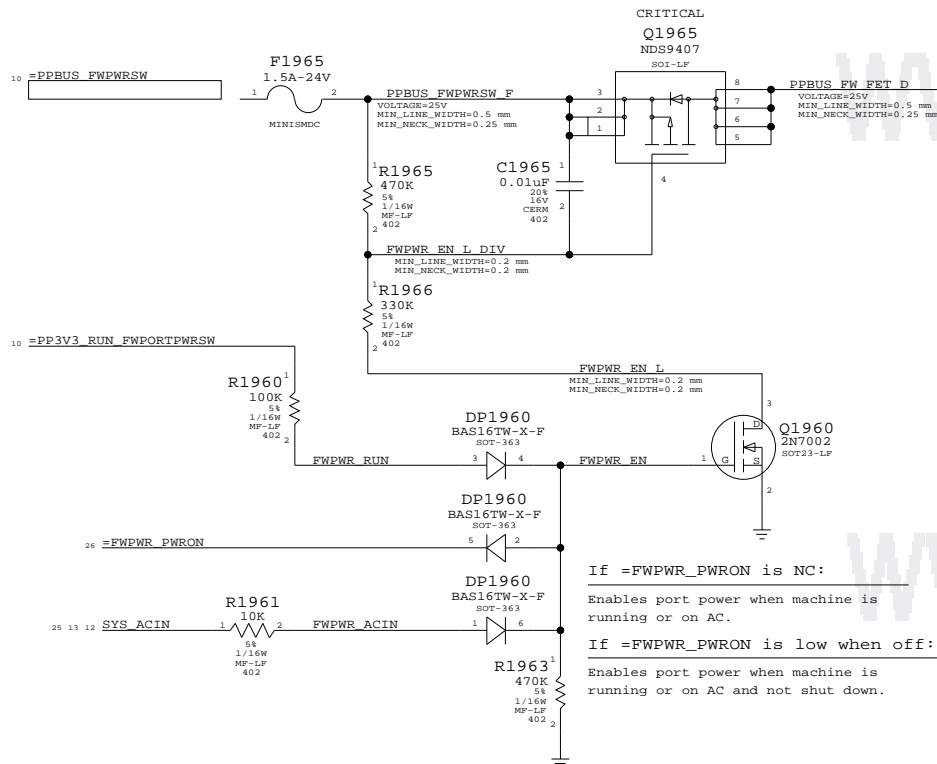
Page Notes

Power aliases required by this page:
 - =PPBUS_FW (system supply for bus power)
 - =PPBU_RUN_FW (backup PHY power)
 - =PP3V3_RUN_FWPORTFWRWSW

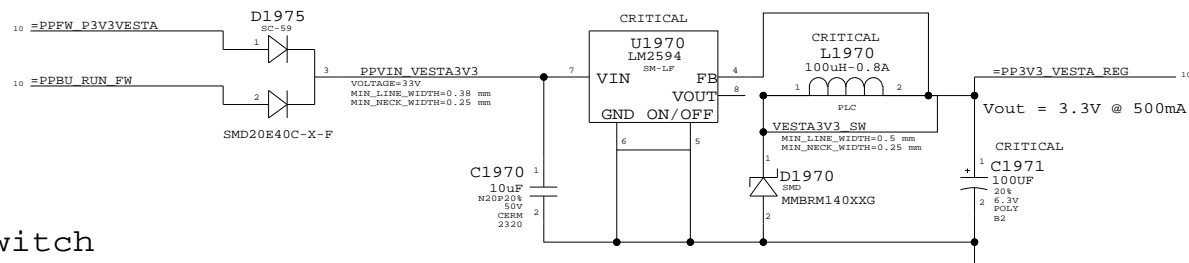
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - VESTALV2_BURST / VESTALV2_PULSE
 Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

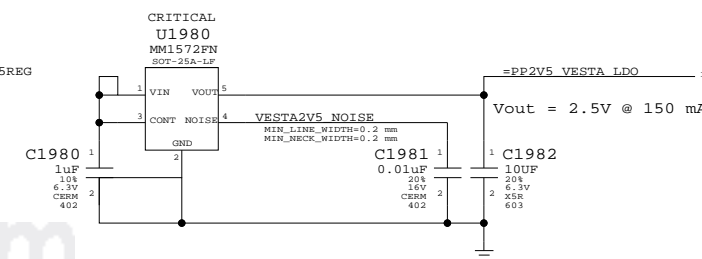
Port Power Switch



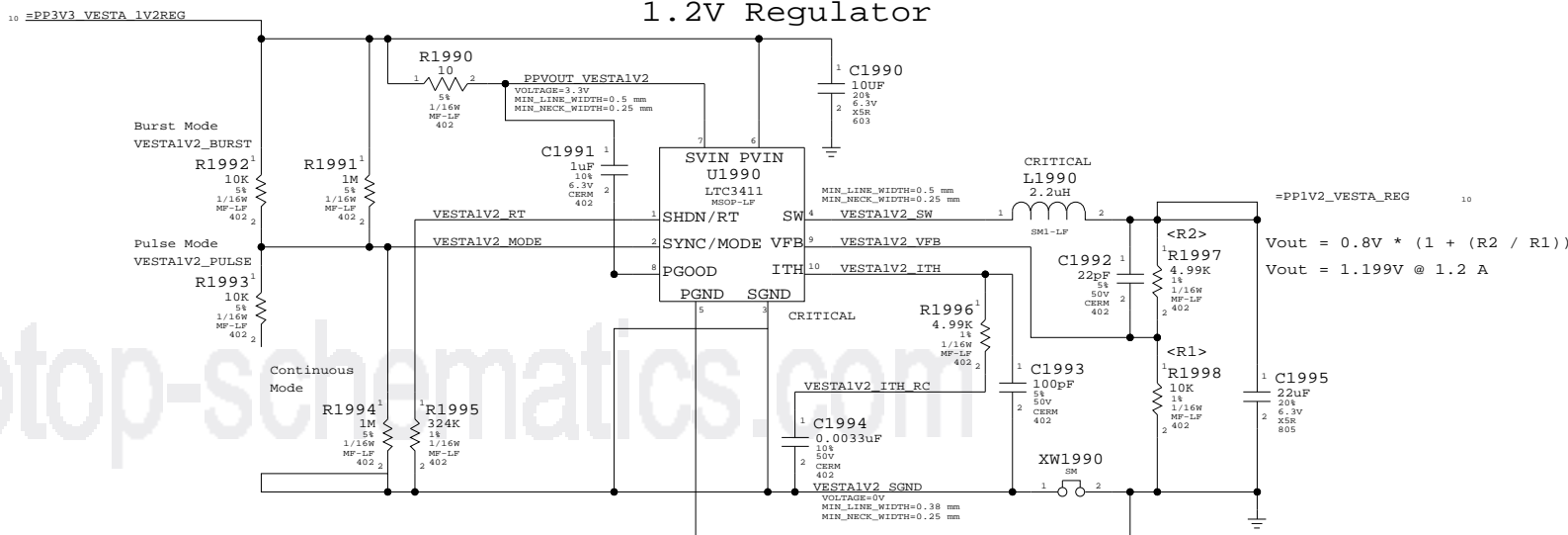
3.3V Regulator



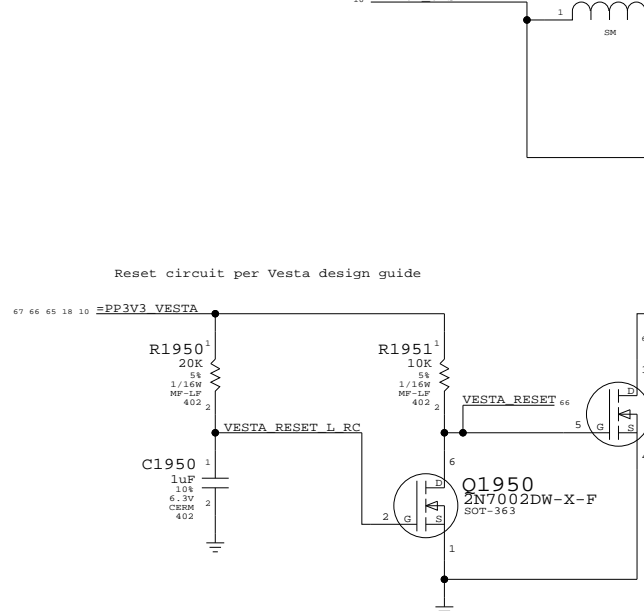
2.5V LDO



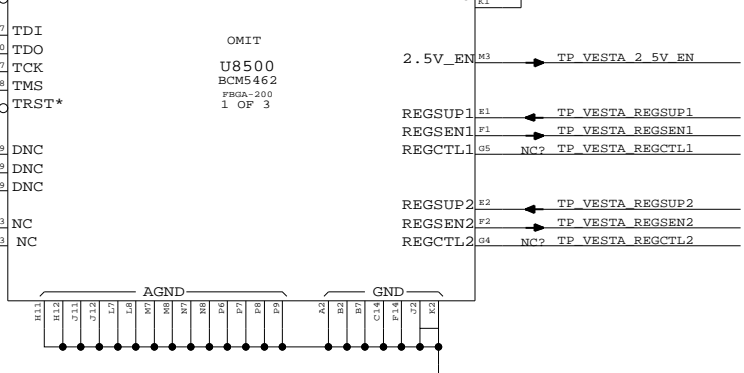
1.2V Regulator



Reset circuit per Vesta design guide



VESTA MISC



Vesta Power & Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	19	115	

Page Notes

Power aliases required by this page:
- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_AGPCCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.
NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

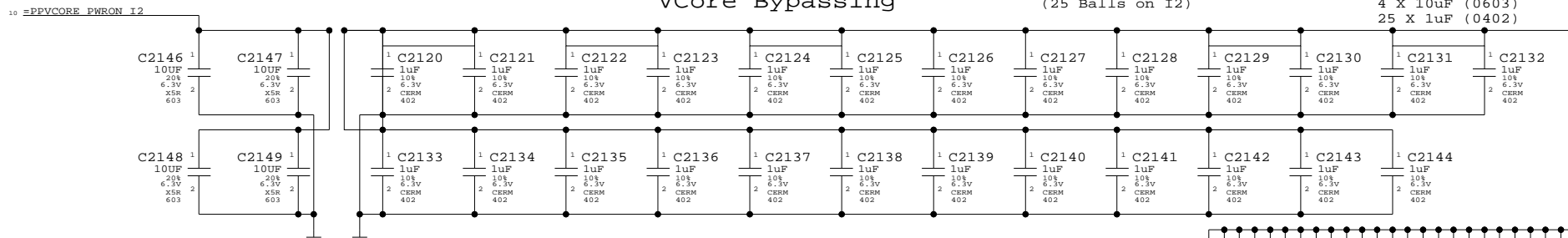
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

VCore Bypassing

(25 Balls on I2)

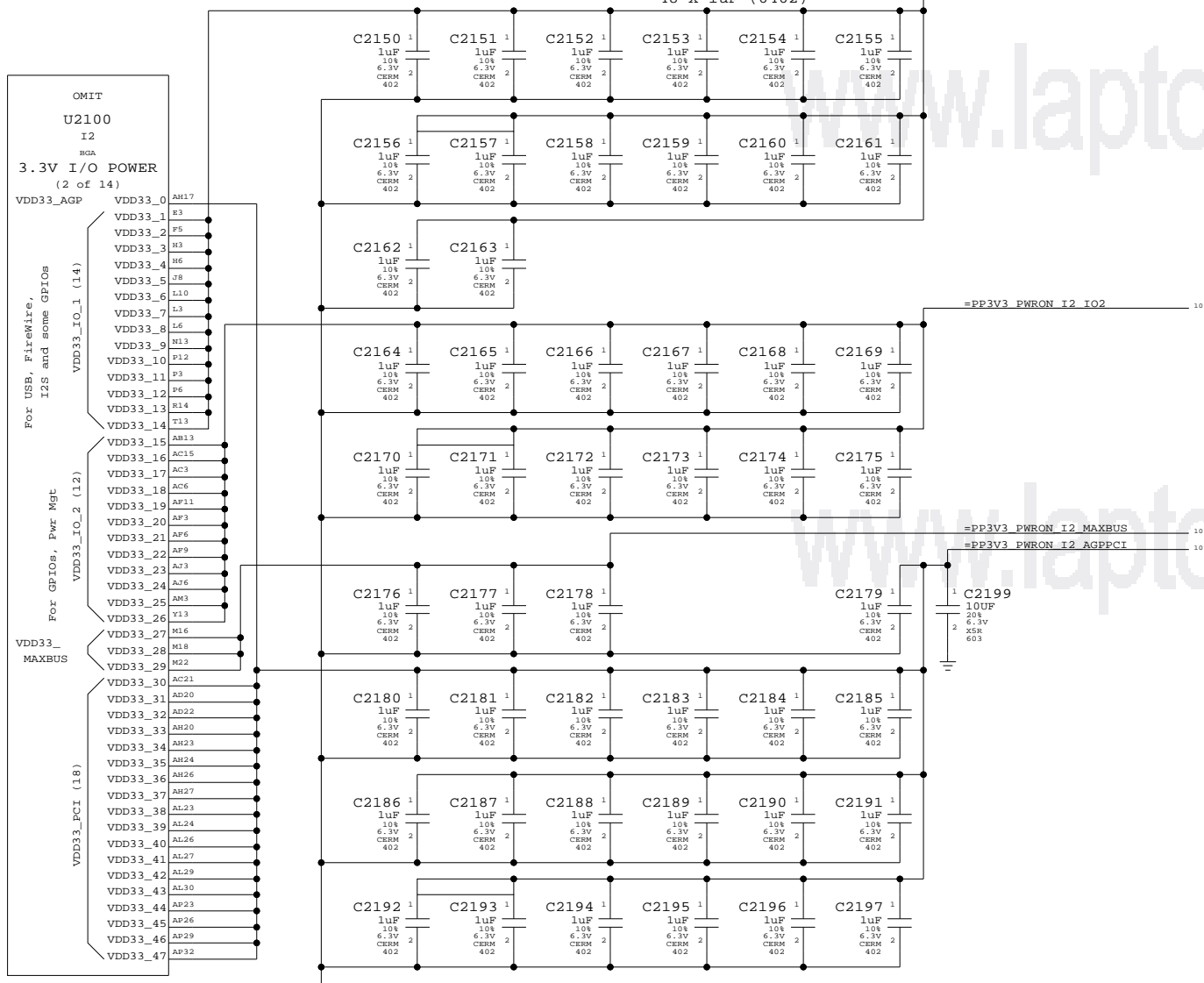
4 X 10uF (0603)
25 X 1uF (0402)



3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)



=PP1V5_PWRON_I2_PLL

=PP3V3_PWRON_I2_IO1

=PP3V3_PWRON_I2_IO2

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

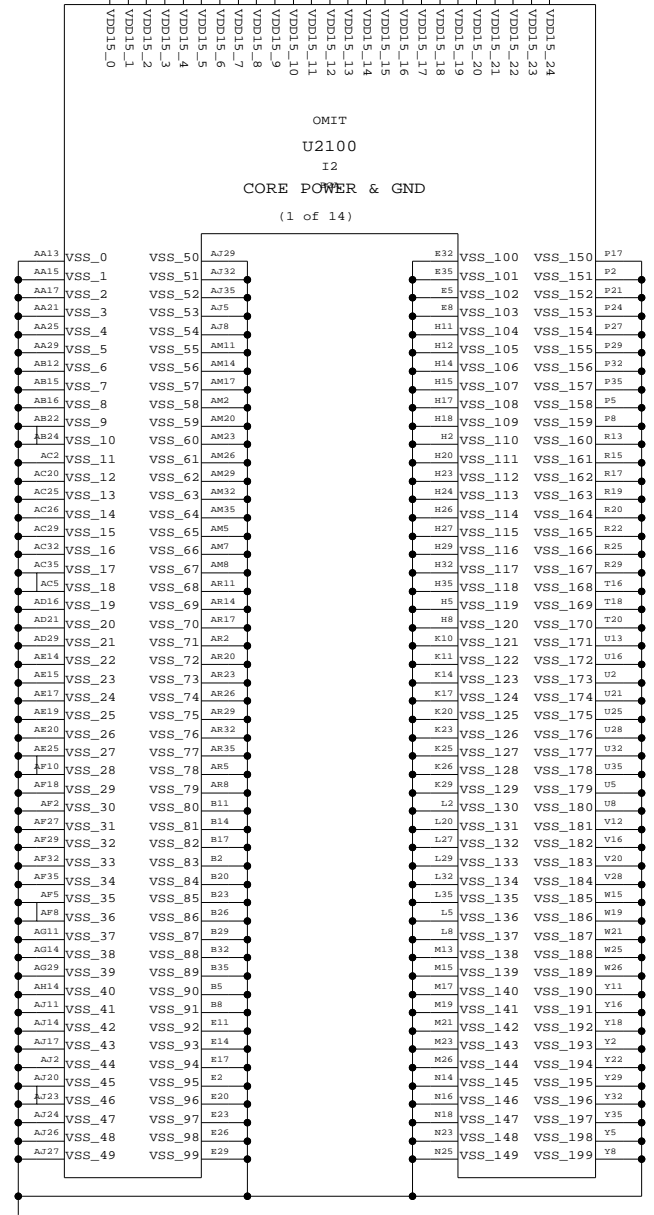
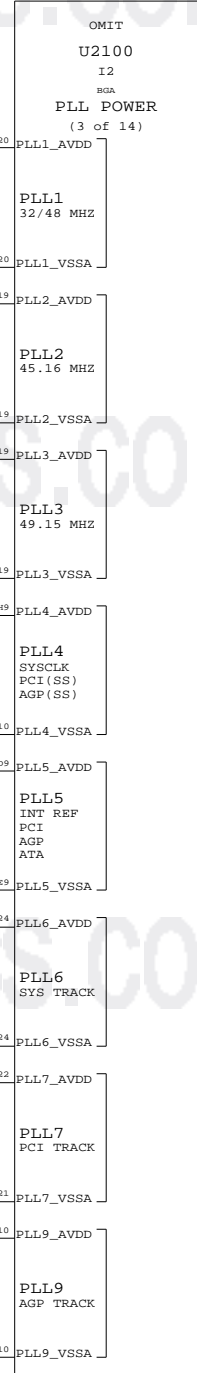
=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI

=PP3V3_PWRON_I2_MAXBUS

=PP3V3_PWRON_I2_AGPCCI



I2 Power
SYNC_MASTER=N/A SYNC_DATE=N/A
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Table with columns for Apple logo, Drawing Number (D 051-7001), Rev. (D), Scale (NONE), and Sheet (21 OF 115).

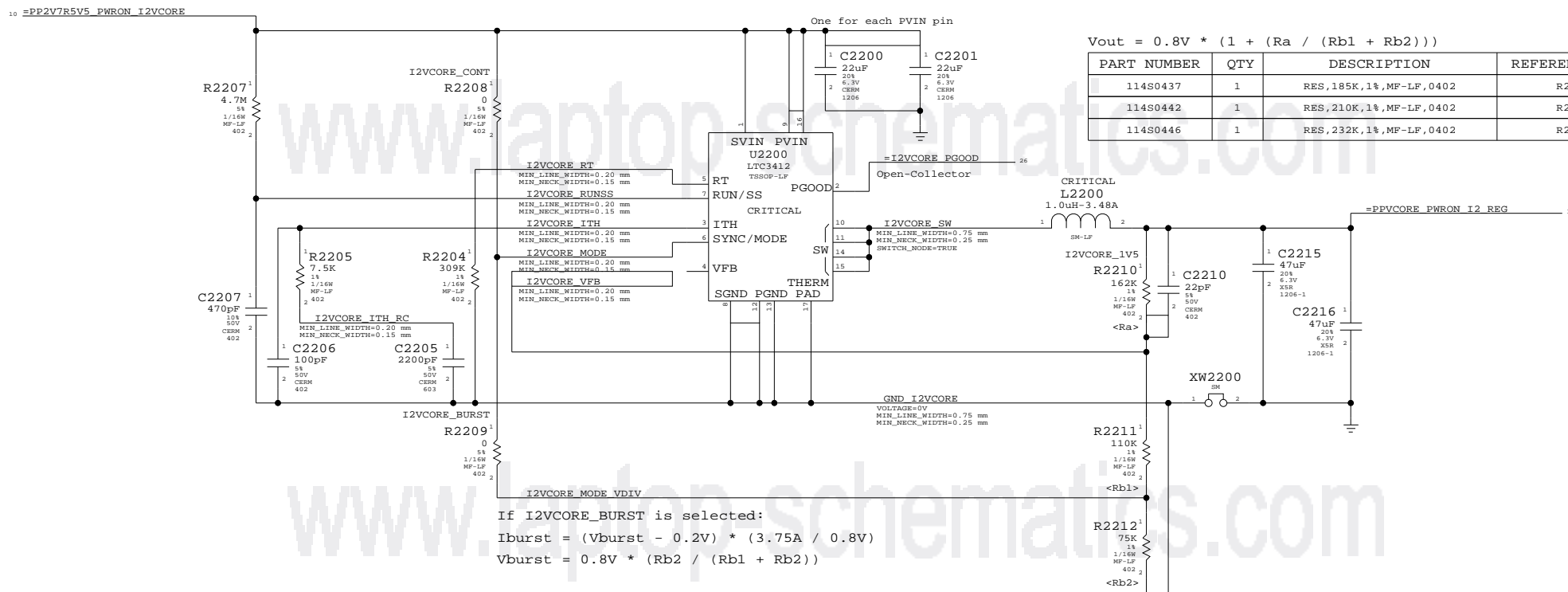
Page Notes

Power aliases required by this page:
 - =PP2V7R5V5_PWRON_I2VCORE
 - =PPVCORE_PWRON_I2_REG
 - =PPVIN_PWRON_I2PLLVD
 - =PP1V5_PWRON_I2PLLVD_LDO

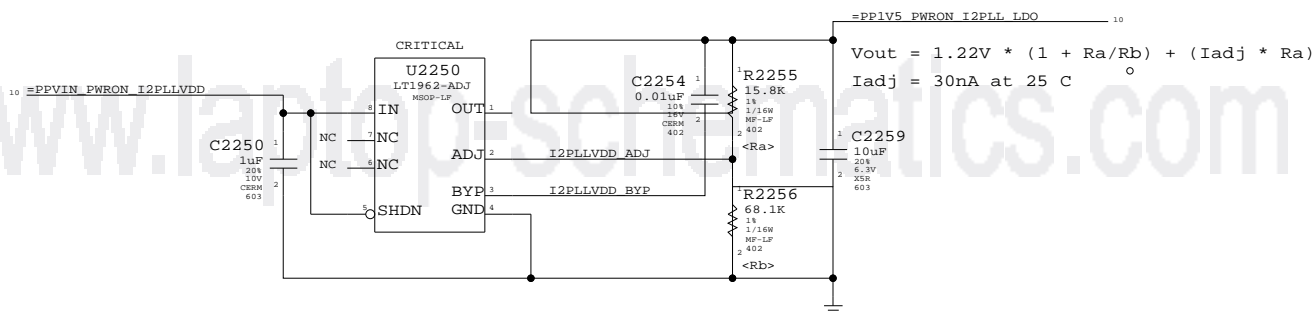
Signal aliases required by this page:
 - =I2VCORE_PGOOD

BOM options provided by this page:
 - I2VCORE_CONT / I2VCORE_BURST
 Selects between forced continuous and burst mode for LTC3412 regulator.
 - I2VCORE_XVX
 Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator



I2 PLL LDO



I2 Power Supplies
 SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT	OF	
NONE	22	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTT	I2S	128	128	
I2S0_DTO	I2S	128	128	
I2S0_MCLK	I2S	128	128	
I2S0_BITCLK	I2S	128	128	
I2S0_SYNC	I2S	128	128	
I2S1_DTT	I2S	128	128	
I2S1_DTO	I2S	128	128	
I2S1_MCLK	I2S	128	128	
I2S1_BITCLK	I2S	128	128	
I2S1_SYNC	I2S	128	128	
I2_KTAL	KTAL	KTAL	KTAL	
I2_KTAL	KTAL	KTAL	KTAL	
I2_KTAL	KTAL	KTAL	KTAL	

NET	DESCRIPTION	LOC
I2S0_DEV_TO_SB_DTT	I2S0 DEV TO SB DTT	7 22 74
I2S0_SB_TO_DEV_DTO	I2S0 SB TO DEV DTO	6 22
I2S0_MCLK_R	I2S0 MCLK R	6 22
I2S0_BITCLK_R	I2S0 BITCLK R	6 22
I2S0_SYNC_R	I2S0 SYNC R	6 22
I2S1_DEV_TO_SB_DTT	I2S1 DEV TO SB DTT	22 30
I2S1_SB_TO_DEV_DTO	I2S1 SB TO DEV DTO	6 22
I2S1_MCLK_R	I2S1 MCLK R	6 22
I2S1_BITCLK_R	I2S1 BITCLK R	6 22
I2S1_SYNC_R	I2S1 SYNC R	6 22
I2_CLK18M_XOUT_R	I2 CLK18M XOUT R	22
I2_CLK18M_XOUT	I2 CLK18M XOUT	22
I2_CLK18M_XIN	I2 CLK18M XIN	22

Page Notes

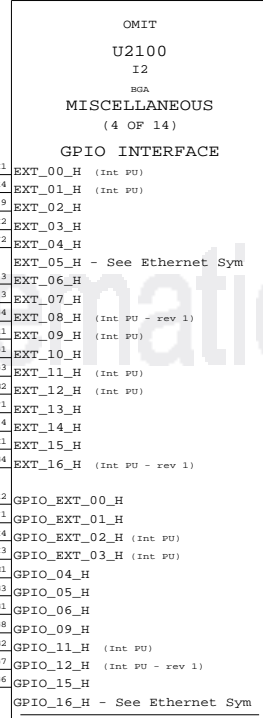
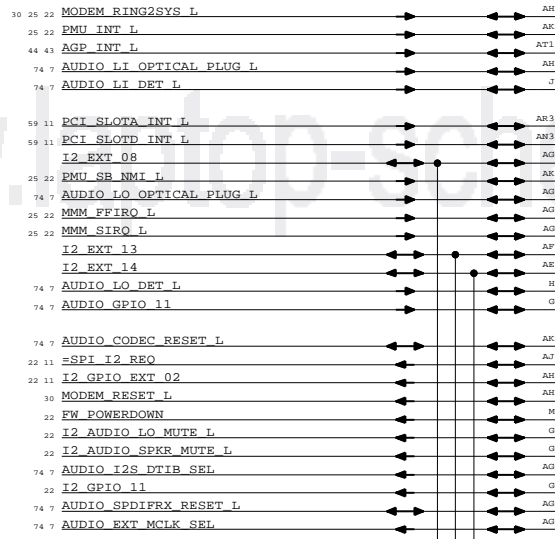
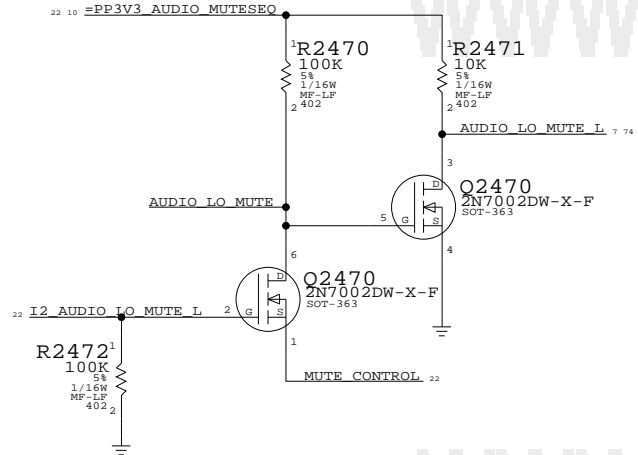
Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0

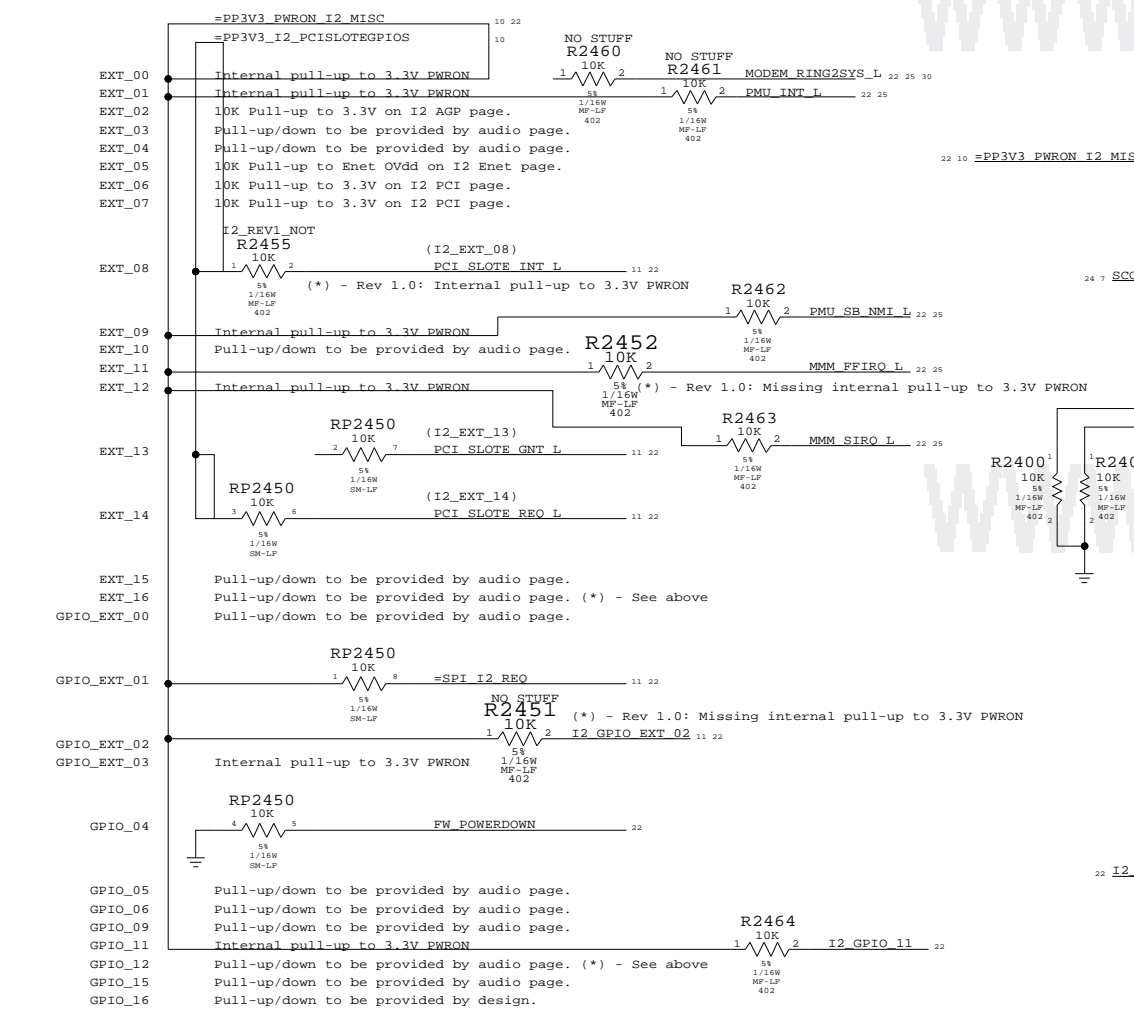
Audio Mute Sequencing

Prevents mute glitch from reaching audio circuit



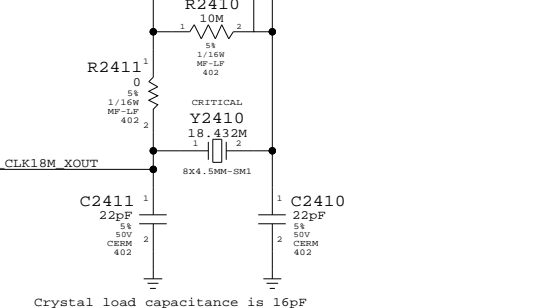
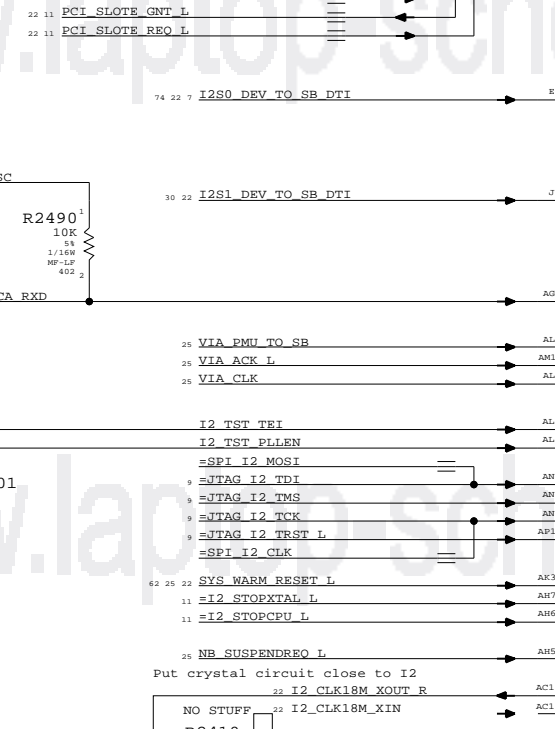
Pin	Address	MPIC	Int	Int PU?	Alt Func	
EXT_00	0x0_0058	46 (0x2E)	Yes		PCI_REQ_2_L	When PCI1_Slot2En = 10)
EXT_01	0x0_0059	47 (0x2F)	Yes			
EXT_02	0x0_005A	48 (0x30)	No			
EXT_03	0x0_005B	49 (0x31)	No			
EXT_04	0x0_005C	50 (0x32)	No			
EXT_05	0x0_005D	51 (0x33)	No			
EXT_06	0x0_005E	52 (0x34)	No			
EXT_07	0x0_005F	53 (0x35)	No			
EXT_08	0x0_0060	54 (0x36)	Yes			
EXT_09	0x0_0061	55 (0x37)	Yes			
EXT_10	0x0_0062	56 (0x38)	No			
EXT_11	0x0_0063	57 (0x39)	Yes			
EXT_12	0x0_0064	58 (0x3A)	Yes			
EXT_13	0x0_0065	59 (0x3B)	No		PCI_GNT_2_L	When PCI1_Slot2En = 11)
EXT_14	0x0_0066	60 (0x3C)	No		PCI_REQ_2_L	When PCI1_Slot2En = 11)
EXT_15	0x0_0067	61 (0x3D)	No			
EXT_16	0x0_0068	62 (0x3F)	Yes			
GPIO_00	0x0_006A	14 (0x0E)	No			
GPIO_01	0x0_006B	15 (0x0F)	No		SPIREQ	(When SPISReqEn = 1)
GPIO_02	0x0_006C	16 (0x10)	Yes		PCI_GNT_2_L	When PCI1_Slot2En = 10)
GPIO_03	0x0_006D	17 (0x11)	Yes			
GPIO_04	0x0_006E	N/A	No			
GPIO_05	0x0_006F	N/A	No			
GPIO_06	0x0_0070	N/A	No			
GPIO_09	0x0_0073	N/A	No			
GPIO_11	0x0_0075	N/A	Yes			
GPIO_12	0x0_0076	N/A	Yes			
GPIO_15	0x0_0079	N/A	No			
GPIO_16	0x0_007A	N/A	No			

GPIO Pull-ups / Pull-downs



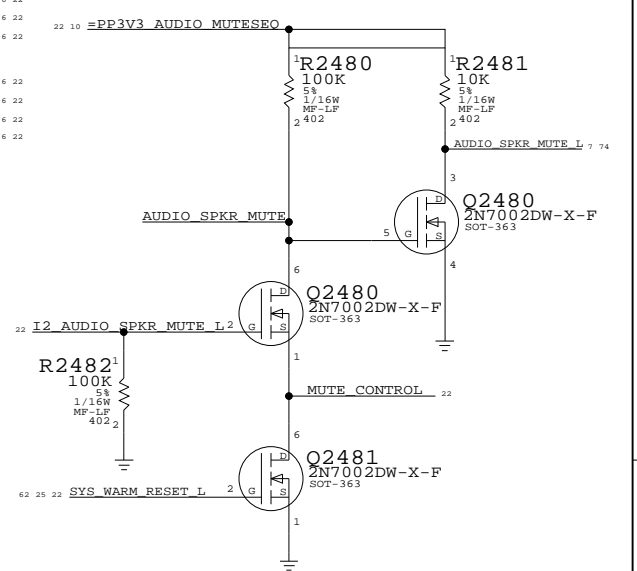
Alternate GPIO Functions

Use MAKE_BASE to force net name



Audio Mute Sequencing

Prevents mute glitch from reaching audio circuit



I2 Miscellaneous

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	
NONE	24	115	

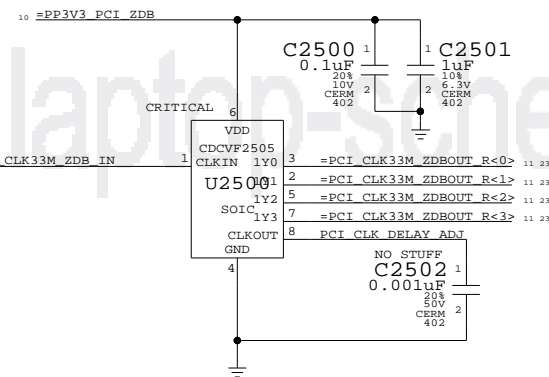
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
PCI_ZDBOUT0	CLOCK	CLOCK	
PCI_ZDBOUT1	CLOCK	CLOCK	
PCI_ZDBOUT2	CLOCK	CLOCK	
PCI_ZDBOUT3	CLOCK	CLOCK	

Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_I2_GPIO
 - =PP3V3_I2_PCISLOTGPIO (PWRON or PCI)
 Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - I2_REV1_NOT
 Use for I2 revisions > 1.0



PCI Clock Buffer

SYNC_MASTER=N/A SYNC_DATE=N/A

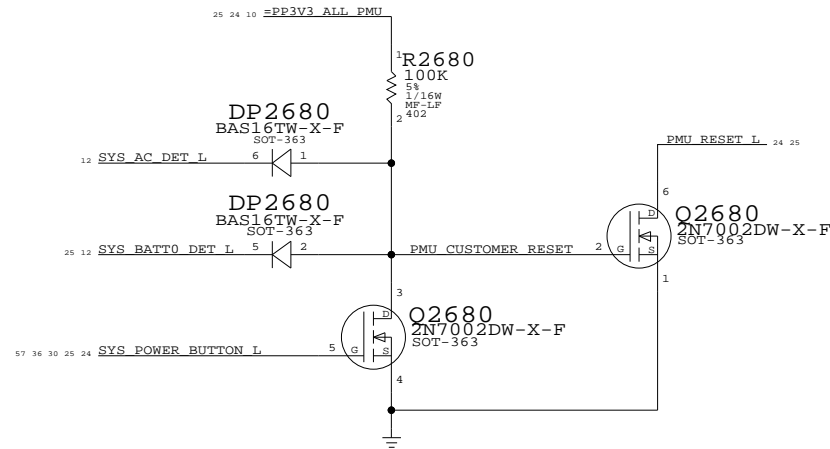
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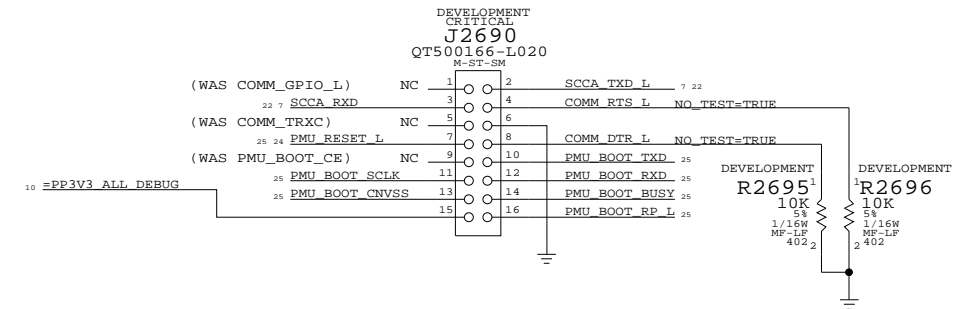
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	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	25	115	

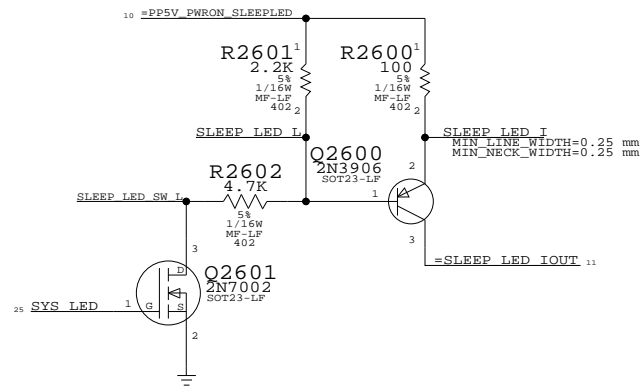
PMU RESET CIRCUIT



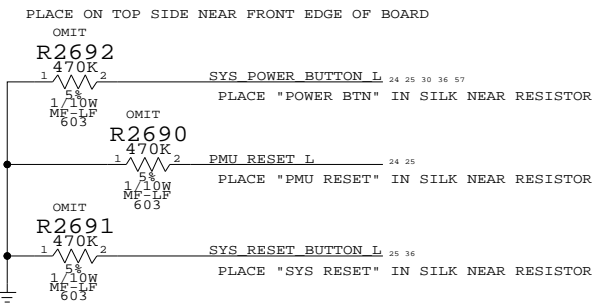
SERIAL DEBUG INTERFACE



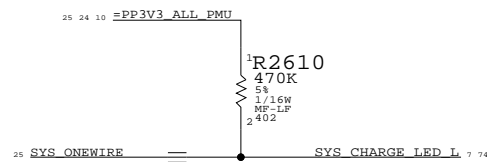
SLEEP LED



DEBUGGING AIDS



CHARGE LED



LEDs/Reset/Debug

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT	OF	
NONE	26	115	

ELECTRICAL_CONSTRAINT_SET		NET_TYPE		
		SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PMU_CLK10M_XTAL	XTAL		XTAL	PMU_CLK10M_XIN 25
	XTAL		XTAL	PMU_CLK10M_XOUT 25
	XTAL		XTAL	PMU_CLK10M_XOUT_R 25
PMU_CLK32K_XTAL	XTAL		XTAL	PMU_CLK32K_XIN 25
	XTAL		XTAL	PMU_CLK32K_XOUT 25
	XTAL		XTAL	PMU_CLK32K_XOUT_R 25

Power Management Unit

Page Notes

Power aliases required by this page:
 - =PP3V3_ALL_PMU
 - =PP3V3_PWRON_PMU
 - =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:
 - =I2C_PMU_SCL
 - =I2C_PMU_SDA
 - =I2C_PMU_SMB_SCL
 - =I2C_PMU_SMB_SDA
 - =JTAG_BBANGER_TCK
 - =JTAG_BBANGER_TDI
 - =JTAG_BBANGER_TMS
 - =JTAG_BBANGER_TRST_L

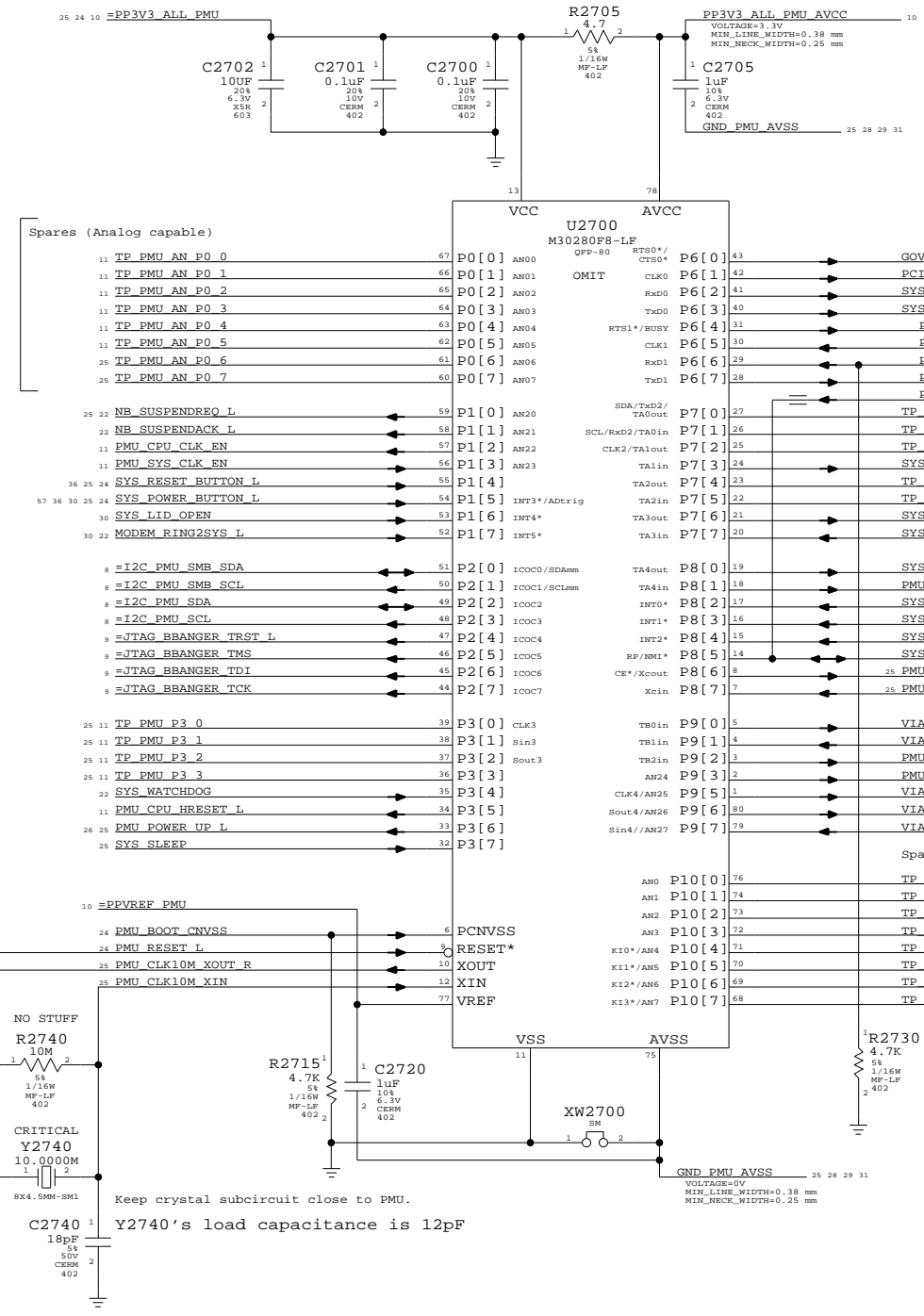
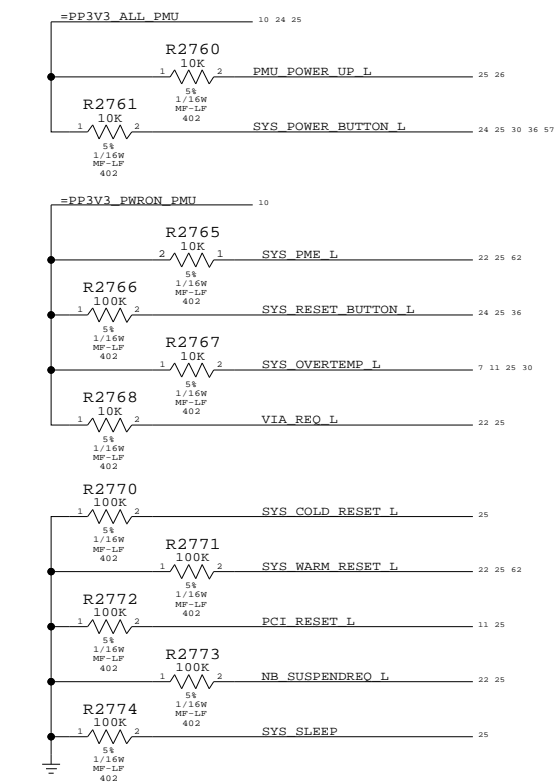
NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page:
 (NONE)

NOTE: TP_PMU_Fx_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Fx_x signals are general-purpose spares that can also be used as analog inputs.

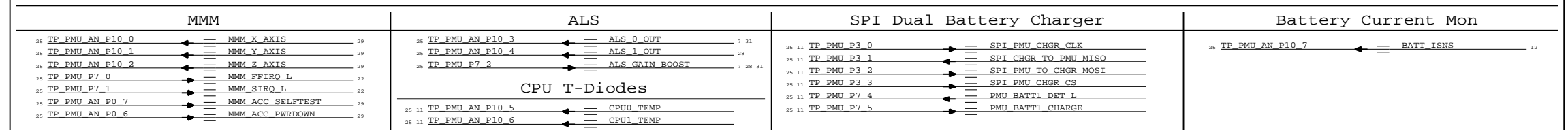
NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

PMU Pull-ups / pull-downs



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750163	1	XTAL, 32.768KHZ, 4.1X1.5X0.9MM, 4MD	Y2750	CRITICAL	?

Additional PMU05 "Modules"



Power Management Unit (PMU05)

SYNC_MASTER=N/A SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

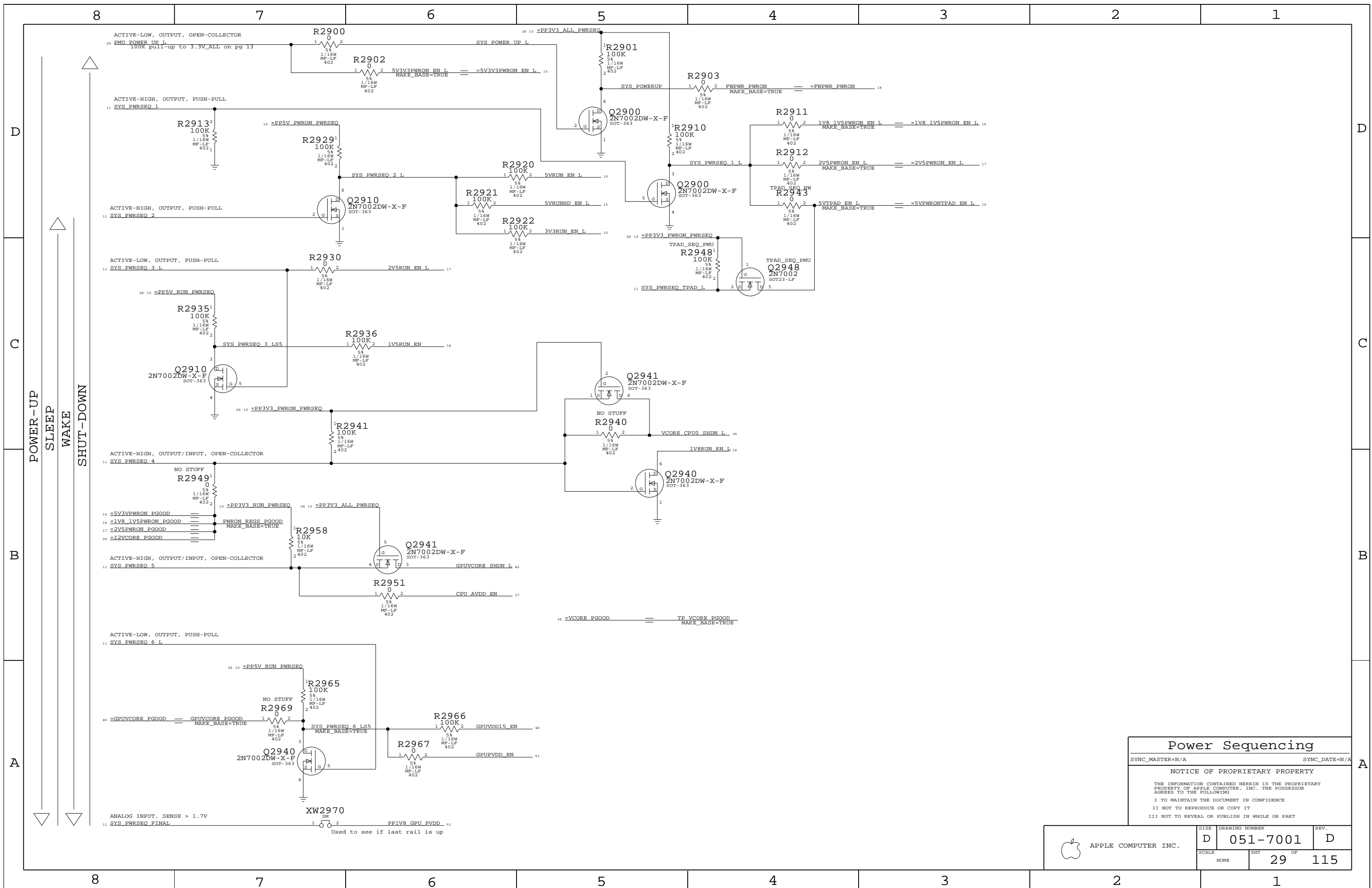
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	D	051-7001	D
SCALE	SHEET	OF	
NONE	27	115	



Power Sequencing

SYNC_MASTER=N/A SYNC_DATE=N/A

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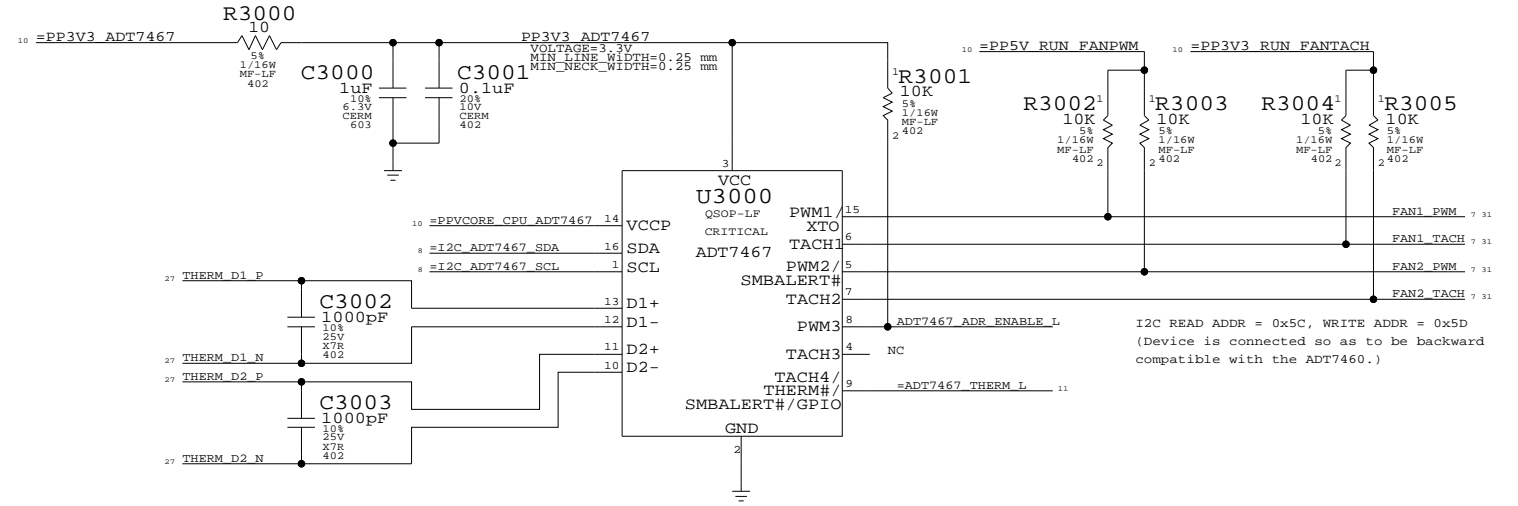
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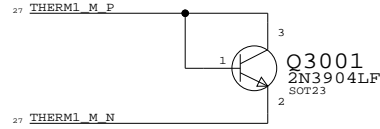
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	29	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E320	THERM	THERM	THERM1_M
E320	THERM	THERM	THERM1_M_N
E330	THERM	THERM	THERM2_M
E330	THERM	THERM	THERM2_M_N
E332	THERM	THERM	THERM1_A
E332	THERM	THERM	THERM1_A_N
E333	THERM	THERM	THERM2_A
E333	THERM	THERM	THERM2_A_N
E337	THERM	THERM	THERM_D1
E337	THERM	THERM	THERM_D1_N
E338	THERM	THERM	THERM_D2
E338	THERM	THERM	THERM_D2_N

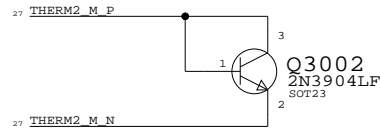
FAN CONTROLLER



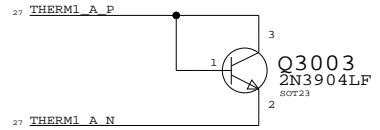
PLACE CLOSE TO CPU MAIN1



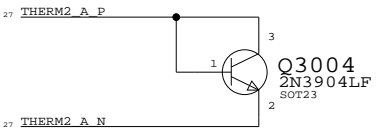
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY MAIN2



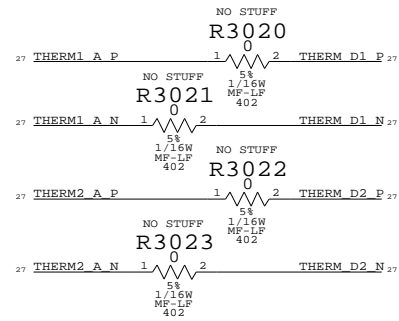
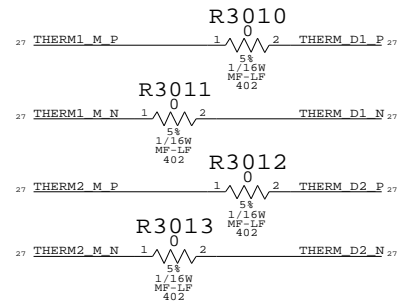
PLACE UNDERNEATH UPPER RAM ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2

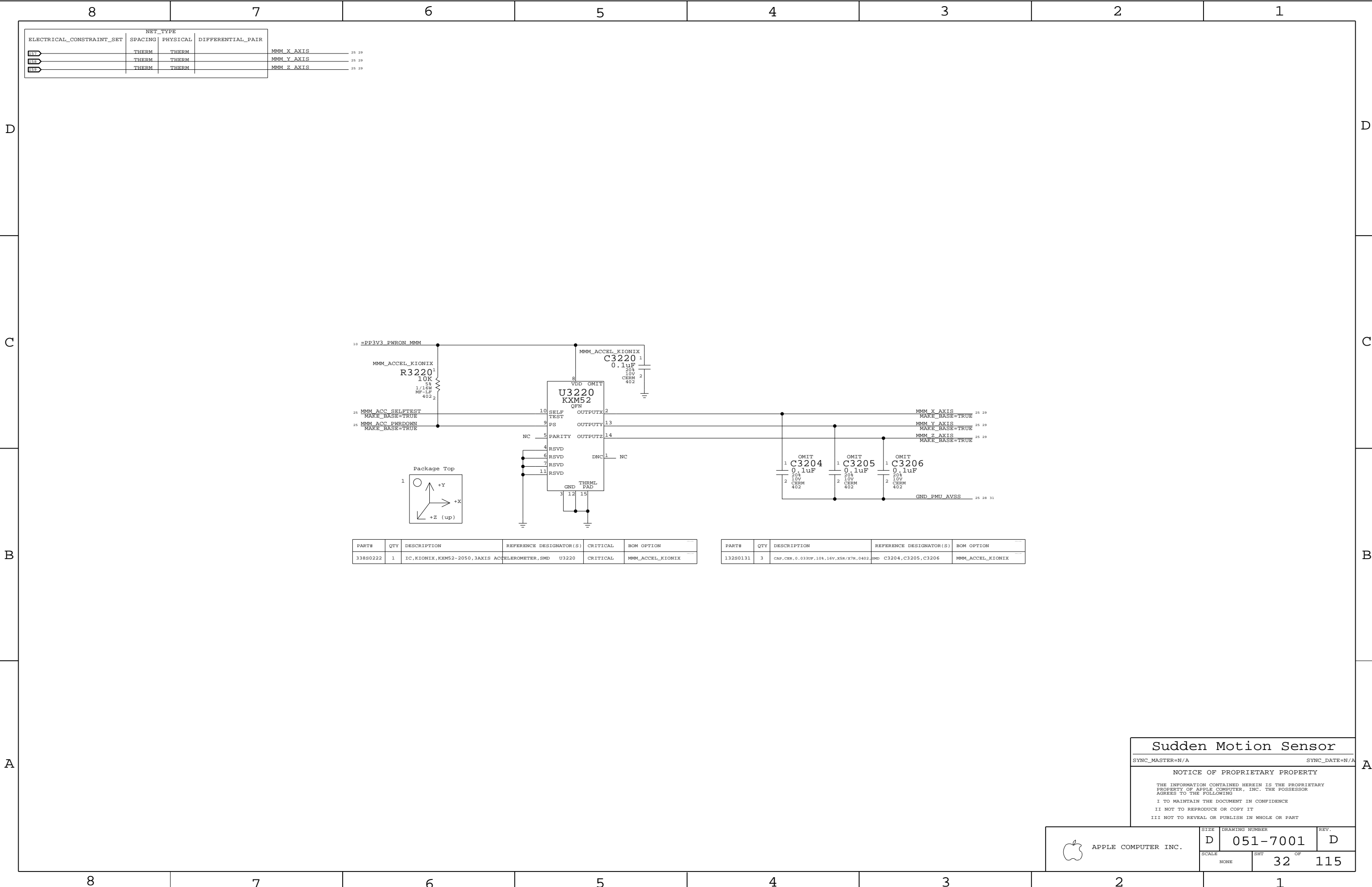


KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

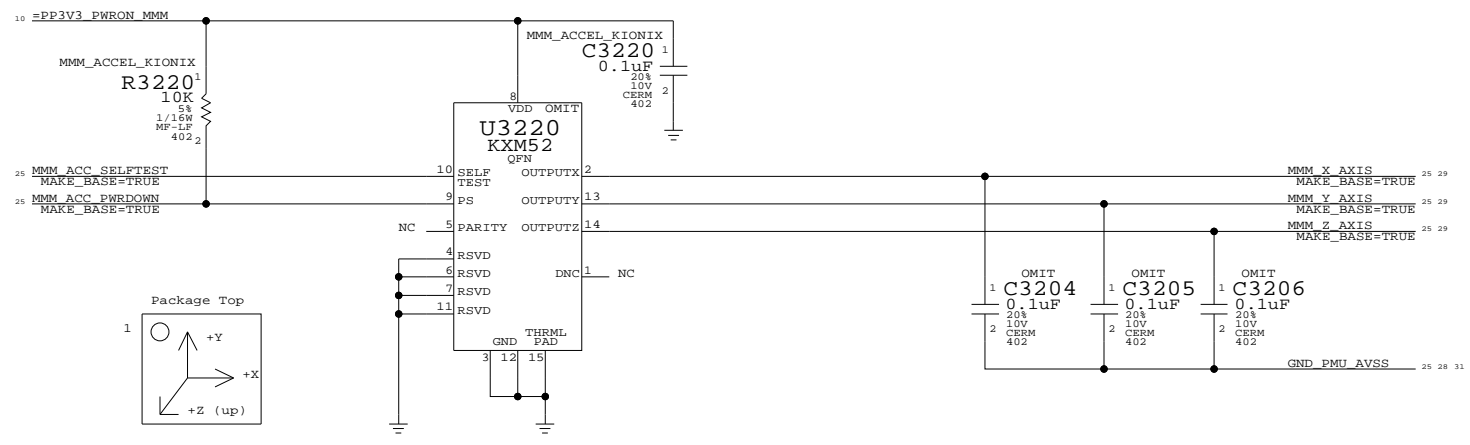


Fan Controller
 SYNC_MASTER=N/A SYNC_DATE=N/A
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT OF		REV.
NONE	30		115

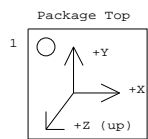


ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
ES7	THERM	THERM	MMM X AXIS
ES8	THERM	THERM	MMM Y AXIS
ES9	THERM	THERM	MMM Z AXIS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC, KIONIX, KXM52-2050, 3AXIS ACCELEROMETER, SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0131	3	CAP, CER, 0.033UF, 10%, 1.0V, XSR/X7R, 0402, SMD	C3204, C3205, C3206	MMM_ACCEL_KIONIX



Sudden Motion Sensor

SYNC_MASTER=N/A SYNC_DATE=N/A

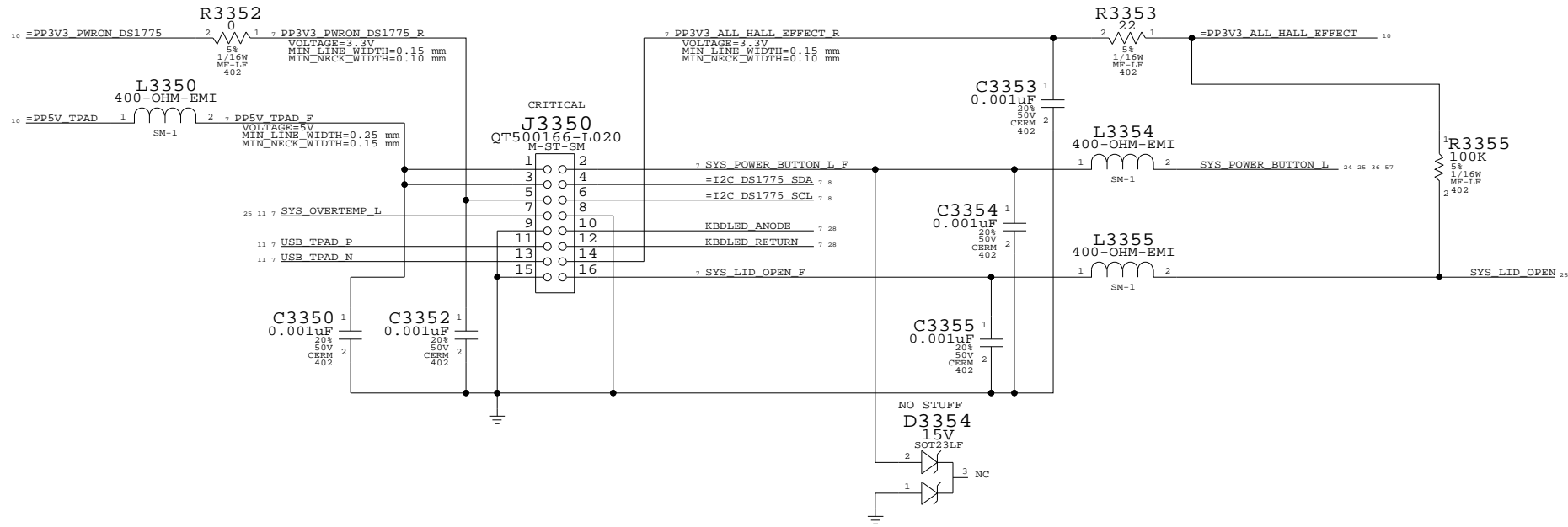
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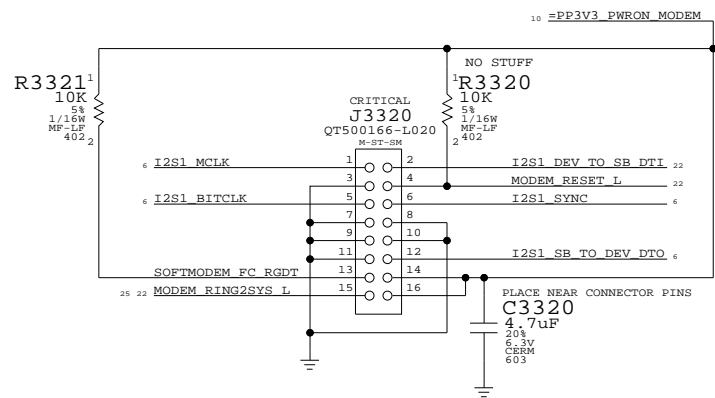
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SCALE	SHT OF		
NONE	32 OF		115

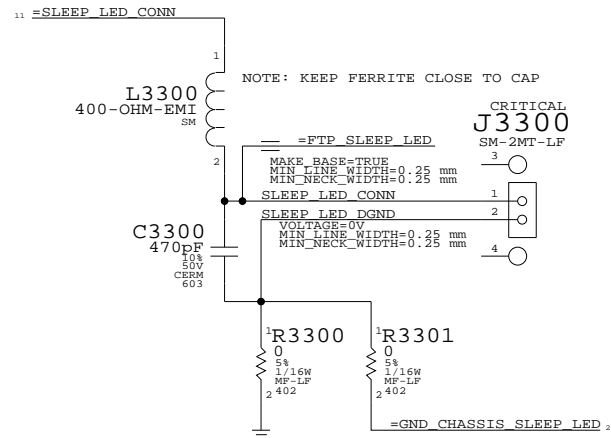
USB Trackpad Connector



SOFT MODEM CONN



SLEEP LED CONNECTOR



Q16C Internal I/O I

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		33	115

8

7

6

5

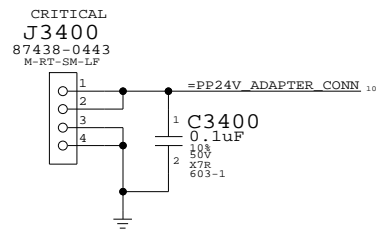
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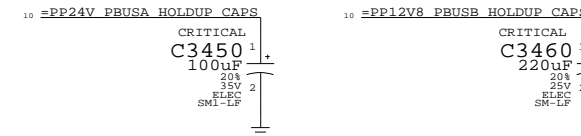
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1

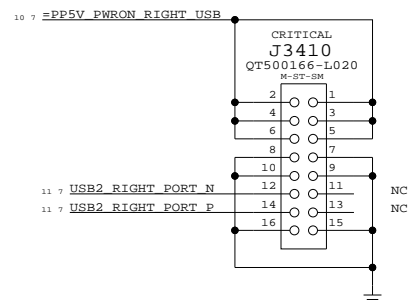
ADAPTER CONNECTOR



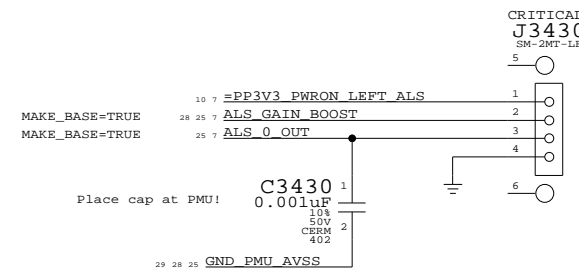
PBUS HOLD-UP CAPS



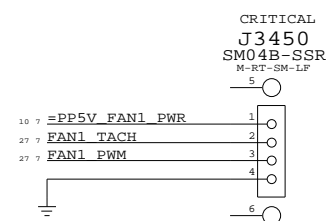
RIGHT USB BOARD



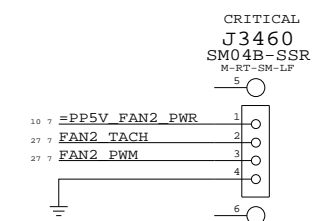
LEFT ALS CONNECTOR



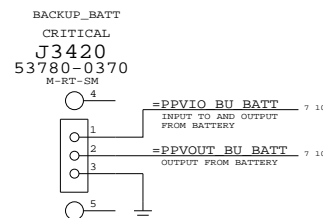
CPU FAN



GPU FAN



BACKUP BATTERY CONNECTOR



Q16C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	NONE	SHT	OF
		34	115

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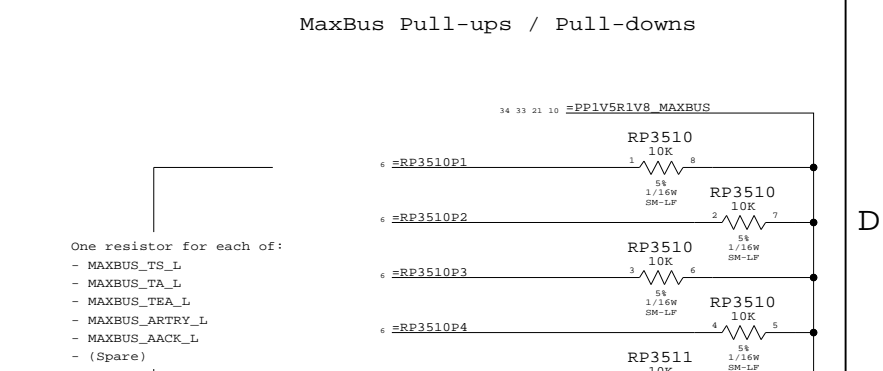
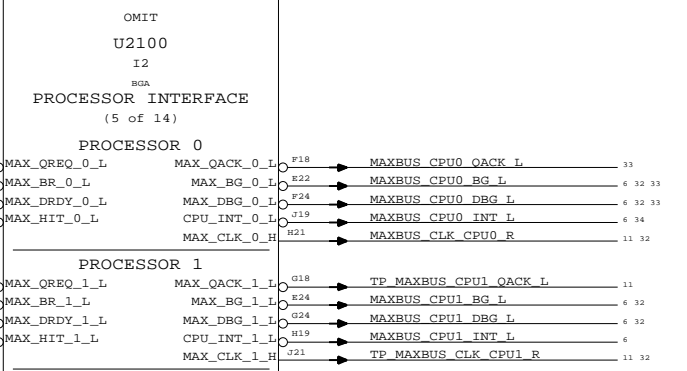
4

3

2

1

ELECTRICAL_CONSTRAINT_SET		NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
MAXBUS_CLK_CPU0	CLOCK	CLOCK		MAXBUS_CLK_CPU0_R	11 32
MAXBUS_CLK_CPU1	CLOCK	CLOCK		TP_MAXBUS_CLK_CPU1_R	11 32
I2_MAXBUS_FBCLK	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_OUT_R	32
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_OUT	21 32
MAXBUS_CPU0_B1N0	MAXBUS	MAXBUS		MAXBUS_ADDR<0..31>	9 32 33
MAXBUS_CPU0_B1N1	MAXBUS	MAXBUS		MAXBUS_DATA<0..40>	9 32 33
MAXBUS_DATA41	MAXBUS	MAXBUS		MAX_ADDR<41>	33 32
MAXBUS_DATA42	MAXBUS	MAXBUS		MAXBUS_DATA<42>	9 32 33
MAXBUS_DATA43	MAXBUS	MAXBUS		MAXBUS_DATA<43>	9 32 33
MAXBUS_DATA44	MAXBUS	MAXBUS		MAXBUS_DATA<44>	9 32 33
MAXBUS_CPU0_B1N2	MAXBUS	MAXBUS		MAXBUS_DATA<45..53>	9 32 33
MAXBUS_DATA54	MAXBUS	MAXBUS		MAX_ADDR<54>	33 32
MAXBUS_CPU0_B1N3	MAXBUS	MAXBUS		MAXBUS_DATA<55..61>	9 32 33
MAXBUS_DATA62	MAXBUS	MAXBUS		MAX_ADDR<62>	33 32
MAXBUS_CPU0_B1N4	MAXBUS	MAXBUS		MAXBUS_DATA<63>	9 32 33
MAXBUS_CPU0_B1N5	MAXBUS	MAXBUS		MAXBUS_TS_L	6 32 33
MAXBUS_CPU0_B1N6	MAXBUS	MAXBUS		MAXBUS_TA_L	6 32 33
MAXBUS_CPU0_B1N7	MAXBUS	MAXBUS		MAXBUS_TEA_L	6 32 33
MAXBUS_CPU0_B1N8	MAXBUS	MAXBUS		MAXBUS_AACK_L	6 32 33
MAXBUS_CPU0_B1N9	MAXBUS	MAXBUS		MAXBUS_ARTRY_L	6 32 33
MAXBUS_CPU0_B1N10	MAXBUS	MAXBUS		MAXBUS_CI_L	6 32 33
MAXBUS_CPU0_B1N11	MAXBUS	MAXBUS		MAXBUS_DTI<0..2>	9 32 33
MAXBUS_CPU0_B1N12	MAXBUS	MAXBUS		MAXBUS_GBL_L	9 32 33
MAXBUS_CPU0_B1N13	MAXBUS	MAXBUS		MAXBUS_TBST_L	9 32 33
MAXBUS_CPU0_B1N14	MAXBUS	MAXBUS		MAXBUS_TSIZ<0..2>	9 32 33
MAXBUS_CPU0_B1N15	MAXBUS	MAXBUS		MAXBUS_TT<0..4>	9 32 33
MAXBUS_CPU0_B1N16	MAXBUS	MAXBUS		MAXBUS_WT_L	9 32 33
MAXBUS_CPU0_B1N17	MAXBUS	MAXBUS		MAXBUS_CPU0_BG_L	6 32 33
MAXBUS_CPU0_B1N18	MAXBUS	MAXBUS		MAXBUS_CPU0_DR_L	6 32 33
MAXBUS_CPU0_B1N19	MAXBUS	MAXBUS		MAXBUS_CPU0_DRDY_L	6 32 33
MAXBUS_CPU0_B1N20	MAXBUS	MAXBUS		MAXBUS_CPU0_HIT_L	6 32 33
MAXBUS_CPU0_B1N21	MAXBUS	MAXBUS		MAXBUS_CPU1_BG_L	6 32 33
MAXBUS_CPU0_B1N22	MAXBUS	MAXBUS		MAXBUS_CPU1_DR_L	6 32 33
MAXBUS_CPU0_B1N23	MAXBUS	MAXBUS		MAXBUS_CPU1_DRDY_L	6 32 33
MAXBUS_CPU0_B1N24	MAXBUS	MAXBUS		MAXBUS_CPU1_HIT_L	6 32 33

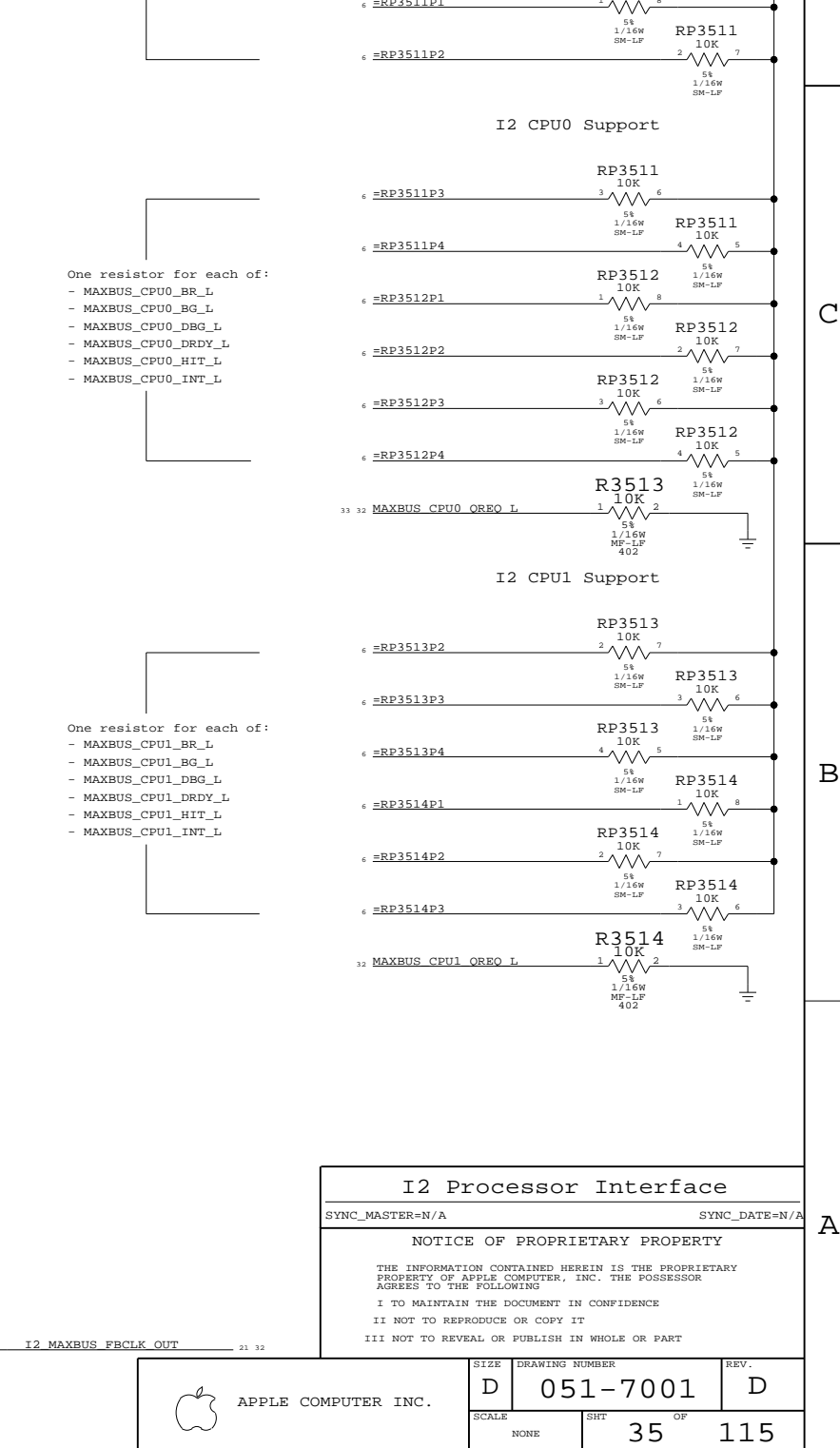
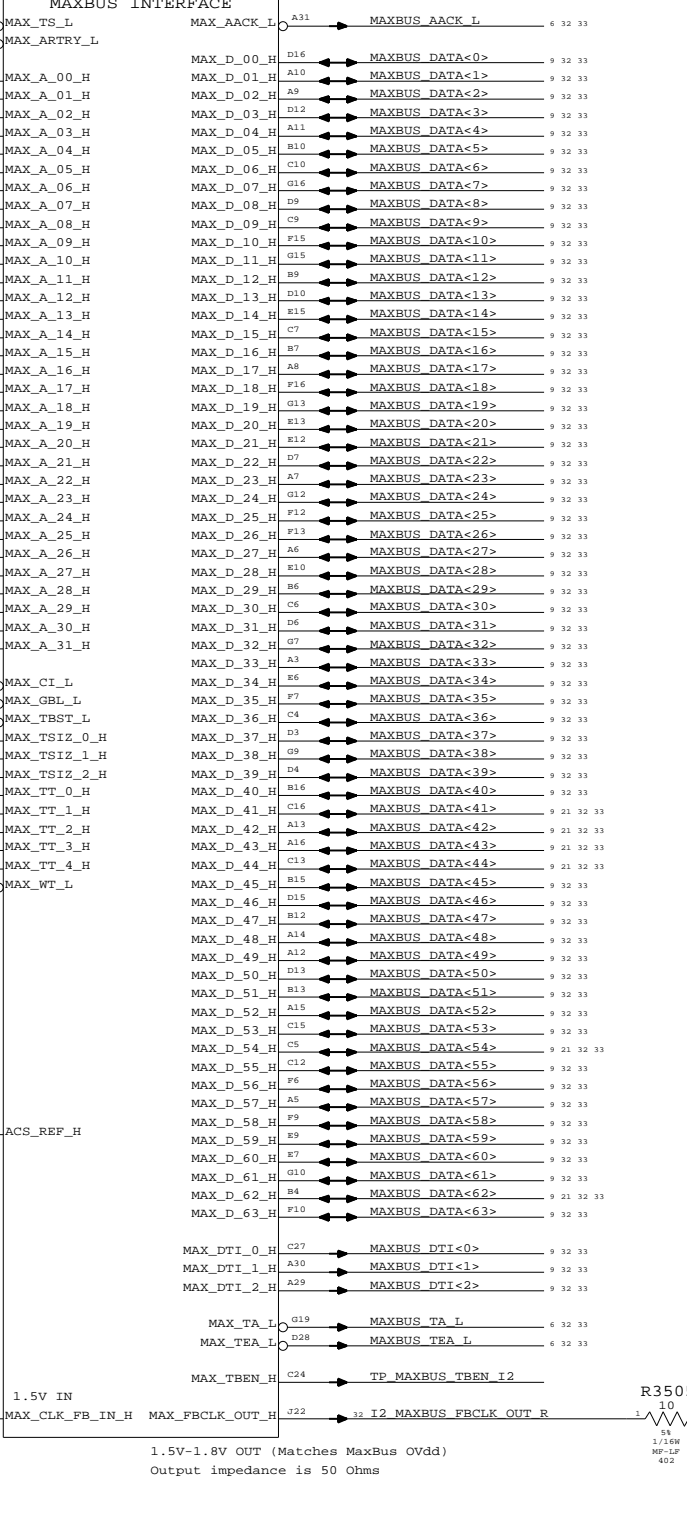
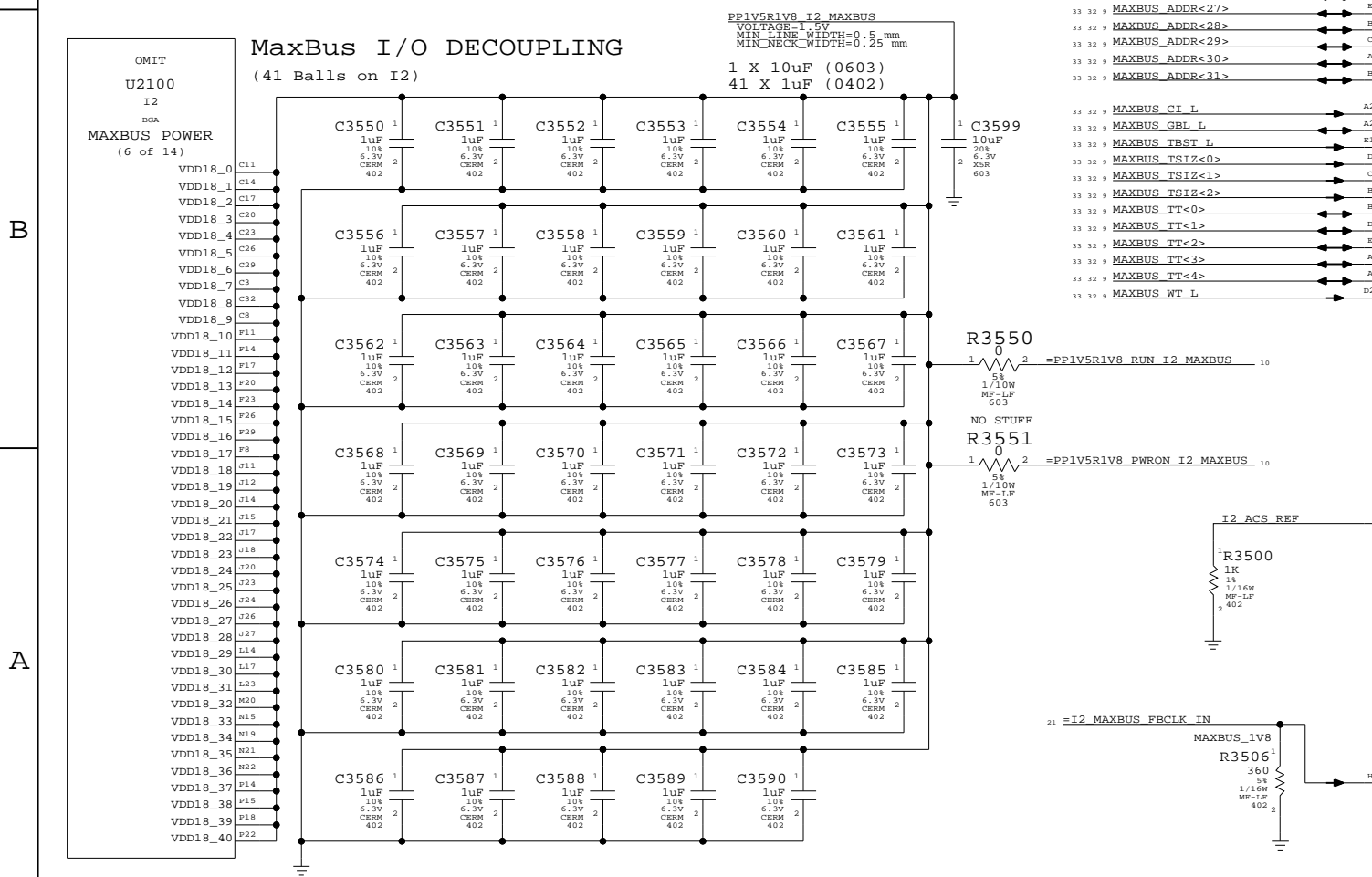


Page Notes

Power aliases required by this page:
 - =PPIV5R1V8_RUN_I2_MAXBUS - =PPIV5R1V8_PWRON_I2_MAXBUS

BOM options provided by this page:
 - MAXBUS_LV8 - Provides required voltage divider for FBCLK if MaxBus Ovdd=1.8V.

Signal aliases required by this page:
 - =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).



I2 Processor Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS	CLOCK	CLOCK		

Page Notes

Power aliases required by this page:
 - =PPIV5R1V8_MAXBUS

Signal aliases required by this page:
 - =MAXBUS_CPU0_CLK

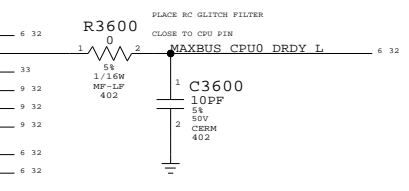
BOM options provided by this page:
 (NONE)

- 32 9 MAXBUS_DATA<0> R15 D0
- 32 9 MAXBUS_DATA<1> M15 D1
- 32 9 MAXBUS_DATA<2> T14 D2
- 32 9 MAXBUS_DATA<3> V16 D3
- 32 9 MAXBUS_DATA<4> W16 D4
- 32 9 MAXBUS_DATA<5> T15 D5
- 32 9 MAXBUS_DATA<6> U15 D6
- 32 9 MAXBUS_DATA<7> P14 D7
- 32 9 MAXBUS_DATA<8> V13 D8
- 32 9 MAXBUS_DATA<9> M13 D9
- 32 9 MAXBUS_DATA<10> T13 D10
- 32 9 MAXBUS_DATA<11> P13 D11
- 32 9 MAXBUS_DATA<12> U14 D12
- 32 9 MAXBUS_DATA<13> M14 D13
- 32 9 MAXBUS_DATA<14> R12 D14
- 32 9 MAXBUS_DATA<15> T12 D15
- 32 9 MAXBUS_DATA<16> M12 D16
- 32 9 MAXBUS_DATA<17> V12 D17
- 32 9 MAXBUS_DATA<18> M11 D18
- 32 9 MAXBUS_DATA<19> M10 D19
- 32 9 MAXBUS_DATA<20> R11 D20
- 32 9 MAXBUS_DATA<21> U11 D21
- 32 9 MAXBUS_DATA<22> M11 D22
- 32 9 MAXBUS_DATA<23> T11 D23
- 32 9 MAXBUS_DATA<24> R10 D24
- 32 9 MAXBUS_DATA<25> M9 D25
- 32 9 MAXBUS_DATA<26> P10 D26
- 32 9 MAXBUS_DATA<27> U10 D27
- 32 9 MAXBUS_DATA<28> R9 D28
- 32 9 MAXBUS_DATA<29> M10 D29
- 32 9 MAXBUS_DATA<30> U9 D30
- 32 9 MAXBUS_DATA<31> V9 D31
- 32 9 MAXBUS_DATA<32> W5 D32
- 32 9 MAXBUS_DATA<33> U6 D33
- 32 9 MAXBUS_DATA<34> T5 D34
- 32 9 MAXBUS_DATA<35> U5 D35
- 32 9 MAXBUS_DATA<36> W7 D36
- 32 9 MAXBUS_DATA<37> R6 D37
- 32 9 MAXBUS_DATA<38> P7 D38
- 32 9 MAXBUS_DATA<39> V6 D39
- 32 9 MAXBUS_DATA<40> P17 D40
- 32 21 MAXBUS_DATA<41> R19 D41
- 32 21 MAXBUS_DATA<42> V18 D42
- 32 21 MAXBUS_DATA<43> R18 D43
- 32 21 MAXBUS_DATA<44> V19 D44
- 32 9 MAXBUS_DATA<45> T19 D45
- 32 9 MAXBUS_DATA<46> U19 D46
- 32 9 MAXBUS_DATA<47> M19 D47
- 32 9 MAXBUS_DATA<48> U18 D48
- 32 9 MAXBUS_DATA<49> M17 D49
- 32 9 MAXBUS_DATA<50> M18 D50
- 32 9 MAXBUS_DATA<51> T18 D51
- 32 9 MAXBUS_DATA<52> T18 D52
- 32 9 MAXBUS_DATA<53> T17 D53
- 32 21 MAXBUS_DATA<54> M3 D54
- 32 9 MAXBUS_DATA<55> V17 D55
- 32 9 MAXBUS_DATA<56> U4 D56
- 32 9 MAXBUS_DATA<57> U8 D57
- 32 9 MAXBUS_DATA<58> U7 D58
- 32 9 MAXBUS_DATA<59> R7 D59
- 32 9 MAXBUS_DATA<60> P6 D60
- 32 9 MAXBUS_DATA<61> R8 D61
- 32 21 MAXBUS_DATA<62> W8 D62
- 32 9 MAXBUS_DATA<63> T8 D63

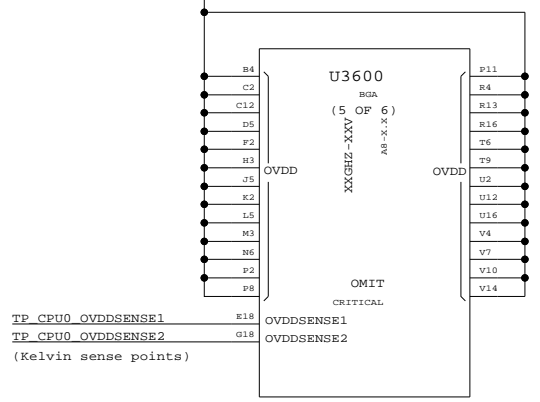
U3600
 BGA
 (2 OF 6)
 XXGHZ-XXV
 AB-X-X

OMIT
 CRITICAL

- DP0 T3 NC
- DP1 W4 NC
- DP2 T4 NC
- DP3 W5 NC
- DP4 M6 NC
- DP5 V3 NC
- DP6 N8 NC
- DP7 W6 NC
- DBG* M2 MAXBUS_CPU0_DBG_L
- DRDY* R3 MAXBUS_CPU0_DRDY_L R
- DTIO G1 MAXBUS_EDTI
- DTI1 K1 MAXBUS_DTI<0>
- DTI2 P1 MAXBUS_DTI<1>
- DTI3 N1 MAXBUS_DTI<2>
- TA* K6 MAXBUS_TA_L
- TEA* L1 MAXBUS_TEA_L
- HIT* R2 MAXBUS_CPU0_HIT_L

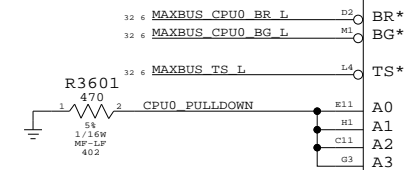


34 33 32 21 10 =PPIV5R1V8_MAXBUS



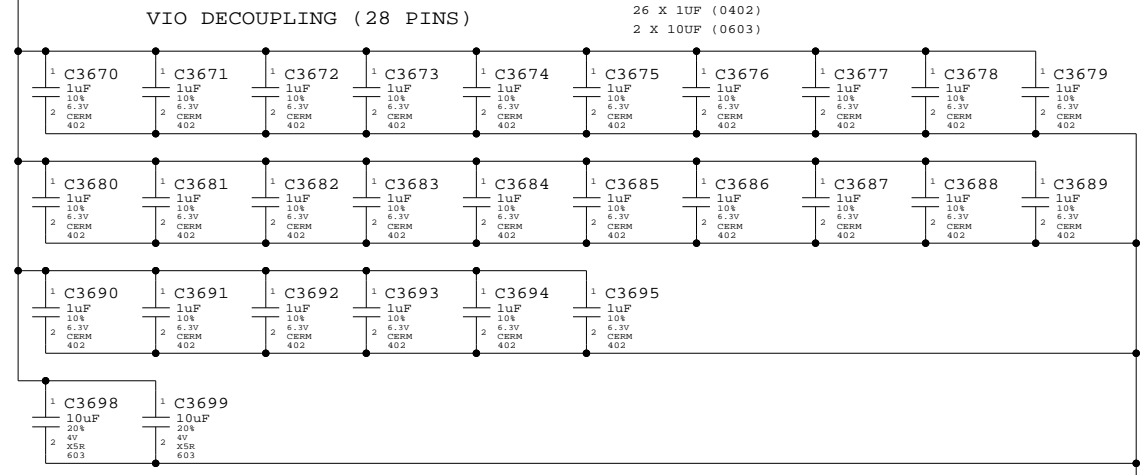
U3600
 BGA
 (1 OF 6)
 XXGHZ-XXV
 AB-X-X

OMIT
 CRITICAL

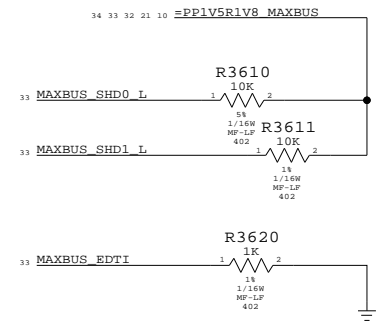


- AP0 C1 NC
- AP1 R3 NC
- AP2 H6 NC
- AP3 P5 NC
- AP4 G7 NC
- TT0 R5 MAXBUS_TT<0>
- TT1 R6 MAXBUS_TT<1>
- TT2 P6 MAXBUS_TT<2>
- TT3 R9 MAXBUS_TT<3>
- TT4 C5 MAXBUS_TT<4>
- TBST* P11 MAXBUS_TBST_L
- TSIZ0 G6 MAXBUS_TSIZ<0>
- TSIZ1 P7 MAXBUS_TSIZ<1>
- TSIZ2 R7 MAXBUS_TSIZ<2>
- GBL* R2 MAXBUS_GBL_L
- WT* D3 MAXBUS_WT_L
- CI* J1 MAXBUS_CI_L
- AACK* R1 MAXBUS_AACK_L
- ARTRY* N2 MAXBUS_ARTRY_L
- SHD0* R4 MAXBUS_SHD0_L
- SHD1* H5 MAXBUS_SHD1_L
- SYSCLK A10 =MAXBUS_CPU0_CLK
- CLK_OUT H2 TP_CPU0_CLKOUT
- TBEN R1 MAXBUS_TBEN
- QREQ* P4 MAXBUS_CPU0_QREQ_L
- QACK* G5 MAXBUS_CPU0_QACK_L
- CKSTP_IN* A3
- CKSTP_OUT* B1 CPU_CHKSTP_OUT_L

=PPIV5R1V8_MAXBUS 10 21 32 33 34



MAXBUS Straps



A8 MaxBus (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=08/02/2005

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	D	051-7001	D
SCALE	NONE	SHT	OF
		36	115

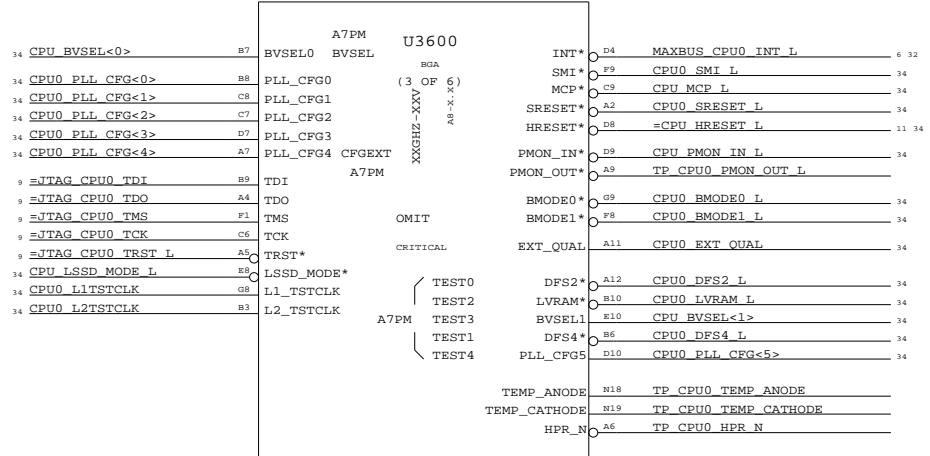
Page Notes

Power aliases required by this page:

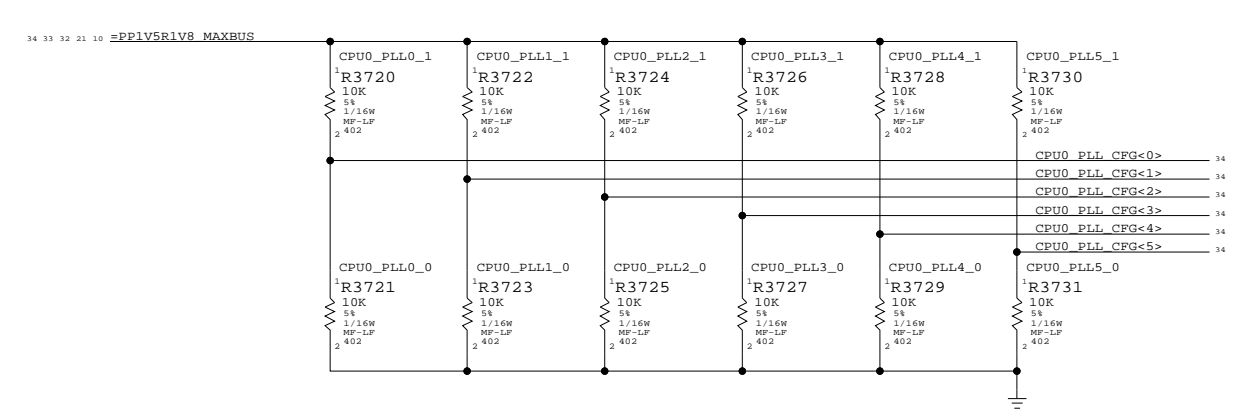
- =PPIV5R1V8_MAXBUS
 - =PP3V3_PWRON_PLLSEL
- Signal aliases required by this page:
- =CPU0_JTAG_TDI
 - =CPU0_JTAG_TDO
 - =CPU0_JTAG_TMS
 - =CPU0_JTAG_TCK
 - =CPU0_JTAG_TRST_L
 - =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:

- CPU0_PLL0_0/1
 - CPU0_PLL1_0/1
 - CPU0_PLL2_0/1
 - CPU0_PLL3_0/1
 - CPU0_PLL4_0/1
 - CPU0_PLL5_0/1
- These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec
- MAXBUS_1V5 - MAXBUS_1V8
- One of these must be selected to set the Maxbus voltage
- * the MAXBUS_1V5 option does not exist for A7PM
 - CPU_A7PM - CPU_A8
- One of these must be selected to ensure the the above strap is interpreted correctly

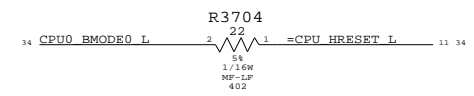


CPU0 PLL CONFIG CIRCUITRY

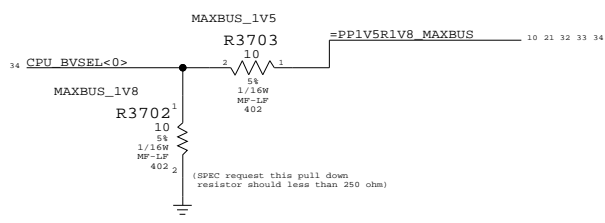


BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE



MAXBUS VSEL



A7PM

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
2.5V INTERFACE	CPU_HRESET_L	OVDD
RESERVED(1.5V)	CPU_HRESET_INV	OVDD

A8

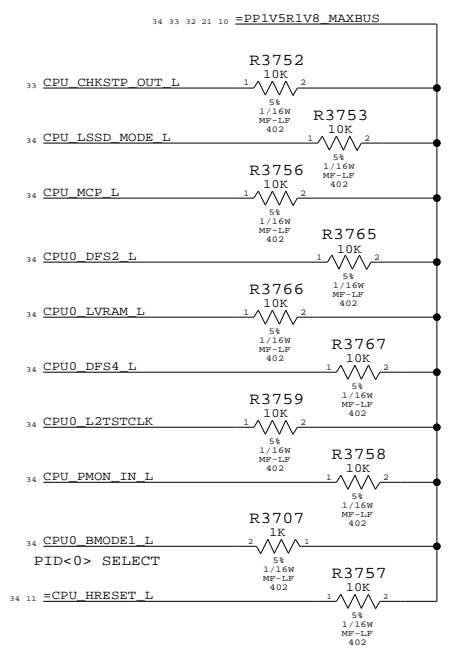
OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	GND
1.5V INTERFACE	OVDD	GND
RESERVED	CPU_HRESET_L	GND
RESERVED	CPU_HRESET_INV	GND
2.5V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
RESERVED	CPU_HRESET_L	OVDD
RESERVED	CPU_HRESET_INV	OVDD

CPU0 FREQUENCY CONFIGURATION

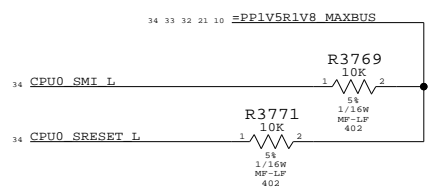
() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT	F/2	F/4	PLL BITS 012345	BOM OPTIONS
CPU0_BUSRATIO_1_0X	-	-	-	001100	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_2_0X	-	-	-	010000	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_3_0X	-	-	-	100000	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_4_0X	2.0X	-	-	101000	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_5_0X	2.5X	-	-	101100	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_5_5X	(2.75X)	-	-	100100	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_6_0X	3.0X	-	-	110100	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_6_5X	(3.25X)	-	-	010100	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_7_0X	3.5X	-	-	001000	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_7_5X	(3.75X)	-	-	000100	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_8_0X	4.0X	2.0X	-	110000	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_8_5X	(4.25X)	-	-	011000	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_9_0X	4.5X	(2.25X)	-	011110	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_9_5X	(4.75X)	-	-	011100	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_10_0X	5.0X	2.5X	-	101010	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_10_5X	(5.25X)	-	-	100010	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_11_0X	5.5X	(2.75X)	-	100110	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_11_5X	(5.75X)	-	-	000000	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_12_0X	6.0X	3.0X	-	101110	CPU0_PLL0_1, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_12_5X	(6.25X)	-	-	111110	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_13_0X	6.5X	(3.25X)	-	010110	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_13_5X	(6.75X)	-	-	111000	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_0, CPU0_PLL5_0
CPU0_BUSRATIO_14_0X	7.0X	3.5X	-	110010	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_15_0X	7.5X	(3.75X)	-	000110	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_16_0X	8.0X	4.0X	-	110110	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_17_0X	8.5X	(4.25X)	-	000010	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_18_0X	9.0X	4.5X	-	001010	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_20_0X	10.0X	5.0X	-	001110	CPU0_PLL0_0, CPU0_PLL1_0, CPU0_PLL2_1, CPU0_PLL3_1, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_21_0X	10.5X	(5.25X)	-	010010	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_0, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_24_0X	12.0X	6.0X	-	011010	CPU0_PLL0_0, CPU0_PLL1_1, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0
CPU0_BUSRATIO_28_0X	14.0X	7.0X	-	111010	CPU0_PLL0_1, CPU0_PLL1_1, CPU0_PLL2_1, CPU0_PLL3_0, CPU0_PLL4_1, CPU0_PLL5_0

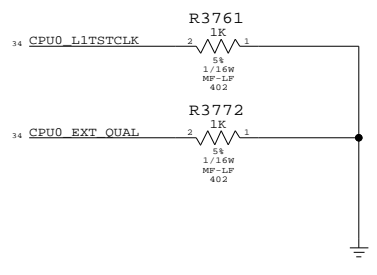
CPU PULLUPS



INTERRUPT PULL-UPS



CPU PULLDOWNS



A8 Configuration Straps

SYNC_MASTER=MULLET SYNC_DATE=08/02/2005

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SCALE	SHT	OF	
NONE	37	115	

Page Notes

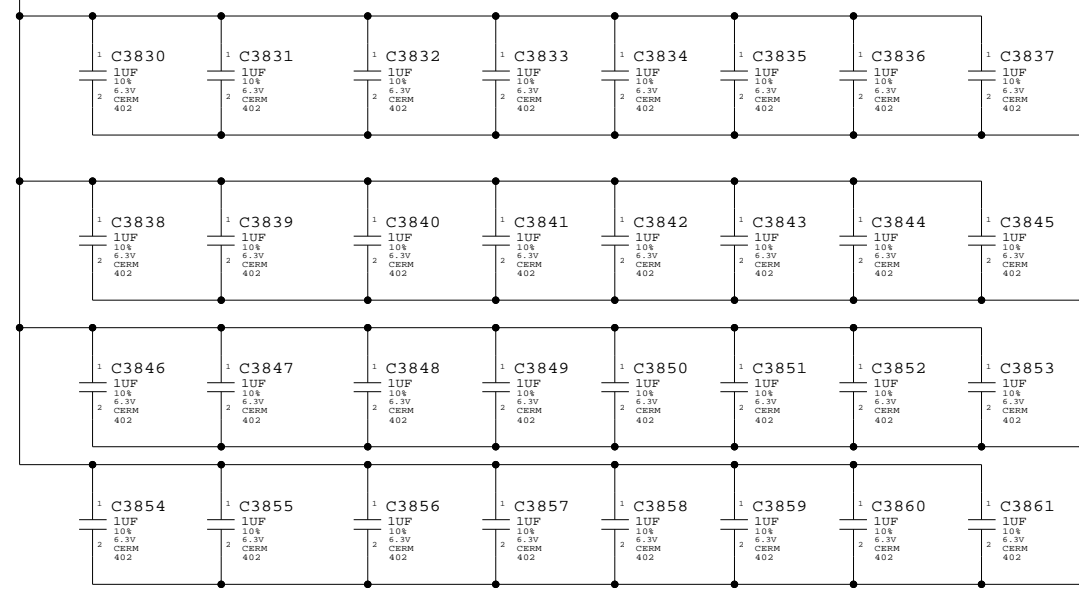
Power aliases required by this page:
 - =PPVCORE_CPU0

Signal aliases required by this page:
 (NONE)

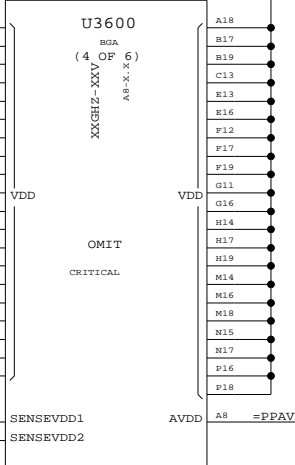
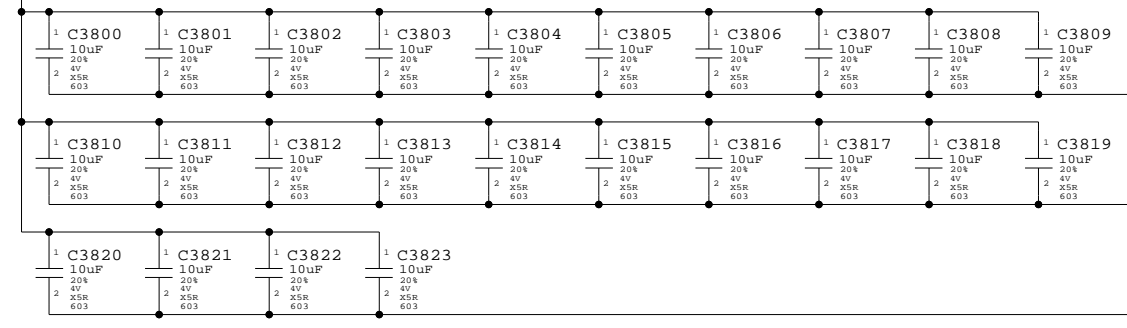
BOM options provided by this page:
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VCORE BULK CAPS

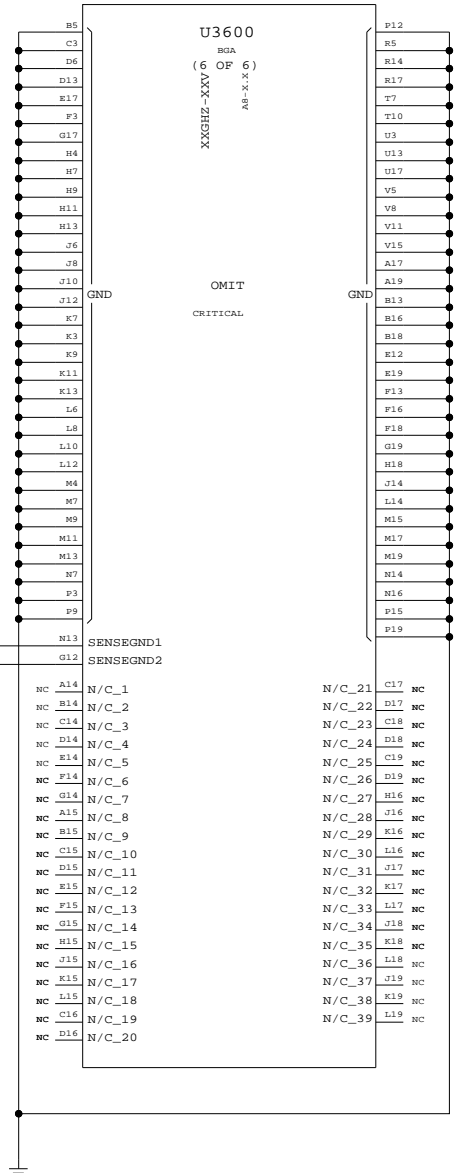
40 X 1 UF (0402)



24 X 10 UF (0603)



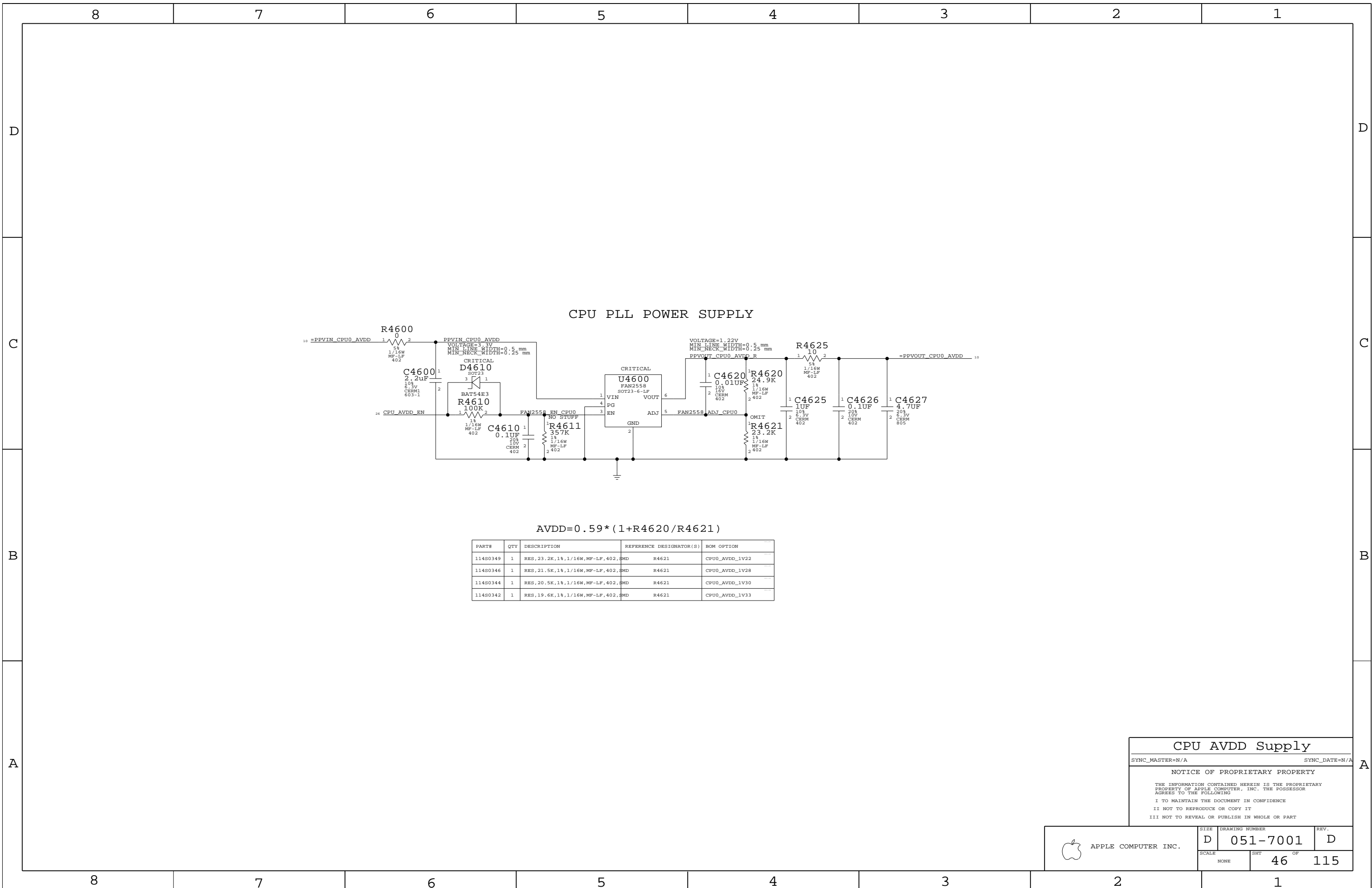
TP_CPU0_SENSEVDD1
 TP_CPU0_SENSEVDD2
 (Kelvin sense points)



A8 Power (CPU0)
 SYNC_MASTER=MULLET SYNC_DATE=08/02/2005

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	D	051-7001	D
SCALE	NONE	SHT OF	38 OF 115



$$AVDD = 0.59 * (1 + R4620 / R4621)$$

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11480349	1	RES, 23.2K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V22
11480346	1	RES, 21.5K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V28
11480344	1	RES, 20.5K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V30
11480342	1	RES, 19.6K, 1%, 1/16W, MF-LF, 402, SMD	R4621	CPU0_AVDD_1V33

CPU AVDD Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT OF		
NONE	46 OF		115

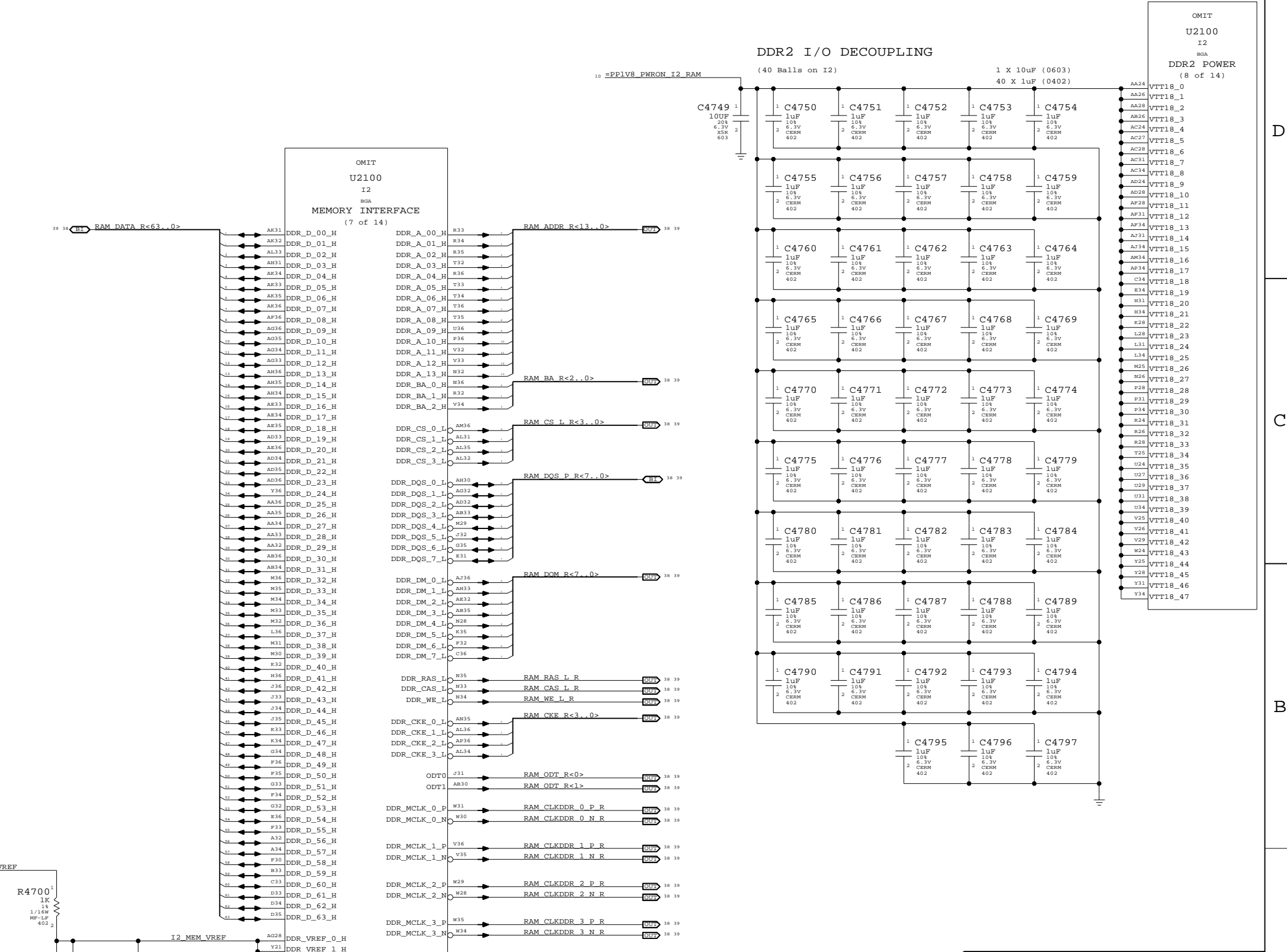
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	NET_TYPE	
				RAM_CLK_0	RAM_CLKDDR_0_P_R 38 39
				RAM_CLK_0	RAM_CLKDDR_0_N_R 38 39
				RAM_CLK_1	RAM_CLKDDR_1_P_R 38 39
				RAM_CLK_1	RAM_CLKDDR_1_N_R 38 39
				RAM_CLK_2	RAM_CLKDDR_2_P_R 38 39
				RAM_CLK_2	RAM_CLKDDR_2_N_R 38 39
				RAM_CLK_3	RAM_CLKDDR_3_P_R 38 39
				RAM_CLK_3	RAM_CLKDDR_3_N_R 38 39
				RAM_CKE_0	RAM_CKE_R<1..0> 38 39
				RAM_CKE_1	RAM_CKE_R<3..2> 38 39
				RAM_CS_0	RAM_CS_L_R<1..0> 38 39
				RAM_CS_1	RAM_CS_L_R<3..2> 38 39
				RAM_ADDR_CTTI	RAM_ADDR_R<13..0> 38 39
				RAM_ADDR_CTTI	RAM_BA_R<2..0> 38 39
				RAM_ADDR_CTTI	RAM_RAS_L_R 38 39
				RAM_ADDR_CTTI	RAM_CAS_L_R 38 39
				RAM_ADDR_CTTI	RAM_WE_L_R 38 39
				RAM_ODT0	RAM_ODT_R<0> 38 39
				RAM_ODT1	RAM_ODT_R<1> 38 39
				RAM_DQS0	RAM_DQS_P_R<0> 38 39
				RAM_DQS1	RAM_DQS_P_R<1> 38 39
				RAM_DQS2	RAM_DQS_P_R<2> 38 39
				RAM_DQS3	RAM_DQS_P_R<3> 38 39
				RAM_DQS4	RAM_DQS_P_R<4> 38 39
				RAM_DQS5	RAM_DQS_P_R<5> 38 39
				RAM_DQS6	RAM_DQS_P_R<6> 38 39
				RAM_DQS7	RAM_DQS_P_R<7> 38 39
				RAM_DQM0	RAM_DQM_R<0> 38 39
				RAM_DQM1	RAM_DQM_R<1> 38 39
				RAM_DQM2	RAM_DQM_R<2> 38 39
				RAM_DQM3	RAM_DQM_R<3> 38 39
				RAM_DQM4	RAM_DQM_R<4> 38 39
				RAM_DQM5	RAM_DQM_R<5> 38 39
				RAM_DQM6	RAM_DQM_R<6> 38 39
				RAM_DQM7	RAM_DQM_R<7> 38 39
				RAM_DATA_0	RAM_DATA_R<7..0> 38 39
				RAM_DATA_1	RAM_DATA_R<15..8> 38 39
				RAM_DATA_2	RAM_DATA_R<23..16> 38 39
				RAM_DATA_3	RAM_DATA_R<31..24> 38 39
				RAM_DATA_4	RAM_DATA_R<39..32> 38 39
				RAM_DATA_5	RAM_DATA_R<47..40> 38 39
				RAM_DATA_6	RAM_DATA_R<55..48> 38 39
				RAM_DATA_7	RAM_DATA_R<63..56> 38 39

Page Notes

Power aliases required by this page:
 - =PP1V8_PWRON_I2_RAM
 - =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



I2 Memory Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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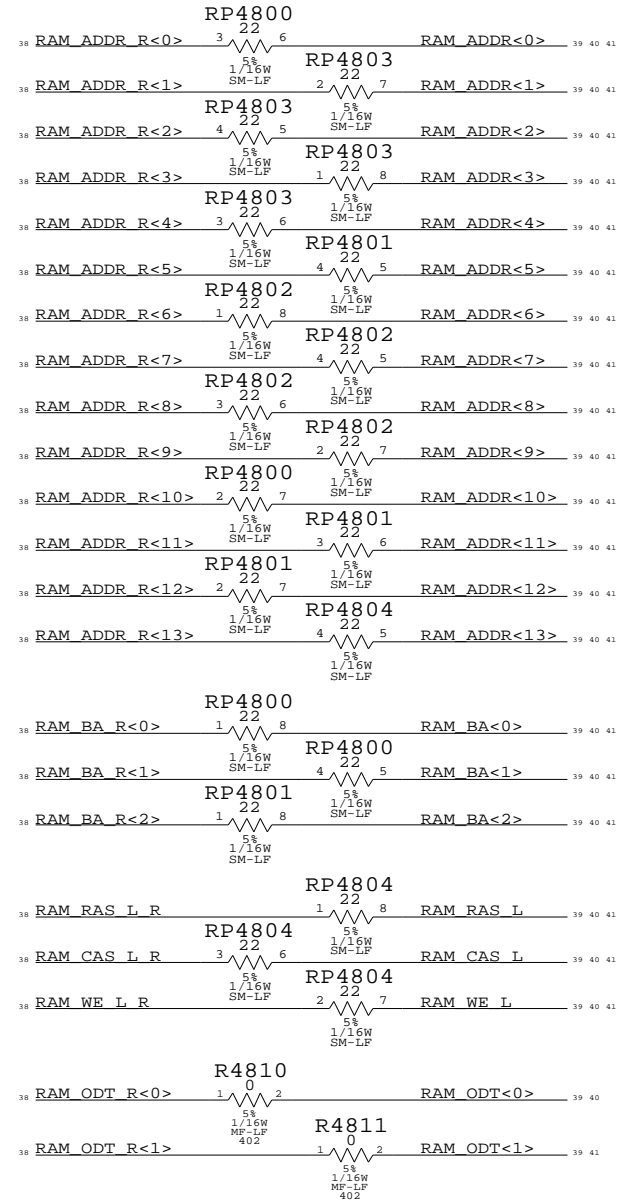
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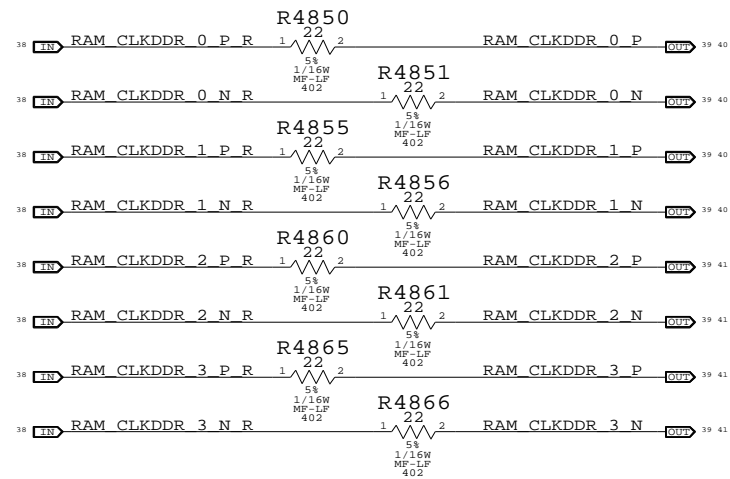
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

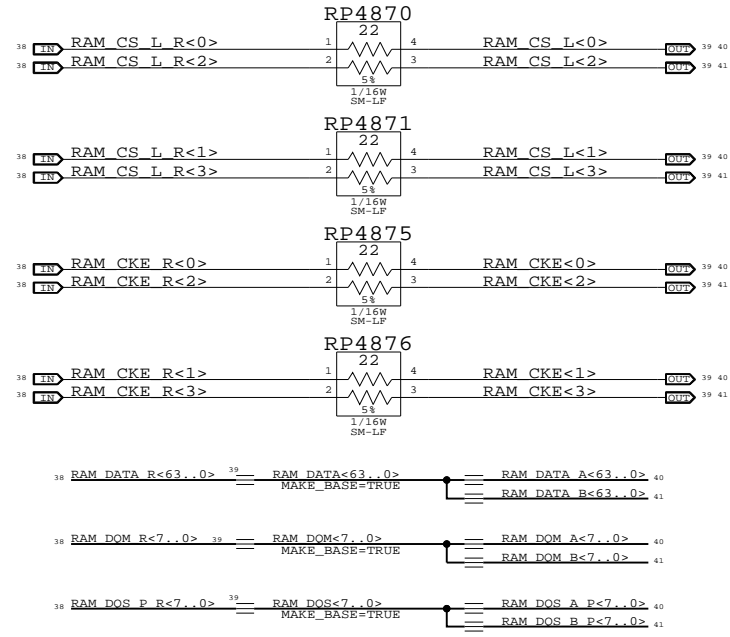


SERIES RESISTORS FOR CLOCKS



SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKs



ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR 0 P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR 0 N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR 1 P 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR 1 N 39 40
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR 2 P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR 2 N 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR 3 P 39 41
DIFF	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR 3 N 39 41
DIFF	RAM	RAM	RAM_CKE<3..0>	39 40 41
DIFF	RAM	RAM	RAM_CS L<3..0>	39 40 41
DIFF	RAM	RAM	RAM_ADDR<13..0>	39 40 41
DIFF	RAM	RAM	RAM_BA<2..0>	39 40 41
DIFF	RAM	RAM	RAM_RAS L	39 40 41
DIFF	RAM	RAM	RAM_CAS L	39 40 41
DIFF	RAM	RAM	RAM_WE L	39 40 41
DIFF	RAM	RAM	RAM_ODT<1..0>	39 40 41
DIFF	RAM	RAM	RAM_DOS<7..0>	39
DIFF	RAM	RAM	RAM_DOM<7..0>	39
DIFF	RAM	RAM	RAM_DATA<63..0>	39

ECSETS provided by memory controller.

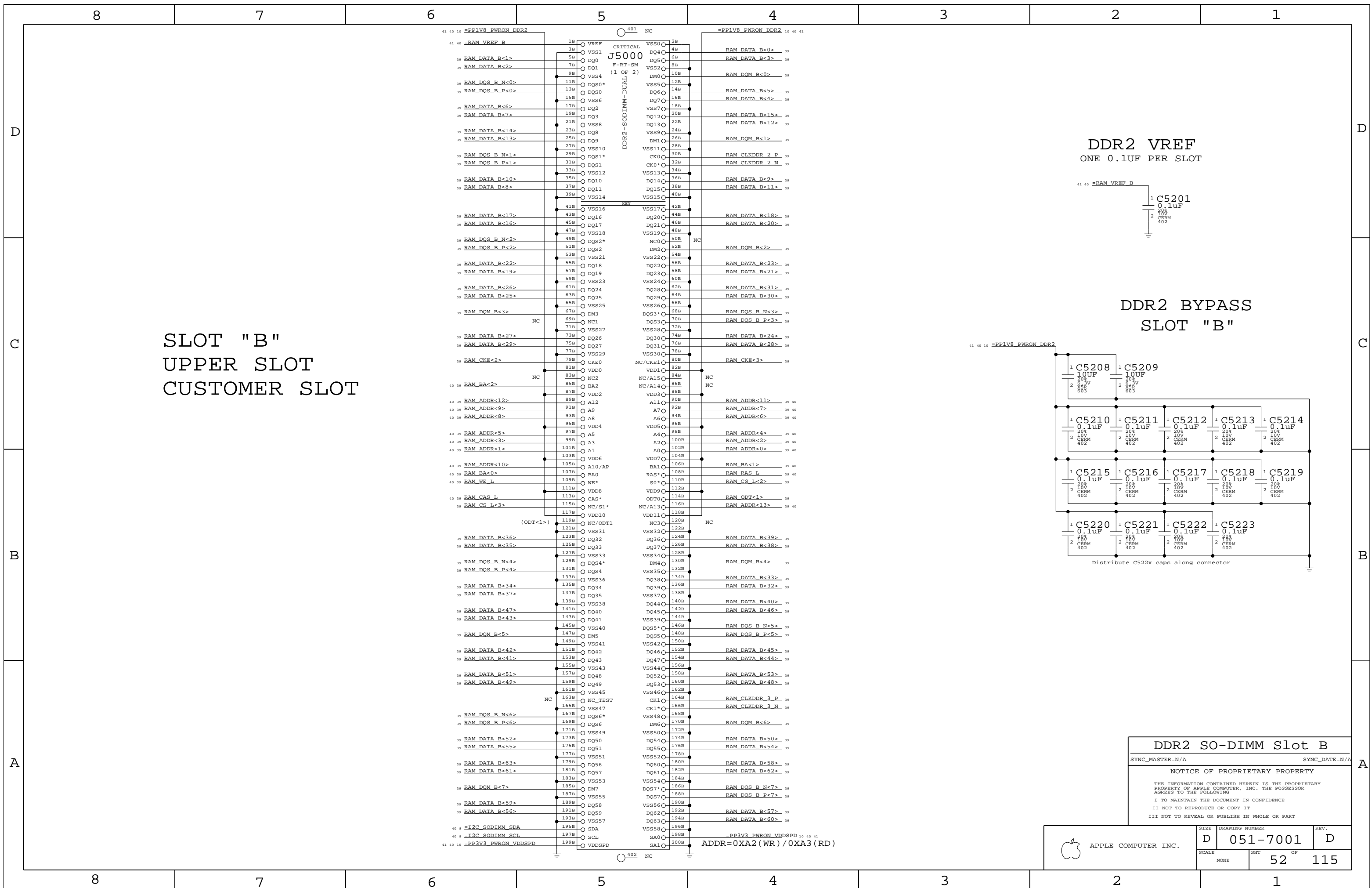
Memory Series Termination

SYNC_MASTER=N/A SYNC_DATE=N/A

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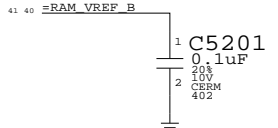
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SCALE	NONE	SHT	OF
		48	115

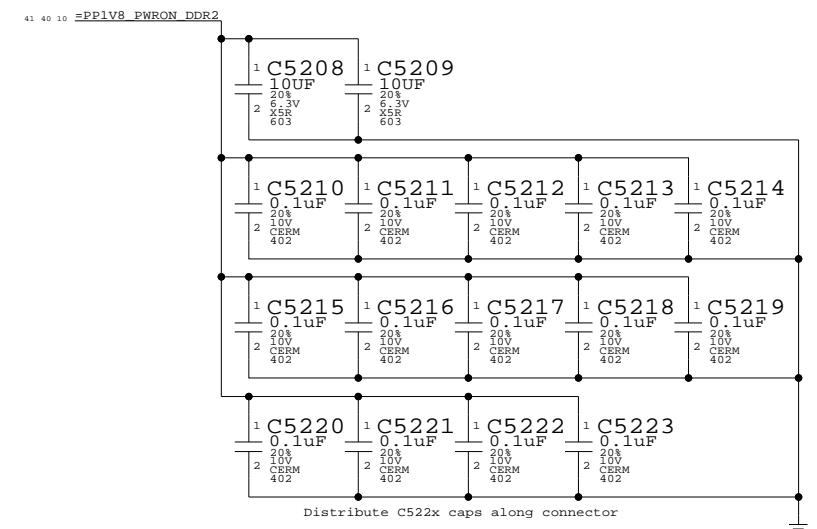


SLOT "B"
UPPER SLOT
CUSTOMER SLOT

DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "B"



Distribute C522x caps along connector

DDR2 SO-DIMM Slot B
 SYNC_MASTER=N/A SYNC_DATE=N/A
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SCALE	NONE	SHT	OF
		52	115

ADDR=0XA2 (WR) / 0XA3 (RD)

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
R100	FB_A_CLK_0	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_0_P_R
R100	(provided above)	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_0_N_R
R100	FB_A_CLK_1	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_1_P_R
R100	(provided above)	SAM_DIFF	SAM_DIFF	FB_A_CLKDDR_1_N_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CKE_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_ADDR_R<12..0>
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_BA_R<2..0>
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_RAS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_CAS_L_R
R100	FB_A_ADDR_CTL	SAM	SAM	FB_A_WE_L_R
R100	FB_A_DQS0	SAM	SAM	FB_A_DQS_R<0>
R100	FB_A_DQS1	SAM	SAM	FB_A_DQS_R<1>
R100	FB_A_DQS2	SAM	SAM	FB_A_DQS_R<2>
R100	FB_A_DQS3	SAM	SAM	FB_A_DQS_R<3>
R100	FB_A_DQS4	SAM	SAM	FB_A_DQS_R<4>
R100	FB_A_DQS5	SAM	SAM	FB_A_DQS_R<5>
R100	FB_A_DQS6	SAM	SAM	FB_A_DQS_R<6>
R100	FB_A_DQS7	SAM	SAM	FB_A_DQS_R<7>
R100	FB_A_DQM0	SAM	SAM	FB_A_DQM_R<0>
R100	FB_A_DQM1	SAM	SAM	FB_A_DQM_R<1>
R100	FB_A_DQM2	SAM	SAM	FB_A_DQM_R<2>
R100	FB_A_DQM3	SAM	SAM	FB_A_DQM_R<3>
R100	FB_A_DQM4	SAM	SAM	FB_A_DQM_R<4>
R100	FB_A_DQM5	SAM	SAM	FB_A_DQM_R<5>
R100	FB_A_DQM6	SAM	SAM	FB_A_DQM_R<6>
R100	FB_A_DQM7	SAM	SAM	FB_A_DQM_R<7>
R100	FB_A_DO0	SAM	SAM	FB_A_DO_R<7..0>
R100	FB_A_DO1	SAM	SAM	FB_A_DO_R<15..8>
R100	FB_A_DO2	SAM	SAM	FB_A_DO_R<23..16>
R100	FB_A_DO3	SAM	SAM	FB_A_DO_R<31..24>
R100	FB_A_DO4	SAM	SAM	FB_A_DO_R<39..32>
R100	FB_A_DO5	SAM	SAM	FB_A_DO_R<47..40>
R100	FB_A_DO6	SAM	SAM	FB_A_DO_R<55..48>
R100	FB_A_DO7	SAM	SAM	FB_A_DO_R<63..56>

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
R110	FB_B_CLK_0	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_0_P_R
R110	(provided above)	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_0_N_R
R110	FB_B_CLK_1	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_1_P_R
R110	(provided above)	SAM_DIFF	SAM_DIFF	FB_B_CLKDDR_1_N_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CKE_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_ADDR_R<12..0>
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_BA_R<2..0>
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_RAS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_CAS_L_R
R110	FB_B_ADDR_CTL	SAM	SAM	FB_B_WE_L_R
R110	FB_B_DQS0	SAM	SAM	FB_B_DQS_R<0>
R110	FB_B_DQS1	SAM	SAM	FB_B_DQS_R<1>
R110	FB_B_DQS2	SAM	SAM	FB_B_DQS_R<2>
R110	FB_B_DQS3	SAM	SAM	FB_B_DQS_R<3>
R110	FB_B_DQS4	SAM	SAM	FB_B_DQS_R<4>
R110	FB_B_DQS5	SAM	SAM	FB_B_DQS_R<5>
R110	FB_B_DQS6	SAM	SAM	FB_B_DQS_R<6>
R110	FB_B_DQS7	SAM	SAM	FB_B_DQS_R<7>
R110	FB_B_DQM0	SAM	SAM	FB_B_DQM_R<0>
R110	FB_B_DQM1	SAM	SAM	FB_B_DQM_R<1>
R110	FB_B_DQM2	SAM	SAM	FB_B_DQM_R<2>
R110	FB_B_DQM3	SAM	SAM	FB_B_DQM_R<3>
R110	FB_B_DQM4	SAM	SAM	FB_B_DQM_R<4>
R110	FB_B_DQM5	SAM	SAM	FB_B_DQM_R<5>
R110	FB_B_DQM6	SAM	SAM	FB_B_DQM_R<6>
R110	FB_B_DQM7	SAM	SAM	FB_B_DQM_R<7>
R110	FB_B_DO0	SAM	SAM	FB_B_DO_R<7..0>
R110	FB_B_DO1	SAM	SAM	FB_B_DO_R<15..8>
R110	FB_B_DO2	SAM	SAM	FB_B_DO_R<23..16>
R110	FB_B_DO3	SAM	SAM	FB_B_DO_R<31..24>
R110	FB_B_DO4	SAM	SAM	FB_B_DO_R<39..32>
R110	FB_B_DO5	SAM	SAM	FB_B_DO_R<47..40>
R110	FB_B_DO6	SAM	SAM	FB_B_DO_R<55..48>
R110	FB_B_DO7	SAM	SAM	FB_B_DO_R<63..56>

M11 Frame Buffer Constraints

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-7001	D
SCALE	SHT	OF
NONE	55	115

8

7

6

5

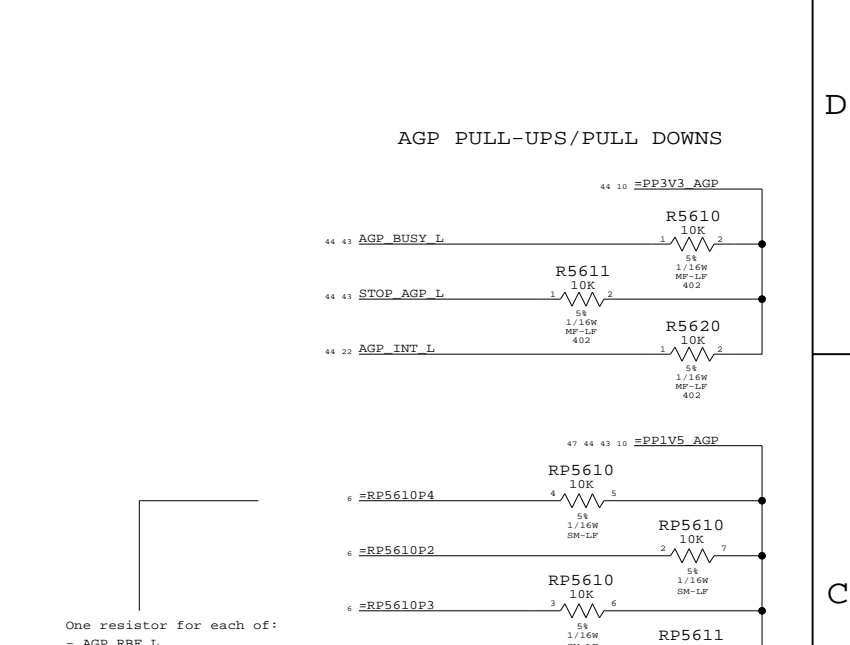
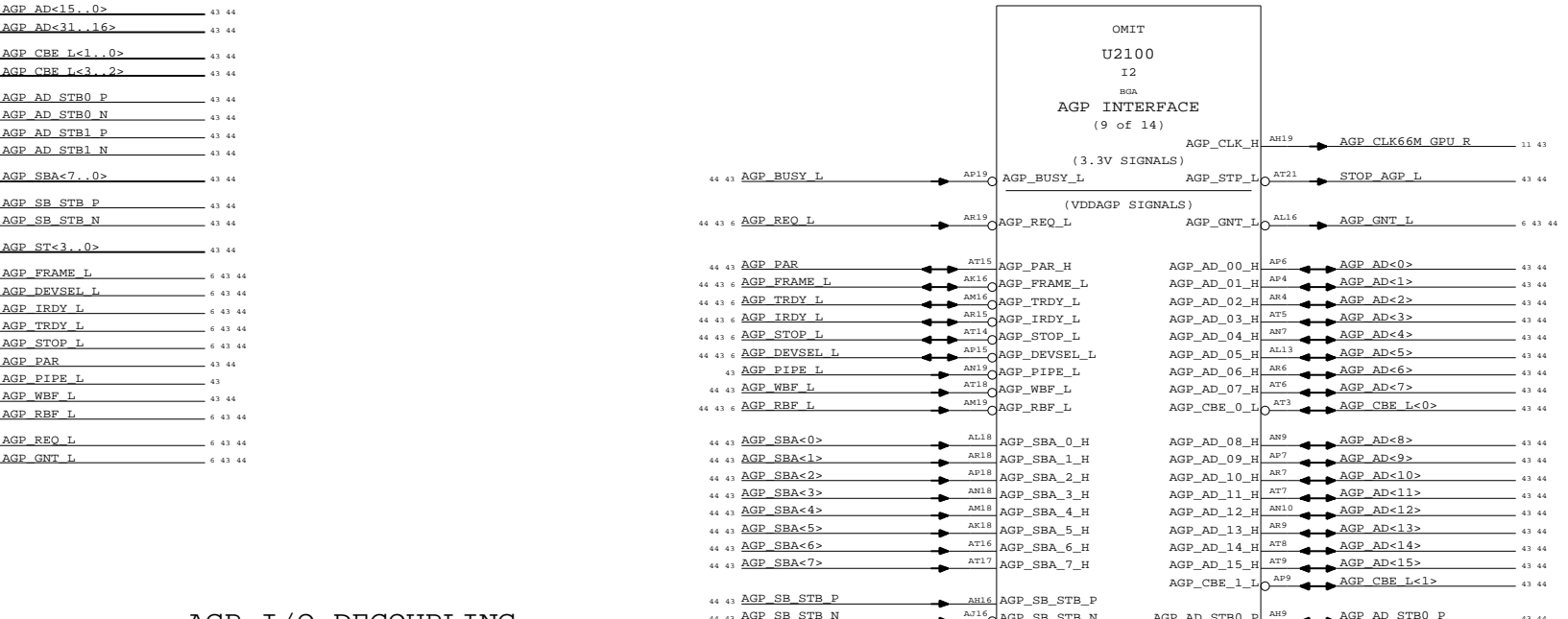
4

3

2

1

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
AGP_CLK	CLOCK	CLOCK	
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK	
AGP_AD_0	AGP	AGP	
AGP_AD_1	AGP	AGP	
AGP_AD_2	AGP	AGP	
AGP_AD_3	AGP	AGP	
AGP_AD_4	AGP	AGP	
AGP_AD_5	AGP	AGP	
AGP_AD_6	AGP	AGP	
AGP_AD_7	AGP	AGP	
AGP_AD_8	AGP	AGP	
AGP_AD_9	AGP	AGP	
AGP_AD_10	AGP	AGP	
AGP_AD_11	AGP	AGP	
AGP_AD_12	AGP	AGP	
AGP_AD_13	AGP	AGP	
AGP_AD_14	AGP	AGP	
AGP_AD_15	AGP	AGP	
AGP_AD_16	AGP	AGP	
AGP_AD_17	AGP	AGP	
AGP_AD_18	AGP	AGP	
AGP_AD_19	AGP	AGP	
AGP_AD_20	AGP	AGP	
AGP_AD_21	AGP	AGP	
AGP_AD_22	AGP	AGP	
AGP_AD_23	AGP	AGP	
AGP_AD_24	AGP	AGP	
AGP_AD_25	AGP	AGP	
AGP_AD_26	AGP	AGP	
AGP_AD_27	AGP	AGP	
AGP_AD_28	AGP	AGP	
AGP_AD_29	AGP	AGP	
AGP_AD_30	AGP	AGP	
AGP_AD_31	AGP	AGP	
AGP_CBE_0	AGP	AGP	
AGP_CBE_1	AGP	AGP	
AGP_CBE_2	AGP	AGP	
AGP_CBE_3	AGP	AGP	
AGP_CBE_4	AGP	AGP	
AGP_CBE_5	AGP	AGP	
AGP_CBE_6	AGP	AGP	
AGP_CBE_7	AGP	AGP	
AGP_CBE_8	AGP	AGP	
AGP_CBE_9	AGP	AGP	
AGP_CBE_10	AGP	AGP	
AGP_CBE_11	AGP	AGP	
AGP_CBE_12	AGP	AGP	
AGP_CBE_13	AGP	AGP	
AGP_CBE_14	AGP	AGP	
AGP_CBE_15	AGP	AGP	
AGP_CBE_16	AGP	AGP	
AGP_CBE_17	AGP	AGP	
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AGP_CBE_27	AGP	AGP	
AGP_CBE_28	AGP	AGP	
AGP_CBE_29	AGP	AGP	
AGP_CBE_30	AGP	AGP	
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AGP_CBE_32	AGP	AGP	
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AGP_CBE_34	AGP	AGP	
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AGP_CBE_36	AGP	AGP	
AGP_CBE_37	AGP	AGP	
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AGP_CBE_39	AGP	AGP	
AGP_CBE_40	AGP	AGP	
AGP_CBE_41	AGP	AGP	
AGP_CBE_42	AGP	AGP	
AGP_CBE_43	AGP	AGP	
AGP_CBE_44	AGP	AGP	
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AGP_CBE_46	AGP	AGP	
AGP_CBE_47	AGP	AGP	
AGP_CBE_48	AGP	AGP	
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AGP_CBE_73	AGP	AGP	
AGP_CBE_74	AGP	AGP	
AGP_CBE_75	AGP	AGP	
AGP_CBE_76	AGP	AGP	
AGP_CBE_77	AGP	AGP	
AGP_CBE_78	AGP	AGP	
AGP_CBE_79	AGP	AGP	
AGP_CBE_80	AGP	AGP	
AGP_CBE_81	AGP	AGP	
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AGP_CBE_91	AGP	AGP	
AGP_CBE_92	AGP	AGP	
AGP_CBE_93	AGP	AGP	
AGP_CBE_94	AGP	AGP	
AGP_CBE_95	AGP	AGP	
AGP_CBE_96	AGP	AGP	
AGP_CBE_97	AGP	AGP	
AGP_CBE_98	AGP	AGP	
AGP_CBE_99	AGP	AGP	
AGP_CBE_100	AGP	AGP	



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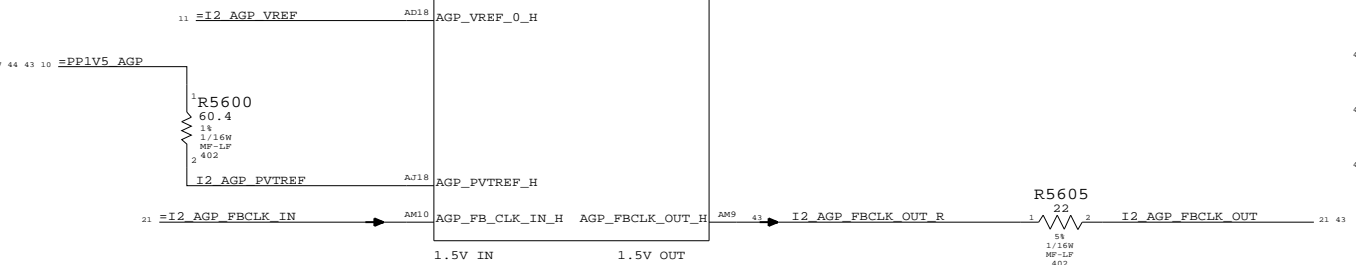
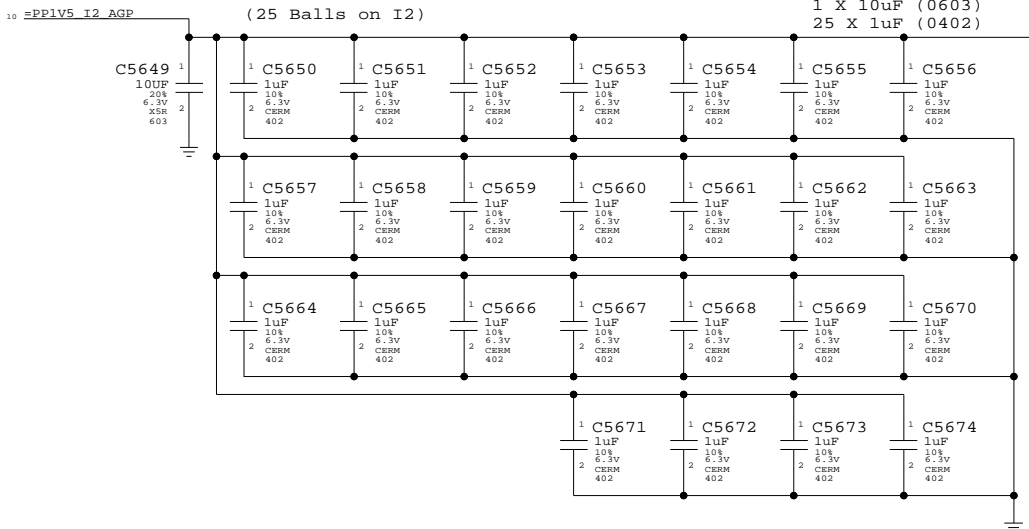
Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP
 - =PP1V5_I2_AGP

Signal aliases required by this page:
 - =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
 - =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:
 (NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

AGP I/O DECOUPLING



I2 AGP Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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	NONE	56	115	D

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
720	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

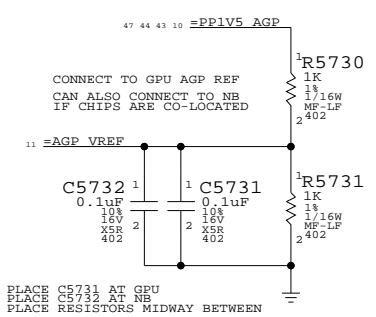
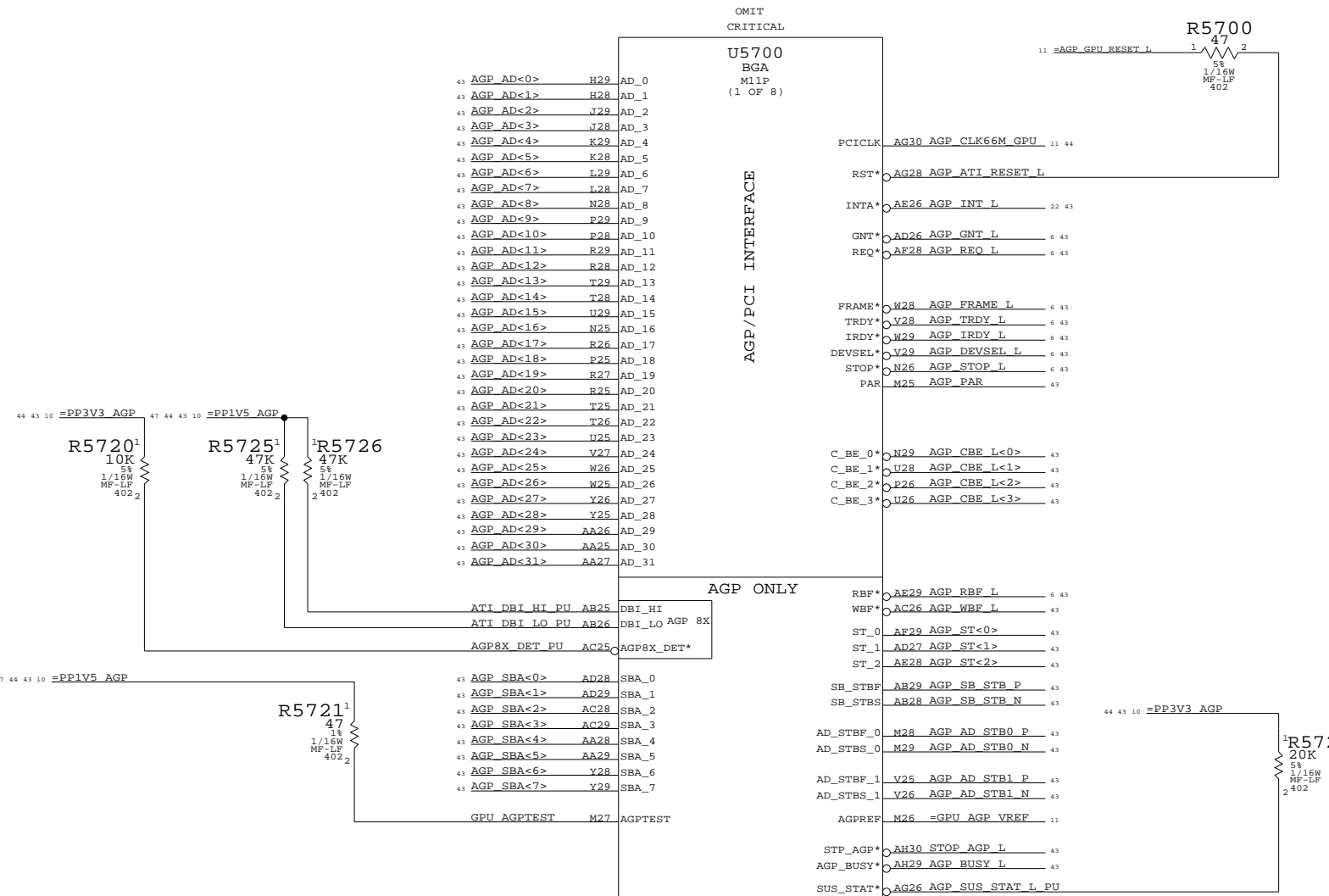
Page Notes

Power aliases required by this page:
 - =PP3V3_AGP
 - =PP1V5_AGP

Signal aliases required by this page:
 - =AGP_VREF - Vref divider output for both GPU and NB
 - =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
 (NONE)

NOTE: AGP 8x signals are not provided by this page.



GPU (M11) AGP Interface

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	D	051-7001	D
SCALE	NONE	SHT OF	57 OF 115

Page Notes

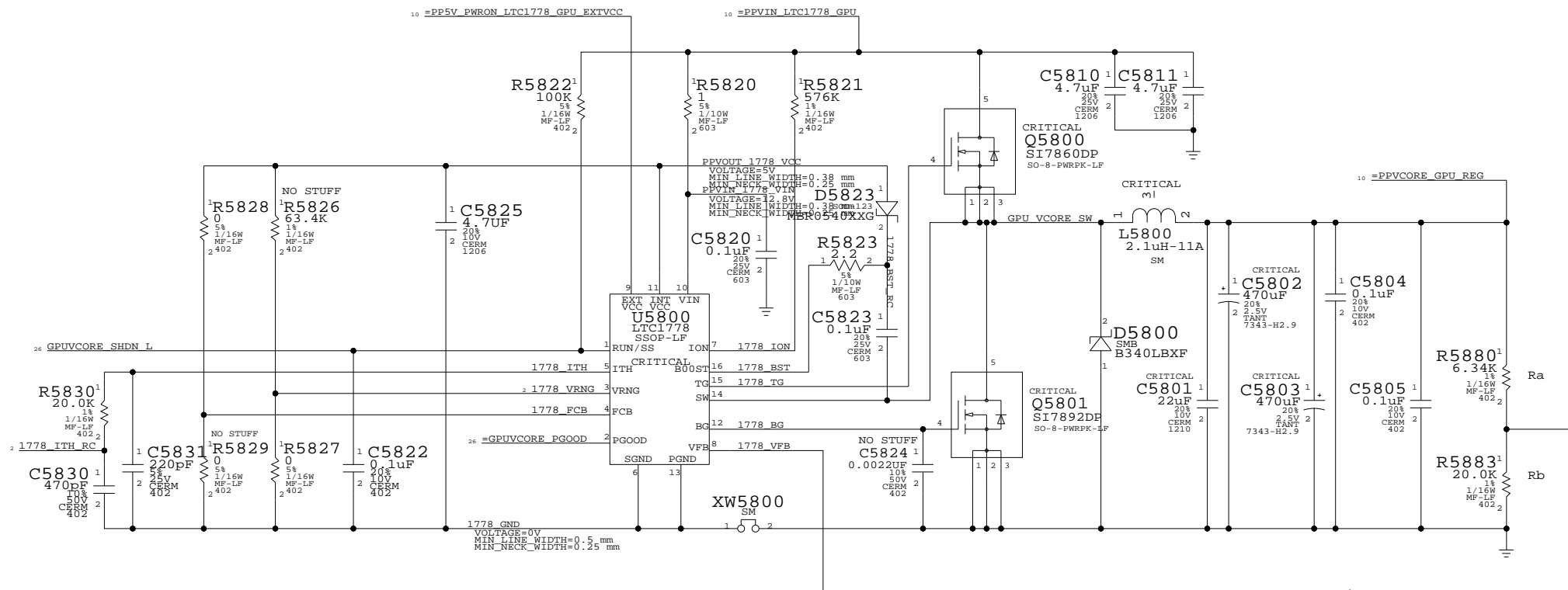
Power aliases required by this page:
 - =PPVIN_LTC1778_GPU
 - =PP5V_PWRON_LTC1778_GPU_EXTVCC
 - =PPVCORE_GPU_REG

Signal aliases required by this page:
 - =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

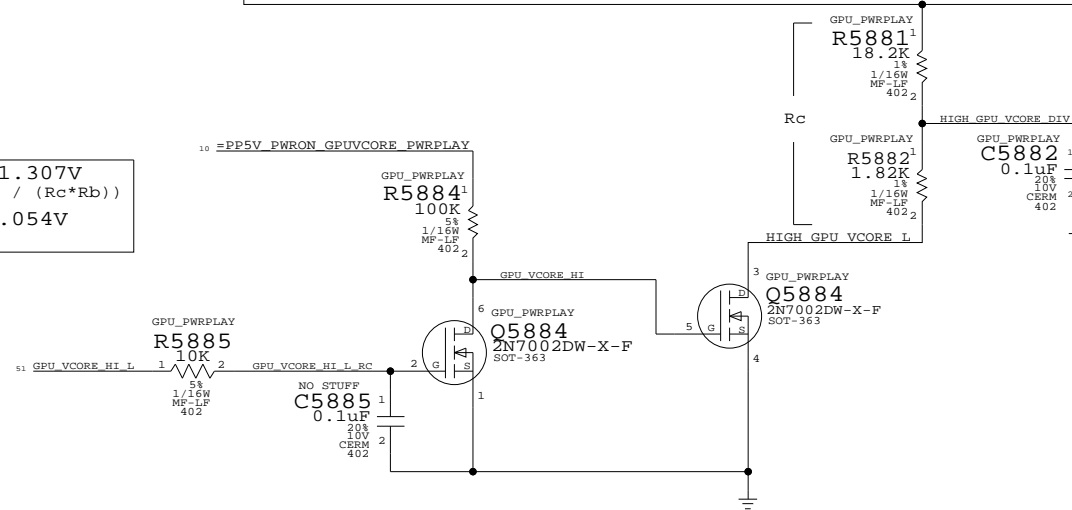
BOM options provided by this page:
 - GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCore SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
 $1.307V = 0.8V * (1 + Ra * (Rc + Rb) / (Rc * Rb))$
 WHEN VCORE_CNTL LOW => 1.054V
 $1.054V = 0.8V * (1 + Ra / Rb)$



GPU VCore Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	NONE	SHT OF	58 OF 115

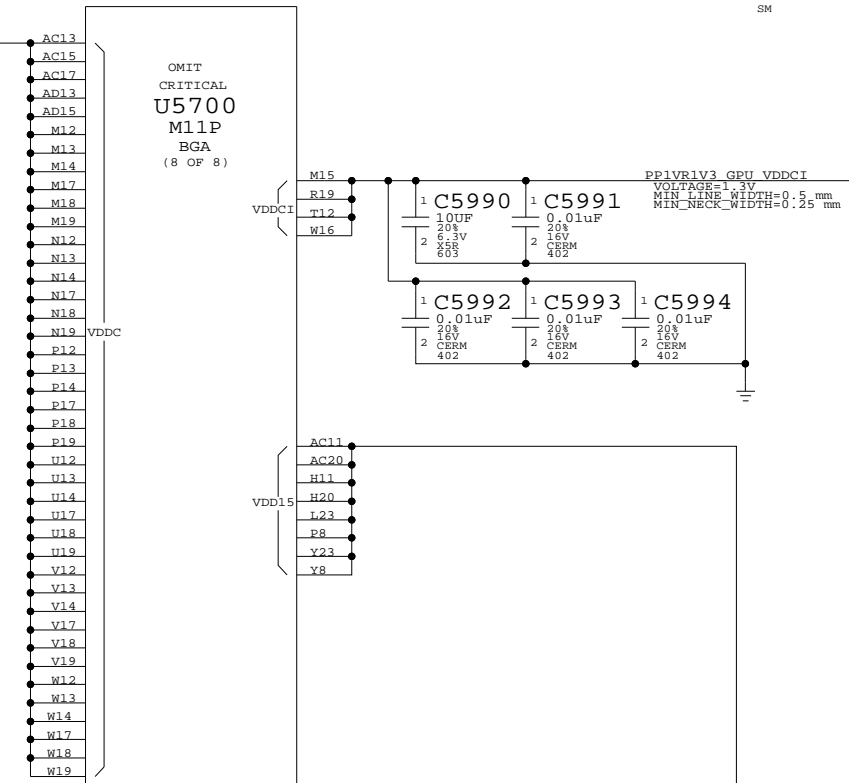
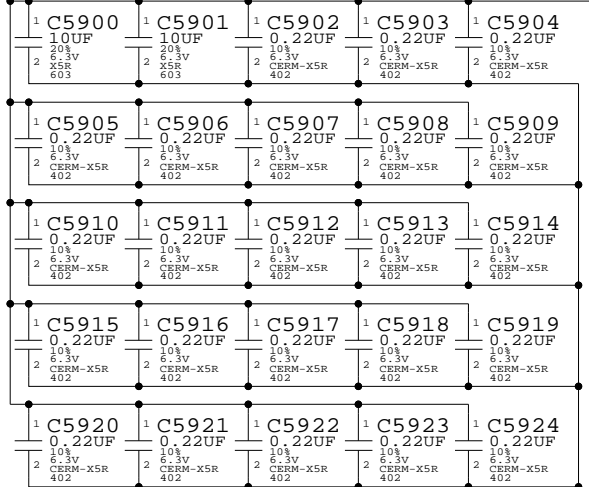
Power aliases required by this page:
 - =PPIV5_GPU_VDD15
 - =PPIV1V3_GPU_VCORE

Signal aliases required by this page:
 (NONE)

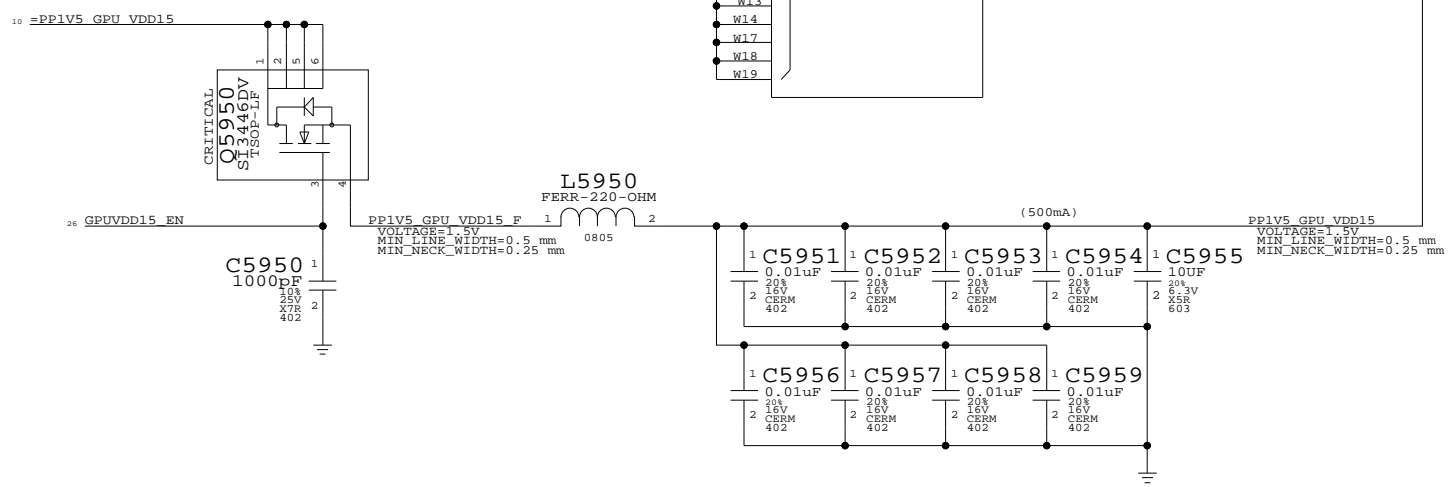
BOM options provided by this page:
 (NONE)

GPU VCORE - 1.3V/1.05V

Internal I/O - 1.3V/1.05V



Internal I/O - 1.5V



OMIT CRITICAL U5700 M11P BGA (6 OF 8)

HOST GROUND

CORE GND

I/O GROUND

GPU (M11) Core Power

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT	OF
		59	115

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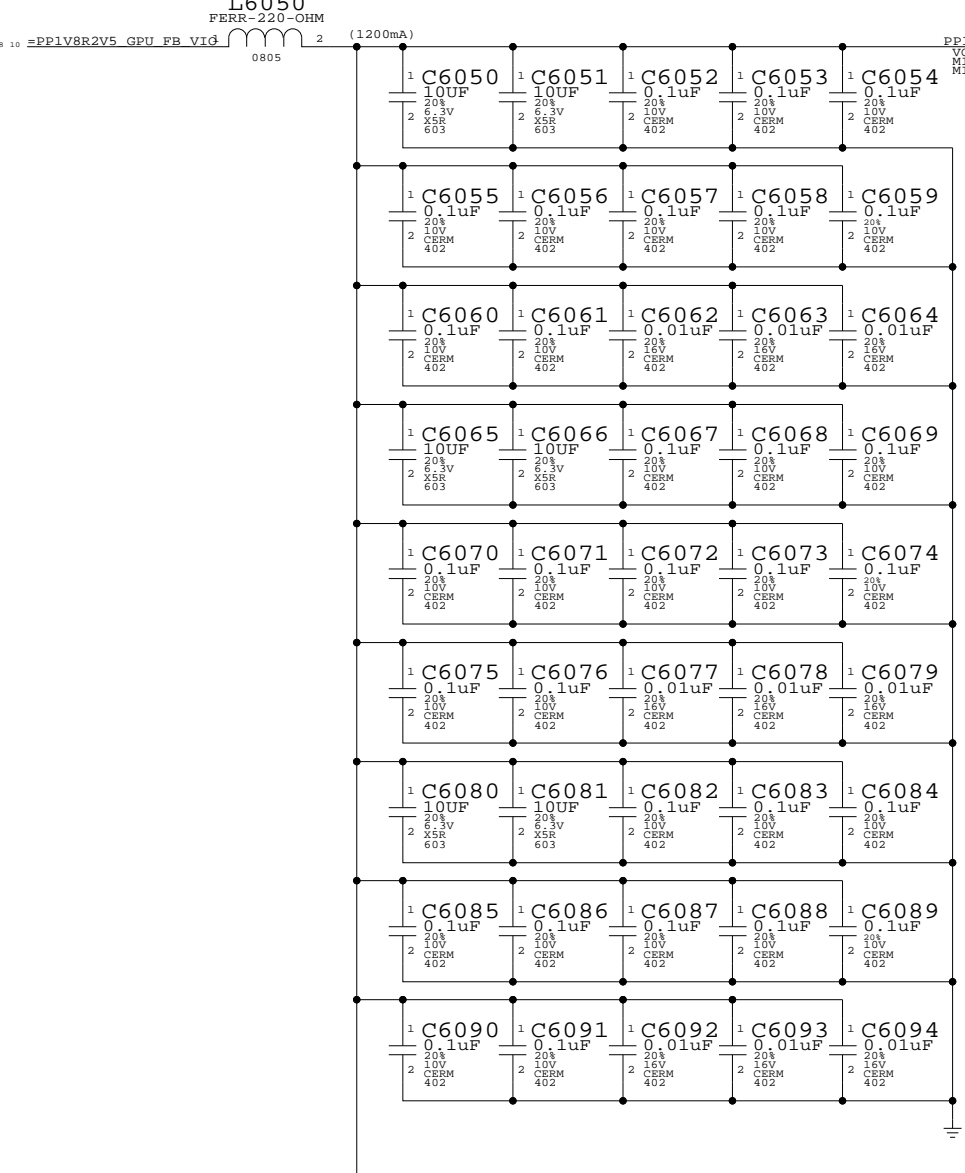
Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO - =PP1V8_GPU_PANEL_IO
 - =PP3V3_GPU_VDDR3 - =PP1V8_GPU_LVDS_PLL
 - =PP1V5_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V8_GPU_DVO - =PP2V5_GPU_LVDS_IO
 - =PP1V5R3V3_DVO_VREF - =PP1V5_AGP

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_LVDDR_2V5
 - DVO_1V8 - GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only

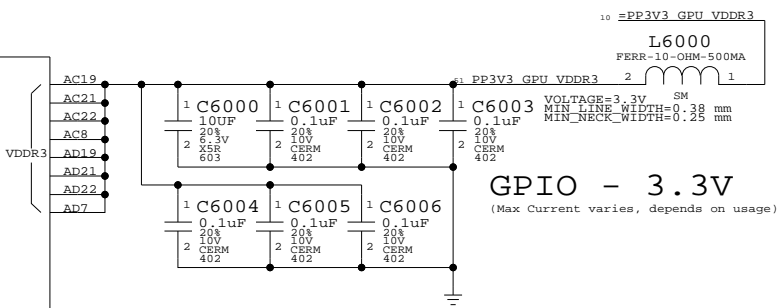
MEMORY I/O - 1.8V/2.5V



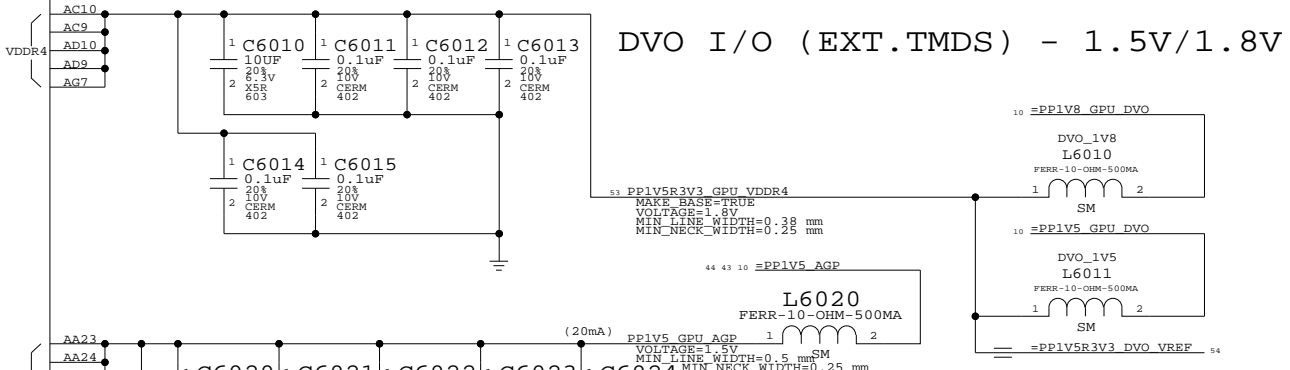
OMIT
 CRITICAL
 U5700
 M11P
 BGA
 (7 OF 8)

- A15
- A21
- A28
- A9
- AA1
- AA4
- AA7
- AA8
- AD4
- B1
- B30
- D11
- D13
- D14
- D17
- D19
- D20
- D23
- D26
- D5
- D8
- E27
- F4
- G10
- G13
- G15
- G19
- G22
- G27
- G7
- H10
- H13
- H15
- H17
- H19
- H22
- J1
- J23
- J24
- J4
- J7
- J8
- L27
- L8
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- R4
- T4
- T7
- T8
- V4
- V7
- V8

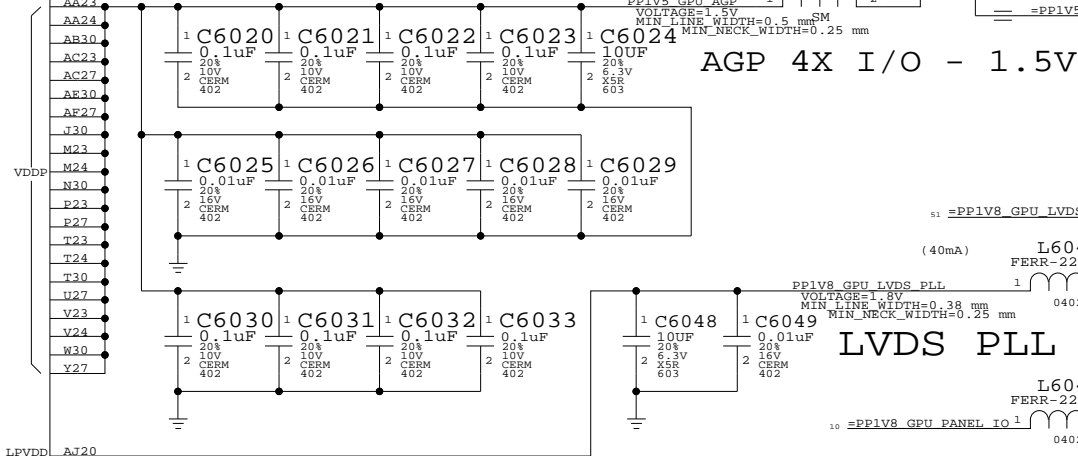
GPIO - 3.3V
 (Max Current varies, depends on usage)



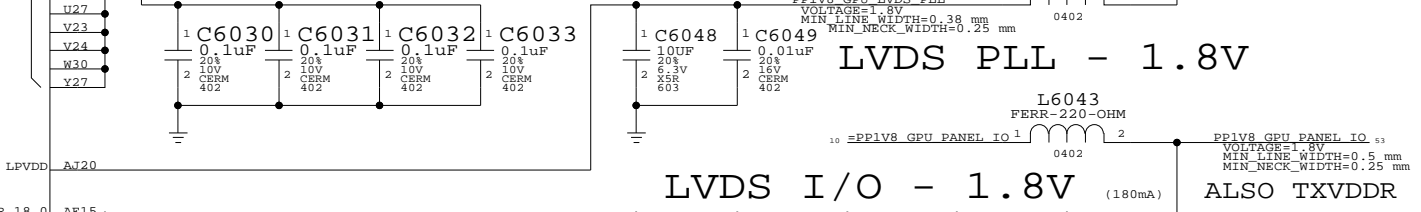
DVO I/O (EXT.TMDS) - 1.5V/1.8V



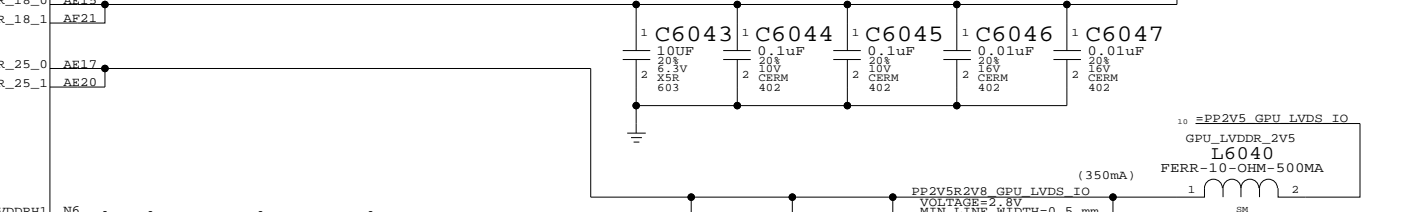
AGP 4X I/O - 1.5V



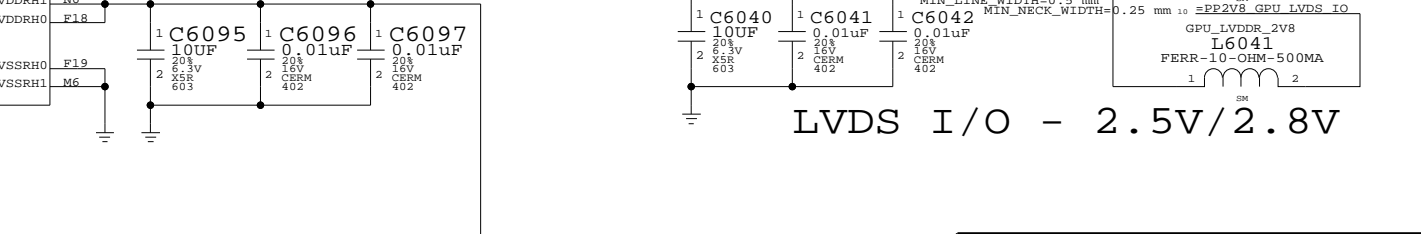
LVDS PLL - 1.8V



LVDS I/O - 1.8V
 (180mA) ALSO TXVDDR



LVDS I/O - 2.5V/2.8V



GPU (M11) I/O Power

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT	OF	
NONE	60	115	

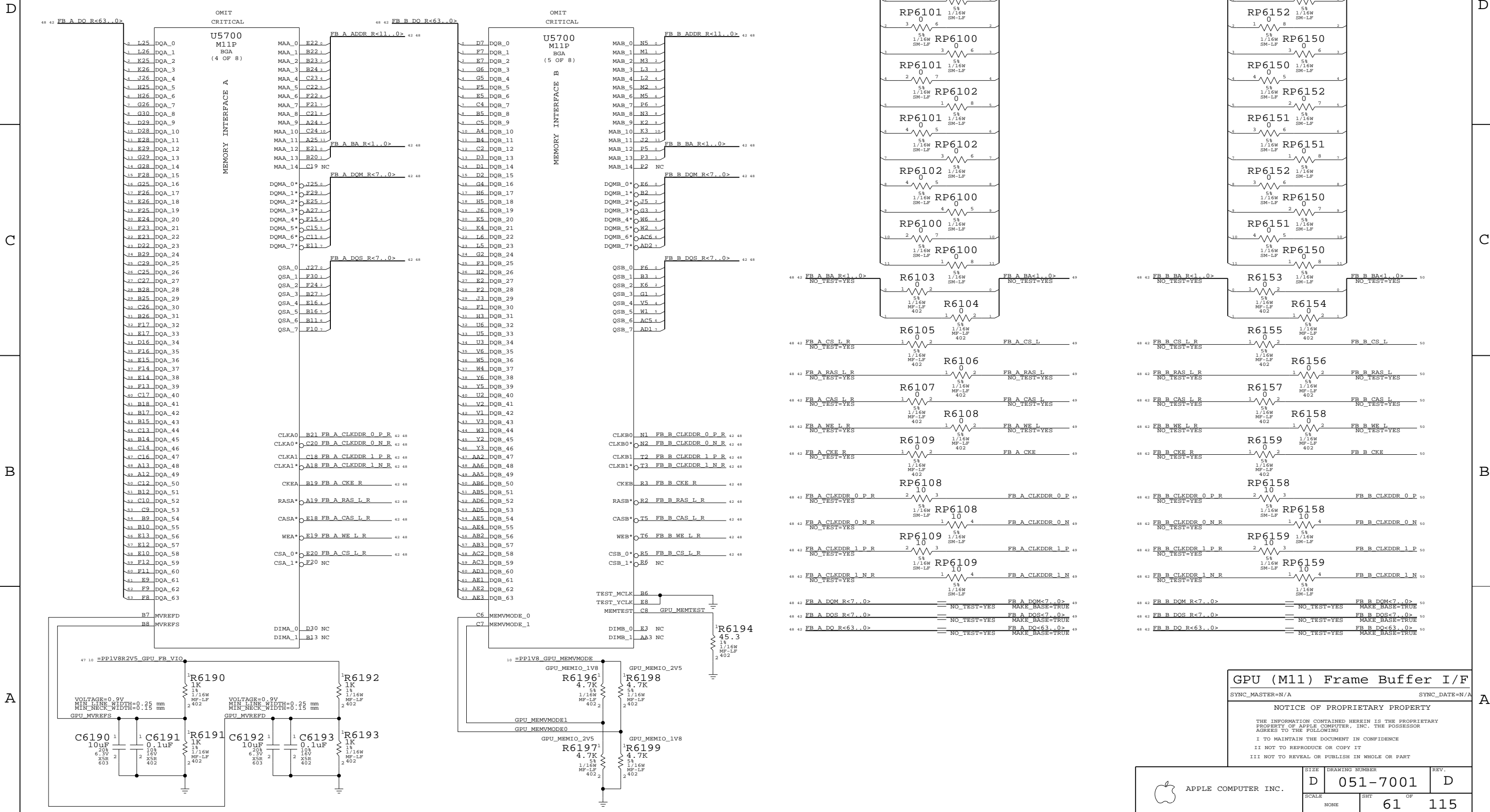
Page Notes

Power aliases required by this page:
 - =PP1V8R2V5_GPU_FB_VIO
 - =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - GPU_MEMIO_1V8
 - GPU_MEMIO_2V5

GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F

SYNC_MASTER=N/A SYNC_DATE=N/A

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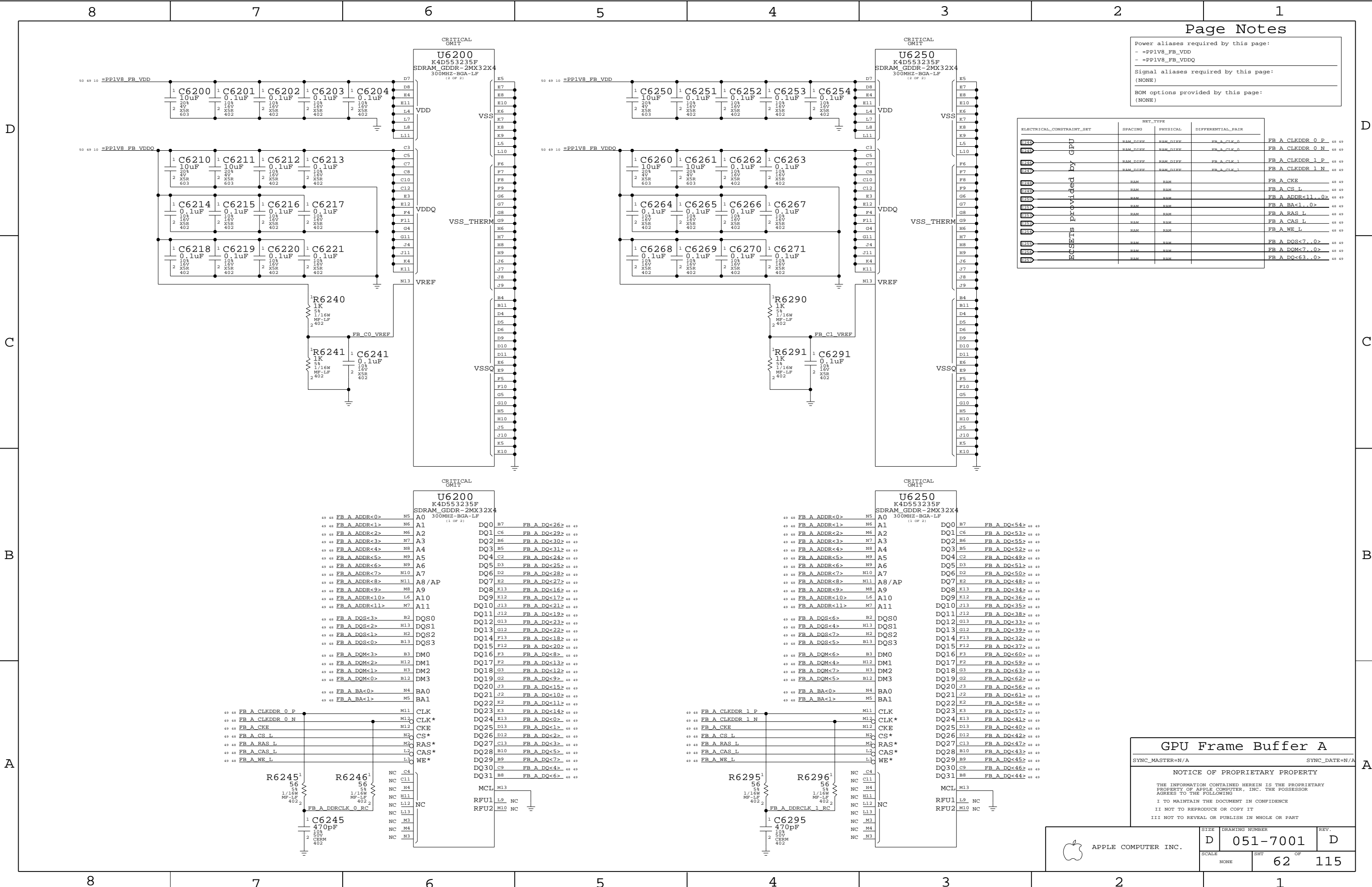
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	SHT	OF	
NONE	61	115	

Power aliases required by this page:
 - =PPIV8_FB_VDD
 - =PPIV8_FB_VDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
FB00	RAM_DIFF	RAM_DIFF	FB_A_CLK_0
FB01	RAM_DIFF	RAM_DIFF	FB_A_CLK_0
FB02	RAM_DIFF	RAM_DIFF	FB_A_CLK_1
FB03	RAM_DIFF	RAM_DIFF	FB_A_CLK_1
FB04	RAM	RAM	FB_A_CKE
FB05	RAM	RAM	FB_A_CS_L
FB06	RAM	RAM	FB_A_ADDR<11..0>
FB07	RAM	RAM	FB_A_BA<1..0>
FB08	RAM	RAM	FB_A_RAS_L
FB09	RAM	RAM	FB_A_CAS_L
FB10	RAM	RAM	FB_A_WE_L
FB11	RAM	RAM	FB_A_DQS<7..0>
FB12	RAM	RAM	FB_A_DQM<7..0>
FB13	RAM	RAM	FB_A_DQ<63..0>



GPU Frame Buffer A

SYNC_MASTER=N/A SYNC_DATE=N/A

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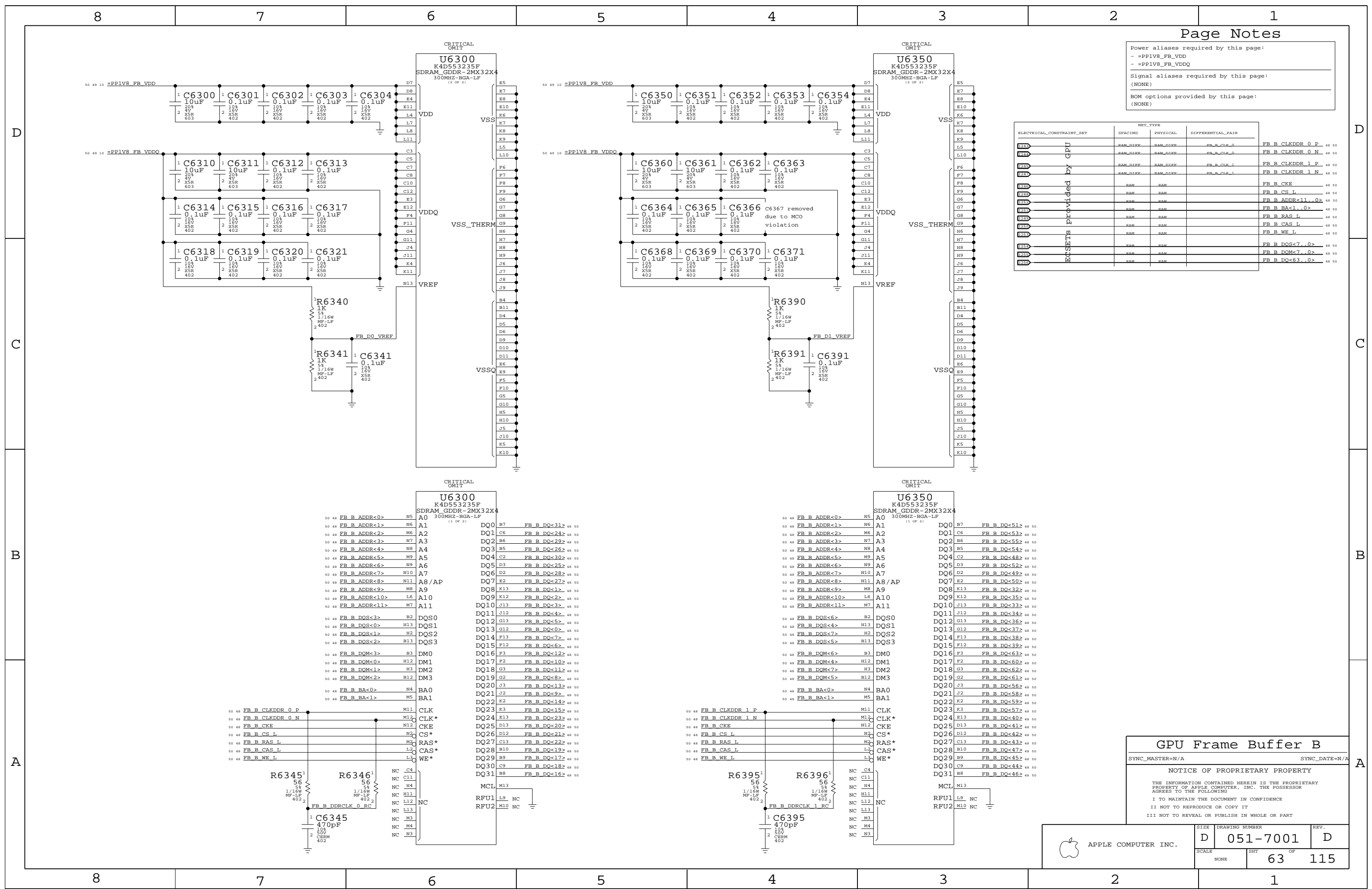
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT	OF
		62	115

Power aliases required by this page:
- =PPIV8_FB_VDD
- =PPIV8_FB_VDDQ
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

Table with columns: ELECTRICAL_CONSTRAINT_SET, SPACING, PHYSICAL, DIFFERENTIAL_PAIR. Lists constraints like FB_B_CLK_0_P, FB_B_CLK_0_N, etc.



GPU Frame Buffer B
SYNC_MASTER=N/A SYNC_DATE=N/A
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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET OF. Values: D, 051-7001, D, NONE, 63 OF 115.



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Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_GPIOS
 - =PP2V5_PVDD
 - =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
 - =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
 - =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
 (NONE)

D

D

C

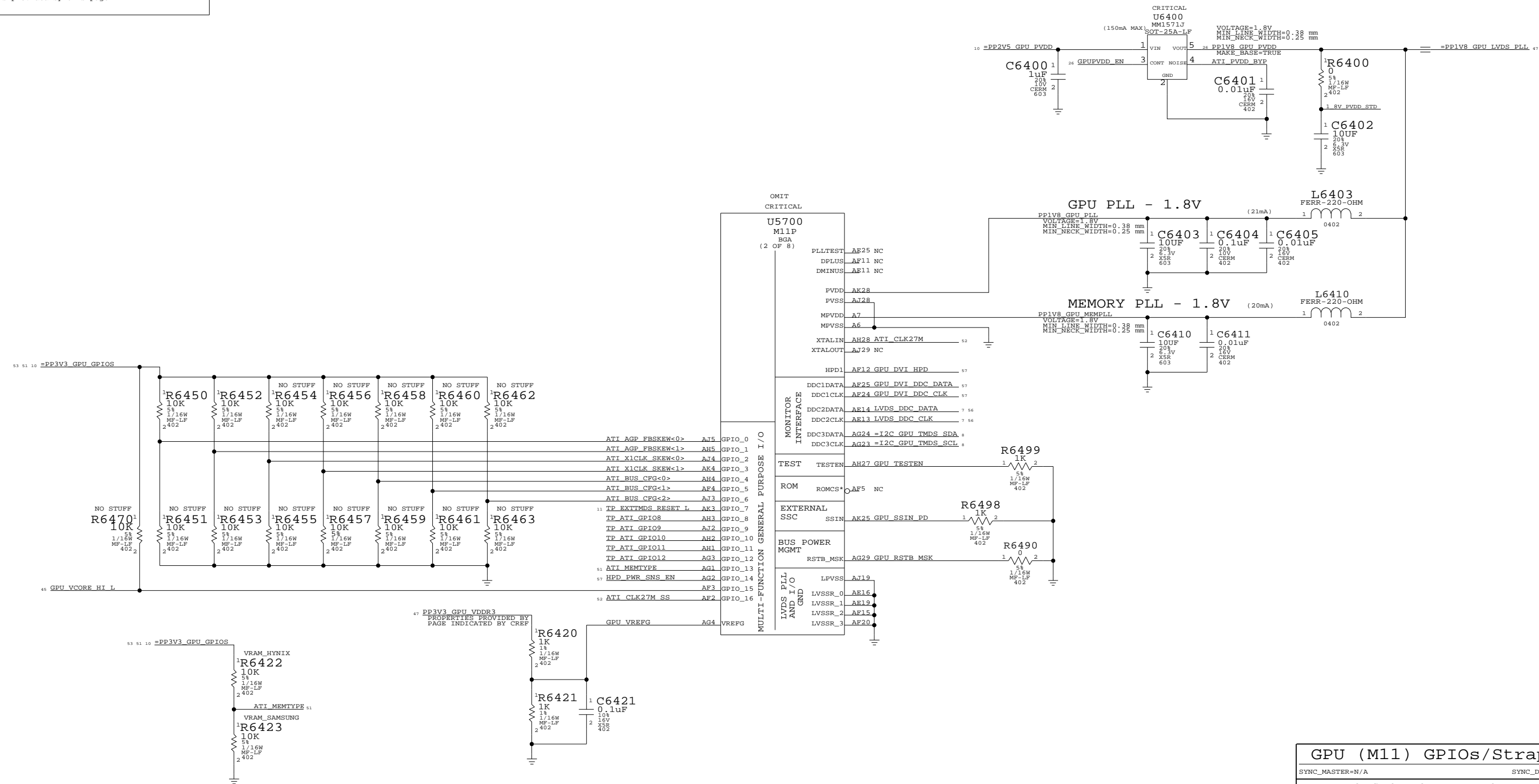
C

B

B

A

A



GPU (M11) GPIOs/Straps

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHEET OF		
NONE	64 OF		115

Page Notes

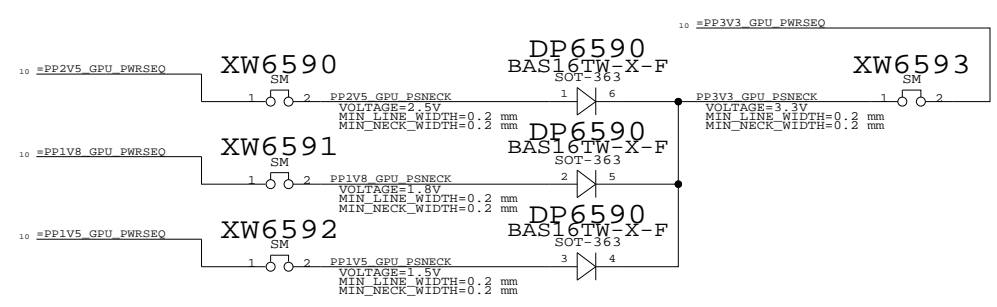
Power aliases required by this page:
 - =PP3V3_GPU_CLOCKS - =PP3V3_GPU_PWRSEQ
 - =PPVIN_GPU_LVDDR_LDO - =PP2V5_GPU_PWRSEQ
 - =PP2V5_GPU_LVDDR_LDO - =PP1V8_GPU_PWRSEQ
 - =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
 (NONE)

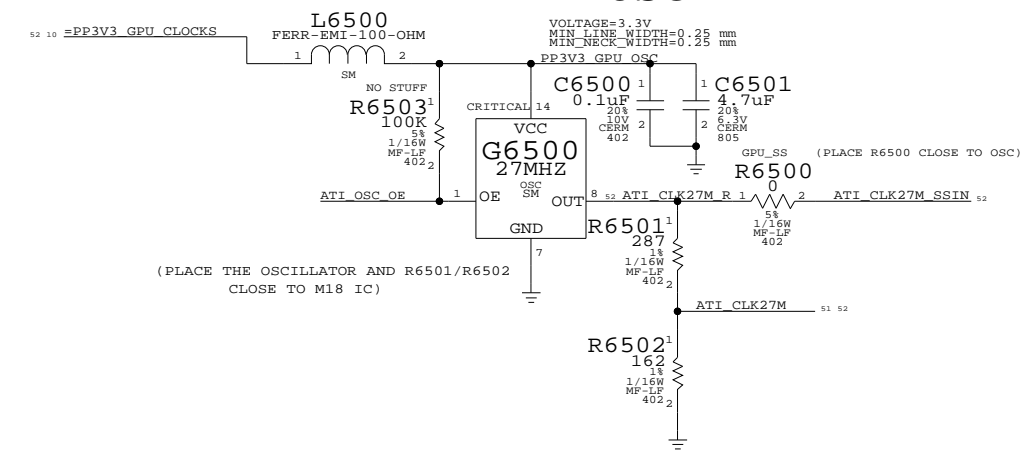
BOM options provided by this page:
 - GPU_SS - GPU_LVDDR_2V8

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R60	ATI_CLK27M	CLOCK	CLOCK
R64	ATI_CLK27M	CLOCK	CLOCK
R65	ATI_CLK27M	CLOCK	CLOCK
R61	ATI_CLK27M_SS	CLOCK	CLOCK
R62	ATI_CLK27M_SS	CLOCK	CLOCK

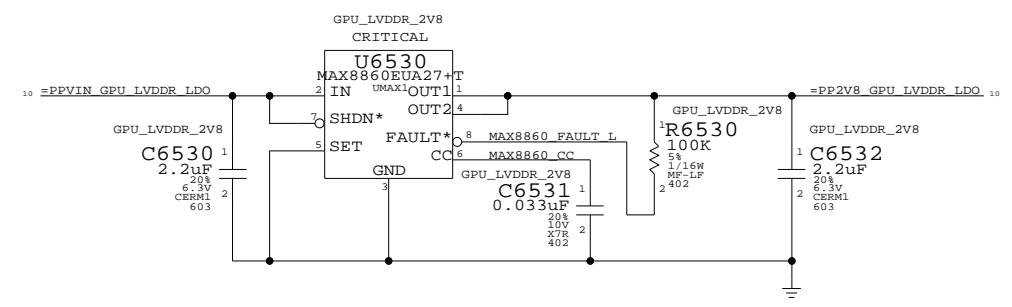
M11 Power Shutdown Sequencing



27M OSC

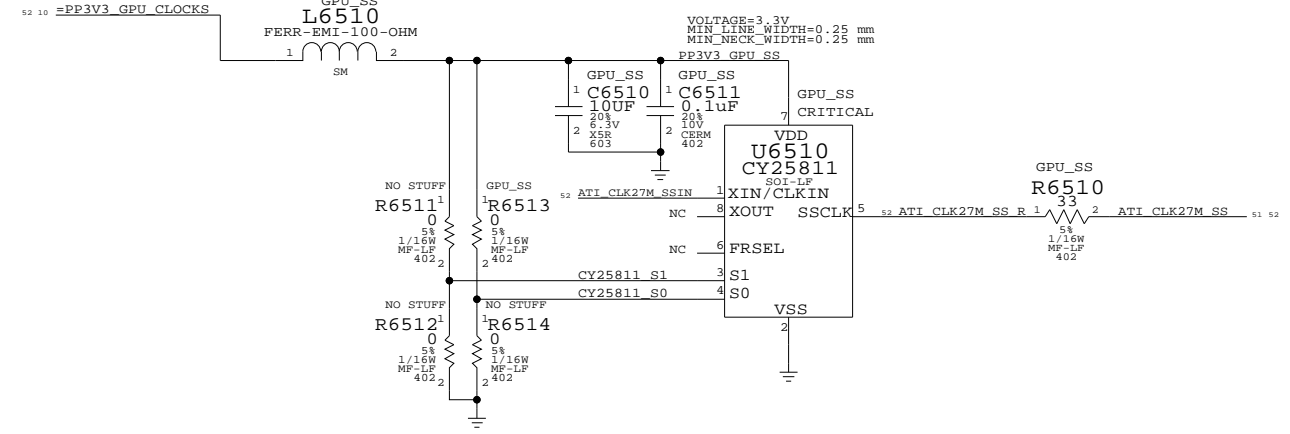


LVDDR 2.8V LDO



PART NUMBER	IS ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1188	353S1140	GPU_LVDDR_2V8	U6530	Primary is 2.7V/Alt is 2.8V

SPREAD SPECTRUM SUPPORT
 S0=1;S1=M => -1.5% DOWN-SPREAD



GPU (M11) Clocks/Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHEET OF		REV.
NONE	65 OF 115		

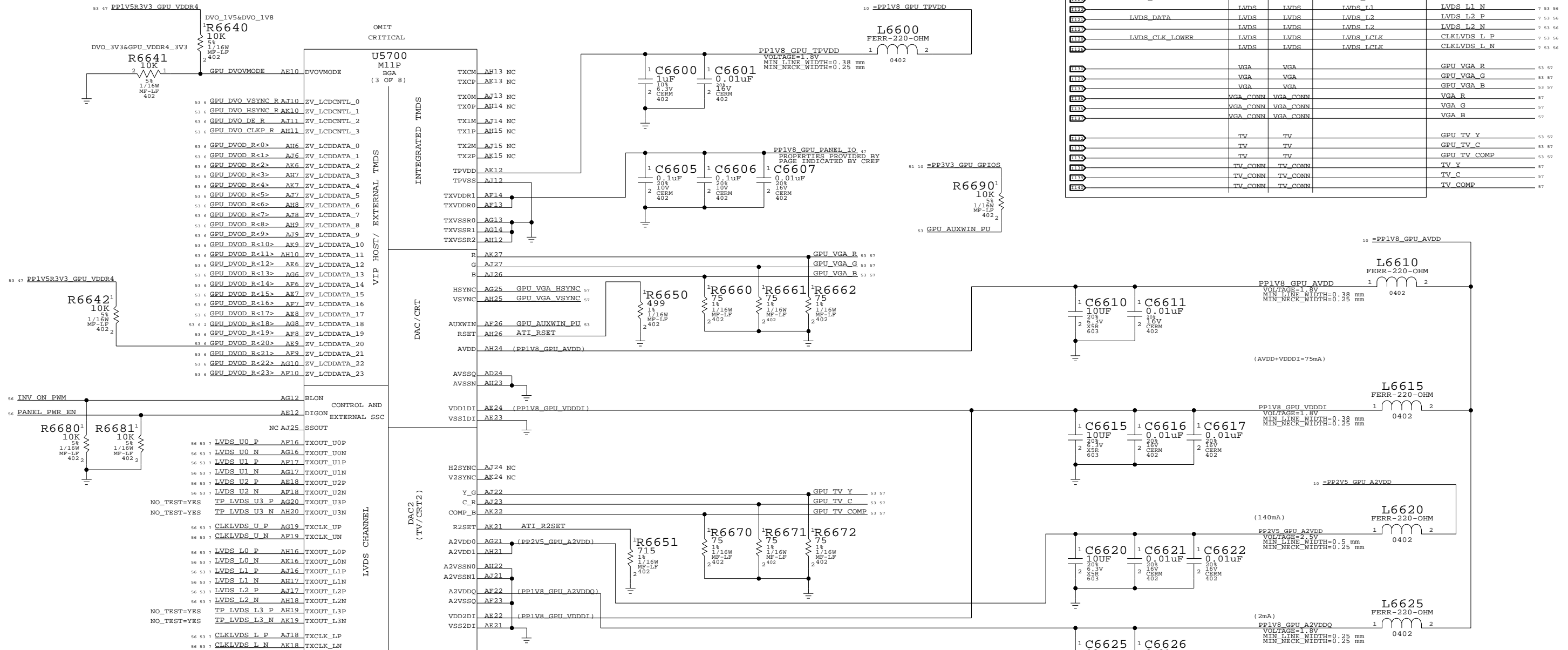
Page Notes

Power aliases required by this page:
 - =PP2V5_GPU_A2VDD - =PP1V8_GPU_AVDD
 - =PP1V8_GPU_TPVDV - =PP3V3_GPU_GPIOS

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - DVO_1V5 - GPU_VDDR4_3V3
 - DVO_1V8 - DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR		
	SPACING	PHYSICAL			
R6600	DVO	DVO	GPU DVOD R<23..0>	2 53 53	
R6601	DVO	DVO	GPU DVO HSYNC R	6 53 53	
R6602	DVO	DVO	GPU DVO VSYNC R	6 53 53	
R6603	DVO	DVO	GPU DVO DE R	6 53 53	
R6604	DVO	DVO	GPU DVO CLKP R	6 53 53	
R6605	LVDS_DATA	LVDS	LVDS_U0	LVDS_U0_P	7 53 56
R6606	LVDS_DATA	LVDS	LVDS_U0	LVDS_U0_N	7 53 56
R6607	LVDS_DATA	LVDS	LVDS_U1	LVDS_U1_P	7 53 56
R6608	LVDS_DATA	LVDS	LVDS_U1	LVDS_U1_N	7 53 56
R6609	LVDS_DATA	LVDS	LVDS_U2	LVDS_U2_P	7 53 56
R6610	LVDS_DATA	LVDS	LVDS_U2	LVDS_U2_N	7 53 56
R6611	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	CLKLVDS_U_P	7 53 56
R6612	LVDS_CLK_UPPER	LVDS	LVDS_UCLK	CLKLVDS_U_N	7 53 56
R6613	LVDS_DATA	LVDS	LVDS_L0	LVDS_L0_P	7 53 56
R6614	LVDS_DATA	LVDS	LVDS_L0	LVDS_L0_N	7 53 56
R6615	LVDS_DATA	LVDS	LVDS_L1	LVDS_L1_P	7 53 56
R6616	LVDS_DATA	LVDS	LVDS_L1	LVDS_L1_N	7 53 56
R6617	LVDS_DATA	LVDS	LVDS_L2	LVDS_L2_P	7 53 56
R6618	LVDS_DATA	LVDS	LVDS_L2	LVDS_L2_N	7 53 56
R6619	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	CLKLVDS_L_P	7 53 56
R6620	LVDS_CLK_LOWER	LVDS	LVDS_LCLK	CLKLVDS_L_N	7 53 56
R6621	VGA	VGA	GPU VGA_R		53 57
R6622	VGA	VGA	GPU VGA_G		53 57
R6623	VGA	VGA	GPU VGA_B		53 57
R6624	VGA_CONN	VGA_CONN	VGA_R		57
R6625	VGA_CONN	VGA_CONN	VGA_G		57
R6626	VGA_CONN	VGA_CONN	VGA_B		57
R6627	TV	TV	GPU TV_Y		53 57
R6628	TV	TV	GPU TV_C		53 57
R6629	TV	TV	GPU TV_COMP		53 57
R6630	TV_CONN	TV_CONN	TV_Y		57
R6631	TV_CONN	TV_CONN	TV_C		57
R6632	TV_CONN	TV_CONN	TV_COMP		57



GPU (M11) DVI/DAC Outputs

SYNC_MASTER=N/A SYNC_DATE=N/A

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	NONE	D 051-7001	D
SCALE		SHT	OF
NONE		66	115



APPLE COMPUTER INC.

Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
 - =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
 - =SI_I2C_CLK
 - =SI_I2C_DATA

BOM options provided by this page:
 - TMDS_EXT - DVO_V15 - DVO_V3V3
 - TMDS_DUAL - DVO_V18

Net Spacing Type: TMDS
 Net Physical Type: TMDS

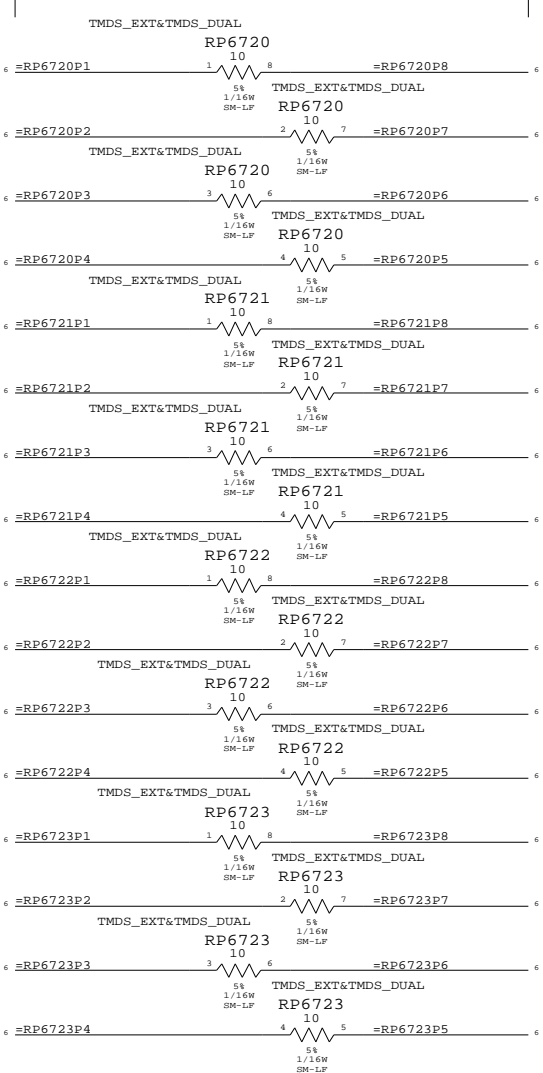
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
TMDS	DVO	DVO	GPU_DVOD<0..11> 6 54
TMDS	DVO	DVO	GPU_DVO_HSYNC 6 54 55
TMDS	DVO	DVO	GPU_DVO_VSYNC 6 54 55
TMDS	DVO	DVO	GPU_DVO_DE 6 54 55
TMDS	DVO	DVO	GPU_DVO_CLKP 6 54 55
TMDS	TMDS	TMDS	SI_TMDS_CLK 2 54
TMDS	TMDS	TMDS	SI_TMDS_CLKP 2 54
TMDS	TMDS	TMDS	SI_TMDS_D0 54
TMDS	TMDS	TMDS	SI_TMDS_D1 2 54
TMDS	TMDS	TMDS	SI_TMDS_D2 2 54
TMDS	TMDS	TMDS	SI_TMDS_D0 54
TMDS	TMDS	TMDS	SI_TMDS_D1 2 54
TMDS	TMDS	TMDS	SI_TMDS_D2 2 54

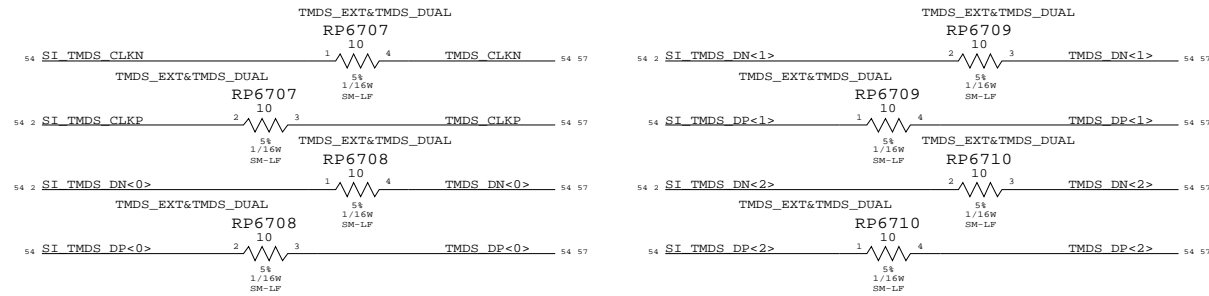
Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>
 GPU_DVO_HSYNC
 GPU_DVO_VSYNC
 GPU_DVO_DE
 GPU_DVO_CLKP

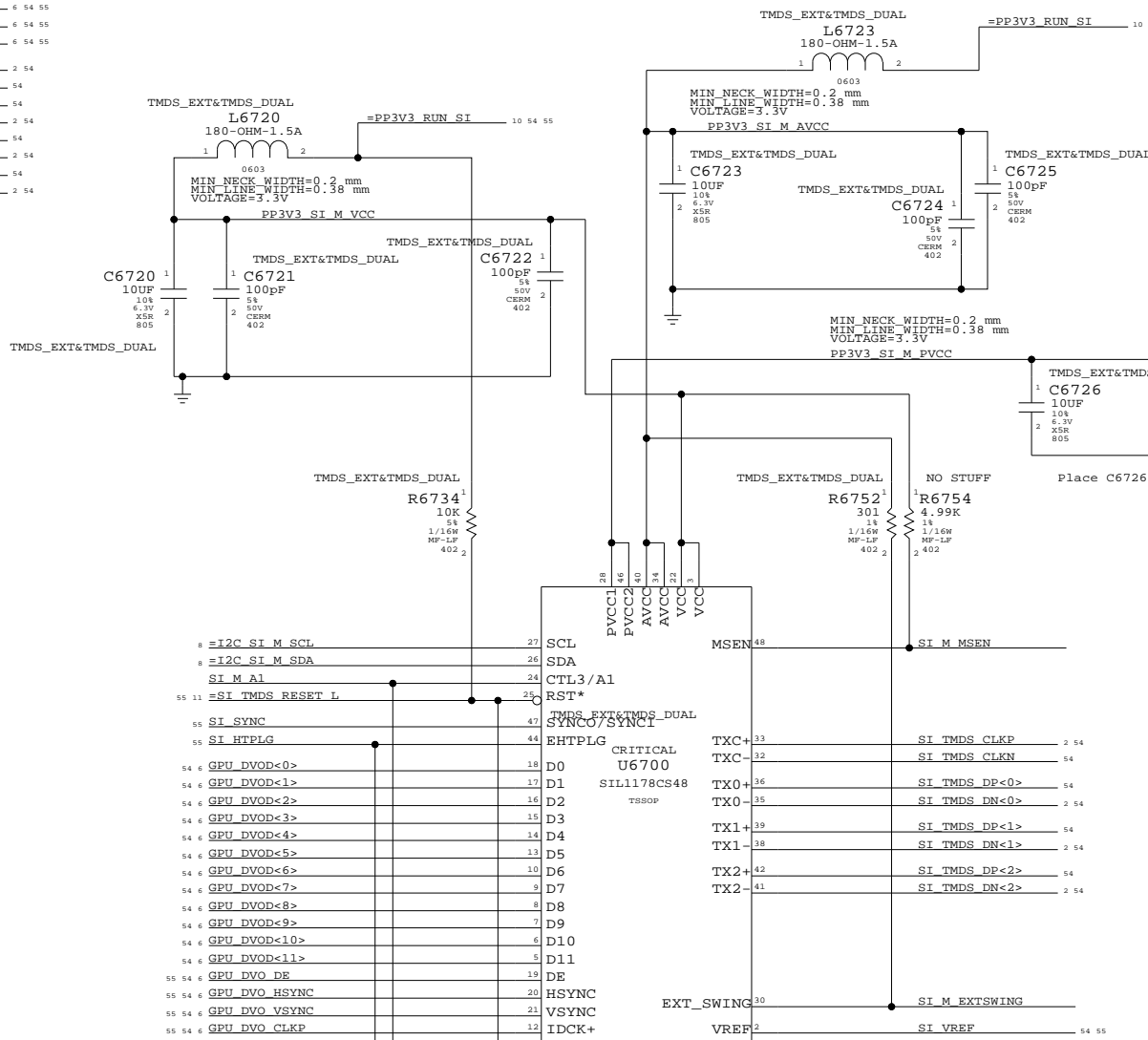
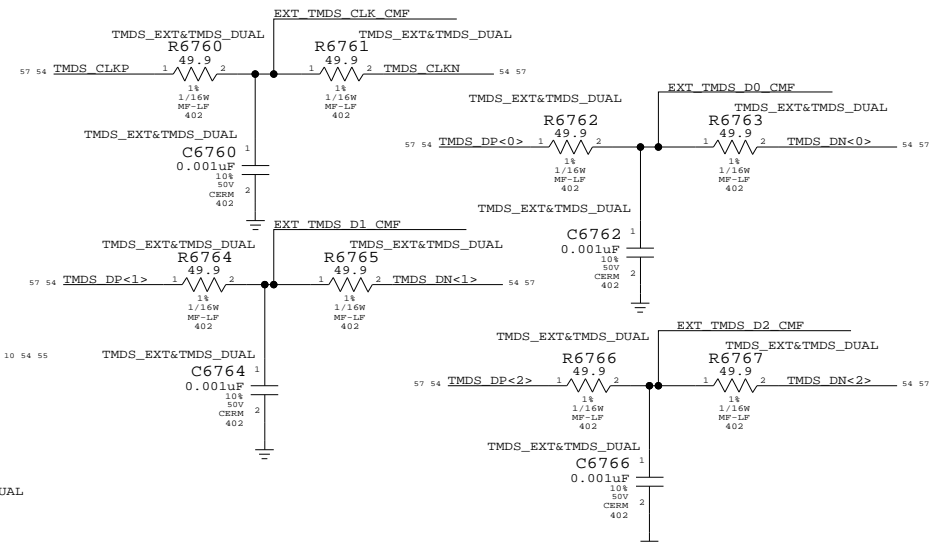


SILICON IMAGE TMDS



EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN



ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
TMDS	TMDS	TMDS	TMDS_CLK 54 57
TMDS	TMDS	TMDS	TMDS_CLKN 54 57
TMDS	TMDS	TMDS	TMDS_D0 54 57
TMDS	TMDS	TMDS	TMDS_D1 54 57
TMDS	TMDS	TMDS	TMDS_D2 54 57
TMDS	TMDS	TMDS	TMDS_DP<0> 54 57
TMDS	TMDS	TMDS	TMDS_DP<1> 54 57
TMDS	TMDS	TMDS	TMDS_DP<2> 54 57

Lower TMDS Transmitter

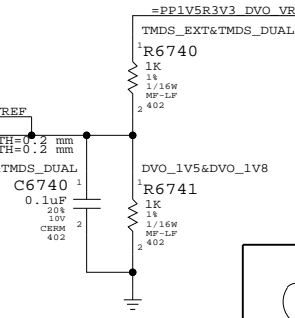
SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF	
NONE	67	115	

The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.



Page Notes

Power aliases required by this page:
 - =PP3V3_RUN_SI

Signal aliases required by this page:
 - =SI_I2C_CLK - =SI_TMDS_RESET_L
 - =SI_I2C_DATA - =RP68xxPy (pin-swappable series R)

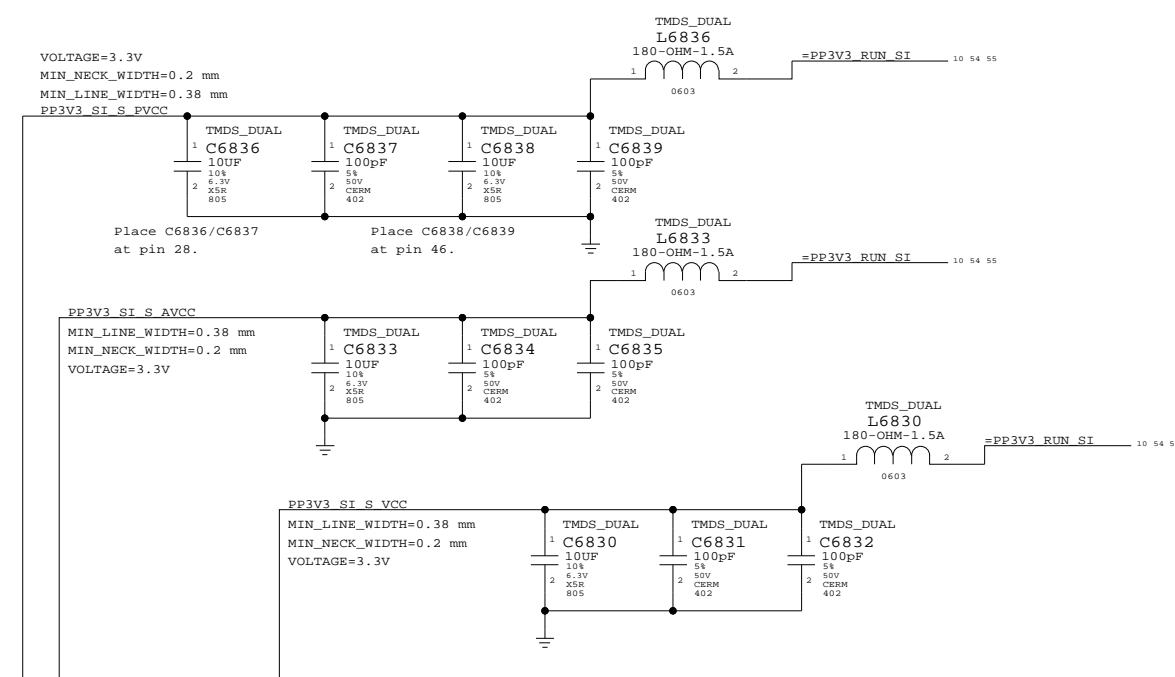
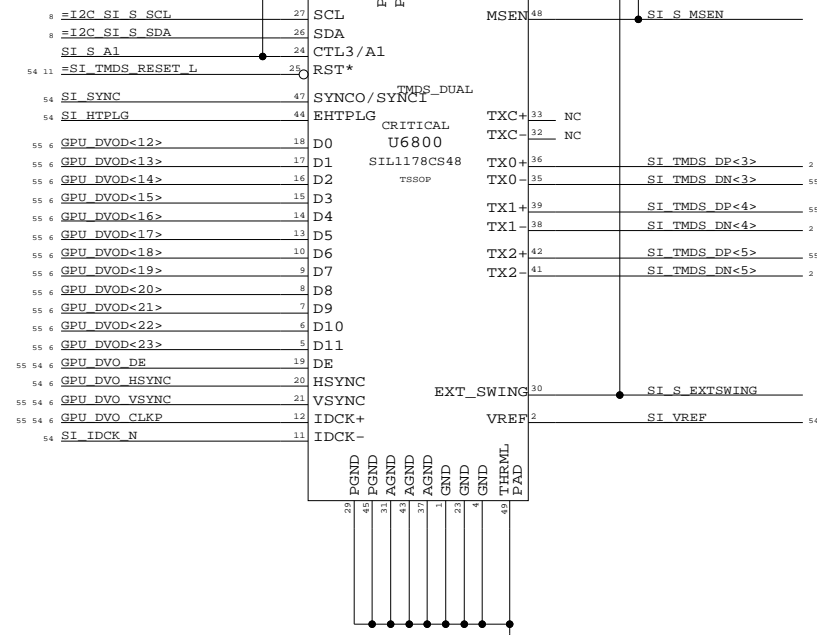
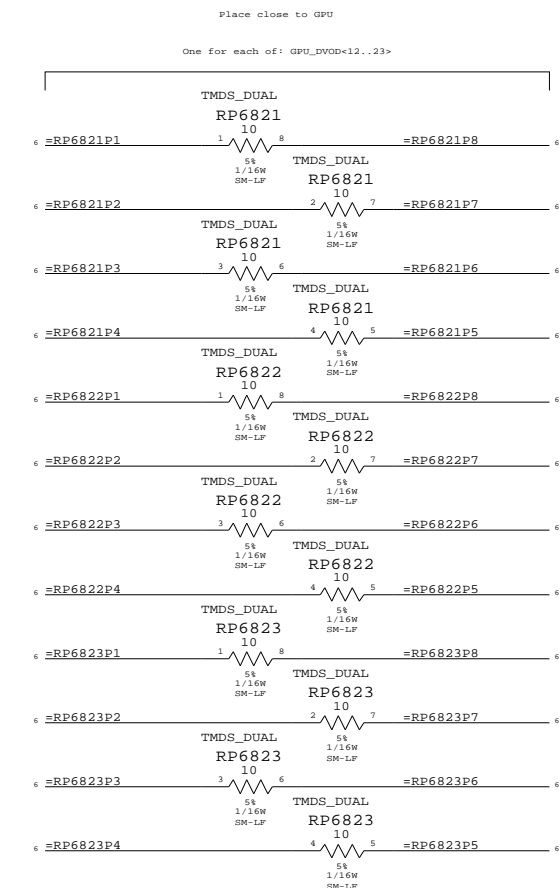
BOM options provided by this page:
 - TMDS_DUAL

Net Spacing Type: TMDS
 Net Physical Type: TMDS

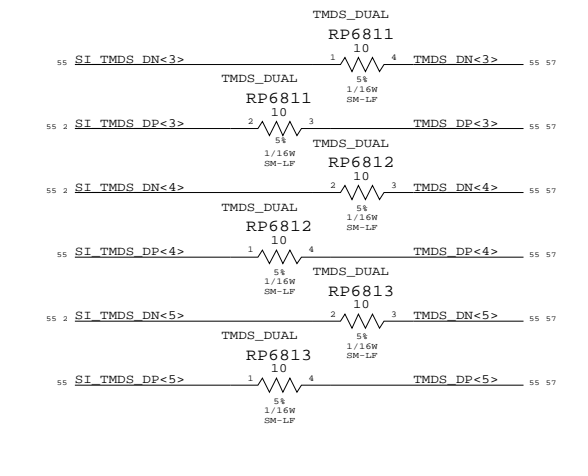
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
GPU_DVO_UPPER	DVO	DVO	
GPU_DVOD20	DVO	DVO	
GPU_DVO_UPPER	DVO	DVO	
GPU_DVO_VSYNC	PROVIDED BY LOWER TXMR		
GPU_DVO_DE	PROVIDED BY LOWER TXMR		
GPU_DVO_CLKP	PROVIDED BY LOWER TXMR		
TMDS_DATA	TMDS	TMDS	SI TMDS_D3
TMDS_DATA	TMDS	TMDS	SI TMDS_D3
TMDS_DATA	TMDS	TMDS	SI TMDS_D4
TMDS_DATA	TMDS	TMDS	SI TMDS_D4
TMDS_DATA	TMDS	TMDS	SI TMDS_D5
TMDS_DATA	TMDS	TMDS	SI TMDS_D5
TMDS_D3	TMDS	TMDS	TMDS_D3
TMDS_D3	TMDS	TMDS	TMDS_D3
TMDS_D4	TMDS	TMDS	TMDS_D4
TMDS_D4	TMDS	TMDS	TMDS_D4
TMDS_D5	TMDS	TMDS	TMDS_D5
TMDS_D5	TMDS	TMDS	TMDS_D5

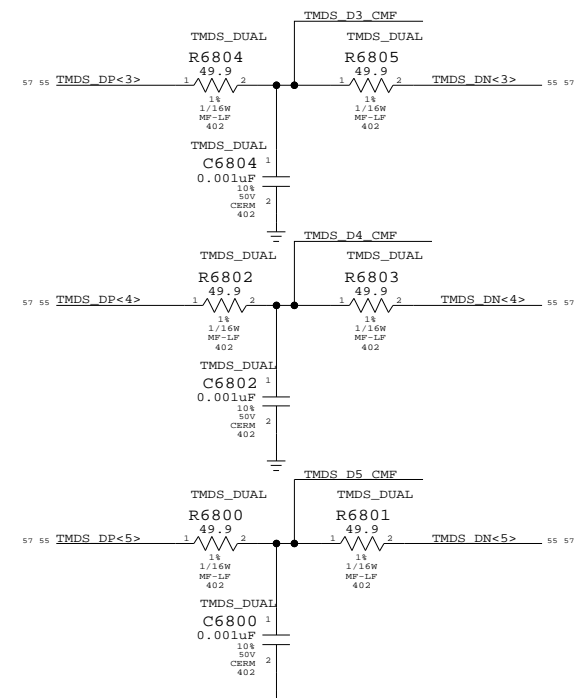
Upper DVO series termination



Upper Channel Series Termination



Upper Channel Common-mode Termination



Upper TMDS Transmitter

SYNC_MASTER=N/A SYNC_DATE=N/A

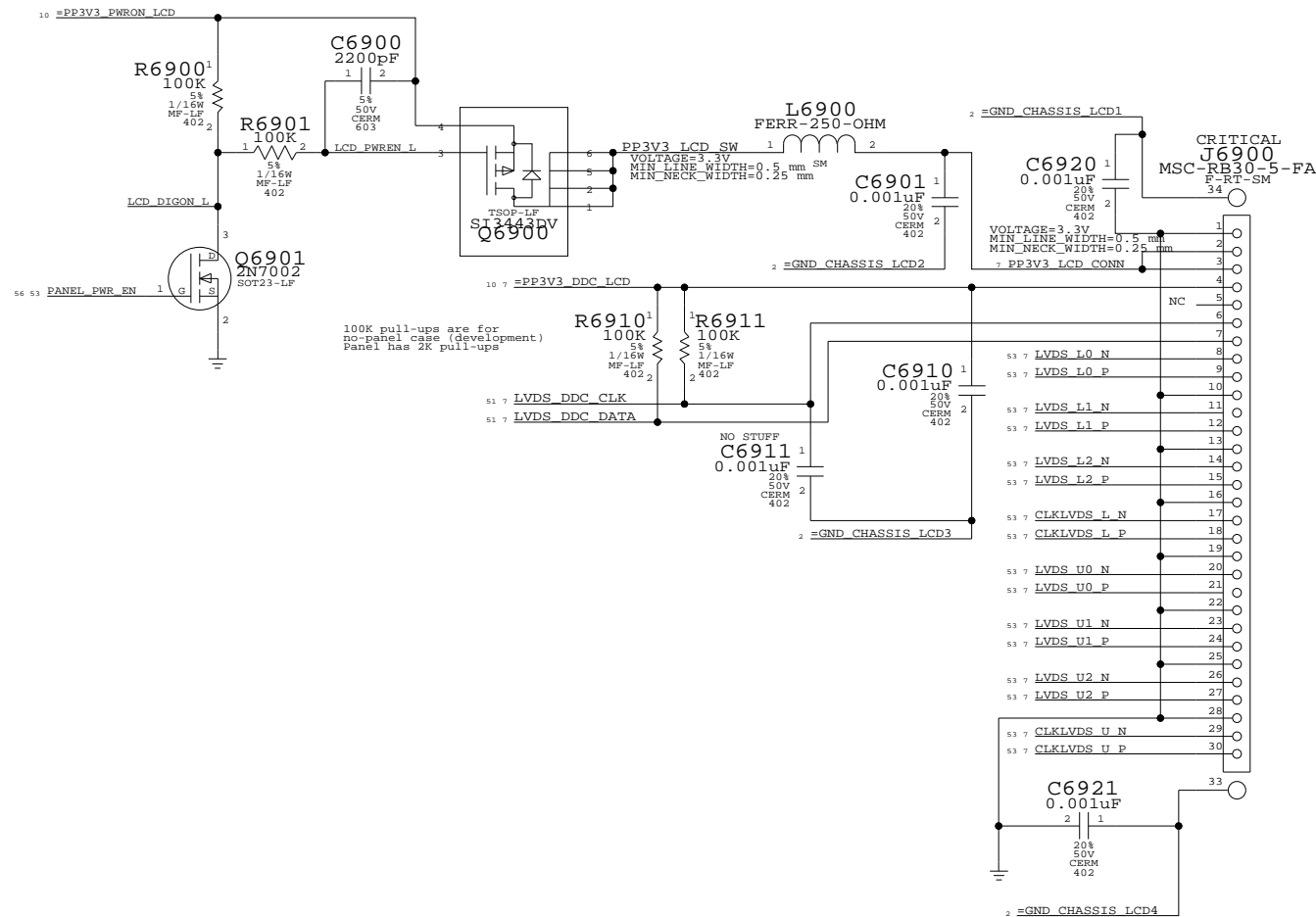
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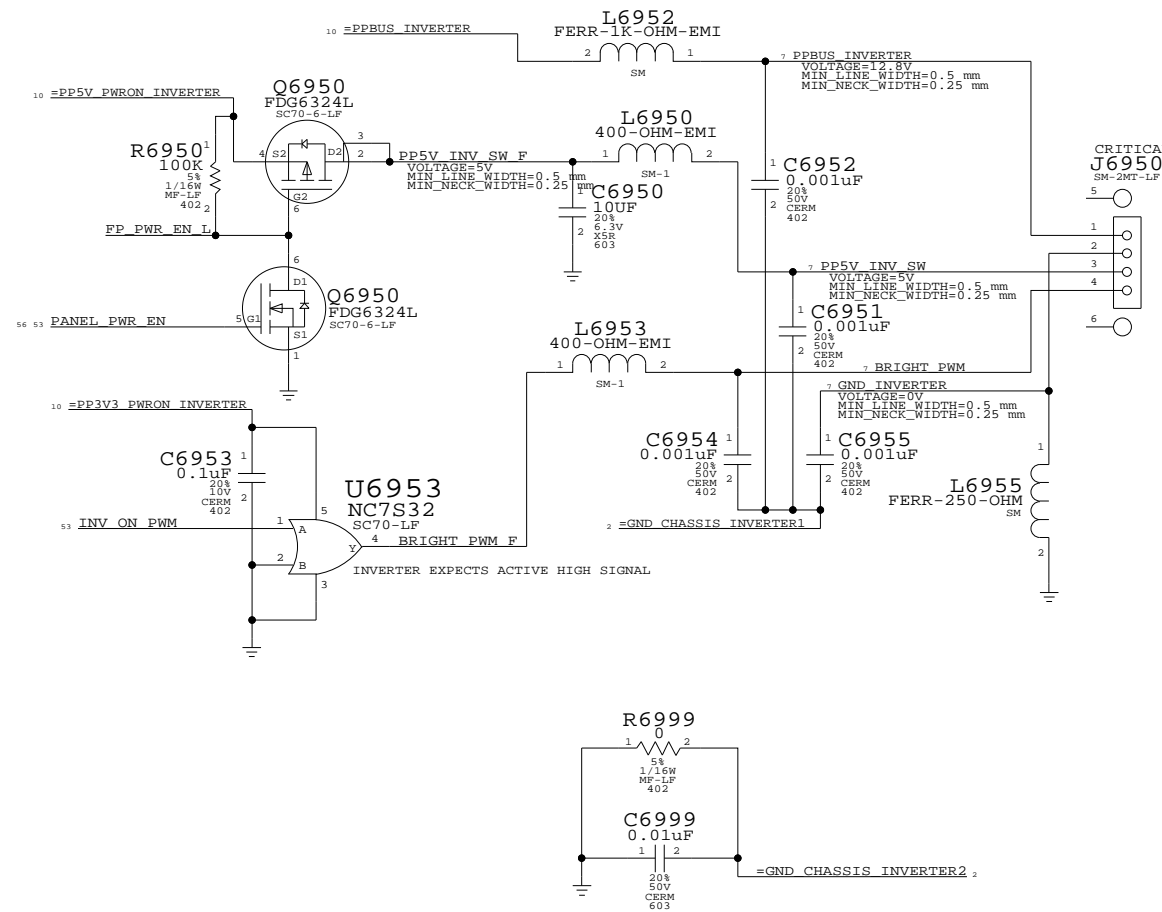
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SCALE	NONE	SHT OF	68 115

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

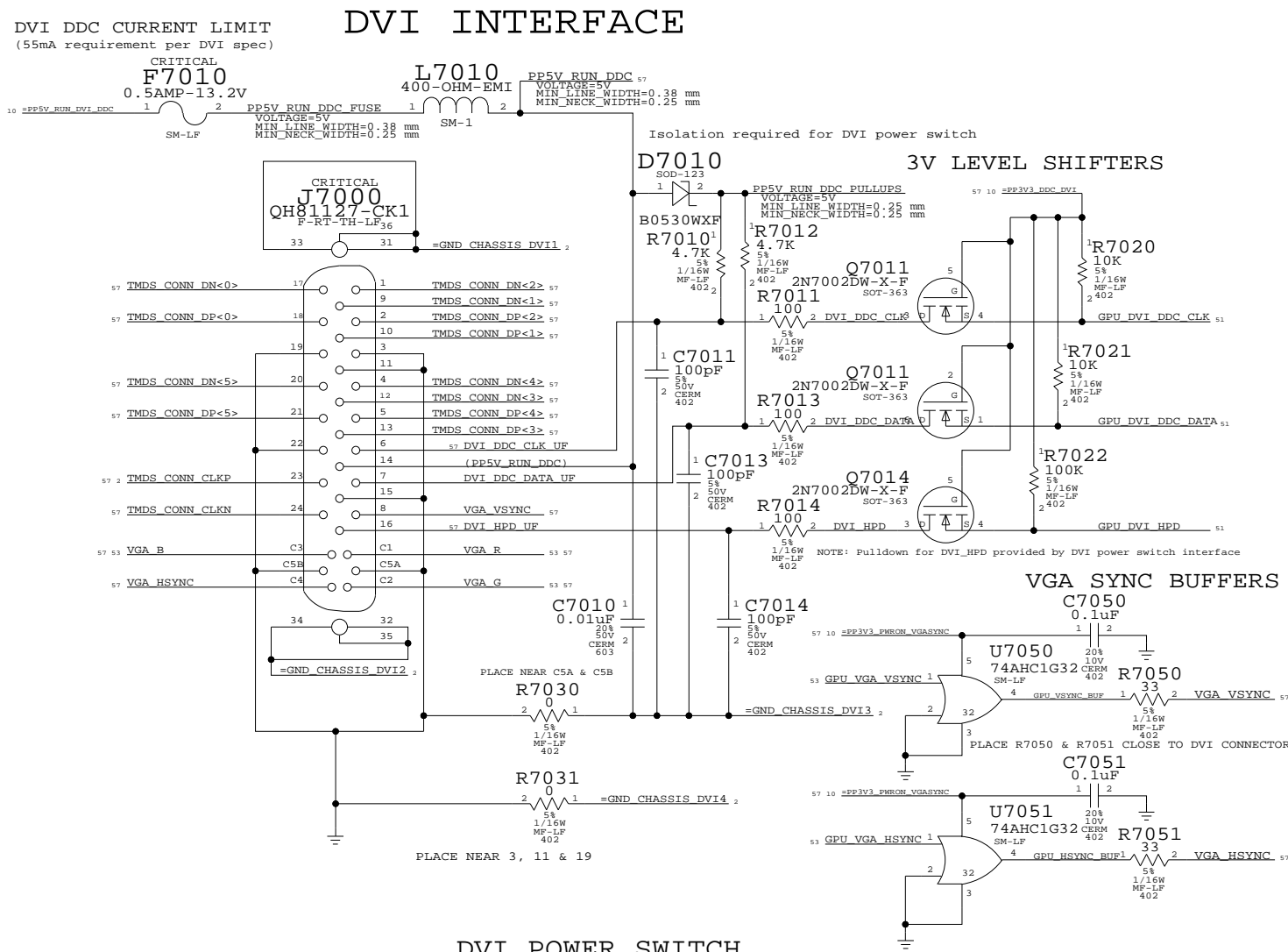
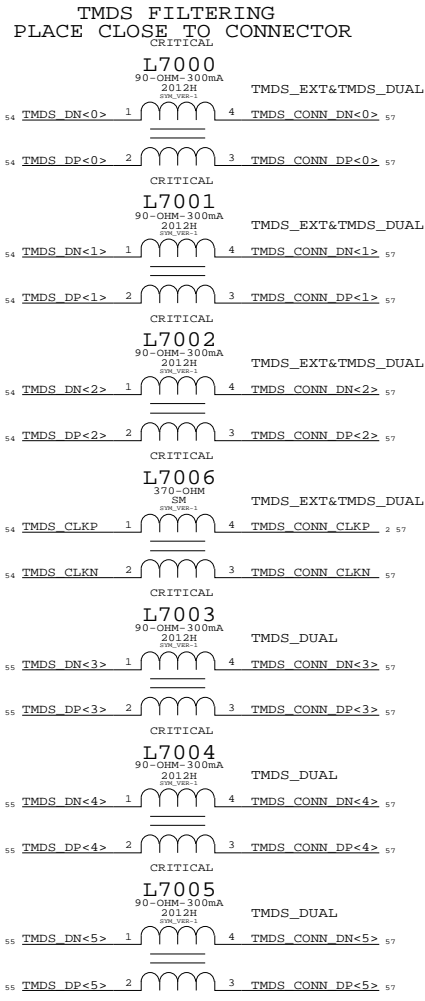
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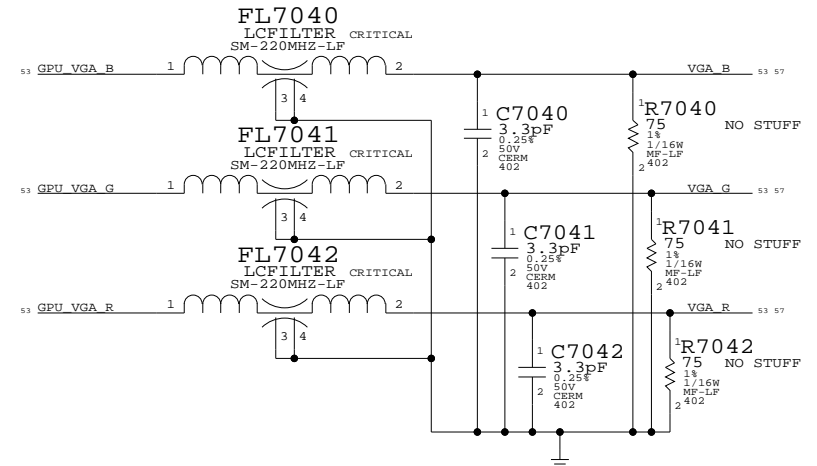
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT OF	69 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLK	TMDS_CONN_CLK
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_CLKN	TMDS_CONN_CLKN
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DP<0>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D0	TMDS_CONN_DN<0>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DP<1>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D1	TMDS_CONN_DN<1>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DP<2>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D2	TMDS_CONN_DN<2>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DP<3>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D3	TMDS_CONN_DN<3>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DP<4>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D4	TMDS_CONN_DN<4>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DP<5>
E540	TMDS_CONN_TMDS_CONN		TMDS_CONN_D5	TMDS_CONN_DN<5>

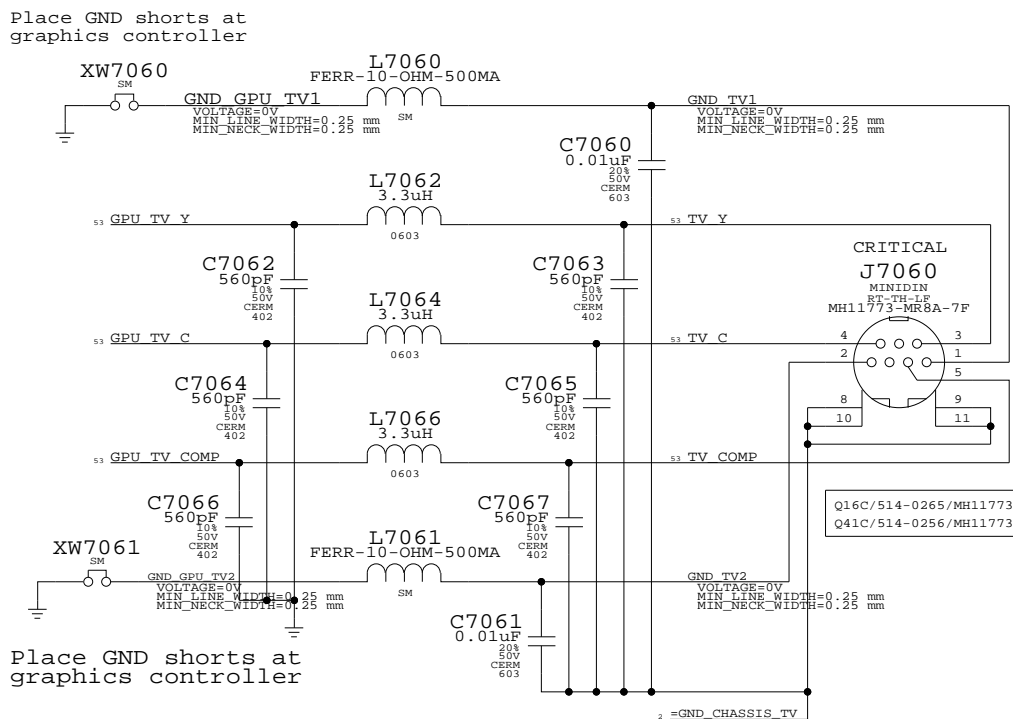


ANALOG FILTERING

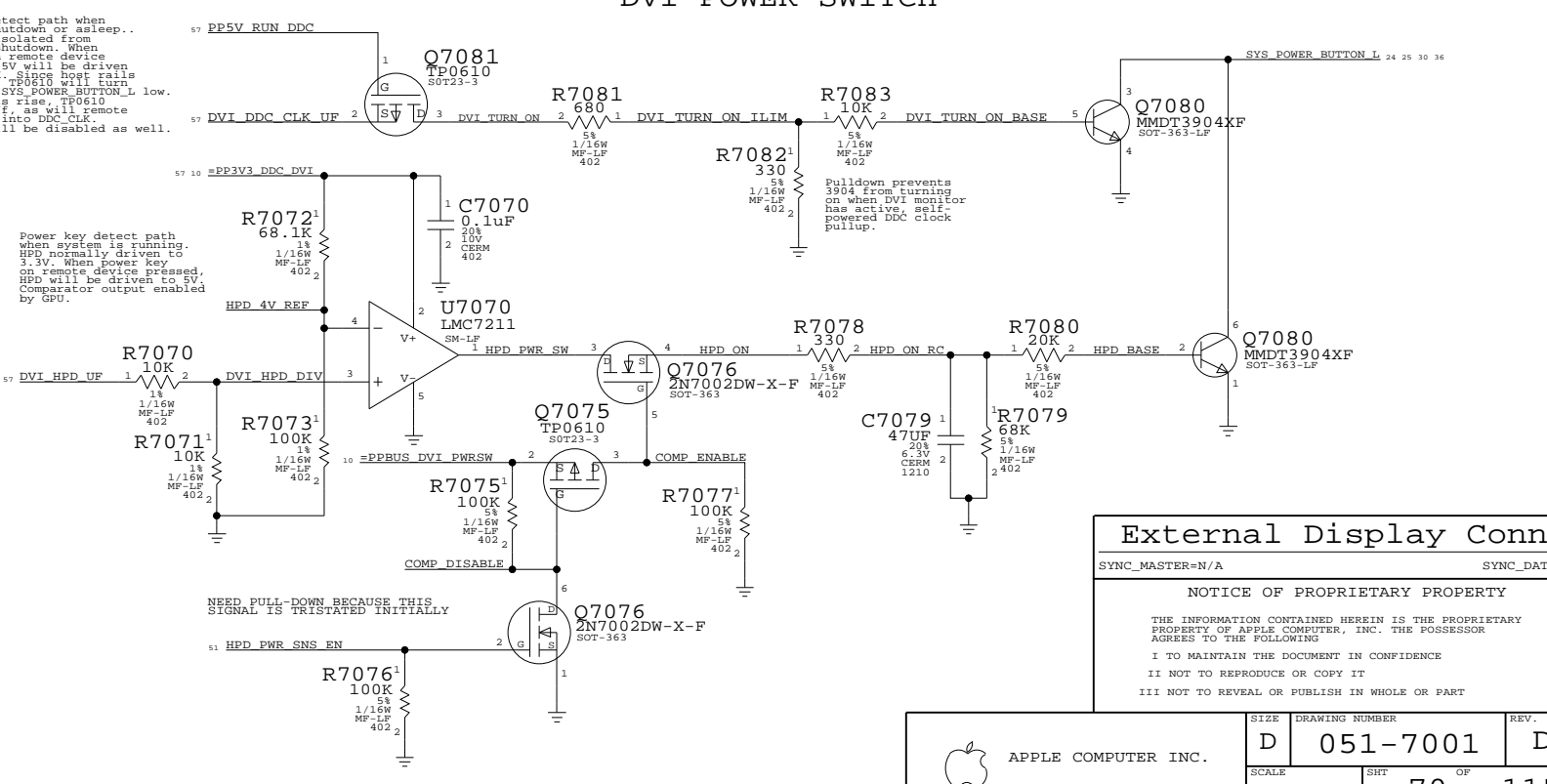
PLACE CLOSE TO CONNECTOR



S-VIDEO/COMP OUT INTERFACE



Power key detect path when system is shutdown or asleep... DDC CLK is isolated from GPU during shutdown. When power key on, remote device is pressed, 5V will be driven into DDC CLK. Since hot rails will be low, TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As hot rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.



External Display Conns

SYNC_MASTER=N/A SYNC_DATE=N/A

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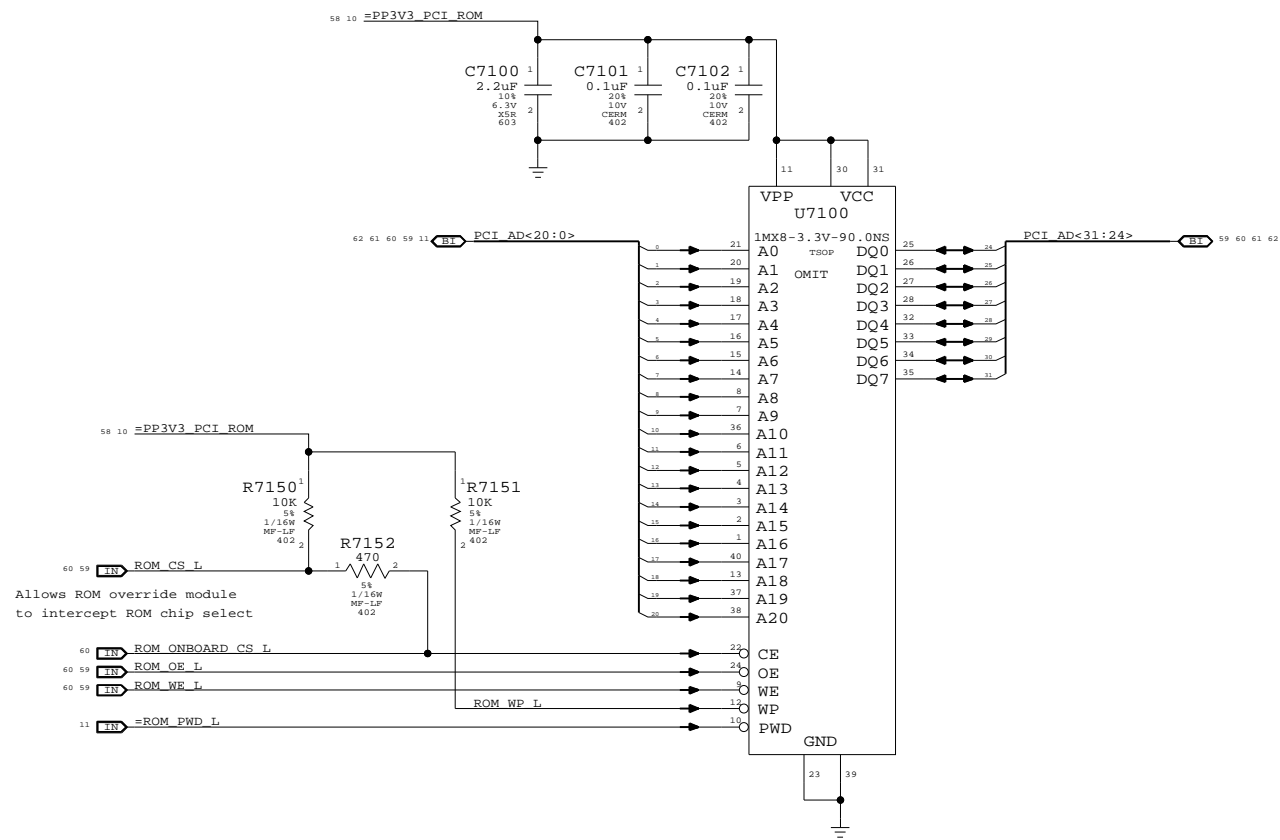
Page Notes

Power aliases required by this page:
 - =PP3V3_PCI_ROM

Signal aliases required by this page:
 - =ROM_PWD_L

BOM options provided by this page:
 (NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7100 part number.



BootROM

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	D	051-7001	D
SCALE	SHT OF		
NONE	71 OF		115

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI_CLK_SLOTA	CLOCK	CLOCK	
PCI_CLK_SLOTD	CLOCK	CLOCK	
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK	
PCI_AD<16..0>	PCI	PCI	
PCI_AD<17>	PCI	PCI	
PCI_AD<19..18>	PCI	PCI	
PCI_AD<20>	PCI	PCI	
PCI_AD<21>	PCI	PCI	
PCI_AD<23..22>	PCI	PCI	
PCI_AD<31..24>	PCI	PCI	
PCI_CBE L<3..0>	PCI	PCI	
PCI_FRAME L	PCI	PCI	
PCI_DEVSEL L	PCI	PCI	
PCI_TRDY L	PCI	PCI	
PCI_STOP L	PCI	PCI	
PCI_PAR	PCI	PCI	
PCI_SLOTA_REQ L	PCI	PCI	
PCI_SLOTA_GNT L	PCI	PCI	
PCI_SLOTD_REQ L	PCI	PCI	
PCI_SLOTD_GNT L	PCI	PCI	

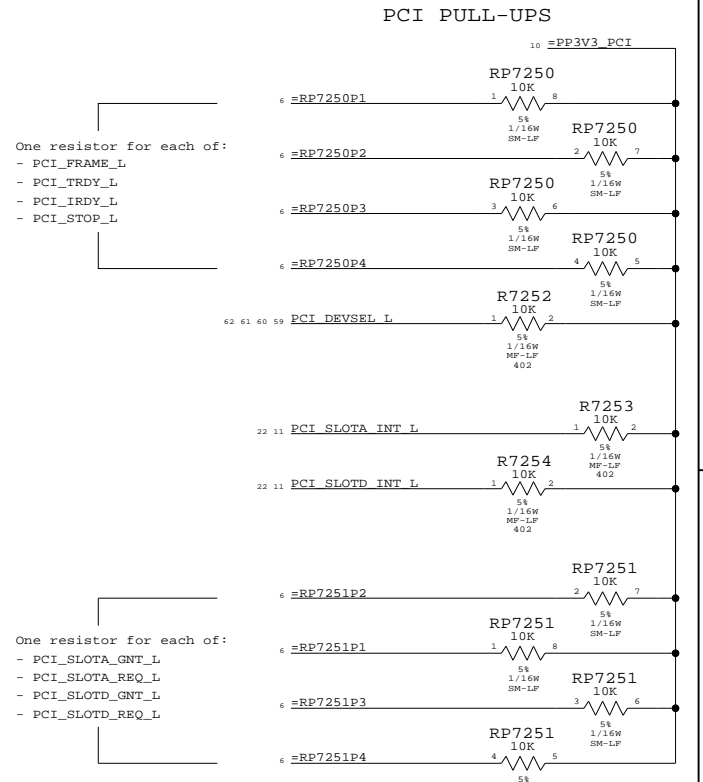
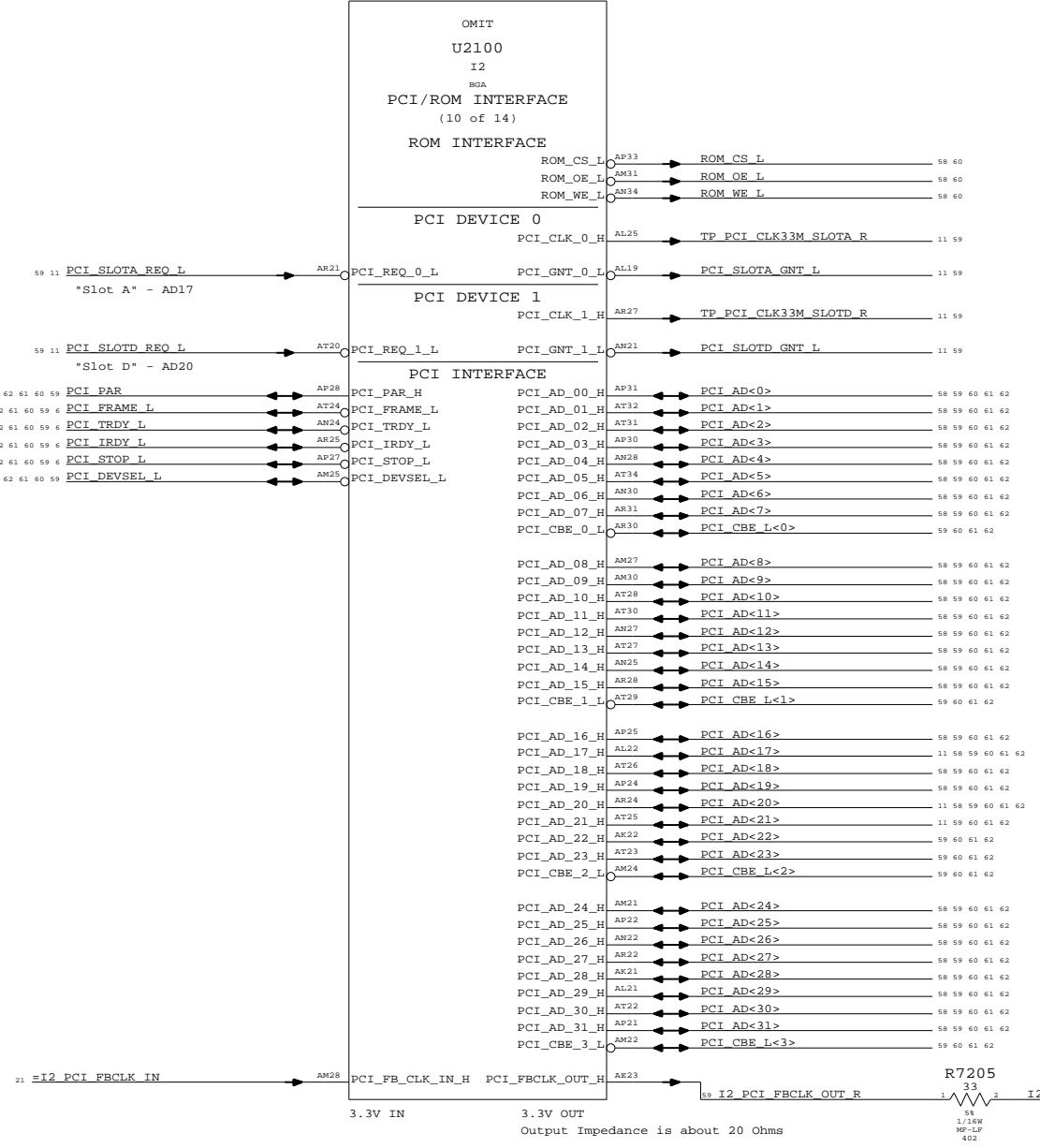
TP_PCI_CLK33M_SLOTA_R	11 59
TP_PCI_CLK33M_SLOTD_R	11 59
I2_PCI_FBCLK_OUT_R	59
I2_PCI_FBCLK_OUT	21 59
PCI_AD<16..0>	58 59 60 61 62 (BOOTROM ADDR)
PCI_AD<17>	11 58 59 60 61 (BOOTROM ADDR/SLOT A IDSEL)
PCI_AD<19..18>	58 59 60 61 62 (BOOTROM ADDR)
PCI_AD<20>	11 58 59 60 61 (SLOT D IDSEL)
PCI_AD<21>	11 59 60 61 62 (SLOT E IDSEL)
PCI_AD<23..22>	(PCI ONLY)
PCI_AD<31..24>	(BOOTROM DATA)
PCI_CBE L<3..0>	59 60 61 62
PCI_FRAME L	6 59 60 61 62
PCI_DEVSEL L	59 60 61 62
PCI_TRDY L	6 59 60 61 62
PCI_STOP L	6 59 60 61 62
PCI_PAR	59 60 61 62
PCI_SLOTA_REQ L	11 59
PCI_SLOTA_GNT L	11 59
PCI_SLOTD_REQ L	11 59
PCI_SLOTD_GNT L	11 59

Page Notes

Power aliases required by this page:
 - =PP3V3_PCI

Signal aliases required by this page:
 - =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
 (NONE)



SLOT E REQ/GNT pull-ups not provided by this page.

I2 PCI Interface
 SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		72	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
MEM	CLOCK	CLOCK	

=PCI_CLK33M_AIRPORT 11 60

Page Notes

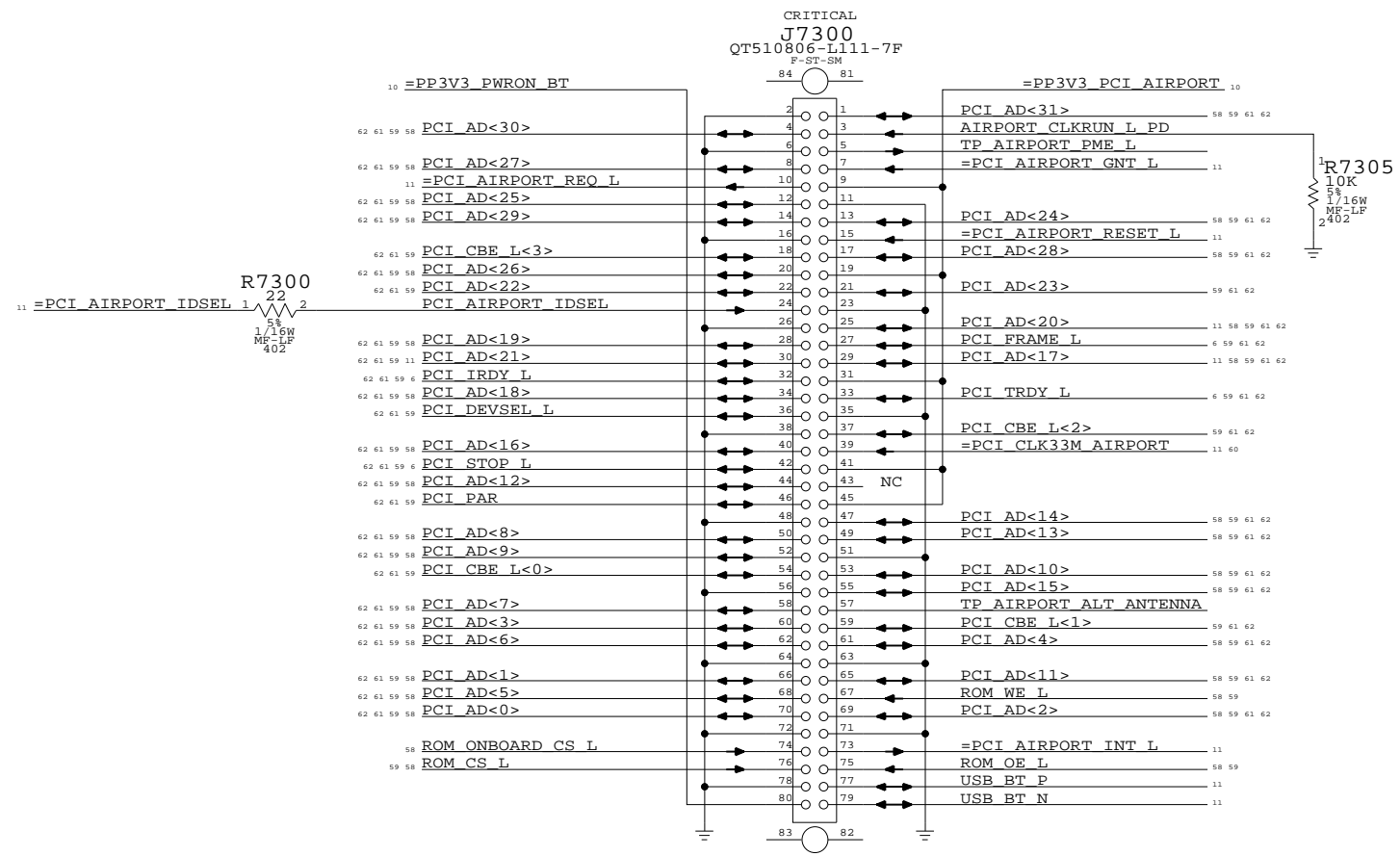
Power aliases required by this page:
 - =PP3V3_PCI (802.11g Power)
 - =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
 - =PCI_CLK33M_AIRPORT (33MHz PCI clock)
 - =PCI_AIRPORT_RESET_L (PCI Reset)
 - =USB_BT_P (Bluetooth USB D+)
 - =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
 (NONE)

PCI Devices implemented on this page:
 ADL7 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



Q85 Connector
 Q16C/516S0361/F-ST-SM
 Q41C/516S0352/M-ST-SM-LF

Q85 Airport/BT Connector

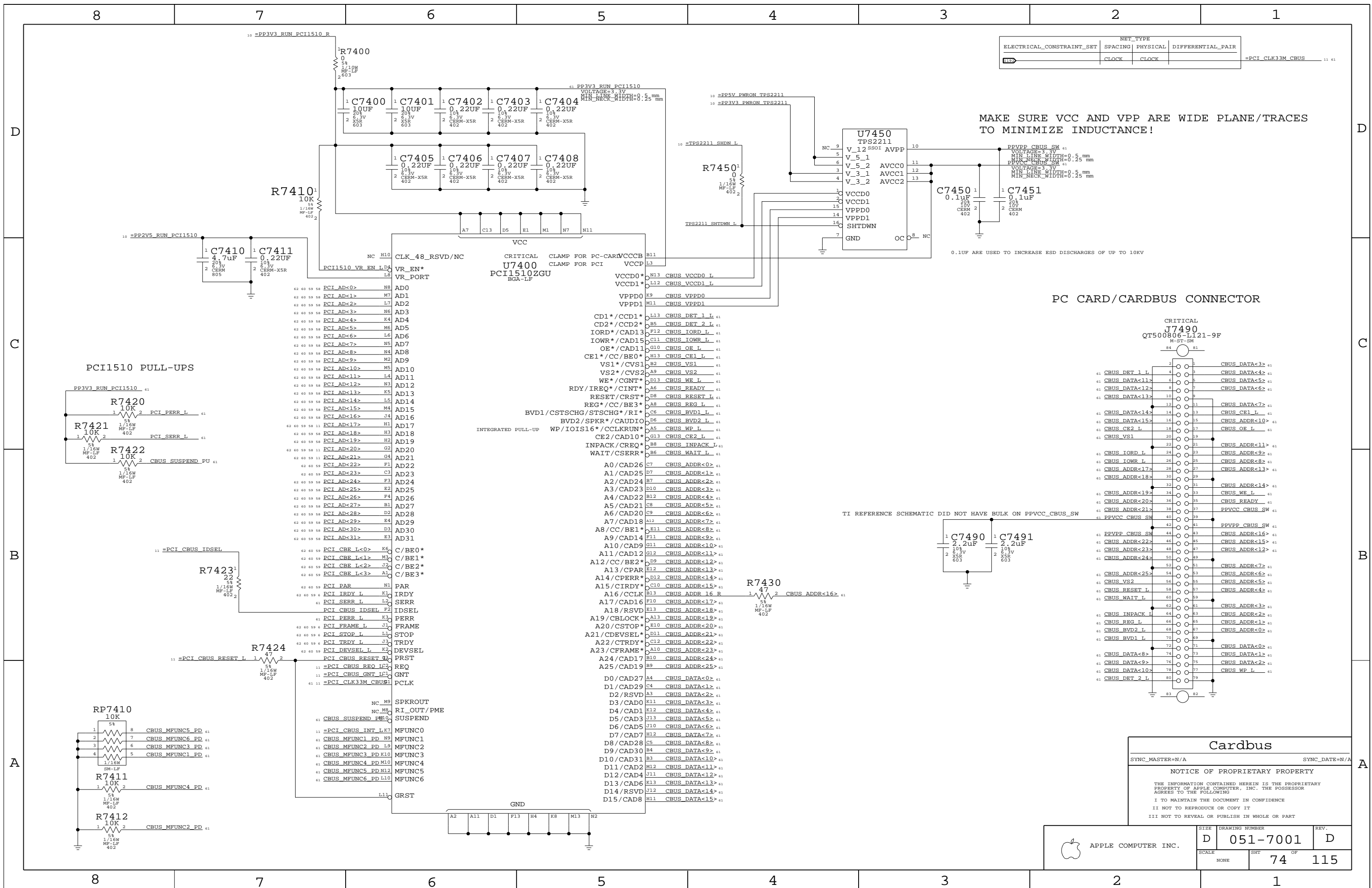
SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		73	115



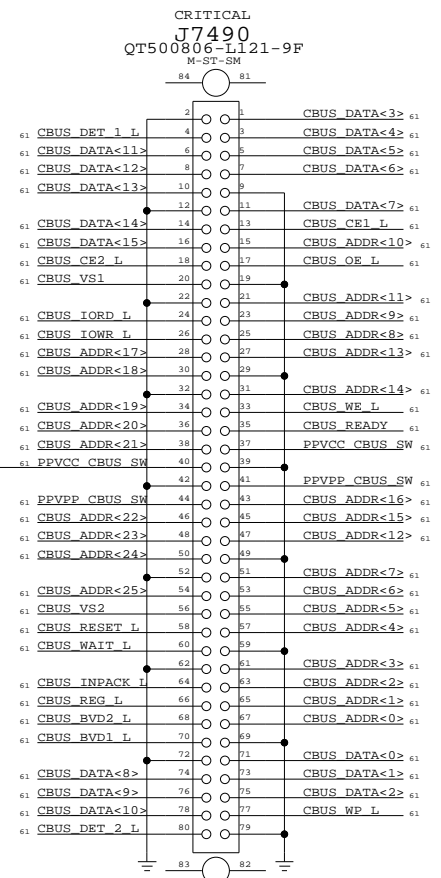
NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E13	CLOCK	CLOCK	

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

VOLTAGE=3.3V
MIN_PLANE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.25mm

0.1uF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10Kv

PC CARD/CARDBUS CONNECTOR



Cardbus

SYNC_MASTER=N/A SYNC_DATE=N/A

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NONE	74	115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFFERENTIAL_PAIR
	SPACING	PHYSICAL	
	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 62

Page Notes

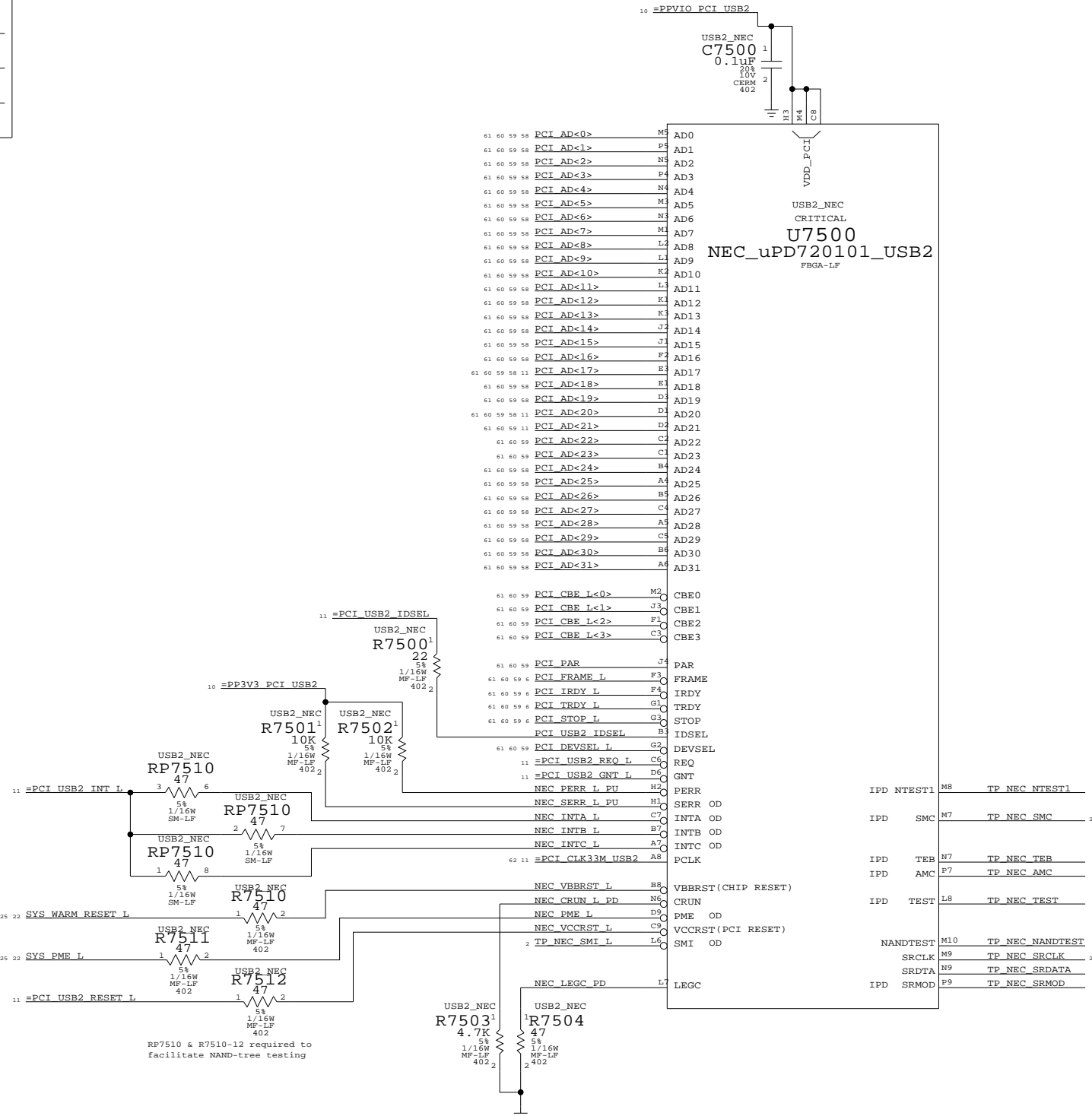
Power aliases required by this page:
 - =PPVIO_PCI (to 3.3V or 5V)
 - =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
 - =PCI_CLK33M_USB2
 - =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
 - =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
 - =PCI_USB2_INT_L

BOM options provided by this page:
 - USB2_NEC

PCI Devices implemented on this page:
 AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



61 60 59 58 PCI_AD<0> M5 AD0
 61 60 59 58 PCI_AD<1> P5 AD1
 61 60 59 58 PCI_AD<2> N5 AD2
 61 60 59 58 PCI_AD<3> P4 AD3
 61 60 59 58 PCI_AD<4> M4 AD4
 61 60 59 58 PCI_AD<5> M3 AD5
 61 60 59 58 PCI_AD<6> N3 AD6
 61 60 59 58 PCI_AD<7> M1 AD7
 61 60 59 58 PCI_AD<8> L4 AD8
 61 60 59 58 PCI_AD<9> L1 AD9
 61 60 59 58 PCI_AD<10> K2 AD10
 61 60 59 58 PCI_AD<11> L3 AD11
 61 60 59 58 PCI_AD<12> K3 AD12
 61 60 59 58 PCI_AD<13> J3 AD13
 61 60 59 58 PCI_AD<14> J1 AD14
 61 60 59 58 PCI_AD<15> J1 AD15
 61 60 59 58 PCI_AD<16> F2 AD16
 61 60 59 58 11 PCI_AD<17> E3 AD17
 61 60 59 58 PCI_AD<18> E1 AD18
 61 60 59 58 PCI_AD<19> D3 AD19
 61 60 59 58 11 PCI_AD<20> D1 AD20
 61 60 59 58 11 PCI_AD<21> D2 AD21
 61 60 59 PCI_AD<22> C2 AD22
 61 60 59 PCI_AD<23> C1 AD23
 61 60 59 58 PCI_AD<24> B4 AD24
 61 60 59 58 PCI_AD<25> A4 AD25
 61 60 59 58 PCI_AD<26> B5 AD26
 61 60 59 58 PCI_AD<27> C4 AD27
 61 60 59 58 PCI_AD<28> A5 AD28
 61 60 59 58 PCI_AD<29> C5 AD29
 61 60 59 58 PCI_AD<30> B6 AD30
 61 60 59 58 PCI_AD<31> A6 AD31

61 60 59 PCI_CBE_L<0> M2 CBE0
 61 60 59 PCI_CBE_L<1> J1 CBE1
 61 60 59 PCI_CBE_L<2> F1 CBE2
 61 60 59 PCI_CBE_L<3> C1 CBE3

61 60 59 PCI_PAR J4 PAR
 61 60 59 4 PCI_FRAME_L F2 FRAME
 61 60 59 4 PCI_IRDY_L F4 IRDY
 61 60 59 4 PCI_TRDY_L G1 TRDY
 61 60 59 4 PCI_STOP_L G3 STOP
 61 60 59 PCI_USB2_IDSEL B3 IDSEL
 61 60 59 PCI_DEVSEL_L G2 DEVSEL

11 =PCI_USB2_REQ_L CC REQ
 11 =PCI_USB2_GNT_L DC GNT
 NEC_PERR_L PU H2 PERR
 NEC_SERR_L PU H1 SERR OD
 NEC_INTA_L PU C1 INTA OD
 NEC_INTB_L PU H1 INTB OD
 NEC_INTC_L PU A1 INTC OD
 62 11 =PCI_CLK33M_USB2 A8 PCLK

NEC_VBRRST_L B6 VBRRST(CHIP RESET)
 NEC_CRUN_L PD M1 CRUN
 NEC_PME_L D3 PME OD
 NEC_VCCRST_L C3 VCCRST(PCI RESET)
 TP_NEC_SMI_L L6 SMI OD

NEC_LEG_C_PD L1 LEGC

IPD NTEST1 M8 TP_NEC_NTEST1
 IPD SMC M7 TP_NEC_SMC
 IPD TEB N7 TP_NEC_TEB
 IPD AMC F7 TP_NEC_AMC
 IPD TEST L8 TP_NEC_TEST
 NANDTEST M10 TP_NEC_NANDTEST
 SRCLK M9 TP_NEC_SRCLK
 SRDATA N9 TP_NEC_SRDATA
 IPD SRMOD F9 TP_NEC_SRMOD

RP7510 & R7510-12 required to facilitate NAND-tree testing

NEC USB2

SYNC_MASTER=N/A SYNC_DATE=N/A

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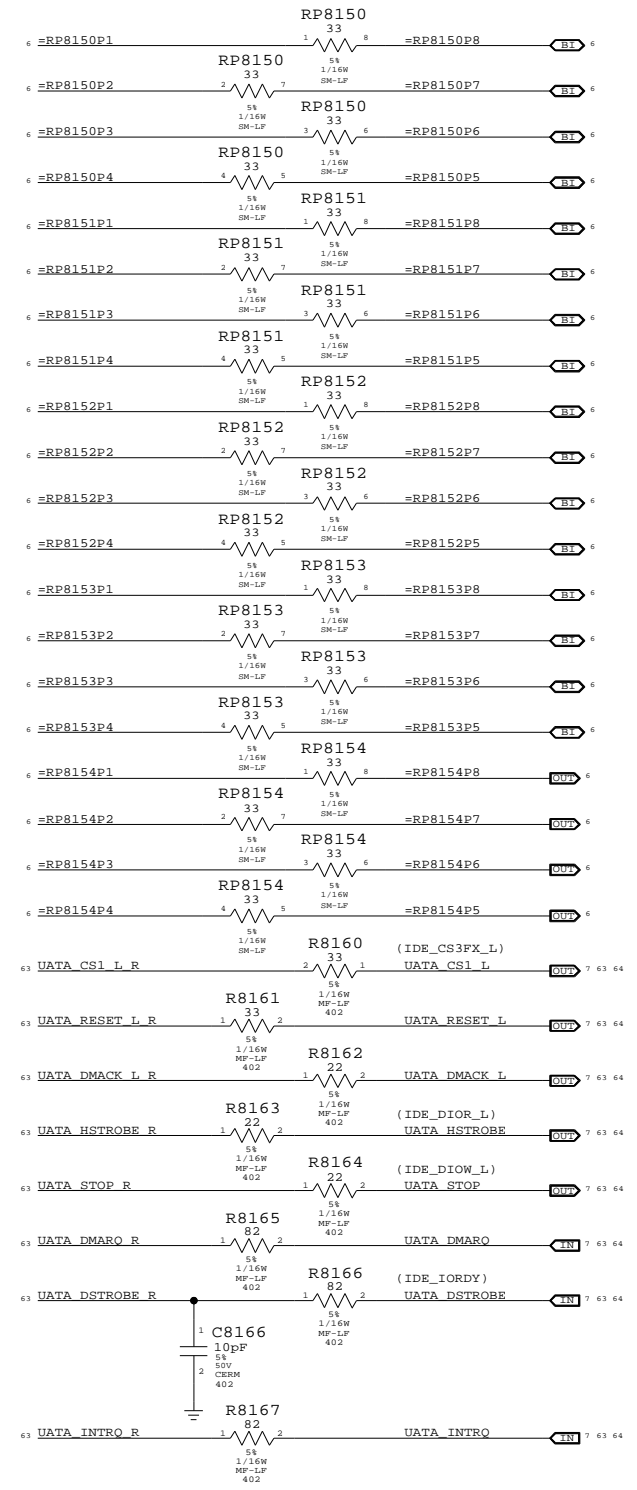
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SCALE	SHEET OF		
NONE	75 OF		115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			PART	QTY
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
UATA_DD<15..8>	DATA	DATA		UATA_DD R<15..8>	2 6 63
UATA_DD<7>	DATA	DATA		UATA_DD R<7>	6 63
UATA_DD<6..0>	DATA	DATA		UATA_DD R<6..0>	2 6 63
UATA_DA R<2..0>	DATA	DATA		UATA_DA R<2..0>	2 6 63
UATA_CS0 L R	DATA	DATA		UATA_CS0 L R	6 63
UATA_CS1 L R	DATA	DATA		UATA_CS1 L R	63
UATA_HSTROBE R	DATA	DATA		UATA_HSTROBE R	63
UATA_STOP R	DATA	DATA		UATA_STOP R	63
UATA_DMACK L R	DATA	DATA		UATA_DMACK L R	63
UATA_RESET L R	DATA	DATA		UATA_RESET L R	63
UATA_DSTROBE R	DATA	DATA		UATA_DSTROBE R	63
UATA_DMARQ R	DATA	DATA		UATA_DMARQ R	63
UATA_INTRO R	DATA	DATA		UATA_INTRO R	63
UATA_DD<15..0>	DATA	DATA		UATA_DD<15..0>	6 7 64
UATA_DA<2..0>	DATA	DATA		UATA_DA<2..0>	6 7 64
UATA_CS0 L	DATA	DATA		UATA_CS0 L	6 7 64
UATA_CS1 L	DATA	DATA		UATA_CS1 L	7 63 64
UATA_HSTROBE	DATA	DATA		UATA_HSTROBE	7 63 64
UATA_STOP	DATA	DATA		UATA_STOP	7 63 64
UATA_DMACK L	DATA	DATA		UATA_DMACK L	7 63 64
UATA_RESET L	DATA	DATA		UATA_RESET L	7 63 64
UATA_DSTROBE	DATA	DATA		UATA_DSTROBE	7 63 64
UATA_DMARQ	DATA	DATA		UATA_DMARQ	7 63 64
UATA_INTRO	DATA	DATA		UATA_INTRO	7 63 64

UATA100 SERIES TERMINATION

PLACE CLOSE TO I2



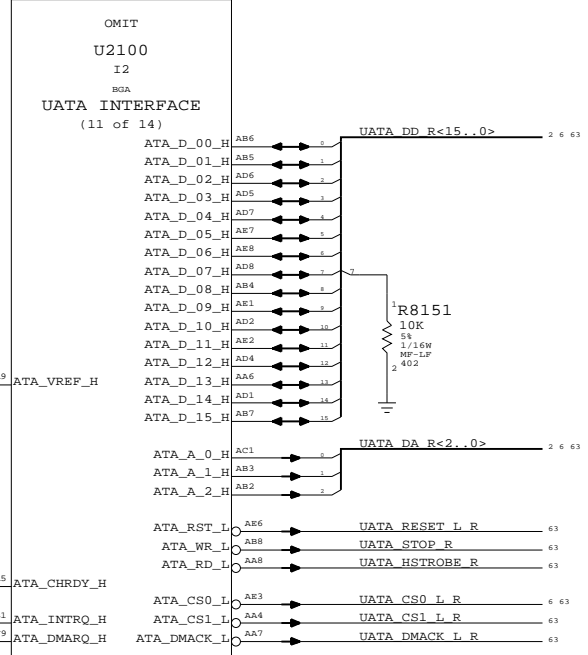
One resistor for each of:
 - UATA_DD<15..0>(_R)
 - UATA_DA<2..0>(_R)
 - UATA_CS0 L(_R) (IDE_CS1FX_L)

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 UATA Interface
 SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	NONE	SHT	OF
		81	115

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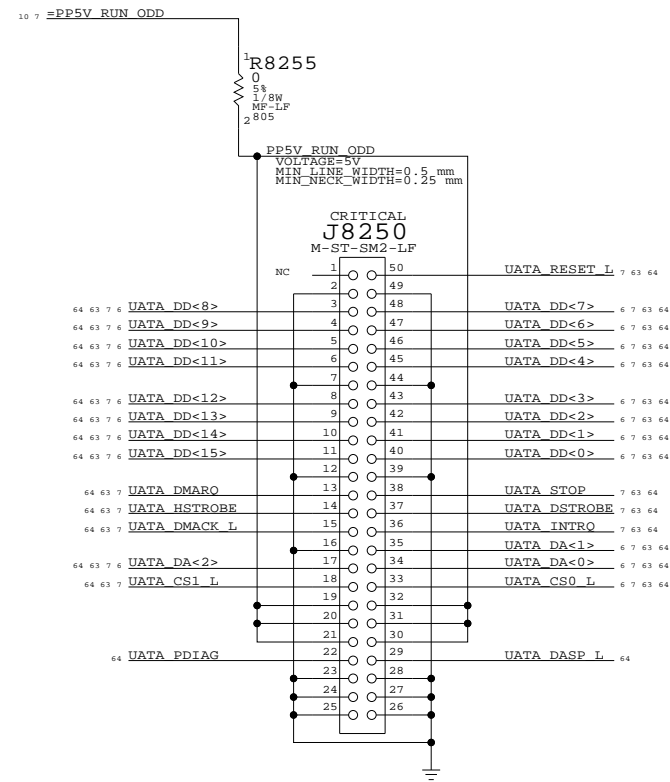
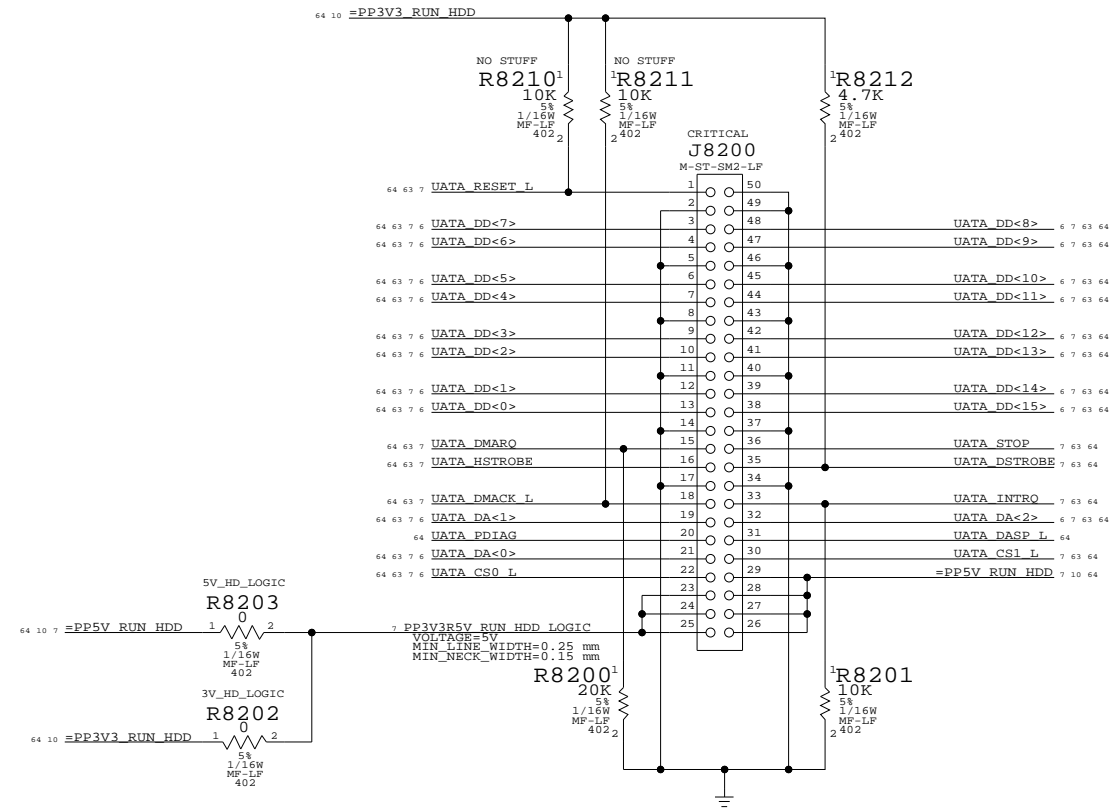
B

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HDD CONNECTOR

ODD CONNECTOR



ATA Connectors
 Q16C/516S0357/M-ST-SM2-LF
 Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors
 SYNC_MASTER=N/A SYNC_DATE=N/A
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	D	051-7001	D
SCALE	SHT OF		
NONE	82		115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
[PROVIDED BY LINK PAGE]	CLOCK	CLOCK		
[PROVIDED BY LINK PAGE]	CLOCK	CLOCK		
[PROVIDED BY LINK PAGE]	CLOCK	CLOCK		
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	
VESTA_CLK25M_XTAL	XTAL	XTAL		
VESTA_CLK25M_XTALO	XTAL	XTAL		
VESTA_CLK25M_XTALO_R	XTAL	XTAL		

Page Notes

Power aliases required by this page:
 - =PP2V5_ENETFW
 - =PP1V2_ENETFW

Signal aliases required by this page:
 (NONE)

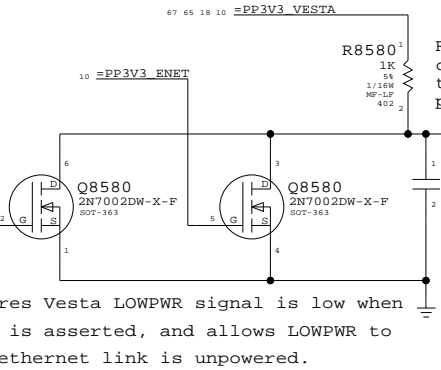
BOM options provided by this page:
 (NONE)

Net Spacing Type: ENET_MDI

Time To Line: 0.38 nms
 Length Tolerance: 50 mils
 Primary Max Sep: 5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils

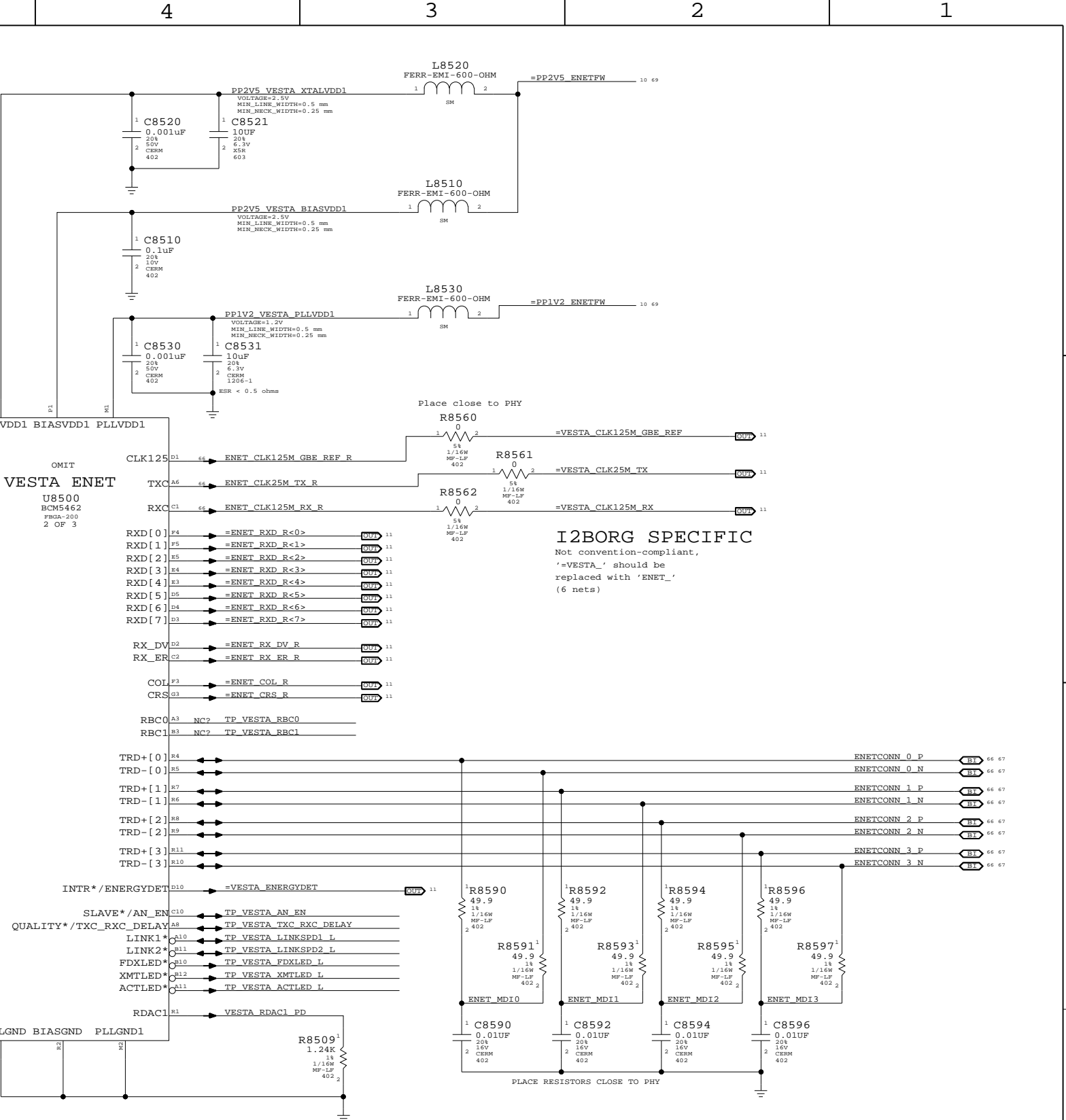
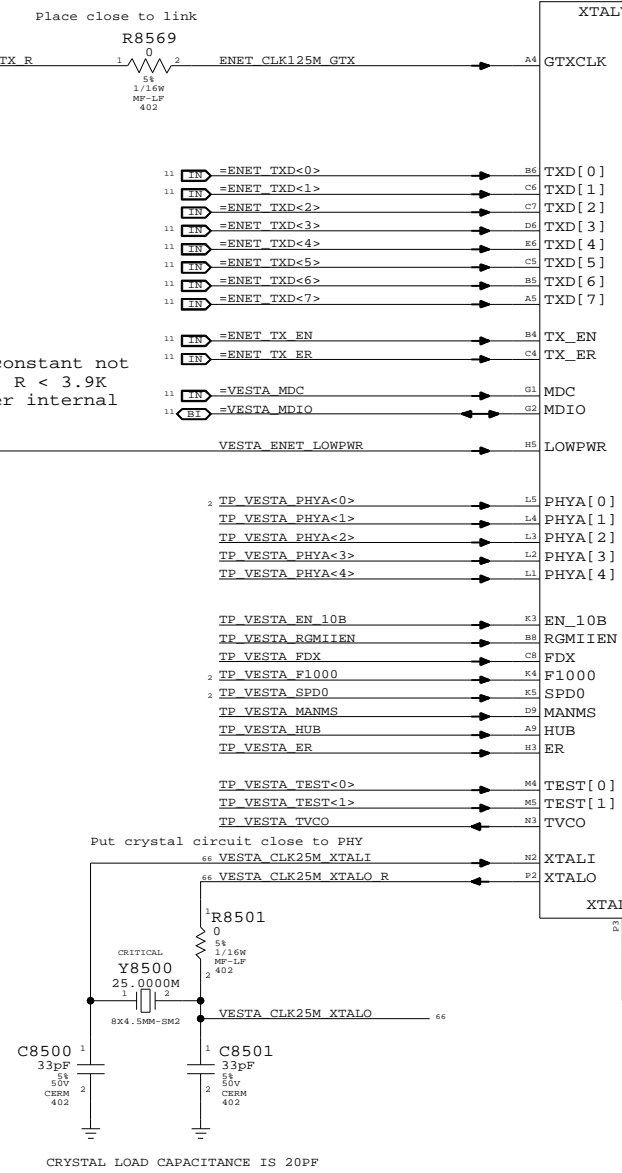
NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Ethernet LowPwr Disables Vesta Ethernet Circuit



Vesta Config Straps:

PHYA<4..0> - PHY Address Select (Internal Pull-downs)	MANMS - Manual Master/Slave Configuration Select (Internal Pull-downs)
EN_10B - TBI Interface Select (Internal Pull-down)	HUB - Repeater Select (Internal Pull-down)
RGMIEN - RGMI Enable (Internal Pull-down)	ER - Edge Rate Select (Internal Pull-down)
FDX - Full-Duplex Select (Internal Pull-up)	AN_EN - Auto-Negotiation Select (Internal Pull-up)
F1000 - Speed Select (Internal Pull-up)	TXC_RXC_DELAY - TXC/RXC Delay (Internal Pull-up)
SPD0 - Speed Select (Internal Pull-down)	
AN_EN F1000 SPD0 Description	
0 0 0	Force 10BASE-T
0 0 1	Force 100BASE-TX
0 1 X	Force 1000BASE-T (test use only)
1 0 0	Auto-negotiate advertise 10BASE-T
1 0 1	Auto-negotiate advertise 10/100BASE-TX
1 1 0	Auto-negotiate advertise 10/100/1000BASE-T
1 1 1	Auto-negotiate advertise 1000BASE-T



I2BORG SPECIFIC
 Not convention-compliant, '=VESTA_' should be replaced with 'ENET_' (6 nets)

Vesta Ethernet PHY

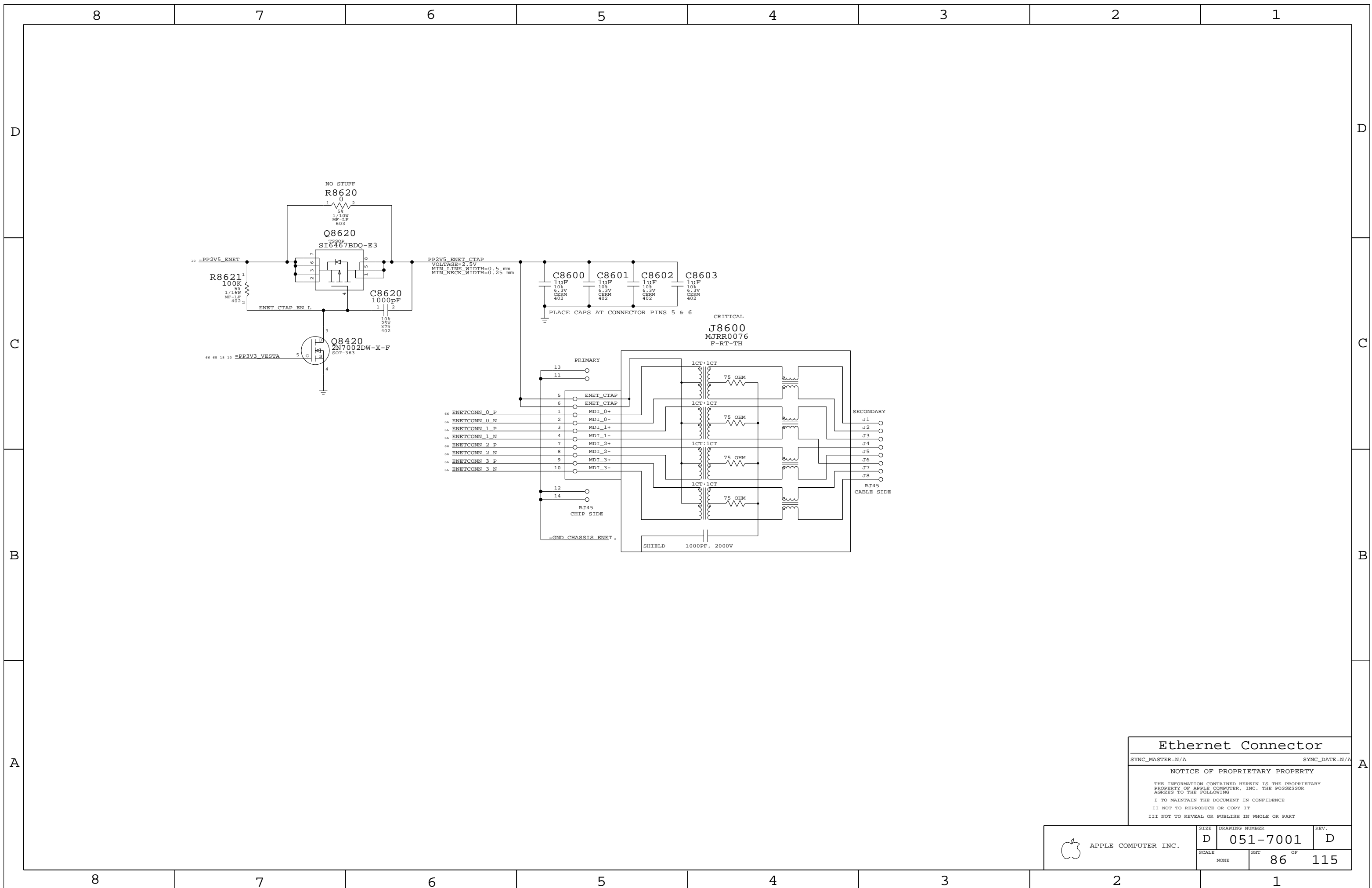
SYNC_MASTER=N/A SYNC_DATE=N/A

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Ethernet Connector

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	D	051-7001	D
SCALE	SHT	OF	REV.
NONE	86	115	

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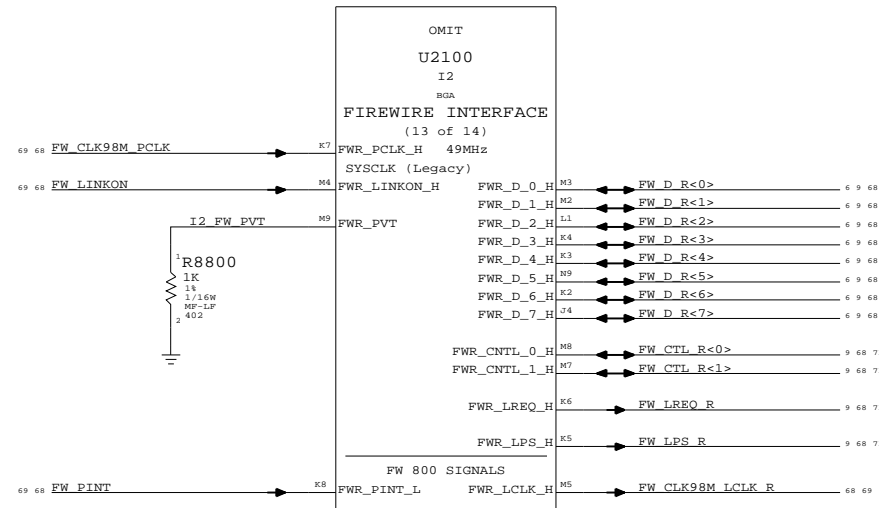
ELECTRICAL_CONSTRAINT_SET	NET_TYPE				
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
FW_D	FW	FW		FW D R<7..0>	6 9 68
FW_CTL	FW	FW		FW CTL R<1..0>	9 68 71
FW_LREQ	FW	FW		FW LREQ R	9 68 71
	FW	FW		FW LPS R	9 68 71
	FW	FW		FW LINKON	68 69
FW_PCLK	CLOCK	CLOCK		FW CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW CLK98M_LCLK R	68 69
FW_PINT	FW	FW		FW PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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	D	051-7001	D
SCALE	SHT OF		
NONE	88 OF		115

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED	FW	FW	FW_PORT1_TPA_P_FL
BY	FW	FW	FW_PORT1_TPA_N_FL
PHY	FW	FW	FW_PORT1_TPB_P_FL
PAGE	FW	FW	FW_PORT1_TPB_N_FL
	FW	FW	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_P_FL
	FW	FW	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
 - _PPFW_PORT1
 - _PPFW_PORT2
 - _PPFW_PORT3
 - _PP3V3_FW
 - _GND_CHASSIS_FW_PORT1
 - _GND_CHASSIS_FW_PORT2
 - _GND_CHASSIS_FW_PORT3

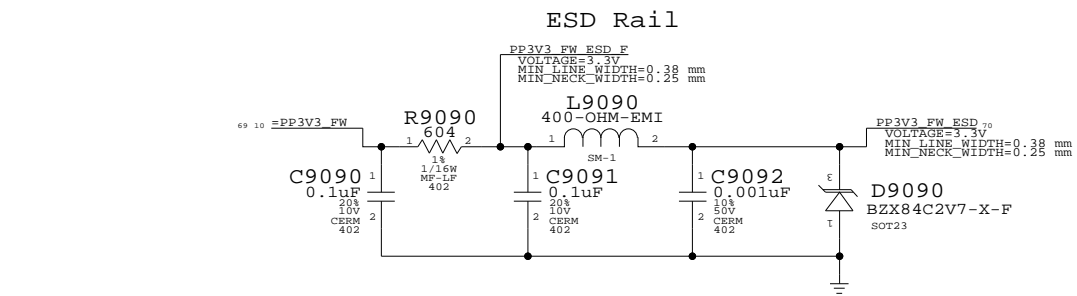
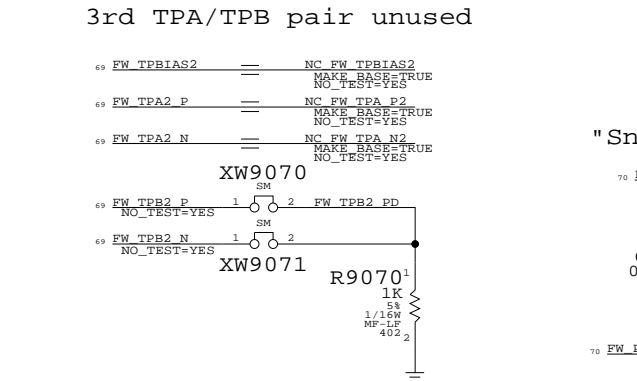
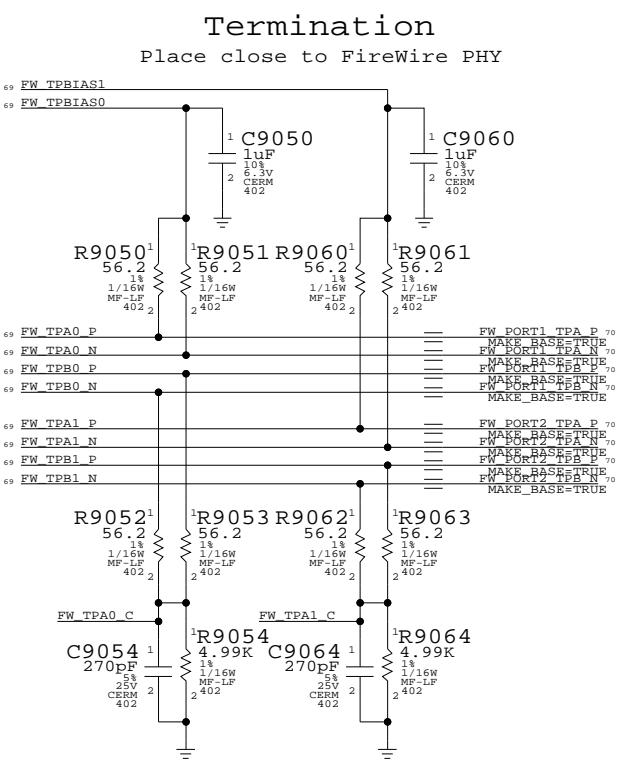
Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

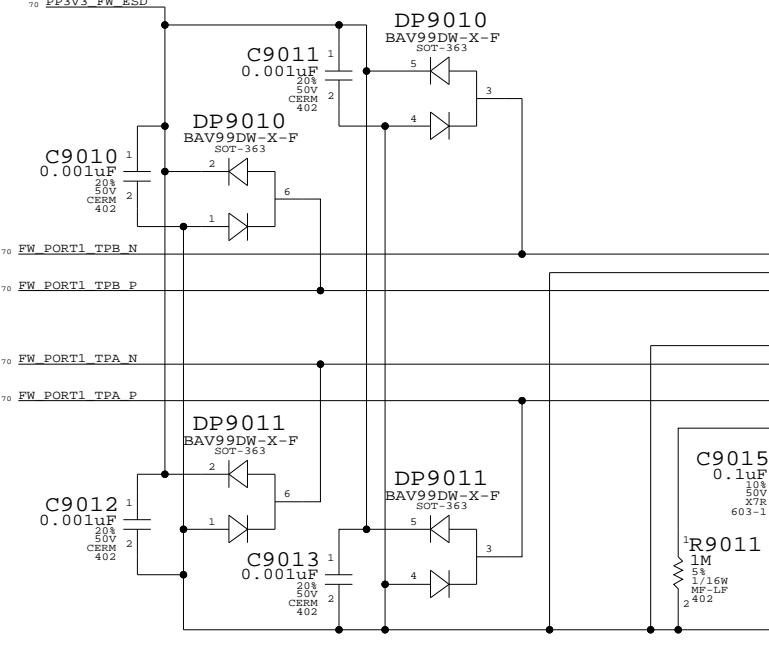
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

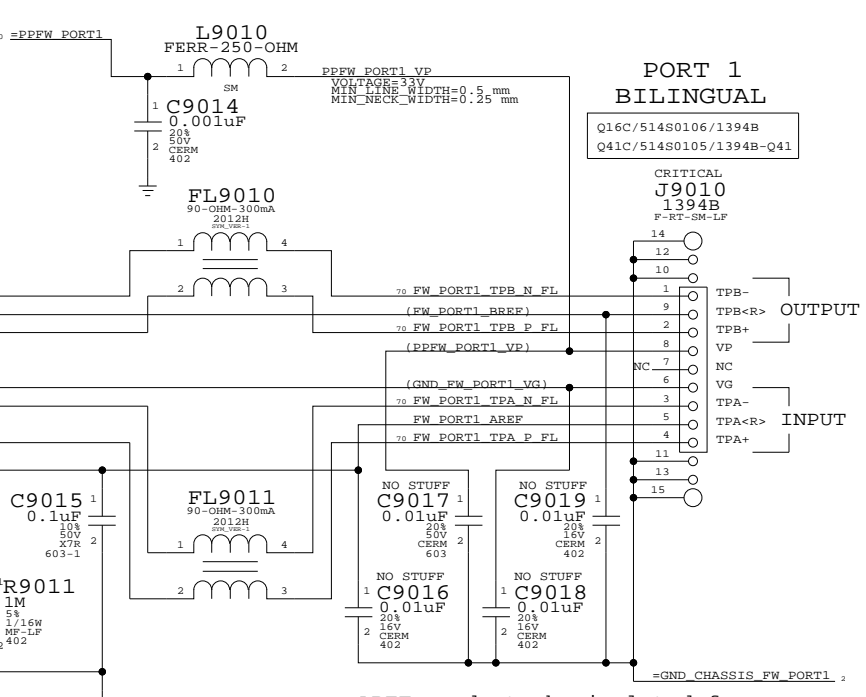
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



"Snapback" & "Late VG" Protection



Cable Power

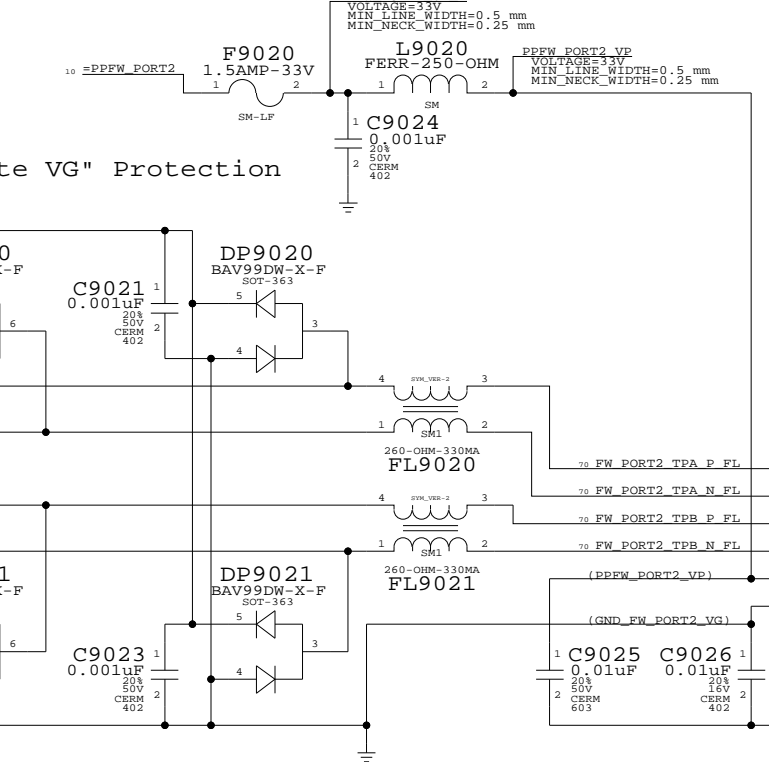


AREF needs to be isolated from all local grounds per 1394b spec

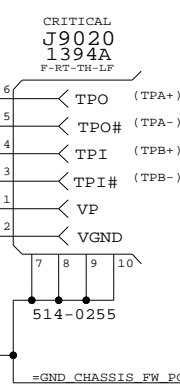
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Cable Power



PORT 2 1394A



FireWire Ports

SYNC_MASTER=N/A SYNC_DATE=N/A

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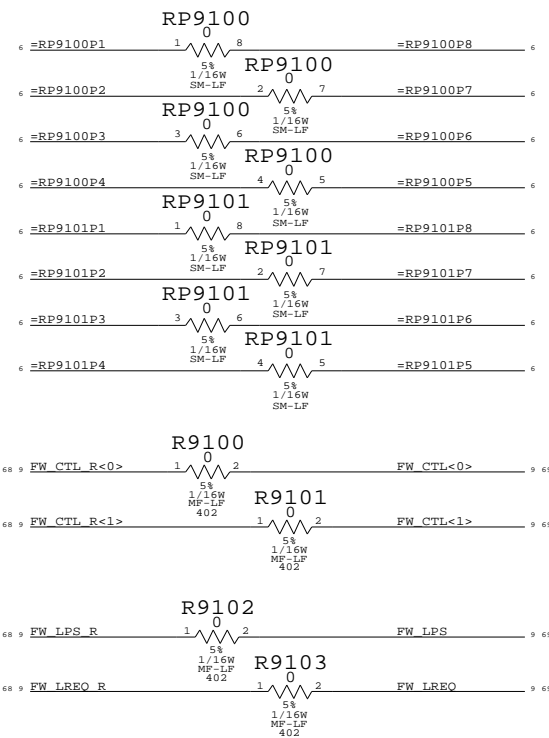
B

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Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.)



FireWire Series Term

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-7001	D
SCALE	SHT	OF
NONE	91	115

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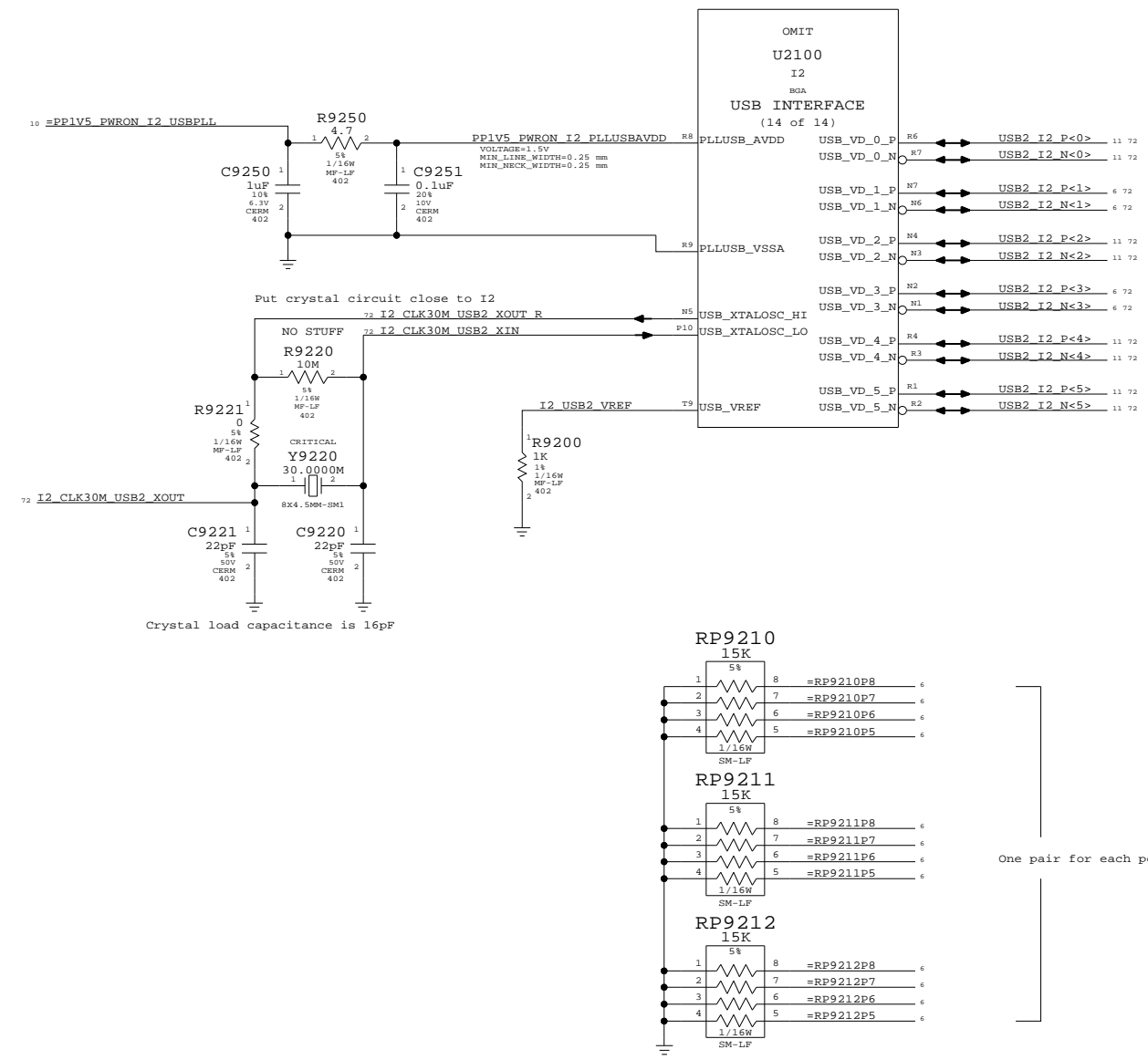
1

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2 P<0>
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2 N<0>
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2 P<1>
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2 N<1>
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2 P<2>
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2 N<2>
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2 P<3>
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2 N<3>
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2 P<4>
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2 N<4>
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2 P<5>
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2 N<5>
USB2_I2_XTAL	XTAL	XTAL		I2_CLK30M_USB2_XOUT_R
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XOUT
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XIN

Page Notes

Power aliases required by this page:
 - =PP3V3_PWRON_USB
 Signal aliases required by this page:
 - =RP92xxPy (pinswappable USB pulldowns)
 BOM options provided by this page:
 (NONE)

Net Spacing Type: USB2
 Line To Line: 19.5 mils
 Length Tolerance: 50 mils
 Primary Max Sep: 7.5 mils
 Secondary Max Sep: 100 mils
 Secondary Length: 500 mils
 NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



One pair for each port USB2_*<0..5>

I2 USB Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE	SHT	OF	
NONE	92	115	

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
E30	USB2	USB2	USB2_NEC_0
E31	USB2	USB2	USB2_NEC_0
E32	USB2	USB2	USB2_NEC_1
E33	USB2	USB2	USB2_NEC_1
E34	USB2	USB2	USB2_NEC_2
E35	USB2	USB2	USB2_NEC_2
E36	USB2	USB2	USB2_NEC_3
E37	USB2	USB2	USB2_NEC_3

PROVIDED BY 12 PAGES

E40	USB2_NEC_XTAL	XTAL	XTAL	NEC_CLK30M_XT1
E41		XTAL	XTAL	NEC_CLK30M_XT2
E42		XTAL	XTAL	NEC_CLK30M_XT2_R

Page Notes

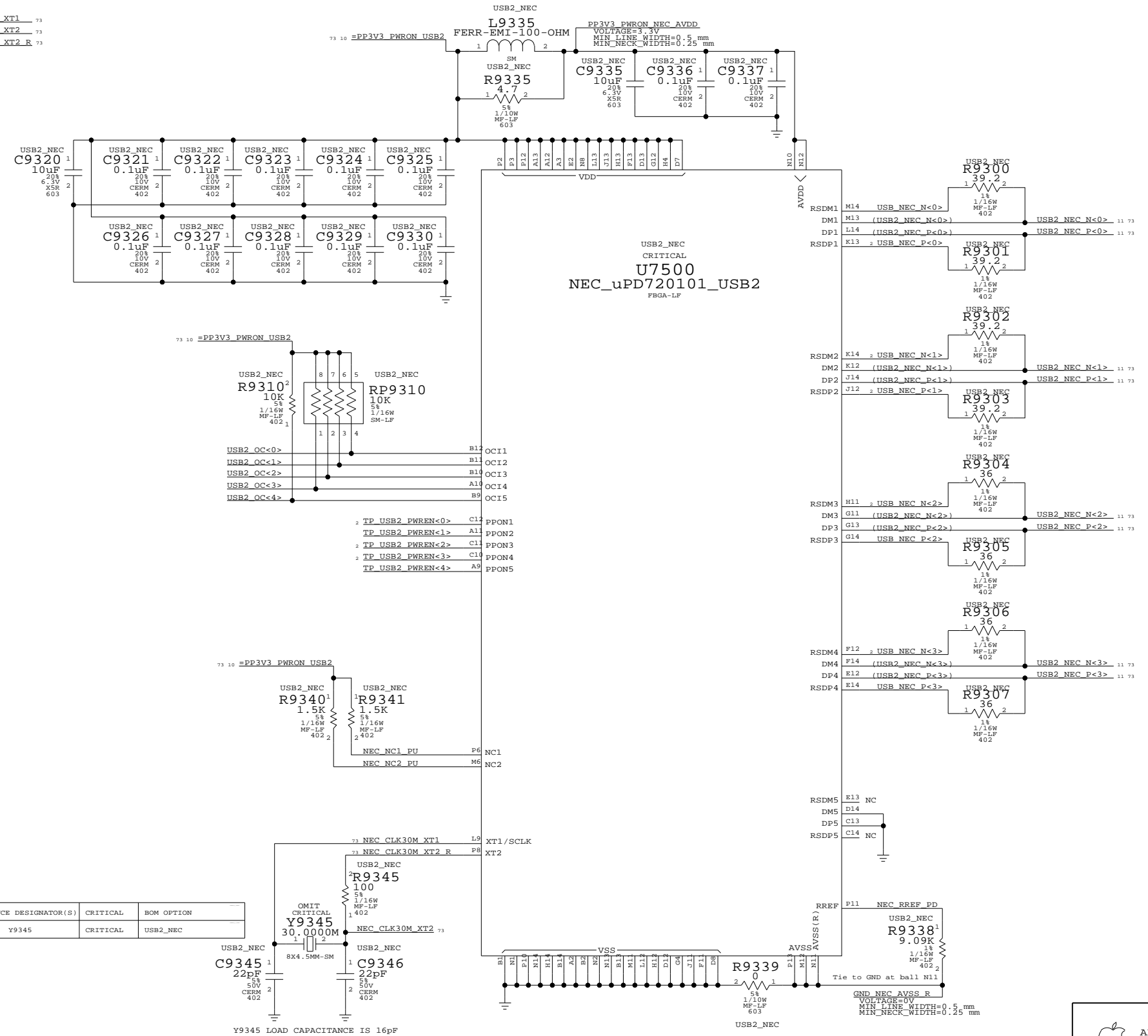
Power aliases required by this page:
 - =PP3V3_PWRON_USB2

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
19750087	1	XTAL_CER_30.000MHZ_1W_PROF_8X4.5MM_SMD	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7001	D
SCALE	NONE	SHT OF	REV.
		93	115

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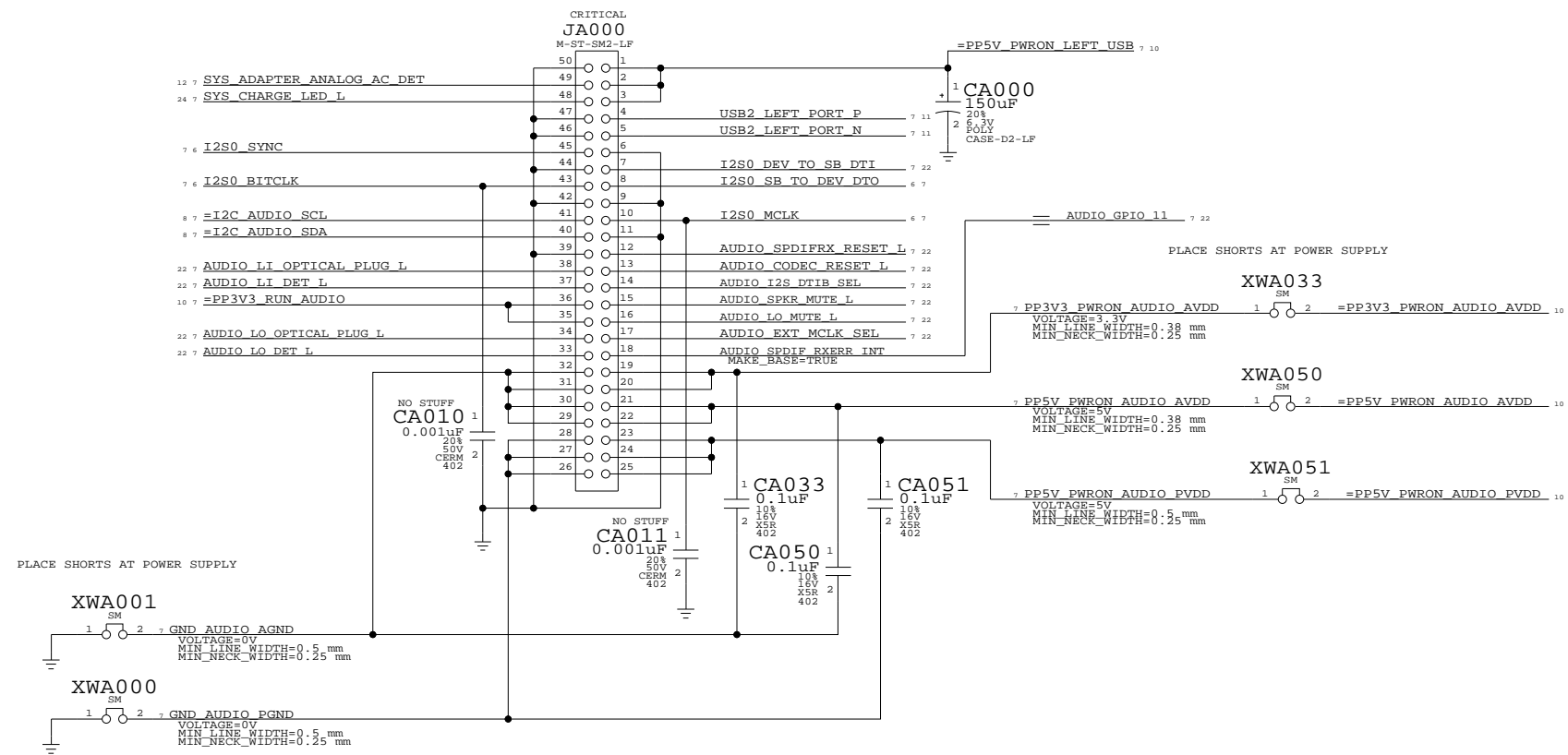
B

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A

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AUDIO BOARD & LEFT I/O



Audio Board Connector

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	D	051-7001	D
SCALE	NONE	SHT OF	100 OF 115

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C								
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	8	7	6	5	4	3	2	1

TABLE_SPACING_RULE								
TABLE_SPACING_RULE	DVO	151	*	0.15 MM	-STANDARD	-STANDARD	-STANDARD	-STANDARD
TABLE_PHYSICAL_RULE	DVO							
TABLE_PHYSICAL_RULE	DVO		*		=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	TV	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	TV_CONN	151	*	-TV	-TV	-TV	-TV	-TV
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	TV		*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_PHYSICAL_RULE	TV_CONN		*	-TV	-TV	-TV	-TV	-TV
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE	VGA_CONN	151	*	-VGA	-VGA	-VGA	-VGA	-VGA
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	VGA		*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_PHYSICAL_RULE	VGA_CONN		*	-VGA	-VGA	-VGA	-VGA	-VGA
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	LVDS	151	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	LVDS		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	TMDS	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE	TMDS_CONN		*	=TMDS	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	TMDS		*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE	TMDS_CONN		*	=TMDS	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_SPACING_RULE								
TABLE_SPACING_RULE	THERM	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE								
TABLE_PHYSICAL_RULE	THERM		*	Y	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

DVO

S-VIDEO

VGA

LVDS

TMDS

THERM

Spacing & Physical Constraints 2

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
NONE	111	115	

