

IM4, 2 - REV B

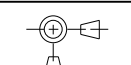
09/11/06

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
B		461143	PRODUCTION RELEASED	09/12/06	06/22/04

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19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
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21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
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24	24	SB: 4 OF 4	M38	01/05/2006	
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector	AMASTER	MASTER	
29	29	DDR2 SO-DIMM Connector	BMASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
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33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
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PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	05/12/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006	
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUM	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX : _____		DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX : _____		ENG APPD	MFG APPD		
X.XXX : _____		QA APPD	DESIGNER		
ANGLES : _____		RELEASE	SCALE		
DO NOT SCALE DRAWING			NONE	TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	DRAWING NUMBER 051-7032
				REV. B	SHT 1 OF 97

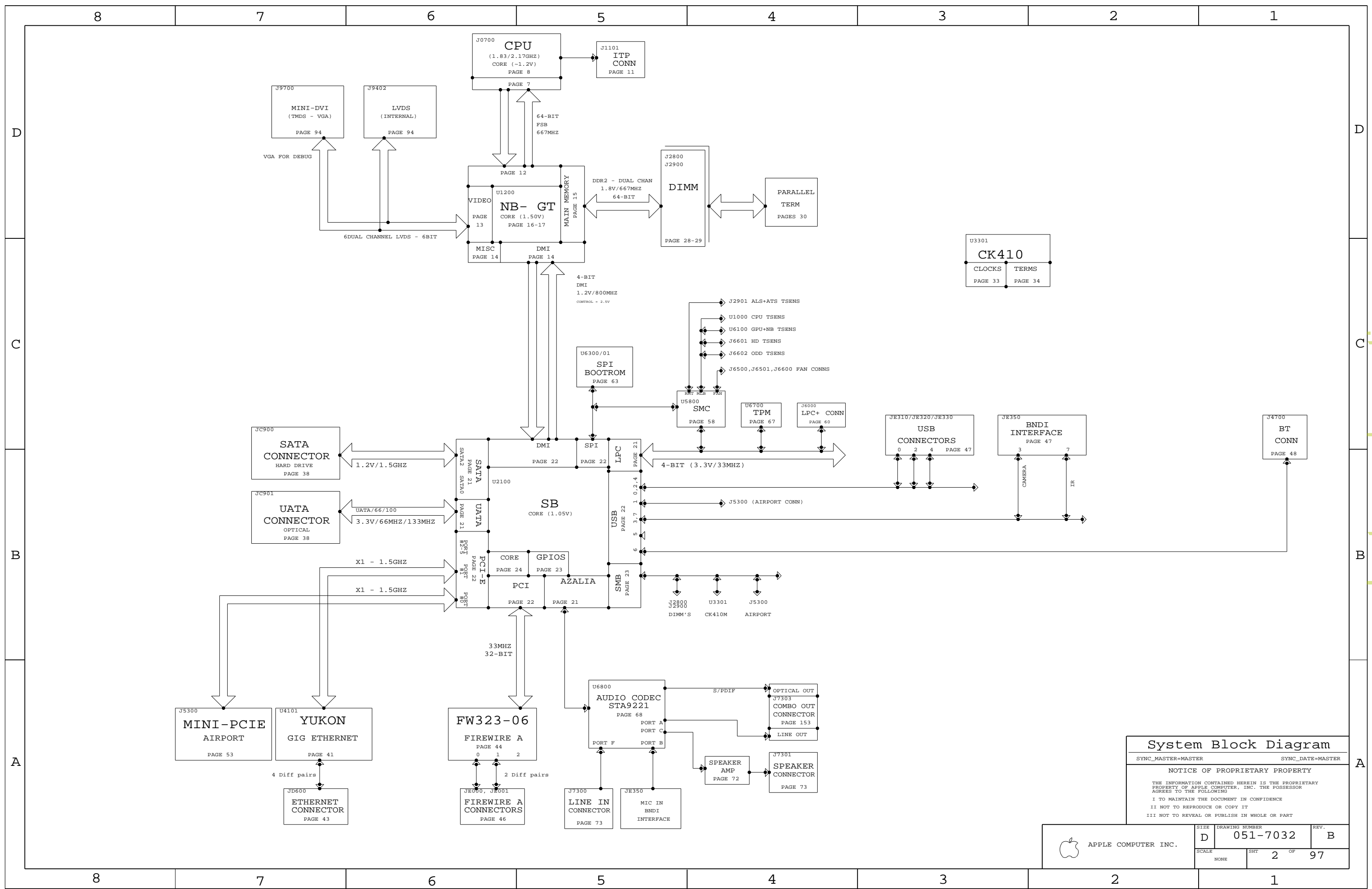
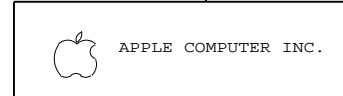
System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

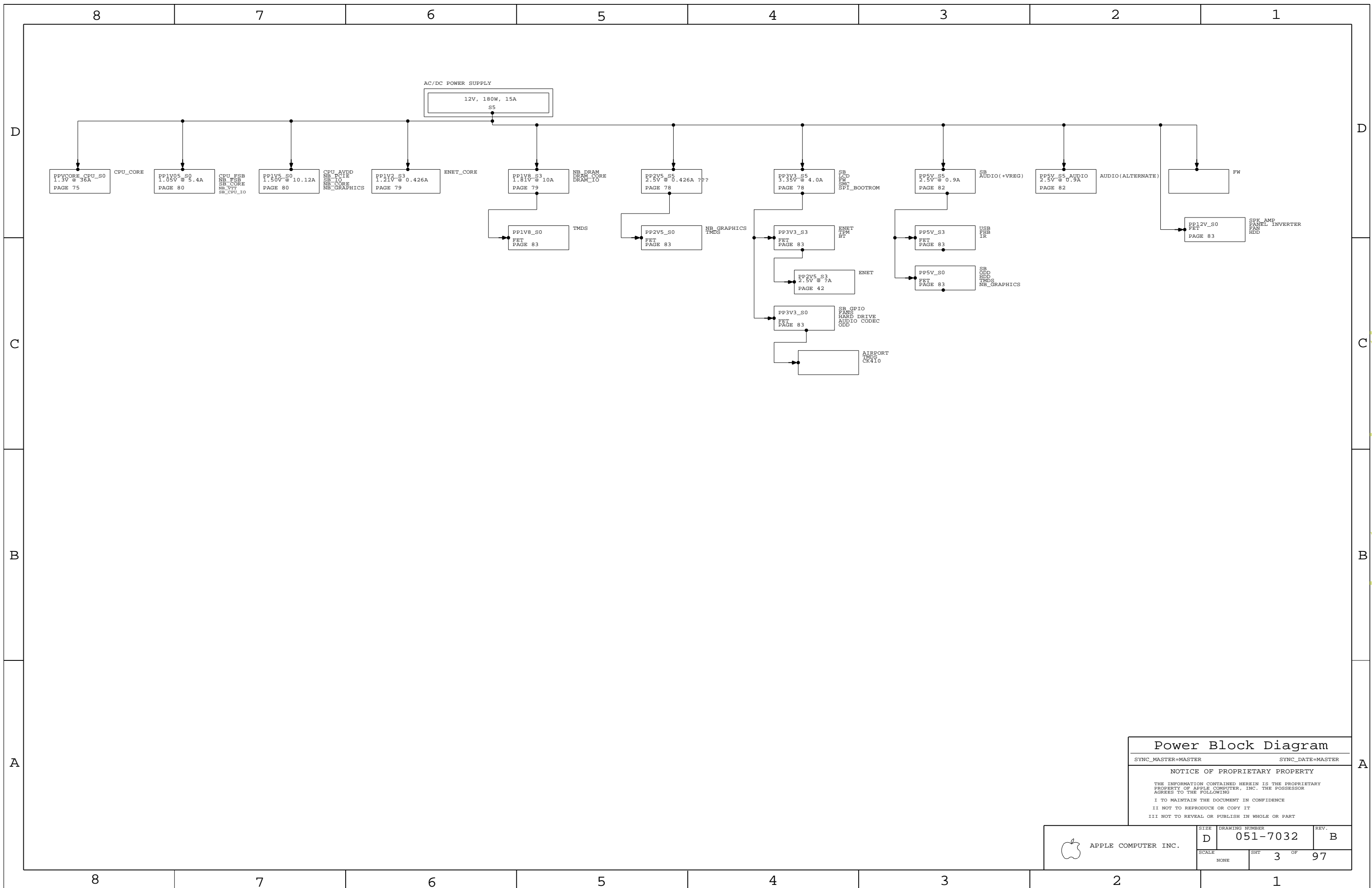
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NONE	2	97



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Power Block Diagram
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NONE	3	97	

8

7

6

5

4

3

2

1

COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFN	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	LEMENU
353S1465	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7032	1	PCB,SCHM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0021	1	EFI ROM,M50	U6301	CRITICAL	
337S3242	1	M38 CPU (C0)	CPU	CRITICAL	YONAH_1_83

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1235	353S1465		U7500	CPU VREG, NON-SCREENED PART

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50	[EEE:XOM]	CRITICAL	YONAH_1_83

Table Items

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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

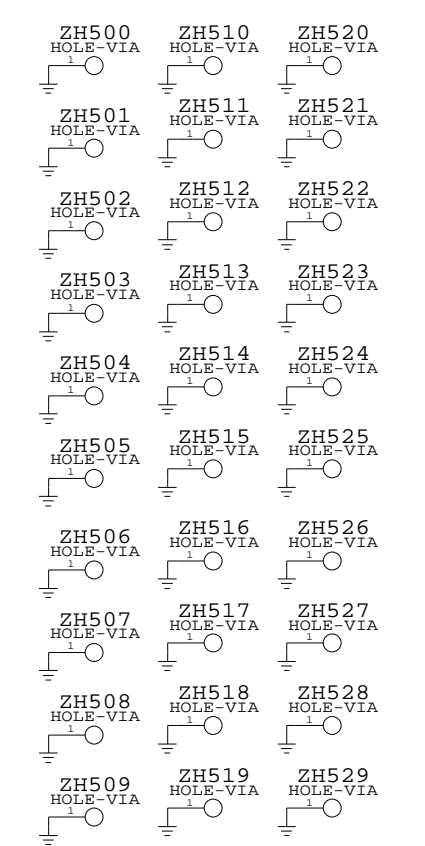
LAYOUT NOTE: PLACE NEAR U4100

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

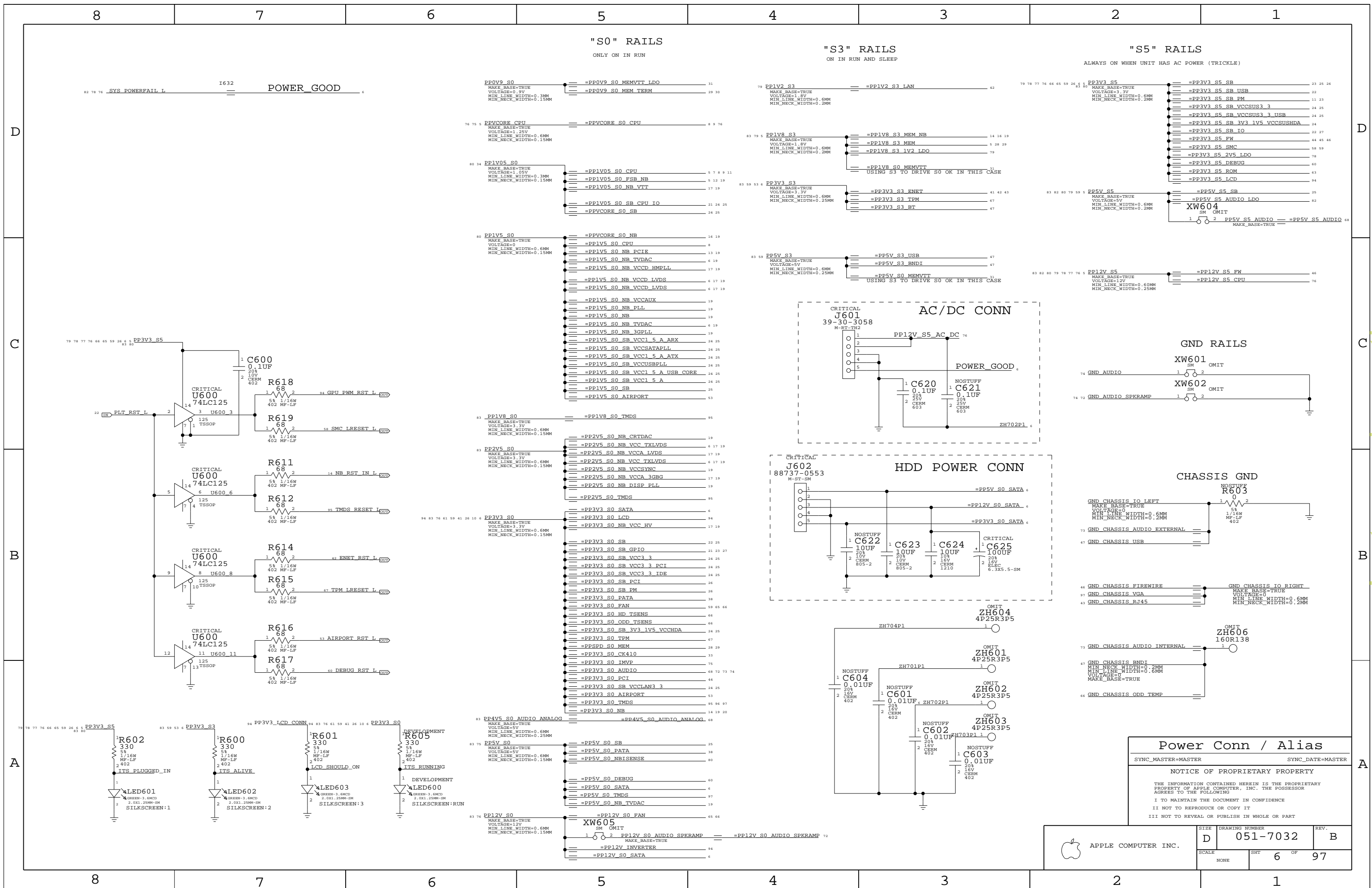
MISC GROUND VIAS



THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

FUNC TEST 1 OF 2
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"S0" RAILS

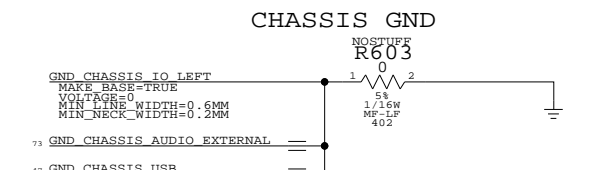
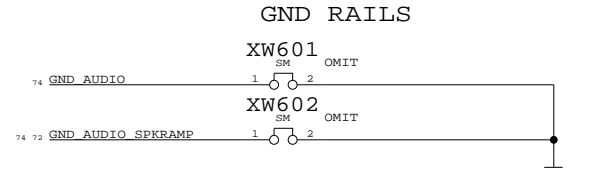
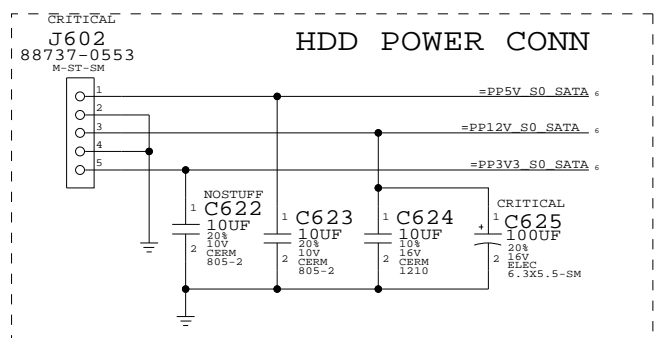
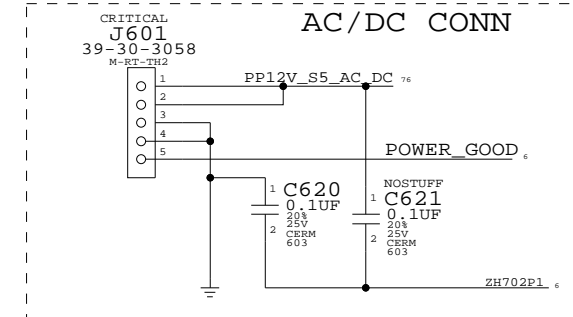
ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



Power Conn / Alias

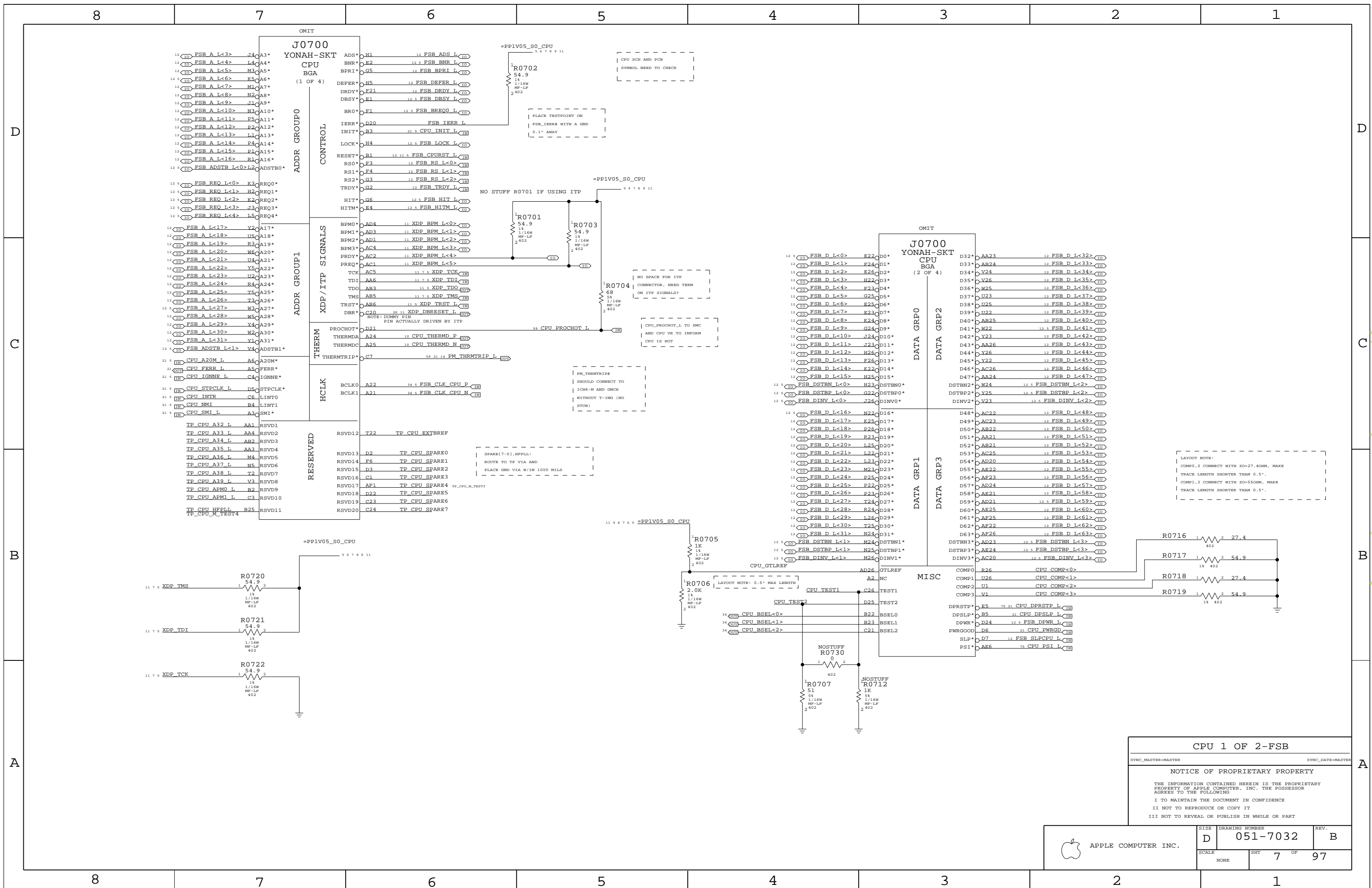
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NONE	6	97	

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CPU 1 OF 2-FSB

SYNC_MASTER-MASTER SYNC_DATE-MASTER

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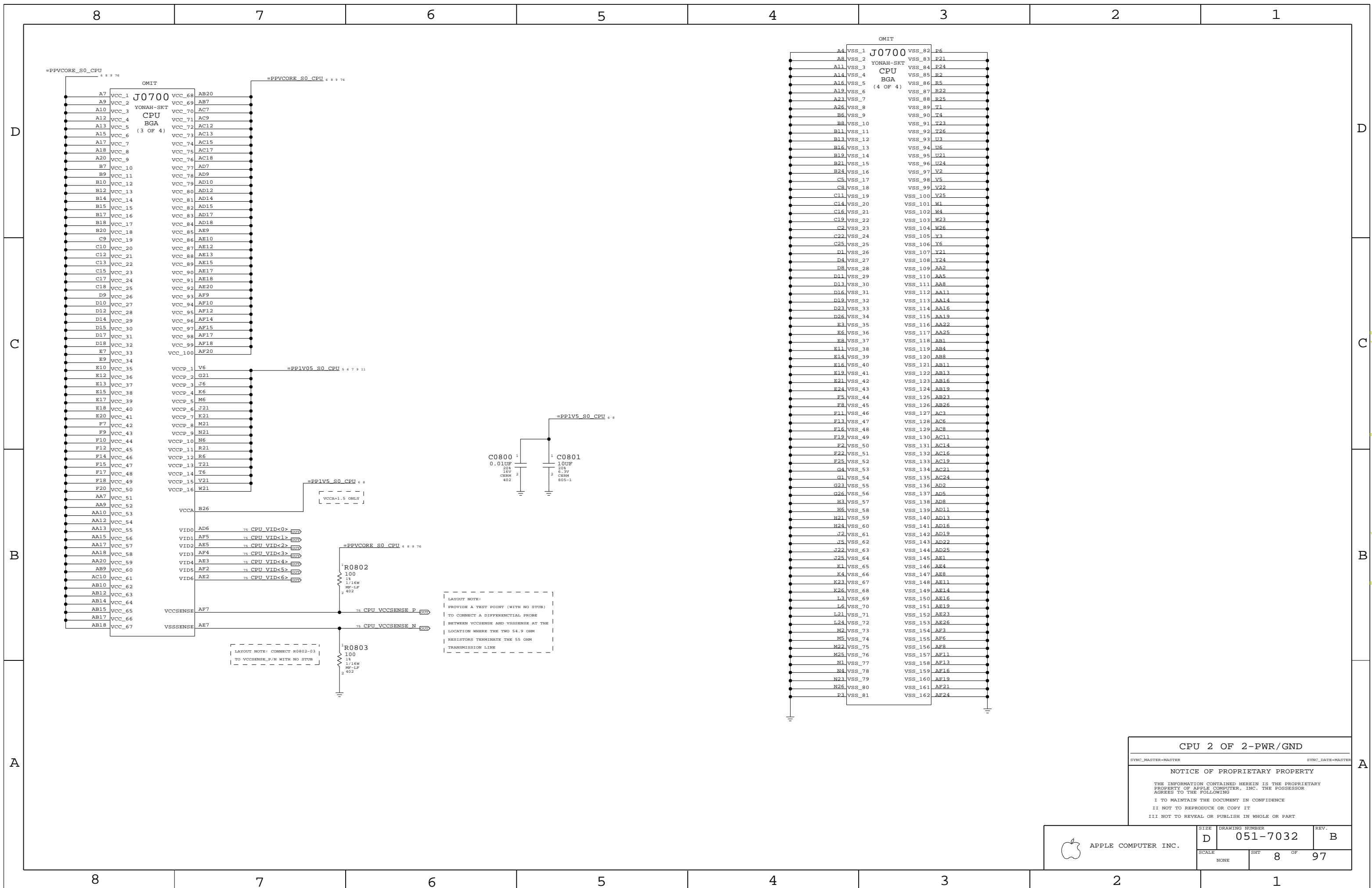
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	SCALE NONE	SHEET 7 OF 97	

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CPU 2 OF 2-PWR/GND

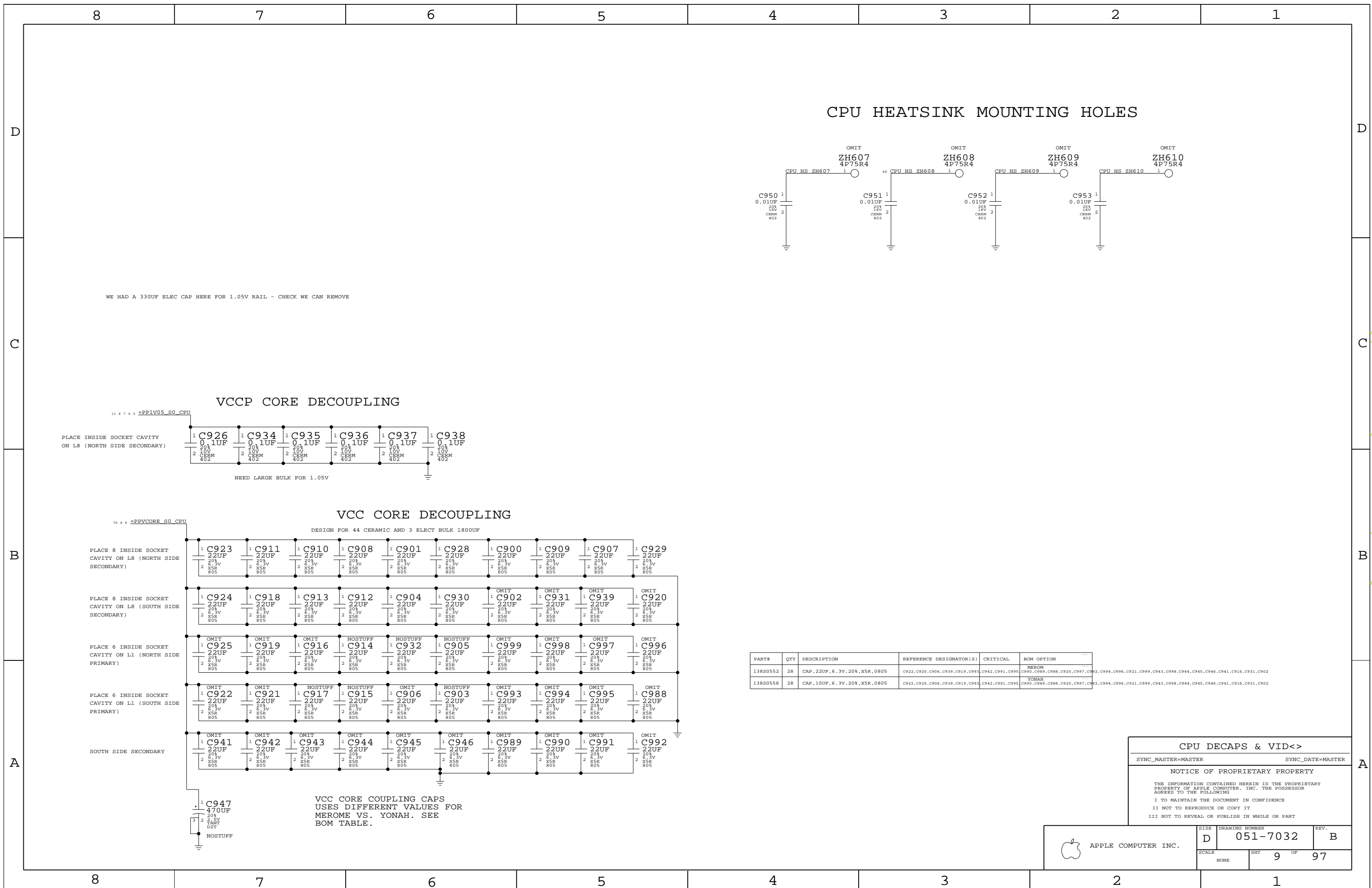
SYNC_MASTER-MASTER SYNC_DATE-MASTER

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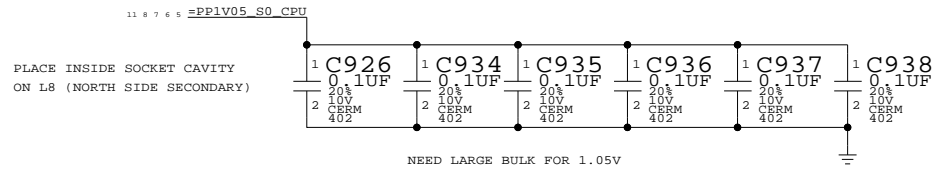
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NONE	8	97	



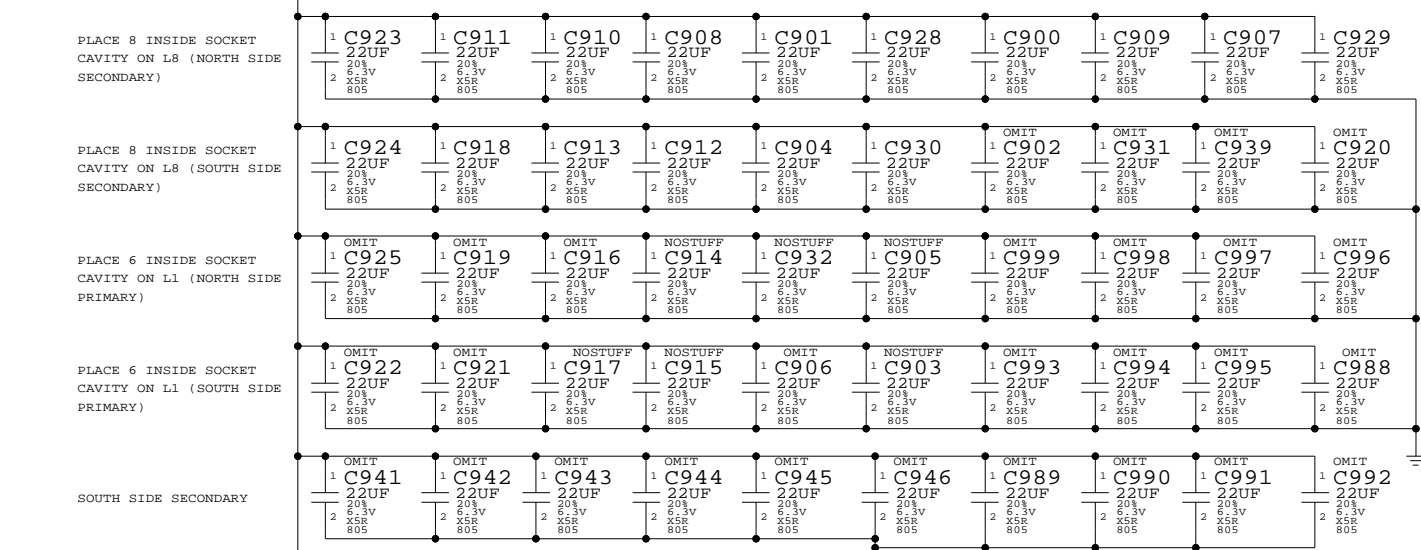
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING



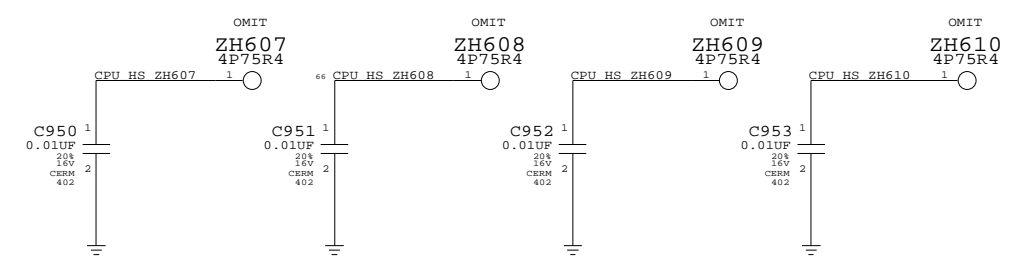
VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



VCC CORE COUPLING CAPS USES DIFFERENT VALUES FOR MEROME VS. YONAH. SEE BOM TABLE.

CPU HEATSINK MOUNTING HOLES



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

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SCALE NONE SHEET 9 OF 97

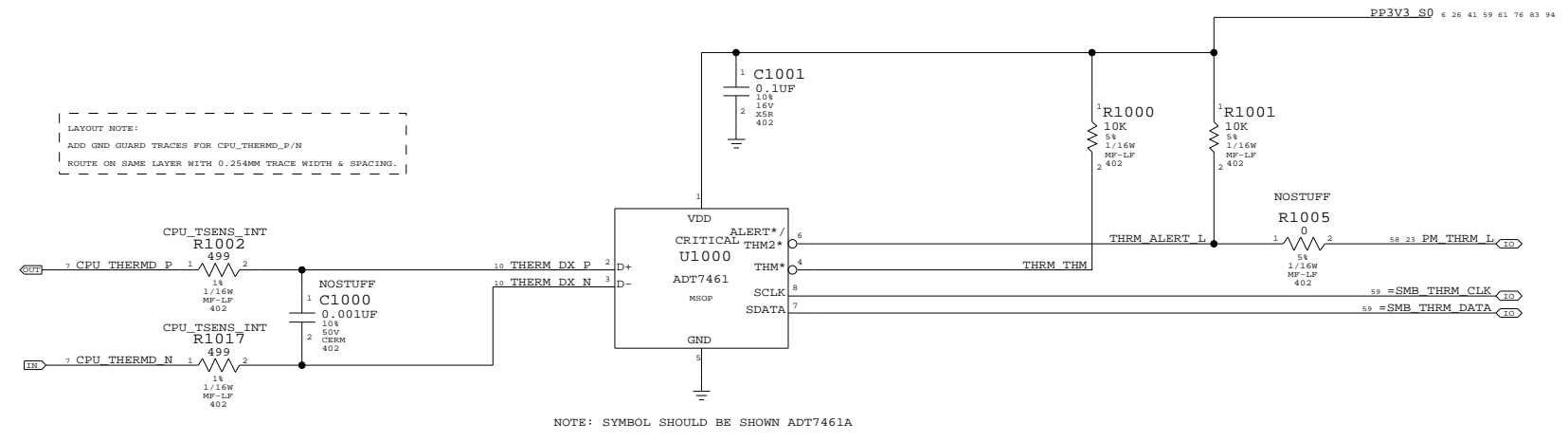
DRAWING NUMBER 051-7032

REV. B

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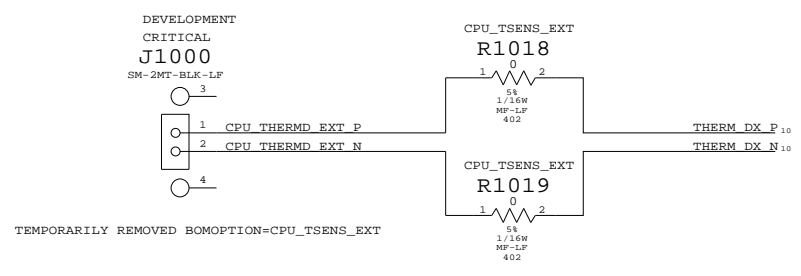
CPU THERMAL SENSOR

NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5



LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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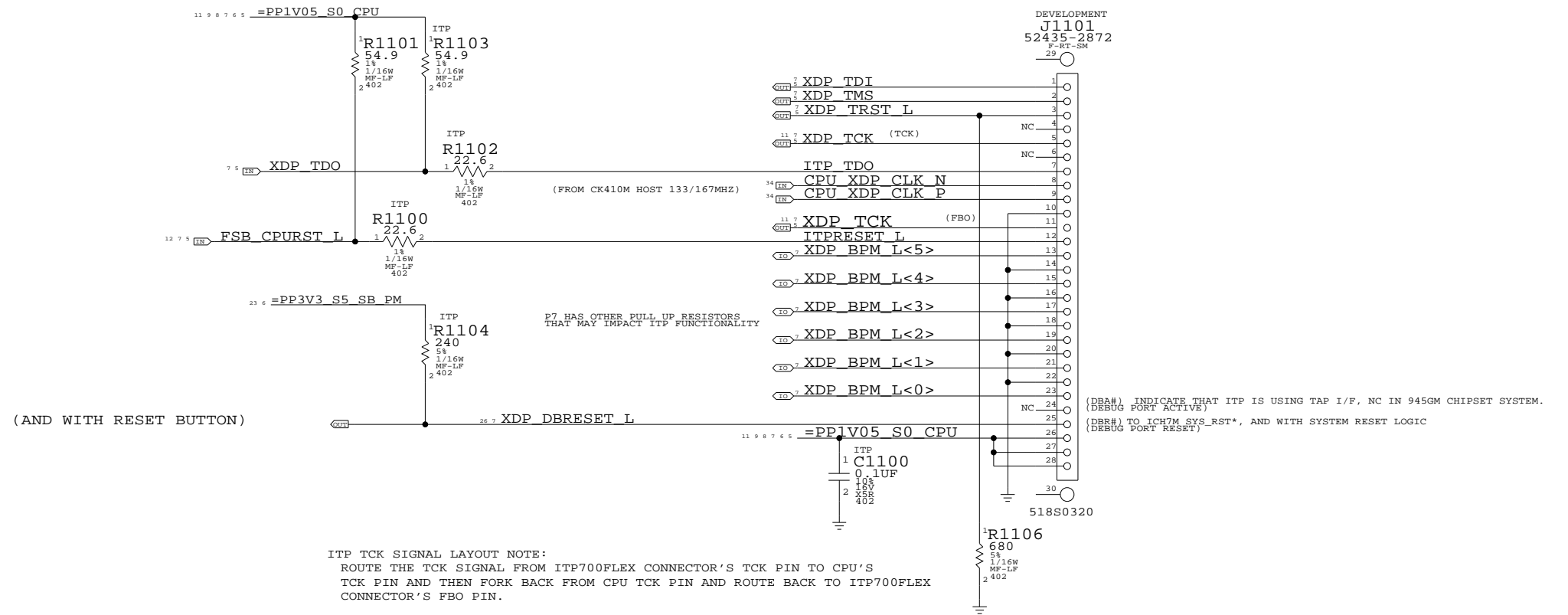
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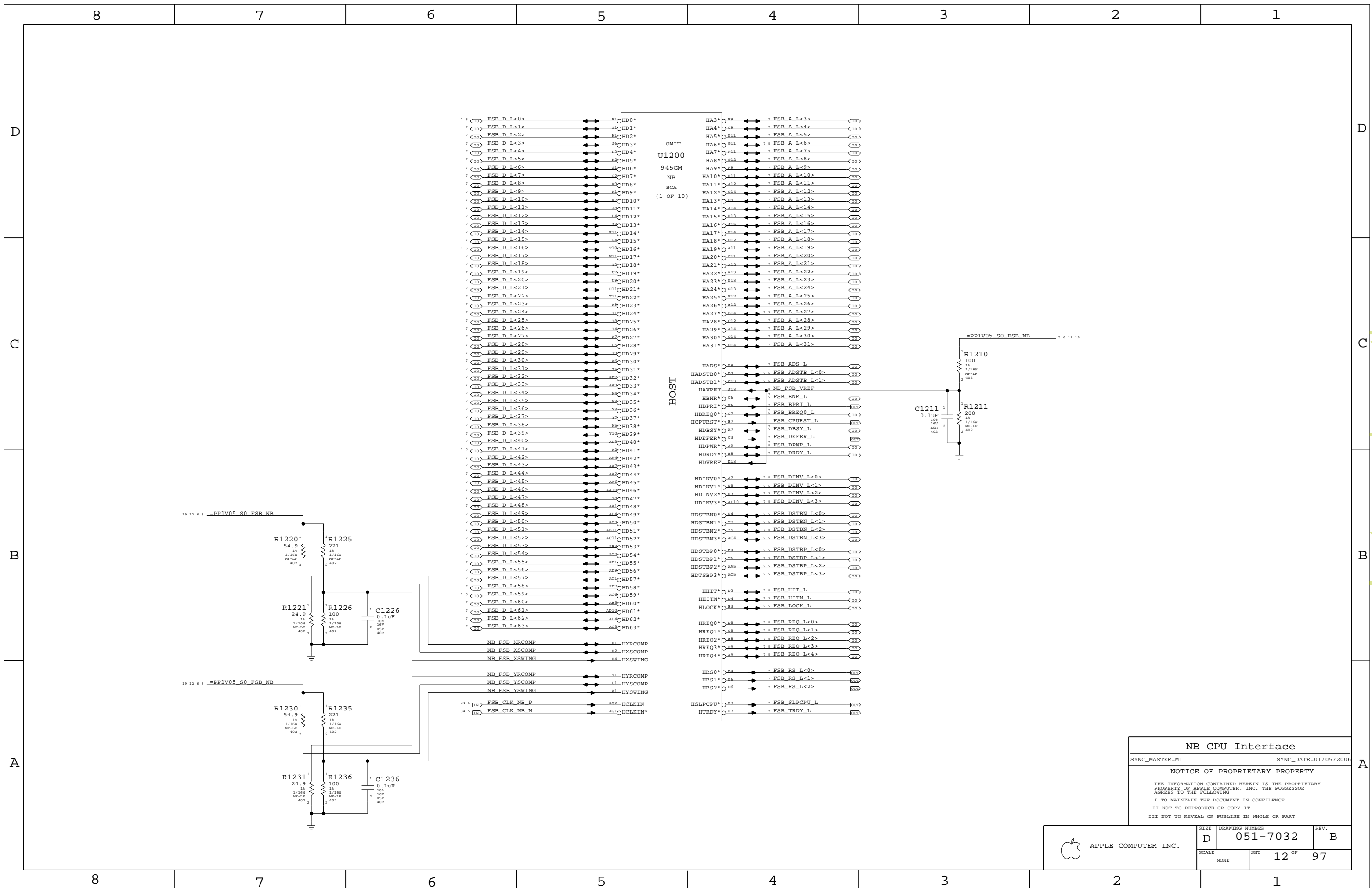
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
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NONE			

CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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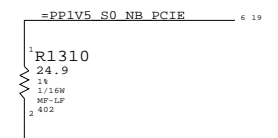
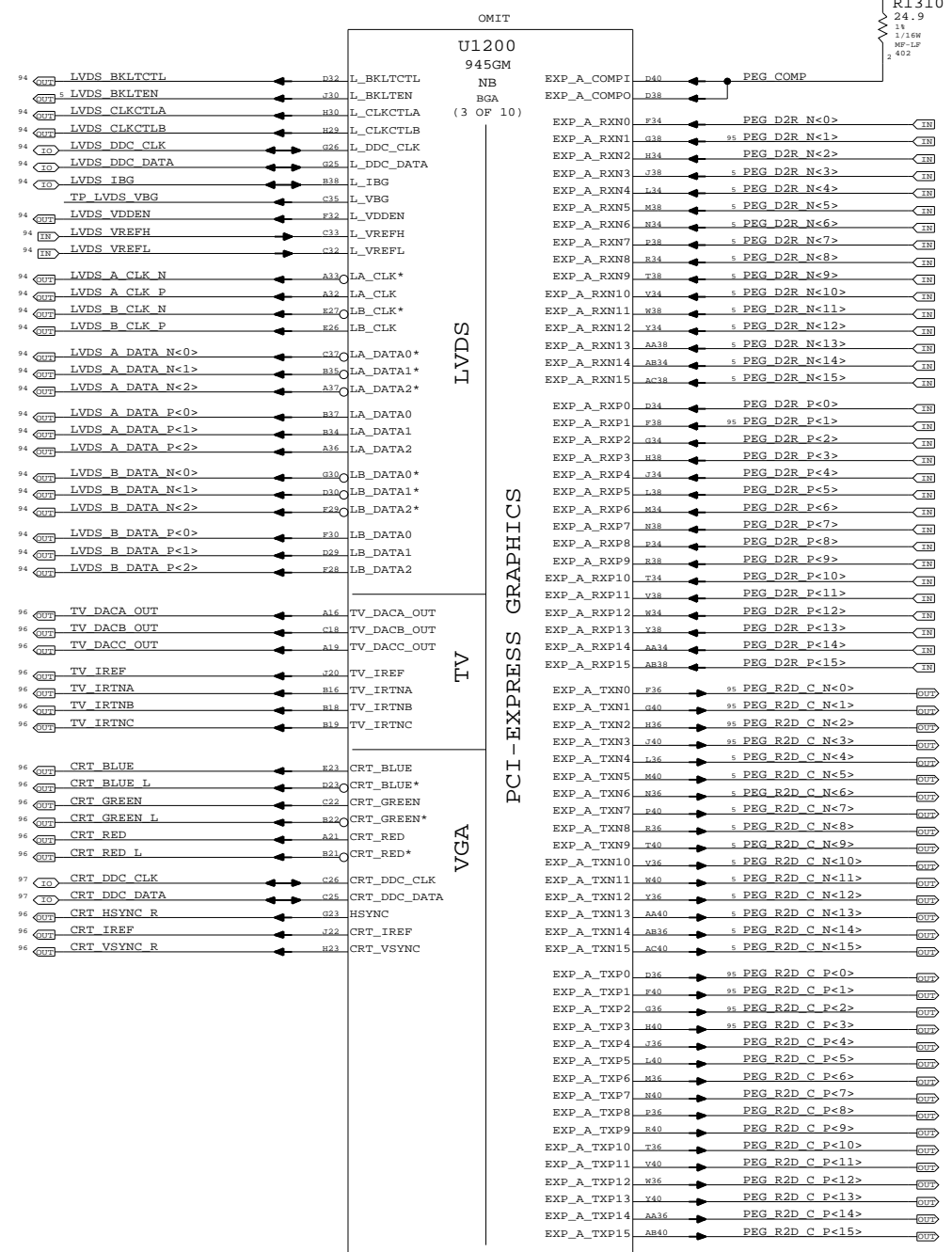
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

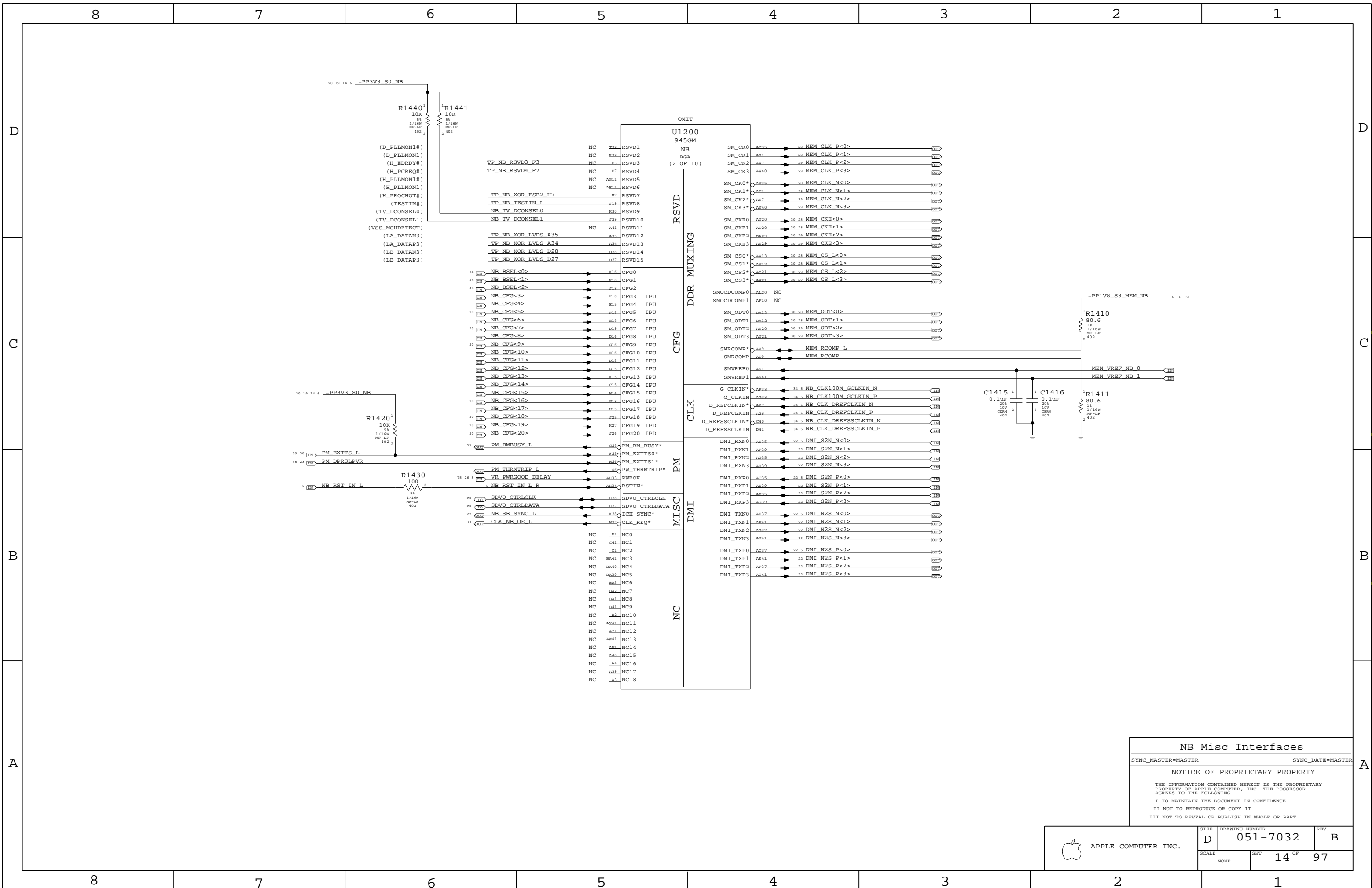
SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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SCALE	SHT	13 OF 97	
NONE			



NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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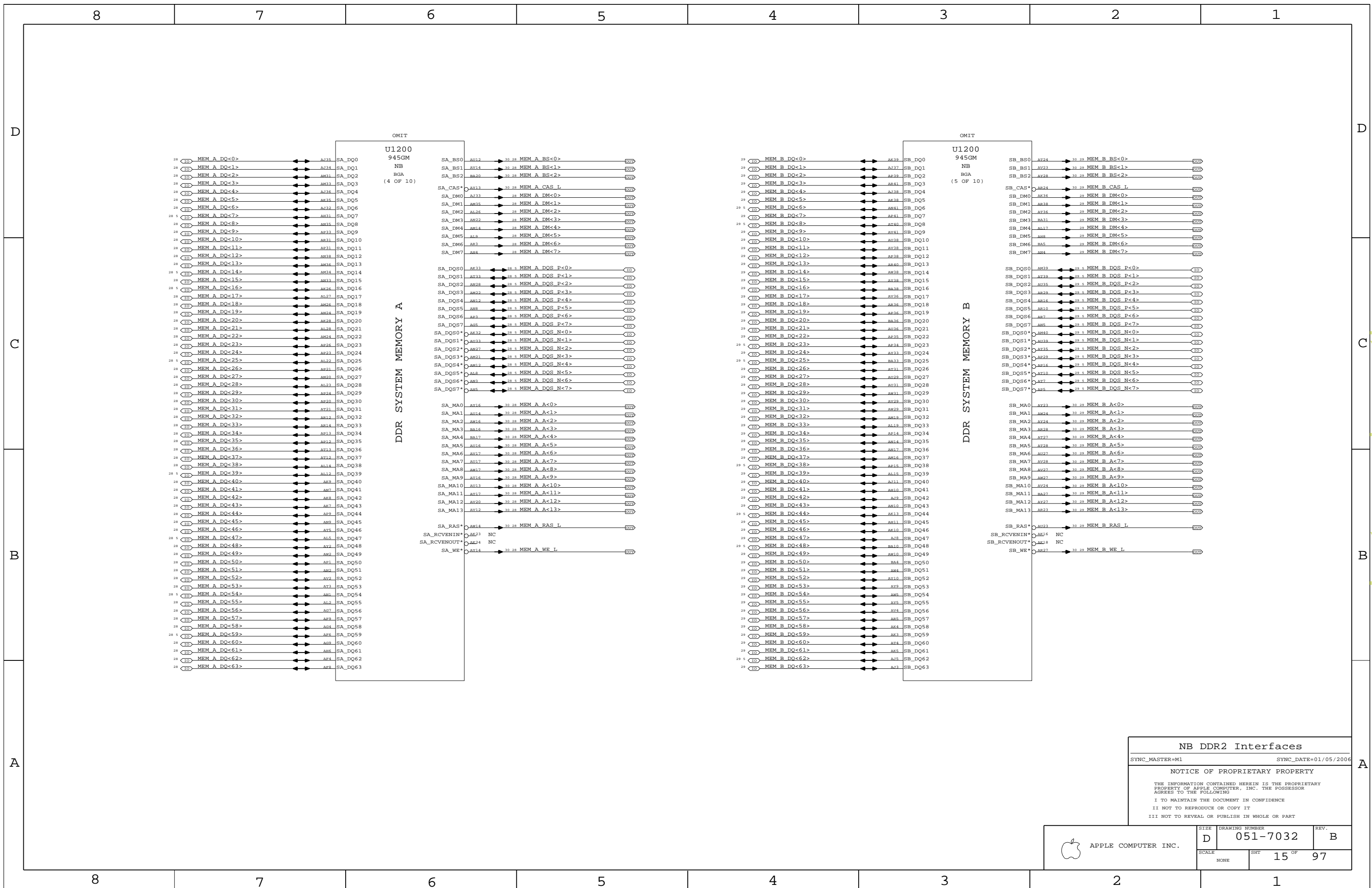
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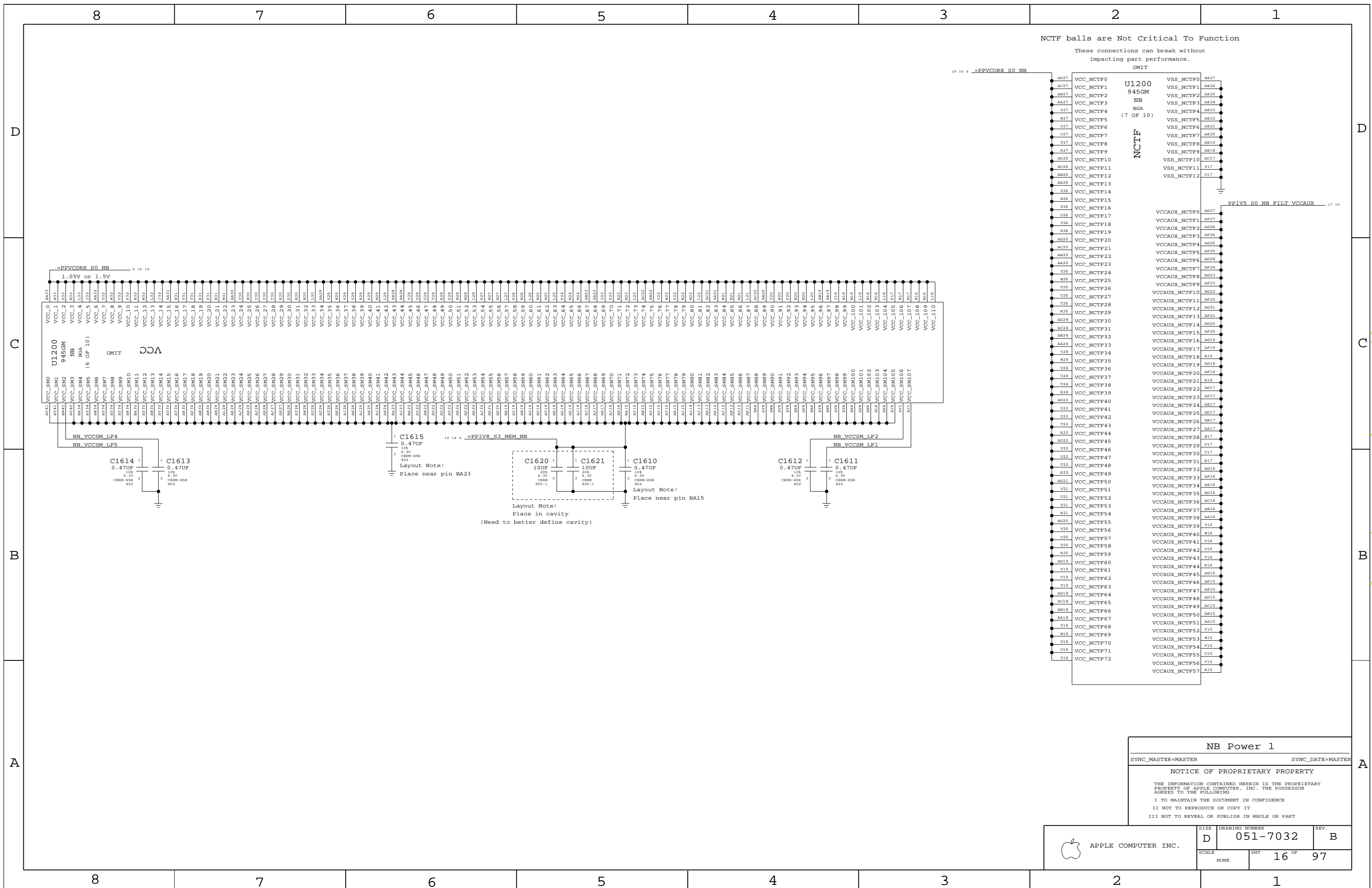
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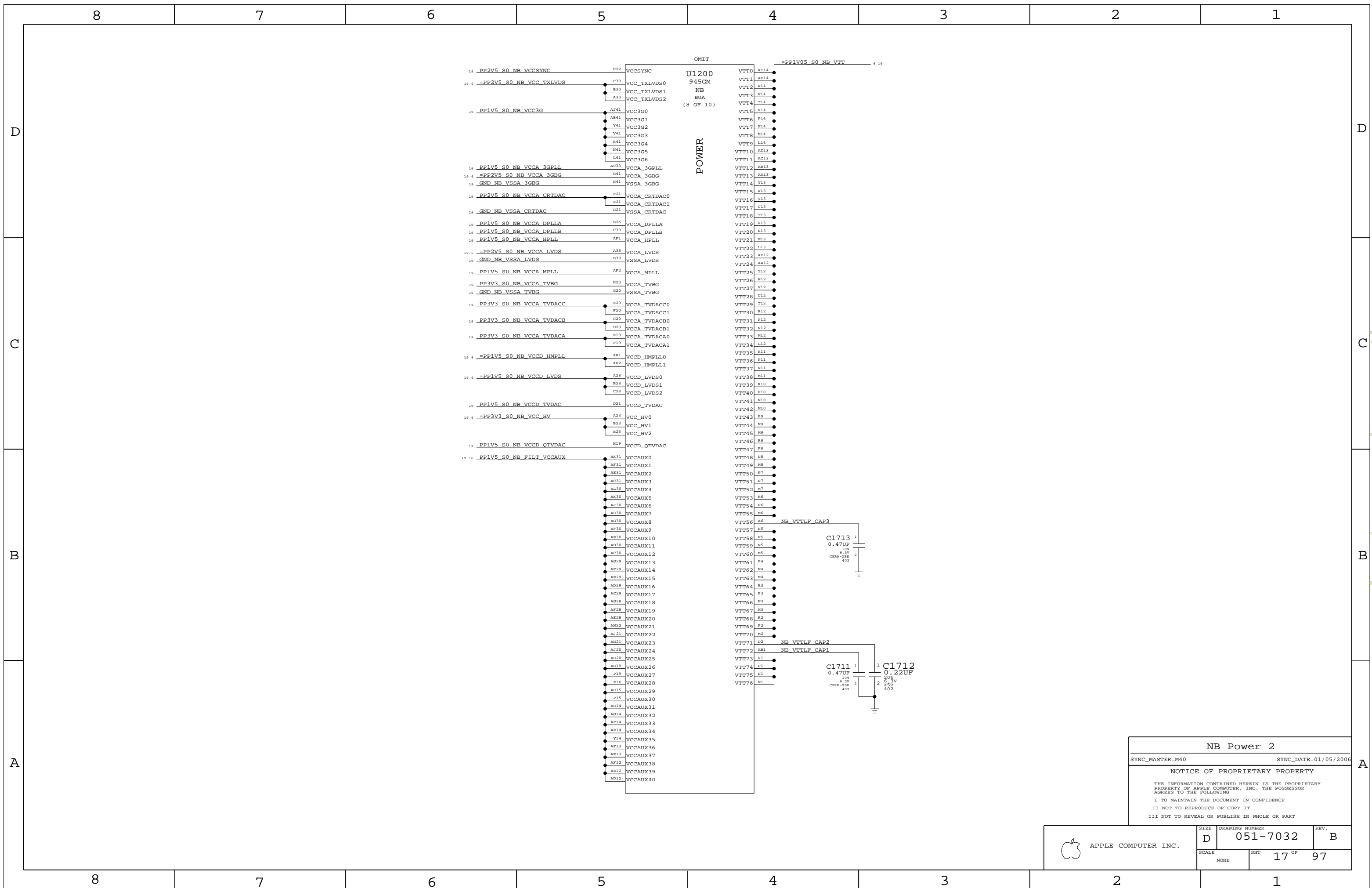
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEETS 14 OF 97	



NB DDR2 Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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	DRAWING NUMBER		REV.
	D	051-7032	B
SCALE		SHT	REV.
NONE		15 OF	97





NB Power 2

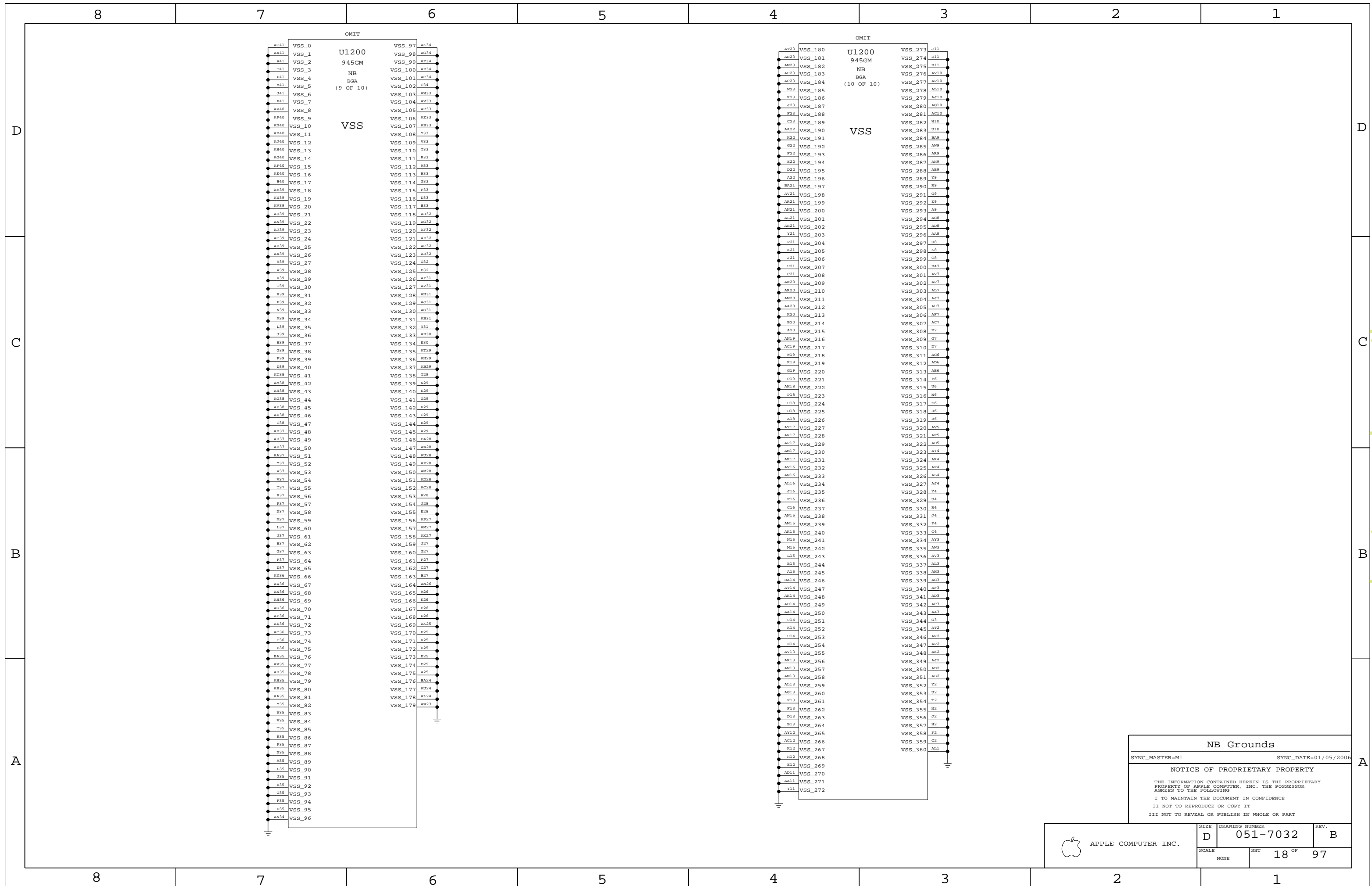
SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 17 OF 97	



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NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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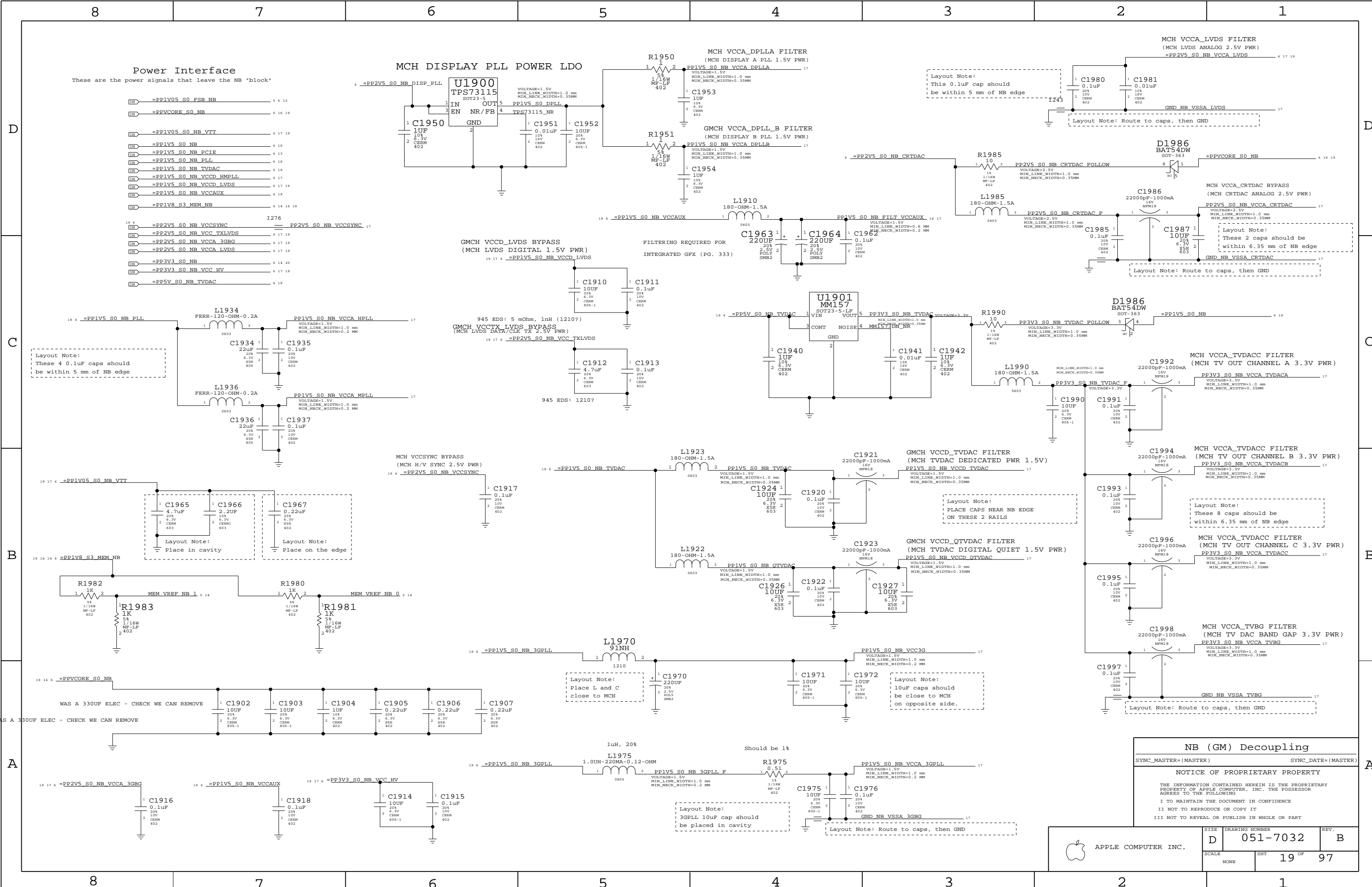
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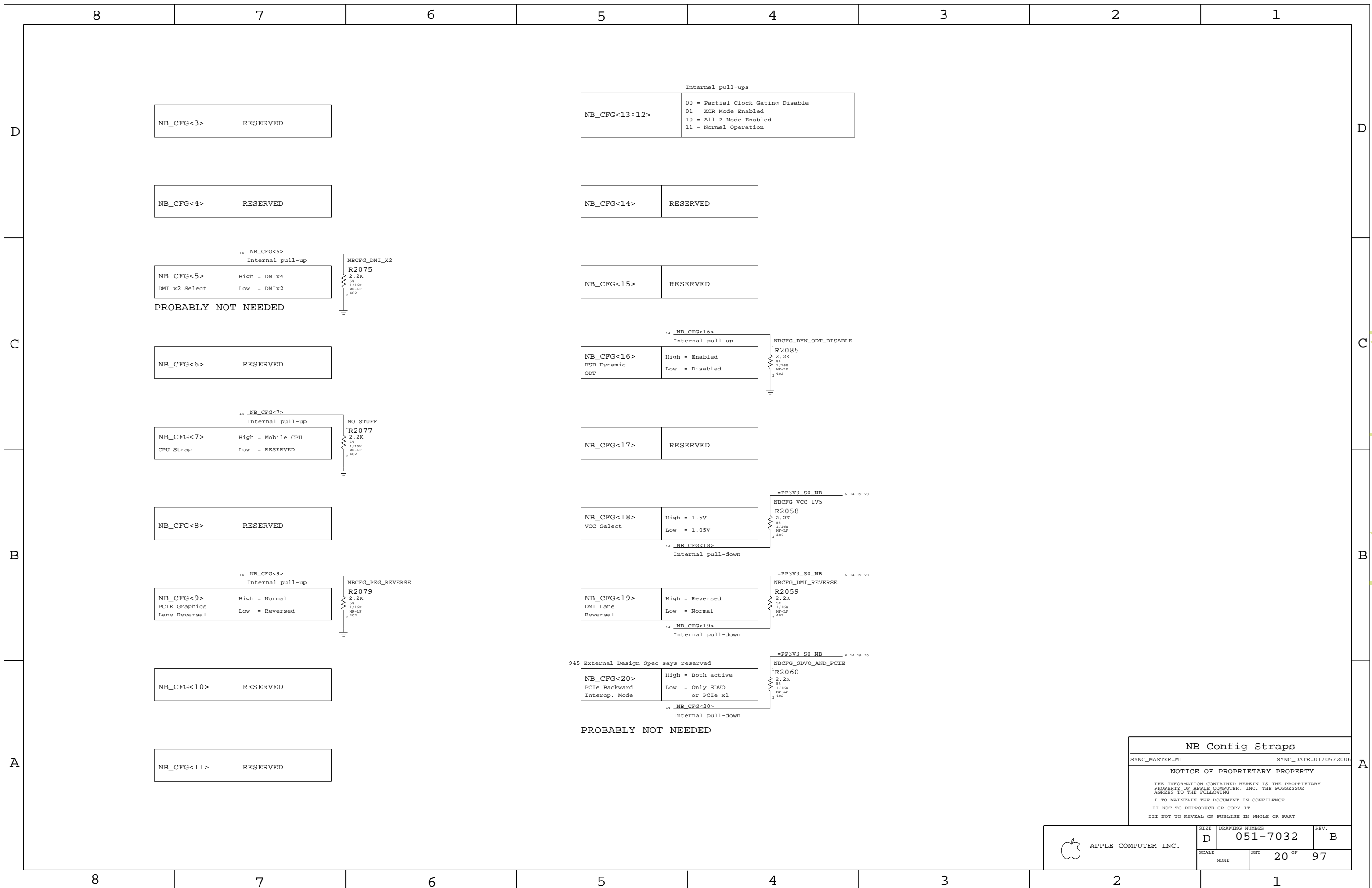
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHT 18 OF	97



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NB (GM) Decoupling
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHT 19 OF 97	



NB Config Straps

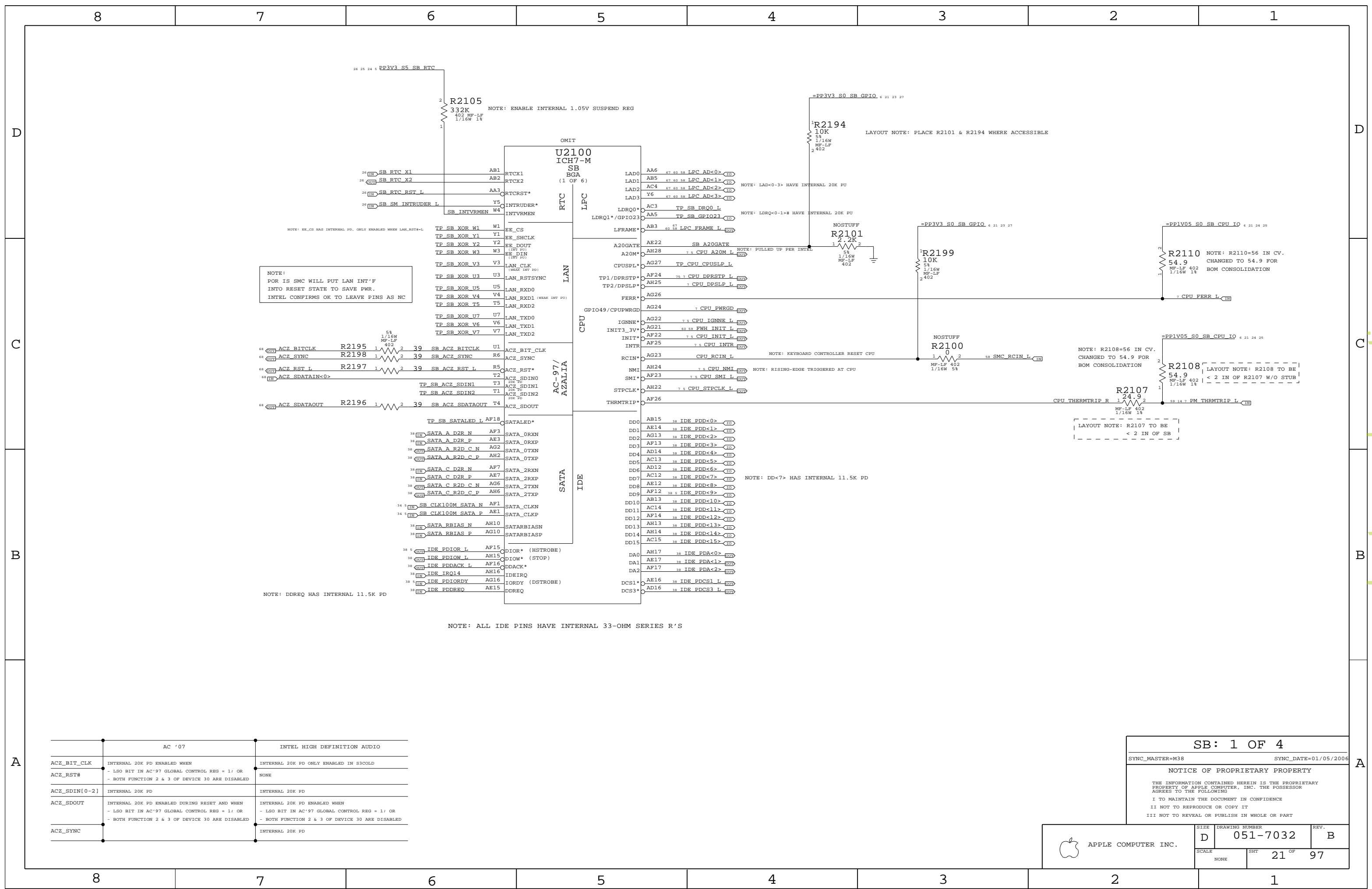
SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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APPLE COMPUTER INC.	SCALE NONE	SHT 20 OF 97	DRAWING NUMBER D 051-7032	REV. B
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NOTE:
POR IS SMC WILL PUT LAN INT'F
INTO RESET STATE TO SAVE PWR.
INTEL CONFIRMS OK TO LEAVE PINS AS NC

NOTE: DDREQ HAS INTERNAL 11.5K PD

NOTE: ALL IDE PINS HAVE INTERNAL 33-OHM SERIES R'S

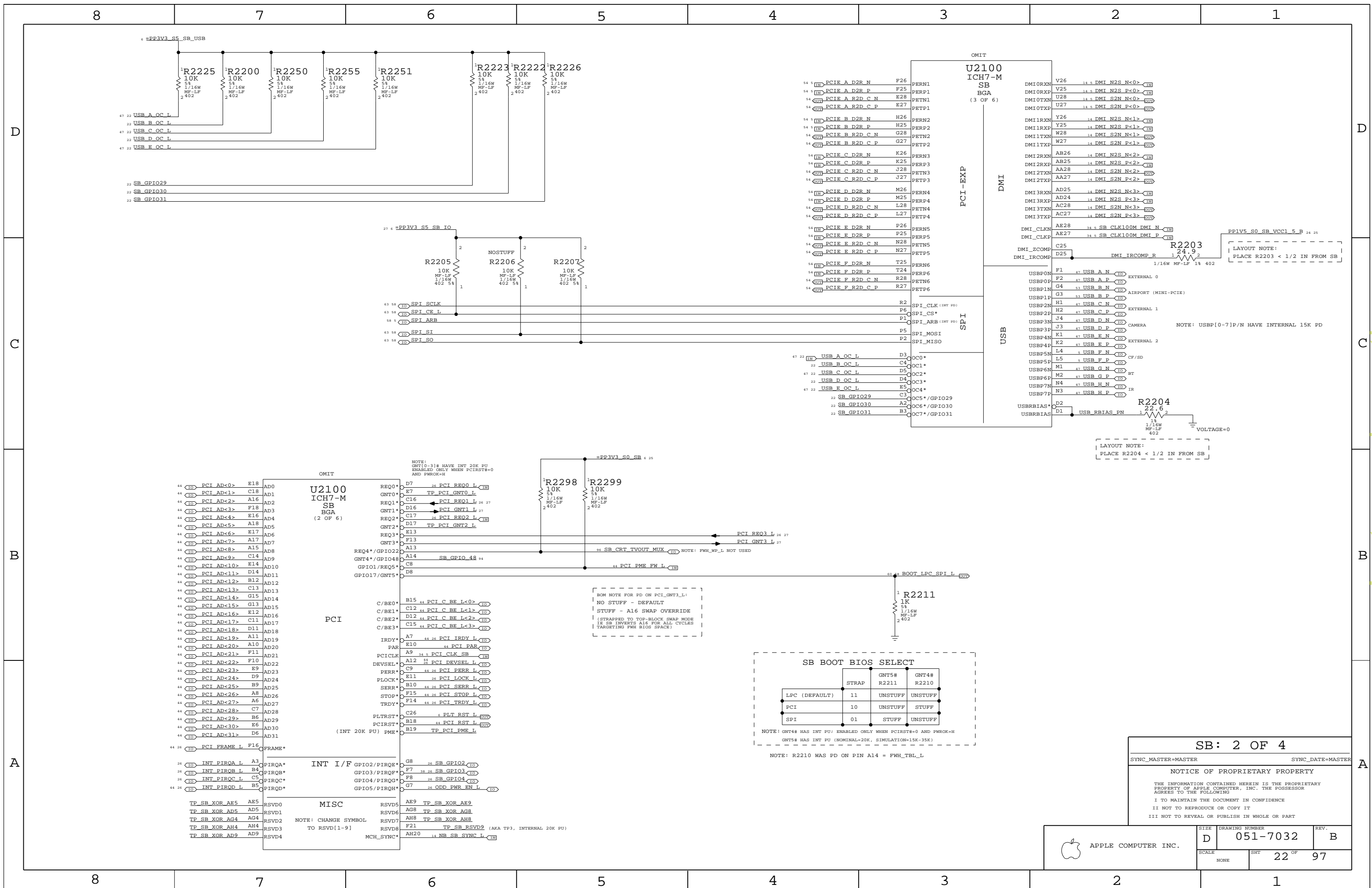
AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	B
SCALE	SHT	21 OF 97
NONE		

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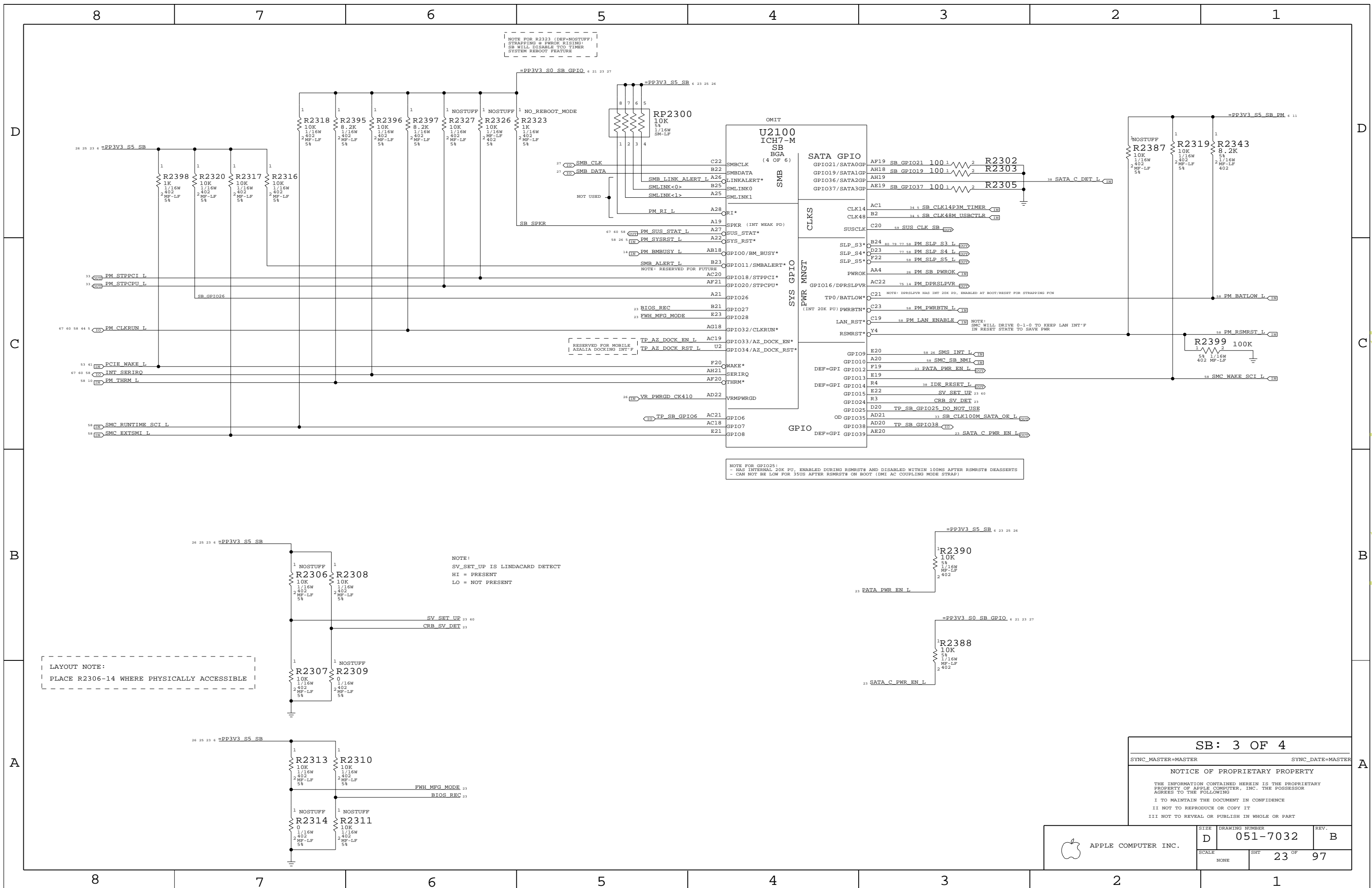
www.laptop-schematics.com

SB: 2 OF 4

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SCALE	SHT	REV.
	NONE	22 OF 97	B



NOTE FOR R2323 (DEF-NOSTUFF)
STRAPPING & PWROK RISING:
SB WILL DISABLE TOO TIMER
SYSTEM REBOOT FEATURE

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

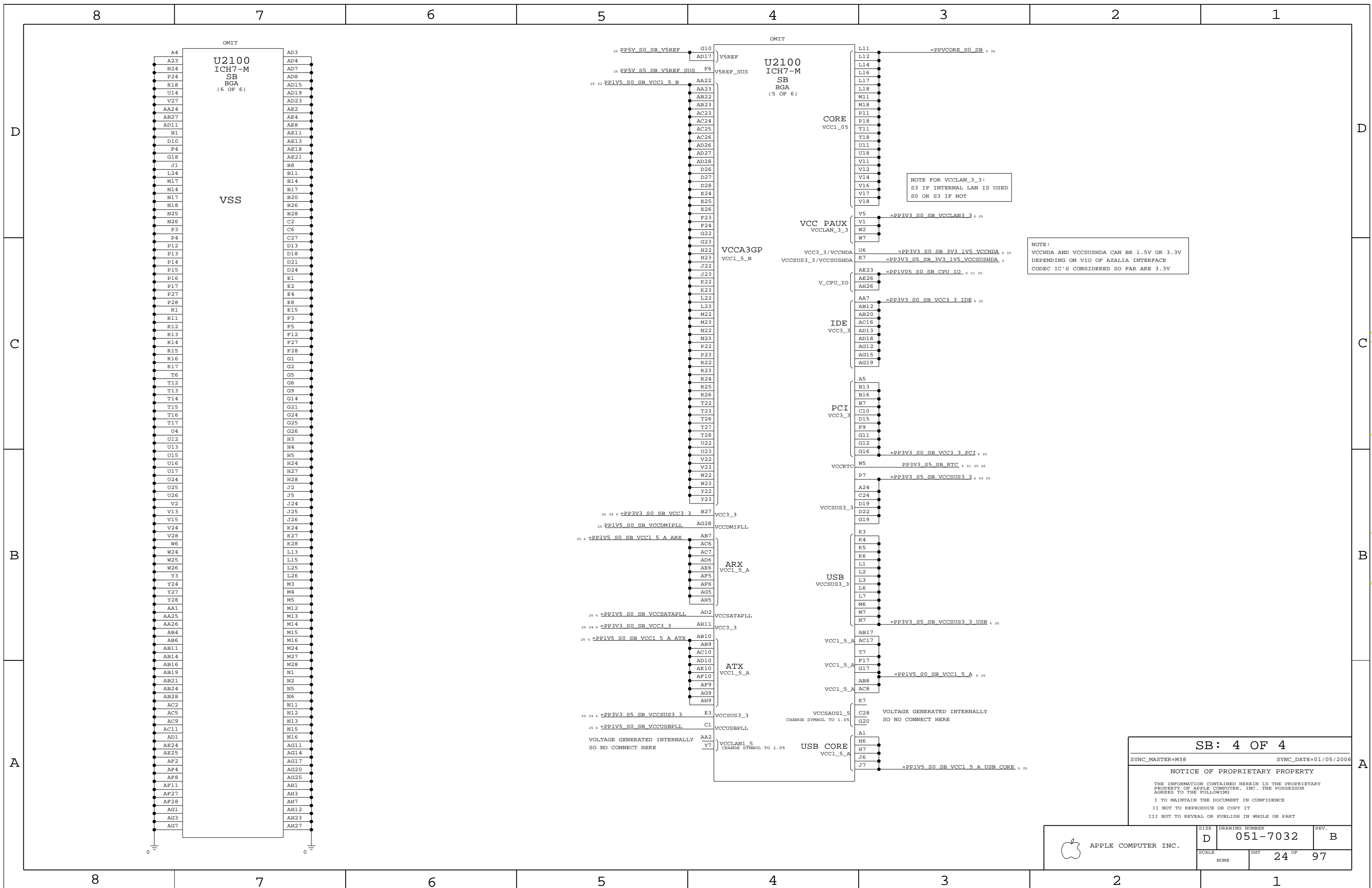
LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SB: 3 OF 4
SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	B
SCALE	NONE	SHT	23 OF 97

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NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

NOTE:
VCC3_3/VCC3_3 AND VCCSUS3_3 CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

SB: 4 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

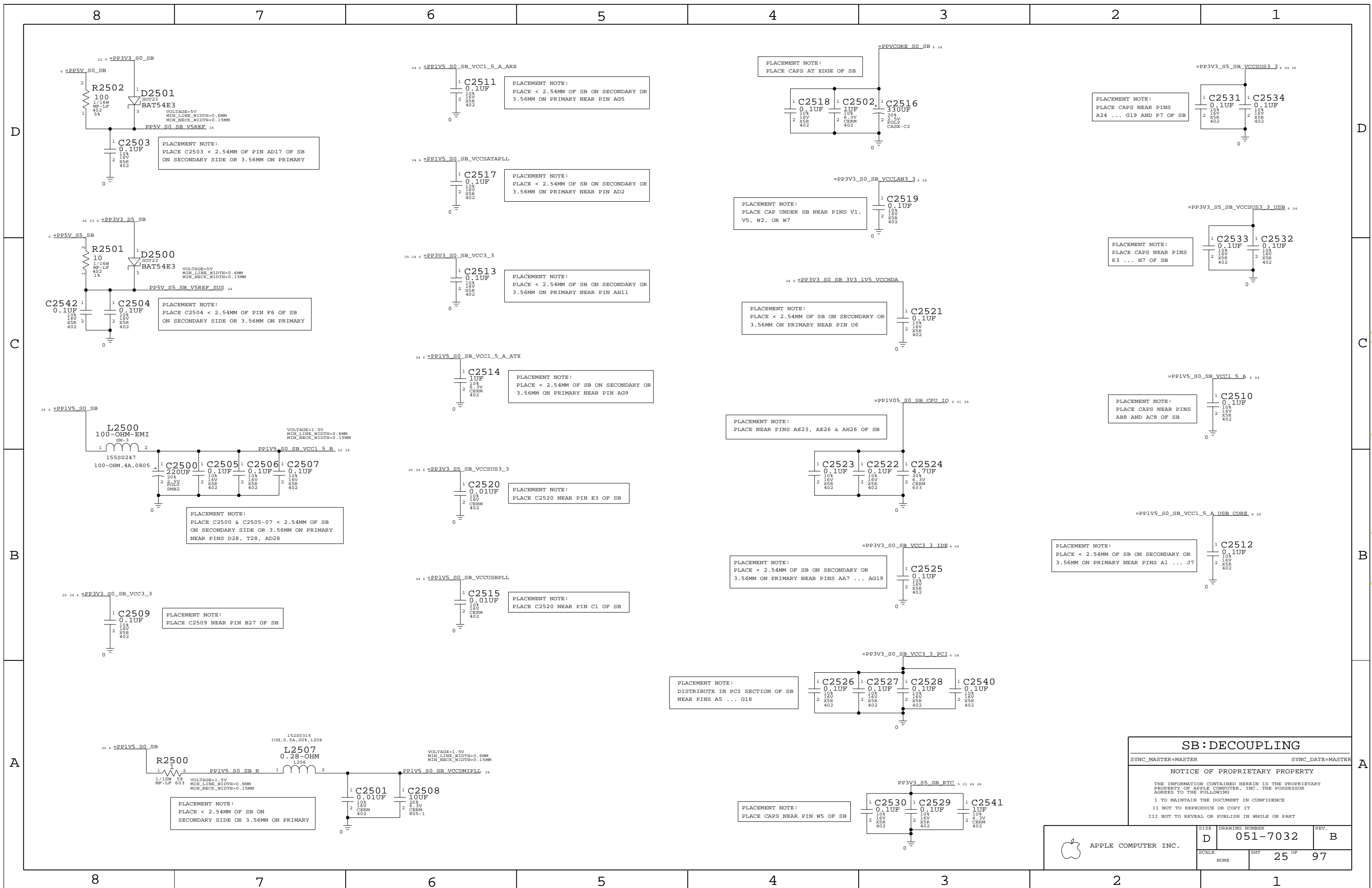
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	D	051-7032	B
SCALE	SHT	24 OF 97	
NONE			

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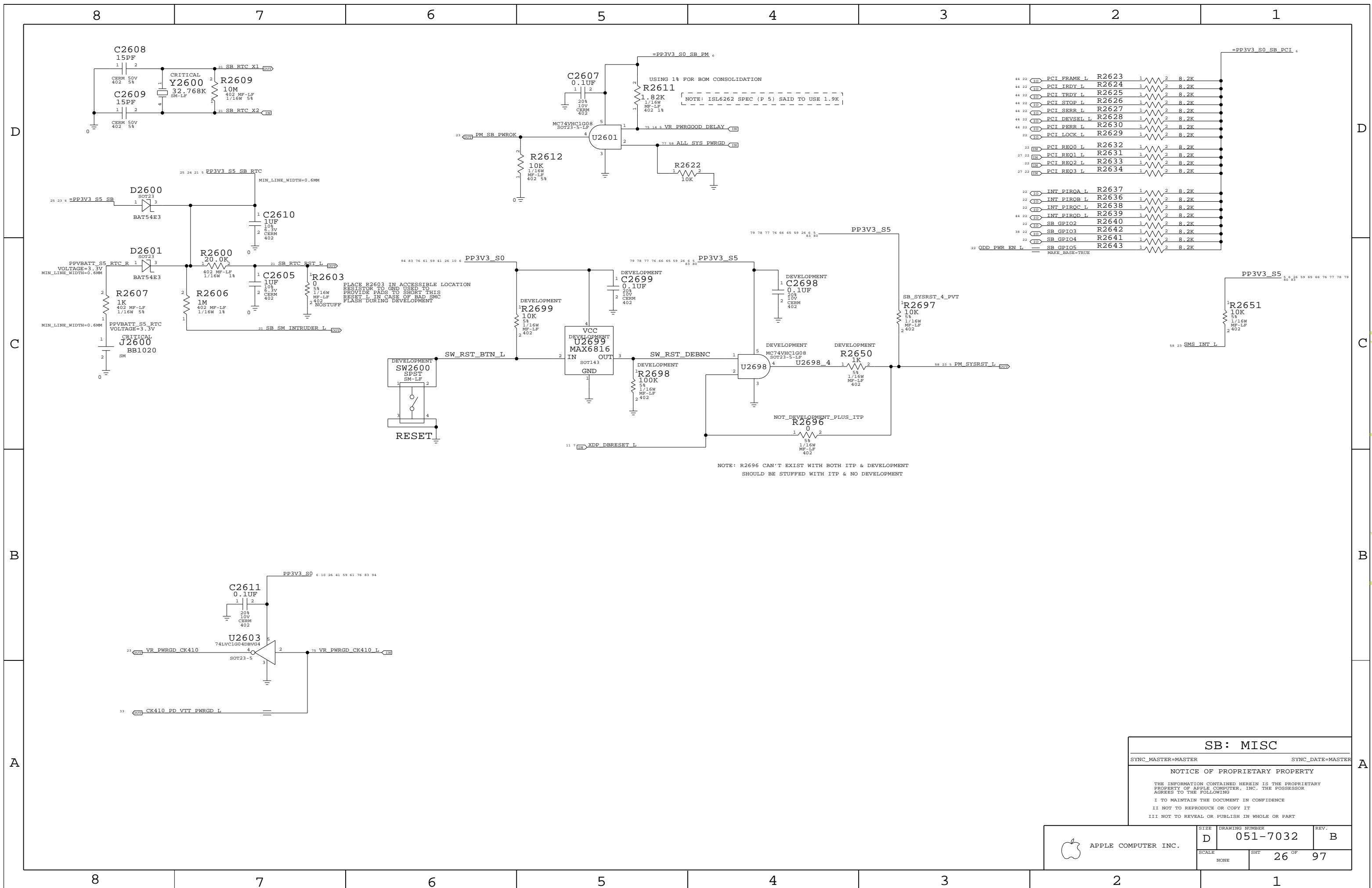
SB: DECOUPLING

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	25 OF	97
NONE			



SB: MISC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	NONE	SHT	26 OF 97

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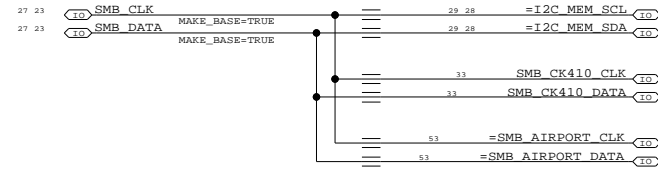
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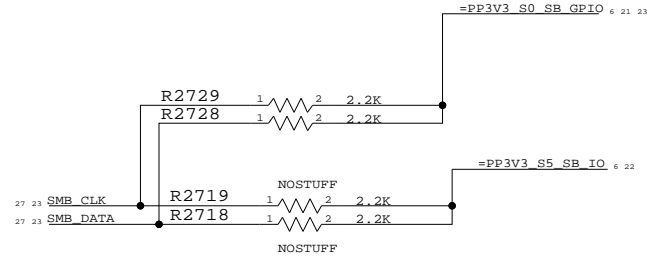
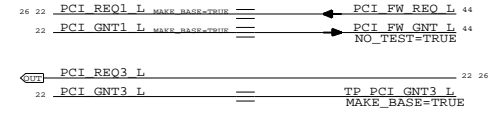
2

1

SB I2C BUSSES



PCI CONTROL



SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	27 OF 97	
NONE			

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Page Notes

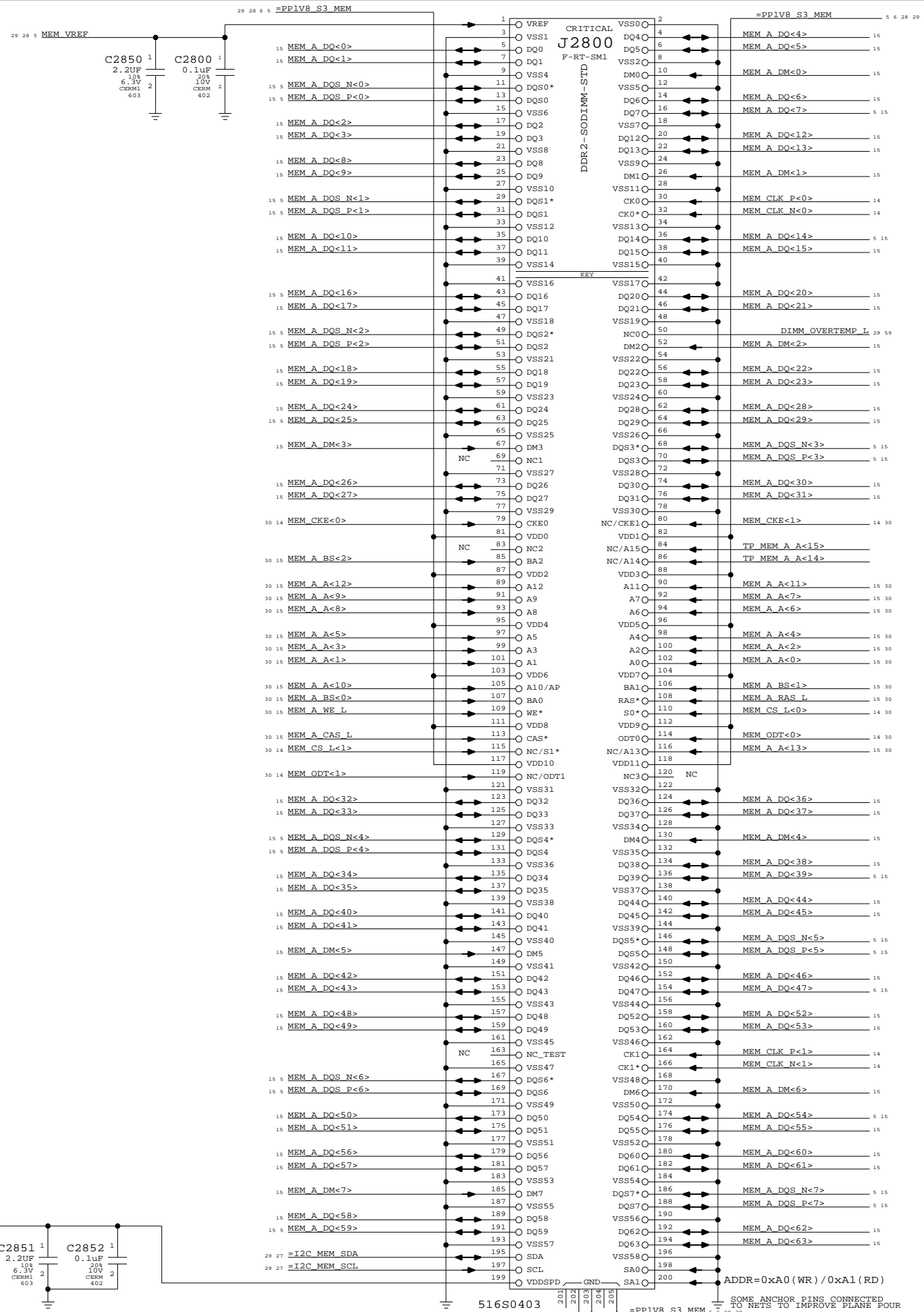
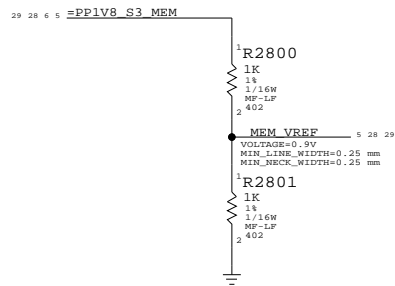
Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

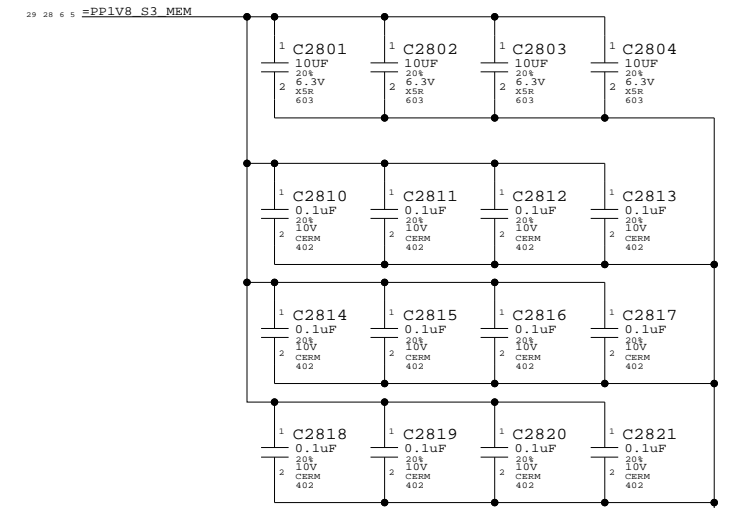
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	28 OF 97	
NONE			

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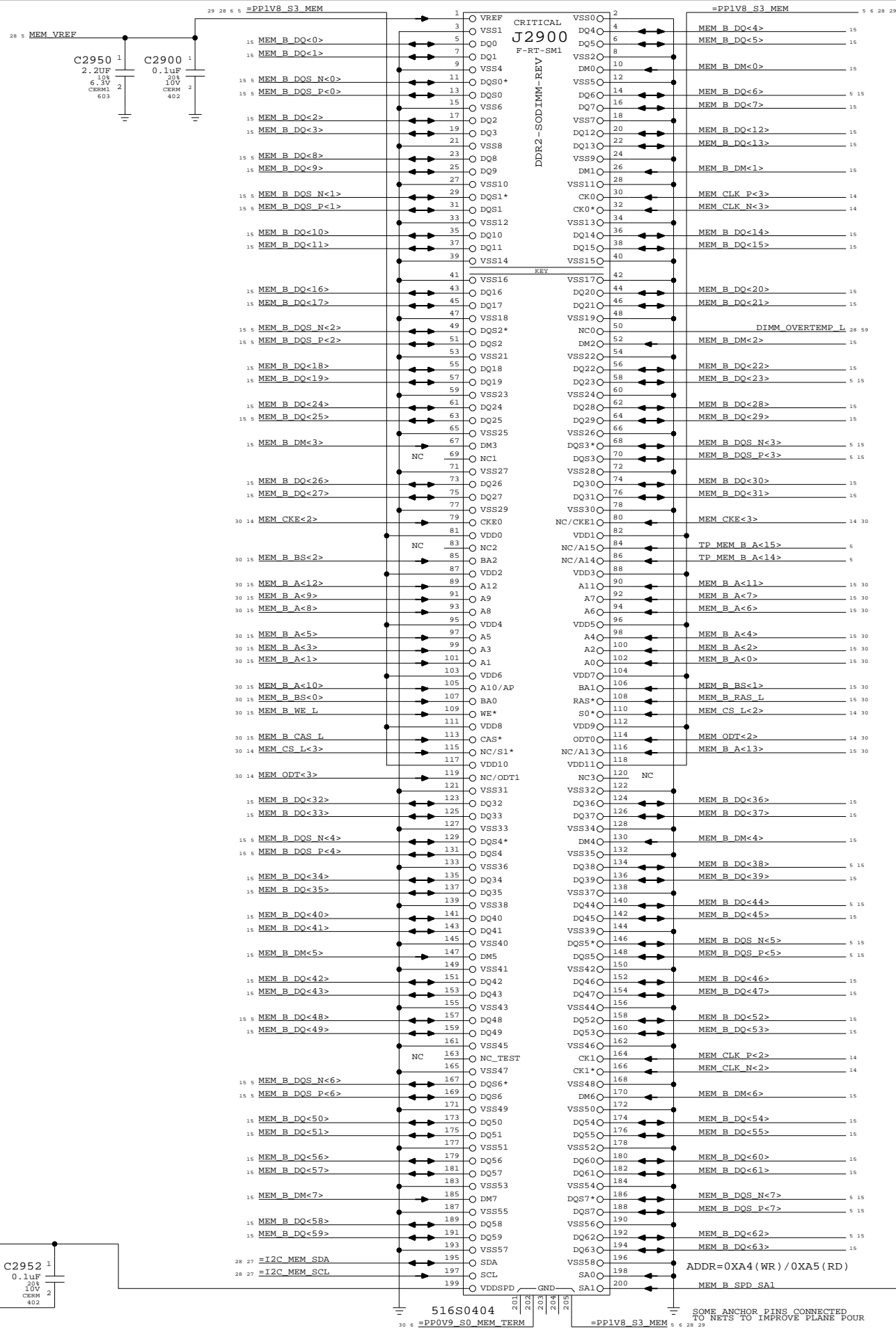
Page Notes

Power aliases required by this page:
 - =PP1V8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

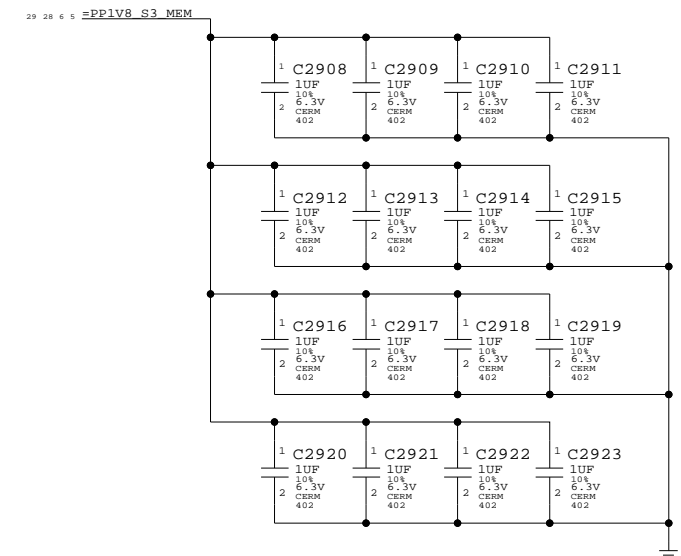
Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

NOTE: This page does not supply VREF.
 The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B

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	SCALE NONE	SHEET 29 OF 97	

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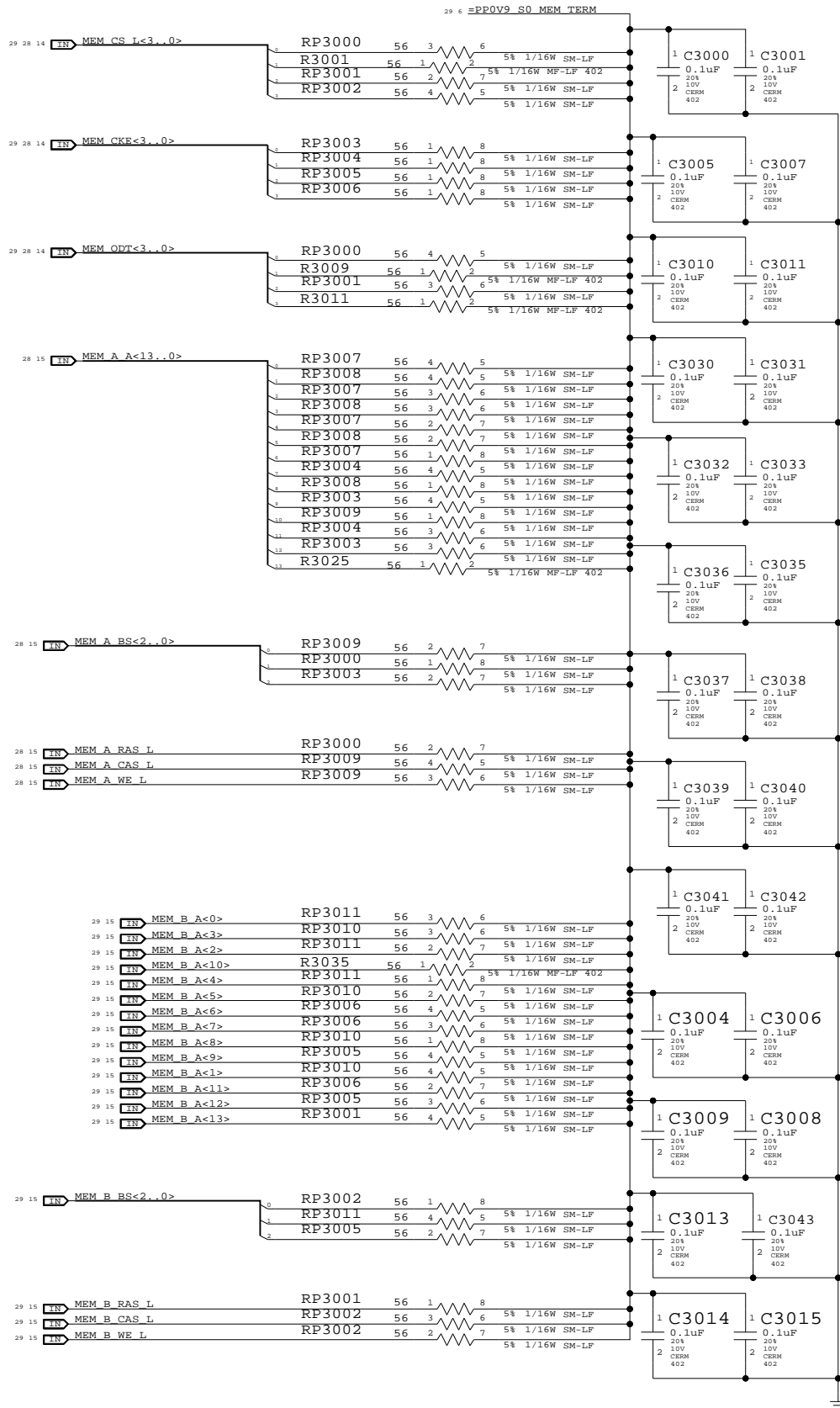
4

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One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7032	B
SCALE	SHT	30 OF 97	
NONE			

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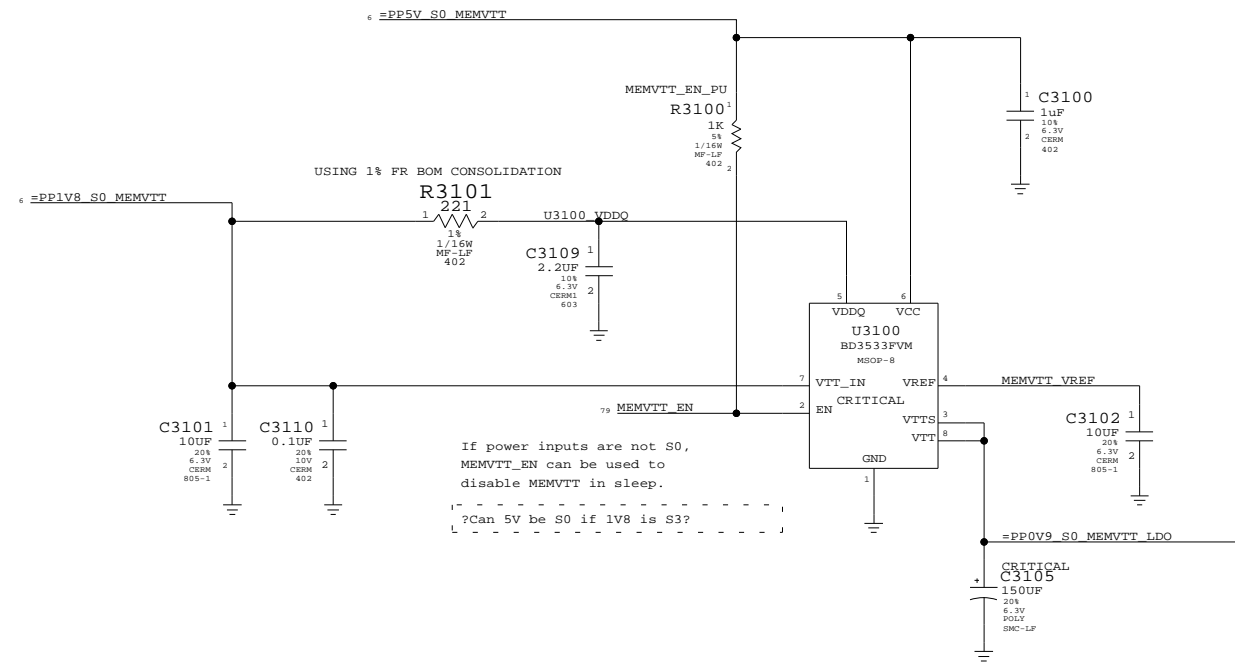
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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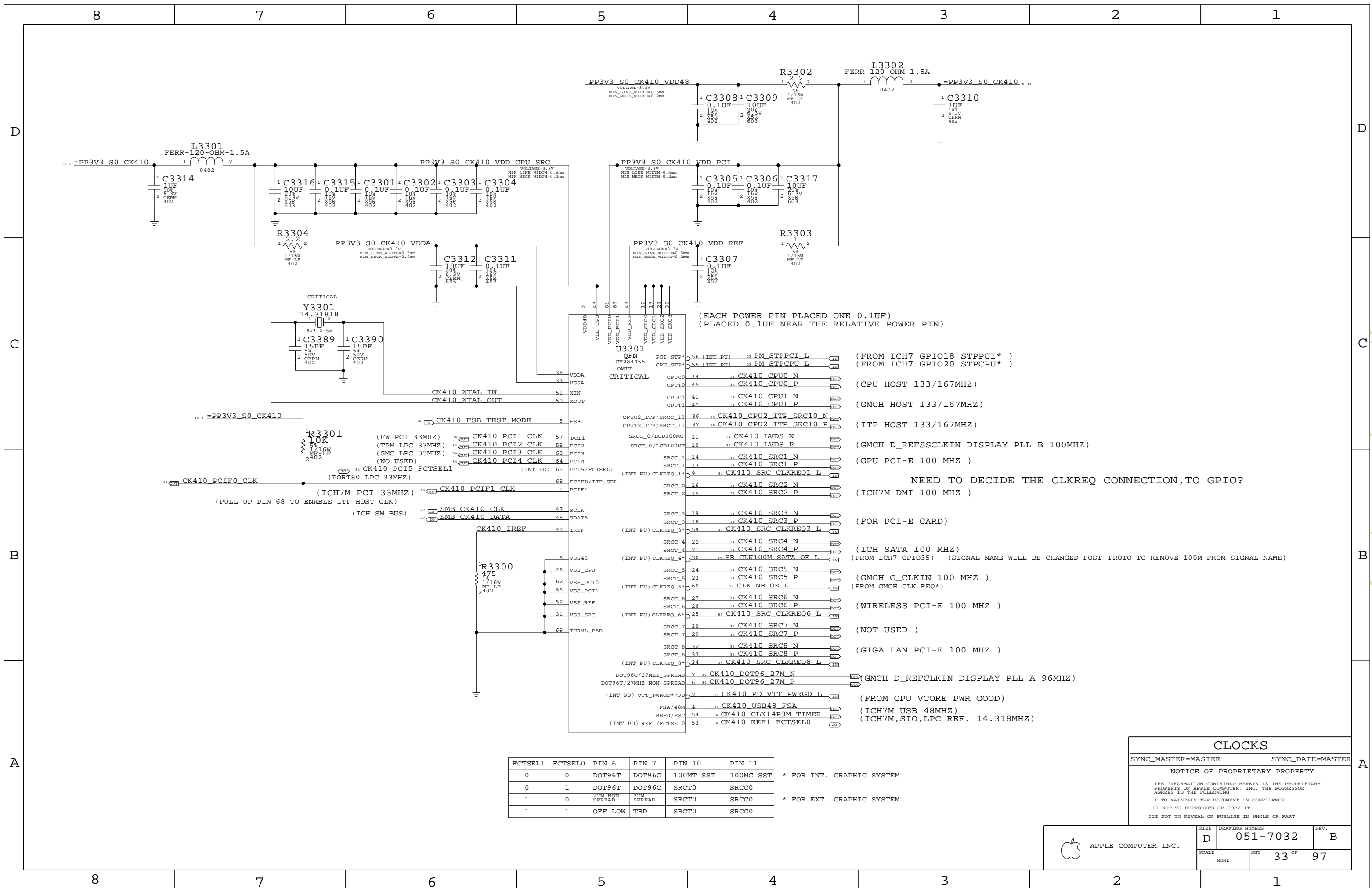
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	D	051-7032	B
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

- 56 (INT PU) PM_STPPCI L (FROM ICH7 GPIO18 STPPCI*)
- 55 (INT PU) PM_STPCPU L (FROM ICH7 GPIO20 STPCPU*)
- 44 CK410 CPU0 N (CPU HOST 133/167MHZ)
- 45 CK410 CPU0 P
- 41 CK410 CPU1 N (GMCH HOST 133/167MHZ)
- 42 CK410 CPU1 P
- 36 CK410 CPU2 ITP_SRC10_N (ITP HOST 133/167MHZ)
- 37 CK410 CPU2 ITP_SRC10_P
- 11 CK410 LVDS N (GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
- 10 CK410 LVDS P
- 14 CK410 SRC1 N (GPU PCI-E 100 MHZ)
- 13 CK410 SRC1 P
- 9 CK410 SRC CLKREQ1 L (NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?)
- 16 CK410 SRC2 N (ICH7M DMI 100 MHZ)
- 15 CK410 SRC2 P
- 19 CK410 SRC3 N (FOR PCI-E CARD)
- 18 CK410 SRC3 P
- 59 CK410 SRC CLKREQ3 L (FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
- 22 CK410 SRC4 N (ICH SATA 100 MHZ)
- 21 CK410 SRC4 P
- 20 SB_CLK100M_SATA_OE L (FROM GMCH CLK_REQ*)
- 24 CK410 SRC5 N (GMCH G_CLKIN 100 MHZ)
- 23 CK410 SRC5 P
- 60 CLK_NB_OE L (FROM GMCH CLK_REQ*)
- 27 CK410 SRC6 N (WIRELESS PCI-E 100 MHZ)
- 26 CK410 SRC6 P
- 25 CK410 SRC CLKREQ6 L (NOT USED)
- 30 CK410 SRC7 N (NOT USED)
- 29 CK410 SRC7 P
- 32 CK410 SRC8 N (GIGA LAN PCI-E 100 MHZ)
- 33 CK410 SRC8 P
- 34 CK410 SRC CLKREQ8 L
- 7 CK410 DOT96 27M N (GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
- 6 CK410 DOT96 27M P
- 2 CK410 PD VTT_PWRGD L (FROM CPU VCORE PWR GOOD)
- 4 CK410 USB48_FSA (ICH7M USB 48MHZ)
- 54 CK410 CLK14P3M_TIMER (ICH7M, SIO, LPC REF. 14.318MHZ)
- 53 CK410 REF1_FCTSEL0

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST
0	1	DOT96T	DOT96C	SRCT0	SRCC0
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0
1	1	OFF LOW	TBD	SRCT0	SRCC0

* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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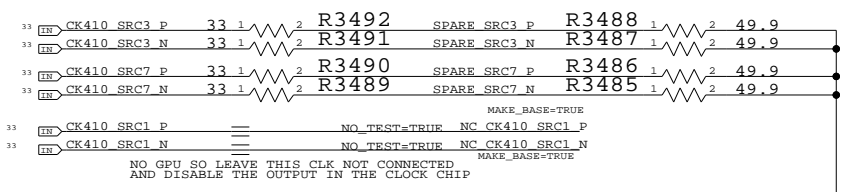
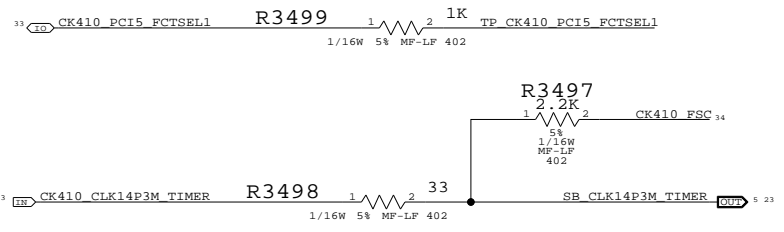
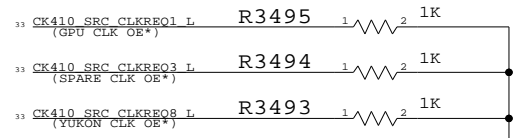
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	D	051-7032	B
SCALE	SHT	33 OF 97	
NONE			

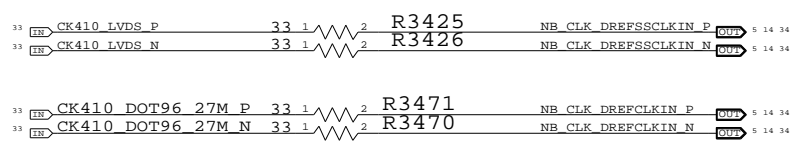
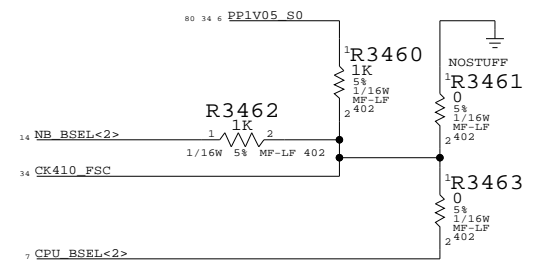
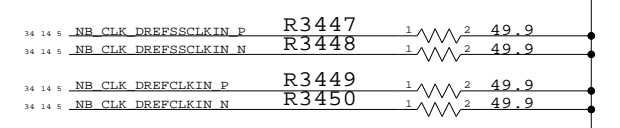
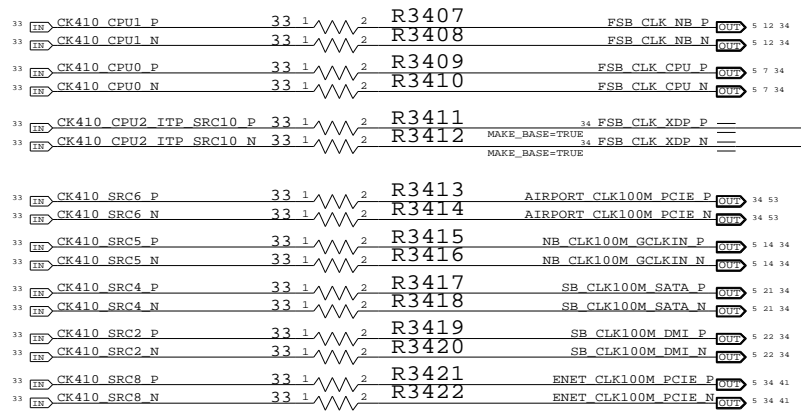
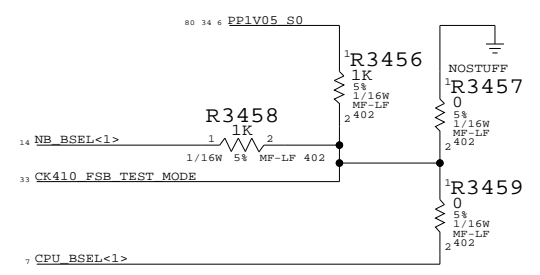
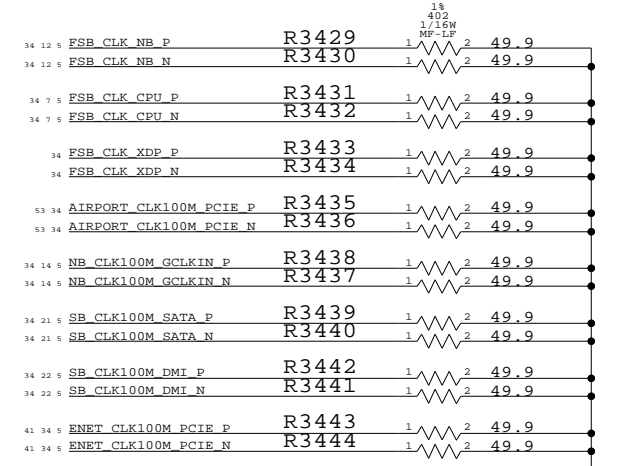
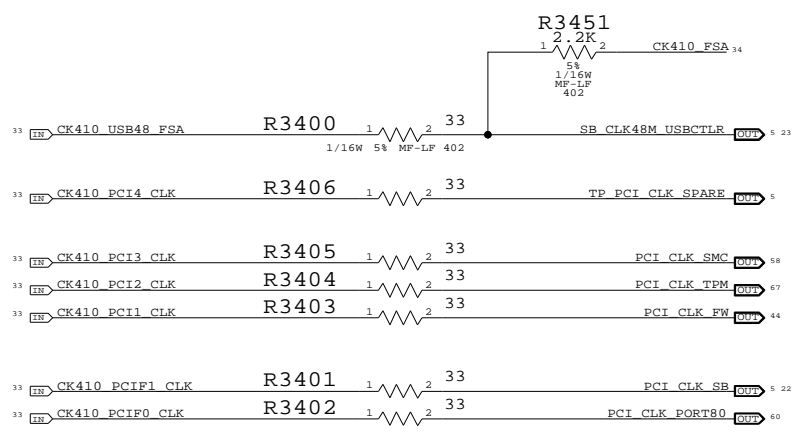
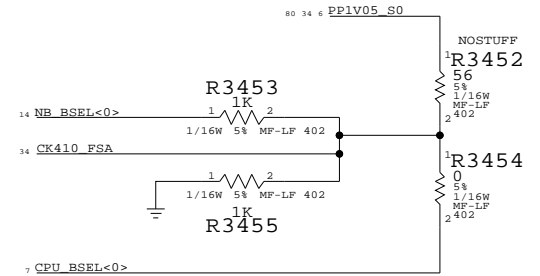
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NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457 R3458
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458



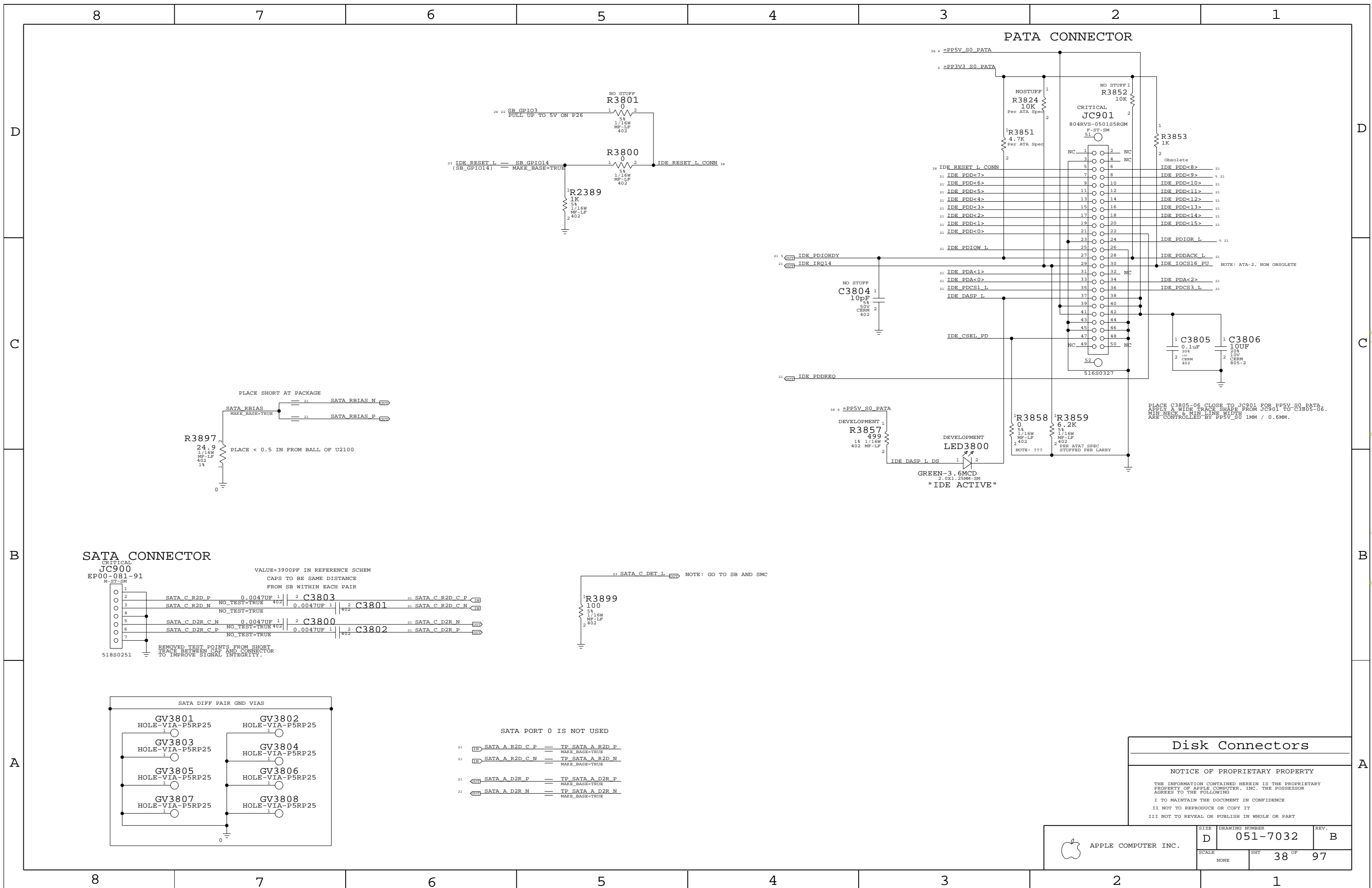
CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

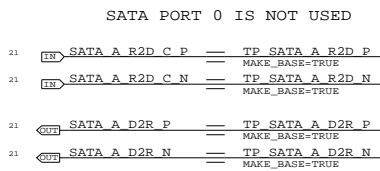
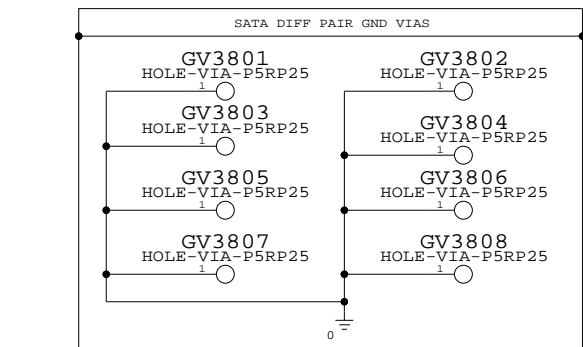
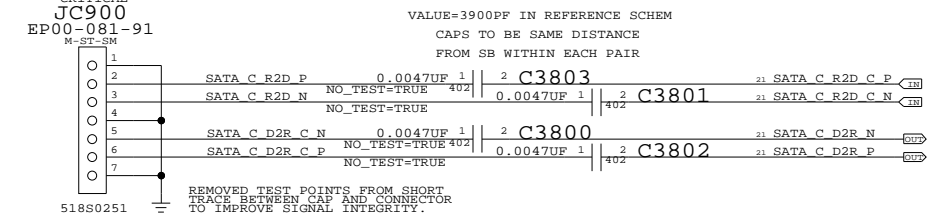
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	34 OF	97
NONE			



SATA CONNECTOR



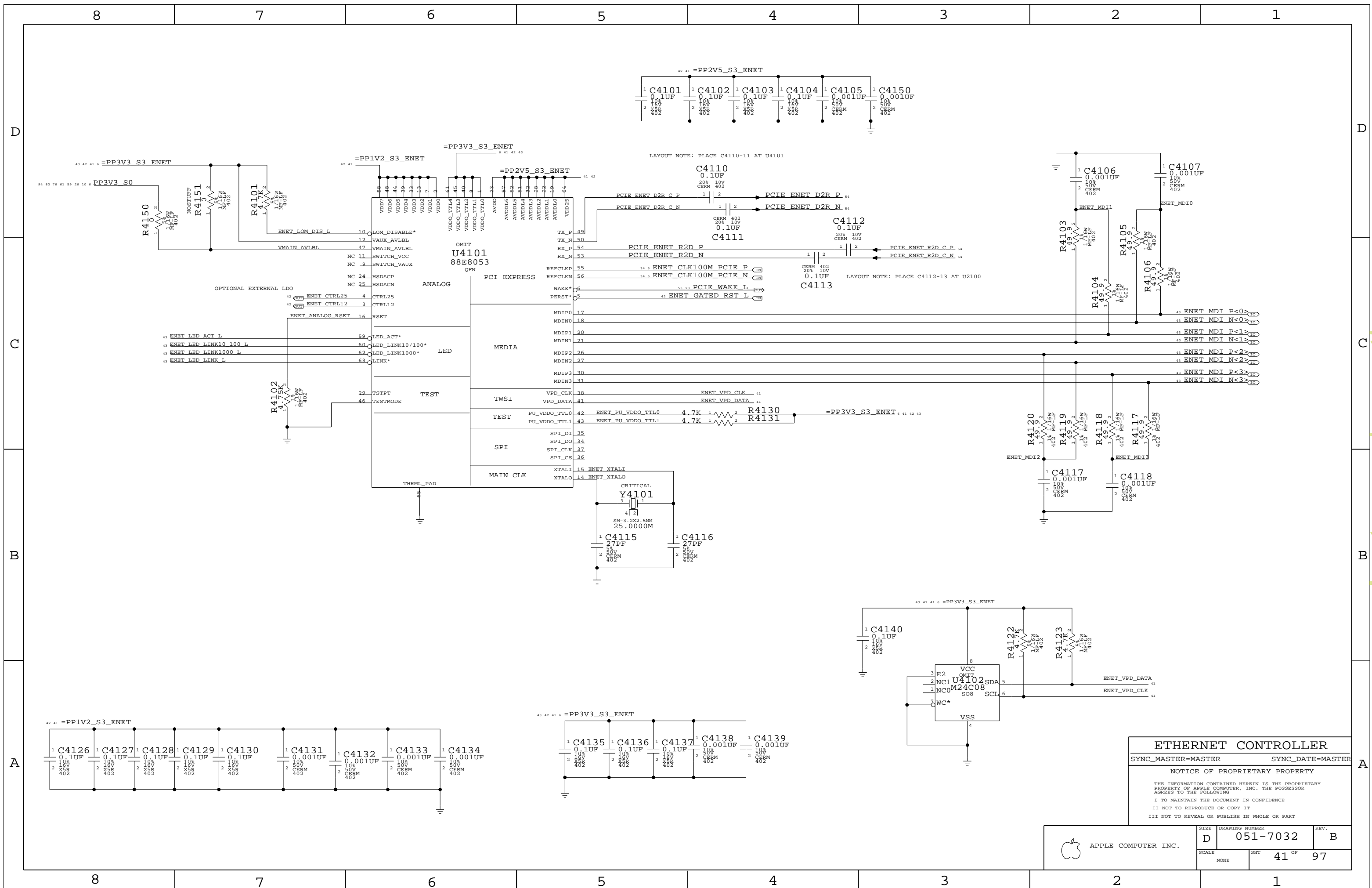
Disk Connectors

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	D	051-7032	B
SCALE	SHT	38 OF 97	
NONE			



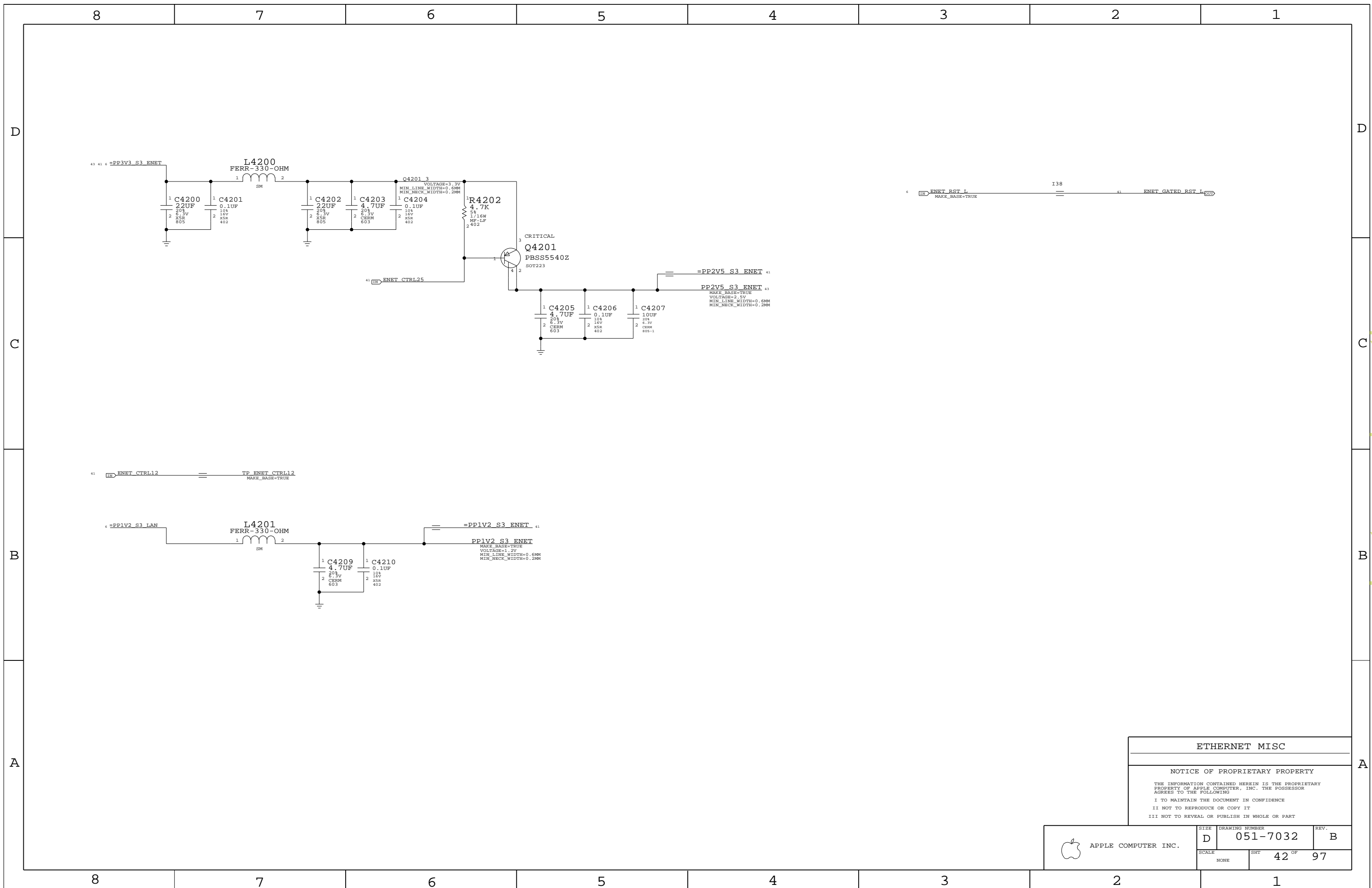
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATA=MASTER

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	D	051-7032	B
SCALE	SHT	41 OF 97	
NONE			



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ETHERNET MISC

NOTICE OF PROPRIETARY PROPERTY

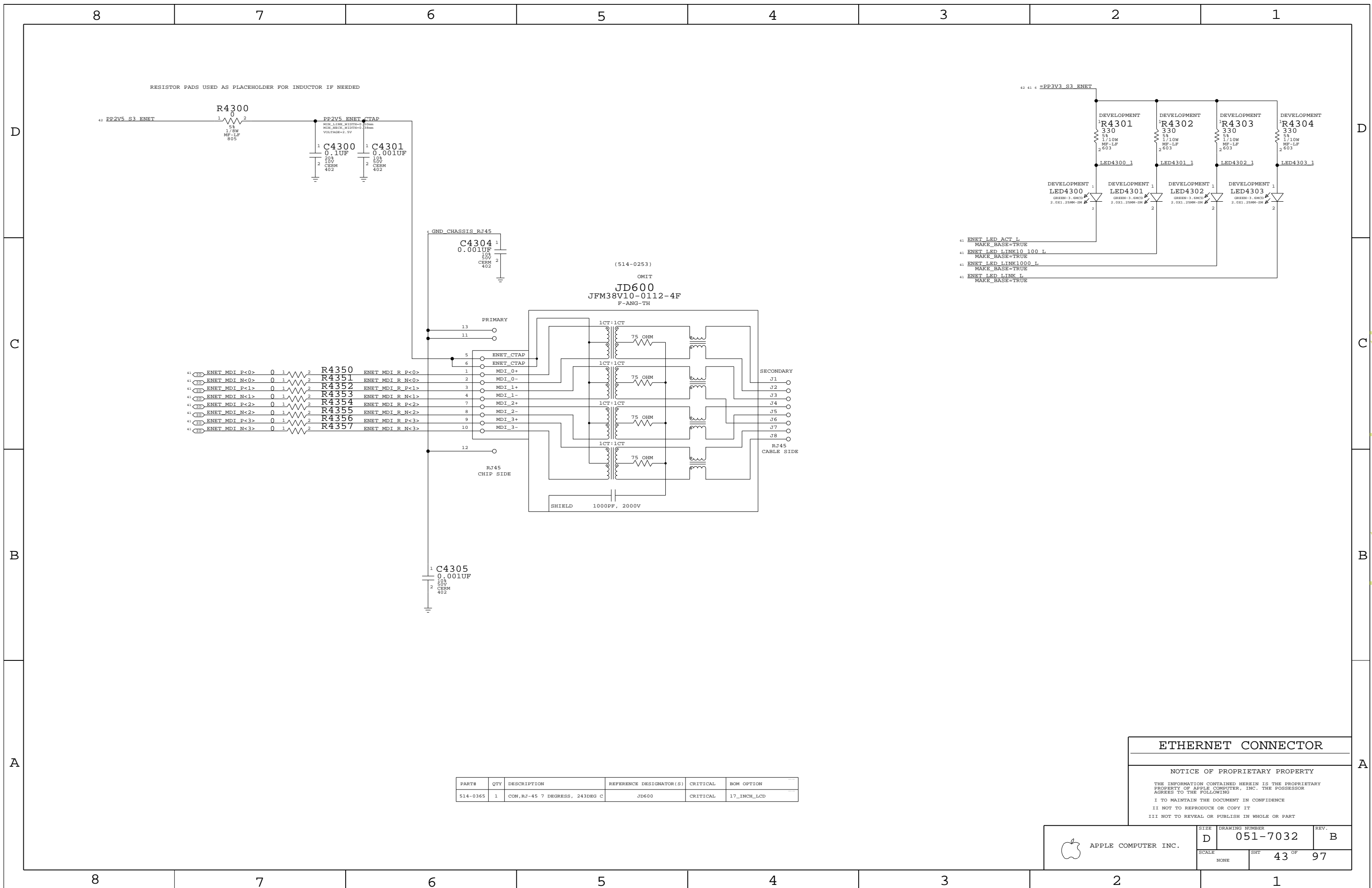
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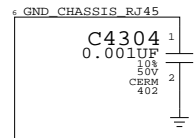
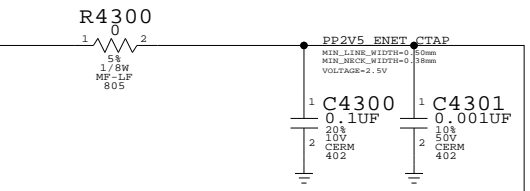
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

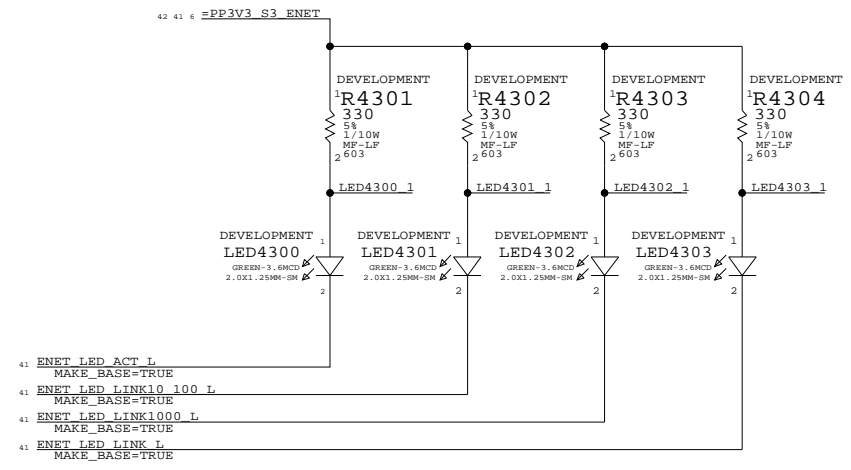
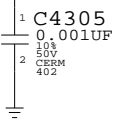
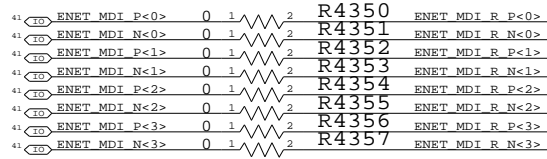
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	42 OF 97	
NONE			



RESISTOR PADS USED AS PLACEHOLDER FOR INDUCTOR IF NEEDED



(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH

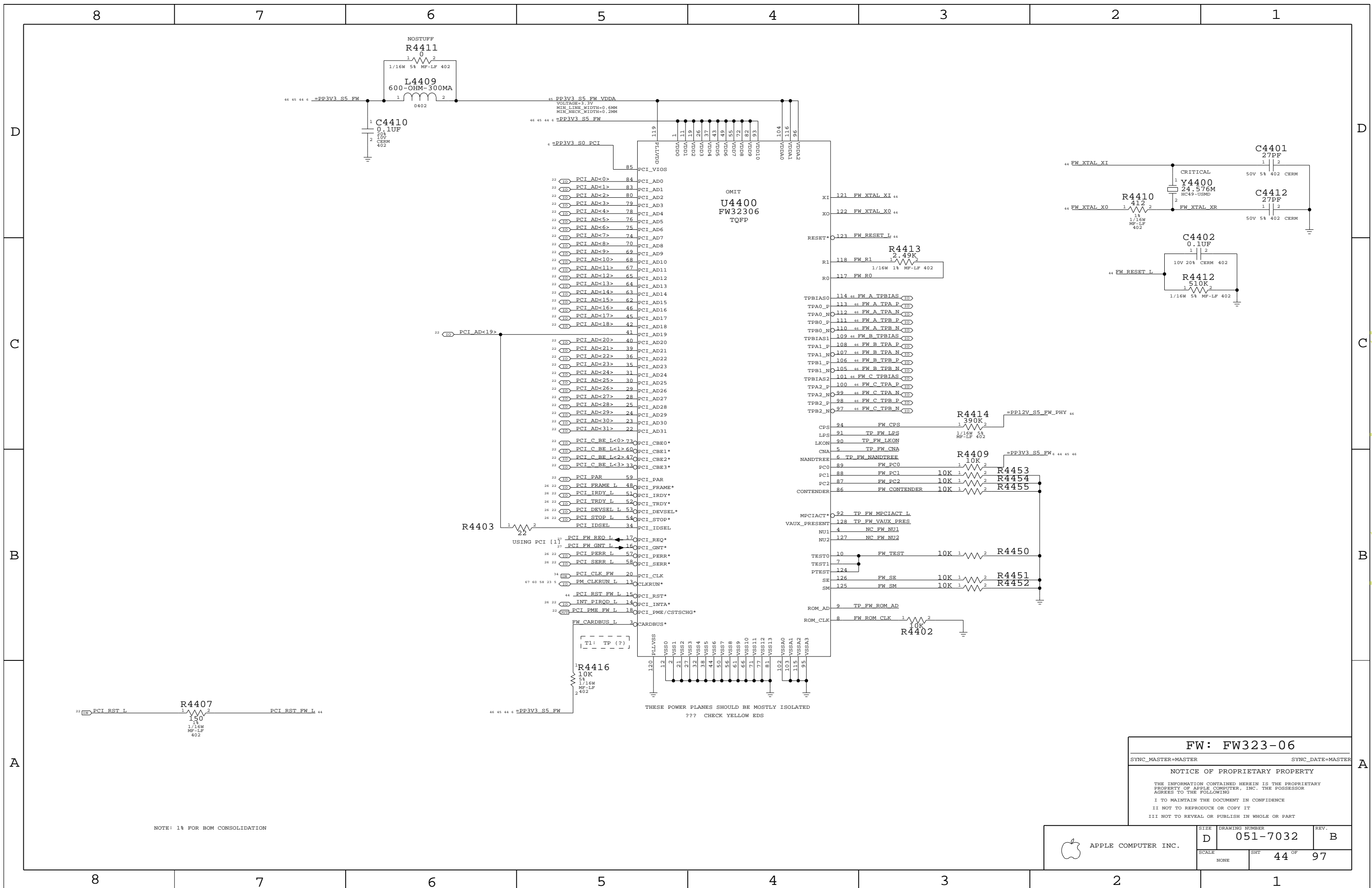


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	43 OF 97	
NONE			

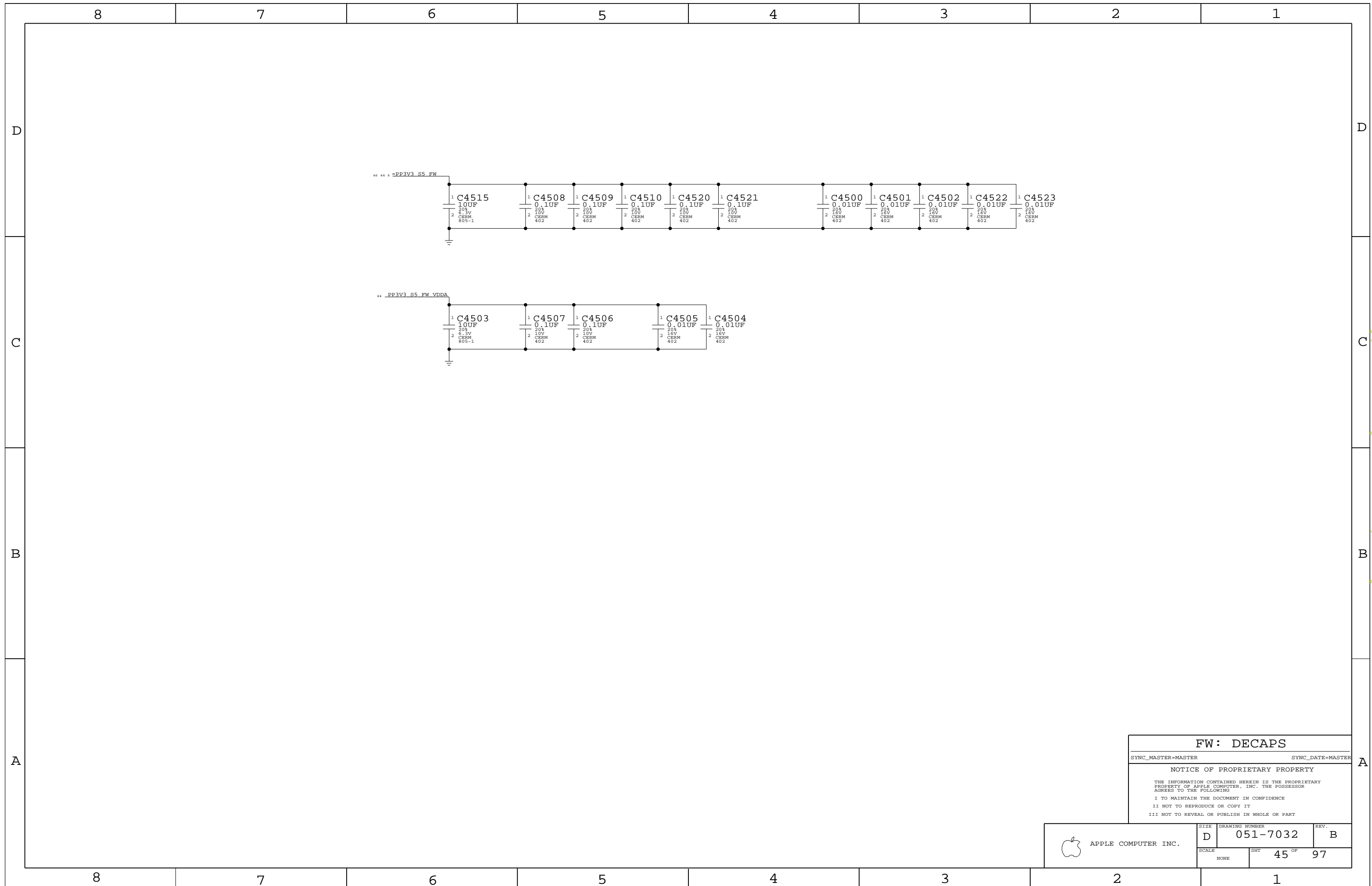


NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	44 OF 97	
NONE			

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FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

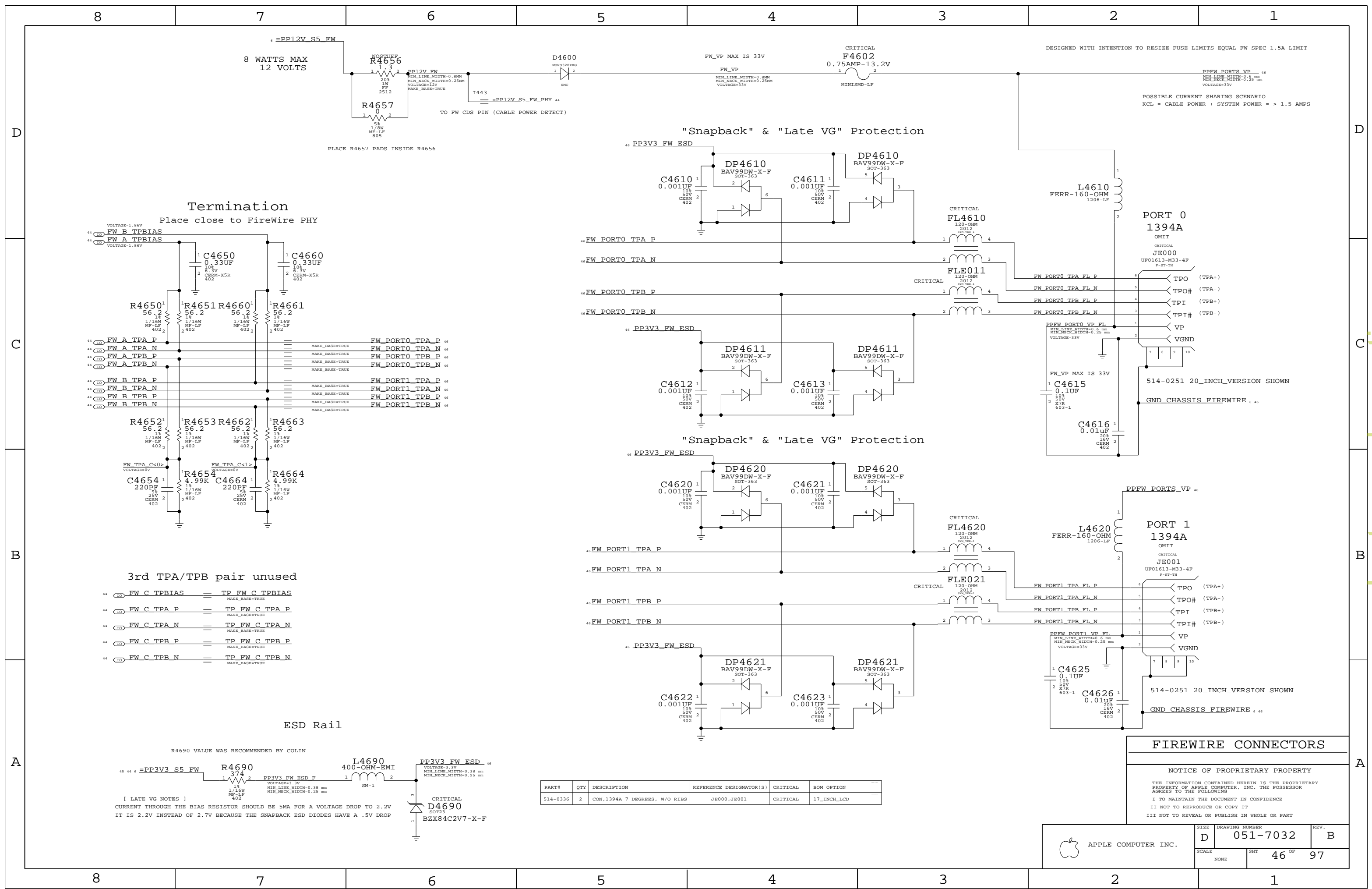
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHIT 45 OF 97	



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

ESD Rail

FIREWIRE CONNECTORS

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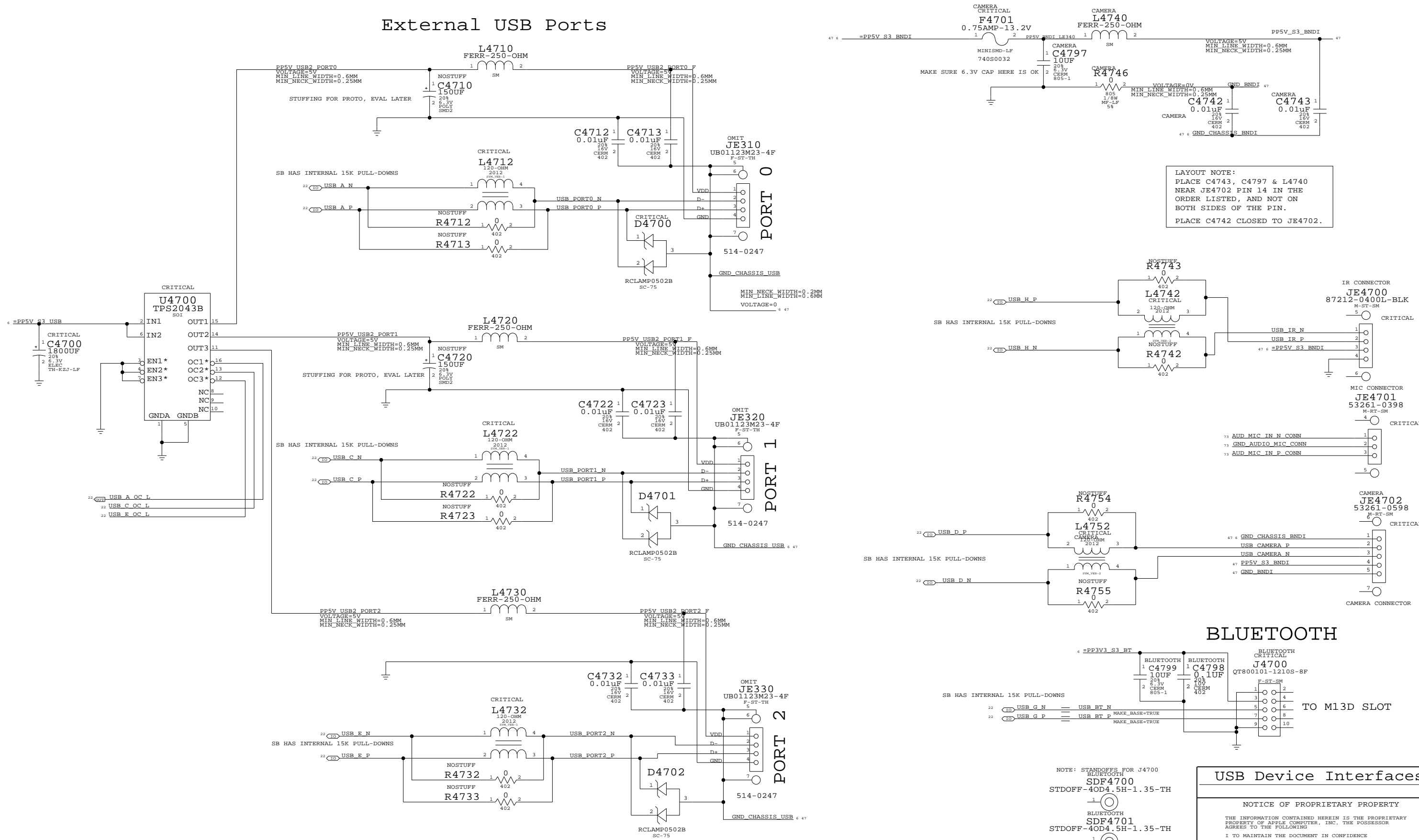
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7032	B
SCALE	SHT	46 OF 97
NONE		

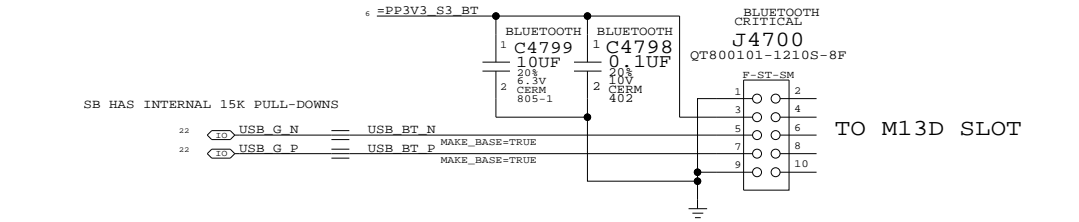
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External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE4702 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE4702.

BLUETOOTH



NOTE: STANDOFFS FOR J4700
 BLUETOOTH
 SDF4700
 STDOFF-40D4.5H-1.35-TH
 BLUETOOTH
 SDF4701
 STDOFF-40D4.5H-1.35-TH

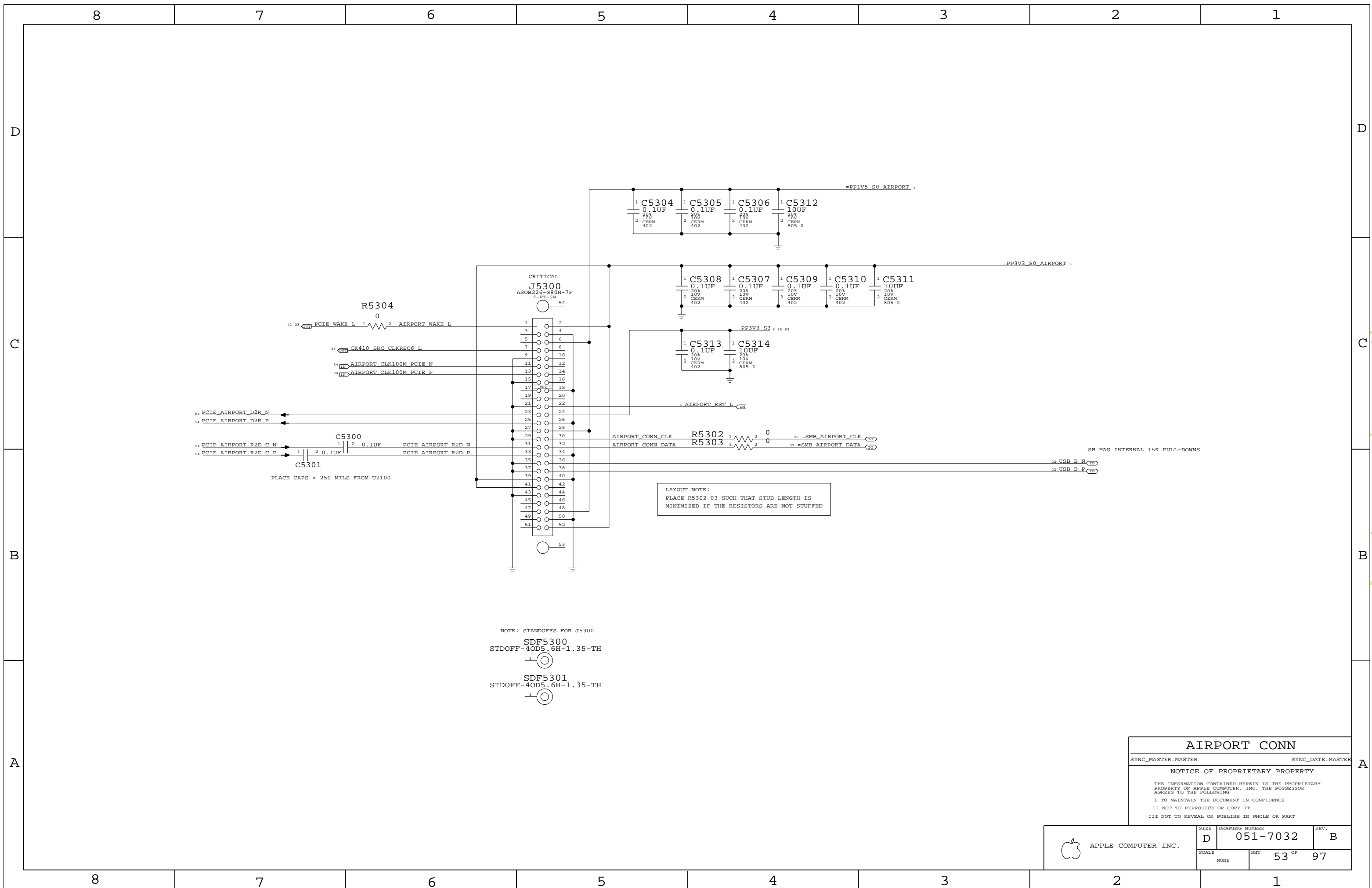
USB Device Interfaces

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

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	47 OF 97	
NONE			

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LAYOUT NOTE:
 PLACE R5302-03 SUCH THAT STUB LENGTH IS
 MINIMIZED IF THE RESISTORS ARE NOT STUFFED

NOTE: STANDOFFS FOR J5300
 SDF5300
 STDOFF-40D5.6H-1.35-TH

 SDF5301
 STDOFF-40D5.6H-1.35-TH


SB HAS INTERNAL 15K PULL-DOWNS


AIRPORT CONN

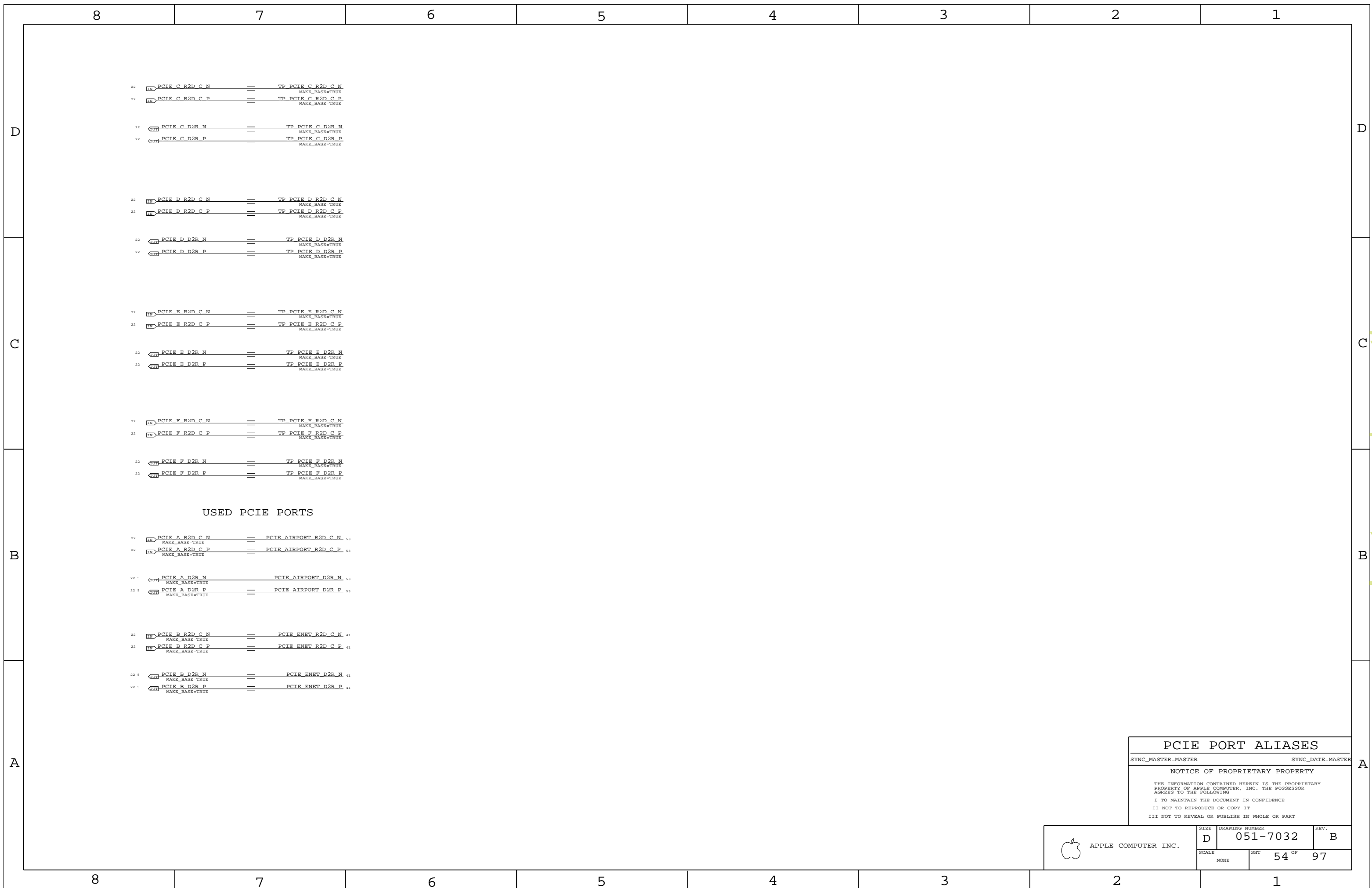
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 53 OF 97	



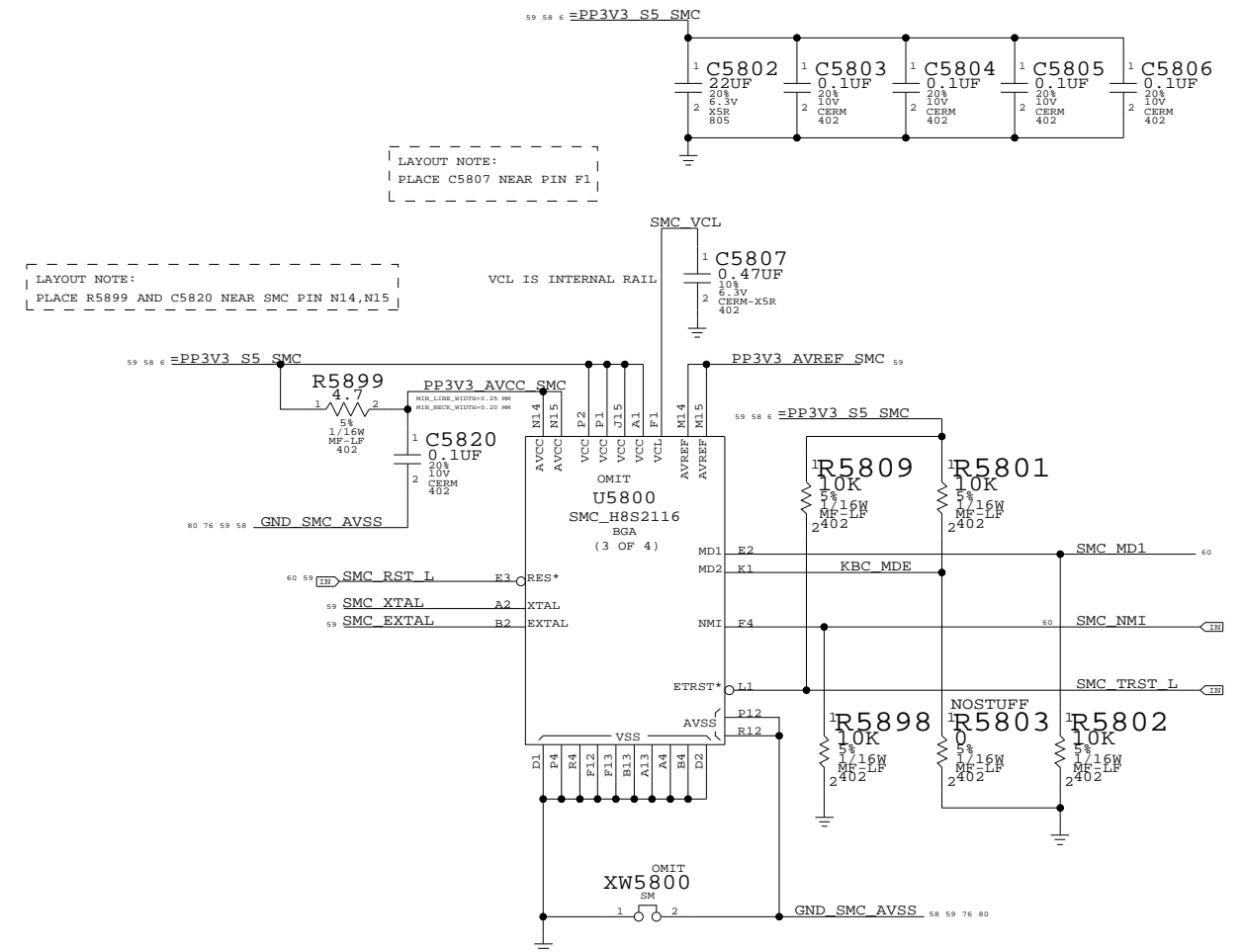
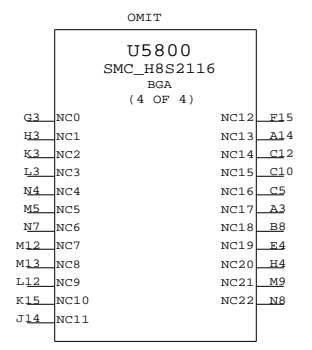
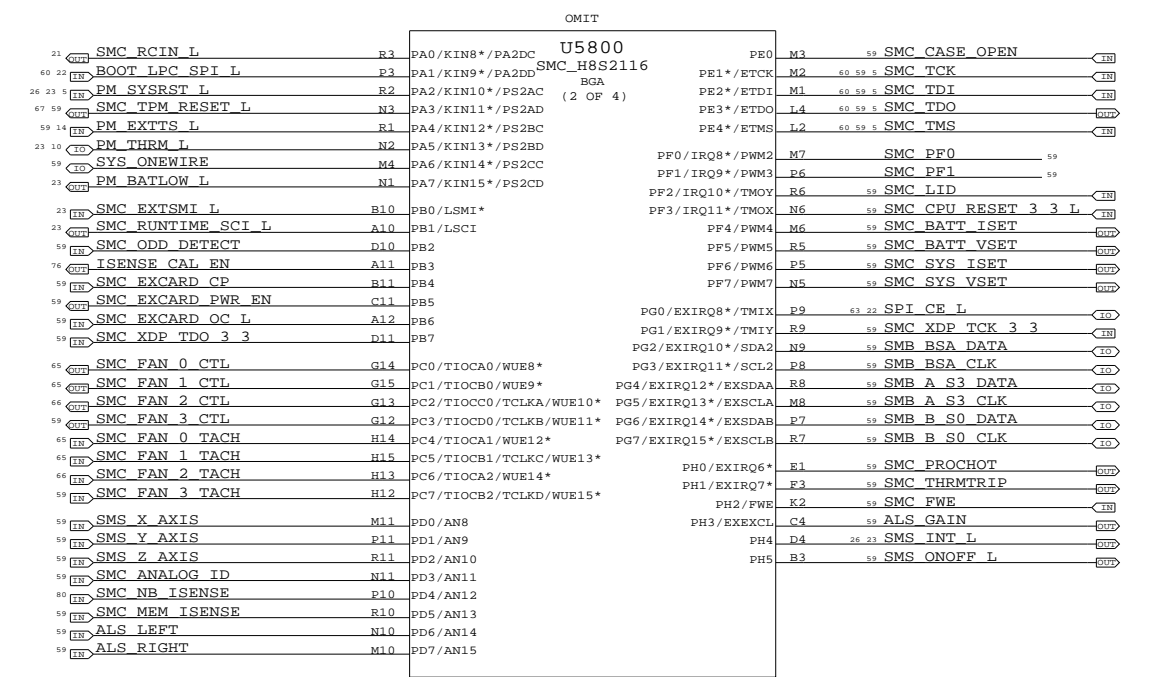
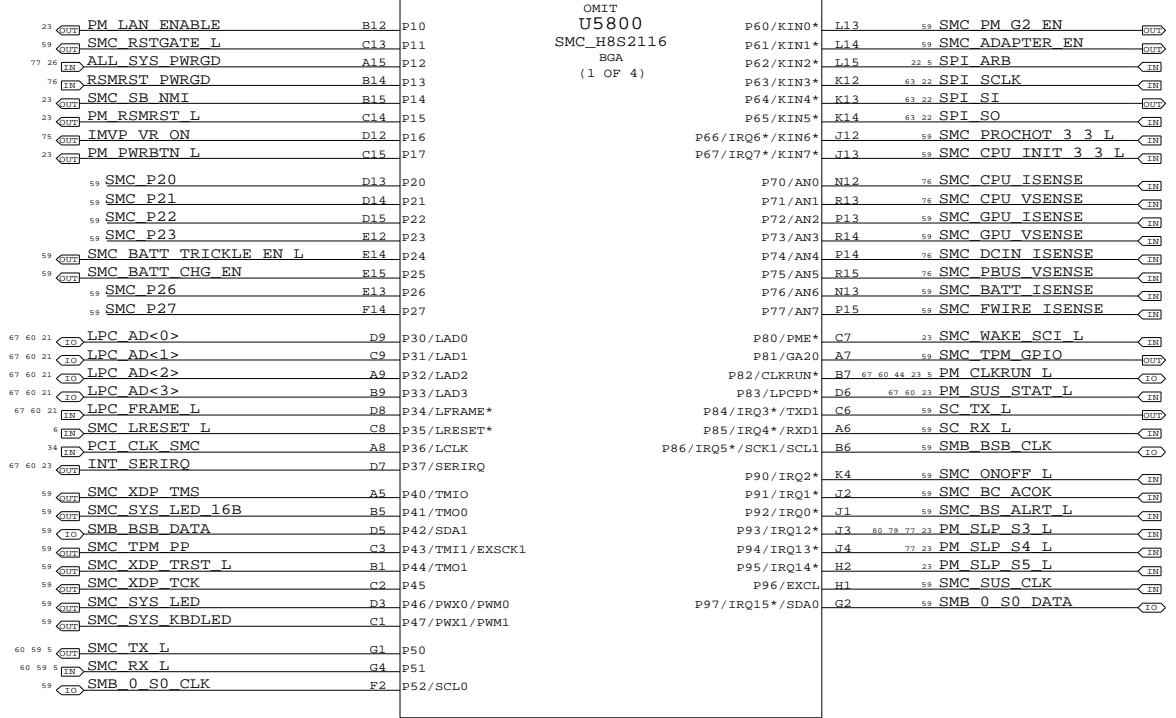
USED PCIE PORTS

22	IN	PCIE A R2D C N	==	PCIE AIRPORT R2D C N	53
		MAKE_BASE=TRUE			
22	IN	PCIE A R2D C P	==	PCIE AIRPORT R2D C P	53
		MAKE_BASE=TRUE			
22 5	OUT	PCIE A D2R N	==	PCIE AIRPORT D2R N	53
		MAKE_BASE=TRUE			
22 5	OUT	PCIE A D2R P	==	PCIE AIRPORT D2R P	53
		MAKE_BASE=TRUE			
22	IN	PCIE B R2D C N	==	PCIE ENET R2D C N	41
		MAKE_BASE=TRUE			
22	IN	PCIE B R2D C P	==	PCIE ENET R2D C P	41
		MAKE_BASE=TRUE			
22 5	OUT	PCIE B D2R N	==	PCIE ENET D2R N	41
		MAKE_BASE=TRUE			
22 5	OUT	PCIE B D2R P	==	PCIE ENET D2R P	41
		MAKE_BASE=TRUE			

PCIE PORT ALIASES
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7032	B
	SCALE	SHT	OF
	NONE	54	97

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



SMC

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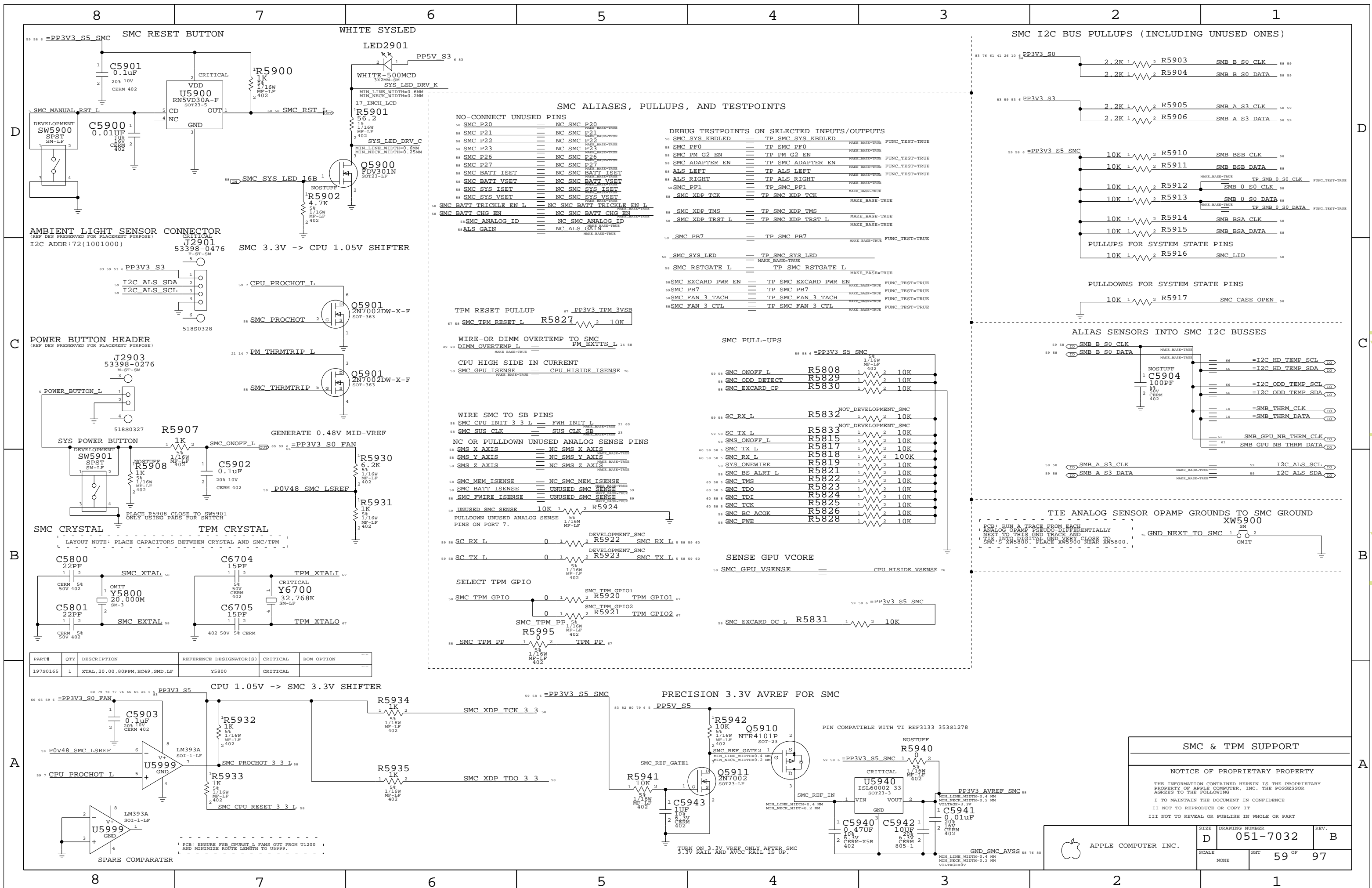
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	D	051-7032	B
SCALE	SHT	58 OF	97
NONE			

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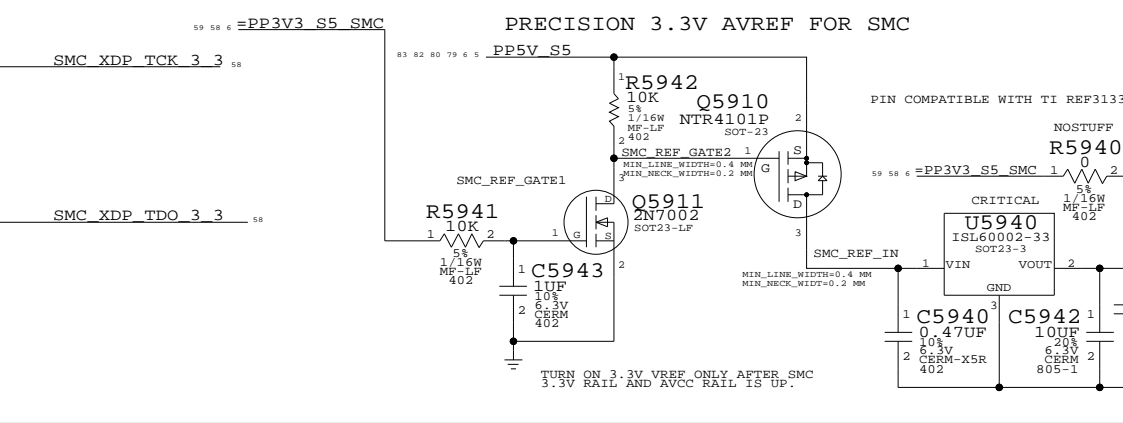
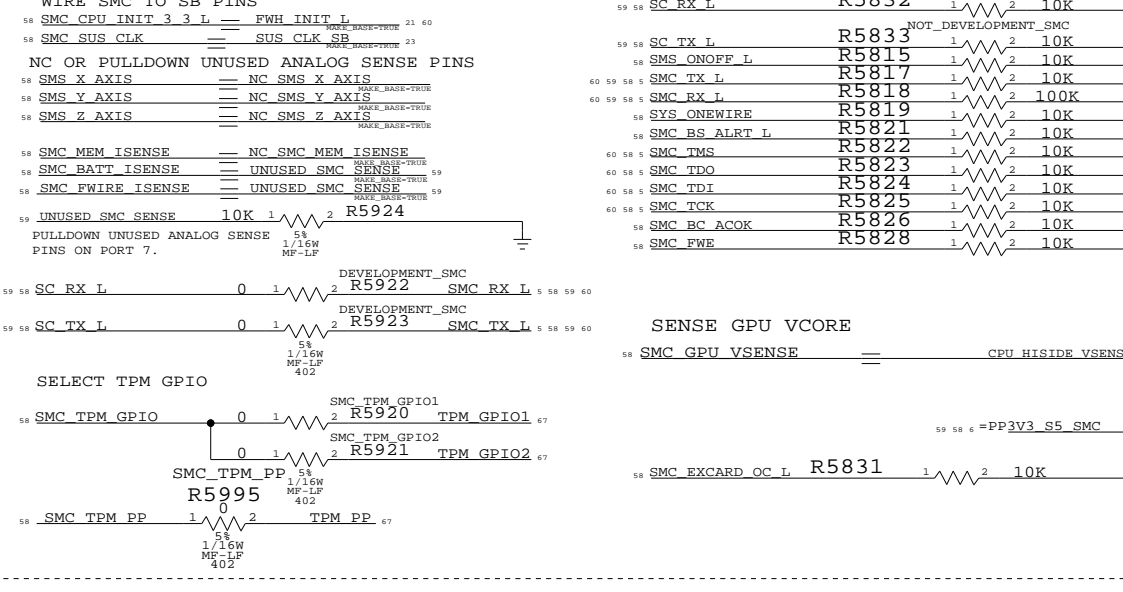


SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
58 SMC P20 == NC SMC P20	58 SMC SYS_KBDLED == TP_SMC_SYS_KBDLED MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P21 == NC SMC P21	58 SMC PF0 == TP_SMC_PF0 MAKE_BASE=TRUE
58 SMC P22 == NC SMC P22	58 SMC_PM_G2_EN == TP_SMC_PM_G2_EN MAKE_BASE=TRUE
58 SMC P23 == NC SMC P23	58 SMC_ADAPTER_EN == TP_SMC_ADAPTER_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P26 == NC SMC P26	58 ALS_LEFT == TP_SMC_ALS_LEFT MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC P27 == NC SMC P27	58 ALS_RIGHT == TP_SMC_ALS_RIGHT MAKE_BASE=TRUE
58 SMC_BATT_ISET == NC SMC_BATT_ISET	58 SMC_PFI == TP_SMC_PFI MAKE_BASE=TRUE
58 SMC_BATT_VSET == NC SMC_BATT_VSET	58 SMC_XDP_TCK == TP_SMC_XDP_TCK MAKE_BASE=TRUE
58 SMC_SYS_ISET == NC SMC_SYS_ISET	58 SMC_XDP_TMS == TP_SMC_XDP_TMS MAKE_BASE=TRUE
58 SMC_SYS_VSET == NC SMC_SYS_VSET	58 SMC_XDP_TRST_L == TP_SMC_XDP_TRST_L MAKE_BASE=TRUE
58 SMC_BATT_TRICKLE_EN_L == NC SMC_BATT_TRICKLE_EN_L	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
58 SMC_BATT_CHG_EN == NC SMC_BATT_CHG_EN	58 SMC_SYS_LED == TP_SMC_SYS_LED MAKE_BASE=TRUE
58 SMC_ANALOG_ID == NC SMC_ANALOG_ID	58 SMC_RSTGATE_L == TP_SMC_RSTGATE_L MAKE_BASE=TRUE
58 ALS_GAIN == NC ALS_GAIN MAKE_BASE=TRUE	58 SMC_EXCARD_PWR_EN == TP_SMC_EXCARD_PWR_EN MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_PB7 == TP_SMC_PB7 MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_TACH == TP_SMC_FAN_3_TACH MAKE_BASE=TRUE FUNC_TEST=TRUE
	58 SMC_FAN_3_CTL == TP_SMC_FAN_3_CTL MAKE_BASE=TRUE FUNC_TEST=TRUE

SMC PULL-UPS

58 SMC_ONOFF_L	R5808	10K
58 SMC_ODD_DETECT	R5829	10K
58 SMC_EXCARD_CP	R5830	10K
58 SC_RX_L	R5832	10K
58 SC_TX_L	R5833	10K
58 SMS_ONOFF_L	R5815	10K
58 SMC_TX_L	R5817	10K
58 SMC_RX_L	R5818	100K
58 SYS_ONEWIRE	R5819	10K
58 SMC_BS_ALERT_L	R5821	10K
58 SMC_TMS	R5822	10K
58 SMC_TDO	R5823	10K
58 SMC_TDI	R5824	10K
58 SMC_TCK	R5825	10K
58 SMC_BC_ACOK	R5826	10K
58 SMC_FWE	R5828	10K



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

SMC & TPM SUPPORT

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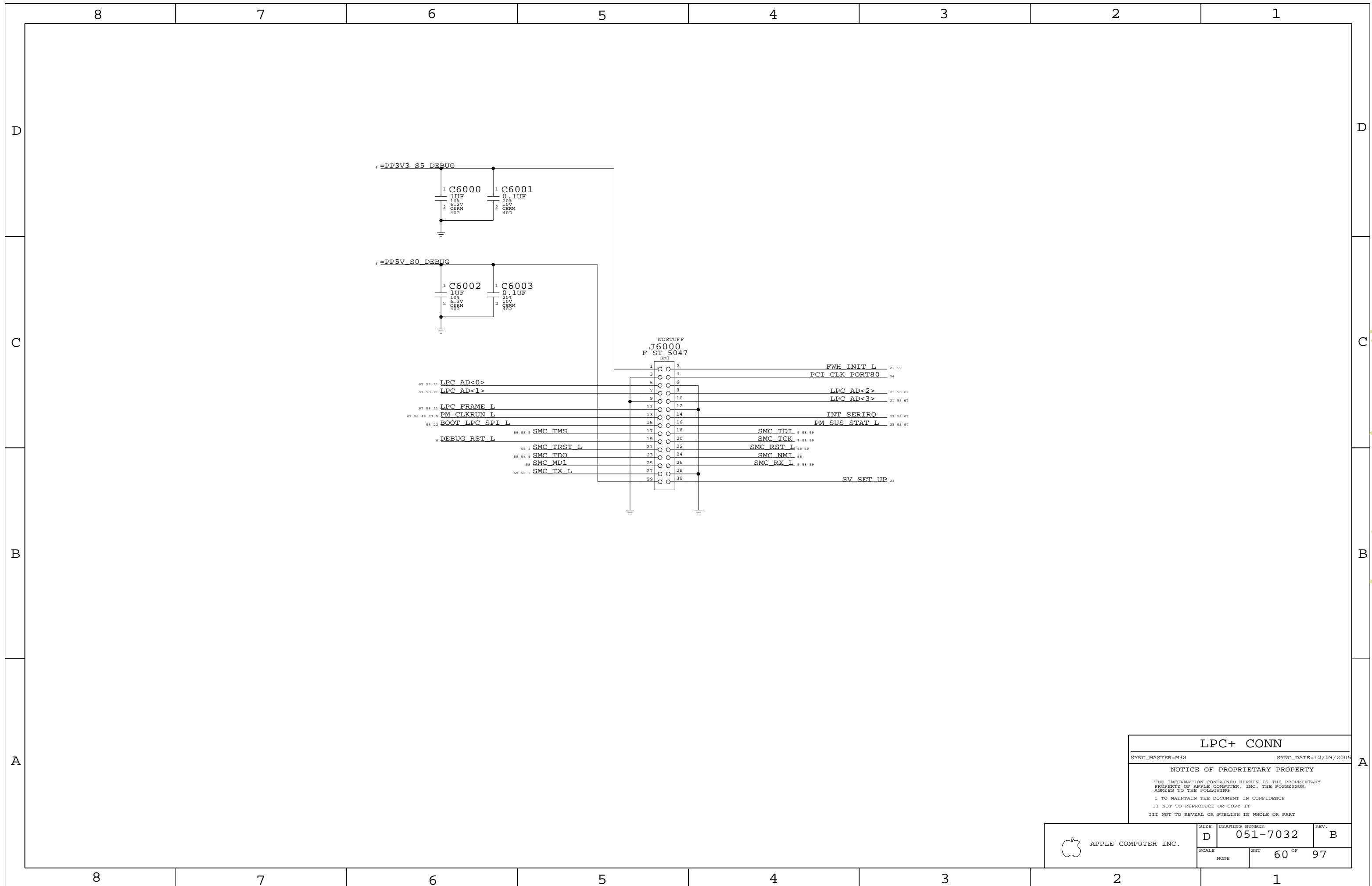
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SCALE	SHT	59 OF 97
NONE		

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LPC+ CONN

SYNC_MASTER=M38 SYNC_DATE=12/09/2005

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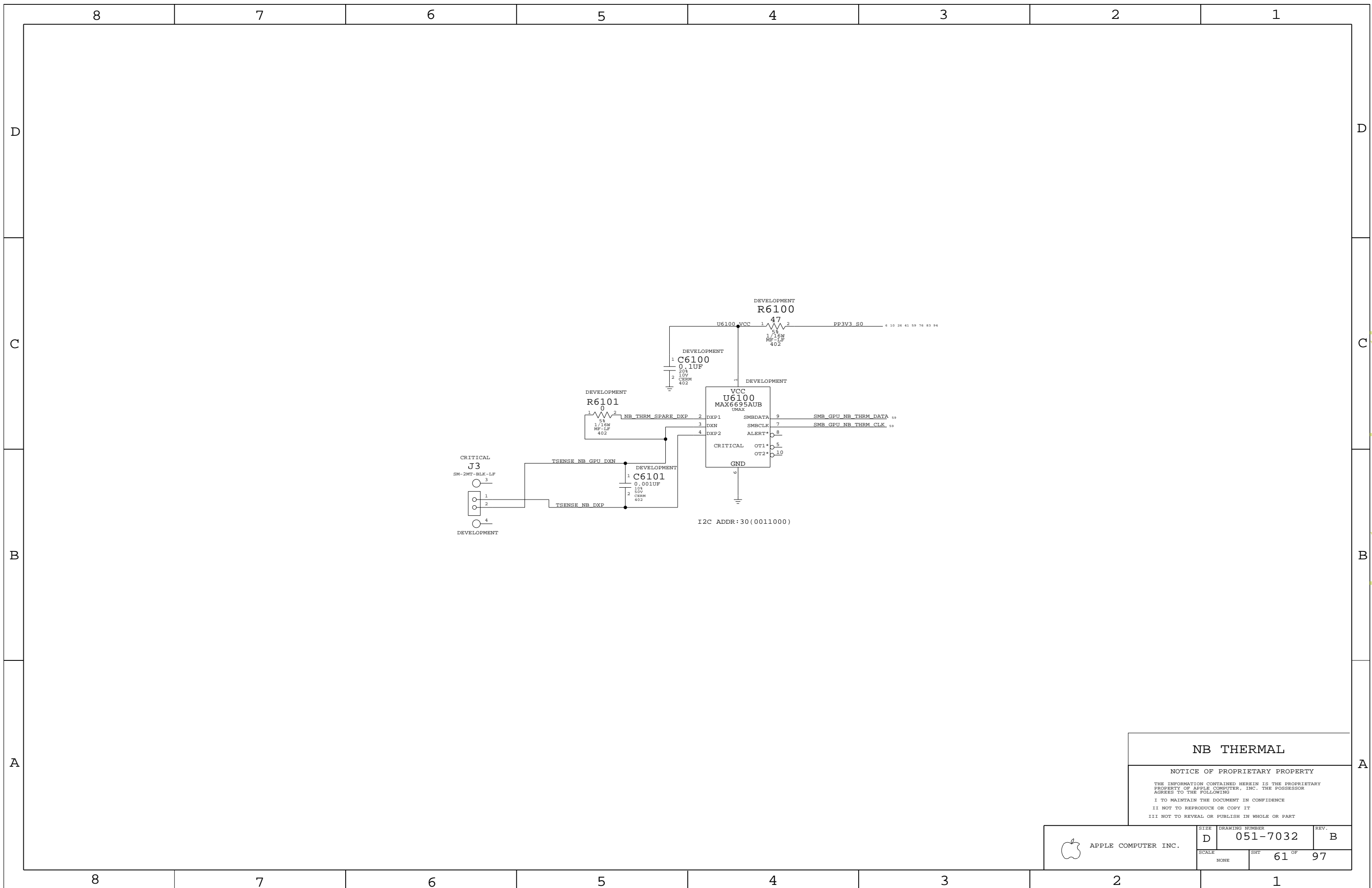
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	D	051-7032	B
SCALE	SHT	60 OF 97	
NONE			



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NB THERMAL

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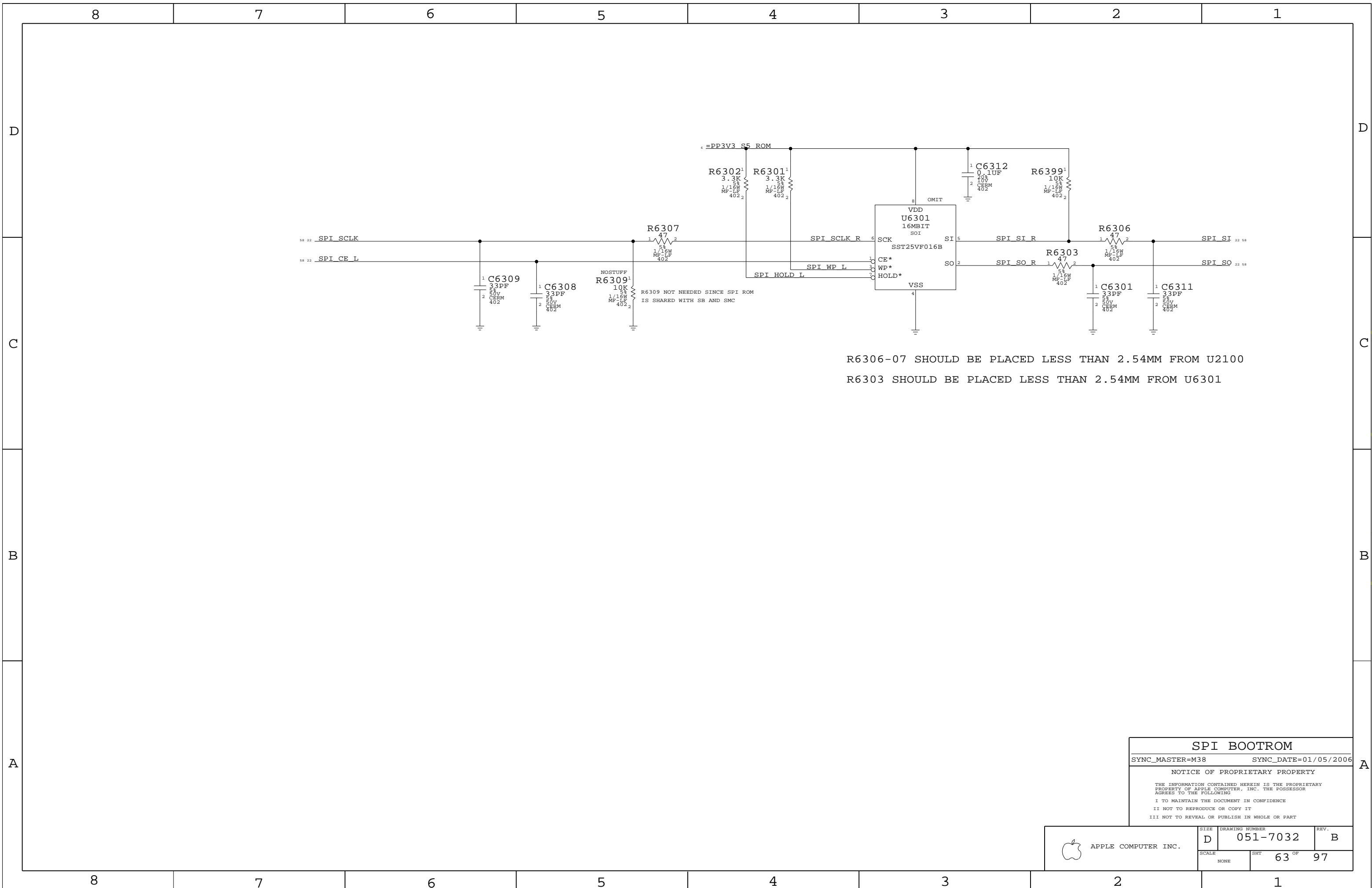
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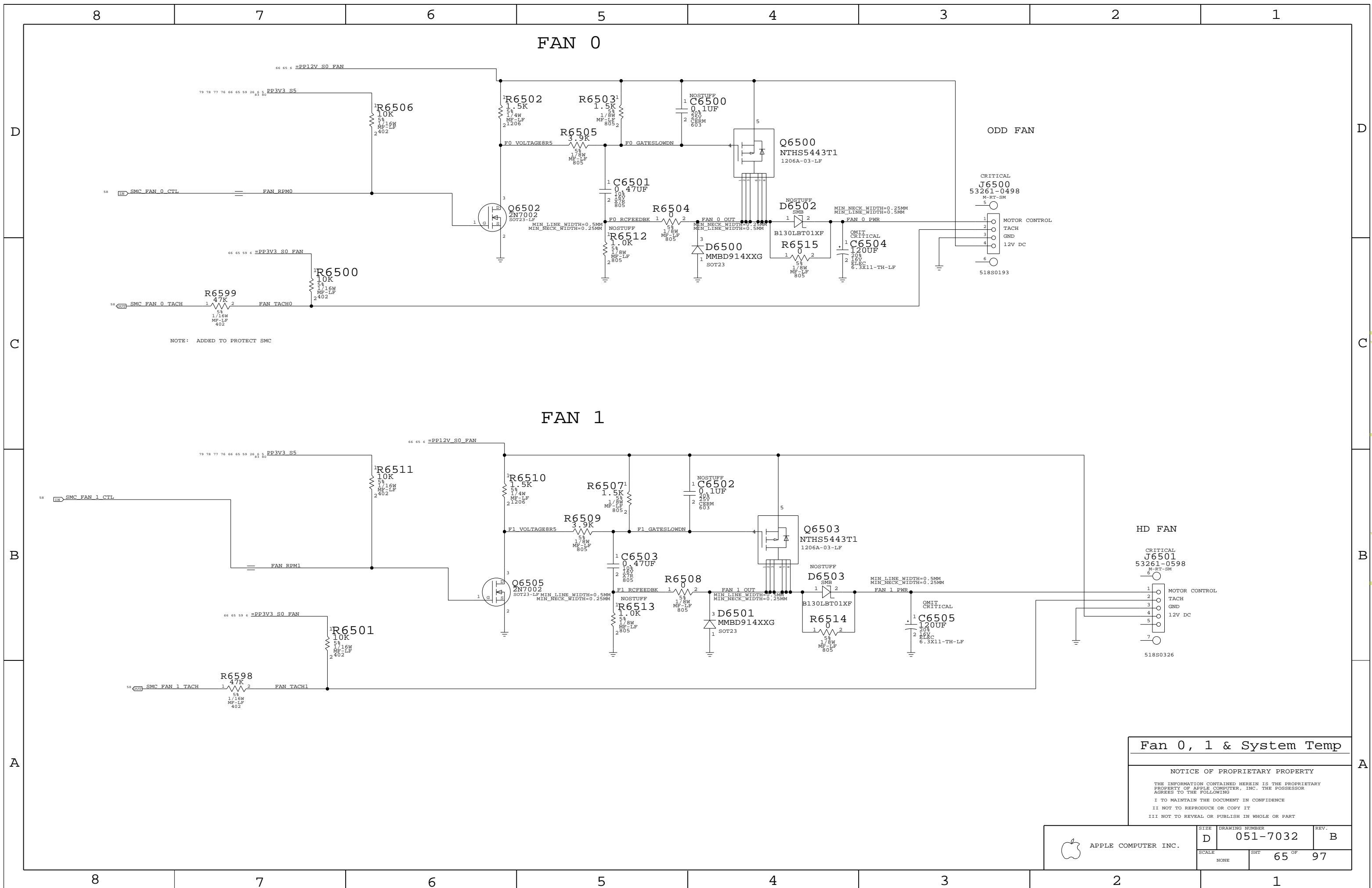
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 61 OF 97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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	D	051-7032	B
SCALE	SHT	63 OF 97	
NONE			



NOTE: ADDED TO PROTECT SMC

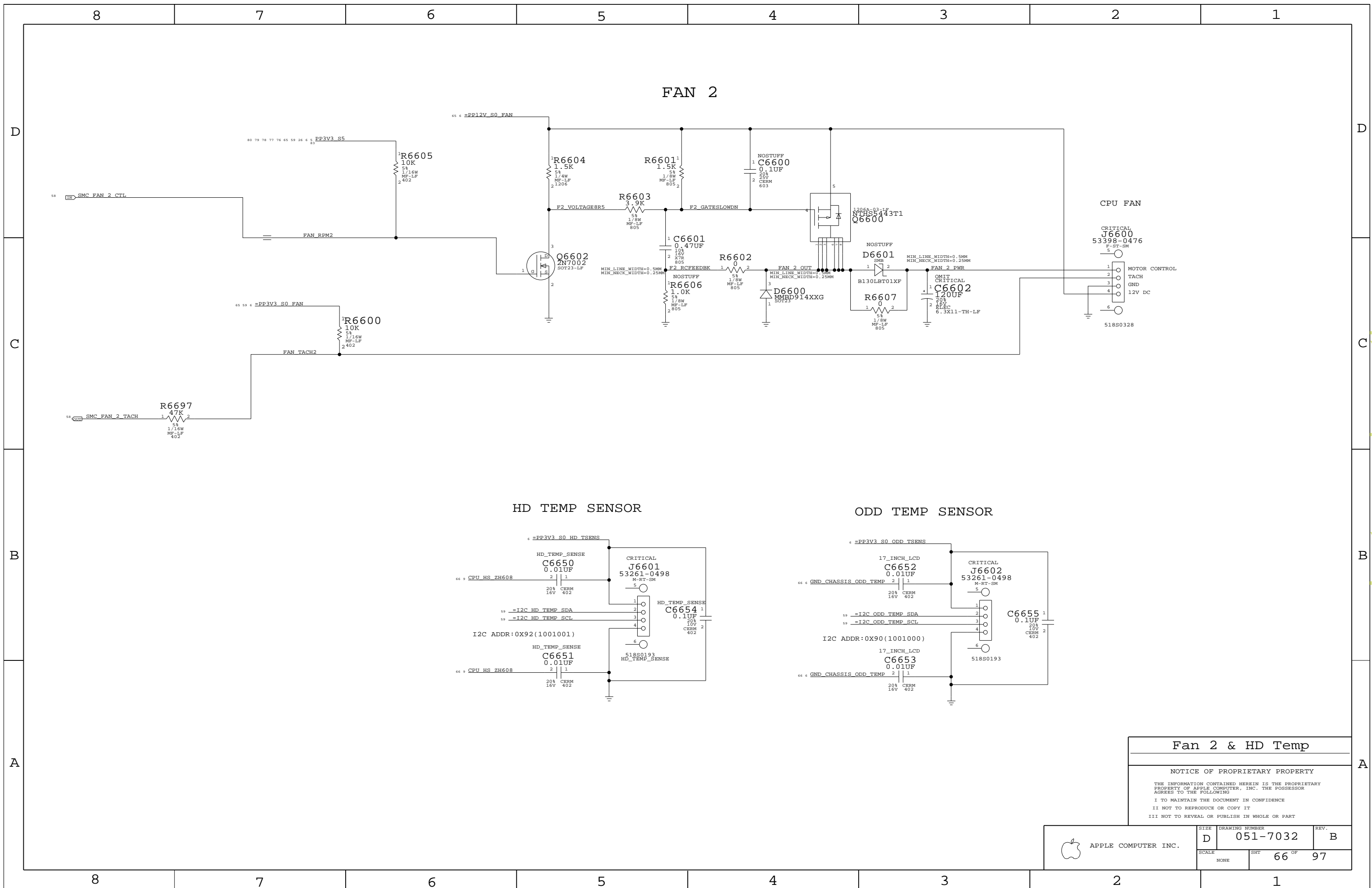
Fan 0, 1 & System Temp

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 65 OF 97	

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Fan 2 & HD Temp

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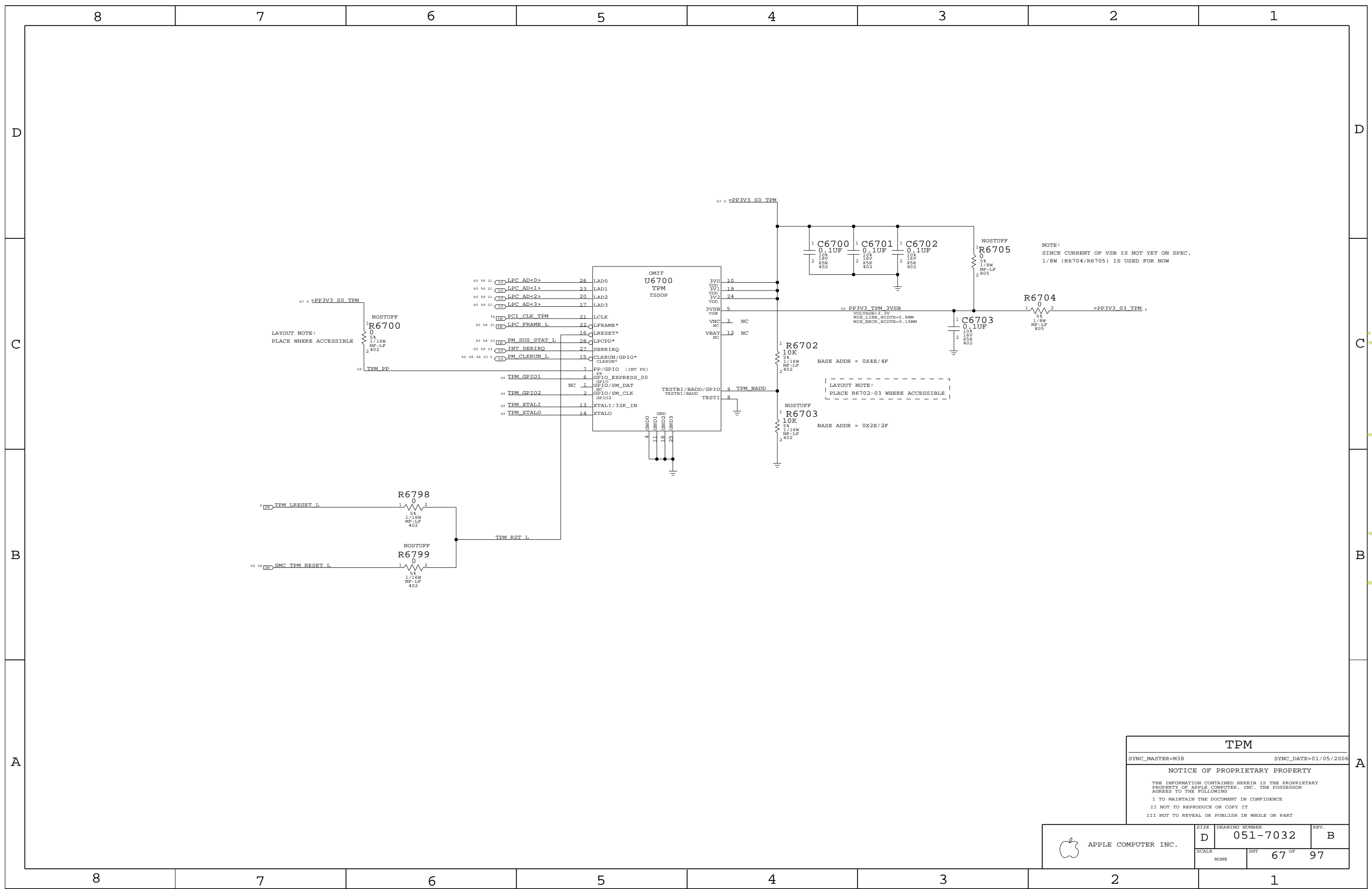
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 66 OF 97	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

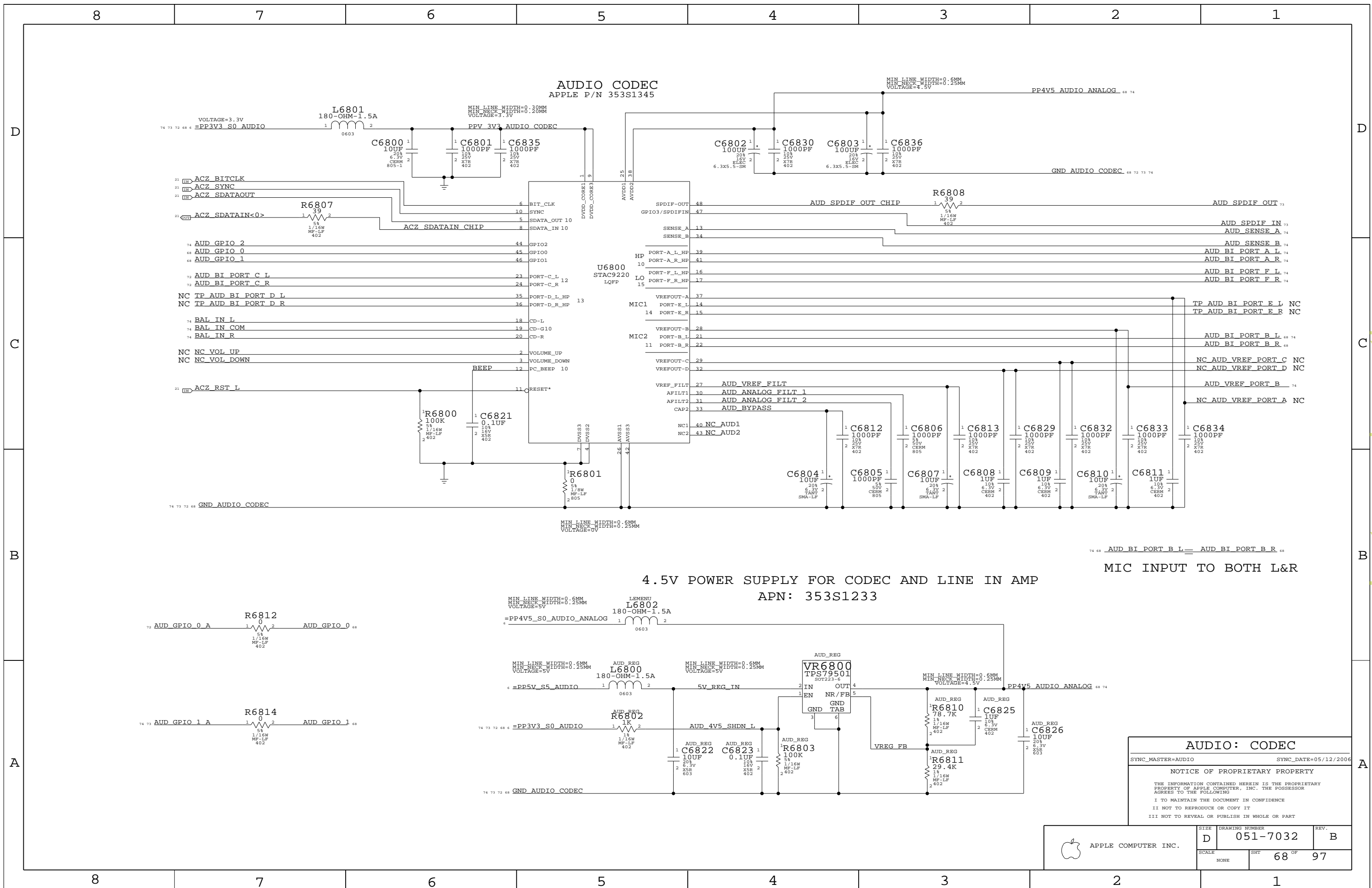
LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM	
SYNC_MASTER=M38	SYNC_DATE=01/05/2006
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	D	051-7032	B
SCALE	SHT	67 OF 97	
NONE			

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AUDIO: CODEC

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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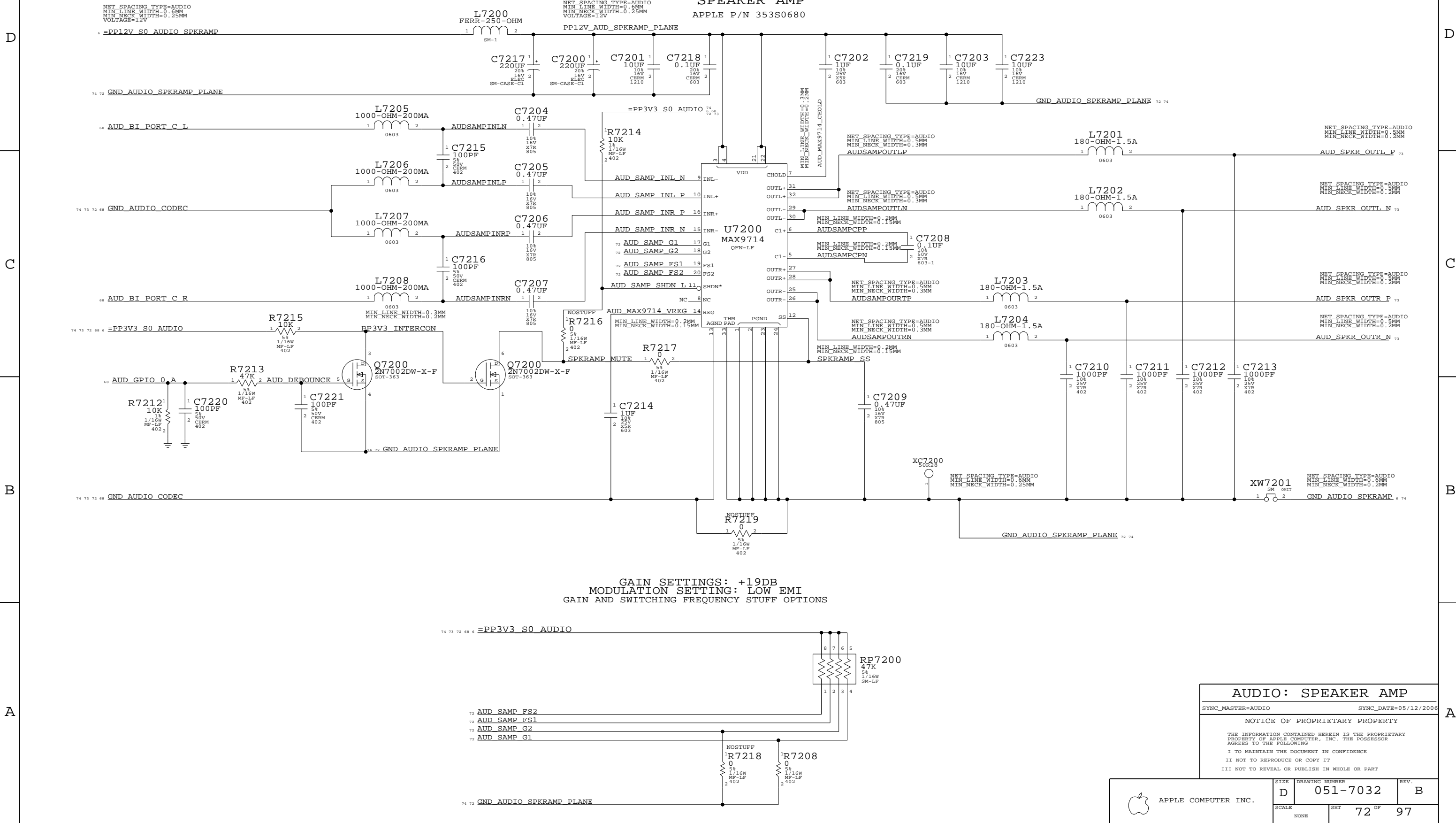
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III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	68 OF 97	
NONE			

SPEAKER AMP APPLE P/N 353S0680



AUDIO: SPEAKER AMP

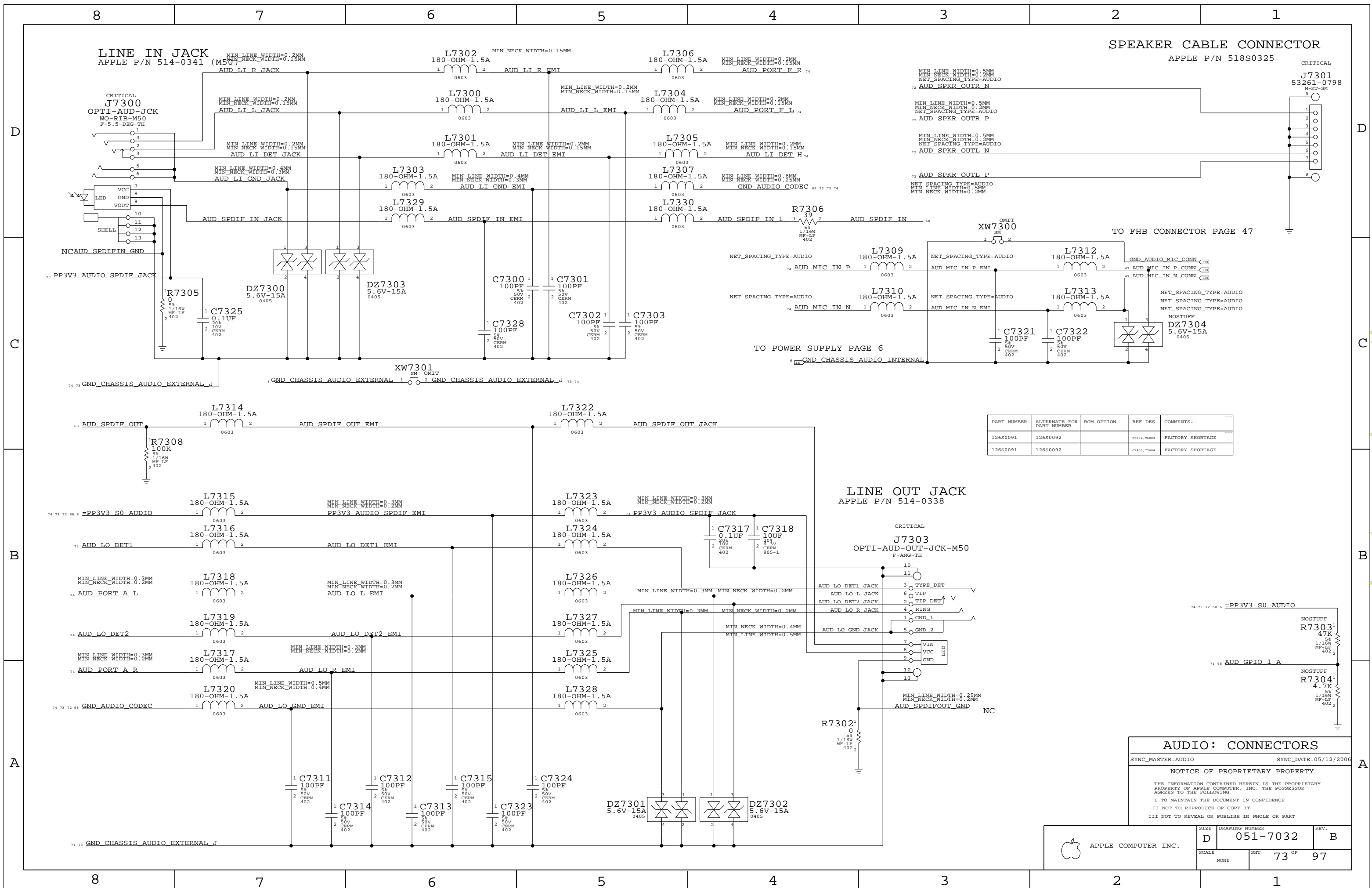
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 72 OF 97	

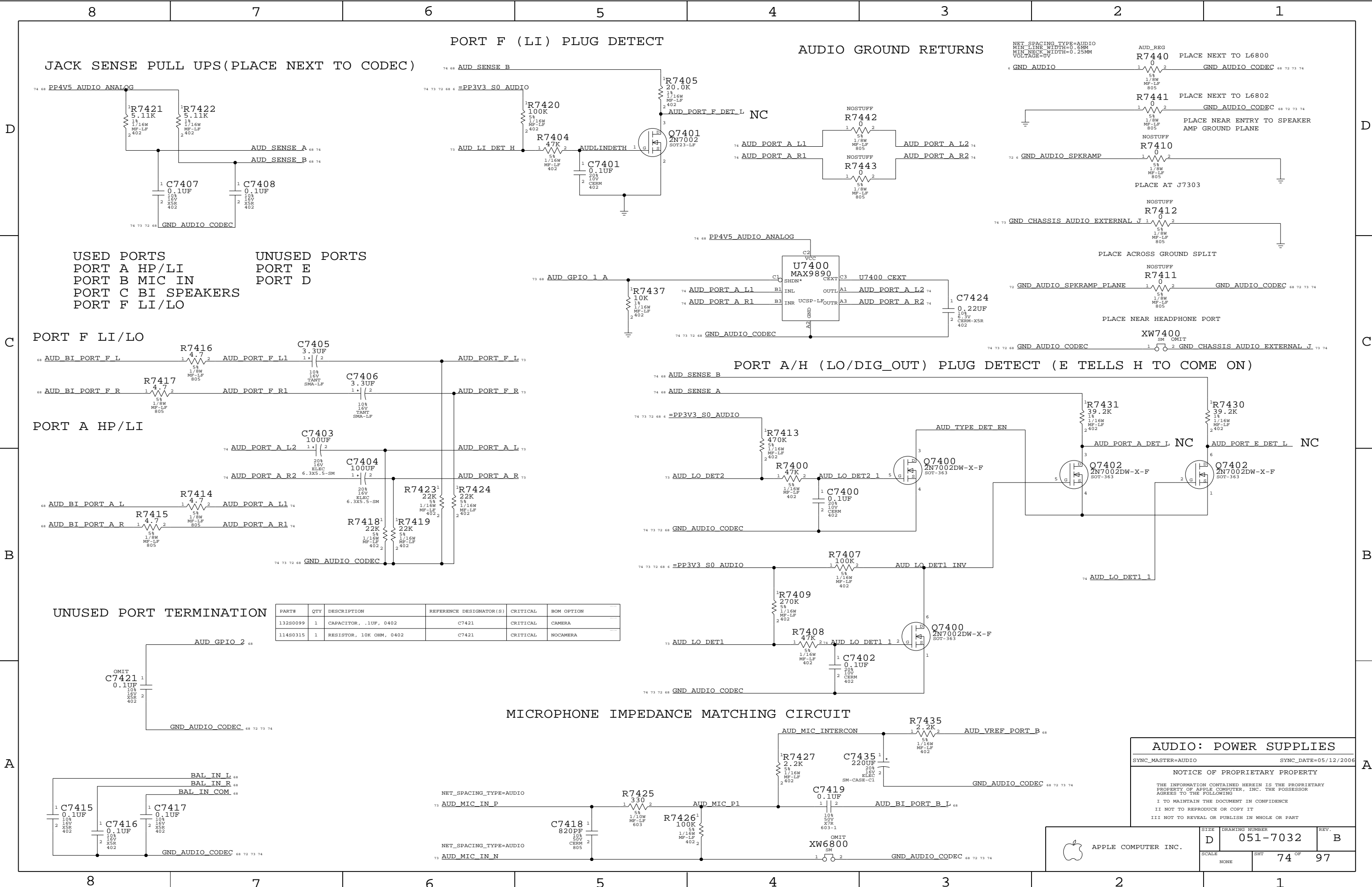


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
126S0091	126S0092		0802, 0803	FACTORY SHORTAGE
126S0091	126S0092		0743, 0744	FACTORY SHORTAGE

AUDIO: CONNECTORS
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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	D	051-7032	B
SCALE	SHT	73 OF	97
NONE			

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JACK SENSE PULL UPS (PLACE NEXT TO CODEC)

PORT F (LI) PLUG DETECT

AUDIO GROUND RETURNS

NET SPACING TYPE=AUDIO
MIN LINE WIDTH=0.6MM
MIN SPC WIDTH=0.25MM
VOLTAGE=0V

USED PORTS
PORT A HP/LI
PORT B MIC IN
PORT C BI SPEAKERS
PORT F LI/LO

UNUSED PORTS
PORT E
PORT D

PORT F LI/LO

PORT A HP/LI

UNUSED PORT TERMINATION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA

PORT A/H (LO/DIG_OUT) PLUG DETECT (E TELLS H TO COME ON)

MICROPHONE IMPEDANCE MATCHING CIRCUIT

AUDIO: POWER SUPPLIES

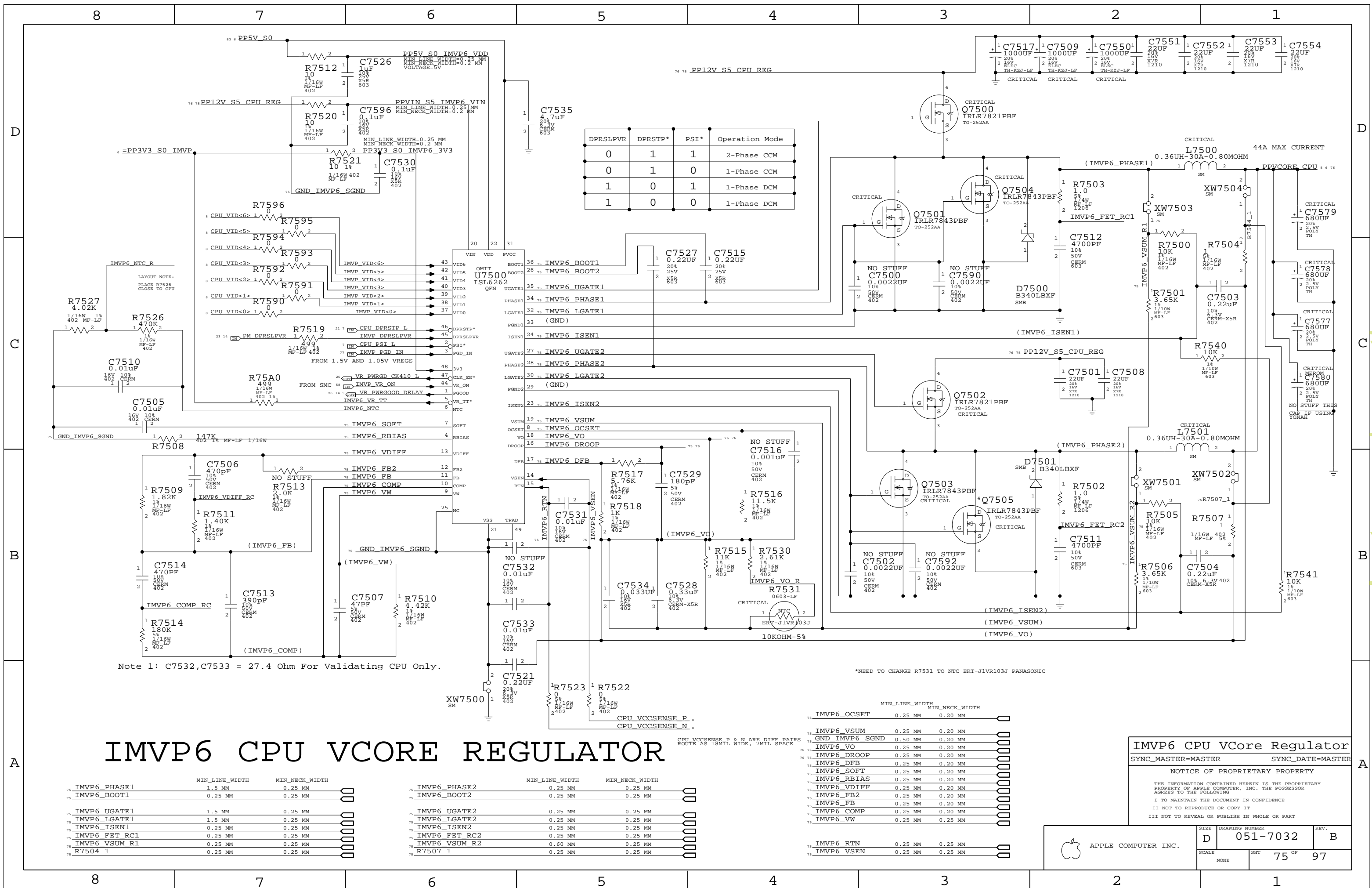
SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	74 OF	97
NONE			

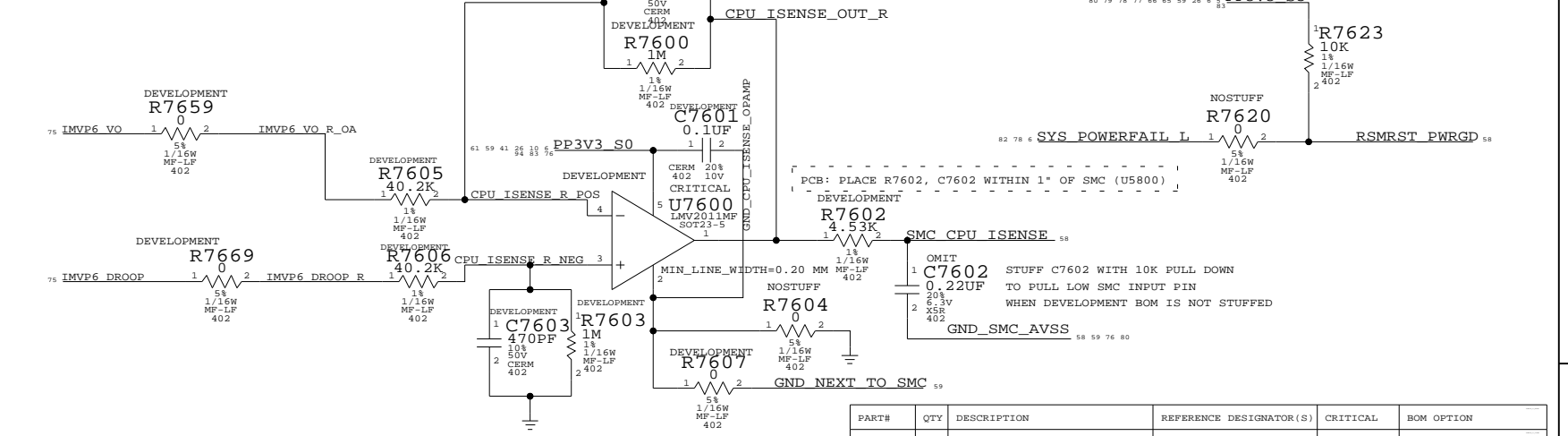
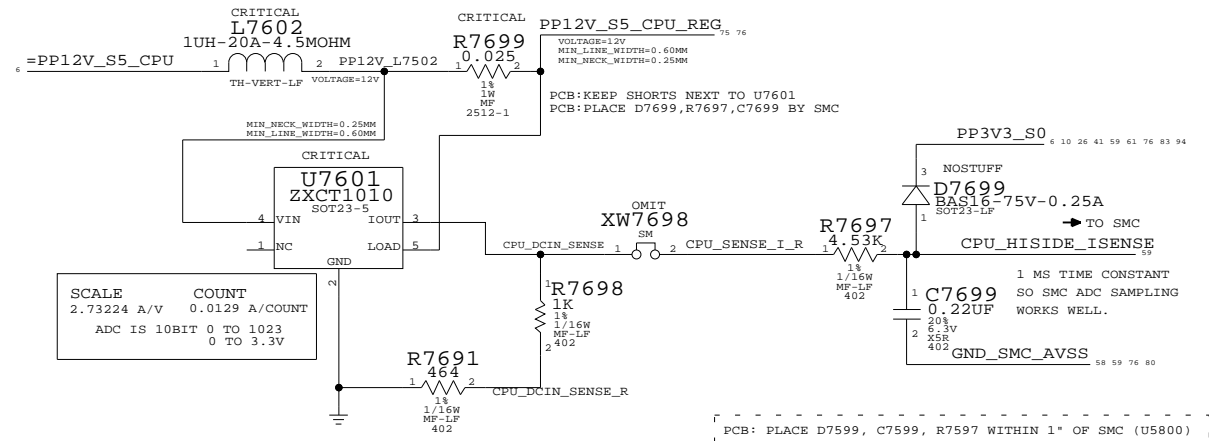
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PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

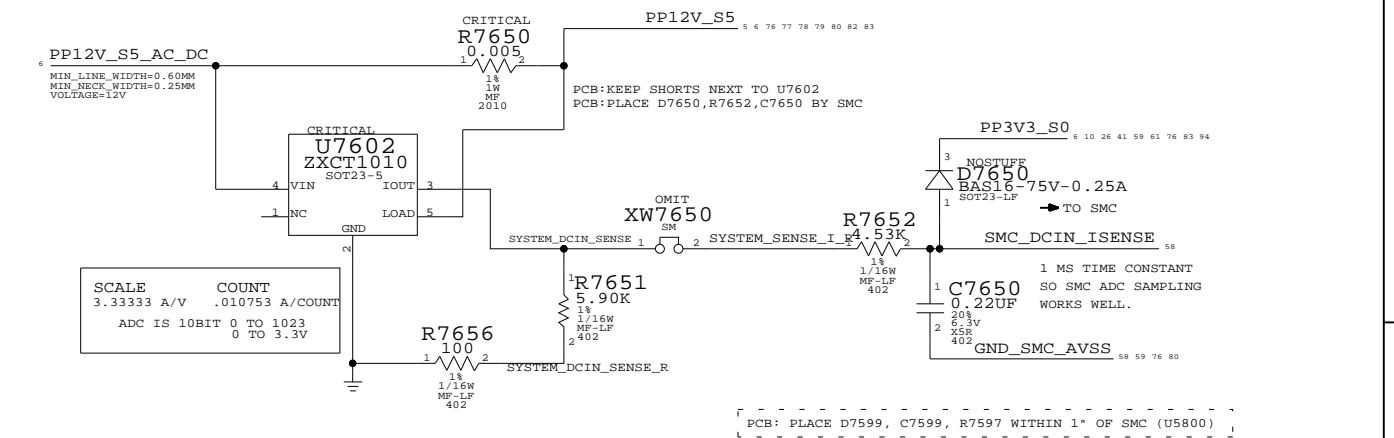
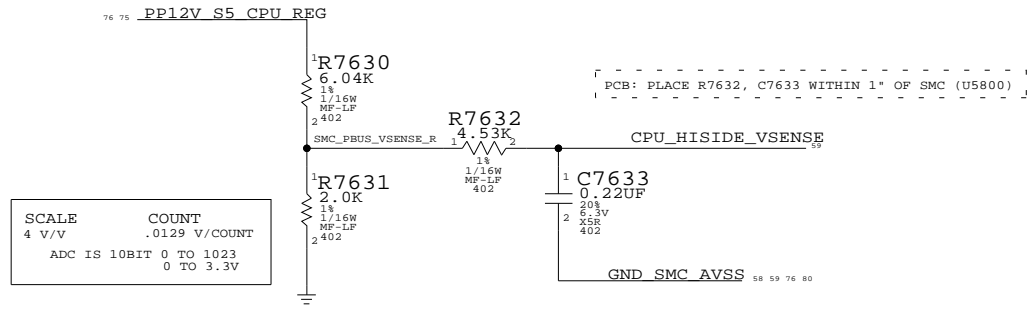
SMC PWRGD PULLUP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP,0.22UF,6.3V,20%,0402	C7602		DEVELOPMENT
116S0090	1	RES,10K,5%,0402	C7602		NOT_DEVELOPMENT

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

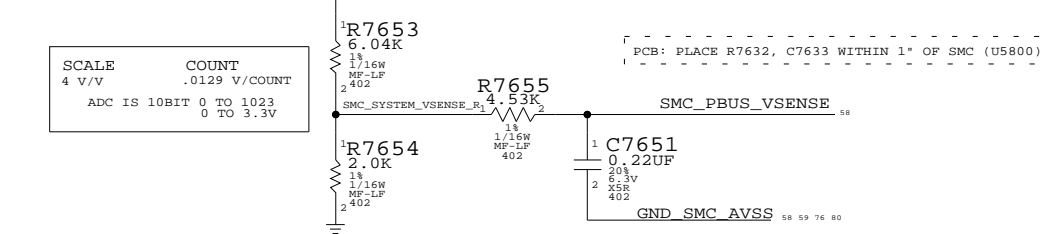
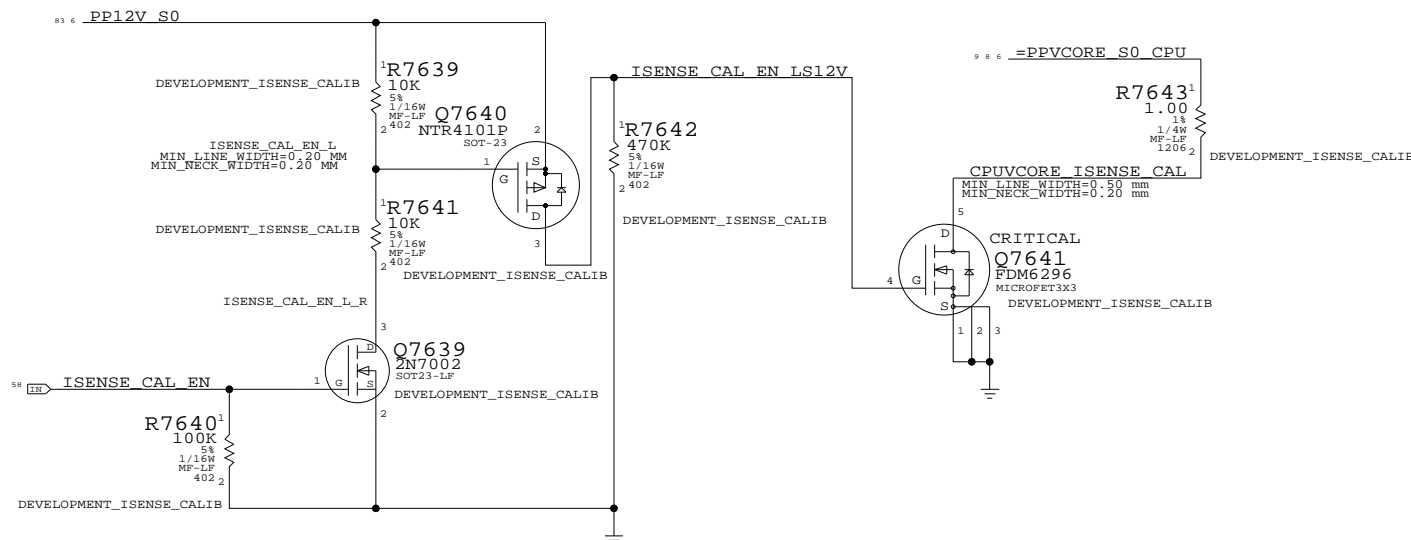
SYSTEM CURRENT SENSE



SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

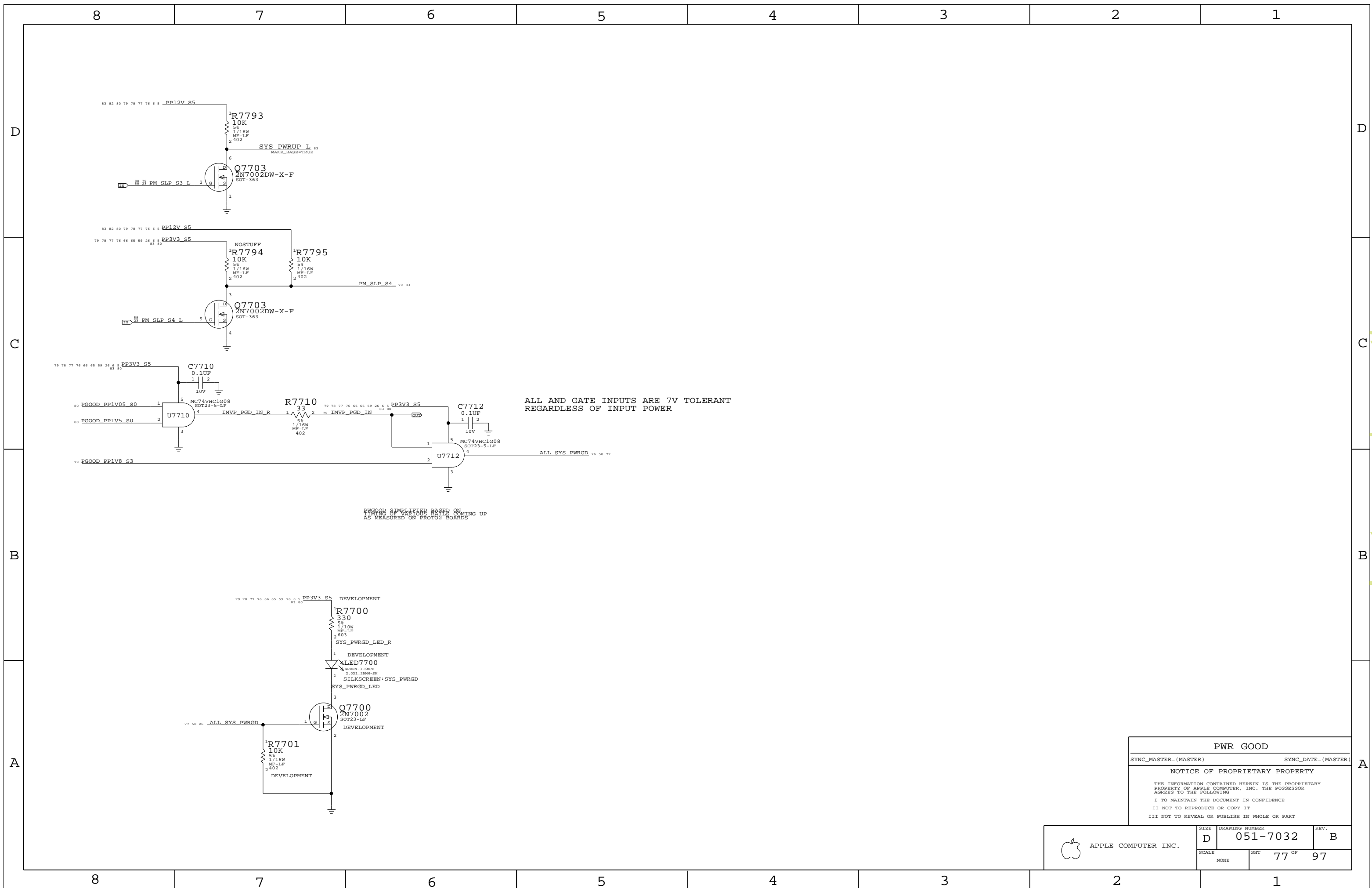
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	D	051-7032	B
SCALE	SHT	76 OF	97
NONE			



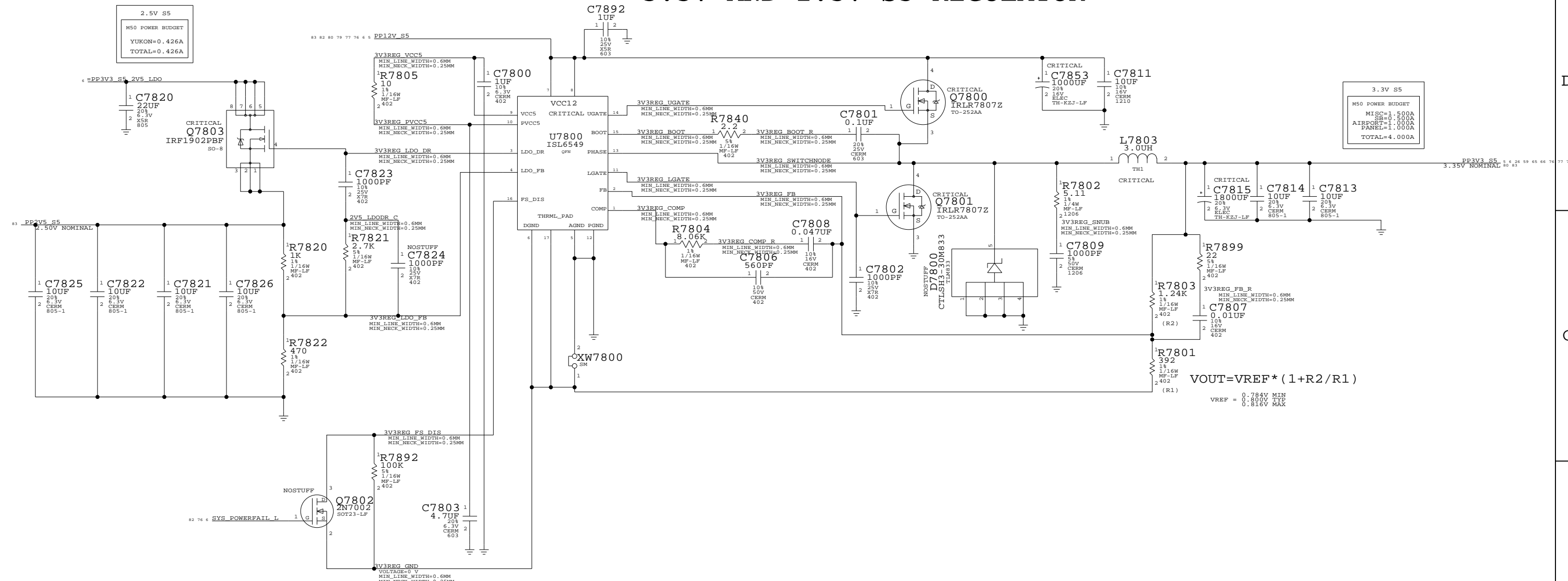
ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

PWGOOD SIMPLIFIED BASED ON
TIMING OF VARIOUS RAILS COMING UP
AS MEASURED ON PROTO2 BOARDS

PWR GOOD	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	77 OF	97
NONE			

3.3V AND 2.5V S5 REGULATOR



3V DC/DC 2.5V

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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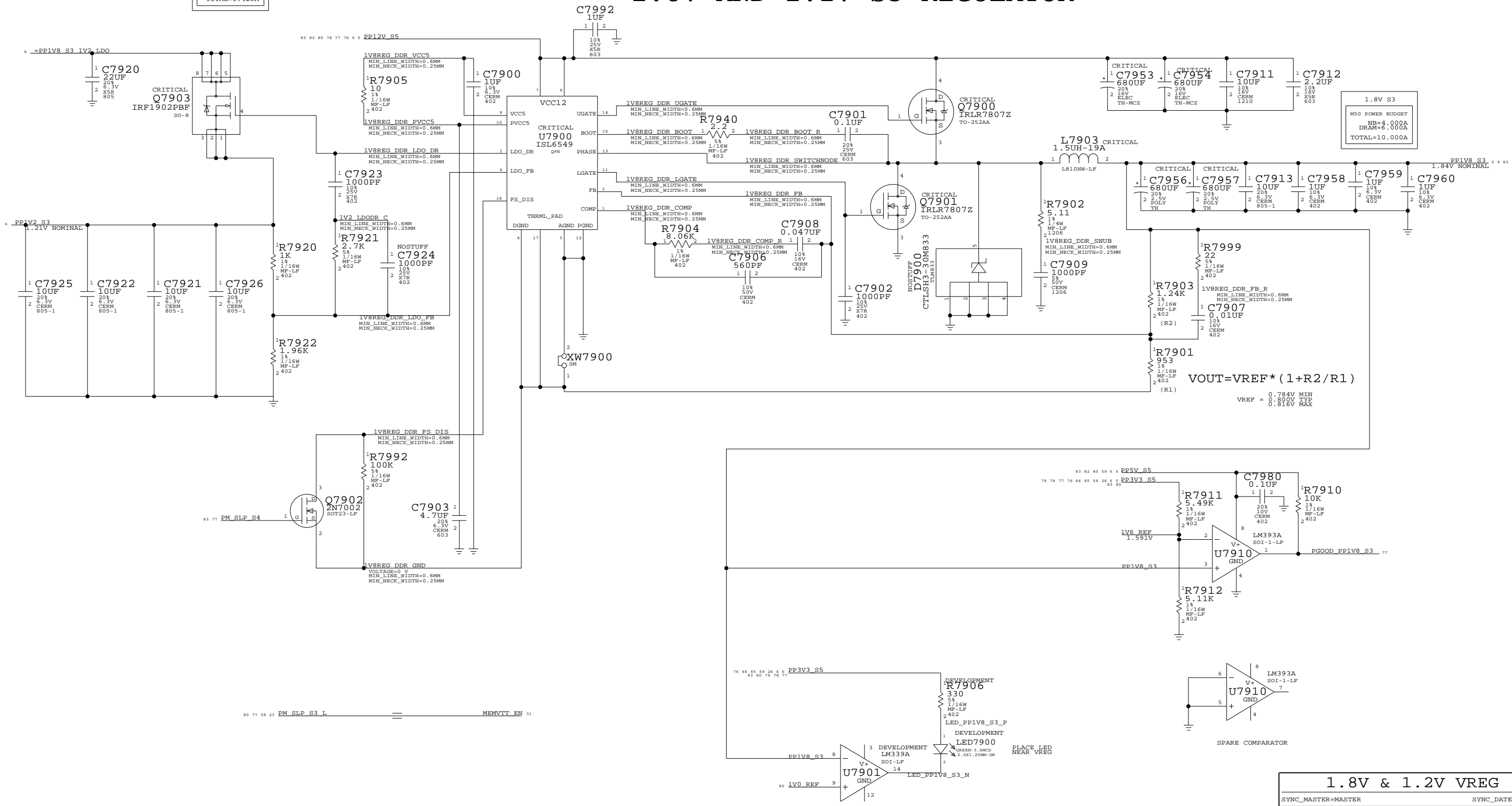
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHT 78 OF 97	

1.8V AND 1.2V S3 REGULATOR

1.2V S3
MS0 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
MS0 POWER BUDGET
NB=4.000A
DRAM=6.000A
TOTAL=10.000A



1.8V & 1.2V VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

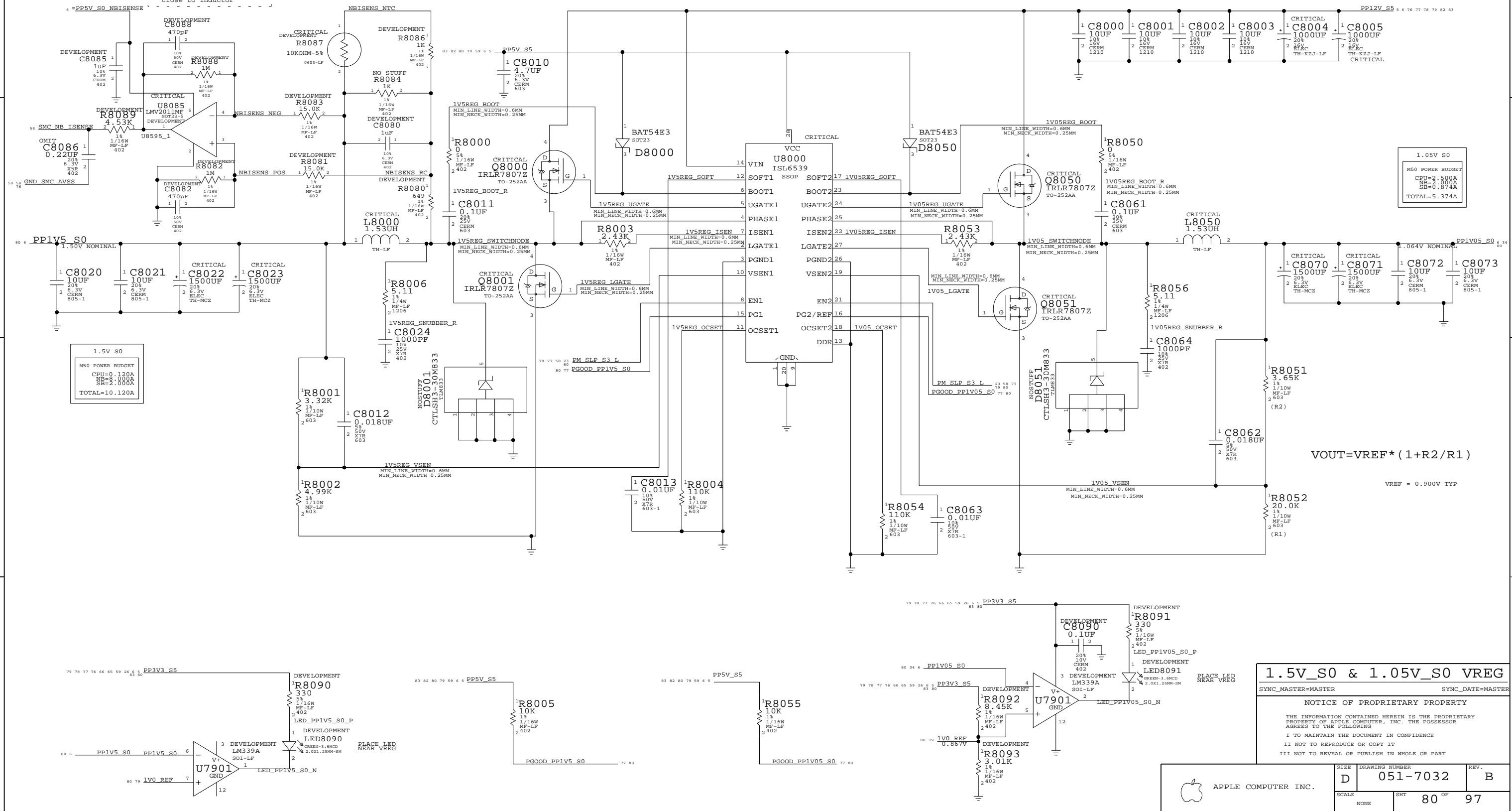
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	D	051-7032	B
SCALE	SHT	79 OF	97
NONE			

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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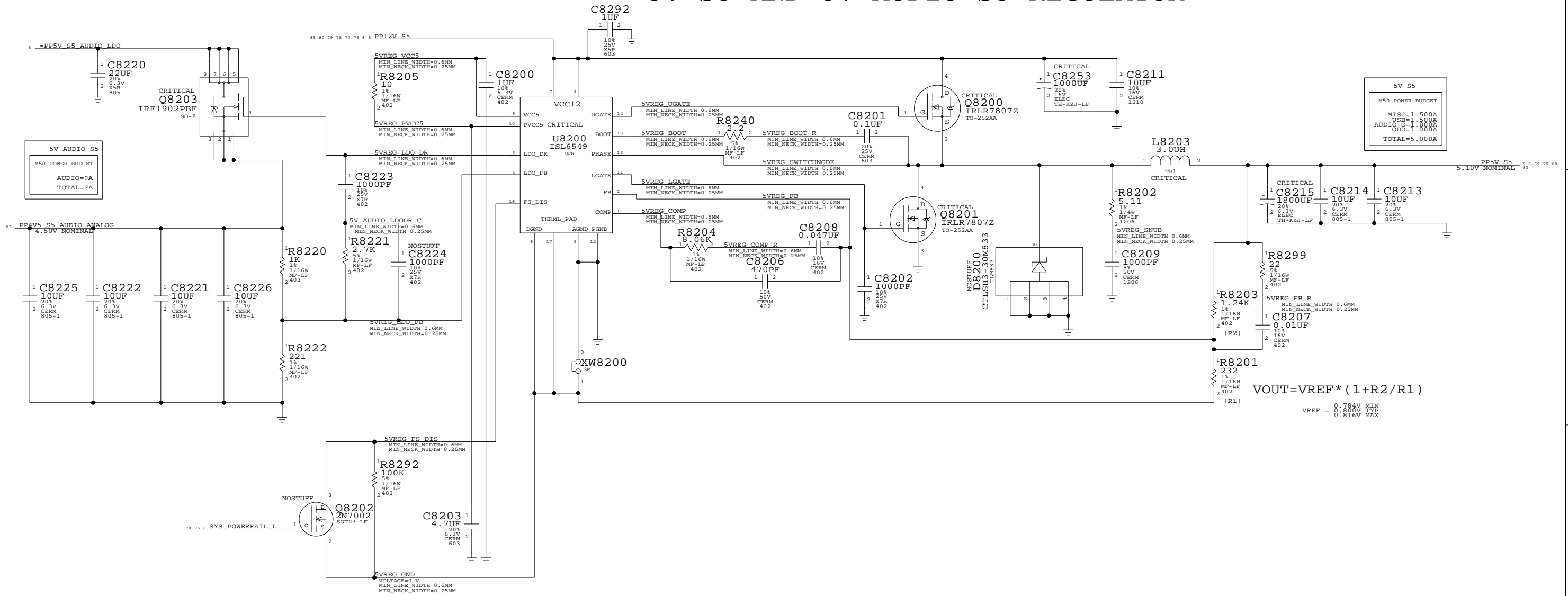
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7032	B
SCALE	SHT	80 OF	97
NONE			

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5V S5 AND 5V AUDIO S5 REGULATOR



5V S5	
MISC	=1.500A
USB	=1.500A
AUDIO_ODD	=1.000A
TOTAL	=5.000A

5V AUDIO S5	
MISC	=7A
TOTAL	=7A

$V_{OUT} = V_{REF} * (1 + R2/R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$

POWER SUPPLY 3.3V/5V MAIN SWITCH

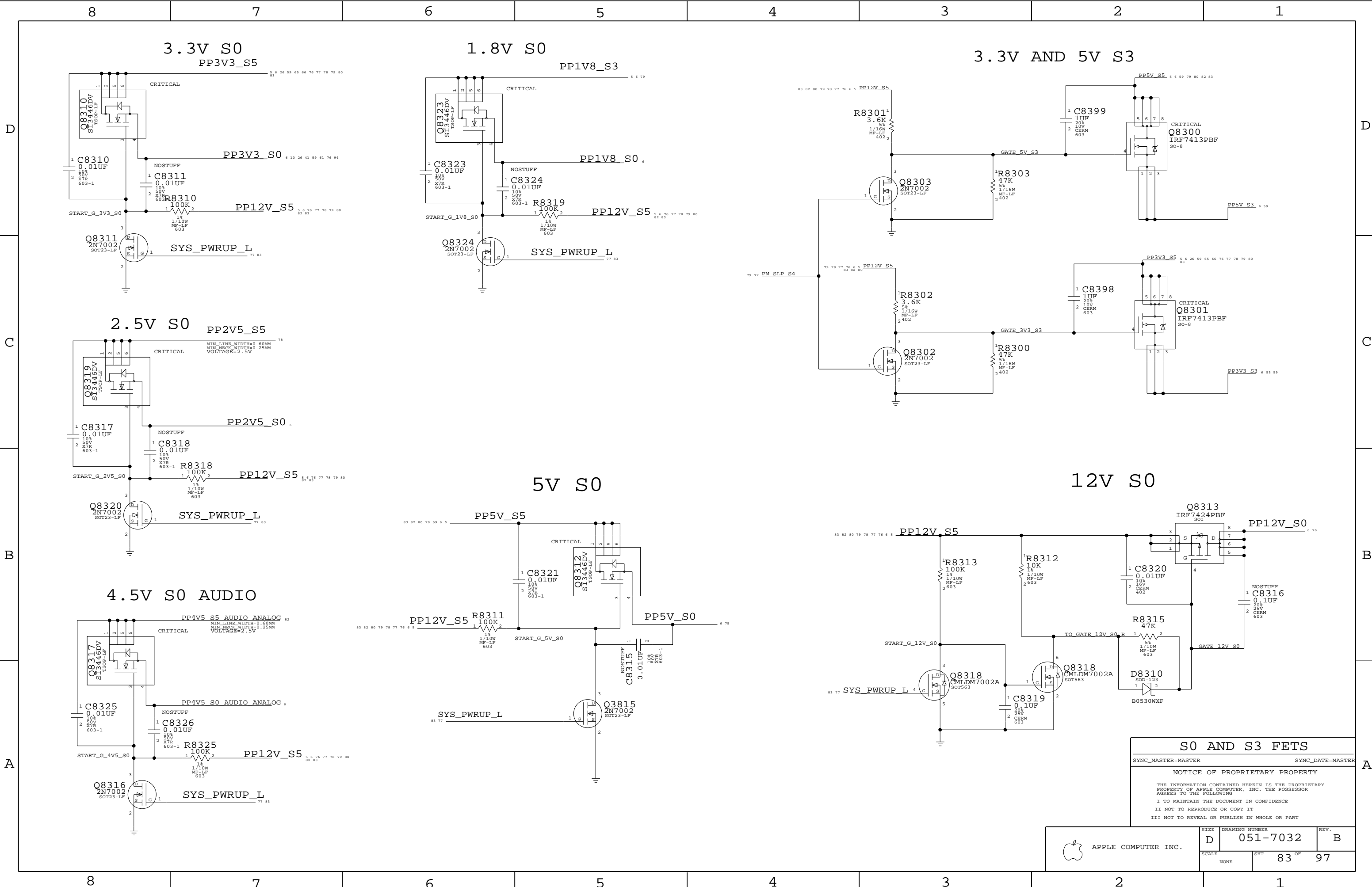
5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7032	B
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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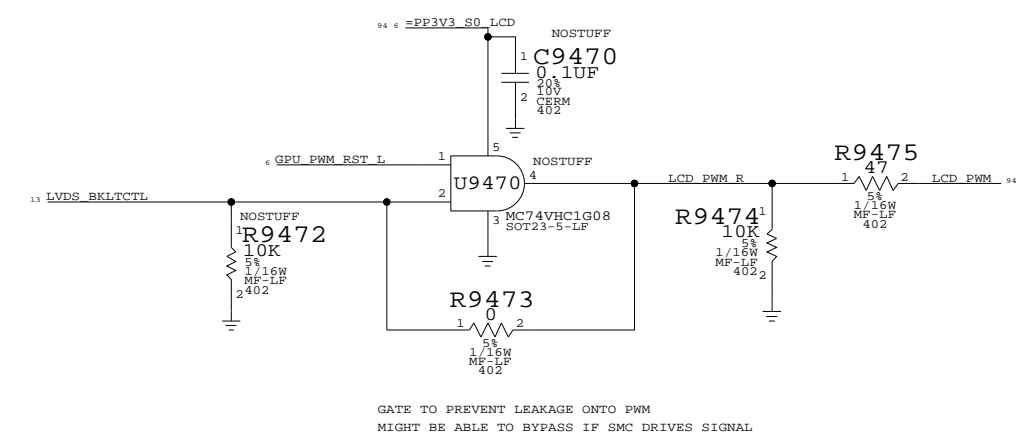
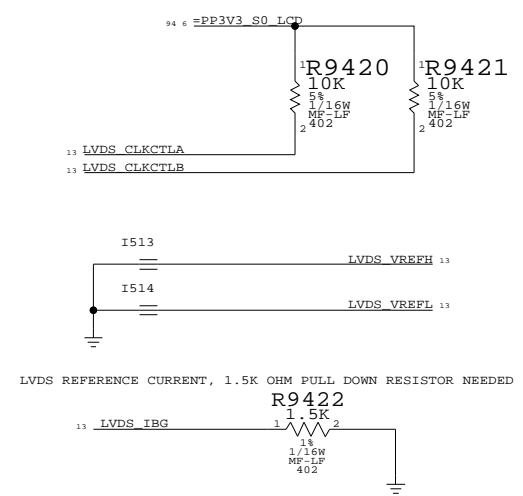
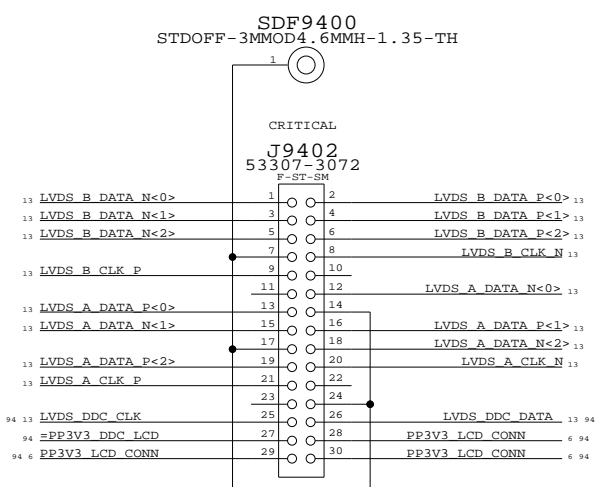
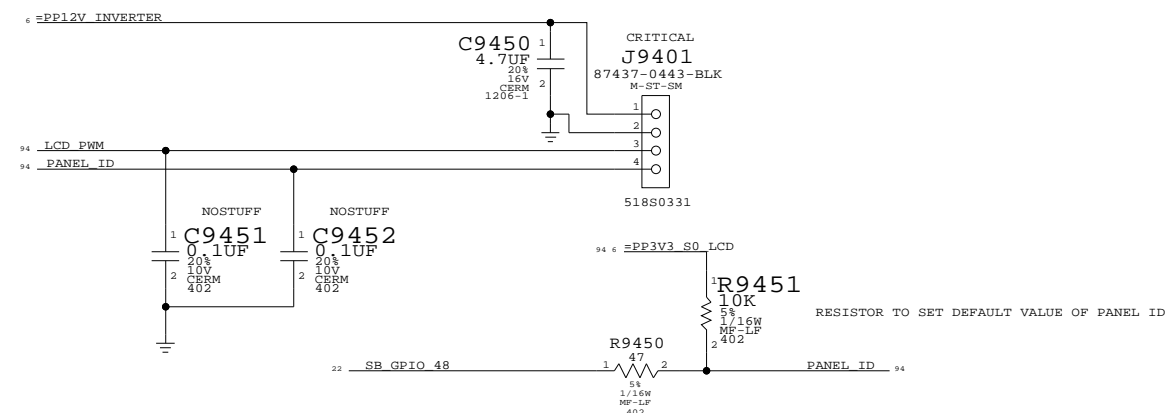
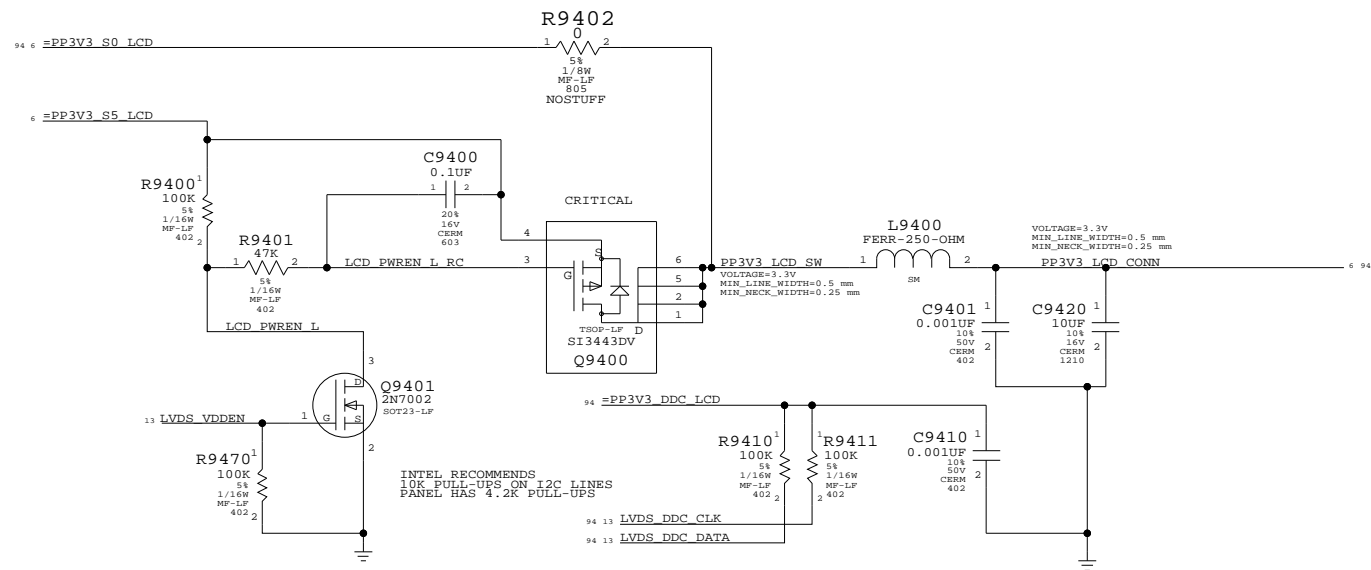
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	D	051-7032	B
SCALE	SHT	83 OF	97
NONE			

LCD (LVDS) INTERFACE

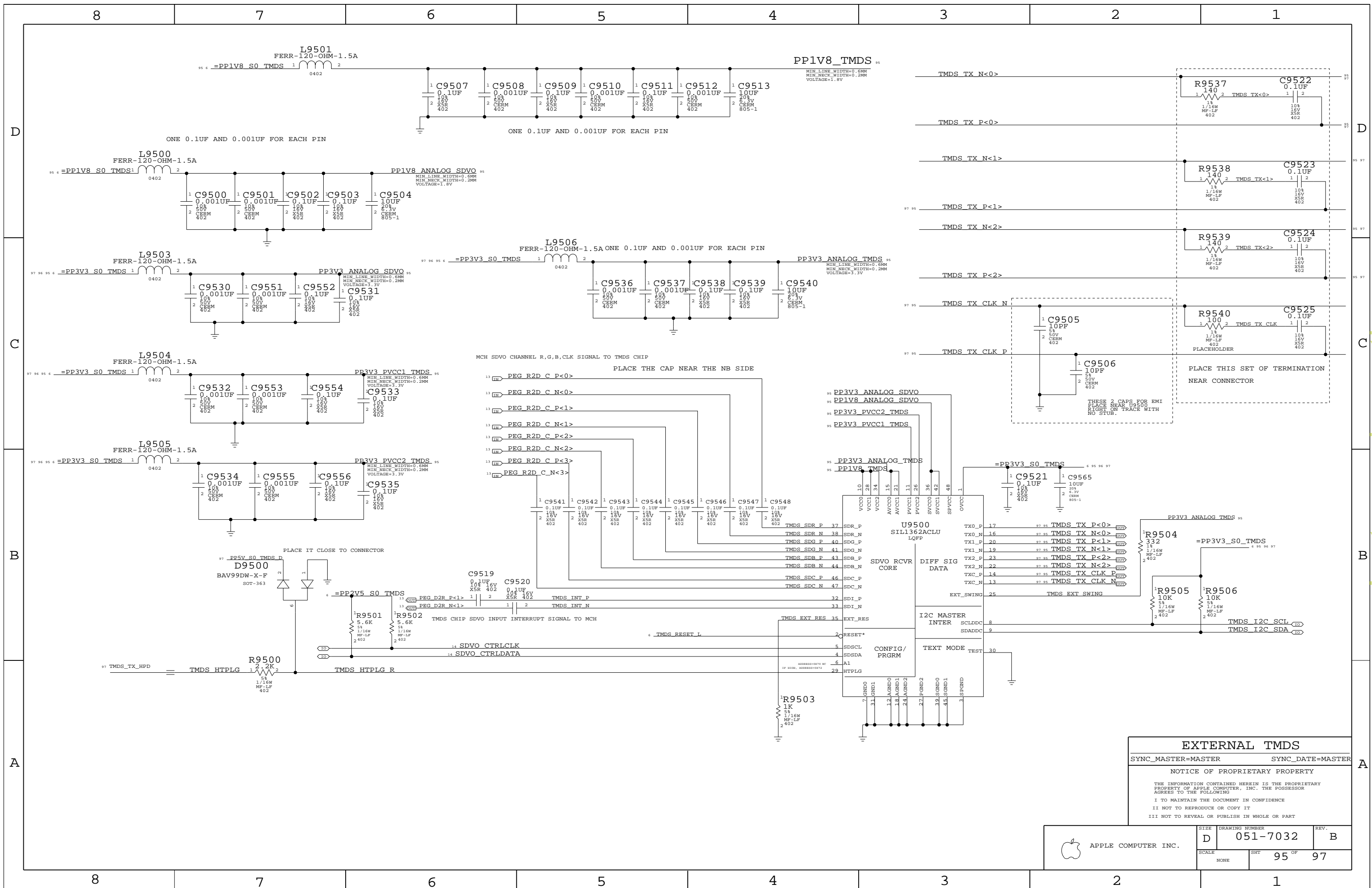
INVERTER INTERFACE



Internal Display Conns	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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SCALE	SHT	94 OF	97
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EXTERNAL TMSD

SYNC_MASTER=MASTER SYNC_DATA=MASTER

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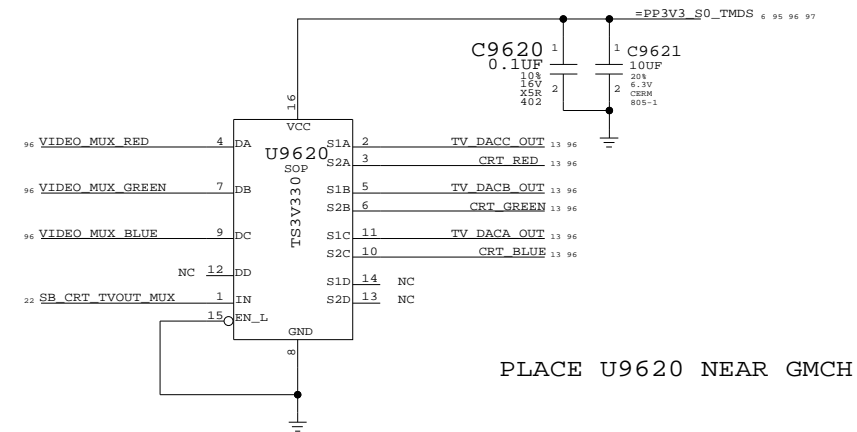
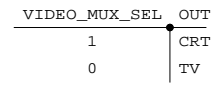
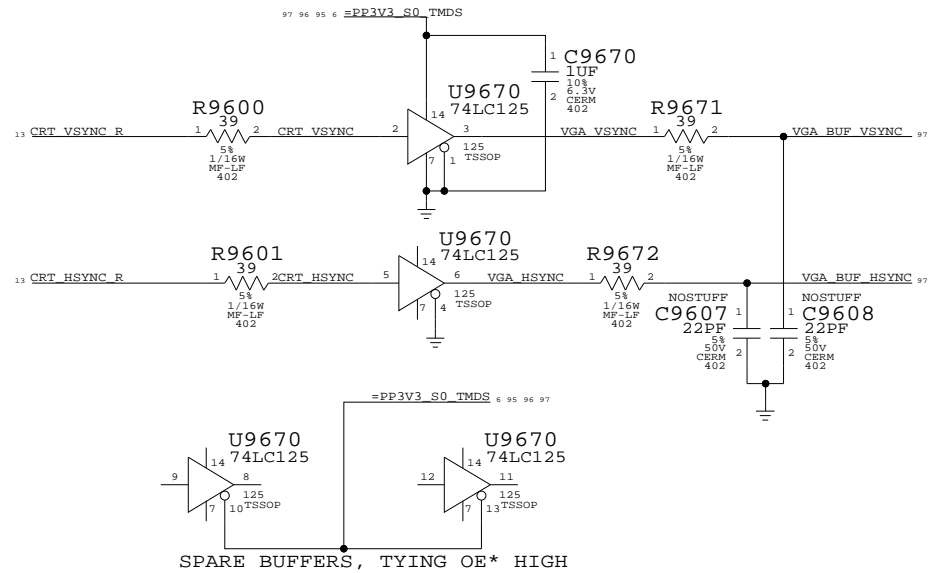
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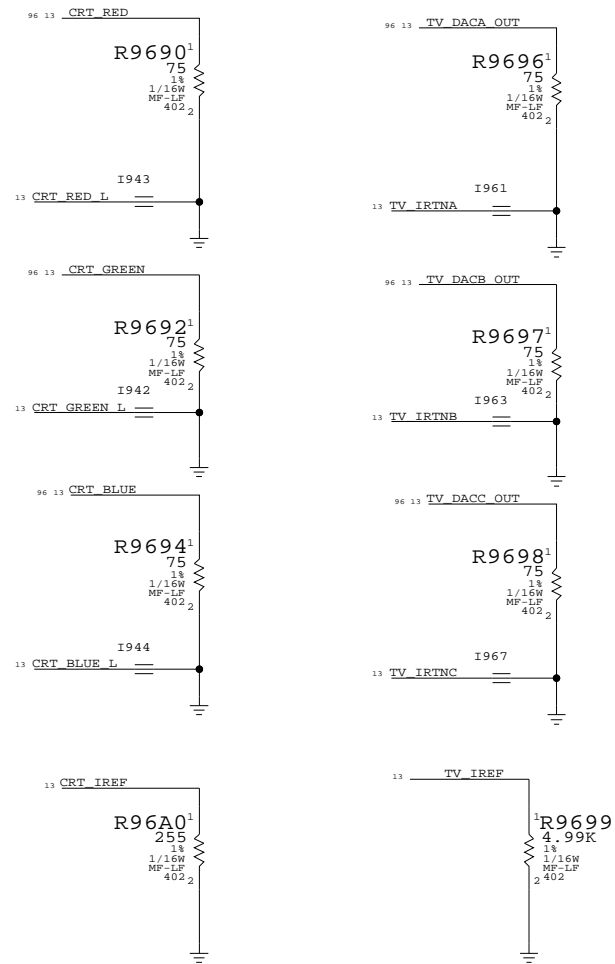
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7032	REV. B
	SCALE NONE	SHEET 95 OF 97	

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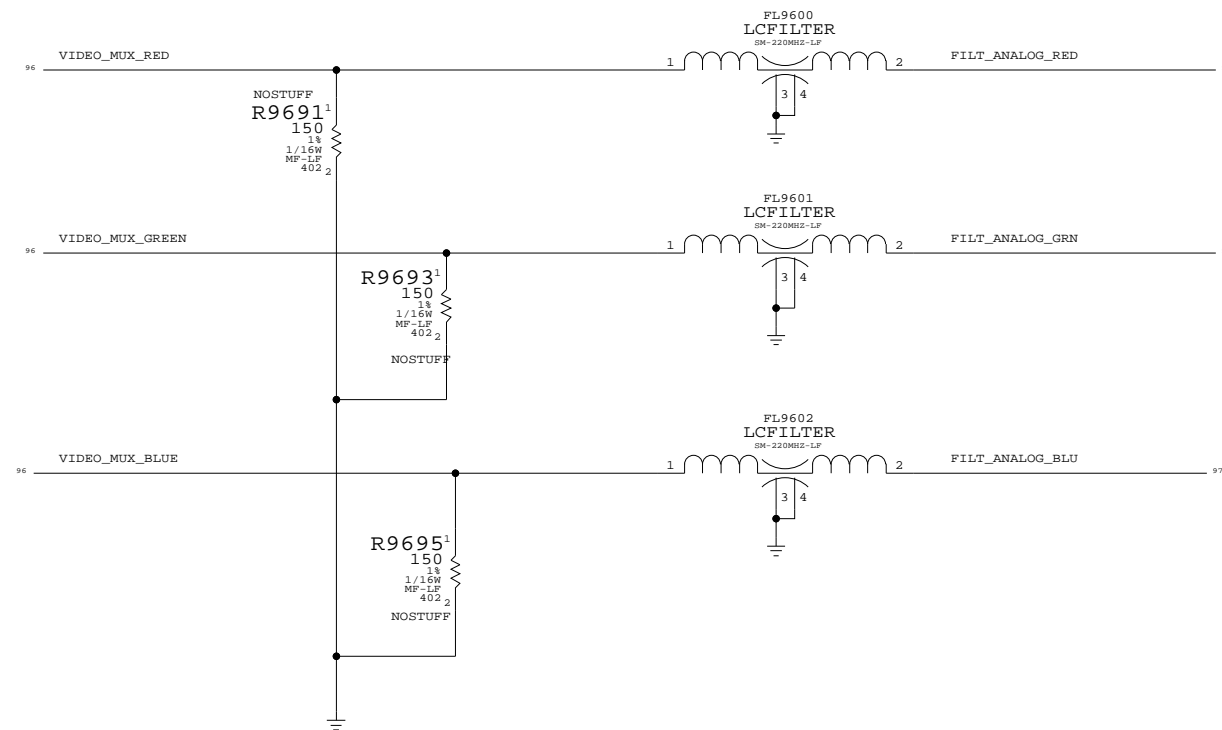
VGA SYNC BUFFERS



PLACE RESISTORS AT NORTHBRIDGE

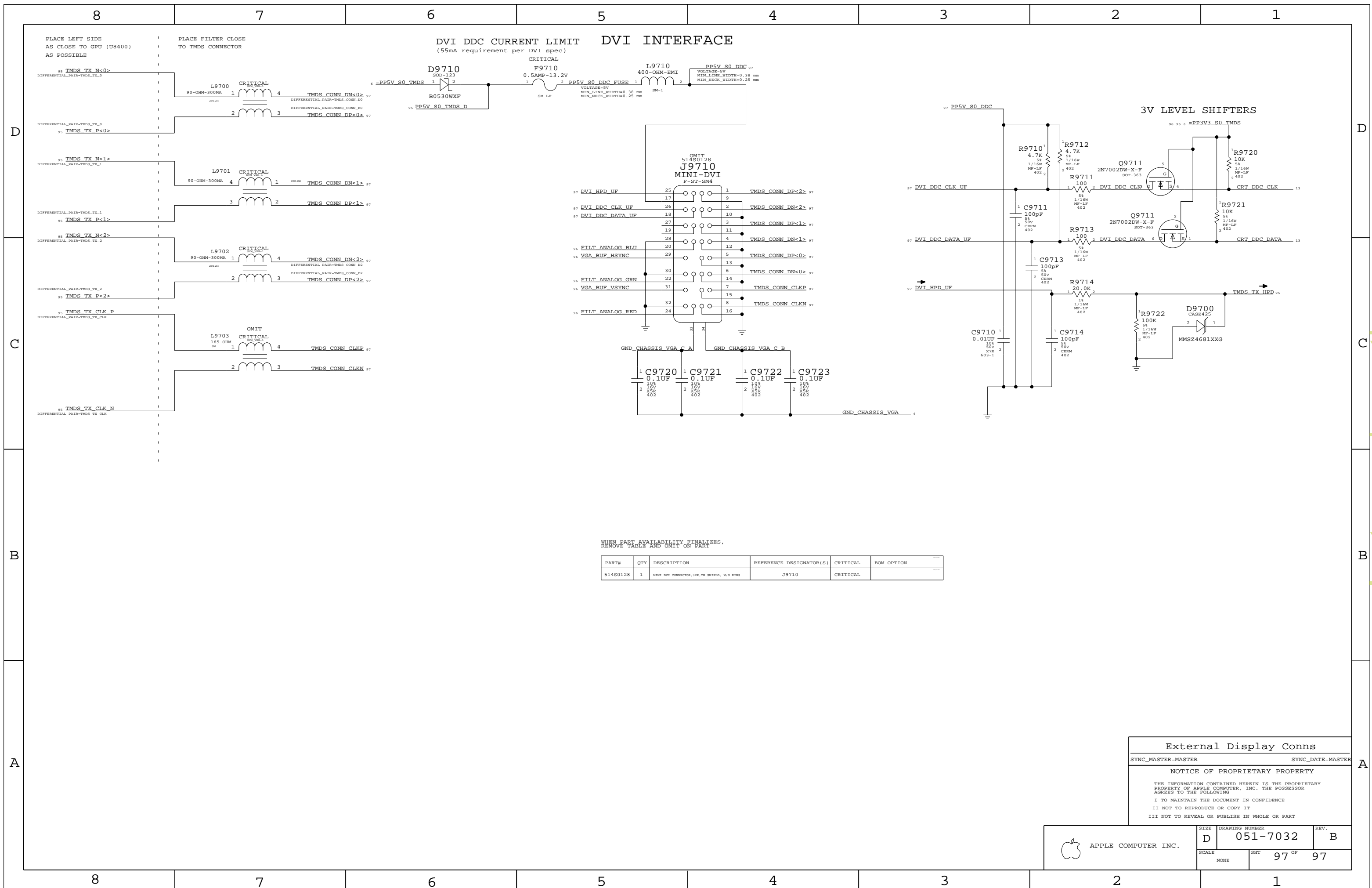


ANALOG FILTERING PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA
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	D	051-7032	B
SCALE	SHT	96 OF	97
NONE			



WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 3P, TH SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	SHT	97 OF 97	
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