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**Sync**

Sync

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78. M1/S Interface Pull-down
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67. ATI M1 Core Power
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73. ATI M1 Video Socket
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79. MAP Platform Connectors
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### Alternate Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
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<tr>
<td>341S1933</td>
<td>IC,PRGRM,SMC,V1.2F10 (M1) MBPRO15</td>
<td>338S0274</td>
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<td>338S0309</td>
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<tr>
<td>337S3268</td>
<td>IC,PRGRM,SMC,V1.2F10 (M1) MBPRO15</td>
<td>338S0274</td>
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<td>826-4393</td>
<td>IC,PRGRM,SMC,V1.2F10 (M1) MBPRO15</td>
<td>338S0274</td>
<td>CRITICAL</td>
<td></td>
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</table>

### Bar Code Label / EEE #’s

<table>
<thead>
<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
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<tr>
<td>630-7758</td>
<td>1</td>
<td>GLB,P/N LABEL,PCB,28MM X 6 MM</td>
<td>630-7758</td>
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<td>GLB,P/N LABEL,PCB,28MM X 6 MM</td>
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### Module Parts

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<tbody>
<tr>
<td>338S0358</td>
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<td>IC,PRGRM,SMC,V1.2F10 (M1) MBPRO15</td>
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<tr>
<td>337S3268</td>
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<td>IC,PRGRM,SMC,V1.2F10 (M1) MBPRO15</td>
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<td>826-4393</td>
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<td>IC,PRGRM,SMC,V1.2F10 (M1) MBPRO15</td>
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### BOM Options

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<th>Reference Des</th>
<th>Critical</th>
<th>BOM Option</th>
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<tbody>
<tr>
<td>VRAM_HY128</td>
<td>PCBA,1.83GHZ,128VRAM,M1-RF_MBP15</td>
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<tr>
<td>M1_COMMON3</td>
<td>PCBA,2.16GHZ,256VRAM,M1-RF_MBP15</td>
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<tr>
<td>M1_COMMON2</td>
<td>PCBA,2.0GHZ,256VRAM,M1-RF_MBP15</td>
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<td>M1_COMMON1</td>
<td>PCBA,2.0GHZ,128VRAM,M1-RF_MBP15</td>
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<tr>
<td>M1_COMMON</td>
<td>PCBA,1.83GHZ,128VRAM,M1-RF_MBP15</td>
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<td></td>
</tr>
</tbody>
</table>

### BOM Configuration

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BOM Number

DRAWING NUMBER

G651-7162
**EXPOSED_VIA** property indicates that the net should have a via with 10-mil soldermask opening for use an engineering probe point.

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**Functional / ICT Test Points**

**Fan Connectors**

**Battery Digital Connector**

**Left I/O Data Connector**

**Left I/O Power Connector**

**Misc EXPOSED_VIA Nets**

**Power Supply NO_TESTs**

**CPU FSB NO_TESTs**

Support for an array of 8 fail-safe points

Note: 10 additional D0 test points are routed separately in same source.
Note: This cap is shared.

VCCA (CPU AVdd) Decoupling

VCCP (CPU I/O) Decoupling

CPU Decoupling & VID Connections

R0990

Sync master = (MASTER)

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Rev. D

Scale: D

051-7182

9 105

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www.laptop-schematics.com
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
- ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU's TCK PIN AND THEN PULL BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PROX PIN.

CPU ITP700FLEX DEBUG

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- REPRODUCTION IN WHOLE OR IN PART WITHOUT PERMISSION IS PROHIBITED.
- FOR INFORMATION CONCERNING LIMITATION OF LIABILITY OR THE WARRANTY, SEE THE APPLICABLE LICENSE AGREEMENT OR THE SOFTWARE USER'S GUIDE.
TV-Out Signal Usage:

- **TV-Out Disable**
  - Component: DACA, DACB & DACC
  - Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used, tie VCC_DAVIDA to VCC DAVIDA rail, and tie VSSA_CRTDAC and VCC_SYNC to GND. HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core and Unused DAC outputs must remain powered, but can omit class D DAC outputs if not used.

- **TV-Out Enable**
  - Component: DACD & DACG
  - Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used, tie VCC_DAVIDA to VCC DAVIDA rail, and tie VSSA_CRTDAC and VCC_SYNC to GND. HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core and Unused DAC outputs must remain powered, but can omit class D DAC outputs if not used.
RTC Battery Connector

**SB RTC Crystal Circuit**

- **R2610**: 402 10V 20% MF-LF
- **C2611**: 0.1UF CERM
- **R2612**: 1/16W 5%

**Platform Reset Connections**

- **Unbuffered**
- **Buffered**

- **R2607**: 1/16W 1K 5%
- **C2607**: 0.1UF CERM
- **R2608**: 1/16W 5%

**Misc**

- **R2614**: 10K
- **R2615**: 100K

This part is never stuffed, to solder a reset button. It provides a set of pads on the board to short or to solder a reset button.
NOTE: This page does not supply VREF.

Power aliases required by this page:
When ENETPWR_S3AC BOMOPTION is active:

- S5          0V      PBUS (3.3V OFF)        0V         Hi-Z (2.5V OFF)   0V  (1.2V OFF)
- S3         3.3V     0V   (3.3V ON)        3.3V         0V  (2.5V ON)   3.3V (1.2V ON)
- G3H Batt     PBUS          0V      PBUS (3.3V OFF)        0V         Hi-Z (2.5V OFF)   0V  (1.2V OFF)
- S5 Batt      PBUS          0V      PBUS (3.3V OFF)        0V         Hi-Z (2.5V OFF)   0V  (1.2V OFF)
- S3 Batt      PBUS         3.3V     PBUS (3.3V OFF)        0V         3.3V (2.5V OFF)   0V  (1.2V OFF)

R4300 470K 5% 1/16W PM_SLP_S3BATT N-CHN Q4300 FDG6332C_NL SC70-6

R4304 100K 5% 1/16W 2N7002 2N7002DW-X-F SOT-363

When ENETPWR_S3 BOMOPTION is active:

- S5          0V      PBUS (3.3V OFF)        0V         Hi-Z (2.5V OFF)   0V  (1.2V OFF)
- S3         3.3V     0V   (3.3V ON)        3.3V         0V  (2.5V ON)   3.3V (1.2V ON)
- G3H Batt     PBUS          0V      PBUS (3.3V OFF)        0V         Hi-Z (2.5V OFF)   0V  (1.2V OFF)
- S5 Batt      PBUS          0V      PBUS (3.3V OFF)        0V         Hi-Z (2.5V OFF)   0V  (1.2V OFF)
- S3 Batt      PBUS         3.3V     PBUS (3.3V OFF)        0V         3.3V (2.5V OFF)   0V  (1.2V OFF)

R4300 470K 5% 1/16W PM_SLP_S3BATT N-CHN Q4300 FDG6332C_NL SC70-6

R4304 100K 5% 1/16W 2N7002 2N7002DW-X-F SOT-363
to apply to entire TPA/TPB XNets.

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is appropriate to terminate unused signals properly.

Provide the appropriate constraints assumed that FireWire PHY page will provide the appropriate constraints to apply to entire 1394b sheet.

The appropriate aliases to map the 1394b implementation based on Apple

- $GND_{CHASSIS/fw}$
- $PPFW_{PORT1}$

SHT 402 21 42 10V 2

FW Power Class Strap

Late-VG Protection Power

"Snapback" & "Late VG" Protection

Cable Power
Port Power Switch

Right USB Port

Place L5200, L5205 and L5206 across most
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKO(A LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM
NOTE: Be aware of pull-up on this signal. If unconnected, powers up with PVIN.

Connect RUNSS off-page to control.

Vout = 0.8V * (1 + Ra / (Rb + Rc))
3.3V S0 FET

3.3V S5 Regulator

3.3V S3 FET

3.3V S0 Regulator

1.05V Current Sense

1.05V S0 Regulator

1.05V Power Supplies

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V

3.3V / 1.05V Power Supplies

APPLE COMPUTER INC.
Left I/O Power Connector

Battery Connector (Digital Signals)

Plug-In & Battery Connectors

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SCALE

NONE

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SYNCD_DATE=(MASTER)
SYNC_MASTER=(MASTER)

82 105
Bluetooth (M13P), IR & SATA HDD Flex Connector

**Left ALS Connector**

518S0395

**M1 Specific Connectors**

---

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APPLE COMPUTER INC.

REV. 051-7162
LVDS Interface Pull-downs

Note: These parts are to connect an isolated state named by the
25th part. Bias voltage is present on LVDS interface pins when
charging and discharging requirements. Resulting pull-up in LVDS interface
and long-term reliability issues. Pull-down resistors reduce
bias voltage on LVDS interface pins even when they should be tri-stated
to meet panel power sequence requirements. Resulting pump-up in LCD panel
can cause startup when they should be 0V.
<table>
<thead>
<tr>
<th>Date</th>
<th>Radar #</th>
<th>Description</th>
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<tr>
<td>2005/08/28</td>
<td>4225433</td>
<td>Changed PBUS Voltage Sense circuit.</td>
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<tr>
<td>2005/08/28</td>
<td>4227323</td>
<td>Repinned Top-Case Flex connector.</td>
</tr>
<tr>
<td>2005/08/31</td>
<td>4227328</td>
<td>Changed EMI caps from 50V to 16V to fit in ESD protection.</td>
</tr>
<tr>
<td>2005/08/31</td>
<td>4237025</td>
<td>Added R8824 and R8827 for GPU memory configuration straps.</td>
</tr>
<tr>
<td>2005/09/03</td>
<td>4227315</td>
<td>Changed SMBus pull-ups to 4.7K.</td>
</tr>
<tr>
<td>2005/08/28</td>
<td>4235203</td>
<td>Changed BOM settings to stuff R2251.</td>
</tr>
<tr>
<td>2005/08/27</td>
<td>4230219</td>
<td>Changed Y3301 to non-obsoleted part.</td>
</tr>
<tr>
<td>2005/09/26</td>
<td>4239505</td>
<td>Updated J4200 (old part no longer exists in library).</td>
</tr>
<tr>
<td>2005/09/02</td>
<td>4243269</td>
<td>Inverted GPU VCore control, adjusted supply R values.</td>
</tr>
<tr>
<td>2005/08/31</td>
<td>4223808</td>
<td>Various power supply R/C updates, plus some R/C adds.</td>
</tr>
<tr>
<td>2005/08/29</td>
<td>4227322</td>
<td>Sync page 44 with M42 to fix FW power net S-states.</td>
</tr>
<tr>
<td>2005/09/06</td>
<td>4246683</td>
<td>Removed NO STUFF option from R8805 per ATI request.</td>
</tr>
<tr>
<td>2005/08/29</td>
<td>4217524</td>
<td>Changed R6430 from 4.5K to 3.5K.</td>
</tr>
<tr>
<td>2005/11/16</td>
<td>4235898</td>
<td>Aliased connection to ALS_GAIN to support M9 request.</td>
</tr>
<tr>
<td>2005/10/13</td>
<td>4247941</td>
<td>Removed NO_TEST properties from CPU FSB strobe signals.</td>
</tr>
<tr>
<td>2005/11/19</td>
<td>4229560</td>
<td>Changed FW chip back to REQ/GNT3.</td>
</tr>
<tr>
<td>2005/10/12</td>
<td>4214494</td>
<td>Implemented circuit to power down ethernet in S3 on battery.</td>
</tr>
<tr>
<td>2005/10/12</td>
<td>4214493</td>
<td>Consolidated 0.22uF caps in design.</td>
</tr>
<tr>
<td>2005/11/16</td>
<td>4227333</td>
<td>Fixed single-pin nets caused by SMC net name updates.</td>
</tr>
<tr>
<td>2005/10/12</td>
<td>4298943</td>
<td>Replaced last remaining non-RoHS compliant connector.</td>
</tr>
<tr>
<td>2005/10/07</td>
<td>4248911</td>
<td>Sync with M38 &amp; M42.</td>
</tr>
<tr>
<td>2005/10/13</td>
<td>4247941</td>
<td>Swapped pins at trackpad ESD protection diode.</td>
</tr>
<tr>
<td>2005/11/15</td>
<td>4310267</td>
<td>Synced 5 pages from mlb_evt branch back to trunk.</td>
</tr>
<tr>
<td>2005/11/16</td>
<td>4235898</td>
<td>Changed Yukon power rail neck widths per M9 request.</td>
</tr>
<tr>
<td>2005/11/18</td>
<td>4347717</td>
<td>Changed SMS self-test pull-up to pull-down.</td>
</tr>
<tr>
<td>2006/03/03</td>
<td>4424175</td>
<td>Changed 8 VRAM strap resistors to enable ICT testing.</td>
</tr>
<tr>
<td>2006/01/05</td>
<td>4362566</td>
<td>Removed 920- number for thin PCB option.</td>
</tr>
<tr>
<td>2006/03/31</td>
<td>4498859</td>
<td>Updated BOM table for screened ISL6262.</td>
</tr>
<tr>
<td>2006/02/13</td>
<td>4437189</td>
<td>Changed R7757 to 1Mohm &amp; R7770 to 100K.</td>
</tr>
<tr>
<td>2006/03/31</td>
<td>4436716</td>
<td>Added BOM table for ATI rev B26.</td>
</tr>
<tr>
<td>2006/01/03</td>
<td>4290282</td>
<td>Removed BOM table, changed L9455 to 155S0002.</td>
</tr>
<tr>
<td>2005/12/01</td>
<td>4362566</td>
<td>Restructured BOM for thick/thin PCB versions.</td>
</tr>
<tr>
<td>2006/03/31</td>
<td>4485021</td>
<td>Changed R7542 from 9.31K to 11.5K for CPU VCore OCP.</td>
</tr>
<tr>
<td>2006/01/03</td>
<td>4391436</td>
<td>Swapped N/P signal names on one portion of SATA_R2D.</td>
</tr>
<tr>
<td>2005/12/01</td>
<td>4352020</td>
<td>Changed 2.5V supply inductor to RoHS-compliant part.</td>
</tr>
<tr>
<td>2006/03/31</td>
<td>4499085</td>
<td>Changed C7532 from 10nF to 15nF to slow CPU slew rate.</td>
</tr>
<tr>
<td>2006/01/03</td>
<td>4347845</td>
<td>Changed LVDS pull-downs from 10K to 8.2K.</td>
</tr>
<tr>
<td>2005/12/01</td>
<td>4355020</td>
<td>RPAK pinswaps to LVDS pull-downs for PCB layout.</td>
</tr>
<tr>
<td>2006/03/31</td>
<td>4485021</td>
<td>Changed R7542 from 9.31K to 11.5K for CPU VCore OCP.</td>
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</table>
FSB (Front-Side Bus) Constraints

CPU Signal Constraints

Napa Platform Constraints

PCI-Express / DMI Bus Constraints

Disk Interface Constraints

USB 2.0 Interface Constraints

Internal Interface Constraints

Clock Signal Constraints

Napa Platform Constraints
### Video Signal Constraints

**LVDS and TMDS pairs should be kept at least 25 mils apart.**

**LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.**

**VGA should be routed as close to 75-ohms single-ended impedence as possible.**

**ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.**

**Ground shields can be used around each pair if spacing cannot be met.**

### GDDR3 (Frame Buffer) Memory Bus Constraints

- **LVDS and TMDS** should be kept at least 25 mils apart.
- **LVDS and TMDS** signals are 100-ohm +/- 10% differential impedence.
- **VGA** should be routed as close to 75-ohms single-ended impedence as possible.
- **ADDR/CTRL lines** should route 35-ohms to T, then 55-ohms to each VRAM device.
- **Ground shields** can be used around each pair if spacing cannot be met.

### High-Speed 1/O Interface Constraints

**PCI Bus**

- **LVDS** and **TMDS** signals are 100-ohm +/- 10% differential impedence.
- **LVDS** and **TMDS** pairs should be kept at least 15 mils apart.
- Ground shielding should be used around each pair of 75-ohm single-ended impedence or more.
- **LVDS** should be routed as close to a 75-ohm single-ended impedence as possible.
- **LVDS** should be kept at least 15 mils from other traces.
- Ground shields recommended around **LVDS** signals.

**PCI**

- **LVDS** and **TMDS** signals are 100-ohm +/- 10% differential impedence.
- **LVDS** and **TMDS** pairs should be kept at least 15 mils apart.
- Ground shielding should be used around each pair of 75-ohm single-ended impedence or more.
- **LVDS** should be routed as close to a 75-ohm single-ended impedence as possible.
- **LVDS** should be kept at least 15 mils from other traces.
- Ground shields recommended around **LVDS** signals.

**NOTE:** Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"
### MI Board-Specific Spacing & Physical Constraints

<table>
<thead>
<tr>
<th>LAYER</th>
<th>TOP, BOTTOM</th>
<th>MINIMUM LINE WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>MINIMUM NECK WIDTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Y</td>
<td>0.102 mm</td>
<td>0.130 mm</td>
<td>0.080 mm</td>
<td>0.220 mm</td>
<td>0.550 mm</td>
</tr>
<tr>
<td>1</td>
<td>Y</td>
<td>0.125 mm</td>
<td>0.140 mm</td>
<td>0.076 mm</td>
<td>0.125 mm</td>
<td>0.550 mm</td>
</tr>
<tr>
<td>2</td>
<td>Y</td>
<td>0.140 mm</td>
<td>0.165 mm</td>
<td>0.100 mm</td>
<td>0.140 mm</td>
<td>0.550 mm</td>
</tr>
<tr>
<td>3</td>
<td>Y</td>
<td></td>
<td>0.190 mm</td>
<td>0.120 mm</td>
<td>0.200 mm</td>
<td>0.550 mm</td>
</tr>
<tr>
<td>4</td>
<td>Y</td>
<td></td>
<td>0.220 mm</td>
<td>0.140 mm</td>
<td>0.220 mm</td>
<td>0.550 mm</td>
</tr>
</tbody>
</table>

### Allow Route On Layer?

- Y:
  - Layers 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11

### Unsupported Rules

- 110_OHM_DIFF
- 90_OHM_DIFF
- 85_OHM_DIFF
- 75_OHM_DIFF
- 27P4_OHM_SE

### Table Physical Rule Item

<table>
<thead>
<tr>
<th>RULE</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
<th>NET_PHYSICAL_TYPE</th>
<th>AREA_TYPE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5:1_SPACING</td>
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<td></td>
<td></td>
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<tr>
<td>4:1_SPACING</td>
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<td></td>
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<td></td>
</tr>
</tbody>
</table>

### Table Spacing Rule Item

- STANDARD
- DEFAULT

### Table Spacing Assignment Item

- Override

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ANGLED CAPS FOR C4 NOISE

CPU AREA

- Connection to unstuffed comp. pads
- RefDes: CRWK01 to CRWK15
- Part Numbers: CRWK01, CRWK02
- Value: 33UF
- Type: OMIT
- Case: CSED2E-SM
- Voltage: 16V
- Tolerance: 20%

GPU AREA

- Connection to unstuffed comp. pads
- RefDes: CRWK05 to CRWK15
- Part Numbers: CRWK05, CRWK06
- Value: 1UF
- Type: CERM
- Case: 805
- Voltage: 25V
- Tolerance: 20%

SB AREA

- Connection to unstuffed comp. pads
- RefDes: CRWK08 to CRWK15
- Part Numbers: CRWK08
- Value: 1UF
- Type: CERM
- Case: 805
- Voltage: 25V
- Tolerance: 20%

---

**BOM OPTION**

- CRWK01 to CRWK15
- Value: 33UF
- Type: OMIT
- Case: CSED2E-SM
- Voltage: 16V
- Tolerance: 20%

---

**REFERENCE DES**

- CRWK10, CRWK12, CRWK14, CRWK15
- CRWK05, CRWK06, CRWK07, CRWK08
- CRWK09, CRWK11, CRWK13

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