3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

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</tr>
</thead>
<tbody>
<tr>
<td>630-7705</td>
<td>376S0448</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>128S0095</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>630-7704</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>630-7685</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>630-7684</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>341S1873</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>359S0101</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>353S1465</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>338S0315</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>341S1875</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>338S0274</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>337S3268</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>337S3267</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>333S0350</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>826-4393</td>
<td>Alternate Parts</td>
</tr>
<tr>
<td>630-7705</td>
<td>826-4393</td>
<td>Alternate Parts</td>
</tr>
</tbody>
</table>

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<table>
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<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>EEE_W36</td>
<td>M1/Common, CPU_1.83GHz, VRAM_SAM128</td>
</tr>
<tr>
<td>EEE_VWQ</td>
<td>M1/Common, CPU_2.16GHz, VRAM_SAM256</td>
</tr>
<tr>
<td>EEE_VWP</td>
<td>M1/Common, CPU_2.0GHz, VRAM_SAM256</td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DEI</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>32221281</td>
<td>1</td>
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<td>T0090</td>
<td>CRITICAL</td>
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</tr>
<tr>
<td>32221281</td>
<td>4</td>
<td>Q1,14.9062 Mohs (0.006W)</td>
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</tr>
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</tr>
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</tr>
</tbody>
</table>

### BOM Configuration

<table>
<thead>
<tr>
<th>BOM NAME</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALTERNATE, COMMON, M1_COMMON1, M1_COMMON2, M1_COMMON3</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

---

**Notes:**
- Bar Code Label / EEE #’s: [EEE:VWP]
- BOM Configuration: [EEE_W36, M1_COMMON, CPU_1.83GHZ, VRAM_SAM128]
- EEE Options: [EEE_VWQ, M1_COMMON, CPU_2.16GHZ, VRAM_SAM256]
- EEE Options: [EEE_VWP, M1_COMMON, CPU_2.0GHZ, VRAM_SAM256]
- Reference Design: [EEE_W37, M1_COMMON, CPU_2.0GHZ, VRAM_SAM256]
- Reference Design: [EEE_VWQ, M1_COMMON, CPU_2.16GHZ, VRAM_SAM256]
- Reference Design: [EEE_VWP, M1_COMMON, CPU_1.83GHZ, VRAM_SAM128]

---

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**Reference:**
- Reference Design: [EEE_W36, M1_Common, CPU_1.83GHZ, VRAM_SAM128]
- Reference Design: [EEE_VWQ, M1_Common, CPU_2_16GHZ, VRAM_SAM256]
- Reference Design: [EEE_VWP, M1_Common, CPU_1_83GHZ, VRAM_SAM128]
Chassis connection to be made at the mounting hole southeast of the LVDS connector.

Chassis connection to be made at the mounting hole northwest of the DVI connector.

Ethernet Power Management Support

NOTE: BOM options "USB_G_OC_PU" and "SB_GPIO30" are mutually-exclusive.

USB Port "A" (Debug Port) = Right USB 2.0 Port
- USB_A_P = USB A_P
- USB_A_N = USB A_N
- USB_BT_P = USB_BT_P
- USB_BT_N = USB_BT_N
- USB_IR_P = USB_IR_P
- USB_IR_N = USB_IR_N
- USB2_RT_N = USB2_RT_N
- RTUSB_OC_L = RTUSB_OC_L
- USB2_EXCARD_N = USB2_EXCARD_N
- USB2_CAMERA_N = USB2_CAMERA_N
- USB2_CAMERA_P = USB2_CAMERA_P
- USB2_LT_P = USB2_LT_P
- UNUSED_USB_B_OC_L = UNUSED_USB_B_OC_L
- USB_BT_P = USB_BT_P
- USB_BT_N = USB_BT_N
- USB2_EXCARD_P = USB2_EXCARD_P
- USB2_CAMERA_P = USB2_CAMERA_P
- USB2_CAMERA_N = USB2_CAMERA_N
- USB2_LT_N = USB2_LT_N
- UNUSED_USB_B_OC_L = UNUSED_USB_B_OC_L

USB Port "B" = Trackpad (Gray)

USB Port "C" = Left USB 2.0 Port
- USB_C_P = USB C_P
- USB_C_N = USB C_N
- USB_BT_P = USB_BT_P
- USB_BT_N = USB_BT_N
- USB_IR_P = USB_IR_P
- USB_IR_N = USB_IR_N
- USB2_RT_N = USB2_RT_N
- RTUSB_OC_L = RTUSB_OC_L
- USB2_EXCARD_N = USB2_EXCARD_N
- USB2_CAMERA_N = USB2_CAMERA_N
- USB2_CAMERA_P = USB2_CAMERA_P
- USB2_LT_P = USB2_LT_P
- UNUSED_USB_B_OC_L = UNUSED_USB_B_OC_L

USB Port "D" = Camera

USB Port "E" = ExpressCard

USB Port "F" = IR Receiver

USB Port "G" = Bluetooth (MI3P)

USB Port "H" = Reserved (PCI-E Mini Card)

Trace deleted to make room for other diffpairs over RAM connector.
**CPU VCORE HF AND BULK DECOUPLING**

- 4x 470uF, 20x 22uF O805

**NOTE:** This cap is shared between CPU and NB

**CPU VCORE VID Connections**

Resistors to allow for override of CPU VID

- CPU VID<6>
- CPU VID<5>
- CPU VID<4>
- CPU VID<3>
- CPU VID<2>
- CPU VID<1>
- CPU VID<0>

**VCCA (CPU AVdd) Decoupling**

- 10µF, 1x 0.01µF

**VCCP (CPU I/O) Decoupling**

- 1x 470uF, 6x 0.1uF 0402

**NOTE:** This cap is shared between CPU and NB
OUT
OUT
OUT
OUT

CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL Layout Note:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S PBO PIN.
**LVDS Disable**

Tie VCC_LVDS and VCC_LVDS to GND. If LVDS is not used, VCC_LVDS must remain powered with proper decoupling. Otherwise, tie VCC_LVDS to GND also.

**CRT Disable**

Tie CRT_DDC_DATA to GND also.

**TV-Out Disable**

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, and tie VSSA_CRTDAC and VCCSYNC to GND.

**Composite: DACA only**

Component: DACA, DACB & DACC

Filtering components. Unused DAC outputs should be tied to VCCD_LVDS also.

**S-Video: DACB & DACC only**

Otherwise, tie VCCD_LVDS to GND also.

**TV-Out Signal Changes**

Composite: DACA only

Component: DACA, DACB & DACC

Unused DAC outputs must remain powered with 75-ohm resistors. Tying DAC outputs to GND through 75-ohm resistors is unnecessary.

**CRT Disable**

Tie DAC_C0, IF/IF, and IFP to 1.5V power rail. Tie DAC_C1, VCC_DAC0, DAC_IREF, and DAC_IREF to 1.5V power rail. Tie VCAP_C0 to GND.

**CRT Disable**

Tie DAC_C0, IF/IF, and IFP to VCC Core rail, tie DAC_IREF to VCC Core rail, and tie DAC_C1, DAC_IREF, and DAC_IREF to GND.
**RTC Battery Connector**

- Critical: VR_PWRGD_CK410
- Power: SB_RTC_X2
- Output: =PP3V3_S0_SB_PM

**SB RTC Crystal Circuit**

10MHz

**Platform Reset Connections**

- **Unbuffered**
  - Debug_RST_L
  - Peg_Reset_L
  - Nb_Reset_In_L

- **Buffered**
  - Lio_Plt_Reset_L
  - Pmi_Io_Reset_L

Initial resistor values are based on CRN, but may change after characterization.

**SB Misc**

- Smt: Master-Quarter
- Smt: Fast-Quarter

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NOTE: This page does not supply VREF.

BOM options provided by this page:
- =PPSPD_S0_MEM (2.5V - 3.3V)
- =I2C_SODIMMA_SDA

"Lower" (surface-mount) slot

---

DDR2 Bypass Caps
(For return current)

---

DDR2 SO-DIMM Connector A

---

APPLE COMPUTER INC.

---

Rev. A
The reference voltage must be provided.

NOTE: This page does not supply VREF.

Power aliases required by this page:

- **C2900**: 2.2uF
- **C2901**: 603
- **CERM**: 1
- **C2900**: 0.1uF
- **C2900**: 10V
- **C2900**: 20%

"Upper" (thru-hole) slot

**DDR2 Bypass Caps**

(For return current)

**DDR2 SO-DIMM Connector B**

- **C2908**: 10uF
- **C2909**: 10uF
- **C2910**: 10uF
- **C2911**: 10uF
- **C2912**: 10uF
- **C2913**: 10uF
- **C2914**: 10uF
- **C2915**: 10uF
- **C2916**: 10uF
- **C2917**: 10uF
- **C2918**: 10uF
- **C2919**: 10uF
- **C2920**: 10uF
- **C2921**: 10uF

Resistance prevents ground shorts.
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure C1L and C2T resistors are close to 8D-DIMM connector
disables MEMVTT in sleep. MEMVTT_EN can be used to leave 1.8V powered in S3. Okay to turn off 5V and DDR2 VTT Regulator
Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformer.

Short shielded RJ-45.
Page Notes

Power aliases required by this page:
- TWPWR_PWRON (system supply for bus power)
- TWPWR_PWRON

Signal aliases required by this page:
- FWPSNCH (see related test note below)

BOM options provided by this page:

- =PP3V3_S0_FWPORTPWRSW
- =PPBUS_S0_FWPWRSW (system supply for bus power)

Port Power Switch
- Enables port power when machine is running or on AC.

FireWire Port Current Sense
- FWPWR_IOUT
- FWPWR_EN_L
- FWPWR_EN_L_DIV
- FWPWR_EN_L

---

**FireWire Port Power**

**SYNC_MASTER**=(MASTER)
**SYNC_DATE**=(MASTER)

**MIN_NECK_WIDTH**=0.2 mm
**MIN_LINE_WIDTH**=0.2 mm

**FWPWR_EN_L**
**FWPWR_EN_L_DIV**

**PM_SLP_S3_L**

**VOLTAGE**=12.6V

---

**Port Power Switch**

**SYNC_MASTER**=(MASTER)
**SYNC_DATE**=(MASTER)

**MIN_NECK_WIDTH**=0.2 mm
**MIN_LINE_WIDTH**=0.2 mm

---

**FireWire Port Current Sense**

**FWPWR_IOUT**

---

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NOTE: This page is expected to contain Signal aliases required by this page:

PROVIDED

Power aliases required by this page:

Place close to FireWire PHY

2nd TPA/TPB pair unused
3rd TPA/TPB pair unused

FW Power Class Strap
Single-point system reset power

Late-VG Protection Power

"Snapback" & "Late VG" Protection

Cable Power
Top-Case Connector

Camera Connector

Internal USB Connections

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MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
GND_CAMERA
VOLTAGE=0V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm

PCI-E x1 Port "A" = Ethernet (Yukon)
PCI-E x1 Port "B" = PCI-E Mini Card
PCI-E x1 Port "C" = ExpressCard
PCI-E x1 Port "D" = Unused
PCI-E x1 Port "E" = Unused
PCI-E x1 Port "F" = Unused

C5710
-0.1uF 10% 16V X5R 402
PCAR5710

C5711
-0.1uF 10% 16V X5R 402
PCAR5711

C5720
-0.1uF 10% 16V X5R 402
PCAR5720

C5721
-0.1uF 10% 16V X5R 402
PCAR5721

PCI-E Connections

PCIE_F_D2R_P
PCIE_F_D2R_N
PCIE_F_R2D_C_N
PCIE_F_R2D_C_P
PCIE_F_R2D_P

PCIE_E_D2R_P
PCIE_E_D2R_N
PCIE_E_R2D_C_N
PCIE_E_R2D_C_P
PCIE_E_R2D_P

PCIE_D_R2D_C_P
PCIE_D_R2D_C_N
PCIE_D_D2R_P
PCIE_D_D2R_N

PCIE_C_D2R_P
PCIE_C_D2R_N
PCIE_C_R2D_C_N
PCIE_C_R2D_C_P
PCIE_C_R2D_P

PCIE_B_D2R_P
PCIE_B_D2R_N
PCIE_B_R2D_C_N
PCIE_B_R2D_C_P
PCIE_B_R2D_P

PCIE_MINI_D2R_P
PCIE_MINI_D2R_N
PCIE_MINI_R2D_C_N
PCIE_MINI_R2D_C_P
PCIE_MINI_R2D_P

PCIE_EXCARD_D2R_P
PCIE_EXCARD_D2R_N
PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_R2D_C_P
PCIE_EXCARD_R2D_P

MAKE_BASE=TRUE
TP_PCIE_F_D2RP
TP_PCIE_F_D2RN
TP_PCIE_F_R2DP
TP_PCIE_F_R2DN
TP_PCIE_E_D2RP
TP_PCIE_E_D2RN
TP_PCIE_E_R2DN
TP_PCIE_E_R2DP
TP_PCIE_D_R2DP
TP_PCIE_D_R2DN
TP_PCIE_D_D2RN
TP_PCIE_D_D2RP
TP_PCIE_C_R2D_C_N
TP_PCIE_C_R2D_C_P
TP_PCIE_C_D2R_P
TP_PCIE_C_D2R_N
TP_PCIE_B_D2R_P
TP_PCIE_B_D2R_N
TP_PCIE_B_R2D_C_P
TP_PCIE_B_R2D_C_N
TP_PCIE_B_R2D_P
TP_PCIE_MINI_D2R_P
TP_PCIE_MINI_D2R_N
TP_PCIE_MINI_R2D_P
TP_PCIE_MINI_R2D_N
TP_PCIE_EXCARD_D2R_P
TP_PCIE_EXCARD_D2R_N
TP_PCIE_EXCARD_R2D_C_P
TP_PCIE_EXCARD_R2D_C_N
TP_PCIE_EXCARD_R2D_P
TP_PCIE_EXCARD_R2D_N
**GPU / Heat Pipe Thermal Sensor**

**Right-Side/Fin Stack Thermal Sensor**

**CPU Back-Up Thermal Diode**

---

**CPU Back-Up Thermal Diode**

- **CPU Back-Up Thermal Diode**
  - **Part Number:** B6110
  - **Device:** 2N3904LF
  - **Package:** SOT23

**Placement note:**
- Place the CPU Back-Up Thermal Diode in between VRAM.
- Place near the GPU center.

**Layout note:**
- Minimize stubs between these R's and R1001 & R1002.

---

**Right-Side/Fin Stack Thermal Sensor**

- **Part Number:** G6120
  - **Device:** 2N3904LF
  - **Package:** SOT23

**CRITICAL**

**J6120**

---

**CPU Back-Up Thermal Diode Placement note:**
- Place the CPU Back-Up Thermal Diode below and to the left of the speaker hole.

---

**General Notes:**
- **Part Number:** C6100
  - **Device:** 0.1uF
  - **Package:** 402

---

**Thermal Sensors**

- **Part Number:** X6100
  - **Device:** SMBUS_RSTHMSNS

---

**References:**
- **Reference Design:** ADT7461
- **Reference Design:** DS18B20

---

**BOM Option:**
- **Part Number:** 518S0226
  - **Device:** CRITICAL

---

**Remark:**
- MB-LF 1/16W 402 5%

---

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**Thermal Sensors**

- **Part Number:** G6120
  - **Device:** 2N3904LF
  - **Package:** SOT23

---

**References:**
- **Reference Design:** ADT7461
- **Reference Design:** DS18B20

---

**BOM Option:**
- **Part Number:** 518S0226
  - **Device:** CRITICAL

---

**Remark:**
- MB-LF 1/16W 402 5%

---

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R6309 is not needed when sharing SPI flash with ICH7M and TEKOA (LAN chip).

R6307 and R6306 should be placed less than 100 mils from ICH7M.

R6303 should be placed less than 100 mils from Flash ROM.
Left ALS Filter

Left ALS circuit has 1K series-R

Right ALS Circuit

Keyboard LED Driver

ALS Support
Connect to RUNSS pins to control outputs.

If disconnected, power up with VIN.

NOTE: Be aware of pull-ups to VIN on these signals.

8A max output

Vout = 4.98V

(L7620 limits)

Vout = 1.49V

(L7660 & Q7660 limit)
NOTE: Be aware of pull-up on this signal. If unconnected, powers up with PVIN.

Vout = 0.8V * (1 + Ra / (Rb + Rc))

Vout = 1.205V

1.25A max output (Switcher limit)

2.5A max output (Switcher limit)
Power Control Signals

3.425V "G3Hot" Supply
Supply needs to guarantee 3.42V delivered to MCU VCore generator

1.5V / 1.05V PWRGD Circuit
Reports when 1.5V S0 and 1.05V S0 are in regulation

Other S0 Rails PWRGD Circuit
Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation

Unused PGOOD Signals
Unused PGOOD Signals

3.3V G3Hot Supply & Power Control
This Master-Couplers and Slave-Couplers

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Please note that removing ethernet power in battery sleep.
Before enabling GPU VCore to support 2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

2N7002DW-X-F SOT-363

Design by IBM

470K 5%
1/16W
10K
1/16W
**Back-Bias Positive Supply**

Back-bias positive supply provides VDDC + 0.5V when active.

Note: BBP tracks VDDC based on GPU voltage GPIO. When inactive, provides VDDC to BBP pins.

**Back-Bias Negative Supply**

Back-bias negative supply provides VDDC - 0.5V when active.

For proper M56 power sequence, this pull-up voltage must be high enough to satisfy BBP VIN (where VIN = 1.1V).

Vin must be > 2.0V.

Recommended values:

- Vin: 5V
- Rb: > 50 Ohm
- Ra: Vin / 50 uA

For proper M56 power sequence, this pull-up voltage must be high enough to satisfy BBP VIN (where VIN = 1.1V).

Vin must be > 2.0V.

Recommended values:

- Vin: 5V
- Rb: > 50 Ohm
- Ra: Vin / 50 uA

**GPU VCore Supply**

Vout(low) = 0.59V * (1 + Ra/Rb)

Vout(high) = 0.6V * (1 + Ra/Req)

Req = Rb || Rc

For proper M56 power sequence, this pull-up voltage must be high enough to satisfy BBP VIN (where VIN = 1.1V).

Vin must be > 2.0V.

Recommended values:

- Vin: 5V
- Rb: > 50 Ohm
- Ra: Vin / 50 uA

Vout = -0.55V

125mA max output

(Regulator limit)

Vout = 1.10V / 0.95V

17A max output

(G8528 limit)
NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.
LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the reset part. Blue voltage in panel is present on LVDS interface pin even when pump-up from backlight has ceased. Pull-down resistors reduce long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the reset part. Blue voltage in panel is present on LVDS interface pin even when pump-up from backlight has ceased. Pull-down resistors reduce long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.
**NOTE:** Design Guide allows closer spacing if signal lengths can be shortened.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 6.2

**TABLE:**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Spacing Type 1</th>
<th>Spacing Type 2</th>
<th>Area Type</th>
<th>Min. Width</th>
<th>Min. Neck Width</th>
<th>Min. Neck Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>1.5:1</td>
<td>3:1</td>
<td>2:1</td>
<td>3:1</td>
<td>1.8:1</td>
<td></td>
</tr>
<tr>
<td>DDR2</td>
<td>1.5:1</td>
<td>3:1</td>
<td>ST</td>
<td>2:1</td>
<td>1.8:1</td>
<td></td>
</tr>
<tr>
<td>PCIE</td>
<td>1.5:1</td>
<td>3:1</td>
<td>ST</td>
<td>2:1</td>
<td>1.8:1</td>
<td></td>
</tr>
</tbody>
</table>

All FSB signals with impedance requirements are 58-Ohm single-ended.

- Most CPU signals with impedance requirements are 58-Ohm single-ended.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

**Clock Signal Constraints**

- Clock signals require 58-Ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

**Internal Interface Constraints**

- USB 2.0 interface requires 58-Ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

**PCI-Express / DMI Bus Constraints**

- PCIe signals require 58-Ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

**Disk Interface Constraints**

- Disk interface signals require 58-Ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

**NOTE:** Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

**NAPA PLATFORM CONSTRAINTS**

- CPU, FSB, and memory signals require 58-Ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

**NAPA PLATFORM CONSTRAINTS**

- All signals require 58-Ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

**DIMENSIONS**

- All signals require 58-Ohm single-ended impedance.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

**NOTE:** Design Guide recommends at least 25 mils, >50 mils preferred.

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

**NOTE:** Design Guide recommends at least 25 mils, >50 mils preferred.
VGA should be routed as close to 75-ohm single-ended impedance as possible.

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.

VGA signals should be kept at least 15 mils from other traces.

Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

LVDS and TMDS pairs should be kept at least 25 mils apart.

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.

DQ/DQM/DQS lines are 40-ohm single-ended impedence.

CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.

LVDS and TMDS pairs should be kept at least 25 mils apart.

LVDS_100D = STANDARD

VGA_75S = STANDARD

FBB_PAIR2PAIR = 2:1_SPACING

15 MIL = MINIMUM LINE WIDTH

TMDS_PAIR2PAIR = 25 MIL

100_OHM_DIFF = DIFFPAIR PRIMARY GAP

75_OHM_DIFF = DIFFPAIR NECK GAP

ENET_100D = STANDARD

PCI_55S = STANDARD

FW_110D = STANDARD

High-Speed I/O Interface Constraints

PCI Bus Constraints

GDDR3 (Frame Buffer) Memory Bus Constraints

Video Signal Constraints

High-Speed I/O Interface Constraints

PCI Bus Constraints

GDDR3 (Frame Buffer) Memory Bus Constraints

Video Signal Constraints

High-Speed I/O Interface Constraints

PCI Bus Constraints

GDDR3 (Frame Buffer) Memory Bus Constraints

Video Signal Constraints

High-Speed I/O Interface Constraints

PCI Bus Constraints

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Video Signal Constraints

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PCI Bus Constraints