1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

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820-2059

051-7164 CRITICAL

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### TRUCKEE, 2.33GHZ, B2, 256 VRAM, SAM, M57

- BOM GROUP: M57_COMMON4
- VRAM_256SAM
- VRAM_128SAM
- VRAM_256INF
- VRAM_128INF

### TRUCKEE, 2.16GHZ, B2, 256 VRAM, SAM, M57

- BOM GROUP: M57_COMMON1
- VRAM_256SAM
- VRAM_128SAM
- VRAM_256INF
- VRAM_128INF

### M57_TPM

- IC, SGRAM, GDDR3, 16MX32, 600MHZ, 136 FBGA
- IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA
- IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA

### LBL, P/N LABEL, PCB, 28MM X 6 MM

- 157S0111
- 128S0060
- 376S0445

### SCREENED ISL6262 FOR ISL9504

- 330UF, 2V, 6MOHM, D2
- 330UF, 2V, 9MOHM, D2

### ALT ALTERNATE FOR

- 3G

### ALTERNATE, COMMON, M57_COMMON1, M57_COMMON2, M57_COMMON3, M57_COMMON4, M57_DEBUG, ISL6255A, M57_NO_3G

- REF DES: C2516
- REF DES: T8900, T8950, U9000, U9050

### ENET胙LOWPWR_EN, ENET_PWR_S3AC, GPU_BB_CTL

- REF DES: U8400
- REF DES: U8400
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD -- ECM * 50

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9
TCK PULL DOWN THROUGH 54.9 OHM (FOLLOW UP XDP DESIGN REFERENCE)

IN
IO
IO
IO
IO
IO
IO
IO

PLACE GND VIA W/ IN 1000 MILS
ROUTE TO TP VIA AND

PLACE TESTPOINT ON

CPU_PROCHOT_L TO SMC

OUT

CPU_BSEL<2>
CPU_BSEL<0>

OUT

CPU_TEST1
**CPU Vcore HF and Bulk Decoupling**

- 4x 330µF, 20% 12V
- 2x 22µF 16V
- 1x 10µF, 1x 0.01µF

**VCCA (CPU AVdd) Decoupling**

- 16V, 20%
- 22µF
- 805
- 20%
- 6.3V
- CERM

**VCCP (CPU I/O) Decoupling**

- 0.1µF
- 402
- 10V
- 20%
- 2.5V

**CPU Vcore VID Connections**

- Resistors to allow for marking of CPU VID
- Will probably be removed before production

---

**NOTE:**

- This cap is shared between CPU and NB.
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S CONNECTOR'S FBO PIN.

AND WITH RESET BUTTON

TO ICH7M SYS_RST, AND WITH SYSTEM RESET LOGIC INDICATE THAT ITP IS USING TAP I/F, NC IN 945GM CHIPSET SYSTEM.

CRITICAL
NC
NC
NC
NC
52435-2872
518S0320

CPU ITP700FLEX DEBUG SUPPORT

SCALE
NONE

DRAWING NUMBER
051-7164 03001

SYNC_DATE=(MASTER) 11 87

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Unused DAC outputs should connect to GND through 75-ohm resistors.

VCCD_LVDS must remain powered with proper decoupling. Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used, leave all signals NC if LVDS is not implemented.
Place in cavity 4.7uF CERM
MIN_NECK_WIDTH=0.25 mm

0.1uF CERM

0.01uF

10uF 603

10V 20%

3200mA Max

3000mA Max

Rail Totals:

40mA Max?

2310mA Max?

1500mA Max

800mA Max

These are the power signals that leave the NB "block"

IN IN IN IN

PP3V3_S0

PP1V8_S3

PP1V5_S0_NB

GMCH VCCA_MPLL FILTER

GMCH VCC_HV BYPASS

MCH VCCA_3GBG BYPASS

MCH VCC_TXLVDS BYPASS

(MCH LVDS TRANSMITTER 2.5V PWR)

MAKE_BASE=TRUE

NO_TEST=TRUE

X5R 0.01UF

10V CERM

MIN_LINE_WIDTH=0.5 mm

1.0UH-220MA-0.12-OHM

10V

3GPLL 10uF cap should

NV sacred 0.01uf 2

TP_CRT_DDC_DATA

NC_NB_XOR_LVDS_A34 NC_NB_XOR_LVDS_A34

3X3 1210

3X3 91nH
This part is never stuffed, on the board to short or fault protection for RTC battery.
### DDR2 Bypass Caps

(For return current)

#### DDR2 SO-DIMM Connector B

- **SMBUS_SB_SDA**: 128
- **MEM_B_DQ**: 2000
- **MEM_B_DQS_P**: 0
- **MEM_B_DQS_N**: 1
- **MEM_B_DM**: 7
- **MEM_CS_L**: 2
- **MEM_B_BS**: 1
- **MEM_B_DQ**: 0
- **MEM_B_DQ**: 8
- **MEM_B_DQ**: 48
- **MEM_B_DQ**: 60
- **MEM_B_DQ**: 61
- **MEM_B_DQ**: 53
- **MEM_B_DQ**: 50
- **MEM_B_DQ**: 57
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- **MEM_B_DQ**: 30
- **MEM_B_DQ**: 26
- **MEM_B_DQ**: 17
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- **MEM_B_DQ**: 12
- **MEM_B_DQ**: 0
- **MEM_B_DQ**: 7
- **MEM_B_DQ**: 6
- **MEM_B_DQ**: 5
- **MEM_B_DQ**: 4
- **MEM_B_DQ**: 3
- **MEM_B_DQ**: 2
- **MEM_B_DQ**: 1

**Page Notes**

*Factory* (thru-hole) slot

- **6.3V**: 402
- **10%**: 402
One cap for each side of every RPAK, one cap for every two discrete resistors.

Mem_B_L and DD resistors are close to 62-65M connectors.

---

**Memory Active Termination**

**技术信息**

文件内容为机密信息，未经Apple计算机公司书面许可，不得复制或分发。
If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep. Leave 1.8V powered in S3. Okay to turn off 5V and (NONE) (NONE) (NONE) (NONE) Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Memory Vtt Supply
- PP5V_S0
- MEMVTT_EN
- PP1V8_S3
- MEMVTT_VREF
- PP0V9_S0

Refer to Apple's documentation for detailed instructions.
When ENETPWR_S3AC BOMOPTION is active:

State     FWPWR_EN_L       PM_SLP_S4_L      PM_SLP_S3BATT         PM_SLP_S3BATT_L       P2V5S3_EN               P1V2S3_RUNSS
S0 Batt       0V              3.3V             0V   (3.3V ON)        3.3V                   3.3V  (2.5V ON)          3.3V (1.2V ON)
G3H Batt     PBUS              0V              PBUS (3.3V OFF)        0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S5 Batt      PBUS              0V              PBUS (3.3V OFF)        0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S3 Batt      PBUS             3.3V             PBUS (3.3V OFF)        0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S3 AC         0V              3.3V             0V   (3.3V ON)        3.3V                   3.3V  (2.5V ON)          3.3V (1.2V ON)

G3H         0V             PBUS (3.3V OFF)       0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S5          0V             PBUS (3.3V OFF)       0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S3         3.3V            0V   (3.3V ON)        3.3V                  3.3V  (2.5V ON)         3.3V (1.2V ON)
S0         3.3V            0V   (3.3V ON)        3.3V                  3.3V  (2.5V ON)         3.3V (1.2V ON)

Yukon Power Control

When ENETPWR_S3 BOMOPTION is active:

State     PM_SLP_S4_L      PM_SLP_S3BATT         PM_SLP_S3BATT_L       P2V5S3_EN               P1V2S3_RUNSS
G3H Batt     PBUS              0V              PBUS (3.3V OFF)        0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S5 Batt      PBUS              0V              PBUS (3.3V OFF)        0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S3 Batt      PBUS             3.3V             PBUS (3.3V OFF)        0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S3 AC         0V              3.3V             0V   (3.3V ON)        3.3V                   3.3V  (2.5V ON)          3.3V (1.2V ON)
S0 Batt       0V              3.3V             0V   (3.3V ON)        3.3V                   3.3V  (2.5V ON)          3.3V (1.2V ON)
S0 AC         0V              3.3V             0V   (3.3V ON)        3.3V                   3.3V  (2.5V ON)          3.3V (1.2V ON)

G3H         0V             PBUS (3.3V OFF)       0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S5          0V             PBUS (3.3V OFF)       0V                    0V (2.5V OFF)           0V  (1.2V OFF)
S3         3.3V            0V   (3.3V ON)        3.3V                  3.3V  (2.5V ON)         3.3V (1.2V ON)
S0         3.3V            0V   (3.3V ON)        3.3V                  3.3V  (2.5V ON)         3.3V (1.2V ON)

Allows powering Yukon down during battery sleep to save power
Enables port power when machine is running or on AC.

Current Limit/Active Late-VG Protection

Late-VG Event Detection

Port Power Switch

Double port power when machine is running or on AC.

Budgets current (current mode of operation constant)
for 100 samples (each sample 100 ms) in weighted
as in 1.2 and the limits can vary during the period
and 1/10th of the limits. In a real-time, the device
needs to be able to detect a fault that produces possible current
spikes. Current limit has been set higher to compensate.
**Page Notes**

- Page 1 of 1
- Check design layout in this page.
- Additional notes here.

---

### Late-VG Protection Power

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**Termination**

- Place wires to Termination FRU.

---

**Note:** The wiring schematic is not exhaustive. Additional notes and details are provided in the text.
Current Sense Calibration Circuit

- CPU Voltage Sense / Filter
- GPU Voltage Sense / Filter
- CPU Current Sense Filter
- GPU Current Sense Filter
- 1.5V 50 (NB) Current Sense Filter
- 1.05V 50 (NB) Current Sense Filter
- DCIN Current Sense Filter
- Battery Current Sense Filter

Current & Voltage Sensing

- CPU Voltage Sense
- GPU Voltage Sense
- CPU Current Sense
- GPU Current Sense
- 1.5V 50 (NB) Current Sense
- 1.05V 50 (NB) Current Sense
- DCIN Current Sense
- Battery Current Sense
If unconnected, powers up with PVIN.

Vout = 0.6V * (1 + Ra / Rb)

Vout = 2.5V * (1 + Ra / (Rb + Rc))

Vout = 2.50V (U7700 limit)

Vout = 1.205V (Switcher limit)

Continuous

---

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SHT
Vref = 3.42V * (R2a / (R1a + R2a))
Vref = 1.20V
Vth = 13.4V
Vth = (Vref / (R2b / (R1b + R2b))

Vref = 3.42V * (R2a / (R1a + R2a))
Vref = 1.20V
Vth = 13.4V
Vth = (Vref / (R2b / (R1b + R2b))
As shown, $I_{sys} \approx 4.6A$ max.
Revision History

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Revision History

Sync Date = (Master)

Sync Master = (Master)

Revision History
**Napa Platform Constraints**

**FSB (Front-Side Bus) Constraints**

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

**SOURCE:** Napa Platform DG, Rev 0.9 (#17978), Section 6.2

**NOTE:** Design Guide allows closer spacing if signal lengths can be shortened.

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**LINE-TO-LINE SPACING**

**ON LAYER?**

- = 1.5:1 SPACING
- = 2:1 SPACING
- = 3:1 SPACING
- = 4:1 SPACING

**Napa Platform Instructions**

**MAXIMUM NECK LENGTH**

**MINIMUM LINE WIDTH**

**MINIMUM NECK WIDTH**

**AREA_TYPE**

**SPACING_RULE_SET**

**TABLE_SPACING_ASSIGNMENT_ITEM**

**SYNC_DATE=(MASTER)**

**DRAWING NUMBER**

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High-Speed I/O Interface Constraints

LVDS and TMDS pairs should be kept at least 25 mils apart.
LVDS and TMDS signals are 100-ohm +/- 10% differential impedance.

GROUND Shield recommended around VGA signals.

Video Signal Constraints

CTRL lines are 55-ohm single-ended impedance.

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

VGA should be routed as close to 75-ohms single-ended impedance as possible.

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.
### M9 Board-Specific Spacing & Physical Constraints

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**Notes:**
- For "Spacing Rule Set" for FSB signals, Appendix D tables D-1 & 4-12.
- For "Spacing Rule Set" for MEM signals, Appendix D tables D-1 & 4-12.

### Board Areas
- Standard: Top, Bottom

### Minimum Line Width
- 0.090 mm
- 0.100 mm

### Minimum Neck Width
- 0.076 mm

### Maximum Neck Length
- 0.125 mm

### Physical Rule Set
- Standard: Y

### Table Physical Rule Item

### Table Physical Assignment Item

### Table Spacing Rule Item
- 0.100 mm
- 0.100 mm

### Table Spacing Assignment Item

### Table Spacing Rule Override
- 0.3 mm

### Table Spacing Rule Head

### Table Spacing Assignment Head

### Table Spacing Override

### Table Spacing Rule Override

### Table Spacing Assignment Override

### Unsupported Rule

### Scale - Physical / Spacing Types

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