1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRystals & DIODE VALUE ARE IN HRETS.
# BOM Variants

<table>
<thead>
<tr>
<th>BOM Number</th>
<th>BOM Name</th>
<th>BOM Options</th>
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<tbody>
<tr>
<td>630-7044</td>
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## M76 BOM Groups

<table>
<thead>
<tr>
<th>BOM Group</th>
<th>BOM Options</th>
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</thead>
<tbody>
<tr>
<td>M76_COMMON</td>
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<tr>
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</tr>
</tbody>
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## Bar Code Labels / EEE #'s

<table>
<thead>
<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Des</th>
<th>CRITICAL</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>B260-0732</td>
<td>2</td>
<td>LBL(ICON)</td>
<td>LBL(ICON)</td>
<td>CRITICAL</td>
<td>SPR_XBP</td>
</tr>
<tr>
<td>B260-0733</td>
<td>2</td>
<td>LBL(ICON)</td>
<td>LBL(ICON)</td>
<td>CRITICAL</td>
<td>SPR_XBU</td>
</tr>
<tr>
<td>B260-0734</td>
<td>2</td>
<td>LBL(ICON)</td>
<td>LBL(ICON)</td>
<td>CRITICAL</td>
<td>SPR_XBT</td>
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</tbody>
</table>

## Module Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Des</th>
<th>CRITICAL</th>
<th>BOM Option</th>
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## Alternate Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>QTY</th>
<th>Description</th>
<th>Reference Des</th>
<th>CRITICAL</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>23301070</td>
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<td>0,00250000, 16 MBIT</td>
<td>16 MBIT</td>
<td>CRITICAL</td>
<td>SPR_XBP</td>
</tr>
<tr>
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<td>0,00250000, 16 MBIT</td>
<td>16 MBIT</td>
<td>CRITICAL</td>
<td>SPR_XBU</td>
</tr>
<tr>
<td>23301090</td>
<td>1</td>
<td>0,00250000, 16 MBIT</td>
<td>16 MBIT</td>
<td>CRITICAL</td>
<td>SPR_XBT</td>
</tr>
</tbody>
</table>

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3/19/07 -- Added three 0603 0 ohm resistors R4740-R4742 for EMC return current path.

3/19/07 -- Deleted R7324 and made C7324 0603 size, still 0.1μF (132S0100).

Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail.

Changes since previous major release (13.4.0):

- Charger PWM limit resistor changed according to MARC K.'s M50 values.

3/08/07 -- Integrated CSA pg. 79 through:

- Battery charge current limit circuit changes.

Changes since previous fab release (14.0.0):

3/28/07 -- Integrated m75/mlb CSA pg. 87 through:

- Changed BOM option on R9960 511K from NOSTUFF to INV_SPLIT to improve current and voltage asymmetry ratio.

3/22/07 -- Modified R7222 and R7221 to be one resistor for 51.1K.

3/21/07 -- Removed R7521.

3/21/07 -- Moved -PP1V8_GPU_P1V8GPUFET from PP1V8_S3_ISNS to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.

3/21/07 -- Changed BOM options for R7520 to choose between 1.8V or 1.825V 0.1% resistors.

3/20/07 -- Removed NOSTUFF BOM option from R7521.

3/19/07 -- Changed BOM option on R7520 to choose between 1.8V or 1.825V 0.1% resistors.

3/18/07 -- Removed BOM option for HDCP as feature is removed.

3/17/07 -- Removed BOM option F149011Y2K2 from M76_CORDIG BOM group.

3/17/07 -- Added Q7970 for potential battery inrush current.

3/17/07 -- Added D7903 for voltage ripple on ISL6257 BOOT and PHASE pins.

3/17/07 -- Changed R8925 to 16.9K.

3/17/07 -- Changed table text notes.

3/16/07 -- Changed resistor for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.125V, 1.25V).

3/15/07 -- FireWire Ports: Changed D4260 to PDS540 for higher current capacity.

3/14/07 -- Integrated m75/mlb pages 25,42,70 through:

- LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882).

3/14/07 -- Removed BOM option on R9960 511K from M76_CORDIG to improve current and voltage asymmetry ratio.

3/13/07 -- Battery charge current limit circuit changes.

3/12/07 -- Added R7920 and R7921 to be one resistor for 51.1K.

3/12/07 -- Cleaned up unused aliases.

3/12/07 -- Changed 1.8V feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.

3/11/07 -- Changed BOM option on R7520 to choose between 1.8V or 1.825V 0.1% resistors.

3/10/07 -- Cleaned up unused aliases.

3/10/07 -- Changed firewire ports to PDS540 for higher current capacity.

3/10/07 -- Changed D7903 for voltage ripple on ISL6257 BOOT and PHASE pins.

3/09/07 -- Changed table text notes.

3/09/07 -- Removed BOM option for HDCP as feature is removed.

3/08/07 -- Changed BOM option F149011Y2K2 to M76_CORDIG BOM group.

3/08/07 -- Moved -PP1V8_GPU_P1V8GPUFET from PP1V8_S3 to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.

3/08/07 -- Removed R7521.

3/07/07 -- Removed D7903 for voltage ripple on ISL6257 BOOT and PHASE pins.

3/07/07 -- Changed charger PWM limit resistor to improve current and voltage asymmetry ratio.

3/07/07 -- Changed charger PWM limit resistor to improve current and voltage asymmetry ratio.

3/07/07 -- Removed BOM option F149011Y2K2 from M76_CORDIG BOM group.

3/07/07 -- Added R7920 and R7921 to be one resistor for 51.1K.

3/07/07 -- Removed R7521.

3/07/07 -- Removed BOM option for HDCP as feature is removed.

3/07/07 -- Changed BOM option F149011Y2K2 to M76_CORDIG BOM group.

3/07/07 -- Moved -PP1V8_GPU_P1V8GPUFET from PP1V8_S3 to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.

3/07/07 -- Removed R7521.

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3/07/07 -- Removed BOM option F149011Y2K2 from M76_CORDIG BOM group.

3/07/07 -- Added R7920 and R7921 to be one resistor for 51.1K.

3/07/07 -- Removed R7521.

3/07/07 -- Removed BOM option for HDCP as feature is removed.

3/07/07 -- Changed BOM option F149011Y2K2 to M76_CORDIG BOM group.

3/06/07 -- Changed BOM option F149011Y2K2 to M76_CORDIG BOM group.

3/05/07 -- Removed BOM option F149011Y2K2 from M76_CORDIG BOM group.

3/05/07 -- Moved -PP1V8_GPU_P1V8GPUFET from PP1V8_S3 to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.

3/05/07 -- Removed R7521.

3/05/07 -- Changed charger PWM limit resistor to improve current and voltage asymmetry ratio.

3/05/07 -- Changed charger PWM limit resistor to improve current and voltage asymmetry ratio.

3/05/07 -- Removed BOM option F149011Y2K2 from M76_CORDIG BOM group.

3/05/07 -- Added R7920 and R7921 to be one resistor for 51.1K.

3/05/07 -- Removed R7521.

3/05/07 -- Removed BOM option for HDCP as feature is removed.

3/05/07 -- Changed BOM option F149011Y2K2 to M76_CORDIG BOM group.

3/04/07 -- Changed BOM option F149011Y2K2 to M76_CORDIG BOM group.

3/04/07 -- Moved -PP1V8_GPU_P1V8GPUFET from PP1V8_S3 to PP1V8_S3. This is to remove the current sense resistor from the GPU 1.8V path.

3/04/07 -- Removed R7521.

3/04/07 -- Changed charger PWM limit resistor to improve current and voltage asymmetry ratio.

3/04/07 -- Changed charger PWM limit resistor to improve current and voltage asymmetry ratio.

3/04/07 -- Removed BOM option F149011Y2K2 from M76_CORDIG BOM group.

3/04/07 -- Added R7920 and R7921 to be one resistor for 51.1K.

3/04/07 -- Removed R7521.

3/04/07 -- Changed charger PWM limit resistor to improve current and voltage asymmetry ratio.

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3/04/07 -- Added R7920 and R7921 to be one resistor for 51.1K.

3/04/07 -- Removed R7521.
### Functional Test Points

**Fan Connectors**
- LPC+ Debug Connector
- Left I/O Power Connector
- Left Clutch Barrel Connector
- Thermal Diode Connectors
- System Validation TPs

**Battery Digital Connector**
- LPC+ Debug Connector
- Left I/O Power Connector
- Left Clutch Barrel Connector
- Other Func Test Points

**RTC Battery Connector**
- Current Sense Calibration
- Inverter Connector
- IR & Sleep LED Connector
- Other Func Test Points

### ICT Test Points

**CPU FSB NO_TESTS**
- NB_NO_TESTSs
- GPU NO_TESTSs

**Inverter Connector**
- Functional / ICT Test

**Functional / ICT Test**

---

**Notes:**
- Request for at least 10 GND test points
- Request for at least 10 GND test points
- Request for at least 10 GND test points
- 10 additional GND test points are available on connectors B, C, and D.

---

**Identifiers:**
- B: 051-7441
- C: 7
- D: 109

---

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Thermal Module Holes

All holes are plated through holes with two exceptions:

Chassis GNDs

Digital Ground

RAM door (Torx) holes

Frame holes

SignalAliases

Min Neck Width=0.25 mm
Min Line Width=0.6 mm
Voltage=0V
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0651 adapter board to support CPU, NB & 2X debugging.

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300
Leave GFX_VID<3..0> and GFX_VR_EN as NC.
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore). 
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
TV_DCONSELx to GND.
VSYNC and CRT_TVO_IREF to GND.
Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC,
All CRT/TVDAC rails must be powered. All CRT Disable / TV-Out Enable share filtering with VCCA_CRT_DAC.
Tie TVx_DAC and TVx_RTN to GND. Must power all should connect to GND through 75-ohm resistors.
Component: DACA, DACB & DACC
S-Video: DACB & DACC only
Unused DAC outputs must remain powered, but can
omit filtering components. Unused DAC outputs
should power all 75-ohm resistance.
TV-Out Disable / CRT Enable
Tie TVA_JAC and TVA_RST to GND: Must power all 
VCCx rails. VCCx is VCCx and VCCA_JAC then can
power the TVA_JAC and TVA_RST.
8 7 6 5 4 3 2 1

20 mA
50 mA
100 mA
5 mA
100 mA
100 mA
640 mA (5/7MHz 22)
500 mA (5/3MHz 22)
60 mA
60 mA
60 mA
60 mA
200 mA
425 mA
515 mA
770 mA @ 667MHz FSB (1.05V)
850 mA @ 800MHz FSB (1.05V)
TBD mA @ 1067MHz FSB (1.25V)

S0 or S3M is acceptable

=PP1V05_S0_NB_VCCRXRDMI
=PP3V3_S0_NB_VCCHV
=PP1V8_S0_NB_VCCTXLVDS
=PP1V25_S0M_NB_VCCAXF
=PP1V25_S0M_NB_VCCAXD
=PP1V25R1V05_S0_NB_VTT

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Crestline Thermal Diode Pins

Mainly for investigation; if not used, alias these nets directly to GND.

NOTE: TDB = _N
NOTE: TDE = _P

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SYNC_MASTER=T9_NOME SYNC_DATE=01/25/2007

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NB Grounds

D

NONE

REV.

051-7461 16

APPLD COMPUTER INC. D 051-7461 14
Current numbers from Crestline EDS Addendum, doc #20127.

VCCD_TVDAC also powers internal thermal sensors.

NOTE: This filter is required even if using only external graphics.

865 mA = PP1V5_S0_NB_TVDAC

8 7 4

2200 µF 402
CERM 10V 20%

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.3 MM

NFM18 16V 2

100 mA (1.7V - 5.5V)

within 6.35 mm of NB edge

These 2 caps should be

Layout Note:

= PPVIN_S0_NB_DPLL

VOLTAGE=1.25V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.4 MM

= PP1V25_S0_NB_DPLL

VOLTAGE=1.25V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.4 MM

= PP1V8_S0_NB_VCCD_TVDAC

= PP1V8_S0_NB_LVDS

GMCH Graphics Core

= TV_C_RTN

= TV_C_DAC

= TV_B_RTN

= TV_B_DAC

= TV_A_DAC

= CRT_TVO_IREF

= CRT_VSYNC_R

= CRT_BLUE_L

= CRT_GREEN_L

= CRT_GREEN

= CRT_RED_L

= CRT_RED

= CRT_DDC_DATA

= CRT_DDC_CLK

= SDVO_CTRLCLK

= SDVO_CTRLDATA

= TV_DCONSEL<1>

TANT 2.5V D2T 20%

2.37K

4.7

5%

50V 10%

C2260 603 X5R 6.3V 20%

1 2

C2261 603 X5R 6.3V 20%

CRITICAL

1.0UH-0.5A

1 2

CRITICAL

1 2

CRITICAL

1 2

1 2

CRITICAL

1 2

CRITICAL

1 2

0.1uF

402

CERM 10V 20%

VOLTAGE=1.25V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.2 MM

= PP1V8_S0_NB_VCCD_LVDS

C2223 0.001UF 402 MF-LF

5%

402 MF-LF

5%

TANT 2.5V D2T 20%

2.5V D2T 20%

2.5V D2T 20%

1UF 0.001UF

CERM 6.3V 10%

CERM 6.3V 10%

3 U4F 0.01UF 402 CRITICAL

1210 470UF TANT

2.5V D2T 20%

C2265 1UF 0.001UF

CERM 6.3V 10%

CERM 6.3V 10%

1 2

C2210 470UF

470UF

CERM 6.3V 20%

TANT 2.5V D2T 20%

C2211 470UF

C2212 22UF CERM-X5R 6.3V 20%

22UF CERM-X5R 6.3V 20%

5%

5%

0.1uF 0.1uF

1 2

1 2

1 2

1 2

1 2
RTC Power Sources

Platform Reset Connections

Unbuffered

SB RTC Crystal

System Reset "Button"

VRMPWRGD Inverter

PWROK Circuit

CPU VCore ForcePSI

Platform Reset Connections

CPU_RESET_R_L

PB_ALL_GPU_PGOOD)

on power down:

This ensures that GPU is put into isolated signals due to sharp edges on VCC and clocks are still running.

PCI Reset Connections

PCI_RST_L

ON POWER DOWN:

This delay ensures that GPU clocks run before GPU is released from reset. RC should be added to trigger and prevent false triggers at the low frequency. R should be tuned to achieve the threshold at approx .8 ms nominal.

This ensures that GPU is put into isolated signals due to sharp edges and VCC. RC prevents glitching of the system. RC prevents glitching of the system.

Muxed GFX GPU Reset Support

ON POWER DOWN:

This ensures that GPU is put into isolated signals due to sharp edges and VCC. RC prevents glitching of the system.
One cap for each side of every RP4K, one cap for every two discrete resistors

Ensure C3_L and C3_T resistors are close to RO-C001M connector.
Page Notes

- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)

- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY

- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps

To support Yukon EC and Ultra on the same board:

- Alias -YUKON_UC_PP2V5_ENET to PP1V8R2V5_ENET_PHY, add 1x 0.1uF and 1x 0.001uF caps
- Use Yukon Ultra: Alias to GND
- Use =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMoptions to select stuffed part

Page Notes

- See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

Circuit symbols required by this page:

-晶体管
-IC
-电阻
-电容
-电源
-连接器
-逻辑门
-混合信号

Signal aliases required by this page:

- =ENET_VMAIN_AVLBL (See note by pin)
- =PP3V3_ENET_PHY

Page Notes

- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

Note:

- Yukon EC

Page Notes

- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

Note:

- Yukon EC

Page Notes

- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

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- Yukon EC

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- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

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- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

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- Yukon EC

Page Notes

- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

Note:

- Yukon EC

Page Notes

- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

Note:

- Yukon EC

Page Notes

- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

Note:

- Yukon EC

Page Notes

- SEE YUKON_EC_PP2V5_ENET_TO_PP1V8R2V5_ENET_PHY

Note:

- Yukon EC
ENET Enable Generation

NOTE: S3 term is guaranteed by pull-up source, MUST BE S3 RAIL.

3.3V ENET FET

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

WLAN Enable Generation

NOTE: S3 term is guaranteed by pull-up source, MUST BE S3 RAIL.

Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests

Yukon Crystal

Yukon Power Control
Transformers should be mirrored on opposite sides of the board.

Place one cap at each pin of transformers.

- Place close to connector.
- Short shielded RJ-45.

**Ethernet Connector**

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

**C3900**

**C3901**

**C3902**

**C3903**

**R3900**

**R3901**

**R3902**

**R3903**

Ethernet Connector

- ENET_CONNECT
- ENET_CONNECT_P
- ENET_CONNECT_N

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

- ENET_MDI_P
- ENET_MDI_N

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

- Ethernet Connector

**C3904**

**C3905**

**C3906**

**C3907**

**R3900**

**R3901**

**R3902**

**R3903**

Ethernet Connector

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

- ENET_MDI_P
- ENET_MDI_N

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

- Ethernet Connector

**C3904**

**C3905**

**C3906**

**C3907**

**R3900**

**R3901**

**R3902**

**R3903**

Ethernet Connector

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

- ENET_MDI_P
- ENET_MDI_N

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

- Ethernet Connector
Strap via alias on port page.

Lo: Beta Mode enable (1394b).

Hi: Data-Strobe only (1394a).

DSx Straps:
- Implement 1K pull-up or pull-down on port page.

Multi-port Portable systems are Power Class 4 ("100").
Single-port / Desktop systems are Power Class 0 ("000").
FireWire PHY Config Straps

- Configure PHY for:
  - 2-port Portable Power Class (4)
  - Port "0" Data-Strobe only (1394A)
  - Port "1" Bilingual (1394B)

Termination

Place close to FireWire PHY

SIGNAL_MODEL=EMPTY

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PORT 1

1394A
CRITICAL

L4300

J4310
F-RT-SM1

SYNC_MASTER=M75_MLB
SYNC_DATE=12/04/2006

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Port Power Switch

Right USB Port

USB/SMC Debug Mux

External USB Connector

SYNC_MASTER=M75_MLB  SYNC_DATE=12/04/2006

External USB Connector

If power source is S3, can tie EN to IN.

SEL=0 Choose SMC

SEL=1 Choose USB

Place L4600 and L4605 across most
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**Left Clutch Barrel Interconnect**

- Connector shield
- Camera Power
- Camera Ground
- Camera TwinAX Shield 1

**SIM Interconnect**

- Connector shield
- WWAN SIM Clock
- WWAN SIM Data
- WWAN SIM Reset
- WWAN Power
- WWAN Ground
- Camera Power
- Camera Ground
- Camera USB D-
- Camera TwinAX Shield
- WWAN USB D-
- WWAN USB D+
- USB_WWAN_F_P
- USB_WWAN_F_N
- USB_CAMERA_F_P
- USB_CAMERA_F_N
- USB_EXTD_F_P
- USB_EXTD_F_N
- M5TICK
- USB_CAMERA_P
- USB_CAMERA_N
- USB_EXTD_P
- USB_EXTD_N
- MAKE_BASE
- PP5V_S3_CAMERA
- PP5V_S3_WWAN
- VOLTAGE=5V
- MIN_LINE_WIDTH=0.25 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.25 mm
- MIN_NECK_WIDTH=0.2 mm
- PPVCC_WWAN_SIM
- PP5V_S3_WWAN_F
- PP5V_S3_WWAN
- USB_WWAN_P
- USB_WWAN_N
- USB_EXTD_P
- USB_EXTD_N
- MAKE_BASE
- PP5V_S3_CAMERA
- PP5V_S3_WWAN
- VOLTAGE=5V
- MIN_LINE_WIDTH=0.25 mm
- MIN_NECK_WIDTH=0.2 mm
- PPVCC_WWAN_SIM
- PP5V_S3_WWAN_F
- PP5V_S3_WWAN
- USB_WWAN_P
- USB_WWAN_N
- USB_EXTD_P
- USB_EXTD_N
- MAKE_BASE
- PP5V_S3_CAMERA
- PP5V_S3_WWAN
- VOLTAGE=5V
- MIN_LINE_WIDTH=0.25 mm
- MIN_NECK_WIDTH=0.2 mm
- PPVCC_WWAN_SIM
- PP5V_S3_WWAN_F
- PP5V_S3_WWAN
- USB_WWAN_P
- USB_WWAN_N
- USB_EXTD_P
- USB_EXTD_N
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- PP5V_S3_WWAN
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- MIN_LINE_WIDTH=0.25 mm
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- PPVCC_WWAN_SIM
- PP5V_S3_WWAN_F
- PP5V_S3_WWAN
- USB_WWAN_P
- USB_WWAN_N
- USB_EXTD_P
- USB_EXTD_N
- MAKE_BASE
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designated as inputs can be left floating. Those designated as inputs require pull-ups.
LPC+ Connector

FWH_INIT_L Generation

PLACEMENT_NOTE=Place Q5190 close to R5190

PLACEMENT_NOTE=Place R5190 to minimize CPU_INIT_L stub

SYNC_MASTER=M75_MLB
SYNC_DATE=12/04/2006

LPC+ Debug Connector

SMC_TX_L
SMC_MD1
SMC_TDO
SMC_TRST_L
DEBUG_RESET_L
LINDACARD_GPIO
SMC_RX_L
SMC_NMI
SMC_RESET_L
SMC_TCK
SMC_TDI
PM_SUS_STAT_L
INT_SERIRQ
LPC_AD<3>
LPC_AD<2>
LPC_AD<1>
LPC_AD<0>
PCI_CLK33M_LPCPLUS
FWH_INIT_L
CPU_INIT_R_L
CPU_INIT_LS3V3
CPU_INIT_L
=PP3V3_S0_LPCPLUS
=PP5V_S0_LPCPLUS

A B C D
1 2 3 4 5 6 7 8

51620394
Sudden Motion Sensor (SMS)

I2C addresses:
- Addr low -> $0x30, $0x31
- Addr high -> $0x32, $0x33
- Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
- Top-through View

Desired orientation when placed on board bottom-side:
- Package Top

- SMS_X_AXIS = I2C_SMS_SDA
- SMS_Y_AXIS = I2C_SMS_SCL
- SMS_Z_AXIS = I2C_SMS_SCL
- SMS_ONOFF_L = SMS_MOT_DIS
- SMS_MOT_EN = SMS_MOT_EN

APN: 338S0354

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SO
VDD
SCK
CE*
WP*
HOLD*
VSS
SI
OUT
IN
IN
IN
IN
SIZE
D
SHT OF
DRAWING NUMBER
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APPLE COMPUTER INC.
REV.
SCALE
NONE
20%
CERM
C6100
0.1UF
10V
5
R6101
15
5%
1/16W
402
R6100
3.3K
MF-LF
2
1
5%
1/16W
402
R6114
15
1 2
86 24
86 24
PLACEMENT_NOTE=Place R6114 within 12.7mm of U6100
PLACEMENT_NOTE=Place R6190 within 12.7mm of U2300
PLACEMENT_NOTE=Place R6191 within 12.7mm of U2300
PLACEMENT_NOTE=Place R6193 within 12.7mm of U2300

SPI BootROM
SYNC_MASTER=T9_NOME
SYNC_DATE=01/25/2007
SPI_SI_R
SPI_SO
SPI_HOLD_L
SPI_CE_L<0>
SPI_A_SI_R
SPI_WP_L
SPI_A_SO_R
SPI_SCLK
SPI_SCLK_R
SPI_CE_R_L<0>
86
8
86
86
86
86
**DC-In Connector**

**Battery Connector**

**Inrush Limiter**

**AC Detection**

**NOTE:** R6910 is on LIO.

System must provide 10k-70k impedance to AC adapter for system load detection.

Reg of R6910 is on LIO; R6912, R6913 is 36Wk.

Vref = 3.42V * (R2a / (R1a + R2a))

Vth = (Vref / (R2b / (R1b + R2b)))

Vref = 1.23V

Vth = 13.0V

Assuming 1% variance for R6910-R6915 and 3.42V:

Worst case Vth: min:12.47V, max: 13.54V

**WARNING:**

- Do not expose or store the component to moisture or dust.
- Do not apply excessive force or pressure to the component.
- Do not operate the component beyond the specified rating.

**ACOK_AND_PS_ON**

**SMC_ADAPTER_EN**

**VOLTAGE=18.5V**

**PP18V5_G3H_DCCتخل**

**MIN_LINE_WIDTH=0.2mm**

**MIN_NECK_WIDTH=0.2mm**

**MAKE_BASE=TRUE**

**ACIN_DISABLE_DIV_L**

**ACIN_DISABLE_DIV2_L**

**MIN_LINE_WIDTH=0.6mm**

**MIN_NECK_WIDTH=0.2mm**

**VOLTAGE=18.5V**

**PP18V5_G3H_DCCتخل**

**MIN_LINE_WIDTH=0.60mm**

**MIN_NECK_WIDTH=0.20mm**

**MAKE_BASE=TRUE**

**ACIN_DISABLE_DIV_L**

**ACIN_DISABLE_DIV2_L**

**VOLTAGE=18.5V**

**PP18V5_G3H_DCCتخل**

**MIN_LINE_WIDTH=0.6mm**

**MIN_NECK_WIDTH=0.2mm**

**MAKE_BASE=TRUE**
PLACEMENT NOTE=Place XW7320 next to C7350.

8A max output (L7320 limit)

Vout = 5.0V

330UF 6.3V 20% =PP5V_S5_REG

10UF 805-2 CERM 10V 20% =PPVIN_S5_P5VS5

CRITICAL CASE-D2-LF

22UF XW7320 SM 20% IHLP2525CZ-SM SI7108DNS 2.2UH-14A PWRPK-1212-8

CRITICAL

Q7320

1UF 603 25V 10% C7341

MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.2 mm

VOLTAGE=0V

R7325 4.22K 4.7 MF-LF 1% MF-LF 1/16W 5%

CRITICAL GATE_NODE=TRUE SWITCH_NODE=TRUE

5V Fixed GND_P5VS5_PGND P5VS5_CS P5VS5_DRVL P5VS5_LL P5VS5_DRVH P5VS5_VBST

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable

=PP5V_S5_EN5 =P5VP3V3_EN5 =P3V3S5_EN =P3V3S5_PGOOD =P5VS5_PGOOD =P5VS5_EN

GATE_NODE=TRUE SWITCH_NODE=TRUE

5V Fixed GND_P5VP3V3_SGND P5VP3V3_CS P5VP3V3_DRVL P5VP3V3_LL P5VP3V3_DRVH P5VP3V3_VBST

When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable

5.5A max output (L7360 limit)

Vout = 3.3V

3.57K MF-LF 1/16W 5%

MIN_NECK_WIDTH=0.6 mm MIN_LINE_WIDTH=0.2 mm

VOLTAGE=5V

CRITICAL

O7360

1UF 603-1 X7R 50V 10% XW7365 SM 20% IHLP

CRITICAL

Q7360

SI7114DN PWRPK-1212-8

CRITICAL

Q7365

24 17 25 16 26 15 27 14 30 11 28 13 31

CRITICAL

VIN SYM (3 OF 3) U7300 LLP VREG5

5V / 3.3V Power Supply

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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CRITICAL

O7380

22UF C7392 CASE-B2 POLY 6.3V 20%

CRITICAL

C7390

10UF X5R 6.3V 20% L7360 limit

5.5A max output

Vout = 3.3V

3.57K MF-LF 1/16W 5%

402 V5FILT

GND THRML_PAD 5

CRITICAL

VIN

SYM (3 OF 3) U7300 LLP VREG5

5V / 3.3V Power Supply

SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006

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CRITICAL
Vout = 0.75V \times (1 + \frac{R_a}{R_b})

\[ V_{out} = 1.50V \]

8A max output (L7620 limit)

5%

CERM

NO STUFF

C7610

100PF

50V

402

1

2

6

3

2

1

8

7

4

3

2

1

8

7

6

5

4

3

2

1

CRITICAL

C7620

22UF

20%

25V

POLY

CASE-D2-LF

1

2

CRITICAL

C7632

330UF

2.5V

CASE-D2E-LF

1

2

402

2

1

1UF

10V

X5R

C7600

10%

1

2

R7601

200

1%

1/16W

MF-LF

C7601

16V

1

2

200K

1%

1/16W

MF-LF

C7621

25V

X5R

1

2

CRITICAL

Q7620

SI7114DN

PWRPK-1212-8

5

4

1 2 3

CRITICAL

Q7625

SI7108DNS

PWRPK-1212-8

5

4

1 2 3

1UF

10%

603

1

2

CRITICAL

IHLP2525CZ-SM

L7620

1.0UH-22A

1 2

1.5V Power Supply

SYNC_MASTER=M75_MLB

SYNC_DATE=03/05/2007

PP1V5_S0_VDDQSNS

=PP1V5_S0_REG

P1V5S0_TRIP

=PP1V5_S0_REG

GND_P1V5S0_SGND

MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.25 mm

VOLTAGE=0V

MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.2 mm

PP5V_S5_P1V5S0_V5FILT

VOLTAGE=5V

MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.2 mm

P1V5S0_VFB

MIN_NECK_WIDTH=0.2 mm

GATE_NODE=TRUE

MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.2 mm

P1V5S0_DRVH

GATE_NODE=TRUE

MIN_LINE_WIDTH=0.6 mm

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.2 mm

MIN_NECK_WIDTH=0.2 mm

P1V5S0_LL

SWITCH_NODE=TRUE

MIN_LINE_WIDTH=0.6 mm

P1V5S0_TON

P1V5S0_VBST

MIN_LINE_WIDTH=0.25 mm

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.2 mm
3.3V FW PHY Supply

Vout = 3.316V
20mA max output
(Switcher limit)

Vout = 1.25V \times (1 + \frac{R_a}{R_b})

1.95V FW PHY Supply

Backup power in case of FW bus
VP short to keep PHY powered.

FW PHY Power Supplies

SYNC_MASTER=M75_MLB
FW PHY Power Supplies
SYNC_DATE=12/04/2006

CRITICAL
U7720
LT3470
TSOT23-8

CRITICAL
L7700
CDPH4D19F-SM
3.425V "G3Hot" Supply

Supply needs to guarantee 3.3V delivered to SMC VRef generator

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

Other S0 Rails PWRGD Circuit

Does not include S0 rails

Unused PGOOD Signals

- NOT USED

- CRITICAL

- NO STUFF

- SCALE

- SIZE

- DRAWING NUMBER

- REV.

- SHEET

- DATE

- ISSUE

- PART NUMBER

- REVISION

- BOM

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- TRADEMARKS

- NUMBER OF ORIGINAL SHEETS

- NUMBER OF SHEETS

- WORKING DRAWING

- PACKAGE

- POWER CONTROL SIGNALS
null
LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

GPU LVDS I/F

Mux Select Conditioning

NOTE: Make sure selected output is not grounded (PDN = 0V) until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset or deasserted). Could be eliminated if GPIO moved to resume well.

Panel/Backlight Control Mux

NOTE: New H/M and D/W challenge since NB gfs might be powered on if selecting advanced GPU. For all three to guarantee that the "inter" device is ready before a switch can occur. If any selected FET is rail to rail core well, this could mean powering up to supply will be necessary before going to sleep to keep PGOD delays provided.
PWM does not glitch during RESET.

PLT_RST_L input ensures backlight...
**CPU / FSB Net Properties**

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
<td>FSB_ADDR &amp; FSB_DSTB</td>
<td>7 MIL</td>
<td>7 MIL</td>
<td>STANDARD</td>
<td>STANDARD</td>
<td>STANDARD</td>
</tr>
<tr>
<td>FSB_DATA &amp; FSB_DSTB</td>
<td>7 MIL</td>
<td>7 MIL</td>
<td>STANDARD</td>
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<td>STANDARD</td>
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</tbody>
</table>

**CPU Signal Constraints**

- **CPU_VCCSENSE**
  - Prop.: 27P4_OHM_SE
  - Pred.: 27P4_OHM_SE

**SOURCE:** Santa Rosa Platform D2, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

---

**CPU / FSB Net Properties**

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</tr>
<tr>
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**CPU Signal Constraints**

- **CPU_VCCSENSE**
  - Prop.: 27P4_OHM_SE
  - Pred.: 27P4_OHM_SE

**SOURCE:** Santa Rosa Platform D2, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4
**CRT & TVDAC signal single-ended impedence varies by location:**

LVDS signals are 100-ohm +/- 20% differential impedence.

**CRT HSYNC/CRT VSYNC signals are 55-ohm +/- 15% single-ended impedence.**

- 55-ohm +/- 15% from second termination resistor to connector.
- 50-ohm +/- 15% from first to second termination resistor.
- 37.5-ohm +/- 15% from GMCH to first termination resistor.

**PCI-Express / DMI Bus Constraints**

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<tbody>
<tr>
<td>PHYSICAL_RULE_SET</td>
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**Video Signal Constraints**

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<tbody>
<tr>
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<td>CRT_SYNC2SYNC</td>
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LVDS signals are 100-ohm +/- 20% differential impedence.

- CRT & TVDAC: signal single-ended impedence varies by location:
  - 51.5-ohm +/- 15% from GMCH to first termination resistor.
  - 51.5-ohm +/- 15% from first to second termination resistor.
  - 51.5-ohm +/- 15% from second termination resistor to connector.
  - 51.5-ohm +/- 15% from GMCH to first termination resistor.

LVDS_B_DATA/LVDS_B_CLK signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

NB Constraints

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.
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**Source**: Santa Rosa Platform DS, Rev 1.0 (#41112), Section 10.9.1

**Disk Interface Constraints**

**Internal Interface Constraints**

**USB 2.0 Interface Constraints**

**HD Audio Interface Constraints**
**PCI Bus Constraints**

<table>
<thead>
<tr>
<th>Controller Link (AMT) Constraints</th>
<th>Controller Link (AMT) Constraints</th>
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<tr>
<td><strong>PHYSICAL RULE SET</strong></td>
<td><strong>PHYSICAL RULE SET</strong></td>
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<tr>
<td><strong>LAYER</strong></td>
<td><strong>MINIMUM NECK WIDTH</strong></td>
</tr>
<tr>
<td><strong>MAXIMUM NECK LENGTH</strong></td>
<td><strong>DIFFPAIR PRIMARY GAP</strong></td>
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<tr>
<td><strong>SPACING RULE SET</strong></td>
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<tr>
<td><strong>LINE-TO-LINE</strong></td>
<td><strong>SPACING</strong></td>
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<tr>
<td><strong>WEIGHT</strong></td>
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<tr>
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**SB Constraints (2 of 2)**

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<tr>
<td><strong>SOURCE:</strong> Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 &amp; 10.30</td>
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**Controller Link (AMT) Constraints**

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<th>Controller Link (AMT) Constraints</th>
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**Ethernet (Yukon) Constraints**

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### Clock Signal Constraints

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### Clock Net Properties

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### SMC SMBus Net Properties

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<td>SMB_55S</td>
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**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

**Clock & SMC Constraints**

APPLE COMPUTER INC.
## FireWire Interface Constraints

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<td>Port 3</td>
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<td>Port 6</td>
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## FireWire Net Properties

### Electrical Constraints

- FW_PHY_CLK: 98M, 304M
- FW_LPS: FW_PHY_PCLK
- FW_LPS: FW_LINK_LCLK
- FW_LPS: FW_PHY_LCLK

### Physical Constraints

- FW_PHY_CLK: FW_PHY_PCLK
- FW_PHY_CLK: FW_LINK_PCLK
- FW_PHY_CLK: FW_LINK_LCLK

### Spacing Rules

- FW_PHY_CLK: FW_PHY_PCLK
- FW_PHY_CLK: FW_LINK_PCLK
- FW_PHY_CLK: FW_LINK_LCLK
### GDDR3 Frame Buffer Signal Constraints

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<thead>
<tr>
<th>SPACING RULE SET</th>
<th>LAYER</th>
<th>LINE-TO-LINE SPACING</th>
<th>WEIGHT</th>
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### GDDR3 FB A/B Net Properties

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### GDDR3 FB C/D Net Properties

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### Video Signal Constraints

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### G84M Net Properties

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### GPU (G84M) Constraints

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</tbody>
</table>
**Alternate Diffpair Width/gap through BGA Fanout Areas (95-Ohm Diff)**

**Memory Constraint Relaxations**

- Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

**Graphics Constraint Relaxations**

- Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

**SIM Card Constraints**

**PHYSICAL RULE SET**

**SPACING RULE SET**
- Layer: Line-to-line Spacing, Weight

**M76 Specific Net Properties**
- DIFFPAIR: Width, Gap
- PRIMARY GAP: Width, Gap
- DIFFPAIR NECK GAP: Width, Gap

**Net Physical Type**
- AREA_TYPE: Physical Assignment Item, Spacing Rule Item

**Table**
- Physical Assignment Item, Spacing Assignment Item

**THERM**
- Diffpair: VGA_SYNC, VGA_G_TV_C, VGA_R_TV_Y
- SENSE: ISL4, ISL10, 0.100 MM, 2.54 MM

**ANNEX A**

- Property: Apple Computer, Inc. The Possessor
- Scale: 1/8 REV.
### M75/M76 Board-Specific Spacing & Physical Constraints

#### PHYSICAL RULE SET

**LAYER**
- **MINIMUM NECK WIDTH**
- **MAXIMUM NECK LENGTH**
- **DIFFPAIR PRIMARY GAP**
- **DIFFPAIR NECK GAP**

**TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM**

**NO_TYPE, BGA MM**

- **110_OHM_DIFF ISL9, ISL10 Y**
  - 0.077 MM
  - 0.077 MM

- **90_OHM_DIFF TOP, BOTTOM Y**
  - 0.130 MM
  - 0.130 MM

- **90_OHM_DIFF ISL2, ISL11 Y**
  - 0.130 MM
  - 0.130 MM

- **85_OHM_DIFF**

- **80_OHM_DIFF ISL2, ISL11 Y**
  - 0.140 MM
  - 0.140 MM

- **70_OHM_DIFF TOP, BOTTOM Y**
  - 0.185 MM
  - 0.185 MM

- **70_OHM_DIFF ISL2, ISL11 Y**
  - 0.185 MM
  - 0.185 MM

- **70_OHM_DIFF**

- **70_OHM_DIFF**

- **70_OHM_DIFF**

- **27P4_OHM_SE TOP, BOTTOM Y**
  - 0.335 MM
  - 0.335 MM

- **45_OHM_SE Y**
  - 0.105 MM
  - STANDARD

**ON LAYER?**

- **ALLOW ROUTE**

**MINIMUM LINE WIDTH**

- **0.200 MM**
- **0.200 MM**
- **0.125 MM**
- **0.125 MM**
- **0.125 MM**
- **0.125 MM**
- **0.125 MM**
- **0.125 MM**
- **0.125 MM**
- **0.125 MM**
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- **0.125 MM**
- **0.125 MM**

**SPACING RULE SET**

**LAYER**
- **LINE-TO-LINE SPACING**
- **WEIGHT**

**TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM**

- **1.8:1_SPACING**
  - 0.18 MM

- **1.5:1_SPACING**
  - 0.15 MM

**BGA P3MM**

**BGA P1MM**

**6**

**NOTE:** 100_DIFF_BGA is for select 100-ohm differential pairs with routing difficulties through BGAs.

**Table PHYSICAL_RULE**

- **TABLE PHYSICAL_RULE_ITEM**
- **TABLE PHYSICAL_RULE_HEAD**

**Table SPACING_RULE**

- **TABLE_SPACING_RULE_ITEM**
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- **TABLE_SPACING_ASSIGNMENT_HEAD**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**

**Table BOARD_INFO**

**NOTE:** M75/M76 Rule Definitions

APPLE COMPUTER INC. 031-7941 16 504 109 109