SCHEM, MLB, MBP17
10/24/2007

1. All resistance values are in ohms, 0.1 Watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.

1 PCB CRITICAL
820-2132 PCBF, MLB, MBP17
Left Clutch Barrel Interconnect
External USB Connector
FireWire Port Power
FireWire PHY (TSB83AA22)
Yukon Power Control
Memory Active Termination
Clock Termination
SB Power & Ground
SB PCI, PCIe, DMI, USB
SB Enet, Disk, PFS, LPC
SB FCl, PCIe, SM, USB
SB Power & Ground
SB decoupling
SB Misc
Clock ECE505
Clock Termination
DDR2 SC-01HM Connector A
DDR2 SC-01HM Connector B
Memory Active Termination
Left I/O Board Connectors
Yokon Power Control
Ethernet Connector
Firewire Link (TSB83AAA22)
Firewire PHY
Firewire Ports
PATA Connector
Left Clutch Barrel Interconnect
SNC

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10 | CPU PFS | 10/24/2007
11 | CPU Power & Ground | 10/24/2007
12 | CPU Decoupling & VID | 10/24/2007
13 | extended Debug Port (XDP) | 10/24/2007
14 | NB CPU Interface | 10/24/2007
15 | NB FES / Video Interfaces | 10/24/2007
16 | NB Misc Interfaces | 10/24/2007
17 | NB DDR2 Interfaces | 10/24/2007
18 | NB Power 1 | 10/24/2007
19 | NB Power 2 | 10/24/2007
20 | NB Grounds | 10/24/2007
21 | NB Standard Decoupling | 10/24/2007
22 | NB Graphics Decoupling | 10/24/2007
23 | SB Enet, Disk, PFS, LPC | 10/24/2007
24 | SB PCIe, PCIe, SM, USB | 10/24/2007
25 | SB Power, GPD, EDC, Clink | 10/24/2007
26 | SB Power & Ground | 10/24/2007
27 | SB Decoupling | 10/24/2007
28 | SB Misc | 10/24/2007
29 | Clock ECE505 | 10/24/2007
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Schematic / PCB #’s

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### BOM Variants

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>BTM</th>
<th>REF</th>
<th>CRITICAL</th>
<th>COMMENTS</th>
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<tbody>
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<td>630-9174</td>
<td></td>
<td></td>
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<tr>
<td>630-9175</td>
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### M76 BOM Groups

<table>
<thead>
<tr>
<th>BOM GROUP</th>
<th>PART NUMBER</th>
<th>CRITICAL</th>
<th>COMMENTS</th>
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</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

### Bar Code Labels / EEE #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>EEE #</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>COMMENTS</th>
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<tbody>
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</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, MM & IO debugging.

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

NOTE: This is not the standard XDP pinout.
Tie VCC_AXG and VCC_AXG_NCTF to GND. Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND. TV_DCONSELx to GND.

Can tie the following rails to GND:
- CRT & TV-Out Disable
- CRT:
- Unused DAC outputs must remain powered, but can filter them using 75-ohm resistors. TV-Out Disable / CRT Enable: Tie TVLACK and TV_N to GND. Must power all TVDAC2 rails. VCC_TV_DAC and VCC_DAC_N can share filtering with VCC_CRT_DAC.
- CRT Disable / TV-Out Enable: Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC2 rails must be powered. All rails must be filtered except for VCC_CRT.
- CRT & TV-Out Disable: Tie TVLACK, VCC_TV_DAC and CRT_VGA to GND. Must tie the following rails to GND: CRT_VGA, CRT_DAC, VCC_CRT, VCC_DAC, and VCC_VSYNC.

Internal Graphics Disable

Warning: Instructions for CRT and CRT & TV-Out Disable above. Can also tie CRT_DAC, CRT_VGA, and TV_DAC to GND.

LBO Disable

If unused, all signals NC if LBO is not implemented. Tie VCC_LBO and VCC_LBO_N to GND. If SHD is used, VCC_LBO must remain powered with proper decoupling. Otherwise, tie VCC_LBO to GND also.

Note: SHD adds a glitch during wake-up on LVDS DATA/CIE pairs. Best recommendation is to float both signals, see note #5057636.
Current numbers from Crestline EDS, doc #21749.

- 87654321
- 87654321

550 mA (533MHz DDR)
150 mA

- 60 mA
- 60 mA
- 35 mA
- 40 mA
- 40 mA
- 40 mA
- 50 mA
- 80 mA
- 30 mA
- 10 mA
- 5 mA

- 22
- 21
- 22
- 22
- 22
- 22
- 22
- 22
- 22
- 21
- 21
- 22
- 22
- 22
- 22
- 22
- 21
- 21
- 21
- 21
- 19
- 22
- 22
- 22

S0 or S3M is acceptable
=PP1V8_S0_NB_VCCD_LVDS
=PP1V25_S0M_NB_VCCD_HPLL
PP1V5_S0_NB_VCCD_QDAC
PP1V5_S0_NB_VCCD_TVDAC
=PP1V5_S0_NB_VCCD_CRT
PP3V3_S0_NB_VCCA_TVDACA
PP3V3_S0_NB_VCCA_TVDACB
PP3V3_S0_NB_VCCA_TVDACC
PP1V25_S0M_NB_VCCA_SM_CK
PP1V25_S0M_NB_VCCA_SM
PP1V25_S0_NB_PEG_PLL
=GND_NB_VSSA_PEG_BG
=PP3V3_S0_NB_VCCA_PEG_BG
=GND_NB_VSSA_LVDS
PP1V8_S0_NB_VCCTXLVDS
PP1V25_S0M_NB_VCCA_MPLL
PP1V25_S0M_NB_VCCA_HPLL
PP1V25_S0_NB_VCCA_DPLLB
PP1V25_S0_NB_VCCA_DPLLA
=GND_NB_VSSA_DAC_BG
PP3V3_S0_NB_VCCA_DAC_BG
PP3V3_S0_NB_VCCA_CRTDAC
=PP3V3_S0_NB_VCCSYNC

VCCD_CRT
VCCA_SM5
VCCA_PEG_PLL
VCCA_HPLL
VCC_SYNC
VCCD_LVDS2
VCCD_LVDS1
VCCD_PEG_PLL
VCCD_HPLL
VCCD_QDAC
VCCD_TVDAC
VCCD_TVC_DAC2
VCCA_TVC_DAC1
VCCA_TVB_DAC2
VCCA_TVB_DAC1
VCCA_TVA_DAC1
VCCA_SM_CK4
VCCA_SM_CK3
VCCA_SM_CK2
VCCA_SM_CK1
VCCA_SM_CK11
VCCA_SM_CK10
VCCA_SM_C9
VCCA_SM_C8
VCCA_SM_C7
VCCA_SM_C6
VCCA_SM_C5
VCCA_SM_C4
VCCA_SM_C3
VCCA_SM_C2
VCCA_SM_C1
VCCA_SM1
VCCA_SM2
VCCA_SM3
VCCA_SM4
VCCA_SM5
VCCA_SM6
VCCA_SM7
VCCA_SM8
VCCA_SM9
VCCA_SM10
VCCA_SM11
VSSA_PEG_BG
VCCA_LVDS
VCCA_DPLLB
VCCA_DPLLA
VSSA_DAC_BG
VCCA_DAC_BG
VCCA_CRT_DAC1

Current numbers from Crestline EDS Addendum, doc #20127.

**NOTE:** This filter is required even if using only external graphics. VCCD_TVDAC also powers internal thermal sensors.

85 mA = PP1V5_S0_NB_TVDAC

These 2 caps should be within 6.35 mm of NB edge

CRITICAL

Vout = 1.25V (Factory Programmed)

VOLTAGE=1.25V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.4 MM

PP1V25_S0_NB_DPLL

PB1V8_S0_NB_LVDS

GMCH Graphics Core Power

CRITICAL

NO STUFF

R2260

1/16W
5%

CRITICAL

C2213

22UF
6.3V
20%

CRITICAL

R2261

1UF
402
CERM6.3V
10%

CRITICAL

C2260

20%
2.5V

CRITICAL

D2TTANT

20%

C2210

470UF
20%

L2220

CRITICAL

TANT
6.3V
1210
POLY
20%

CRITICAL

C2212

2UF
6.3V
20%

C2226

1

MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

MIN_LINE_WIDTH=0.3 MM

VOLTAGE=1.25V

MIN_NECK_WIDTH=0.2 MM

Crestline LVDS Support

NO STUFF

NB_CLK96M_DOT_P

NB_CLK96M_DOT_N

TP_LVDS_VREFH

NC_LVDS_VREFH

NC_LVDS_VREFL

NC_LVDS_VREFL

R2261

1/16W
5%

CRITICAL

C2214

0.1uF
CERM402
10V
20%

CRITICAL

C2201

220UF
0.1uF
CERM402
10V
20%

CRITICAL

C2200

100 mA

CRITICAL

C2205

0.1uF
CERM402
10V
20%

CRITICAL

C2206

0.1uF
CERM402
10V
20%

CRITICAL

C2216

0.1uF
CERM402
10V
20%

CRITICAL

C2217

0.1uF
CERM402
10V
20%

CRITICAL

C2218

0.1uF
CERM402
10V
20%

CRITICAL

C2219

0.1uF
CERM402
10V
20%

CRITICAL

C2220

0.1uF
CERM402
10V
20%

CRITICAL

C2221

0.1uF
CERM402
10V
20%

CRITICAL

C2222

0.1uF
CERM402
10V
20%

CRITICAL

C2223

0.1uF
CERM402
10V
20%

CRITICAL

C2224

0.1uF
CERM402
10V
20%

CRITICAL

C2225

0.1uF
CERM402
10V
20%

CRITICAL

C2226

0.1uF
CERM402
10V
20%

CRITICAL

C2227

0.1uF
CERM402
10V
20%

CRITICAL

C2228

0.1uF
CERM402
10V
20%

CRITICAL

C2229

0.1uF
CERM402
10V
20%

CRITICAL

C2230

0.1uF
CERM402
10V
20%
A
One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CL_L and CST resistors are close to SO-DIMM connector.
Page Notes

Signal aliases required by this page:
- ETHER_CURRENT_L (DC/DC for Yukon EC)
- ETHER_CURRENT_R (same value by pin)

Restrictions for using Yukon EC / Yukon Ultra:
- Yukon EC - Device Yukon EC kit value
- Yukon Ultra - Device Yukon Ultra kit value

- =ENET_VMAIN_AVLBL (See note by pin)

SIGNAL_MODEL=EMPTY

PLACEMENT_NOTE=Place C3730 close to southbridge.

To support Yukon EC and Ultra on the same board:
- Use YUKON_EC and YUKON_ULTRA to select which part to use.
- Use YUKON_EC to select Yukon EC part.
- Use YUKON_ULTRA to select Yukon Ultra part.

---

Ethernet (Yukon)

---

1. Place C3730 close to southbridge.
2. Use YUKON_EC and YUKON_ULTRA to select which part to use.
3. Use YUKON_EC to select Yukon EC part.
4. Use YUKON_ULTRA to select Yukon Ultra part.

---
ENET Enable Generation

```
ENET = S0[ ] || [S3 && AC && WOW_EN]
```

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST be S3 rail.

3.3V ENET FET

```
Vout = 1.2246V * (1 + Ra / Rb) (U3850 limit)
```

500 mA max output

WLAN Enable Generation

```
"WLAN" = "S0" || (S3 && AC && "WOW_EN")
```

Yukon AVDDL LDO

```
Yukon Ultra requires 1.9V on its magnetics to pass compliance tests
```

EC:    Vout = 2.510V

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST be S3 rail.

Yukon Power Control

```
Ultra: Vout = 1.912V
```

500 mA max output (U3850 limit)

Yukon Crystal

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Reviewed by: [Signature]
Date: 12/21/2006

Page Notes

- Power aliases required by this page:
- Signal aliases required by this page:
- Bom options provided by this page:
Lo: Beta Mode enable (1394b).
Hi: Data-Strobe only (1394a).

DSx Straps:
Single-port / Desktop systems are Power Class 0 ('000').
Power Class:
41 = FWPHY_DS1
41 = FWPHY_DS0

R4142
R4140
CRITICAL

Power Class:
Single-port / Desktop systems are Power Class 0 ('000').
Multi-port Portable systems are Power Class 6 ('166').
Implement 1K pull-up or pull-down on port page.

C4150 with internal pull-up provides PHY power-up reset.
FireWire PHY Config Straps

1. Place close to FireWire PHY

Termination

Signal aliases required by this page:

- =GND_CHASSIS_FW_EMI_R
- =PP3V3_FW_LATEVG
- =PPVP_FW_PORT1

Late-VG Protection Power

FireWire Ports

Port 0

Port 1

FireWire PHY Config Straps

- Configured PHY for:
  - 2-port Portable Power Class (4)
  - Port "15" Data-Stream only (1394A)
  - Port "1" Bilingual (1394B)

Back to Top
Battery Current Sense

Battery Charger Thermal Sensor

DCIn Current Sense

(Temp Sensor has address x92,x93)

Placement Note:
Place near R8308
Place sensor on bottom side near L8300 and
Place near R8307

Placement Note:
Battery Charger Thermal Sensor (Tm0P)  R:0x93,W:0x92

Current & Thermal Sensors

CHGR_CSI_R_N = P3V3_S0_PBATTISENS
CHGR_CSI_P = LIO_DCIN_ISENSE
CHGR_CSO_R_P = PP3V3_S0_TMPSNSR

(SMBUS_TMPSNSR_SCL)  (SMBUS_TMPSNSR_SDA)  TMPSNSR_A0

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Sudden Motion Sensor (SMS)

I2C addresses:
A0 low -> 0x30, 0x31
A0 high -> 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
Package Top

Desired orientation when placed on board bottom-side:
Top-through View

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SCL/SCLK
ADDRESS
MOT_ENABLE
ENABLE
VDD
X
Y
Z
FF/MOT
SDA/SDO
GND
IN
OUT
OUT
OUT
OUT
OUT

THT_OH
CRITICAL
LGA
KXPS5-2050
9
8
7

14
13
12
11
10
9
8
7

0

4
3
2
1

100K
5%
1/16W
MF-LF 402

45K
3%
1/16W
MF-LF 402

0.033UF
16V10%
X5R2

WWW.LAPTOP-SCHEMATICS.COM

www.laptop-schematics.com
DC-In Connector

Battery Connector

Inrush Limiter

NOTE: R6910 is on LIO.
System must provide 10K-70K impedance to A52 adapter for system load detection.
RReq of R6910 [on LIO], R6912, & R6913 is 36.9K.

Assuming % variance for R6910-R6915 and 3.42V:
Model case Vth: min: 12.47V, max: 13.54V

Vref = 3.42V * (R2a / (R1b + R2b))
Vth = (Vref / R2b) / (R1b + R2b)

Vref = 1.23V
Vth = 13.8V

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PLACEMENT NOTE=Place XW7320 next to C7350.

Vout = 5.0V
8A max output
(L7320 limit)

Vout = 3.0V
5.5A max output
(L7360 limit)

5V / 3.3V Power Supply

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
GATE_NODE=TRUE
SWITCH_NODE=TRUE

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable

When both are low TPS51120 VIN current drops from 100-150μA to 10-20μA.

VOLTAGE=0V

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Notice of Proprietary Property
3.3V FW PHY Supply

Vout = 1.25V * (1 + Ra / Rb)

1.95V FW PHY Supply

Vout = 3.316V

200mA max output
(Switcher limit)

Backup power in case of FW bus
VP short to keep PHY powered.
**Power Control Signals**

- **POWER-good requirement**: GPU requires rails to come up in the following order:
  1. 1.2V
  2. 1.4V
  3. 1.6V
  4. 1.8V

- **Note**: To ensure that TP535117 PGD2C does not detect while GPU is in L0 state, GPU core voltage needs to be low before 99ms SMC timer expires.

**3.425V "G3Hot" Supply**

Supply needs to guarantee 3.3V delivered to BMC Vcore genera
der.

**Table 1: Power Control Signals**

<table>
<thead>
<tr>
<th>State</th>
<th>1.2V</th>
<th>1.4V</th>
<th>1.6V</th>
<th>1.8V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sleep</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Idle (SS)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery off</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**1.5V / 1.05V PWRGD Circuit**

Reports when 1.5V S0 and 1.05V S0 are in regulation.

**Unused PGD2 Signals**

- **PP1V2_GPU needs to ramp up in the following order:**
  1. 1.2V
  2. 1.4V
  3. 1.6V
  4. 1.8V

**Note**: 0.9V/2.5V is not checked!

---

**Other S0 Rails PWRGD Circuit**

Does not include GPU rails.
As shown, Isys =~ 4.6A max

SMC_SYS_ISET

Adapter Input Current Limit

CHGR_VREF

CHGR_ACPRN

Battery Charge FETs

Battery Charge Current Limit

Energy Star LDO

Adapter Input Current Limit

Battery Charge Current Limit

Voltage follower guarantees current limit circuits are protected with sufficient current without sensing current from Vref.
PGOOD Monitor for GPU Rails

LTC2990 provides a programmable reset delay which is required to play nice with chip PGOOD circuit.

Fast wake condition is most cases. ICMC can wake up in duration of 1 sec clock (12 ms). If PGOOD is in one well and BBV is implemented, glitch filter or other PGOOD insertion time is required for PGOOD to be valid at end of 99 ms SMC timer. If PGOOD on resume well, then observed PGOOD will not change during AS sense. If observer whatever PGOOD delays are provided.

Mux Select Conditioning

GPU LVDS I/F

LVDS Data Mux Power Supply

Panel/Backlight Control Mux

NOTE: New S/W and D/W challenge since BB gfx might be powered off if using external GPU. D/W will have to determine that the output driver is not in sleep before powering on. If output driver is in sleep, then BB gfx, this could mean powering up I/O supply will be necessary before going to sleep to keep PGOOD valid.

LVDS Interface Mux

Apple Inc.
**FSB (Front-Side Bus) Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Layer</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Differential</th>
<th>Neck Width</th>
<th>Gap</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_DSTB_55S</td>
<td>L1</td>
<td>25mil</td>
<td>50mil</td>
<td>1:1</td>
<td>25mil</td>
<td>50mil</td>
<td>FSB_DSTB_L_P&lt;3:0&gt; FSB_DSTB_L_N&lt;3:0&gt;</td>
</tr>
<tr>
<td>FSB_DSTB_55S</td>
<td>L2</td>
<td>25mil</td>
<td>50mil</td>
<td>1:1</td>
<td>25mil</td>
<td>50mil</td>
<td>FSB_DSTB_L_P&lt;3:0&gt; FSB_DSTB_L_N&lt;3:0&gt;</td>
</tr>
<tr>
<td>FSB_DSTB_55S</td>
<td>L3</td>
<td>25mil</td>
<td>50mil</td>
<td>1:1</td>
<td>25mil</td>
<td>50mil</td>
<td>FSB_DSTB_L_P&lt;3:0&gt; FSB_DSTB_L_N&lt;3:0&gt;</td>
</tr>
</tbody>
</table>

All FSB signals with impedance requirements are 55-ohm single-ended.

- Worst-case spacing is 2:1 within Imple box, with 3:1 spacing to the boundary.
- Design Guide recommends FSB signals routed with 7mil spacing.
- FSB_DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

**NOTE:** Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

**All FSB signals with impedance requirements are 55-ohm single-ended.**

**DSTB**

- Complementary pairs are spaced 1:1 and routed as differential pairs.
- Impedance requirements are 55-ohm single-ended.

**NOTE:** Design Guide recommends each DSTB/signal group be routed on the same layer.

**CPU / FSB Net Properties**

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Source</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_DSTB_L_P&lt;3:0&gt;</td>
<td>L1</td>
<td>5mil</td>
<td>10mil</td>
<td>1:1</td>
</tr>
<tr>
<td>FSB_DSTB_L_N&lt;3:0&gt;</td>
<td>L1</td>
<td>5mil</td>
<td>10mil</td>
<td>1:1</td>
</tr>
</tbody>
</table>

**NOTE:** 1mil gap is for common pair, wiring in conductors with 7mil spacing without specifying a target differential impedance.

6mil recommends at least 25mil, >50mil preferred

**CPU Signal Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Layer</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_VCCSENSE</td>
<td>L1</td>
<td>25mil</td>
<td>50mil</td>
<td>1:1</td>
</tr>
<tr>
<td>CPU_VCCSENSE</td>
<td>L2</td>
<td>25mil</td>
<td>50mil</td>
<td>1:1</td>
</tr>
<tr>
<td>CPU_VCCSENSE</td>
<td>L3</td>
<td>25mil</td>
<td>50mil</td>
<td>1:1</td>
</tr>
</tbody>
</table>

**NOTE:** CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 75-ohm single-ended impedance.

**SOURCE:** Santa Rosa Platform D2, Rev D.9 (#20517), Sections 4.4 & 5.9.2.4
### DDR2 Memory Bus Constraints

| Name             | Area_Type | Net_SPACING_TYPE1 | Net_SPACING_TYPE2 | MEM_CLK | MEM_DATA | MEM_CMD | MEM_DQS | MEM_CTRL | MEM_B_DQ | MEM_B_DQS | MEM_B_WE | MEM_B_A | MEM_B_RAS | MEM_B_CAS | MEM_B_CMD | MEM_B_CNTL | MEM_B_CLK | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_B_CNTL | MEM_BCancelar
### Disk Interface Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Max.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
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<td>IDE_DRV</td>
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<tr>
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</tbody>
</table>

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

### HD Audio Interface Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Max.</th>
<th>Note</th>
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<tr>
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<tr>
<td>USB_90D</td>
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<tr>
<td>USB_90D</td>
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<td>USB_90D</td>
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</tr>
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</table>

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.13.2

### Internal Interface Constraints

<table>
<thead>
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<th>Name</th>
<th>Min.</th>
<th>Max.</th>
<th>Note</th>
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<tr>
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</tbody>
</table>

**Source:** Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

### USB 2.0 Interface Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Min.</th>
<th>Max.</th>
<th>Note</th>
</tr>
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<tbody>
<tr>
<td>USB_90D</td>
<td></td>
<td></td>
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<tr>
<td>USB_90D</td>
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<tr>
<td>USB_90D</td>
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<td>USB_90D</td>
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</tr>
</tbody>
</table>

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.17
### Clock Signal Constraints

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Min Length</th>
<th>Max Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>100_OHM_DIFF_CLK_PCIE_100D</td>
<td>20 MIL</td>
<td>25 MIL</td>
</tr>
<tr>
<td>100_OHM_DIFF_CLK_PCIE</td>
<td>20 MIL</td>
<td>25 MIL</td>
</tr>
<tr>
<td>55_OHM_SE_CLK_PCIE_100D</td>
<td>20 MIL</td>
<td>25 MIL</td>
</tr>
<tr>
<td>55_OHM_SE_CLK_PCIE</td>
<td>20 MIL</td>
<td>25 MIL</td>
</tr>
</tbody>
</table>

**Source:** Santa Rosa Platform DD, Rev 1.0 (#11112), Sections 14.1 - 14.4

### Clock Net Properties

<table>
<thead>
<tr>
<th>Action</th>
<th>Constraint</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>=100_OHM_DIFF</td>
<td>*</td>
<td>100_OHM_DIFF</td>
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<tr>
<td>=100_OHM_DIFF</td>
<td>*CLK_FSB_100D</td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td>=100_OHM_DIFF</td>
<td>*CLK_PCIE_100D</td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td>=55_OHM_SE</td>
<td>*</td>
<td>55_OHM_SE</td>
</tr>
<tr>
<td>=55_OHM_SE</td>
<td>*CLK_FSB_100D</td>
<td>55_OHM_SE</td>
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<tr>
<td>=55_OHM_SE</td>
<td>*CLK_PCIE_100D</td>
<td>55_OHM_SE</td>
</tr>
</tbody>
</table>

### SMC SMBus Net Properties

<table>
<thead>
<tr>
<th>Action</th>
<th>Constraint</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>SMB_PCIE</td>
<td>SMBUS_SMC_MGMT_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>SMB_PCIE_100D</td>
<td>SMBUS_SMC_MGMT_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
<td>SMB_PCIE</td>
<td>SMBUS_SMC_BSA_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>SMB_PCIE</td>
<td>SMBUS_SMC_0_S0_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>SMB_PCIE</td>
<td>SMBUS_SMC_B_S0_SCL</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SDA</td>
<td>SMB_PCIE</td>
<td>SMBUS_SMC_0_S0_SDA</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>SMB_PCIE</td>
<td>SMBUS_SMC_B_S0_SDA</td>
</tr>
</tbody>
</table>

**Clock & SMC Constraints**

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- **TO MAINTAIN THE DOCUMENT IN CONFIDENCE**

**Scale:** 051-7520

**Size:** 109105°

**Rev.:** 30

**Notice of Proprietary Property:**

The appearance of certain products in the corresponding libraries is for reference only. It will not be rendered, in whole or in part.
## GDDR3 Frame Buffer Signal Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Height</th>
<th>Width</th>
<th>Rise Time</th>
<th>Settling Time</th>
<th>PD</th>
<th>Vcc</th>
<th>VDD</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_50SE</td>
<td>1500</td>
<td>1000</td>
<td>500 NS</td>
<td>1000 NS</td>
<td>2</td>
<td>3.3V</td>
<td>3.3V</td>
<td>0.8V</td>
</tr>
</tbody>
</table>

**Notes:**
- PD: Power Delay
- Vcc: Supply Voltage
- VDD: Voltage Supply
- VSS: Ground Voltage

## Video Signal Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Height</th>
<th>Width</th>
<th>Rise Time</th>
<th>Settling Time</th>
<th>PD</th>
<th>Vcc</th>
<th>VDD</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMDS_100D</td>
<td>1500</td>
<td>1000</td>
<td>500 NS</td>
<td>1000 NS</td>
<td>2</td>
<td>3.3V</td>
<td>3.3V</td>
<td>0.8V</td>
</tr>
</tbody>
</table>

**Notes:**
- PD: Power Delay
- Vcc: Supply Voltage
- VDD: Voltage Supply
- VSS: Ground Voltage

## G84M Net Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Height</th>
<th>Width</th>
<th>Rise Time</th>
<th>Settling Time</th>
<th>PD</th>
<th>Vcc</th>
<th>VDD</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_50SE</td>
<td>1500</td>
<td>1000</td>
<td>500 NS</td>
<td>1000 NS</td>
<td>2</td>
<td>3.3V</td>
<td>3.3V</td>
<td>0.8V</td>
</tr>
</tbody>
</table>

**Notes:**
- PD: Power Delay
- Vcc: Supply Voltage
- VDD: Voltage Supply
- VSS: Ground Voltage

## GPU (G84M) Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Height</th>
<th>Width</th>
<th>Rise Time</th>
<th>Settling Time</th>
<th>PD</th>
<th>Vcc</th>
<th>VDD</th>
<th>VSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_50SE</td>
<td>1500</td>
<td>1000</td>
<td>500 NS</td>
<td>1000 NS</td>
<td>2</td>
<td>3.3V</td>
<td>3.3V</td>
<td>0.8V</td>
</tr>
</tbody>
</table>

**Notes:**
- PD: Power Delay
- Vcc: Supply Voltage
- VDD: Voltage Supply
- VSS: Ground Voltage
Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GNRH fanout.

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

SIM Card Constraints
### M75/M76 Board-Specific Spacing & Physical Constraints

**Table of Constraints**

<table>
<thead>
<tr>
<th>Constraint Item</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Differential Pair</th>
<th>Primary Gap</th>
<th>Differential Pair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINIMUM LINE WIDTH</td>
<td>0.125 MM</td>
<td>0.330 MM</td>
<td>1:1_DiffPair</td>
<td>0.250 MM</td>
<td>0.125 MM</td>
</tr>
<tr>
<td>ALLOW ROUTE</td>
<td></td>
<td></td>
<td>1:1_DiffPair</td>
<td>0.250 MM</td>
<td>0.125 MM</td>
</tr>
</tbody>
</table>

**Default Width/Spacing**

- Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.

**NOTE:** 100_DIFF_BGA is for select 100-ohm differential pairs with routing difficulties through BGAs.

---

### M75/M76 Rule Definitions

**Table of Definitions**

<table>
<thead>
<tr>
<th>Rule Type</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINIMUM LINE WIDTH</td>
<td>0.125 MM</td>
</tr>
<tr>
<td>ALLOW ROUTE</td>
<td>0.250 MM</td>
</tr>
</tbody>
</table>

**Scale**

- Size: 1224.0x792.0
- Drawn to Scale: None
- Drawing Number: 051-7520 B
- Date: 01/2010

---

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