

# MANTARO

## DVT

04/02/2007

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
16		49641	ENGINEERING RELEASE	04/02/07	

- ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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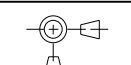
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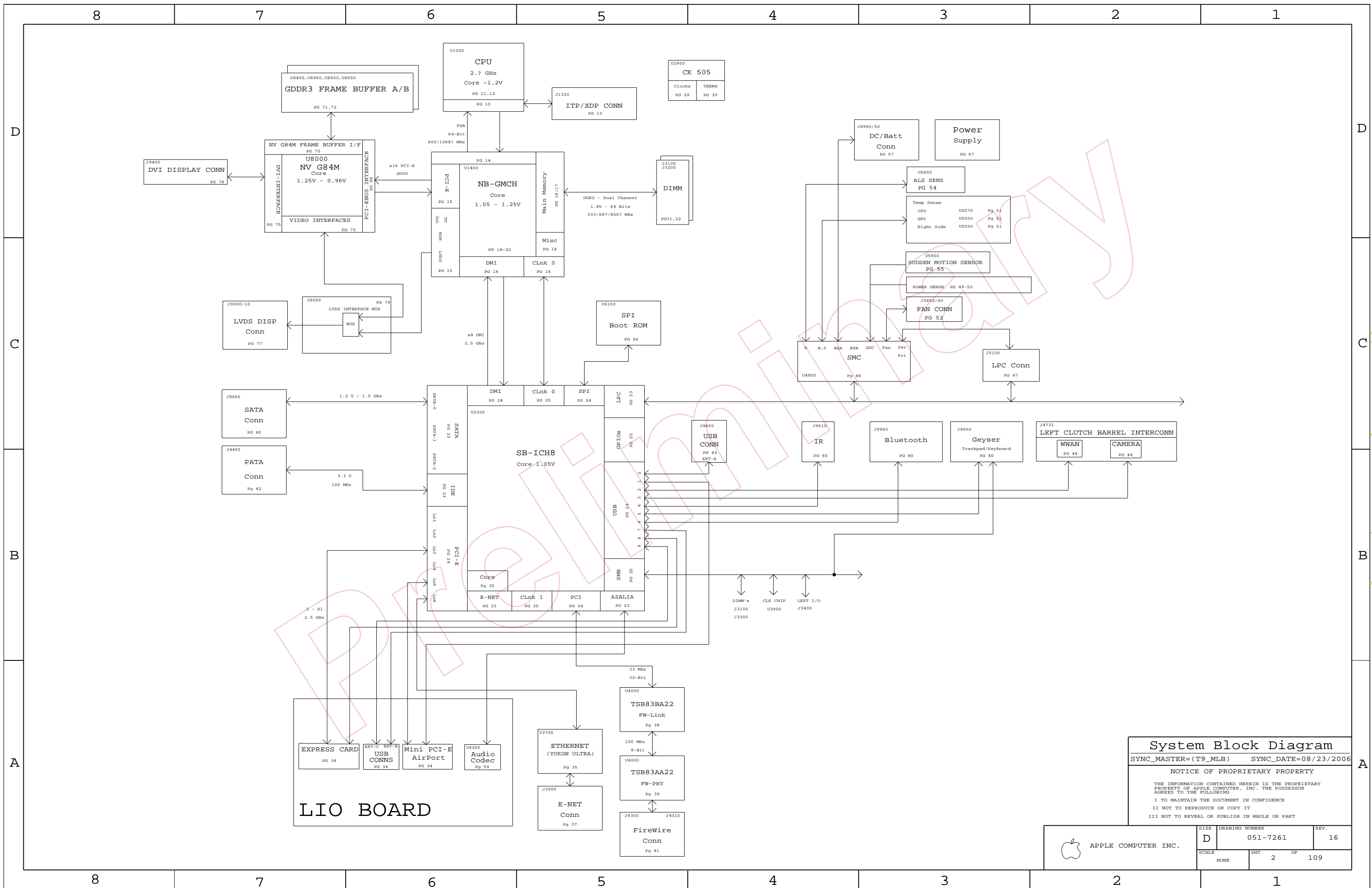
### Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7261	1	SCHEM,MLB,M76	SCH	CRITICAL	
820-2132	1	PCBF,MLB,M76	PCB	CRITICAL	

DRAWING  
TITLE=MLB  
ABBREV=DRAWING  
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DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
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X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE D	
			DRAWING NUMBER		REV.
			051-7261		16
			SHT 1		OF 109

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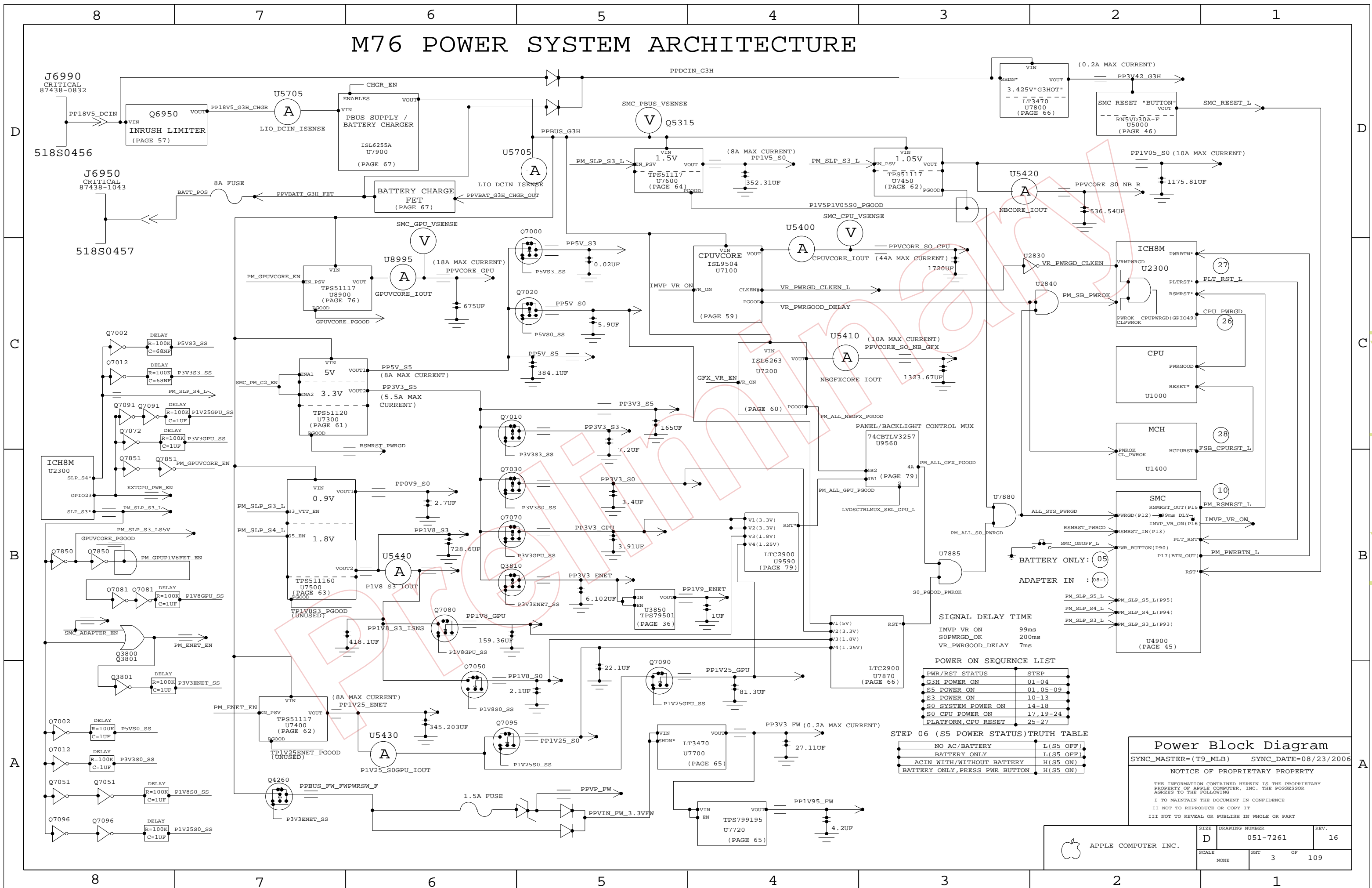
### System Block Diagram

SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/23/2006

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NONE			

# M76 POWER SYSTEM ARCHITECTURE



**SIGNAL DELAY TIME**

IMVP_VR_ON	99ms
SOPWRGD_OK	200ms
VR_PWRGOOD_DELAY	7ms

**POWER ON SEQUENCE LIST**

PWR/RST STATUS	STEP
G3H POWER ON	01-04
S5 POWER ON	01, 05-09
S3 POWER ON	10-13
S0 SYSTEM POWER ON	14-18
S0 CPU POWER ON	17, 19-24
PLATFORM, CPU RESET	25-27

**STEP 06 (S5 POWER STATUS) TRUTH TABLE**

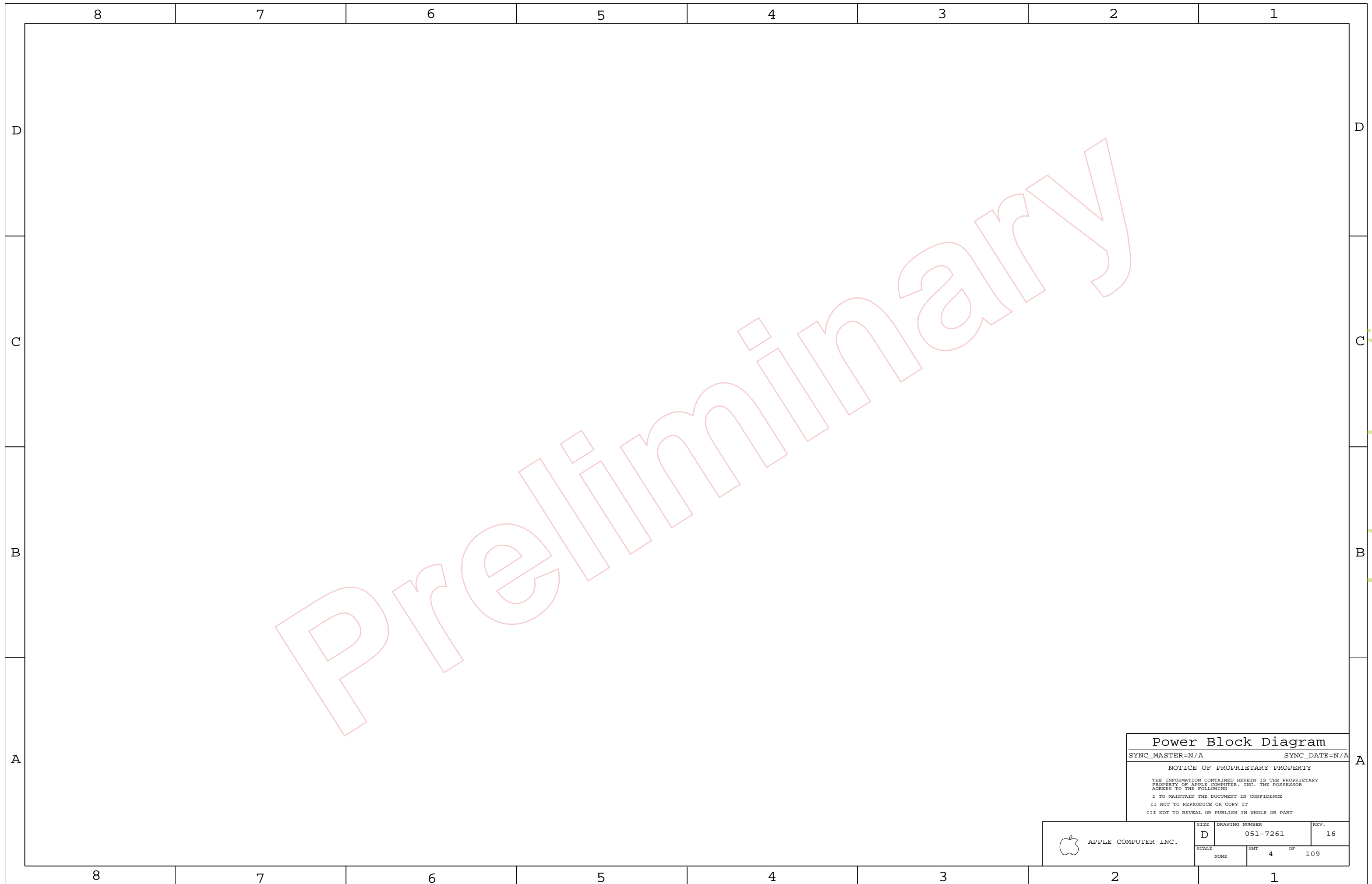
NO AC/BATTERY	BATTERY ONLY	L(S5 OFF)
ACIN WITH/WITHOUT BATTERY	BATTERY ONLY, PRESS PWR BUTTON	L(S5 ON)

**Power Block Diagram**  
 SYNC\_MASTER=(T9\_MLB) SYNC\_DATE=08/23/2006

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**Power Block Diagram**

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## BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7943	PCBA, MANTARO1, BTR, VRAM-SAM, M76	M76_COMMON, CPU_2_4GHZ, FB_256_SAMSUNG, INV_BYPASS, EEE_X6P
630-8549	PCBA, MANTARO2, BTR, VRAM-HY, M76	M76_COMMON, CPU_2_4GHZ, FB_256_HYNIX, INV_BYPASS, EEE_XWU
630-8732	PCBA, MANTARO3, CTO, VRAM-SAM, M76	M76_COMMON, CPU_2_4GHZ, FB_256_SAMSUNG, M76_CTO, EEE_XZ6
630-8733	PCBA, MANTARO4, CTO, VRAM-HY, M76	M76_COMMON, CPU_2_4GHZ, FB_256_HYNIX, M76_CTO, EEE_XZ7

## M76 BOM Groups

BOM GROUP	BOM OPTIONS
M76_COMMON	COMMON, ALTERNATE, M76_COMMON1, M76_COMMON2, M76_DEBUG, M76_PROGPARTS, ISL6257H
M76_COMMON1	EXTGPU_RST_HW, GPU_TMP401, ISL9504B, LVDS_SEL_RESUME, ONEWIRE_PU
M76_COMMON2	P1V8S3_1V825_GPUFB, SLG2AP101, SMS_MOT_DIS, YUKON_ULTRA, VGA_TERM_CONN
M76_CTO	INV_SPLIT, INV_17INCH
M76_DEBUG	SMC_DEBUG_YES, XDP, XDP_CONN, LPCPLUS
M76_PROGPARTS	BOOTROM_PROG, SMC_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM_256, VRAM_SAMSUNG, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM_256, VRAM_HYNIX, VRAM_256_HYNIX

## Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:X6P]	CRITICAL	EEE_X6P
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:XWU]	CRITICAL	EEE_XWU
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:XZ6]	CRITICAL	EEE_XZ6
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:XZ7]	CRITICAL	EEE_XZ7

## Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0388	1	IC, GPU, NV G84M, BGA	U8000	CRITICAL	
338S0426	1	IC, NB, CRESTLINE, GM, CO, QS	U1400	CRITICAL	
338S0427	1	IC, SB, ICH8M, B1, QS, BGA	U2300	CRITICAL	
353S1461	1	IC, ISL9504, SYNC REG CTRL, 2PHAS, QFN48, LF	U7100	CRITICAL	ISL9504A
353S1651	1	IC, ISL9504B, 2PH IMVP6 REG, PMON, QFN48	U7100	CRITICAL	ISL9504B

359S0127	1	IC, 68 PIN, CK505, LOW POWER CLOCK GENER	U2900	CRITICAL	SLG8LP537
359S0130	1	IC, SLG2AP101, LW PWR CLK GEN, CK505, QFN68	U2900	CRITICAL	SLG2AP101
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	
338S0274	1	IC, SMC, HS8/2116	U4900	CRITICAL	SMC_BLANK
341S2050	1	IC, SMC, DEVELOPMENT, M76	U4900	CRITICAL	SMC_PROG
335S0384	1	IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2002	1	IC, EFI ROM, DEVELOPMENT, M75	U6100	CRITICAL	BOOTROM_PROG

333S0382	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0401	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX
337S3458	1	IC, MDC, SR, E1, QS, 2.4G, 35W, 800FSB, 4M, BGA	U1000	CRITICAL	CPU_2_4GHZ

## Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
157S0011	157S0030		ALL	See alt to TR/BitTech magnetism
152S0476	152S0276		ALL	Inductor alternate
138S0603	138S0602		ALL	Make alt to Samsung 22P alternate cap
353S1681	353S1294		ALL	IC alternate to National
376S0543	376S0466		ALL	See alternate to National 88483
376S0526	376S0451		ALL	Passive alt to alternate to OPT707

BOM Configuration	
SYNC_MASTER=N/A	SYNC_DATE=N/A
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SCALE	SHT	OF	
NONE	5	109	



	8	7	6	5	4	3	2	1	
D	<p>DVT</p> <p>13.1.0:  3/05/07 -- Integrated m75/mlb pages 22,25,28,30-32,50,53-55,72,74,76,78,80-82,84-90,94,95 through:  Change 46833 by cerickso@m75_mlb_051-7225_12.5.0_tmp.Ecad on 2007/03/02 09:49:13  Changes since previous major release (12.3.0):  - LVDS Connector: Changed pin 5 of connector from NC to PP3V3_SW_LCD (in case we add extra cable for power - rdar://5024882)  - NB GFX Decoupling: Added R2260 (0.3 ohm, 0603) to bring ESR of regulator output cap in spec (rdar://5000272)  Changes since previous major release (12.2.0):  - Left Clutch IC: Updated both I-PEX connectors to new APN (part update for shell plating)  - NB GFX Core: Changed Vcore controller to ISL6263B (part consolidation effort between Apple/Intersil - rdar://5009109)  - Power Supplies: Replaced APN 152S0511 with 152S0368 (duplicate APNs for same part - rdar://5009109)  - Thermal Sensors: Updated topology of EMC1033 sensors (removed shorts, changed connector caps to 18pF)  - NB GFX Decoupling/Power Aliases: Connected VCCD_CRT of NB to GND per CRT disable guidelines  Changes since previous bom release (12.0.0):  - GPU FB: Changed cal resistors per Nvidia PUN (R8290 to 45.3 ohm and R8291 to 24.9 ohm)  - GPU FB: Changed unterminated-mode reference voltage to 40% (R8297 -&gt; 1.02k, R8432/82, R8532/82 -&gt; 2.21K)  - Power Sequencing: Removed U7885/C7885 to take GFX_PGOOD out of PWR_OK chain (rdar://4974927)  - GPU Vcore: NO STUFFED all PWRCTL related components (feature not to be supported)  - GPU Vcore: Updated voltage setpoints to 1.000/1.070/1.125V  - SB GPIOs: Sync'd page25.csa to T9_MLB to get pullup updates  - Thermal Sensors: Updated topology of EMC1033 filter caps (added C5515 next to IC, moved other caps to connectors)  3/5/07 -- Added GPU Vcore VFB resistor BOM table and GCORE_M76 BOM Option to M76_COMMON BOM group.  3/5/07 -- Removed RX3920-RX3927.  3/5/07 -- FireWire: Changed to Rev C of TI FireWire MCM (APN: 338S0435)  3/5/07 -- ODD Conn: Changed ODD power FET to FDC606P (from FDC638P) for reduced Rds(on)  3/5/07 -- Changed 1.8V supply feedback resistors R7520 to 21.5K 0.1% and R7521 15.0K 0.1%.%  13.2.0  3/07/07 -- Integrated m75/mlb pages 25,42,70 through:  Change 47192 by cerickso@m75_mlb_051-7225_12.7.0_tmp.Ecad on 2007/03/06 18:36:54  Changes since previous major release (12.6.0):  - FireWire Ports: Changed D4260 to PDS540 for higher current capacity  - SB GPIOs: Changed R2514 from pulldown to pullup to correct auto power-on issue (Linda card detect GPIO)  3/07/07 -- Q7080 PPIV8_GPU FET changed for lower Rds on from FDM6296 to RJK0301DPB  13.3.0  3/08/07 -- Removed =PPIV5_S0_NB_VCCD_CRT alias to PPIV5_S0 since VCCD_CRT is GNDed per CRT disable guidelines.  3/08/07 -- Battery charge current limit circuit changes.  3/08/07 -- Changed R9811 from 15.0K to 14.0K. This is so that M57 inverter and split inverter can use same backlight table.  3/08/07 -- Changed R9950 from 220K to NOSTUFF to improve current and voltage asymmetry ratio.  3/08/07 -- Changed BOM option on R9960 511K from NOSTUFF to INV_SPLIT to improve current and voltage asymmetry ratio.  3/08/07 -- Integrated CSA pg. 55 through:  Change 47450 by cerickso@m75_mlb_051-7225_12.8.0_tmp.Ecad on 2007/03/08 10:49:26  Changes since previous major release (12.7.0):  - Thermal Sensors: Added R5515/R5516 in case low pass filter is needed for EMC1033  3/08/07 -- Integrated CSA pg. 79 through:  Change 47440 by xyang@m75_luo_051-7226_7.9.0_tmp.Ecad on 2007/03/08 10:25:46  Changed Charger PWM limit resistor according to MARC K.'S M70 values  13.4.0  3/12/07 -- Added BOM option P1V8S3_1V825 to M76_COMMON2 BOM group.  3/12/07 -- Modified R7520 and R7521 to use symbols for 0.1% resistors.  Removed OMIT BOM option from R7521.  Changed BOM options for R7520 to choose between 1.8V or 1.825V 0.1% resistors.  14.0.0  3/14/07 -- Removed BOM option for HDCP as feature is removed.  3/14/07 -- Moved =PPIV8_GPU_P1V8GPFET from PPIV8_S3_ISNS to PPIV8_S3. This is to remove the current sense resistor from the GPU 1.8V path.  Cleaned up unused aliases.  3/14/07 -- Constraints: Constrained WWAN_SIM signals to 50 ohms  3/14/07 -- Integrated m75/mlb CSA pages 55 &amp; 78 through:  Change 48122 by cerickso@cerickso_m75.Ecad on 2007/03/14 15:27:36  - Thermal Sensors/Aliases: Changed mounting pads of Th2H sensor connector to left clutch chassis gnd  - Power Control: Corrected alias connections for 5V/3V3 S5 enable signals  14.1.0  3/14/07 -- Moved =PPIV8_S0_P1V8S0FET from PPIV8_S3_ISNS to PPIV8_S3.  14.2.0  3/15/07 -- Changes to low voltage inverter for M76 piezo.  14.5.0  3/19/07 --  Integrated m75/mlb CSA pgs. 28,30-32,50,53-55,80-82,84-88,90,94,95 through:  Change 48405 by cerickso@m75_mlb_051-7225_13.3.0_tmp.Ecad on 2007/03/16 12:18:46  Changes since previous major release (13.2.0):  - Thermal Sensors: Moved remote sensor U5500 to SMC SMBus A and S3 power rail to clear I2C addr clash  3/19/07 --Integrated t9/mlb_noME CSA pgs. 15 &amp; 38 through:  Change 48372 by wferry@wferry_projects.Ecad on 2007/03/16 09:11:01  Quick submit of T9 noME branch. Major release will follow once changes are properly documented in Radar and revision history.  Page 15: Sync from main-line (renamed LVDS_VREFx nets).  Page 38: Changed Yukon crystal load caps to 18pF per radar://4946795 (really radar://4945362).  3/19/07 -- Added OMIT BOM option to L4731 and L4741.  3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.  3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.  3/19/07 --  &lt;rdar://problem/5070179&gt; BOM update: boost circuit open causes MLB &amp; SIMM damage (see 5064997)  Deleted R7364 and made C7364 0603 size, still 0.1uF (132S0100).  Deleted R7420 and R7470 and made C7420 and C7470 0603 size, still 0.1uF (132S0100).  Deleted R7525 and made C7525 0805 size, still 0.1uF (132S0201).  Deleted R7615 and made C7615 0603 size, still 0.1uF (132S0100).  Deleted R8915 and made C8915 0603 size, still 0.1uF (132S0100).  3/19/07 -- Changes to low voltage inverter for M76 piezo.  L9950 changed from 152S0527 (15uH, 2.8A, 115mOhm) to 152S0585 (22uH, 2.8A, 129mOhm).  14.6.0  3/19/07 -- Integrated m75/mlb CSA pgs. 55 &amp; 78 through:  Change 48590 by cerickso@m75_mlb_051-7225_13.4.0_tmp.Ecad on 2007/03/19 14:26:14  Changes since previous major release (13.3.0):  - Thermal Sensors: Updated U5500 power alias to indicate device should be on S3 rail  - Power Control: Added U7858 to level shift PM_G2_EN to 3.42V to 5V  3/19/07 -- Updated SMC A SMBus information for Left I/O Board and Top-Case.  3/19/07 -- Deleted R7324 and made C7324 0603 size, still 0.1uF (132S0100).  14.7.0  3/19/07 -- Added three 0603 0 ohm resistors R4740-R4742 for EMC return current path.  3/19/07 -- Battery charge current limit circuit changes for max charge current of 4.5A.  3/19/07 -- Integrated m75/mlb CSA pgs. 22 &amp; 78 through:  Change 48660 by cerickso@m75_mlb_051-7225_13.5.0_tmp.Ecad on 2007/03/19 20:17:1 Changes since previous major release (13.4.0):  - Power Control: Tied all 4 5V/3.3V enables (EN1, EN2, EN3 and EN5) together as part of PM_G2_EN  14.8.0  3/21/07 -- Integrated m75/mlb CSA pgs. 84,85 &amp; 89 through:  Change 48885 by cerickso@m75_mlb_051-7225_14.0.0_tmp.Ecad on 2007/03/20 21:27:14  This fab release is for DVT!  Changes since previous major release (13.5.0):  - GPU Vcore: Updated setpoints for GPU Vcore based upon Nvidia Vmin (i.e. 1.05V, 1.05V, 1.05V, 1.125V)  - FB: Changed FB VREF caps to 2x0.0047uF as required by Nvidia PUN 02736-001-v07 (which requests 1x0.01uF)  3/21/07 -- &lt;rdar://problem/4838347&gt; EMC - M76 MLB changes  Change BOM option on L4764 to OMIT and added BOM table entry for 0 ohm resistor at L4764.  3/21/07 -- &lt;rdar://problem/5073301&gt; M76: Change GPU Vmin  Changed resistors for M76 Vcore setpoints (i.e. 1.05V, 1.05V, 1.05V, 1.125V, 1.25V)  Removed NOSTUFF BOM option from R8924.  Changed R8924 to 28K.  Changed R8925 to 16.9K.  Changed table text notes.  3/22/07 -- Items relating to &lt;rdar://problem/5061583&gt; Task: Current Surge When Insert Battery Without AC Plugged-In  3/22/07 -- Added D7903 for voltage ripple on ISL6257 BOOT and PHASE pins.  3/22/07 -- Added Q7970 for potential battery inrush current.  15.0.0  3/26/07 -- Removed C7930 and R7903 for space reasons.  15.2.0  3/28/07 -- Change BOM option for 1.8V regulator feedback to 1.8V GPU FET input.  3/28/07 -- Added XW7580 and R7580 for option to tie 1.8V S3 regulator feedback point to input of 1.8V GPU FET.  3/28/07 -- Integrated m75/mlb CSA pg. 87 through  Change 49919 by cerickso@cerickso_m75.Ecad on 2007/03/28 14:28:29  Changes since previous fab release (14.0.0):  - GPU Straps: Added PCI_DEVID&lt;3..0&gt; pullup straps  15.3.0  3/29/07-- Moved XW7580 to XW0980, and R7580 to R0980.  15.4.0  3/31/97 -- Changed C9950 from 22uF to 10uF for acoustic noise per Flo Kim.  3/31/97 --Added C9951 B2 case size as placeholder for new cap for acoustic noise per Flo Kim.</p>								D
C									C
B									B
A									A


16

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	6	109	

# Functional Test Points

## Fan Connectors

FUNC_TEST	Pin
TRUE =PP5V_S0_FAN_LT	8 52
TRUE FAN_LT_PWM	52
TRUE FAN_LT_TACH	52
TRUE FAN_RT_PWM	52
TRUE FAN_RT_TACH	52

## LPC+ Debug Connector

FUNC_TEST	Pin
TRUE =PP3V3_S5_LPCPLUS	8 47
TRUE =PP5V_S0_LPCPLUS	8 47
TRUE LPC_AD<0>	23 45 47
TRUE LPC_AD<1>	23 45 47
TRUE LPC_FRAME_L	23 45 47
TRUE PM_CLKRUN_L	25 45 47
TRUE BOOT_LPC_SPI_L	24 47
TRUE SMC_TMS	45 46 47
TRUE DEBUG_RESET_L	28 47
TRUE SMC_TRST_L	45 47
TRUE SMC_TDO	45 46 47
TRUE SMC_MD1	45 47
TRUE SMC_TX_L	43 45 46 47
TRUE FW_H_INIT_L	47
TRUE PCI_CLK33M_LPCPLUS	30 47 88
TRUE LPC_AD<2>	23 45 47
TRUE LPC_AD<3>	23 45 47
TRUE INT_SERIRQ	25 45 47
TRUE PM_SUS_STAT_L	25 45 46 47
TRUE SMC_TDI	45 46 47
TRUE SMC_TCK	45 46 47
TRUE SMC_RESET_L	45 46 47
TRUE SMC_NMI	45 47
TRUE SMC_RX_L	43 45 46 47
TRUE LINDACARD_GPIO	25 47

## Left ALS

FUNC_TEST	Pin
TRUE ALS_GAIN	34 45 54
TRUE LTALS_OUT	34 54
TRUE GND	

## Thermal Diode Connectors

FUNC_TEST	Pin
TRUE HSTHMSNS_D_P	51 91
TRUE HSTHMSNS_D_N	51
TRUE RSFSTHMSNS_D_P	51 91
TRUE RSFSTHMSNS_D_N	51
TRUE CEUTHMSNS_D2_P	51 91
TRUE CEUTHMSNS_D2_N	51

## System Validation TPs

FUNC_TEST	Pin
TRUE CPU_PWRGD	10 13 23 83
TRUE CPU_DPSLP_L	7 10 23 83
TRUE PM_DPRSLEPVR	16 25 59 83
TRUE CPU_DPSLP_L	7 10 23 83
TRUE PM_LAN_ENABLE	25 45
TRUE PCI_RST_L	24 28
TRUE PM_RSMRST_L	25 45
TRUE PM_SB_PWROK	9 25 28
TRUE SB_RTC_RST_L	23 28
TRUE PM_STPCPU_L	25 29 30
TRUE PM_STPPCI_L	25 29 30
TRUE VR_PWRGD_CLKEN	25 28
TRUE VR_PWRGD_DELAY	9 16 28 59
TRUE FSB_CPURST_L	10 13 14 83
TRUE FSB_CPUSLP_L	10 14 83
TRUE FSB_DPWR_L	10 14 83
TRUE NB_SB_SYNC_L	16 25
TRUE PM_BMBUSY_L	16 25

## Battery Digital Connector

FUNC_TEST	Pin
TRUE SMC_BS_ALERT_L	45 46 57
TRUE =SMBUS_BATT_SCL	48 57
TRUE =SMBUS_BATT_SDA	48 57
TRUE =BATT_POS	57 67
TRUE =BATT_NEG	57 67
TRUE GND (HOST_DETECT_L)	

## Left I/O Power Connector

FUNC_TEST	Pin	Notes
TRUE PP18V5_DCIN	57	Request for 2 test points
TRUE =PPBUS_G3H_LIO_CONN	8 57	Request for 3 test points
TRUE GND		

Request for at least 10 GND test points  
NOTE: 10 additional GND test points are called out separately in these notes.

## RTC Battery Connector

FUNC_TEST	Pin
TRUE PPVRATT_G3_RTC	28
TRUE GND	

## Current Sense Calibration

FUNC_TEST	Pin	Notes
TRUE ISENSE_CAL_EN	45 49	2 TPs per
TRUE =PP5V_S0_ISENSECAL	8 49	
TRUE =PPVCORE_S0_NBGFX_REG	8 60	
TRUE =PPVCORE_S0_CPU_REG	8 49 59	
TRUE =PPVCORE_GPU_REG	8 49 76	
TRUE GND		

6 TPs, 2 with each of above TP pairs

## Left Clutch Barrel Connector

FUNC_TEST	Pin
TRUE PP5V_S3_CAMERA_F	44
TRUE USB_CAMERA_F_N	44 91
TRUE USB_CAMERA_F_P	44 91
TRUE PP5V_S3_WWAN_F	44
TRUE USB_WWAN_F_N	44 91
TRUE USB_WWAN_F_P	44 91

## Other Func Test Points

FUNC_TEST	Pin
TRUE PM_SYSRST_L	25 28 45
TRUE SMC_ONOFF_L	45 46 80

# ICT Test Points

## CPU FSB NO\_TESTS

NO_TEST	Pin
TRUE FSB_A_L<31..3>	10 14 83
TRUE FSB_ADS_L	10 14 83
TRUE FSB_ADSTB_L<1..0>	10 14 83
TRUE FSB_BNR_L	10 14 83
TRUE FSB_BREQ0_L	10 14 83
TRUE FSB_D_L<63..0>	10 14 83
TRUE FSB_DBSY_L	10 14 83
TRUE FSB_DINV_L<3..0>	10 14 83
TRUE FSB_DRDY_L	10 14 83
TRUE FSB_DSTB_L_N<3..0>	10 14 83
TRUE FSB_DSTB_L_P<3..0>	10 14 83
TRUE FSB_HIT_L	10 14 83
TRUE FSB_HITM_L	10 14 83
TRUE FSB_LOCK_L	10 14 83
TRUE FSB_REQ_L<4..0>	10 14 83

## NB NO\_TESTS

NO_TEST	Pin
TRUE NC_NB_NC<1..16>	== TP_NB_NC<1..16> 16

## GPU NO\_TESTS

NO_TEST	Pin
TRUE LVDS_I_CLK_P	75 79 90
TRUE LVDS_I_DATA_P<0>	75 79 90
TRUE TP_GPU_MIOB_CLKIN	74
TRUE TP_GPU_MIOB_CLKOUT_P	74
TRUE TP_GPU_MIOB_CTL3	74

## Inverter Connector

FUNC_TEST	Pin
TRUE PPBUS_S0_LCDBKLT_FUSED	82
TRUE =GND_CHASSIS_INVERTER	9 82
TRUE PP5V_SW_LCDBKLT	81 82
TRUE LCDBKLT_PWM	81 82
TRUE GND	

## IR & Sleep LED Connector

FUNC_TEST	Pin
TRUE =PP5V_S3_IR	8 80
TRUE USB_IR_N	24 80 86
TRUE USB_IR_P	24 80 86
TRUE SYS_LED_ANODE	46 80
TRUE GND	

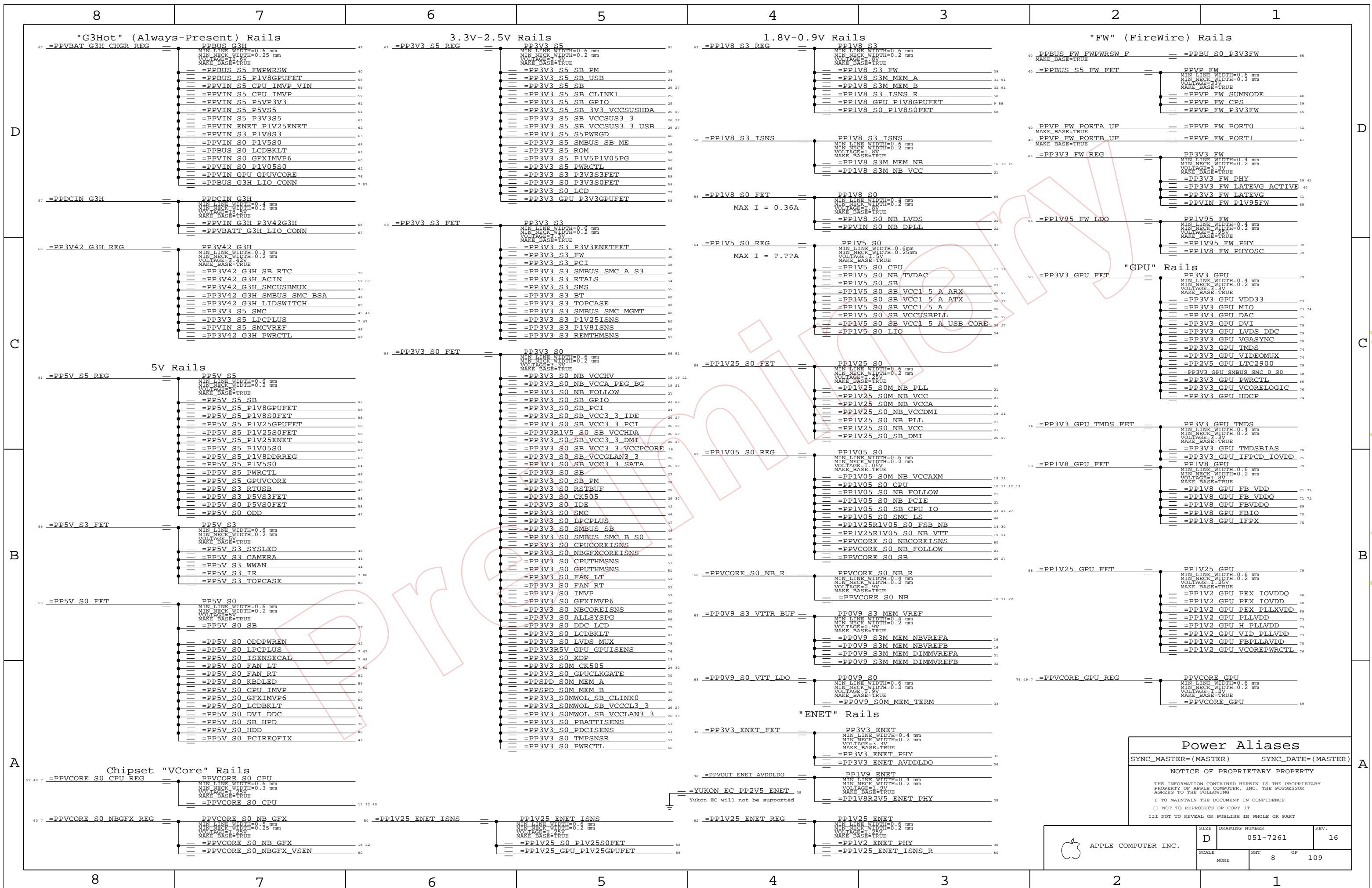
## Functional / ICT Test

SYNC\_MASTER=MASTER SYNC\_DATE=MASTER

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	D	051-7261	16
SCALE	SHT	OF	
NONE	7	109	



### Power Aliases

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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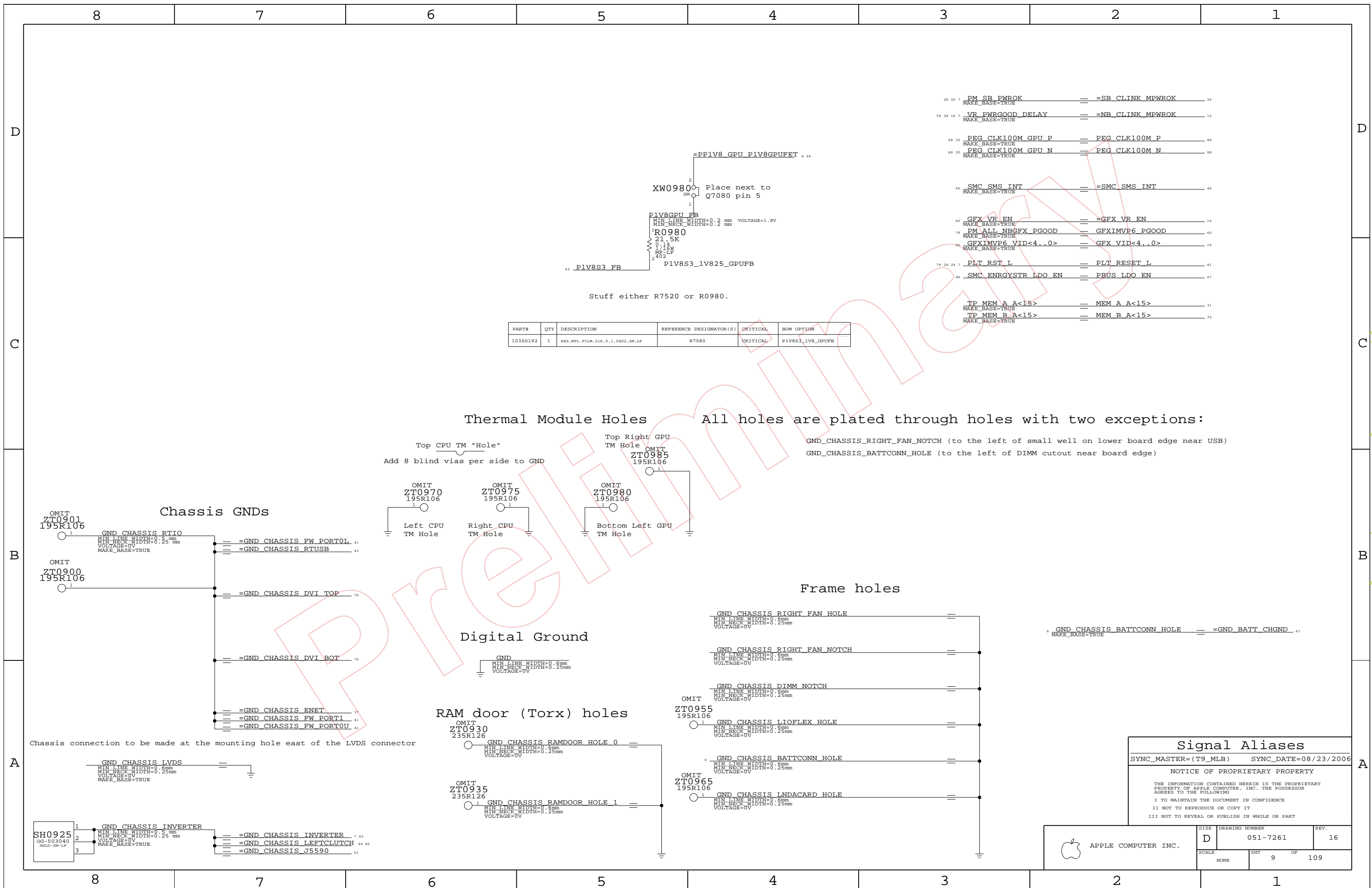
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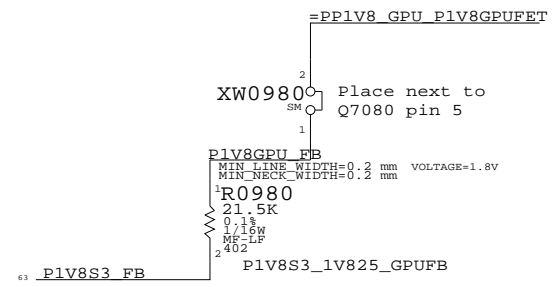
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7261	16
SCALE	SHEET	OF
NONE	8	109





28 25 7	PM_SB_PWROK	=SB_CLINK_MPWROK	25
59 28 16 7	VR_PWRGOOD_DELAY	=NB_CLINK_MPWROK	16
68 30	PEG_CLK100M_GPU_P	PEG_CLK100M_P	88
68 30	PEG_CLK100M_GPU_N	PEG_CLK100M_N	88
55	SMC_SMS_INT	=SMC_SMS_INT	45
60	GFX_VR_EN	=GFX_VR_EN	16
79	PM_ALL_NBGFX_PGOOD	GFXIMVP6_PGOOD	60
40	GFXIMVP6 VID<4..0>	GFX VID<4..0>	16
79 28 24 7	PLT_RST_L	PLT_RESET_L	81
46	SMC_ENRGYSTR_LDO_EN	PBUS_LDO_EN	67
	TP_MEM_A_A<15>	MEM_A_A<15>	31
	TP_MEM_B_A<15>	MEM_B_A<15>	32

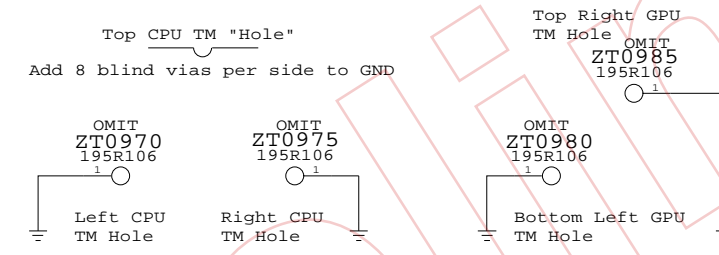


Stuff either R7520 or R0980.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10350192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7580	CRITICAL	P1V8S3_1V8_GPUPFB

### Thermal Module Holes

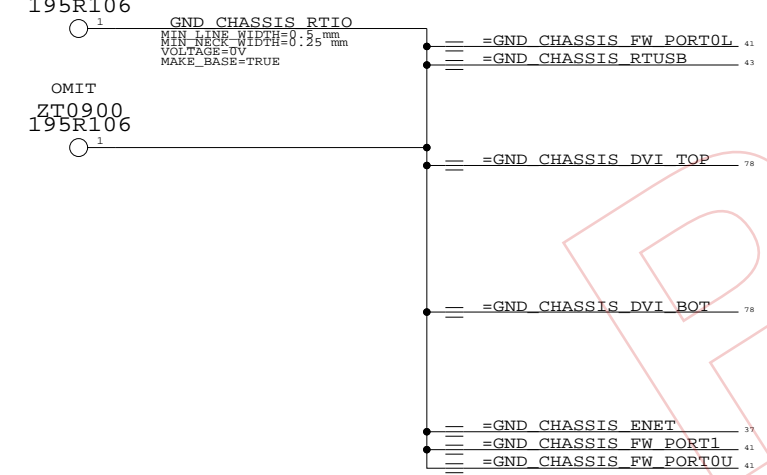
All holes are plated through holes with two exceptions:



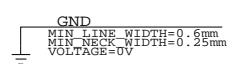
GND\_CHASSIS\_RIGHT\_FAN\_NOTCH (to the left of small well on lower board edge near USB)

GND\_CHASSIS\_BATTCONN\_HOLE (to the left of DIMM cutout near board edge)

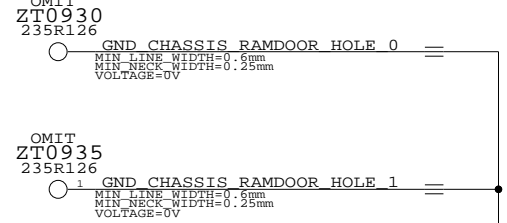
### Chassis GNDS



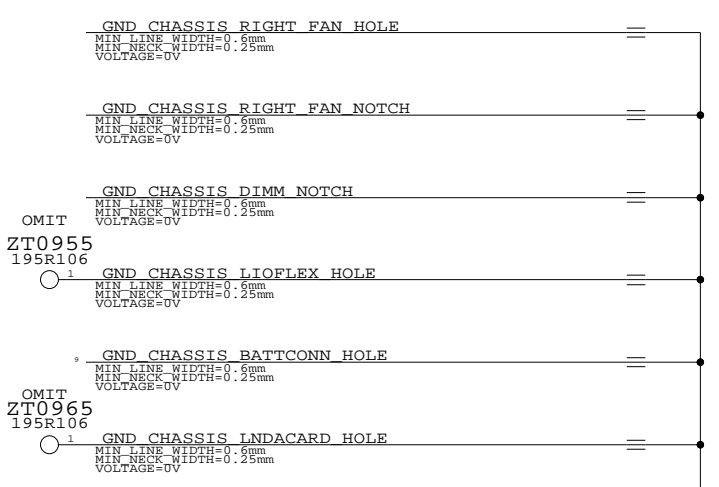
### Digital Ground



### RAM door (Torx) holes



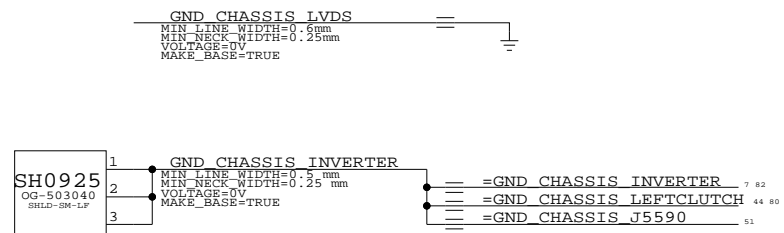
### Frame holes



GND\_CHASSIS\_BATTCONN\_HOLE =GND\_BATT\_CHGND 67

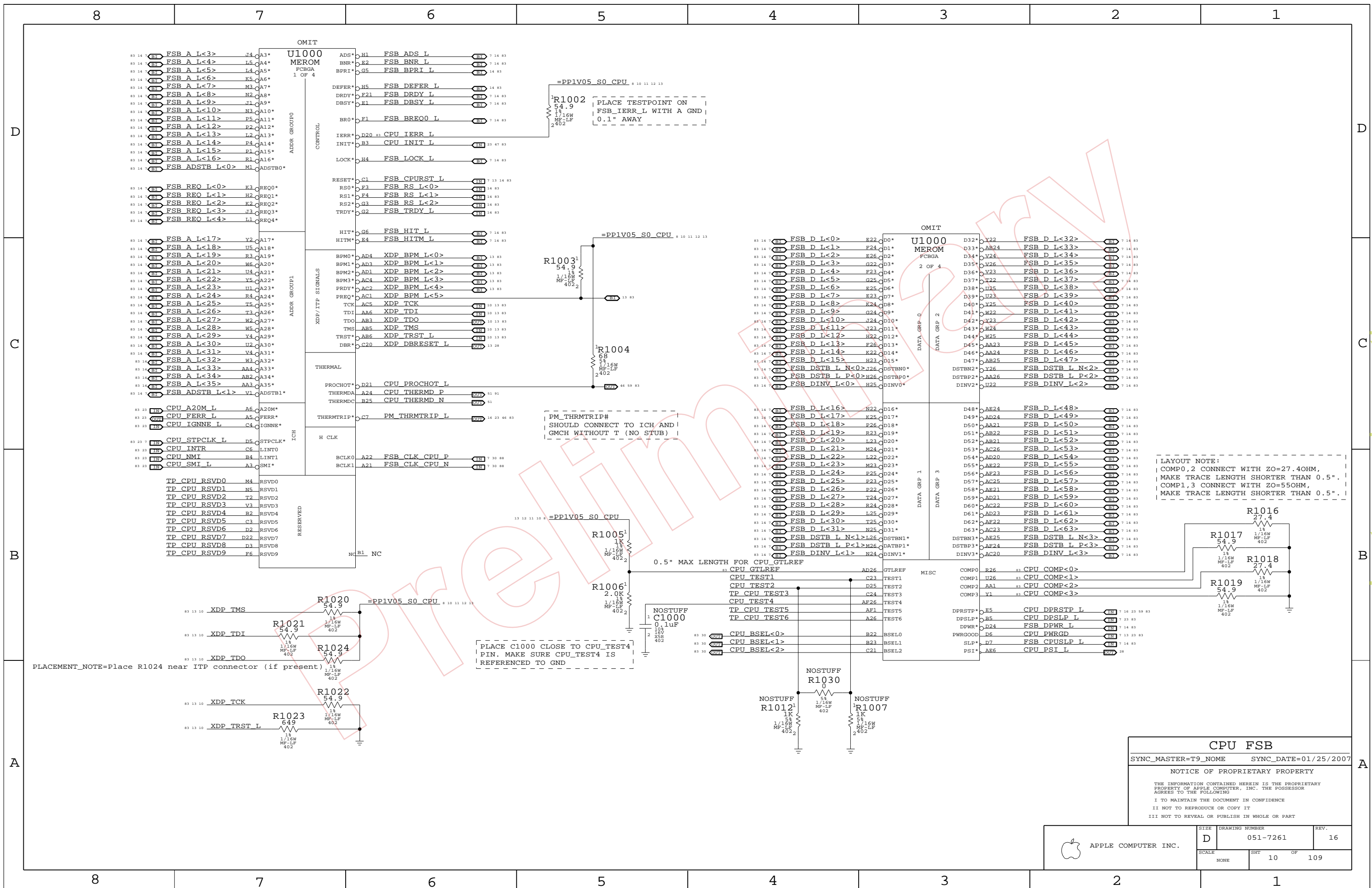
MAKE\_BASE=TRUE

Chassis connection to be made at the mounting hole east of the LVDS connector



Signal Aliases		
SYNC_MASTER=(T9_MLB)	SYNC_DATE=08/23/2006	
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NONE	9	109	



LAYOUT NOTE:  
 COMP0,2 CONNECT WITH ZO=27.4OHM,  
 MAKE TRACE LENGTH SHORTER THAN 0.5".  
 COMP1,3 CONNECT WITH ZO=55OHM,  
 MAKE TRACE LENGTH SHORTER THAN 0.5".

PLACE C1000 CLOSE TO CPU\_TEST4  
 PIN. MAKE SURE CPU\_TEST4 IS  
 REFERENCED TO GND

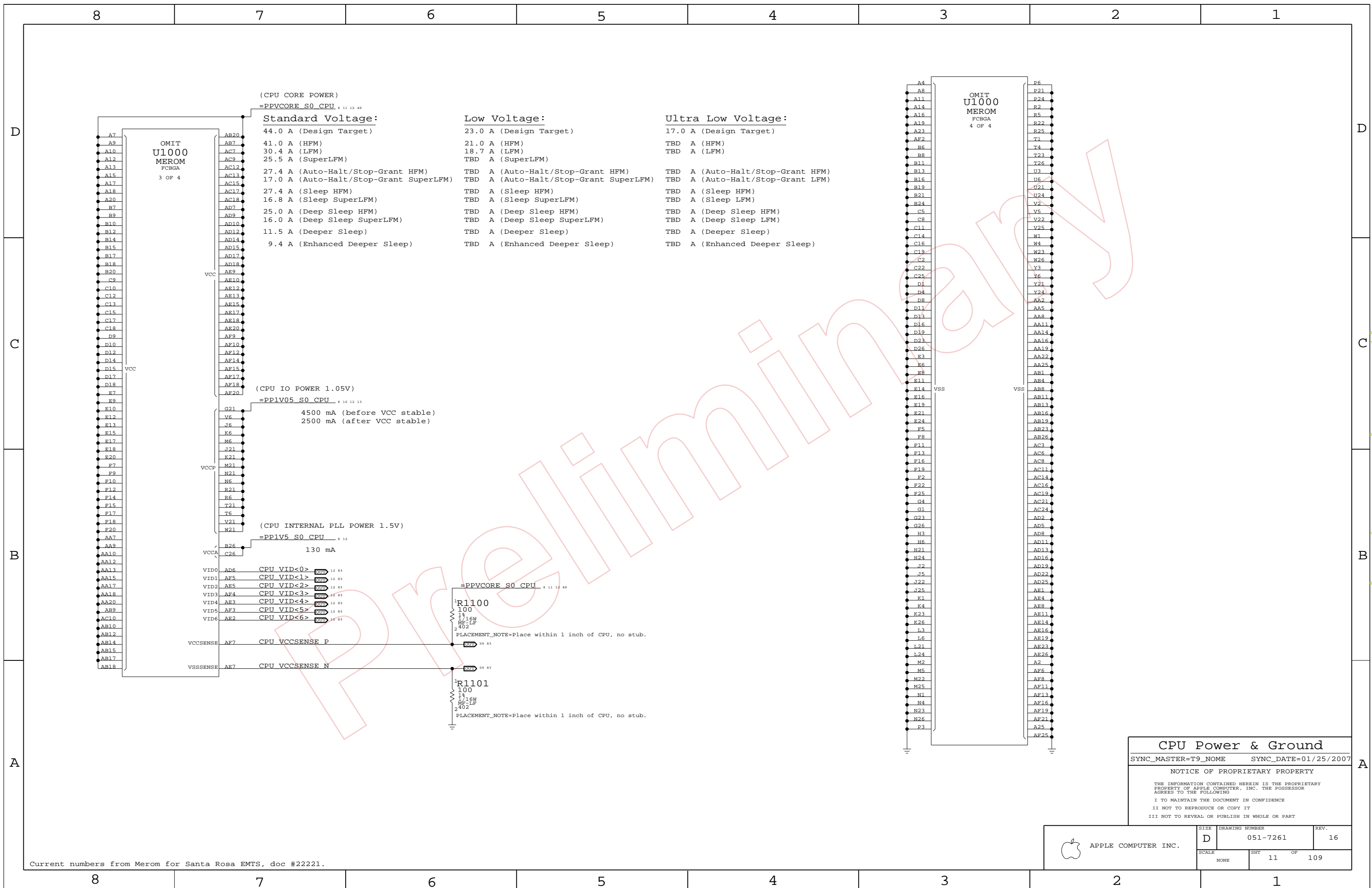
PM\_THRMTRIP#  
 SHOULD CONNECT TO ICH AND  
 GMCH WITHOUT T (NO STUB)

PLACEMENT\_NOTE=Place R1024 near ITP connector (if present)

CPU FSB		
SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	
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	SCALE: NONE	SHEET: 10	OF: 109

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(CPU CORE POWER)

=PPVCORE\_S0\_CPU # 11 12 49

**Standard Voltage:**

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

**Low Voltage:**

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

**Ultra Low Voltage:**

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

(CPU IO POWER 1.05V)

=PP1V05\_S0\_CPU # 10 12 13

- 4500 mA (before VCC stable)
- 2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5\_S0\_CPU # 12

130 mA

- VID0 AD6 CPU VID<0>
- VID1 AE5 CPU VID<1>
- VID2 AE5 CPU VID<2>
- VID3 AF4 CPU VID<3>
- VID4 AE3 CPU VID<4>
- VID5 AF3 CPU VID<5>
- VID6 AE2 CPU VID<6>

VCCSENSE AF7 CPU VCCSENSE P

VSSSENSE AE7 CPU VCCSENSE N

R1100  
100  
14  
17.16W  
MF-1EP  
2402  
PLACEMENT\_NOTE=Place within 1 inch of CPU, no stub.

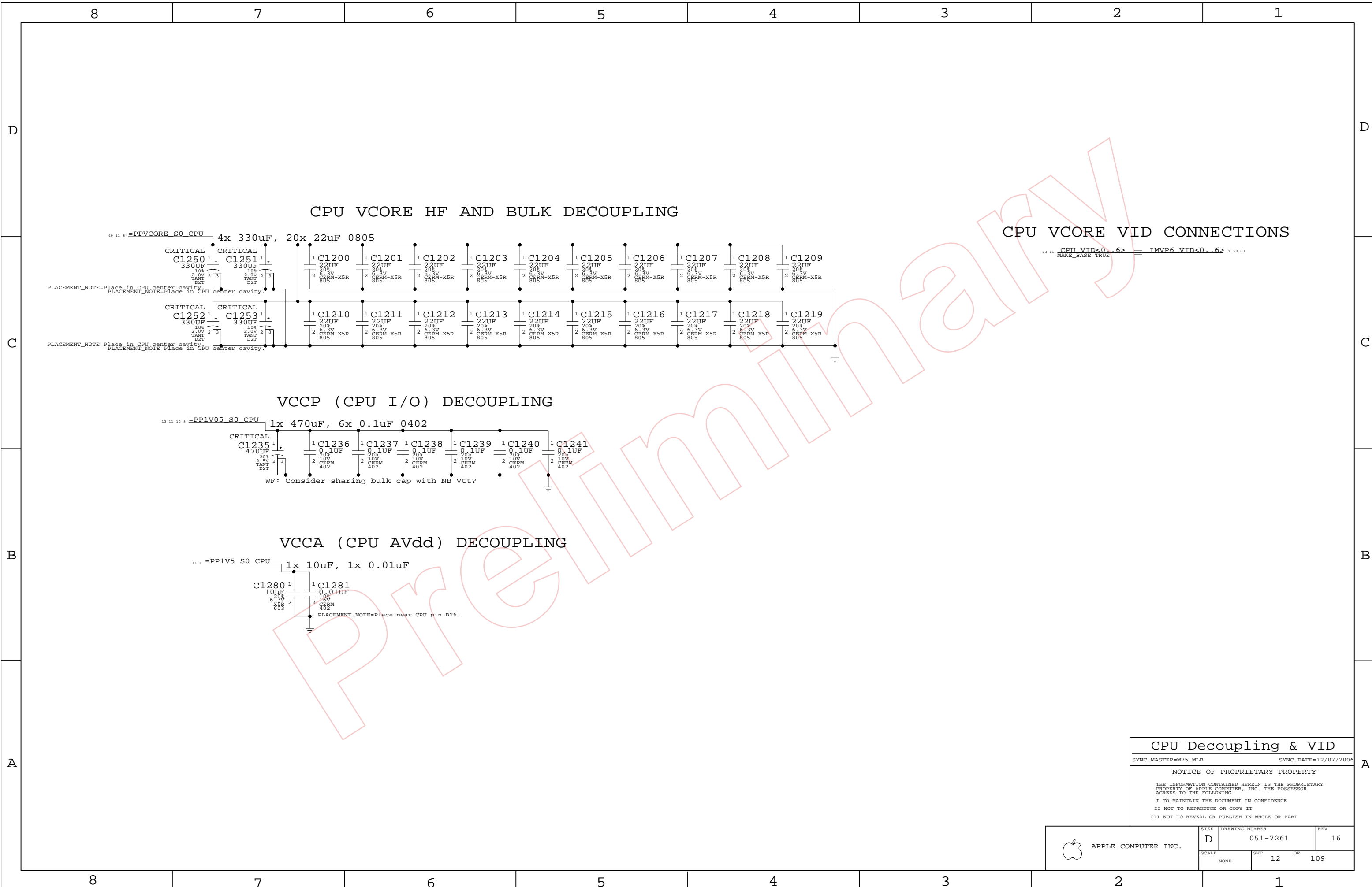
R1101  
100  
14  
17.16W  
MF-1EP  
2402  
PLACEMENT\_NOTE=Place within 1 inch of CPU, no stub.

**CPU Power & Ground**

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007

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SCALE	SHT	OF	
NONE	11	109	



CPU VCORE HF AND BULK DECOUPLING

CPU VCORE VID CONNECTIONS

VCCP (CPU I/O) DECOUPLING

VCCA (CPU AVdd) DECOUPLING

**CPU Decoupling & VID**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/07/2006  
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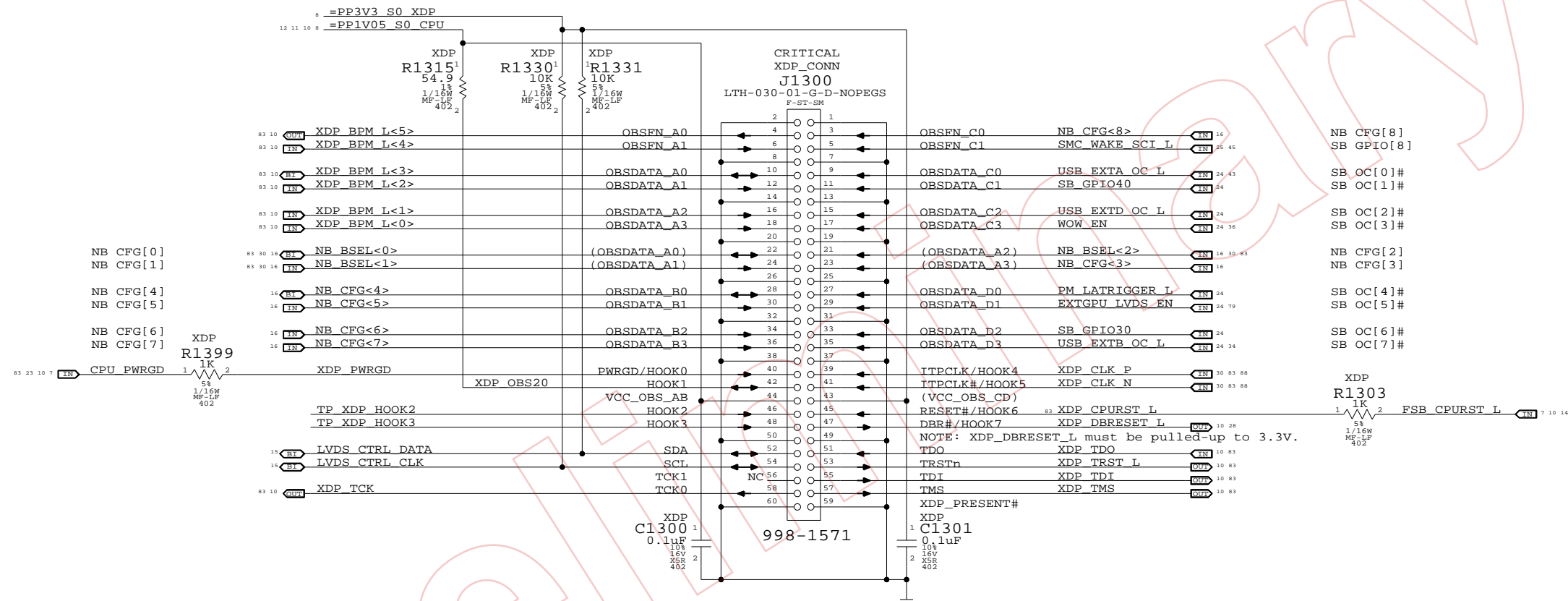
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SCALE	SHT		OF
NONE	12		109

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# Mini-XDP Connector

NOTE: This is not the standard XDP pinout.  
Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

Please avoid any obstructions  
on even-numbered side of J1300

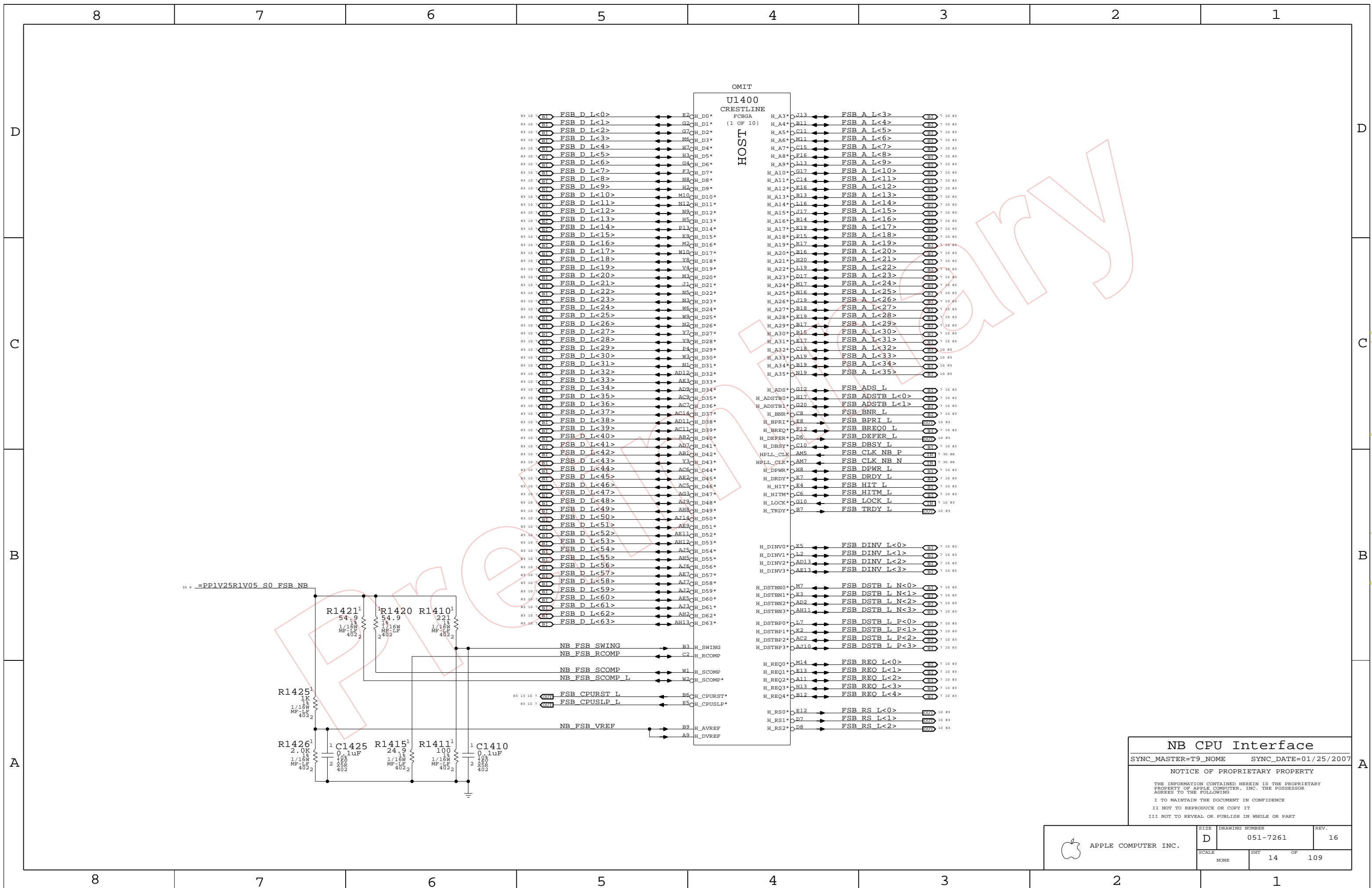
## eXtended Debug Port (XDP)

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/22/2007

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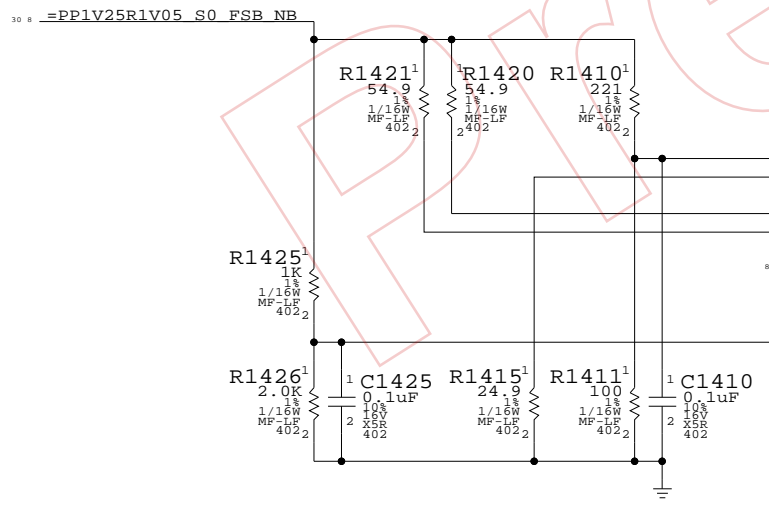
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SCALE	SHT	OF	
NONE	13	109	



OMIT  
U1400  
CRESTLINE  
FCBGA  
(1 OF 10)

Host Pin	Host Label	Processor Pin	Processor Label
H_A3*	J13	E2	FSB D L<0>
H_A4*	B11	G2	FSB D L<1>
H_A5*	C11	G7	FSB D L<2>
H_A6*	M11	M6	FSB D L<3>
H_A7*	C15	H7	FSB D L<4>
H_A8*	F16	H3	FSB D L<5>
H_A9*	L13	G4	FSB D L<6>
H_A10*	G17	F3	FSB D L<7>
H_A11*	C14	N8	FSB D L<8>
H_A12*	K16	H4	FSB D L<9>
H_A13*	B12	M10	FSB D L<10>
H_A14*	L16	N12	FSB D L<11>
H_A15*	J17	N9	FSB D L<12>
H_A16*	B14	H5	FSB D L<13>
H_A17*	K19	P13	FSB D L<14>
H_A18*	E15	K9	FSB D L<15>
H_A19*	R17	M2	FSB D L<16>
H_A20*	B16	M10	FSB D L<17>
H_A21*	H20	Y8	FSB D L<18>
H_A22*	L19	V4	FSB D L<19>
H_A23*	D17	M4	FSB D L<20>
H_A24*	M17	J1	FSB D L<21>
H_A25*	M16	N5	FSB D L<22>
H_A26*	J19	N3	FSB D L<23>
H_A27*	B18	M6	FSB D L<24>
H_A28*	E19	M9	FSB D L<25>
H_A29*	B17	N2	FSB D L<26>
H_A30*	B15	Y7	FSB D L<27>
H_A31*	E17	Y9	FSB D L<28>
H_A32*	C18	F4	FSB D L<29>
H_A33*	A19	W3	FSB D L<30>
H_A34*	B19	N1	FSB D L<31>
H_A35*	N19	AD12	FSB D L<32>
H_A35*	N19	AE3	FSB D L<33>
H_A35*	N19	AD9	FSB D L<34>
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H_A35*	N19	AC14	FSB D L<37>
H_A35*	N19	AD11	FSB D L<38>
H_A35*	N19	AC11	FSB D L<39>
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H_A35*	N19	AD7	FSB D L<41>
H_A35*	N19	AB1	FSB D L<42>
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H_A35*	N19	AC6	FSB D L<44>
H_A35*	N19	AE2	FSB D L<45>
H_A35*	N19	AC5	FSB D L<46>
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H_A35*	N19	AH8	FSB D L<49>
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H_A35*	N19	AH12	FSB D L<53>
H_A35*	N19	AW5	FSB D L<54>
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H_A35*	N19	AW6	FSB D L<56>
H_A35*	N19	AE7	FSB D L<57>
H_A35*	N19	AW7	FSB D L<58>
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H_A35*	N19	AH2	FSB D L<62>
H_A35*	N19	AH13	FSB D L<63>
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H_A35*	N19	C2	NB_FSB_RCOMP
H_A35*	N19	W1	NB_FSB_SCOMP
H_A35*	N19	W2	NB_FSB_SCOMP L
H_A35*	N19	B6	FSB_CPURST L
H_A35*	N19	E5	FSB_CPUSLP L
H_A35*	N19	B9	NB_FSB_VREF
H_A35*	N19	A9	NB_FSB_VREF
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H_A35*	N19	H_A26*	FSB A L<26>
H_A35*	N19	H_A27*	FSB A L<27>
H_A35*	N19	H_A28*	FSB A L<28>
H_A35*	N19	H_A29*	FSB A L<29>
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H_A35*	N19	H_A33*	FSB A L<33>
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H_A35*	N19	H_ADSTB0*	FSB ADSTB L<0>
H_A35*	N19	H_ADSTB1*	FSB ADSTB L<1>
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H_A35*	N19	H_BPRI*	FSB BPRI L
H_A35*	N19	H_BREQ*	FSB BREQ L
H_A35*	N19	H_DEFER*	FSB DEFER L
H_A35*	N19	H_DBSY*	FSB DBSY L
H_A35*	N19	HPLL_CLK*	FSB CLK NB P
H_A35*	N19	HPLL_CLK*	FSB CLK NB N
H_A35*	N19	H_DPWR*	FSB DPWR L
H_A35*	N19	H_DRDY*	FSB DRDY L
H_A35*	N19	H_HIT*	FSB HIT L
H_A35*	N19	H_HITM*	FSB HITM L
H_A35*	N19	H_LOCK*	FSB LOCK L
H_A35*	N19	H_TRDY*	FSB TRDY L
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H_A35*	N19	H_DINV3*	FSB DINV L<3>
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H_A35*	N19	H_DSTBP1*	FSB DSTB L P<1>
H_A35*	N19	H_DSTBP2*	FSB DSTB L P<2>
H_A35*	N19	H_DSTBP3*	FSB DSTB L P<3>
H_A35*	N19	H_REQ0*	FSB REO L<0>
H_A35*	N19	H_REQ1*	FSB REO L<1>
H_A35*	N19	H_REQ2*	FSB REO L<2>
H_A35*	N19	H_REQ3*	FSB REO L<3>
H_A35*	N19	H_REQ4*	FSB REO L<4>
H_A35*	N19	H_RS0*	FSB RS L<0>
H_A35*	N19	H_RS1*	FSB RS L<1>
H_A35*	N19	H_RS2*	FSB RS L<2>



**NB CPU Interface**  
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LVDS Disable

Can leave all signals NC if LVDS is not implemented. Tie VCC\_TX\_LVDS and VCCA\_LVDS to GND.

If SDVO is used, VCCD\_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD\_LVDS to GND also.

Note: SR DG says to tie LVDS\_VREFH/L to GND. This causes a glitch during wake-up on LVDS DATA/CLK pairs. New recommendation is to float both signals, see Radar #5067636.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx\_DAC and TVx\_RTN to GND. Must power all TVDAC rails. VCCA\_TVx\_DAC and VCCA\_DAC\_BG can share filtering with VCCA\_CRT\_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA\_CRT.

CRT & TV-Out Disable

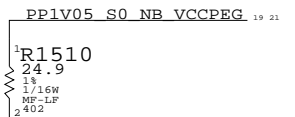
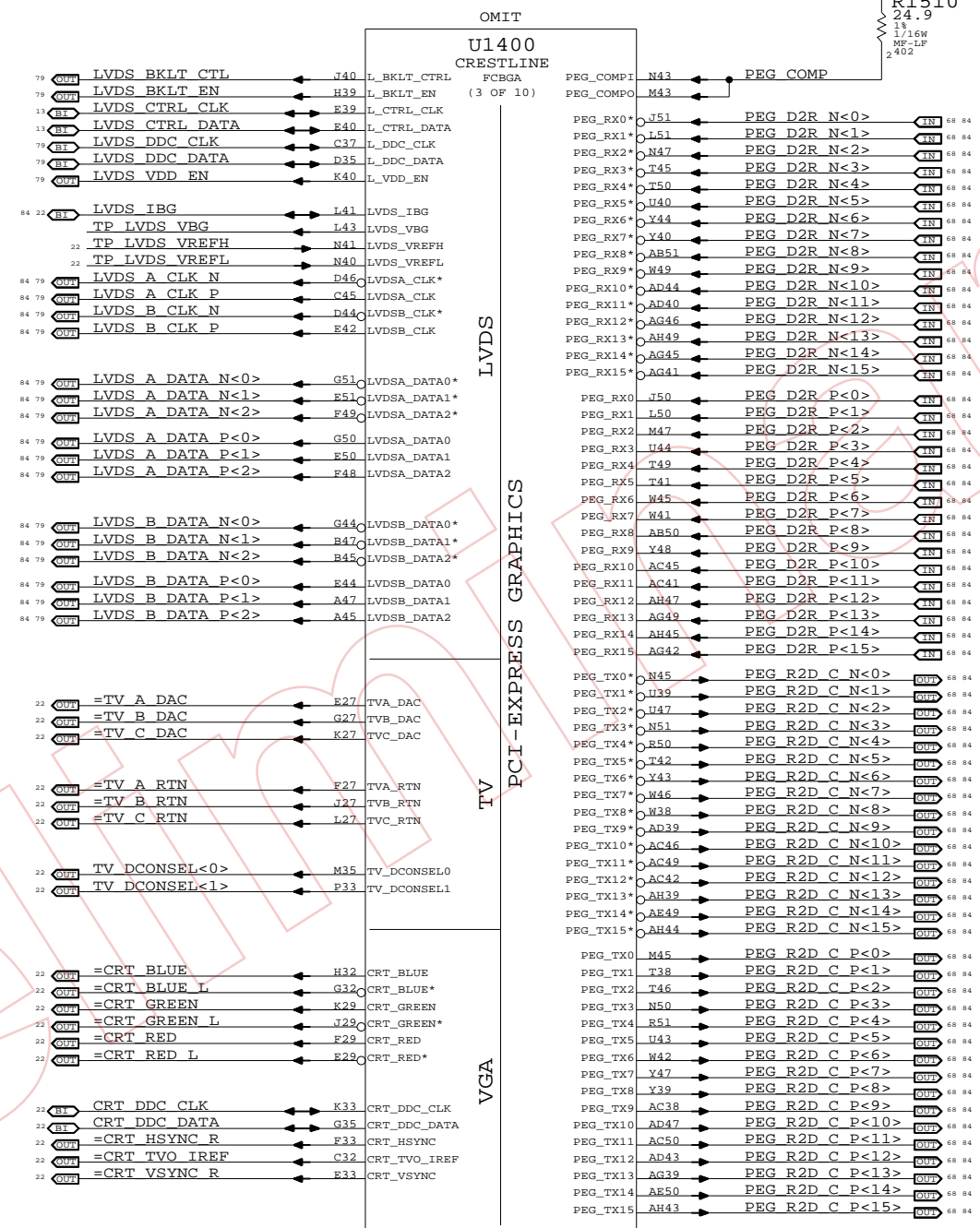
Tie TVx\_DAC, TVx\_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT\_TVO\_IREF to GND. Can tie the following rails to GND: VCCA\_CRT\_DAC, VCCA\_DAC\_BG, VCCA\_TVx\_DAC, VCCD\_CRT, VCCD\_QDAC and VCC\_SYNC.

NOTE: Must keep VDDC\_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT\_DDC\_\*, L\_CTRL\_\*, L\_DDC\_\*, SDVO\_CTRL\_\* and TV\_DCONSELx to GND.

Tie DPLL\_REF\_CLK and DPLL\_REF\_SSCLK to GND. Tie DPLL\_REF\_CLK\* and DPLL\_REF\_SSCLK\* to VCC (VCore). Tie VCCA\_DPLLA and VCCA\_DPLLB to VCC (VCore). Tie VCC\_AXG and VCC\_AXG\_NCTF to GND. Leave GFX\_VID<3..0> and GFX\_VR\_EN as NC.



SDVO Alternate Function

SDVO\_TVCLKIN#
SDVO\_INT#
SDVO\_FLDSTALL#

SDVO\_TVCLKIN
SDVO\_INT
SDVO\_FLDSTALL

SDVOB\_RED#
SDVOB\_GREEN#
SDVOB\_BLUE#
SDVOB\_CLKN
SDVOC\_RED#
SDVOC\_GREEN#
SDVOC\_BLUE#
SDVOC\_CLKN

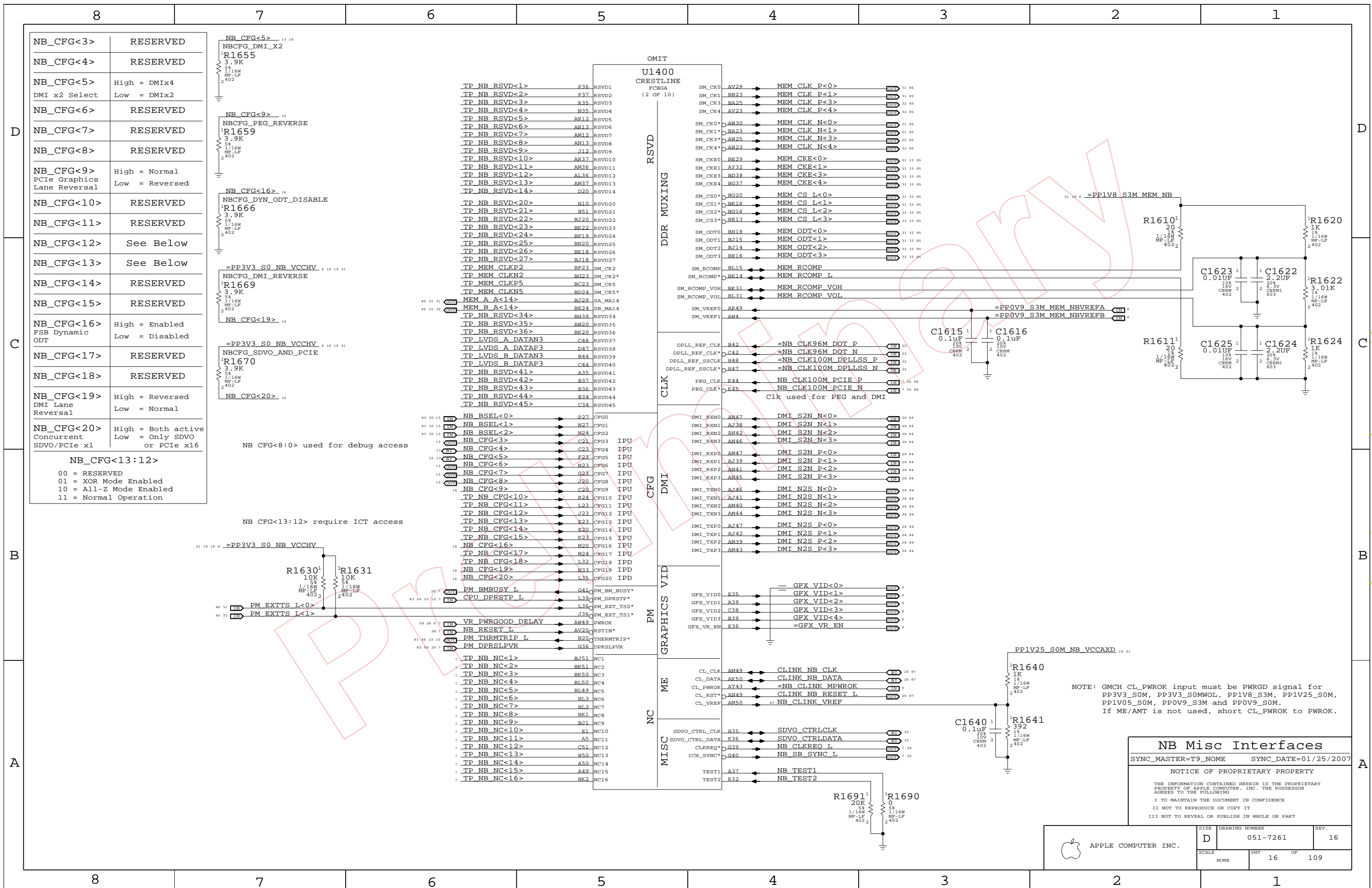
SDVOB\_RED
SDVOB\_GREEN
SDVOB\_BLUE
SDVOB\_CLKP
SDVOC\_RED
SDVOC\_GREEN
SDVOC\_BLUE
SDVOC\_CLKP

NB PEG / Video Interfaces
SYNC\_MASTER=T9\_NOME SYNC\_DATE=03/19/2007

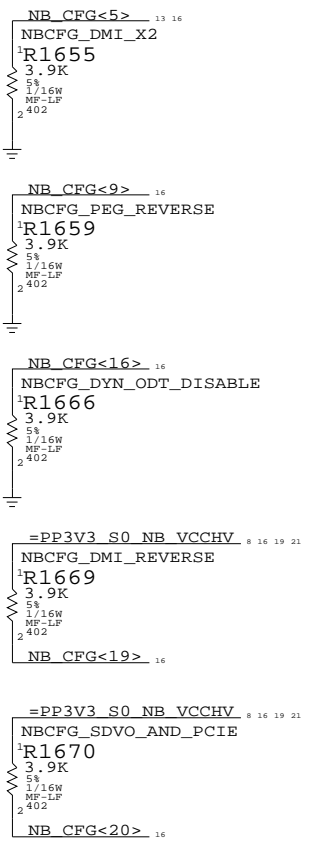
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Table with columns for Apple Computer Inc., Drawing Number (051-7261), Scale (None), Sheet (15 of 109), and Revision (16).



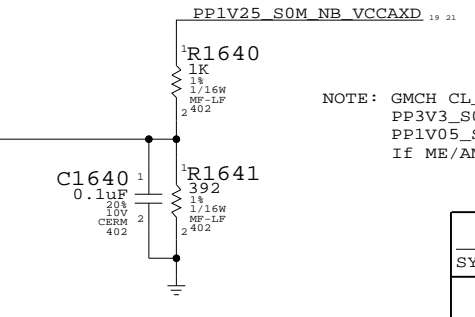
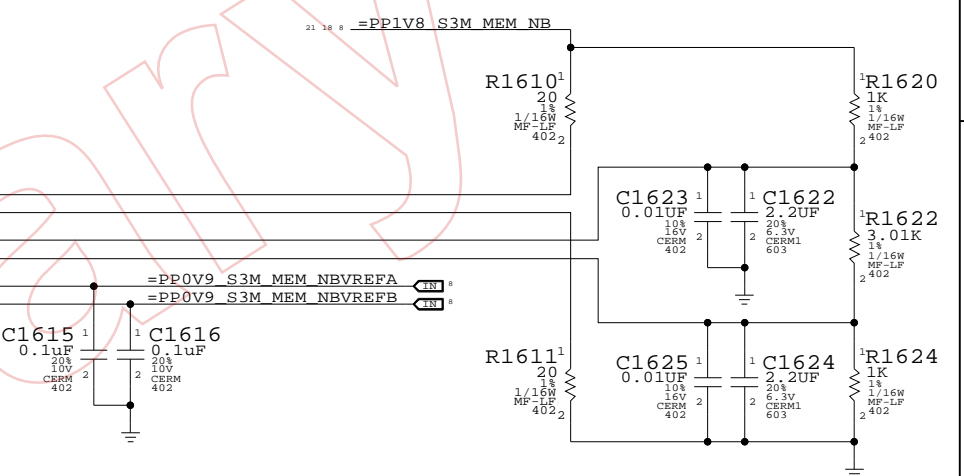
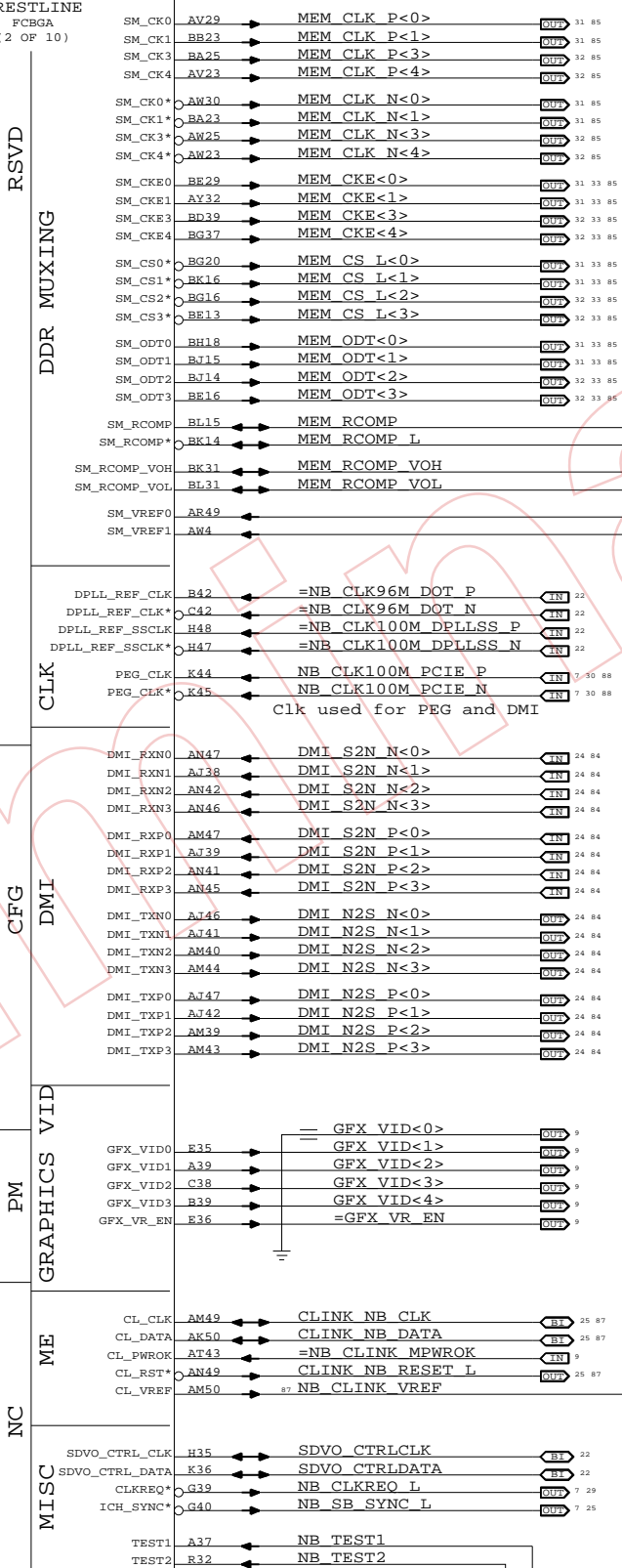
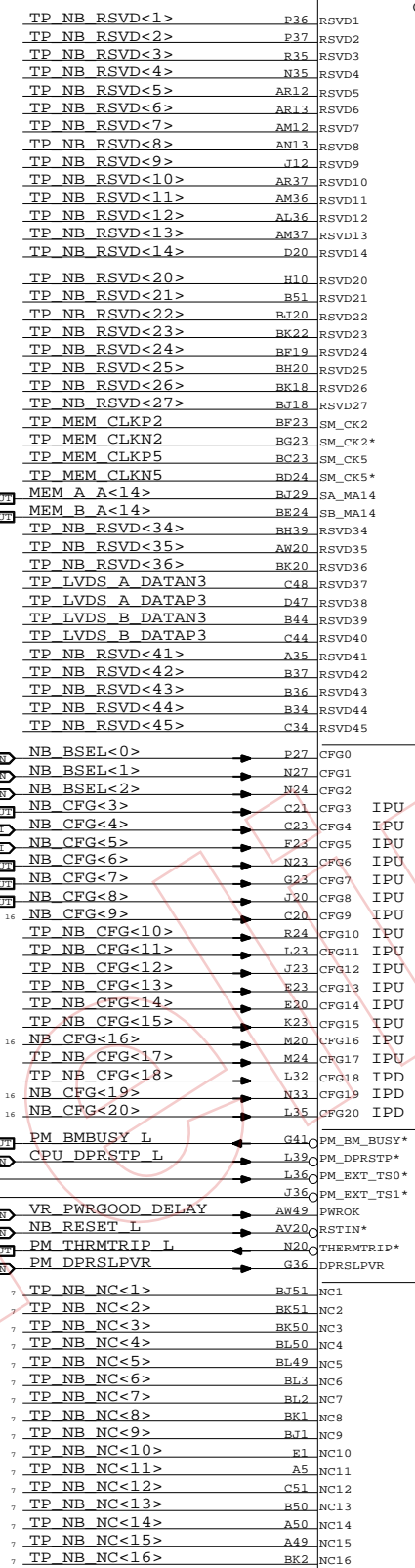
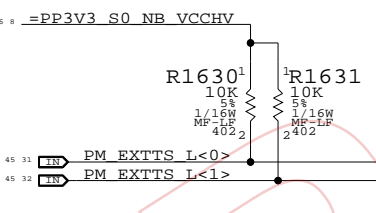


NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5>	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9>	High = Normal PCIe Graphics Lane Reversal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16>	High = Enabled FSB Dynamic ODT Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19>	High = Reversed DMI Lane Reversal Low = Normal
NB_CFG<20>	High = Both active Concurrent Low = Only SDVO SDVO/PCIe x1 or PCIe x16



NB\_CFG<8:0> used for debug access

NB\_CFG<13:12> require ICT access



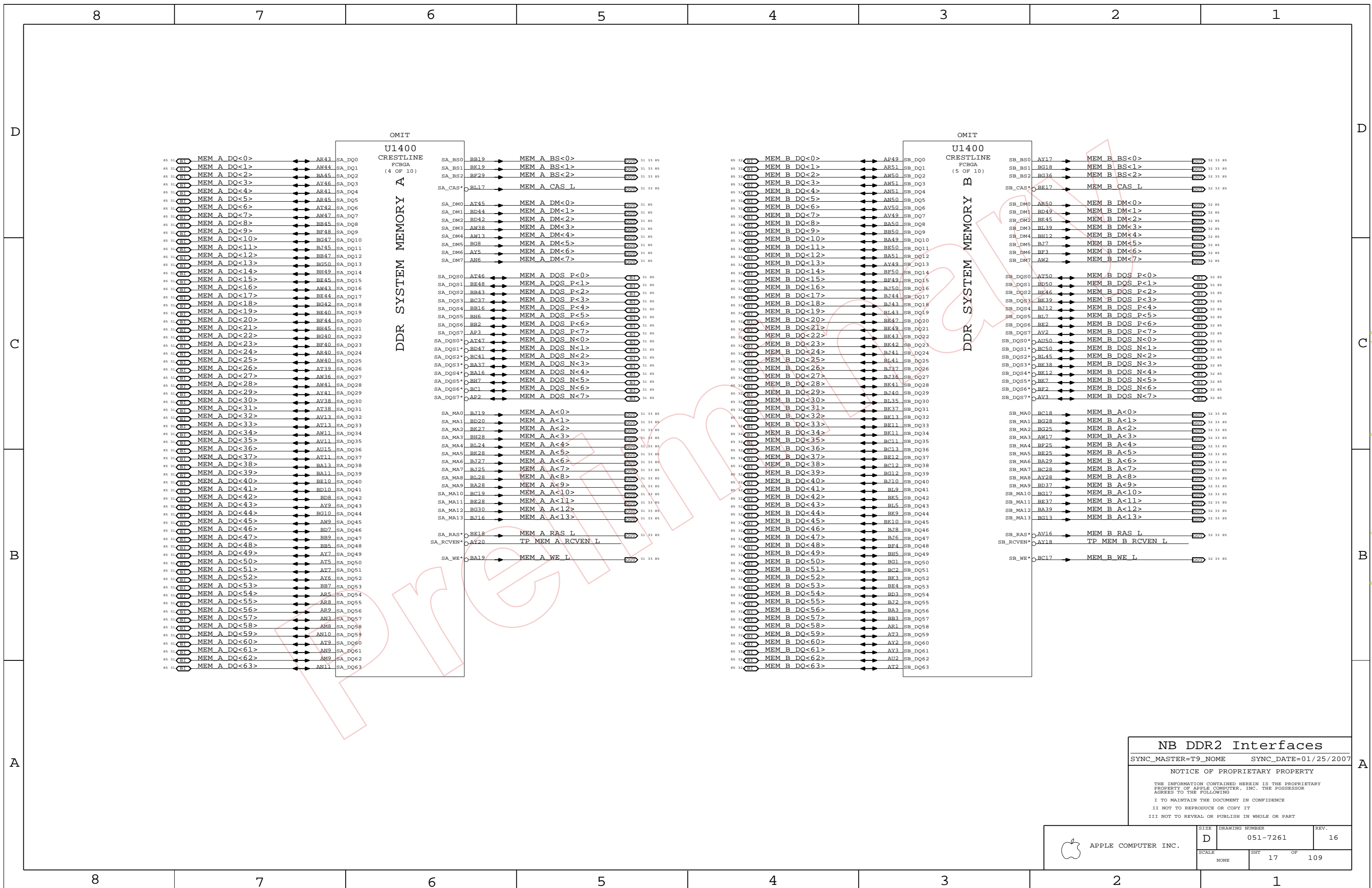
NOTE: GMCH CL\_PWROK input must be PWRGD signal for PP3V3\_S0M, PP3V3\_S0MWOL, PP1V8\_S3M, PP1V25\_S0M, PP1V05\_S0M, PP0V9\_S3M and PP0V9\_S0M. If ME/AMT is not used, short CL\_PWROK to PWROK.

NB Misc Interfaces		
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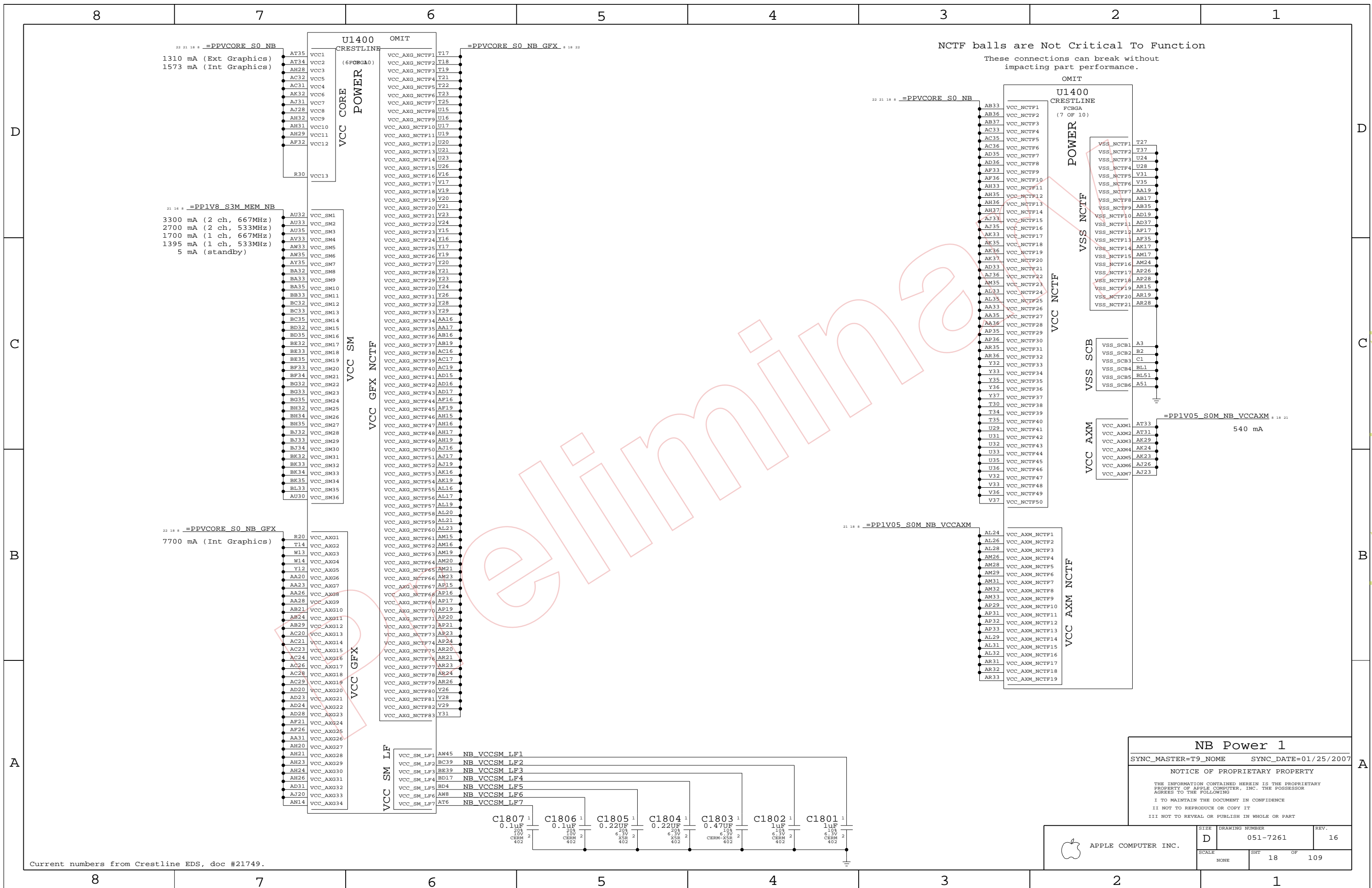
OMIT  
U1400  
CRESTLINE  
FCBGA  
(4 OF 10)  
DDR SYSTEM MEMORY A

OMIT  
U1400  
CRESTLINE  
FCBGA  
(5 OF 10)  
DDR SYSTEM MEMORY B

**NB DDR2 Interfaces**  
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NCTF balls are Not Critical To Function  
 These connections can break without impacting part performance.

22 21 18 # =PPV CORE S0 NB  
 1310 mA (Ext Graphics)  
 1573 mA (Int Graphics)

21 16 # =PPV L8 S3M MEM NB  
 3300 mA (2 ch, 667MHz)  
 2700 mA (2 ch, 533MHz)  
 1700 mA (1 ch, 667MHz)  
 1395 mA (1 ch, 533MHz)  
 5 mA (standby)

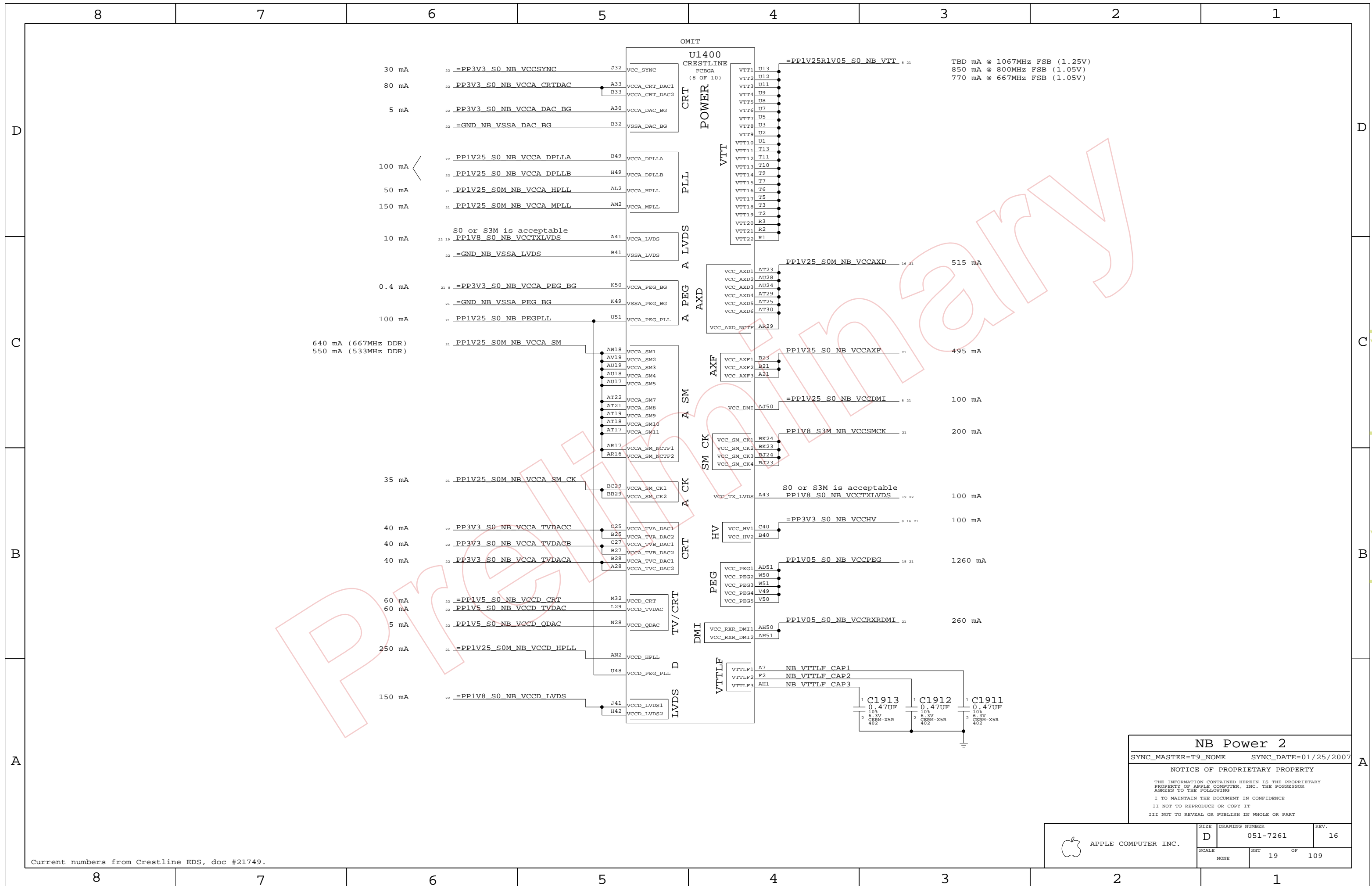
22 18 # =PPV CORE S0 NB GFX  
 7700 mA (Int Graphics)

**NB Power 1**  
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NONE	18	109	

Current numbers from Crestline EDS, doc #21749.

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TBD mA @ 1067MHz FSB (1.25V)  
 850 mA @ 800MHz FSB (1.05V)  
 770 mA @ 667MHz FSB (1.05V)

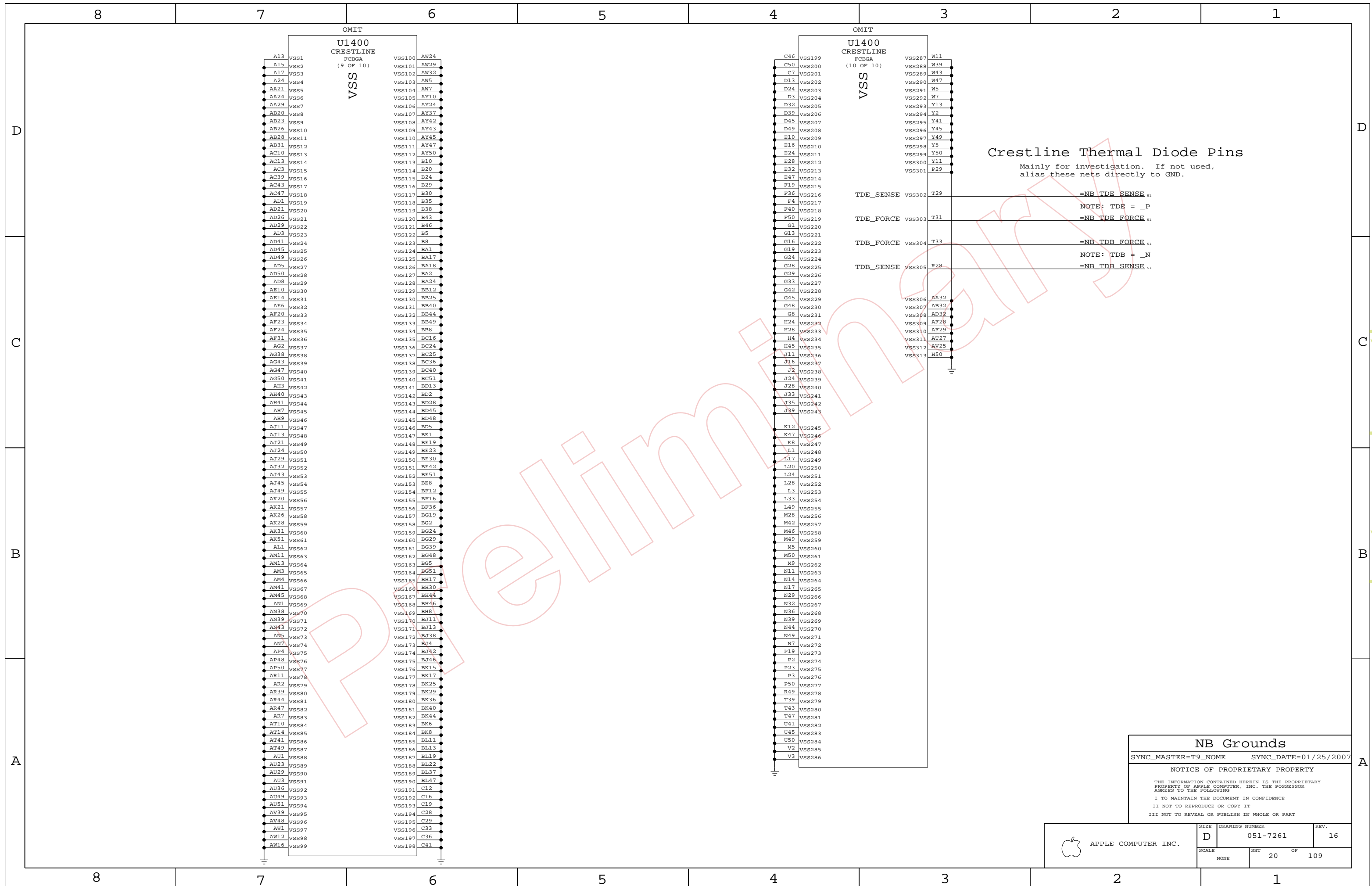
640 mA (667MHz DDR)  
 550 mA (533MHz DDR)

**NB Power 2**  
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SCALE	SHT		OF
NONE	19		109

Current numbers from Crestline EDS, doc #21749.

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**Crestline Thermal Diode Pins**  
 Mainly for investigation. If not used, alias these nets directly to GND.

**NB Grounds**  
 SYNC\_MASTER=T9\_NAME SYNC\_DATE=01/25/2007

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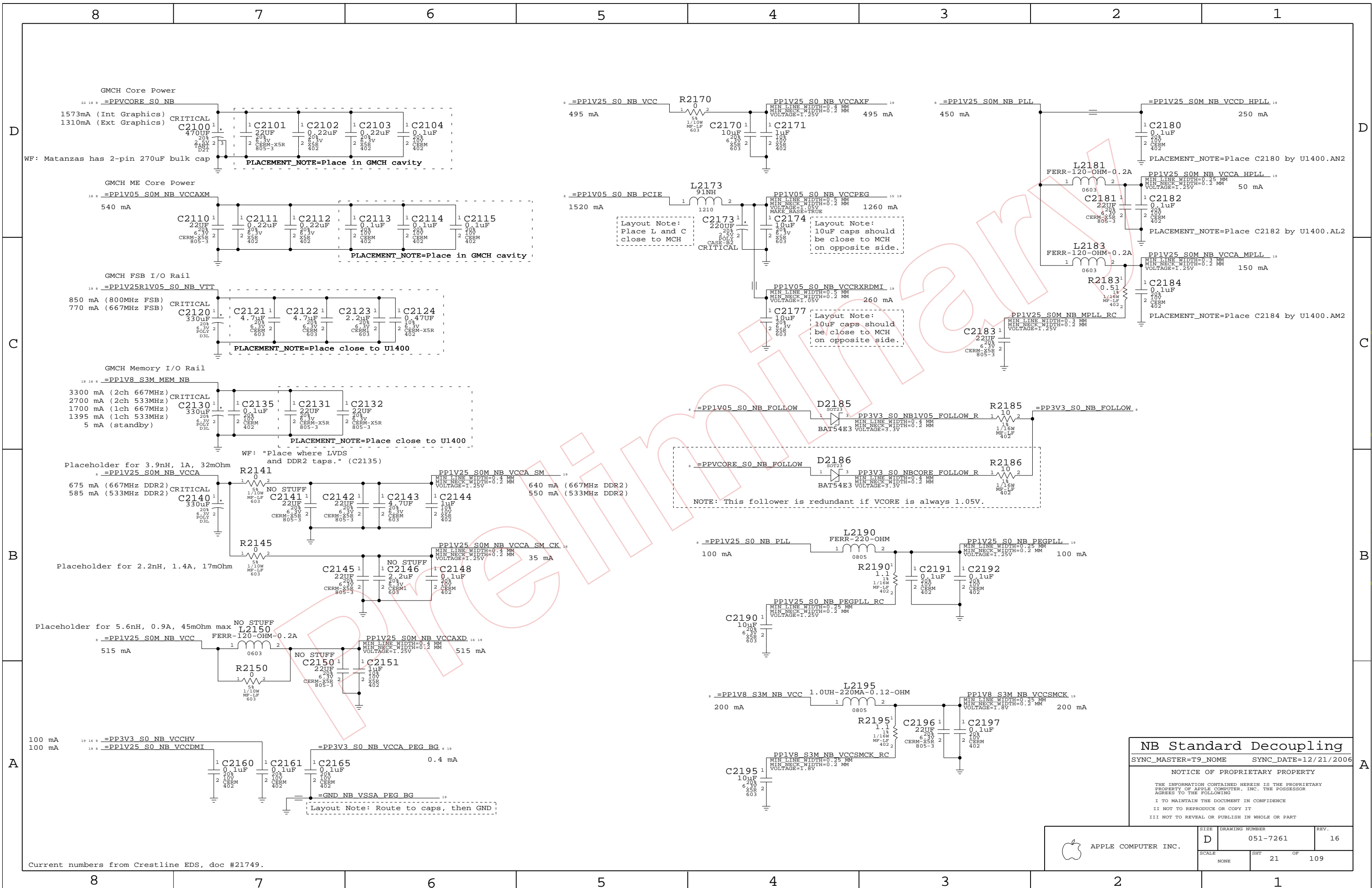
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SCALE	SHT		OF
NONE	20		109

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**NB Standard Decoupling**

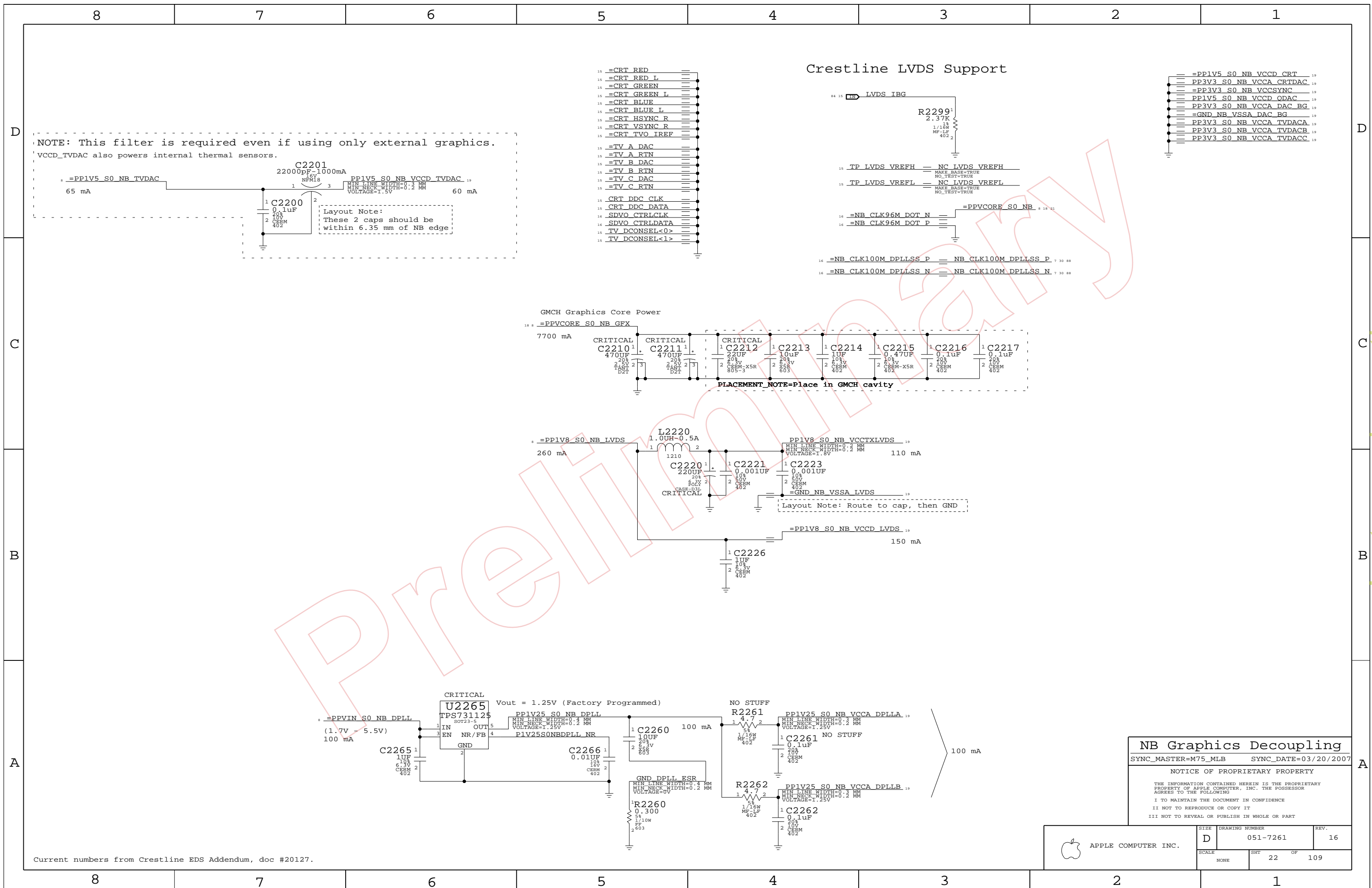
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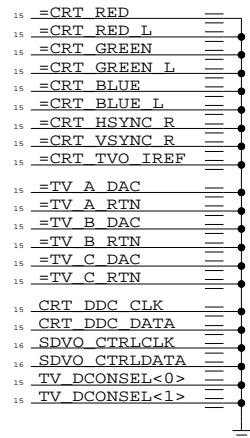
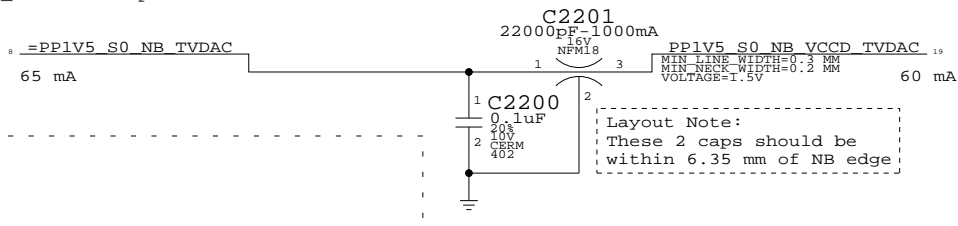
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SCALE	SHT	OF	
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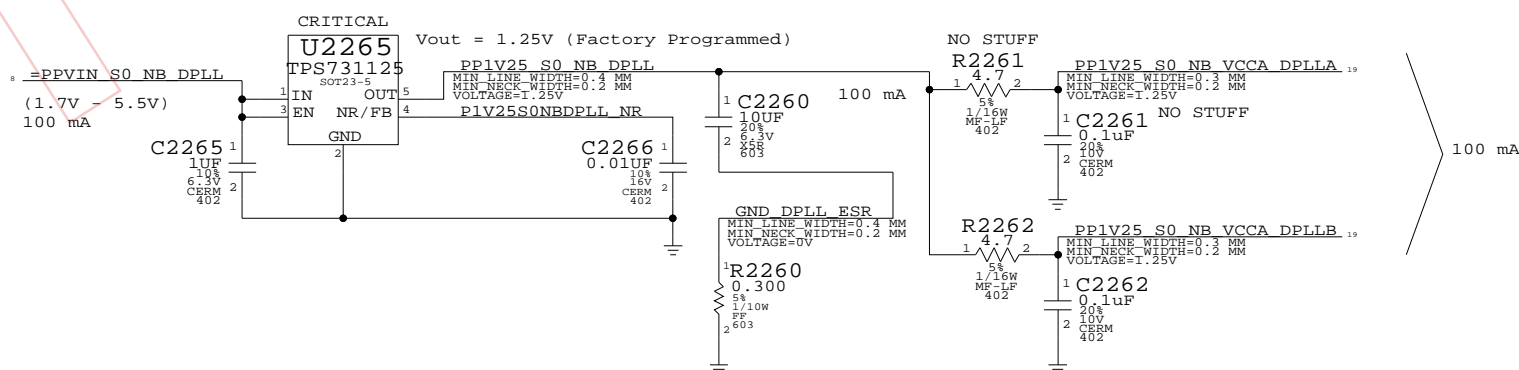
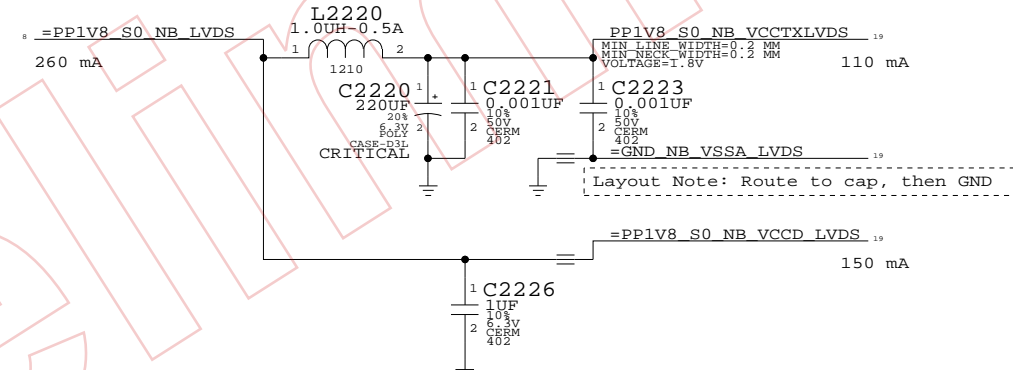
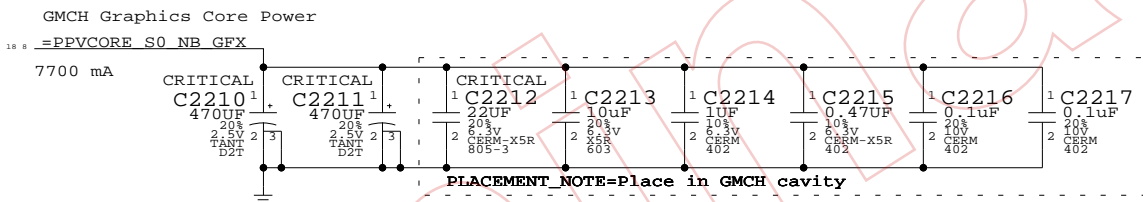
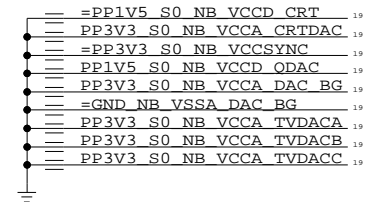
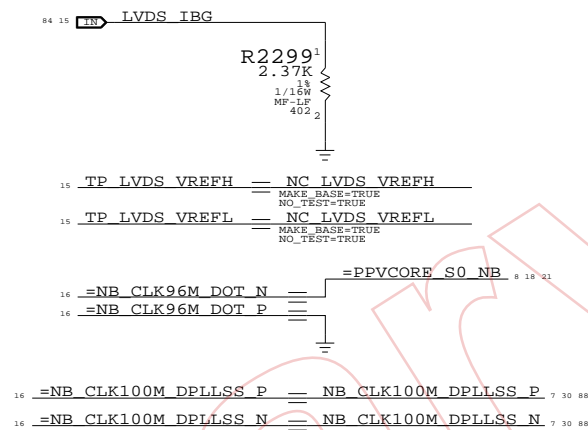
Current numbers from Crestline EDS, doc #21749.



NOTE: This filter is required even if using only external graphics.  
 VCCD\_TVDAC also powers internal thermal sensors.



### Crestline LVDS Support



### NB Graphics Decoupling

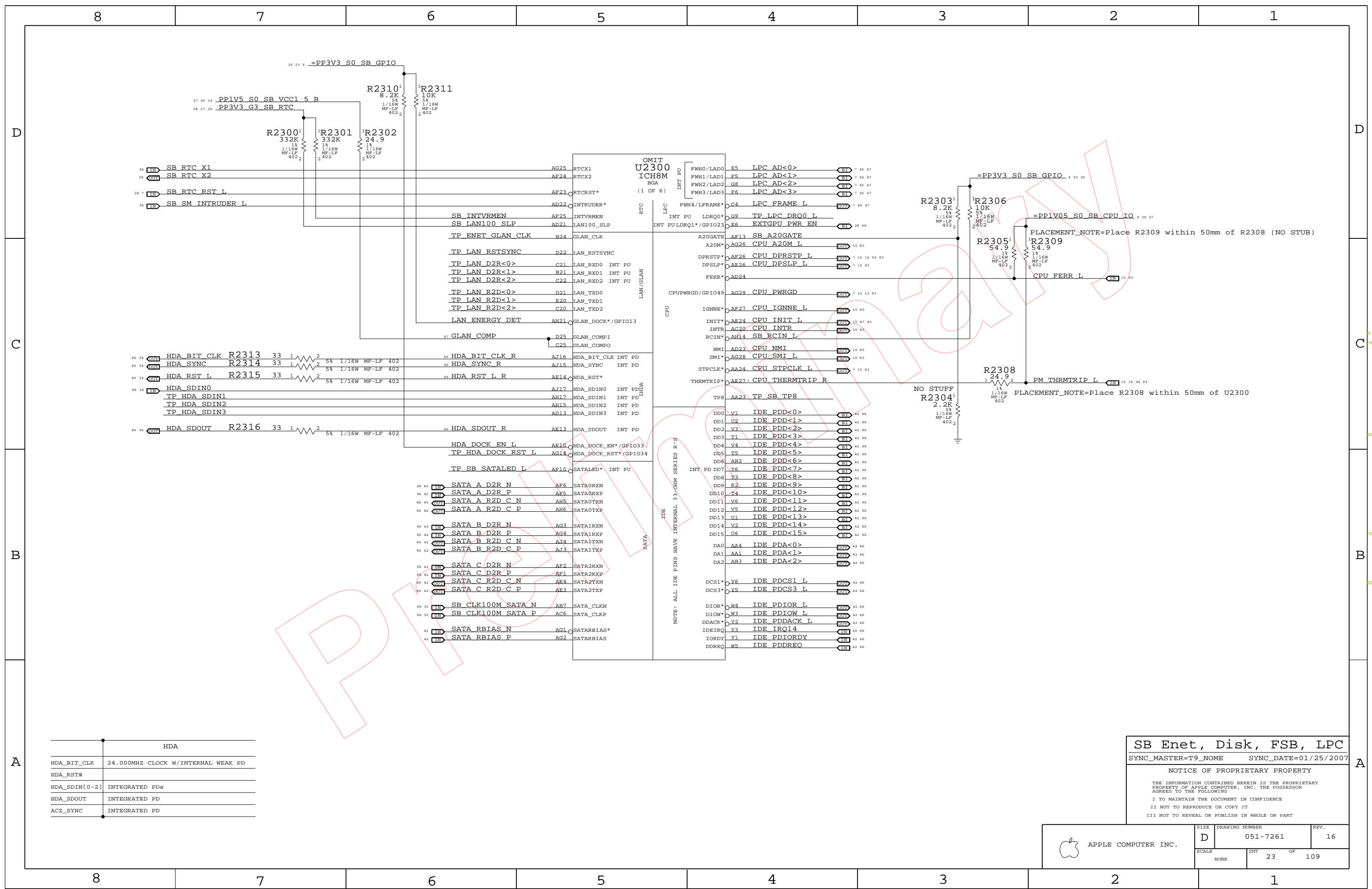
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NONE	22	109	

Current numbers from Crestline EDS Addendum, doc #20127.



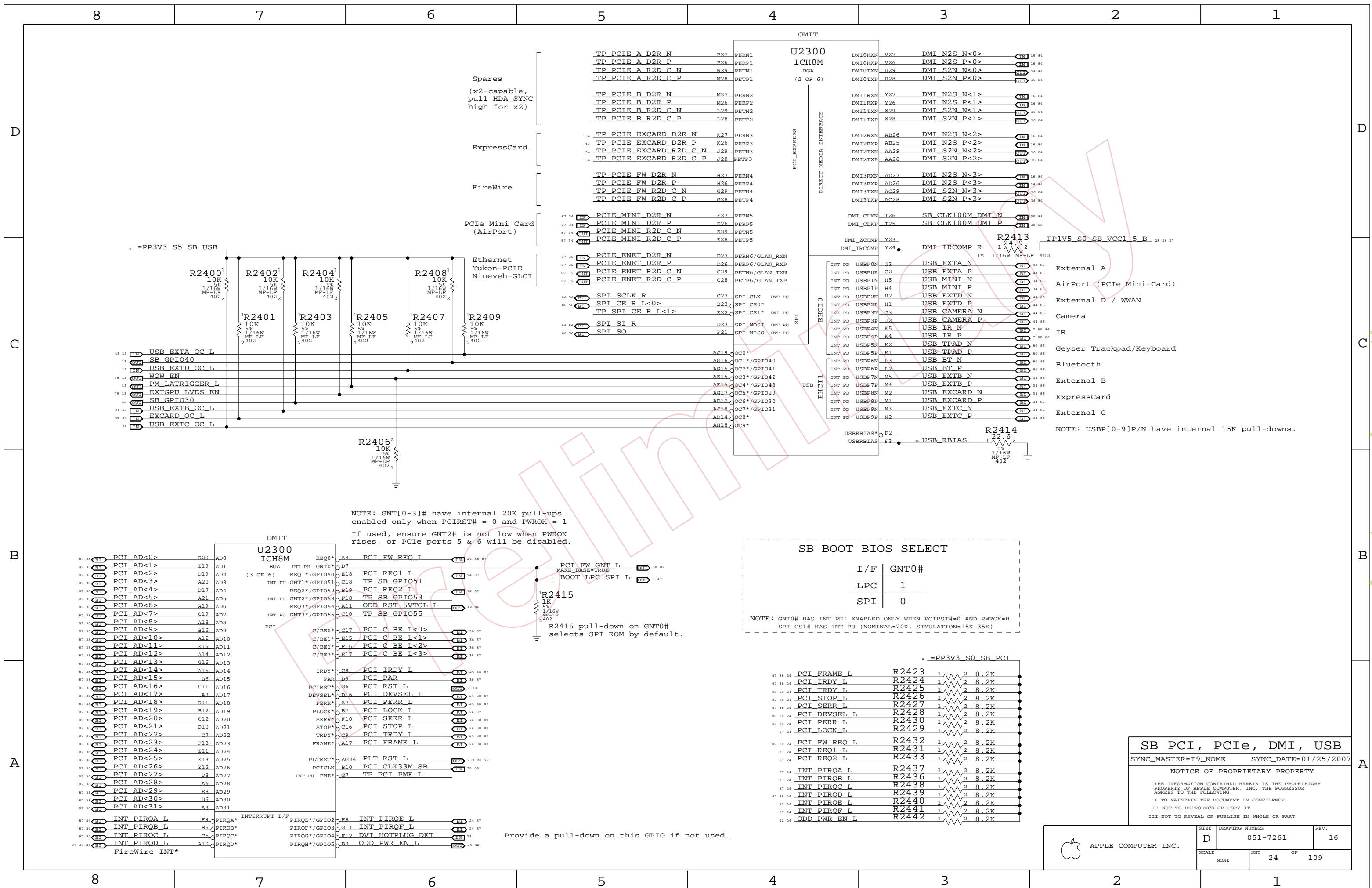
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SB Enet, Disk, FSB, LPC  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007

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Signal	Description
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

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	D	051-7261	16
SCALE	SHT	OF	REV.
NONE	23	109	



NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1. If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

**SB BOOT BIOS SELECT**

I/F	GNT0#
LPC	1
SPI	0

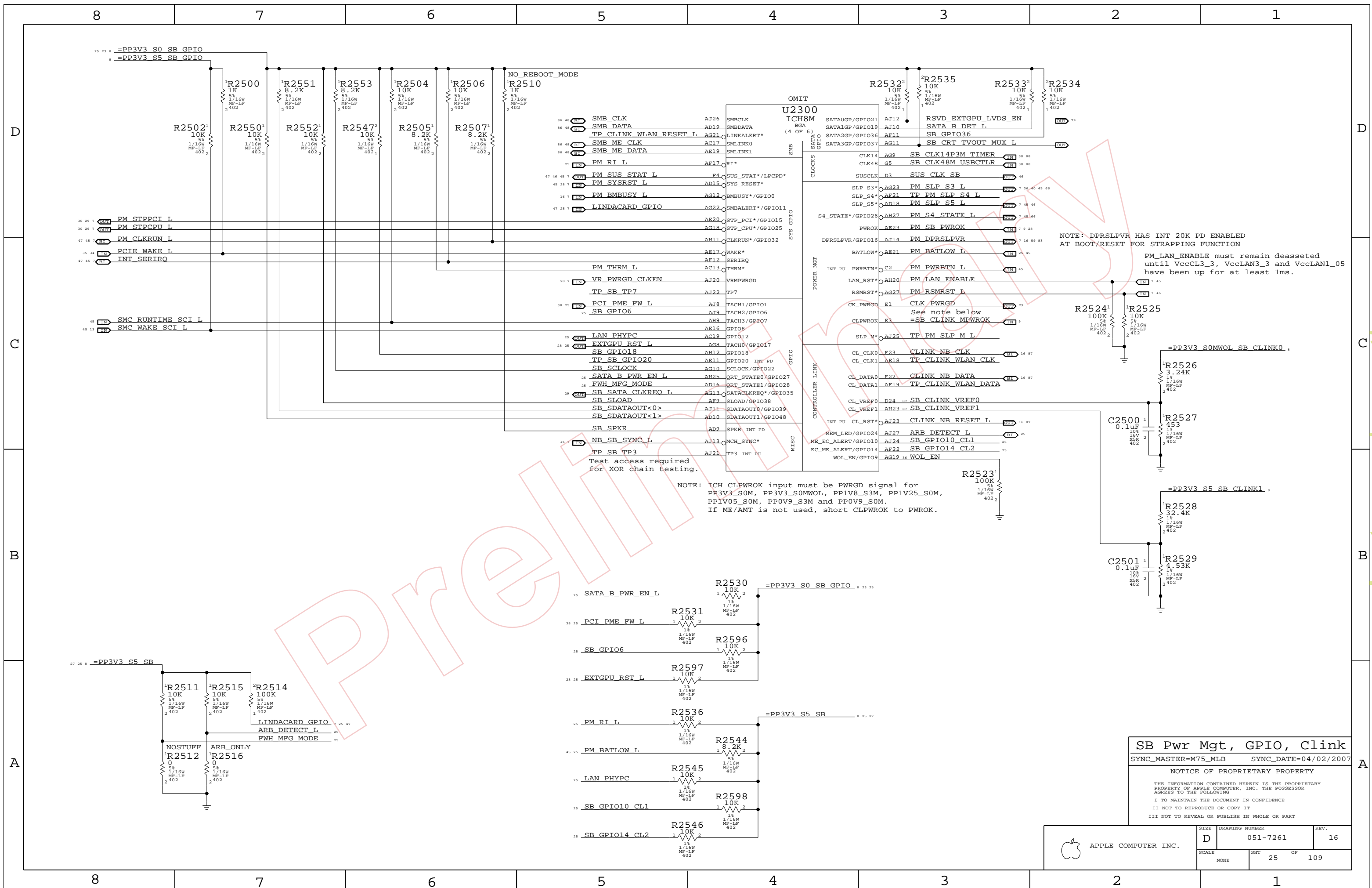
NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H  
SPI\_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

**SB PCI, PCIe, DMI, USB**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007

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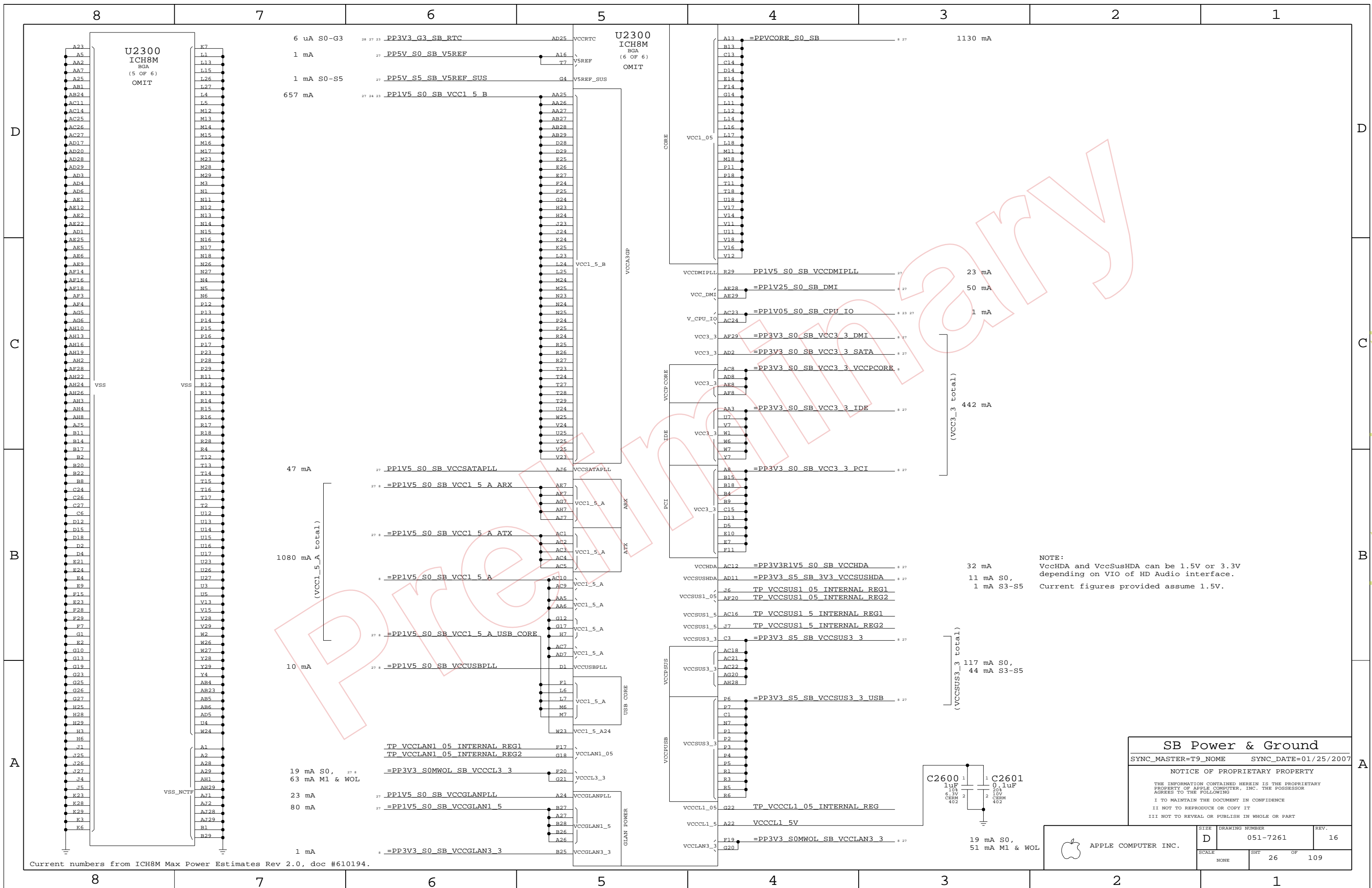
NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION  
 PM\_LAN\_ENABLE must remain deasserted until VccCL3\_3, VccLAN3\_3 and VccLAN1\_05 have been up for at least 1ms.

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3\_S0M, PP3V3\_S0MWOL, PP1V8\_S3M, PP1V25\_S0M, PP1V05\_S0M, PP0V9\_S3M and PP0V9\_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

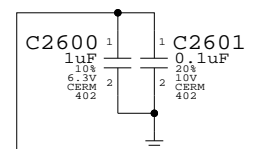
**SB Pwr Mgt, GPIO, Clink**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=04/02/2007

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NONE	25	109	



NOTE:  
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.  
Current figures provided assume 1.5V.



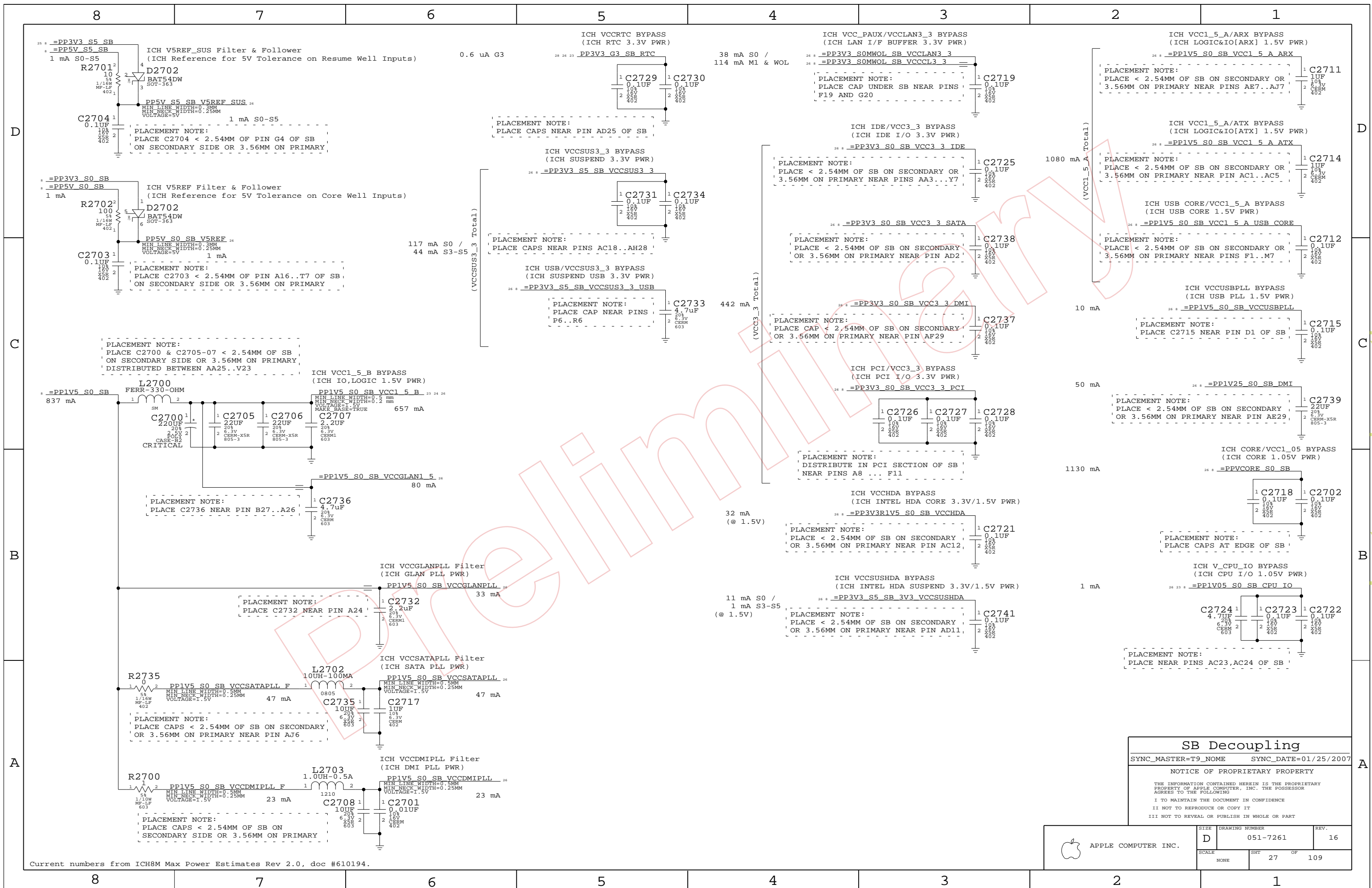
SB Power & Ground		
SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	
NOTICE OF PROPRIETARY PROPERTY		
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SCALE NONE	SIZE D	DRAWING NUMBER 051-7261	REV. 16
	SHT 26	OF 109	



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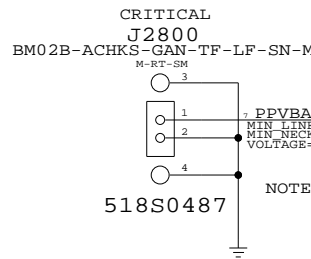
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**SB Decoupling**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007  
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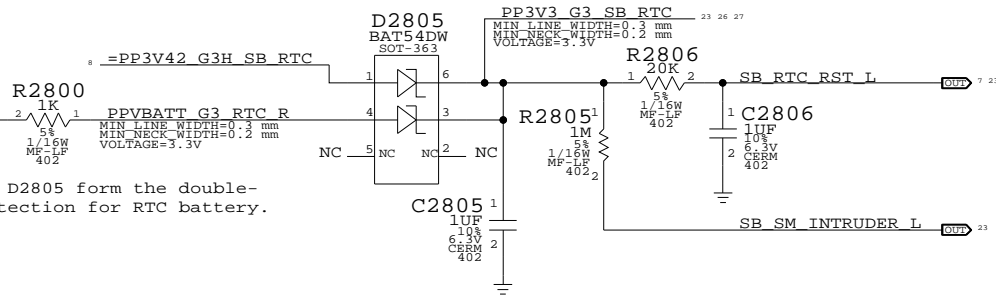
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
NONE	27	109	

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

Coin-Cell Connector

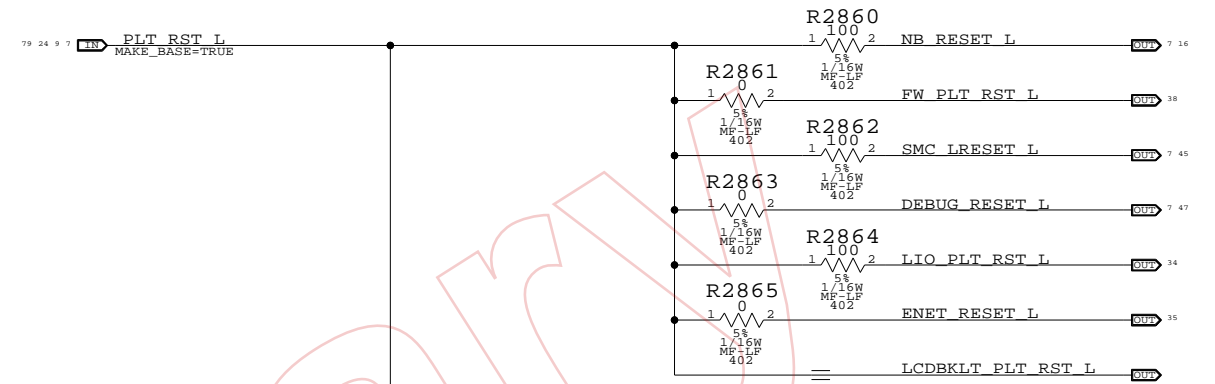


RTC Power Sources

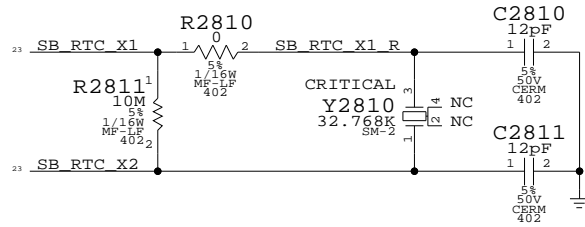


Platform Reset Connections

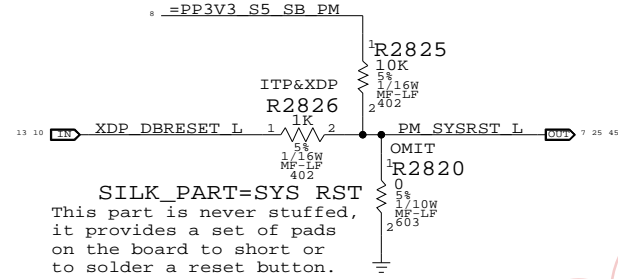
Unbuffered



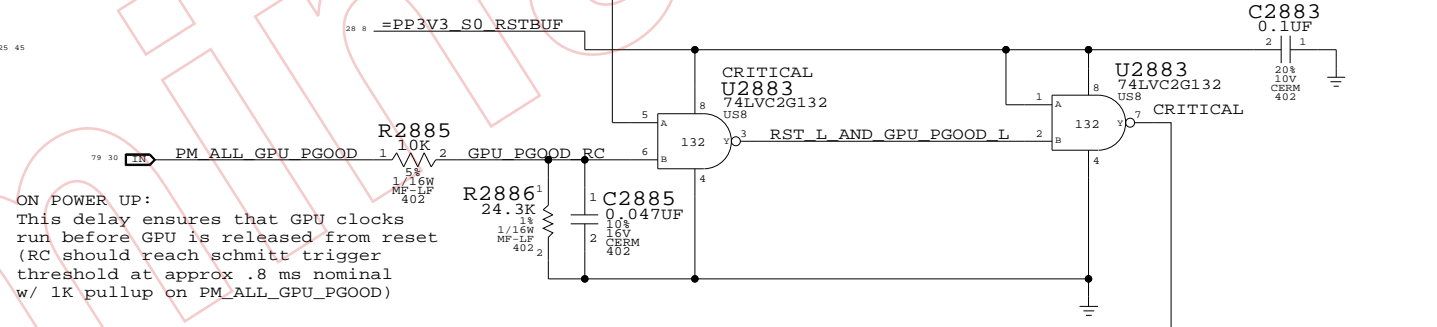
SB RTC Crystal



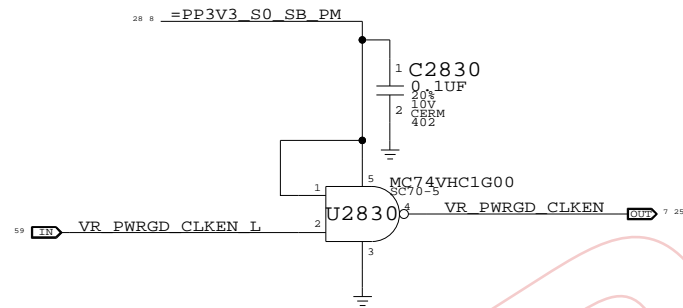
System Reset "Button"



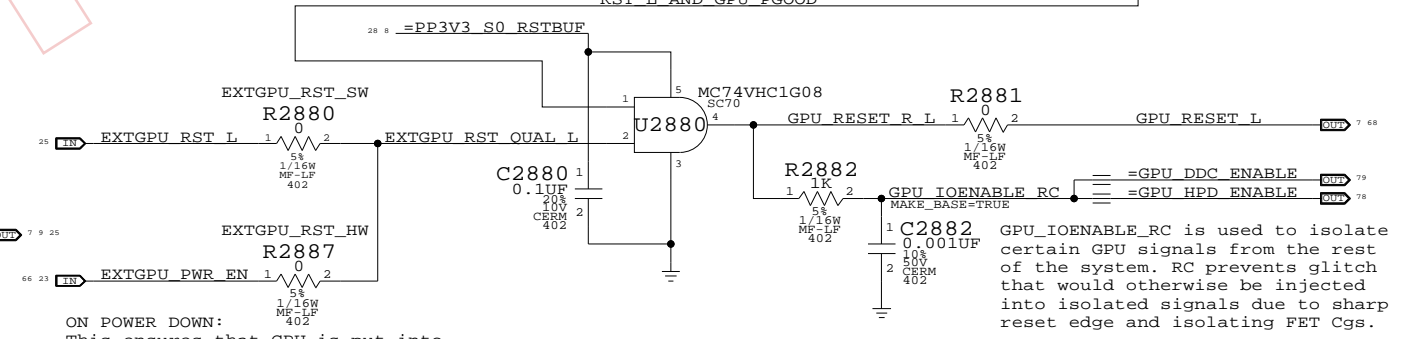
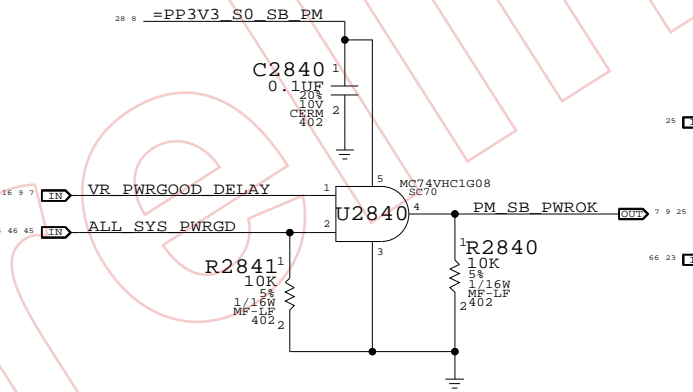
Muxed GFX GPU Reset Support



VRMPWRGD Inverter



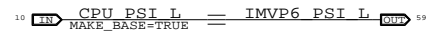
PWROK Circuit



PCI Reset Connections



CPU VCore ForcePSI

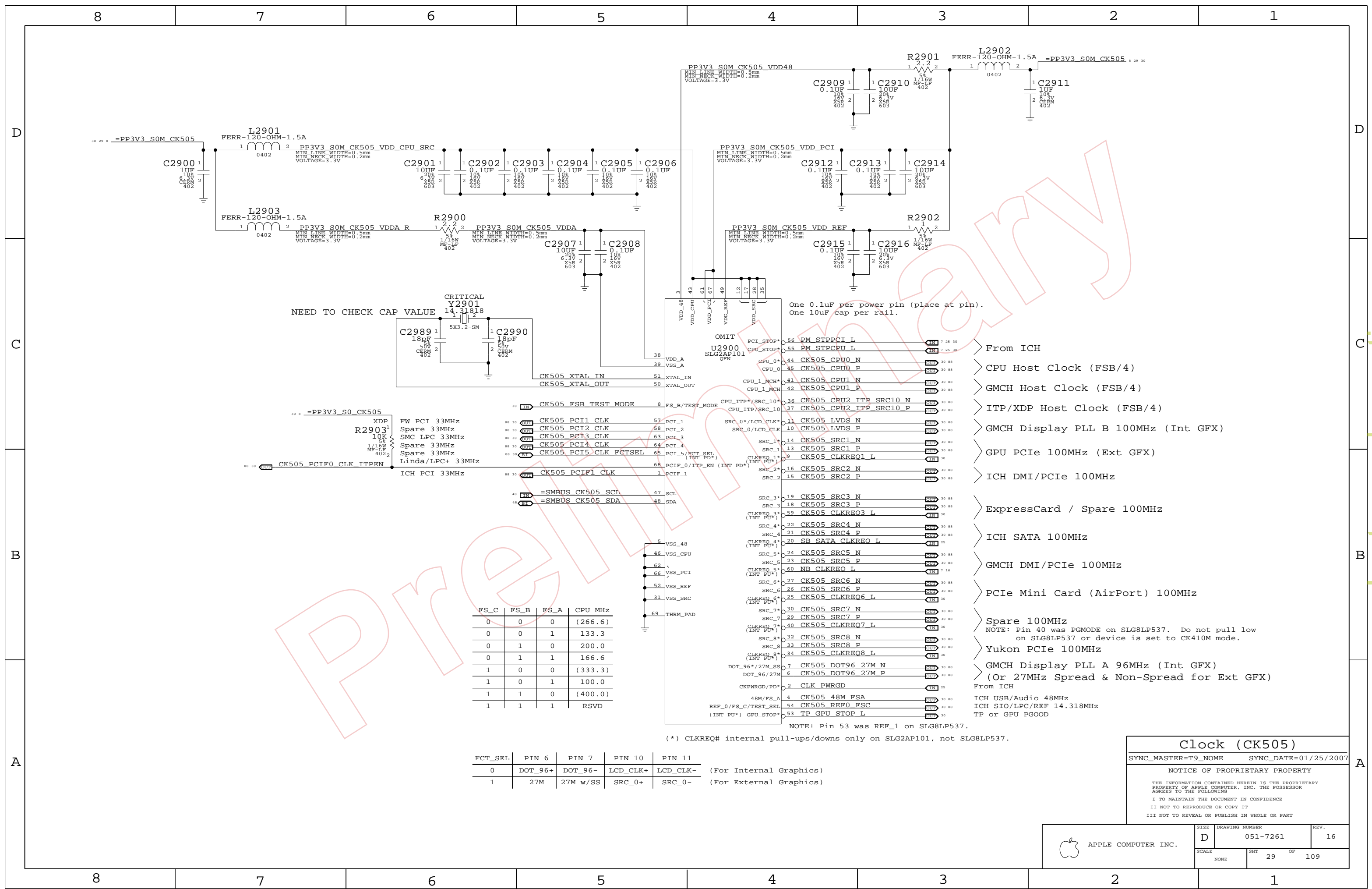


SB Misc  
SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007  
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NEED TO CHECK CAP VALUE

One 0.1uF per power pin (place at pin).  
One 10uF cap per rail.

FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-
1	27M	27M w/SS	SRC_0+	SRC_0-

(For Internal Graphics)  
(For External Graphics)

- > From ICH
- > CPU Host Clock (FSB/4)
- > GMCH Host Clock (FSB/4)
- > ITP/XDP Host Clock (FSB/4)
- > GMCH Display PLL B 100MHz (Int GFX)
- > GPU PCIe 100MHz (Ext GFX)
- > ICH DMI/PCIe 100MHz
- > ExpressCard / Spare 100MHz
- > ICH SATA 100MHz
- > GMCH DMI/PCIe 100MHz
- > PCIe Mini Card (AirPort) 100MHz
- > Spare 100MHz  
NOTE: Pin 40 was PGMODE on SLG8LP537. Do not pull low on SLG8LP537 or device is set to CK410M mode.
- > Yukon PCIe 100MHz
- > GMCH Display PLL A 96MHz (Int GFX)  
(Or 27MHz Spread & Non-Spread for Ext GFX)
- From ICH
- ICH USB/Audio 48MHz
- ICH SIO/LPC/REF 14.318MHz
- TP or GPU PGOOD

NOTE: Pin 53 was REF\_1 on SLG8LP537.

(\*) CLKREQ# internal pull-ups/downs only on SLG2AP101, not SLG8LP537.

**Clock (CK505)**

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SCALE		SHT	OF
NONE		29	109

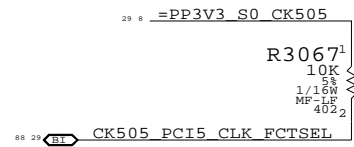
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# CLK Termination

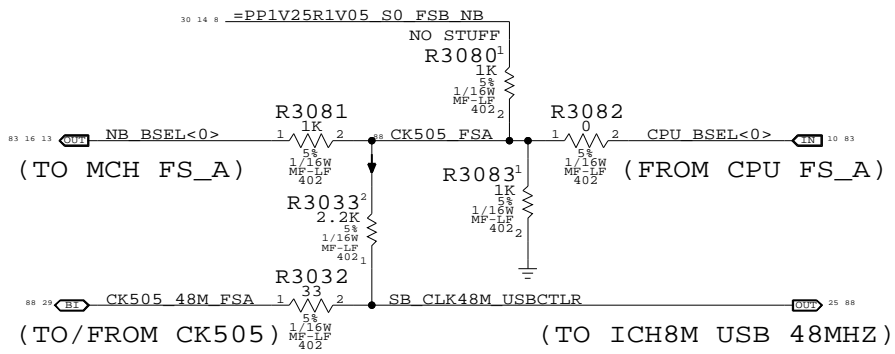
(Note: HOST/SRC/GFX clock termination removed. Siligo SL8GLP536 or equiv. support only)

## CK505 Configuration Straps

FCT\_SEL (GFX clock select)



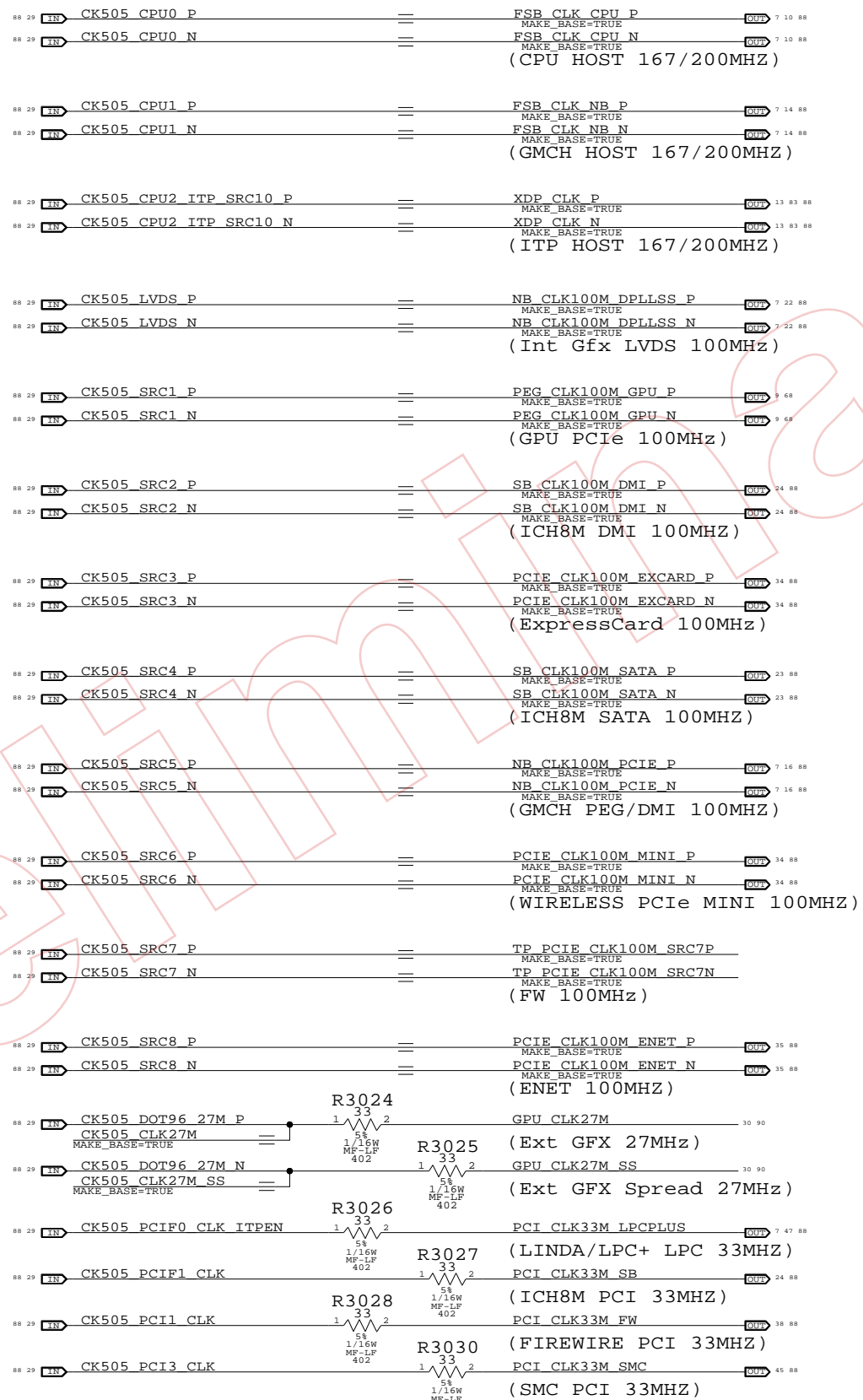
FS\_A, FS\_B, FS\_C (Host clock freq select)



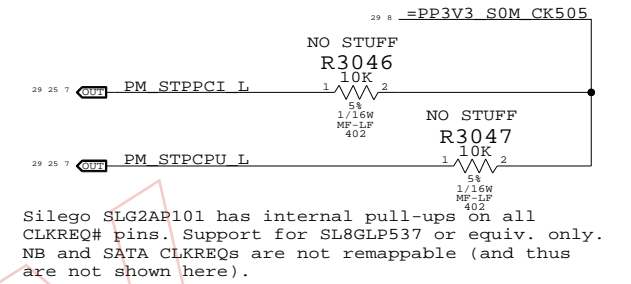
FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090 for manual CPU clk frequency.

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

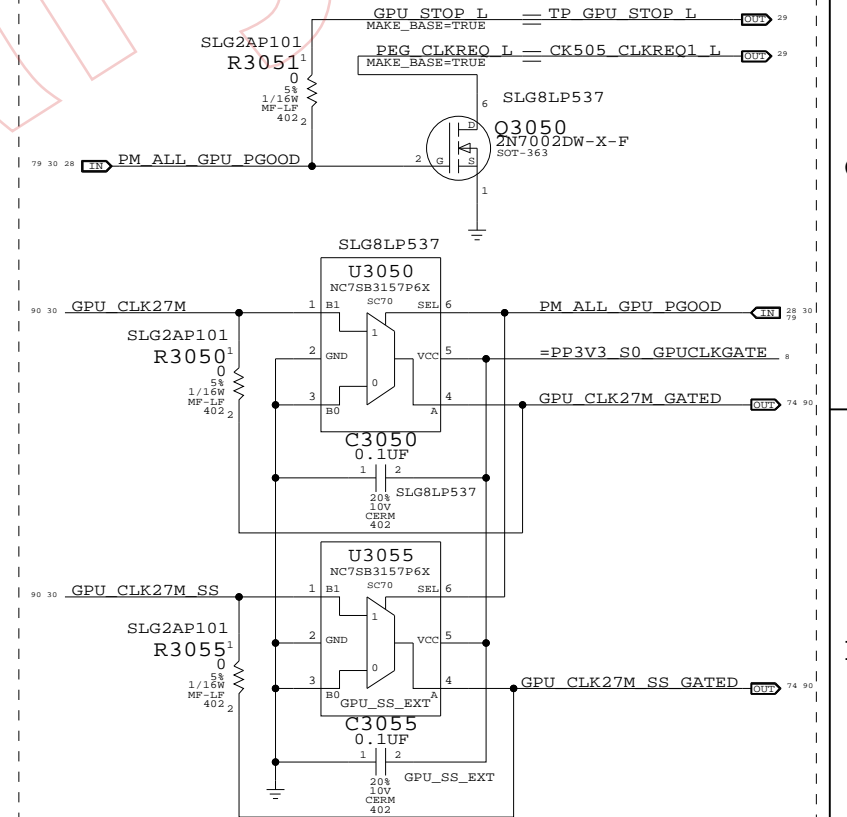


## CLKREQ Controls

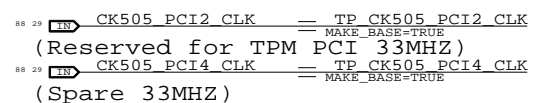


Silego SLG2AP101 has internal pull-ups on all CLKREQ# pins. Support for SL8GLP537 or equiv. only. NB and SATA CLKREQs are not remappable (and thus are not shown here).

## GPU Clock Gating



## Unused Clocks



## Clock Termination

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SCALE	SHT	OF	
NONE	30	109	

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# Page Notes

Power aliases required by this page:

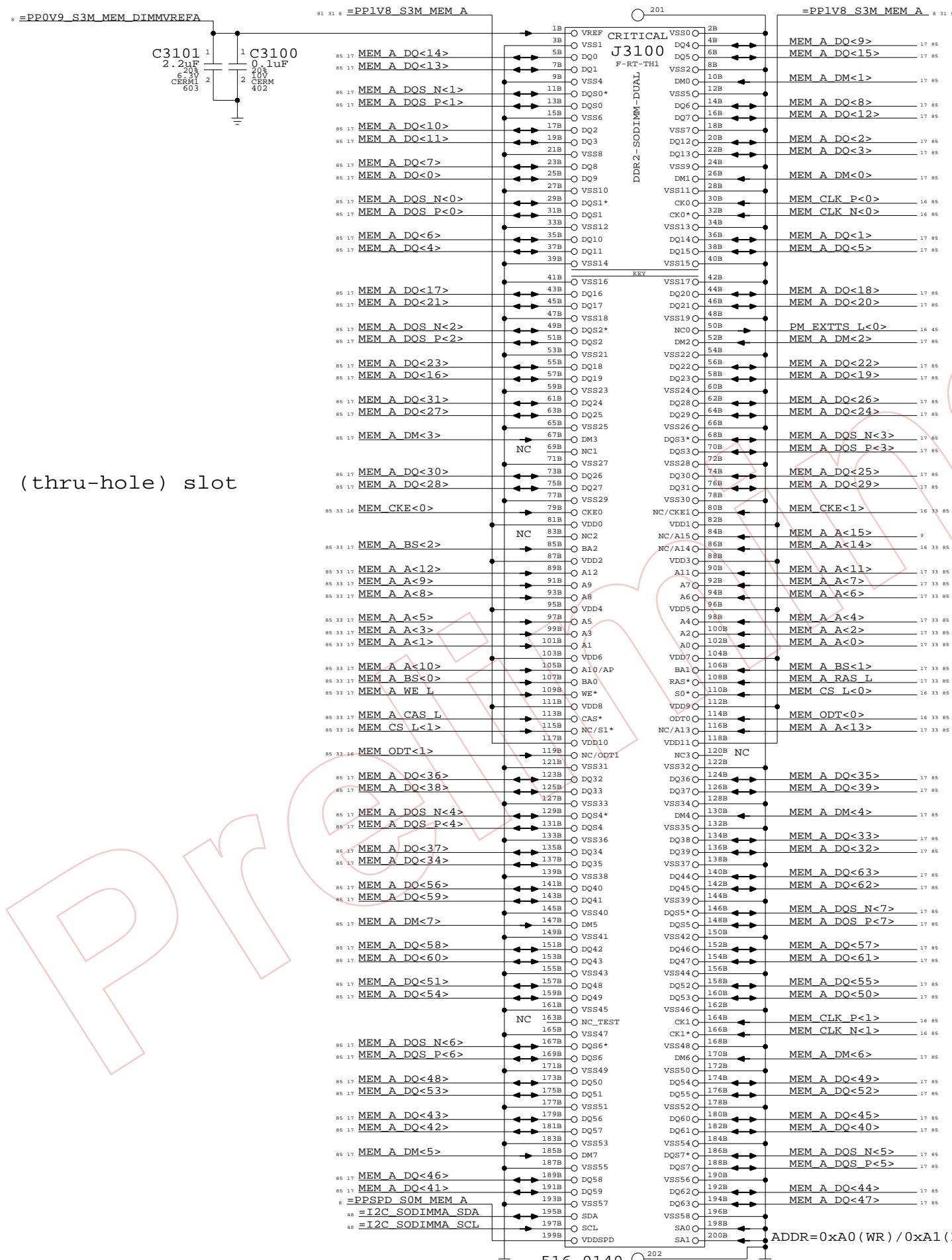
- =PP1V8\_S3M\_MEM\_A
- =PP0V9\_S3M\_MEM\_DIMMVREFA
- =PPSPD\_S0M\_MEM\_A (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C\_SODIMMA\_SCL
- =I2C\_SODIMMA\_SDA

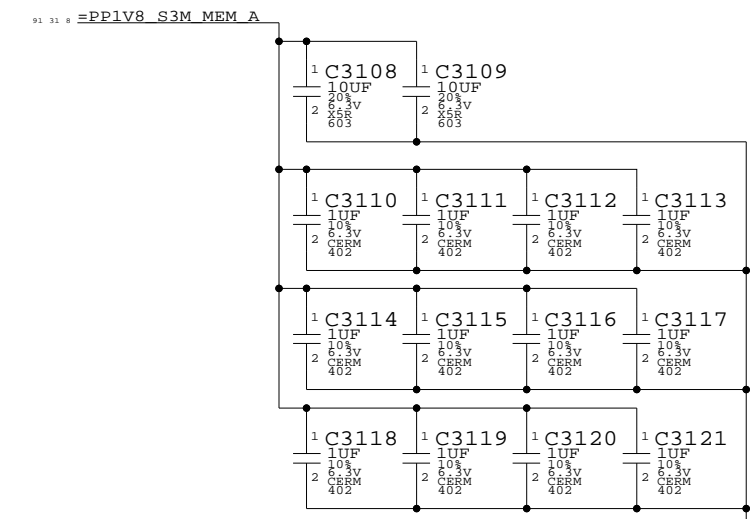
BOM options provided by this page:  
(NONE)

"Factory" (thru-hole) slot



## DDR2 Bypass Caps

(For return current)



### DDR2 SO-DIMM Connector A

SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007

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SCALE	SHT	OF	
NONE	31	109	

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# Page Notes

Power aliases required by this page:

- =PP1V8\_S3M\_MEM\_B
- =PP0V9\_S3M\_MEM\_DIMMVREFB
- =PPSPD\_S0M\_MEM\_B (2.5V - 3.3V)

Signal aliases required by this page:

- =I2C\_SODIMMB\_SCL
- =I2C\_SODIMMB\_SDA

BOM options provided by this page:

(NONE)

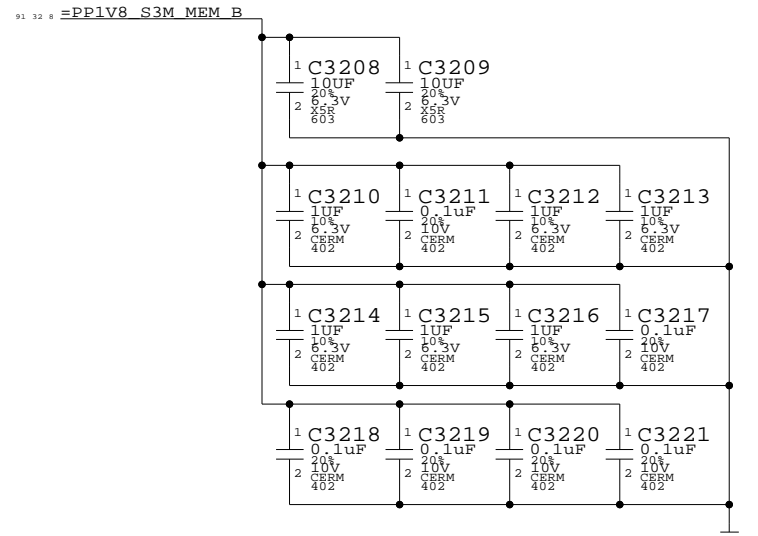
"Expansion" (surface-mount) slot

PRO



## DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector B  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007

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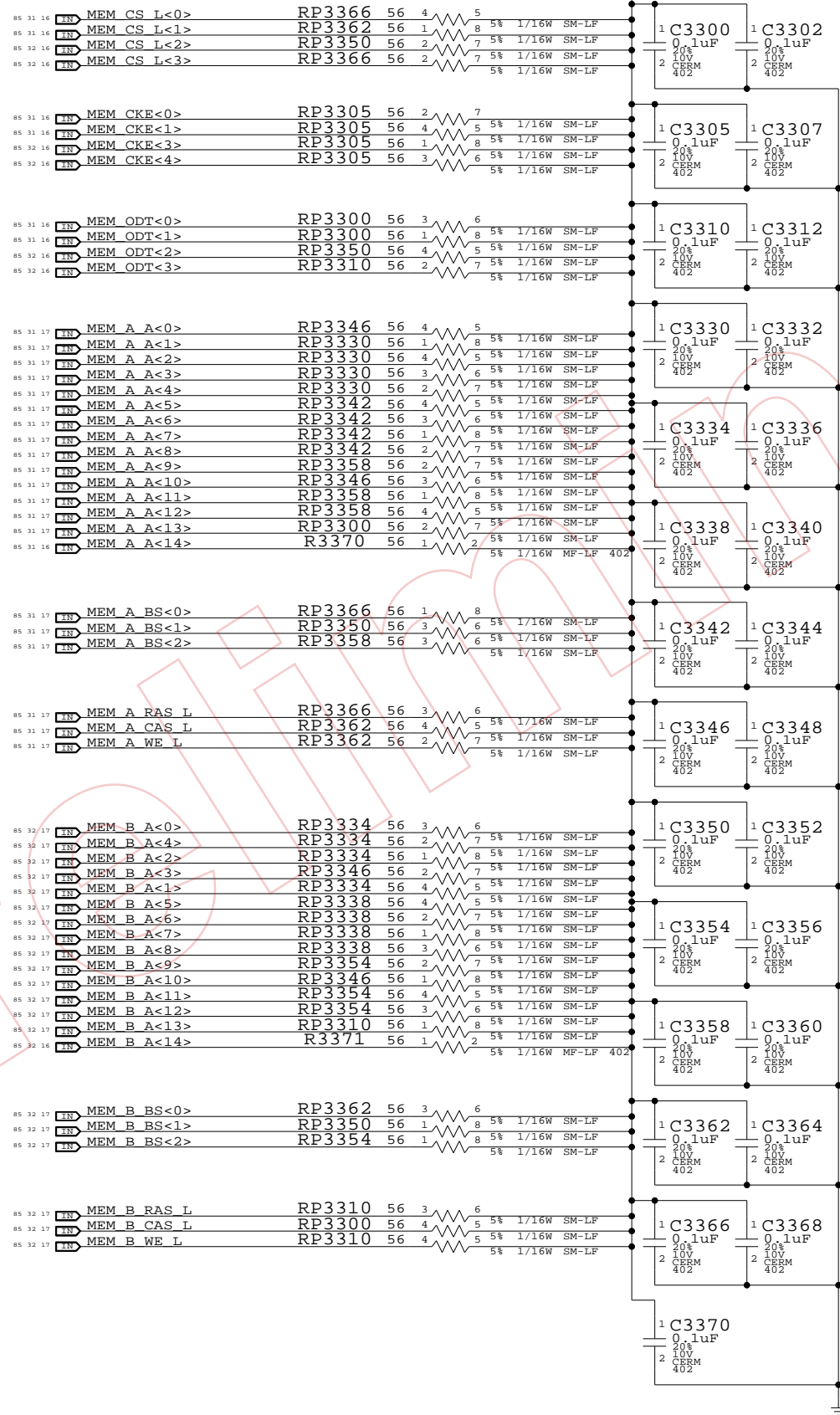
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NONE	32	109	

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One cap for each side of every RPAK, one cap for every two discrete resistors  
Ensure CS\_L and ODT resistors are close to SO-DIMM connector

:=PPOV9 SOM MEM TERM



PR

RAM

Memory Active Termination

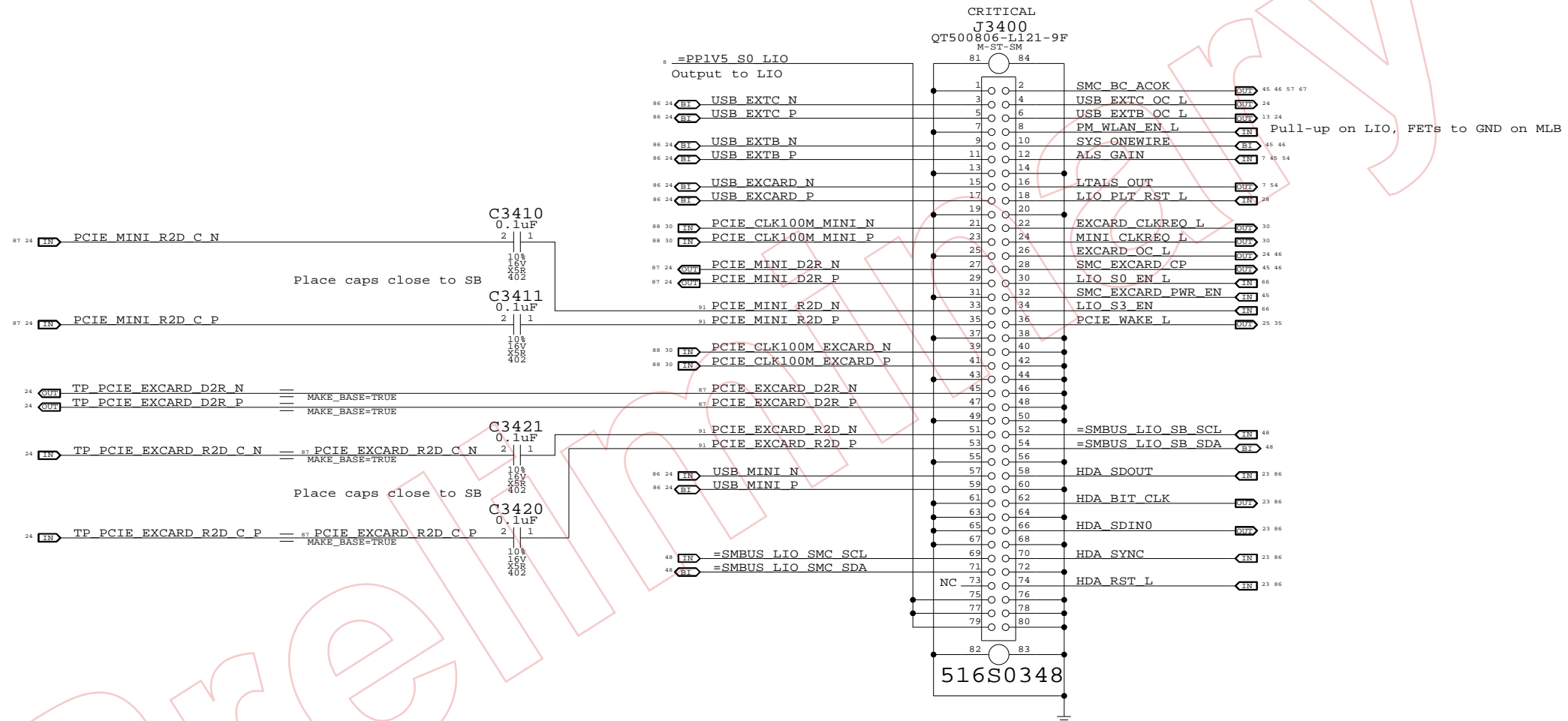
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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NONE	33	109	

# Left I/O Board Connector



PREVIEW

## Left I/O Board Connector

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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NONE	34		109

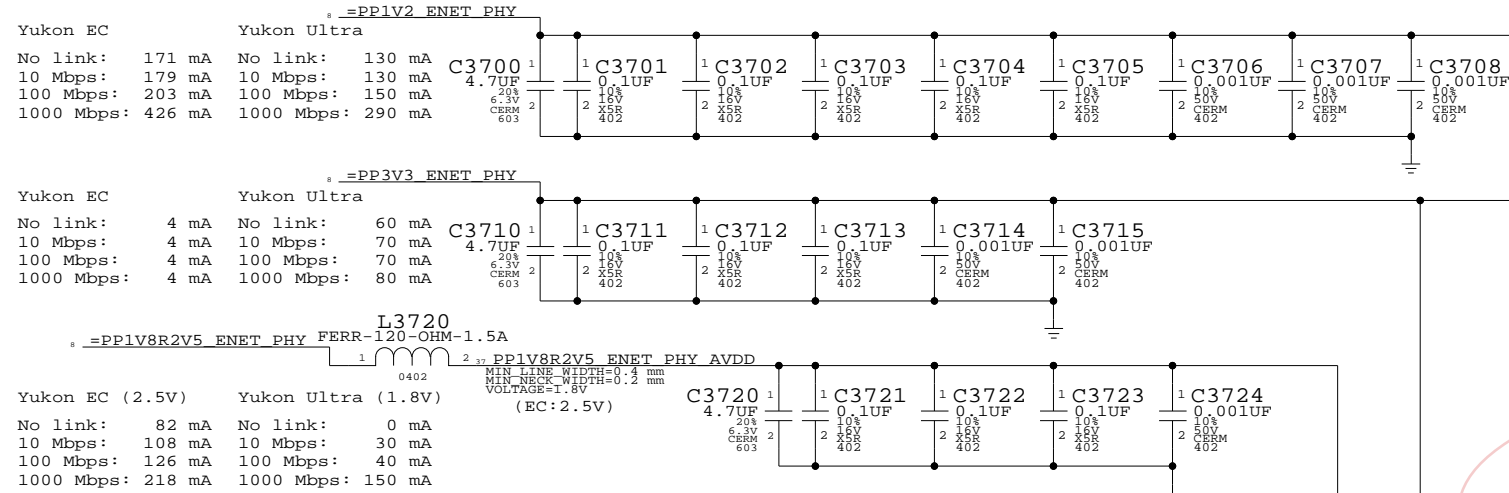
# Page Notes

Power aliases required by this page:  
 - =PP3V3\_ENET\_PHY (EC / Ultra)  
 - =PP1V8R2V5\_ENET\_PHY (2.5V / 1.8V)  
 - =YUKON\_EC\_PP2V5\_ENET (2.5V / GND)  
 - =PP1V2\_ENET\_PHY

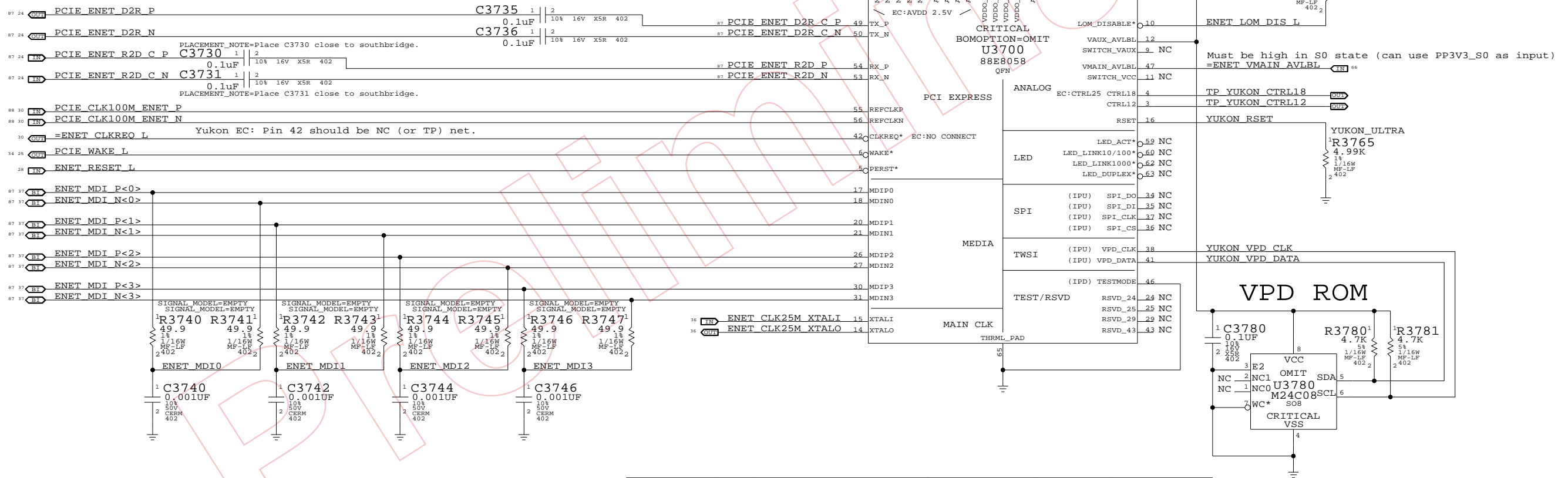
Signal aliases required by this page:  
 - =ENET\_CLKREQ\_L (NC/TP for Yukon EC)  
 - =ENET\_VMAIN\_AVLBLE (See note by pin)

BOM options provided by this page:  
 YUKON\_EC - Selects Yukon EC RSET value.  
 YUKON\_ULTRA - Selects Yukon Ultra RSET.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.



=YUKON\_EC\_PP2V5\_ENET  
 Yukon EC: Alias to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF & 1x 0.001uF caps  
 Yukon Ultra: Alias to GND



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0386	1	IC, 88E8058, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_ULTRA
341S2060	1	IC, FLASH, 88E8058 ETHERNET VPD, IIC, SO8	U3780	CRITICAL	YUKON_ULTRA
338S0270	1	IC, 88E8053, GIGABIT ENET XCVR, 64P QFN	U3700	CRITICAL	YUKON_EC
341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U3780	CRITICAL	YUKON_EC
114S0285	1	RES, 4.87K, 1%, 1/16W, 0402, LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:

- Alias =YUKON\_EC\_PP2V5\_ENET to PP1V8R2V5\_ENET\_PHY\_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5\_ENET\_PHY and magnetics. Can also use BCP69T1 connected to CTRL18 pin 4 for internal VR.
- Connect =ENET\_CLKREQ\_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON\_ULTRA)
- Use YUKON\_EC and YUKON\_ULTRA BOMOPTIONS to select stuffed part

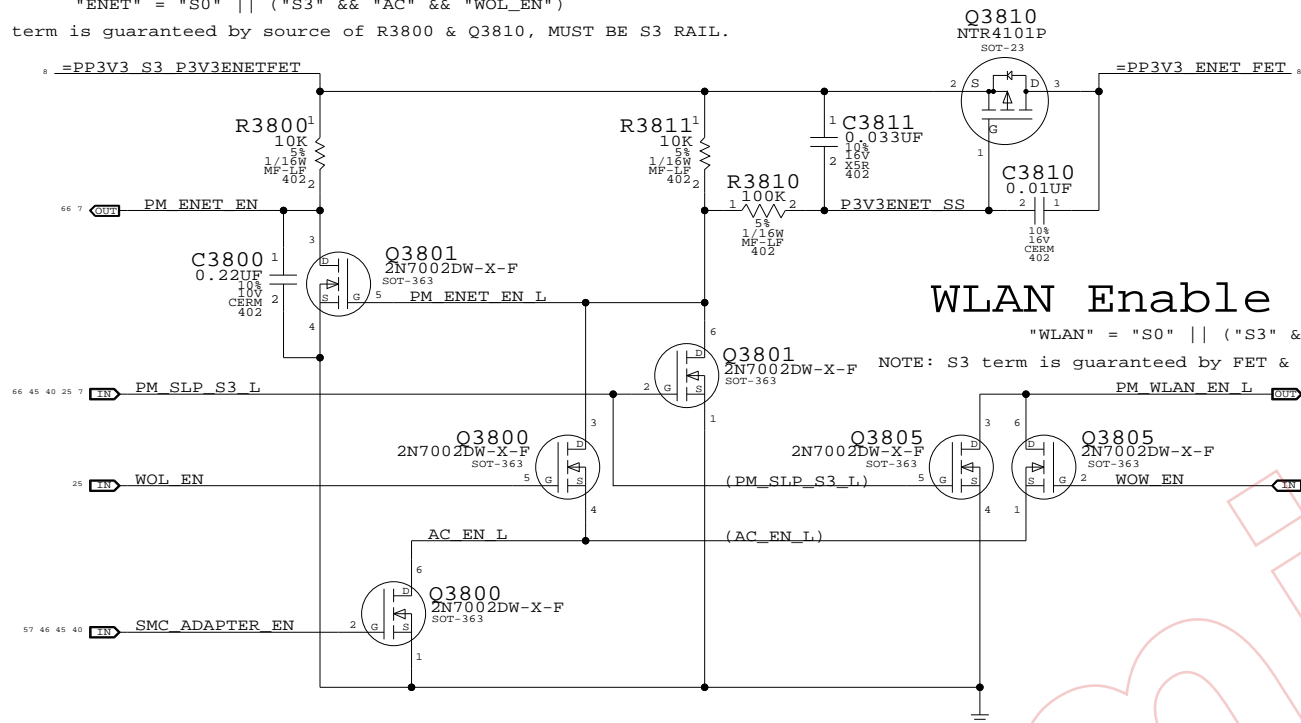
**Ethernet (Yukon)**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007  
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## ENET Enable Generation

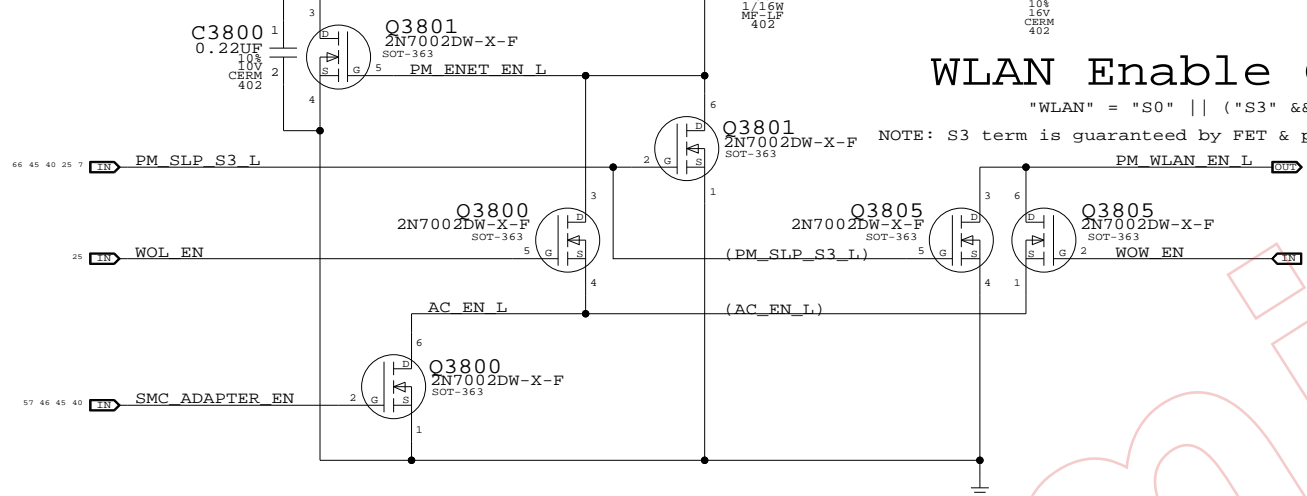
"ENET" = "S0" || ("S3" && "AC" && "WOL\_EN")  
 NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.



## 3.3V ENET FET

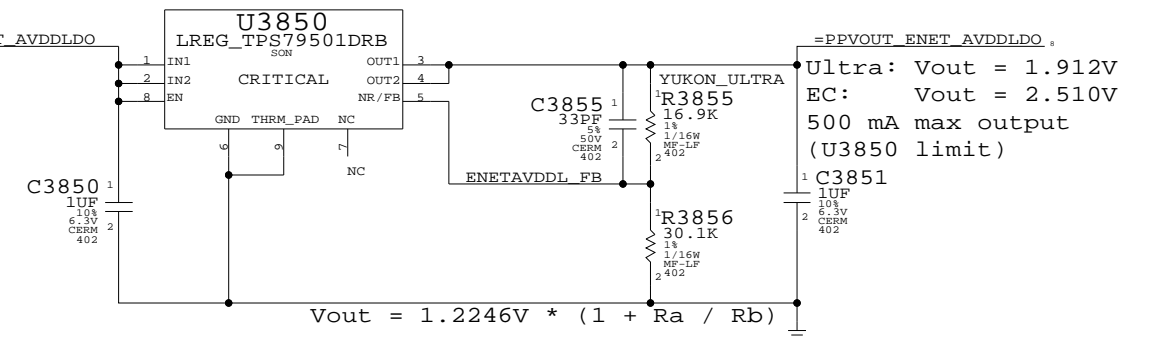
## WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW\_EN")  
 NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.



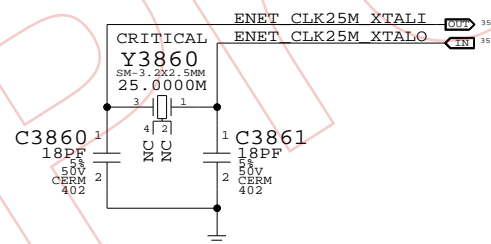
## Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC  
 Yukon Ultra requires 1.9V on its magnetics to pass compliance tests



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0363	1	RES, 31.6K, 1%, 1/16W, 402, LF	R3855		YUKON_EC

## Yukon Crystal



## Yukon Power Control

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SCALE	SHT	OF	
NONE	38	109	



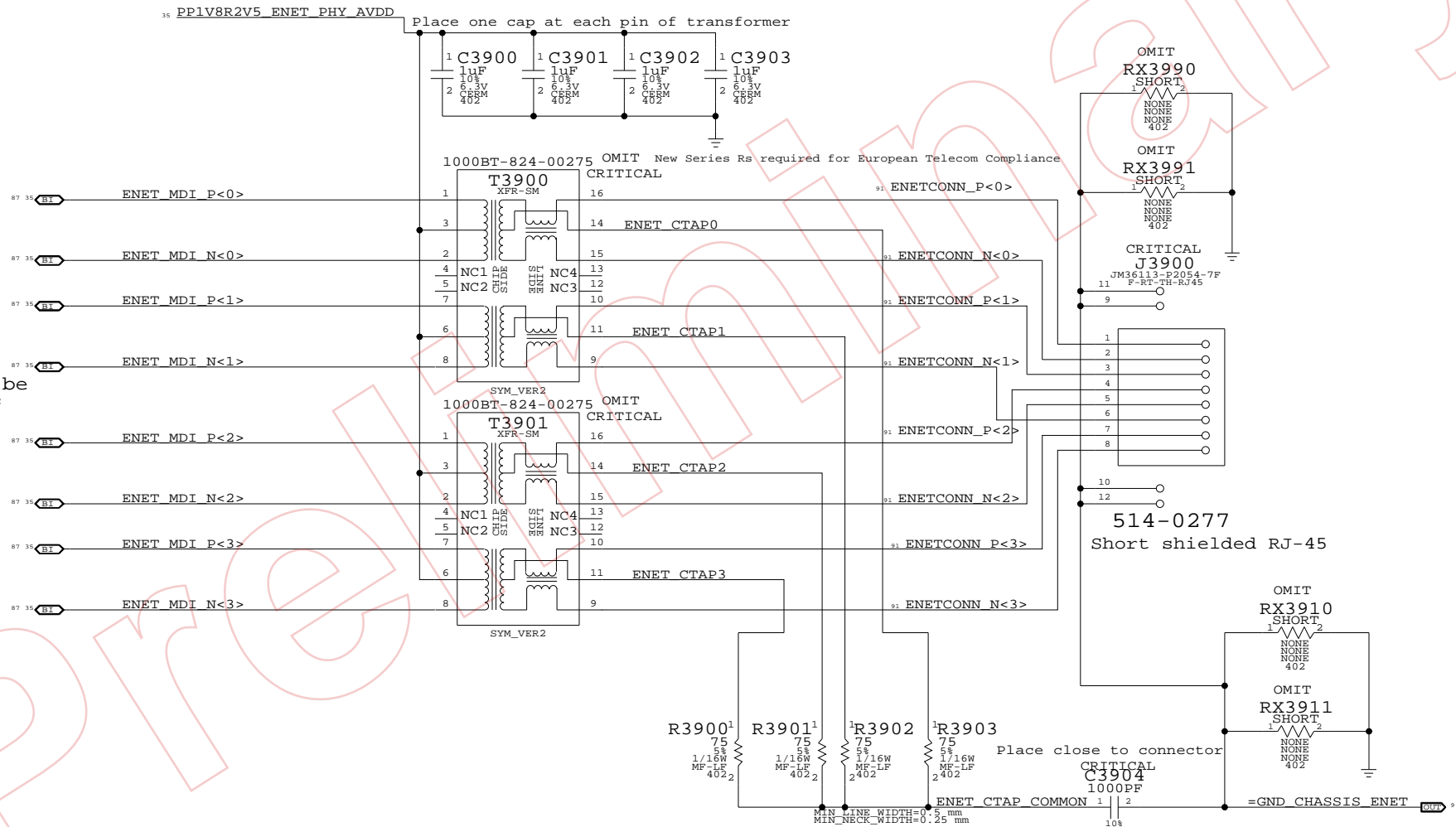
# Page Notes

Power aliases required by this page:  
 - =GND\_CHASSIS\_ENET

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

Transformers should be mirrored on opposite sides of the board



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15780030	2	XPR, ISO, HALP-PORT, 1000T, 16P, SMD, 2MM	T3900, T3901	CRITICAL	

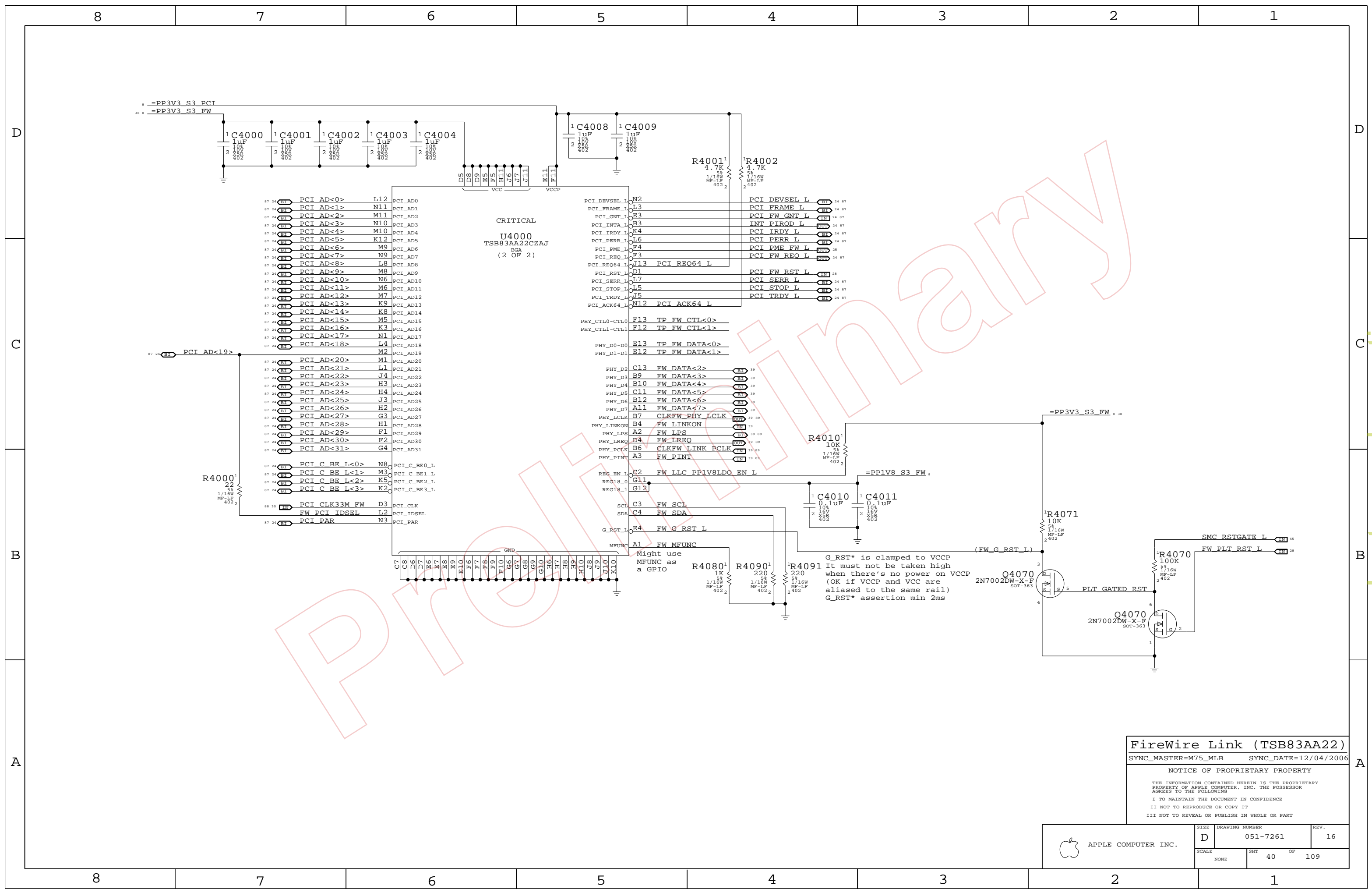
**Ethernet Connector**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/21/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	39	109	



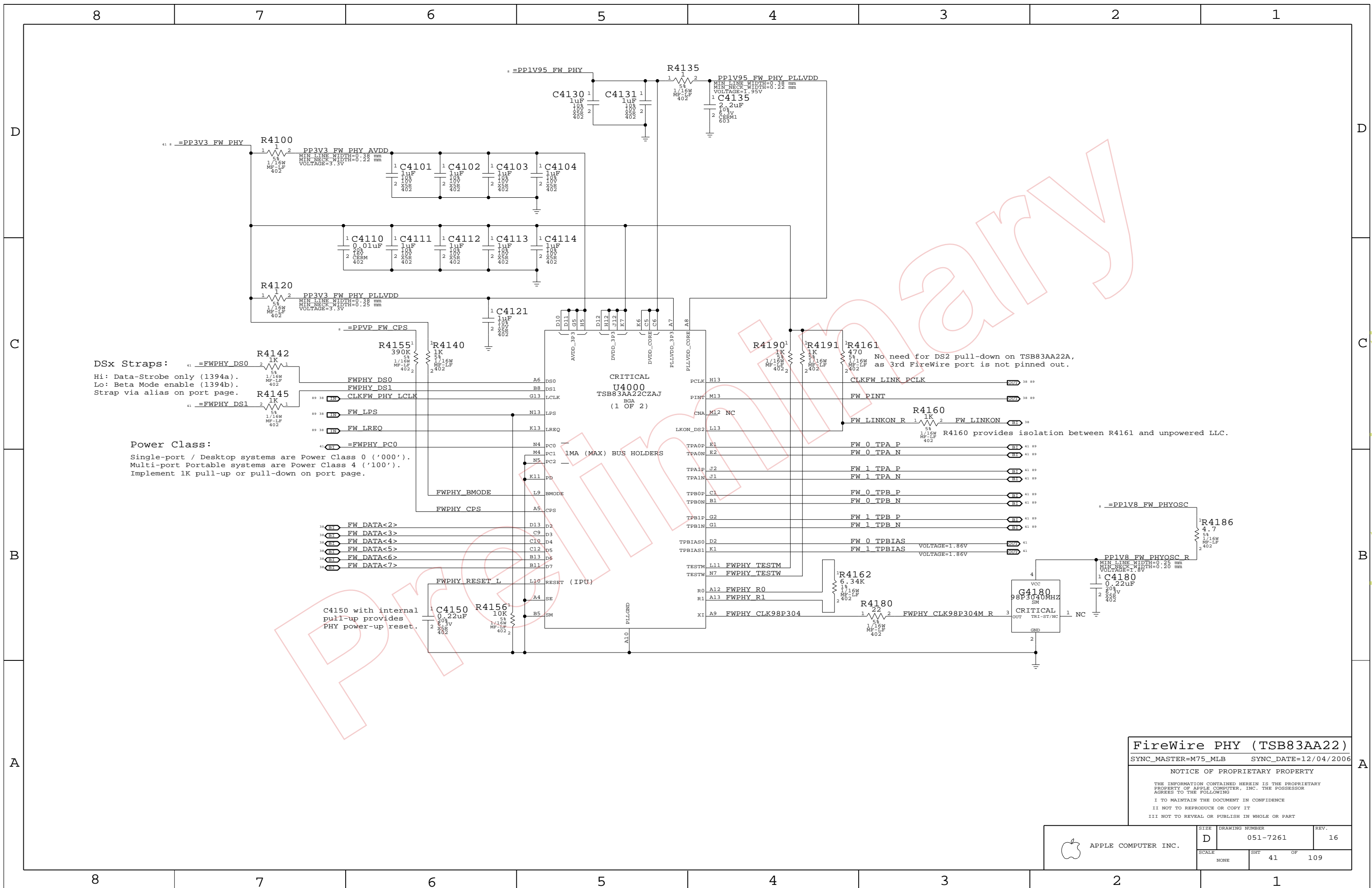
**FireWire Link (TSB83AA22)**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006

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APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHEET 40	OF 109



PP3V3 FW PHY AVDD

R4100

PP3V3 FW PHY PLLVDD

R4120

PP3V3 FW PHY PLLVDD

DSx Straps:

Hi: Data-Strobe only (1394a).

Lo: Beta Mode enable (1394b).

Strap via alias on port page.

R4142

R4145

Power Class:

Single-port / Desktop systems are Power Class 0 ('000').

Multi-port Portable systems are Power Class 4 ('100').

Implement 1K pull-up or pull-down on port page.

C4150 with internal pull-up provides PHY power-up reset.

No need for DS2 pull-down on TSB83AA22A, as 3rd FireWire port is not pinned out.

R4160 provides isolation between R4161 and unpowered LLC.

FireWire PHY (TSB83AA22)

SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHIT 41	OF 109

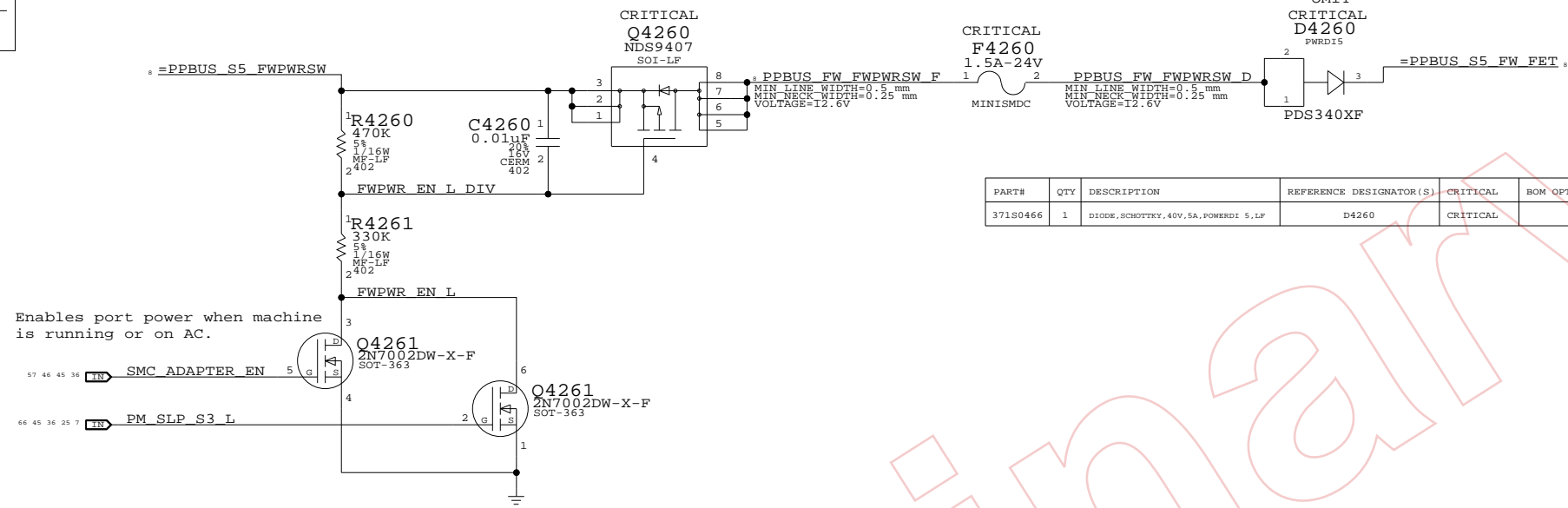
# Page Notes

Power aliases required by this page:  
 - =PPBUS\_S5\_FWPWRSW (system supply for bus power)  
 - =PP3V3\_FW\_LATEVG\_ACTIVE  
 - =PPVP\_FW\_SUMNODE (power passthru summation node)

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 - FW\_PORT\_FAULT\_PU

## FireWire Port Power Switch

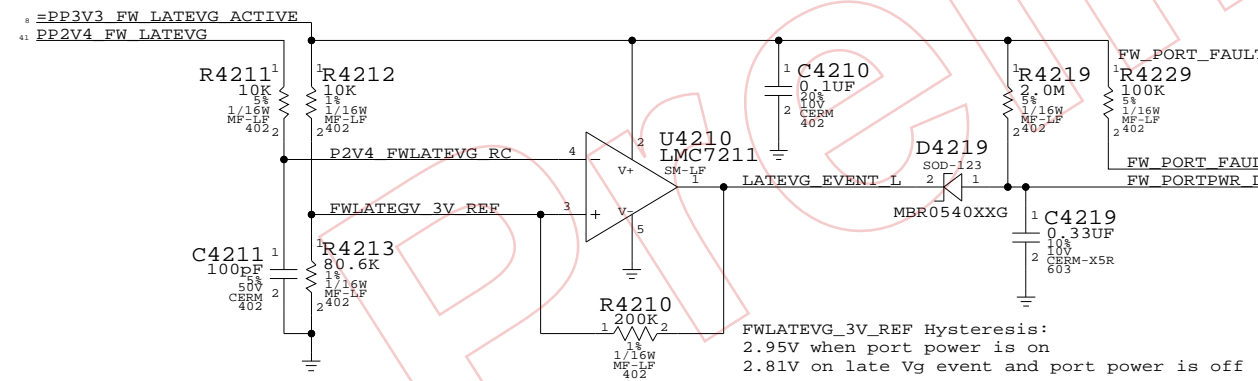


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
371S0466	1	DIODE,SCHOTTKY,40V,5A,POWERDI 5_LF	D4260	CRITICAL	

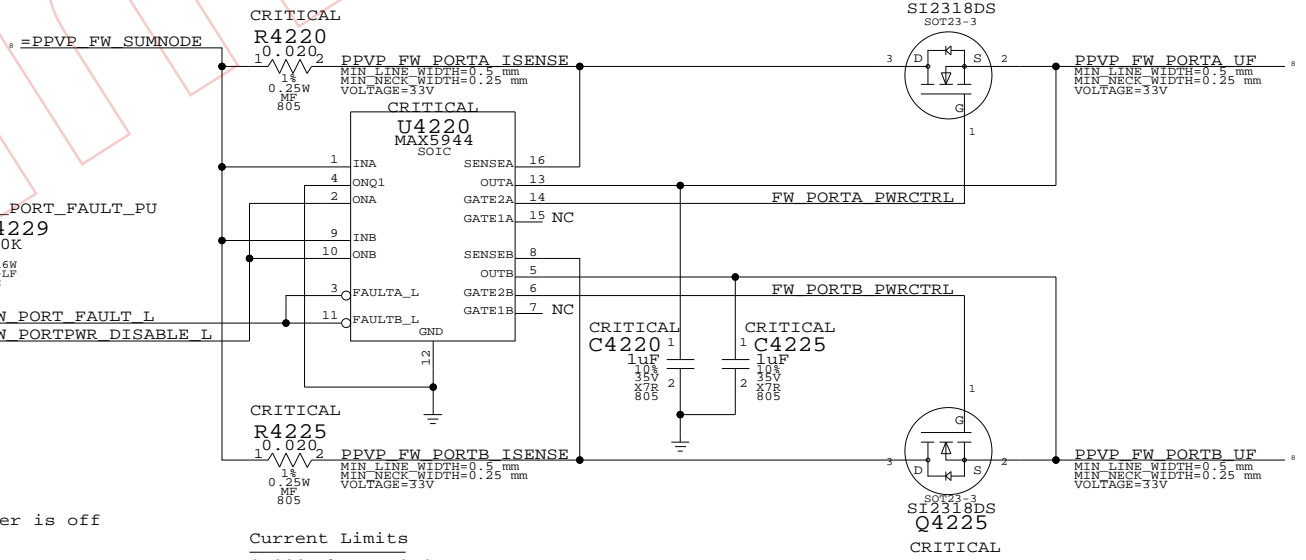
Enables port power when machine is running or on AC.

## Current Limit/Active Late-VG Protection

### Late-VG Event Detection



FWLATEGV\_3V\_REF Hysteresis:  
 2.95V when port power is on  
 2.81V on late Vg event and port power is off



Current Limits  
 0.020 ohm => 2.4A  
 0.025 ohm => 2A  
 0.030 ohm => 1.66A (Ideal)  
 0.033 ohm => 1.5A

MAX5944 current limiter trips if integrator (counter) reaches 16. A new sample (taken every 125 us) is weighted as +1 if over the limit (at any point during the period) and -1/128 if under the limit. As a result, the device tends to trip easily on devices that produce periodic current spikes. Current limit has been set higher to compensate.

### FireWire Port Power

SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/07/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	42	109	



# Page Notes

Power aliases required by this page:  
 - =PPVP\_FW\_PORT0  
 - =PPVP\_FW\_PORT1  
 - =PP3V3\_FW\_LATEVG  
 - =GND\_CHASSIS\_FW\_PORT0L  
 - =GND\_CHASSIS\_FW\_PORT0U  
 - =GND\_CHASSIS\_FW\_PORT1  
 - =GND\_CHASSIS\_FW\_EMI\_R

Signal aliases required by this page:  
 (NONE)

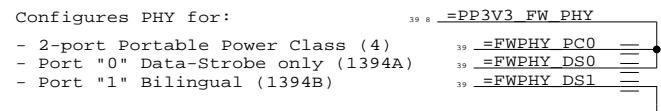
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:  
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

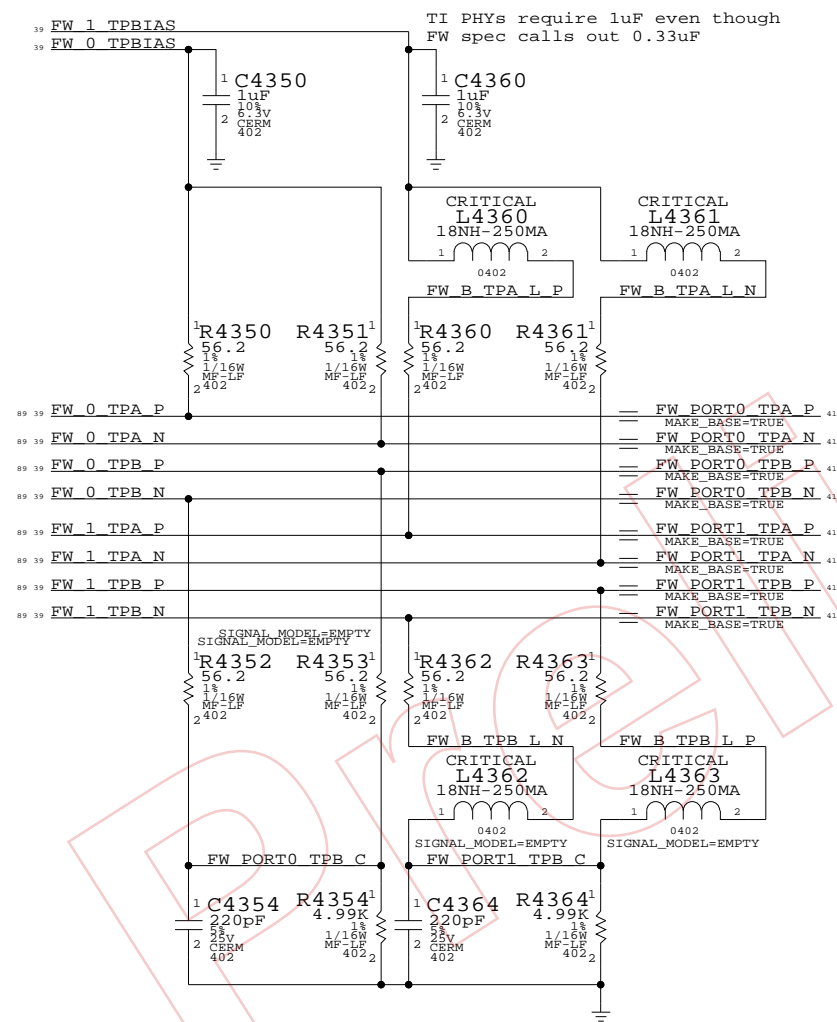
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

## FireWire PHY Config Straps

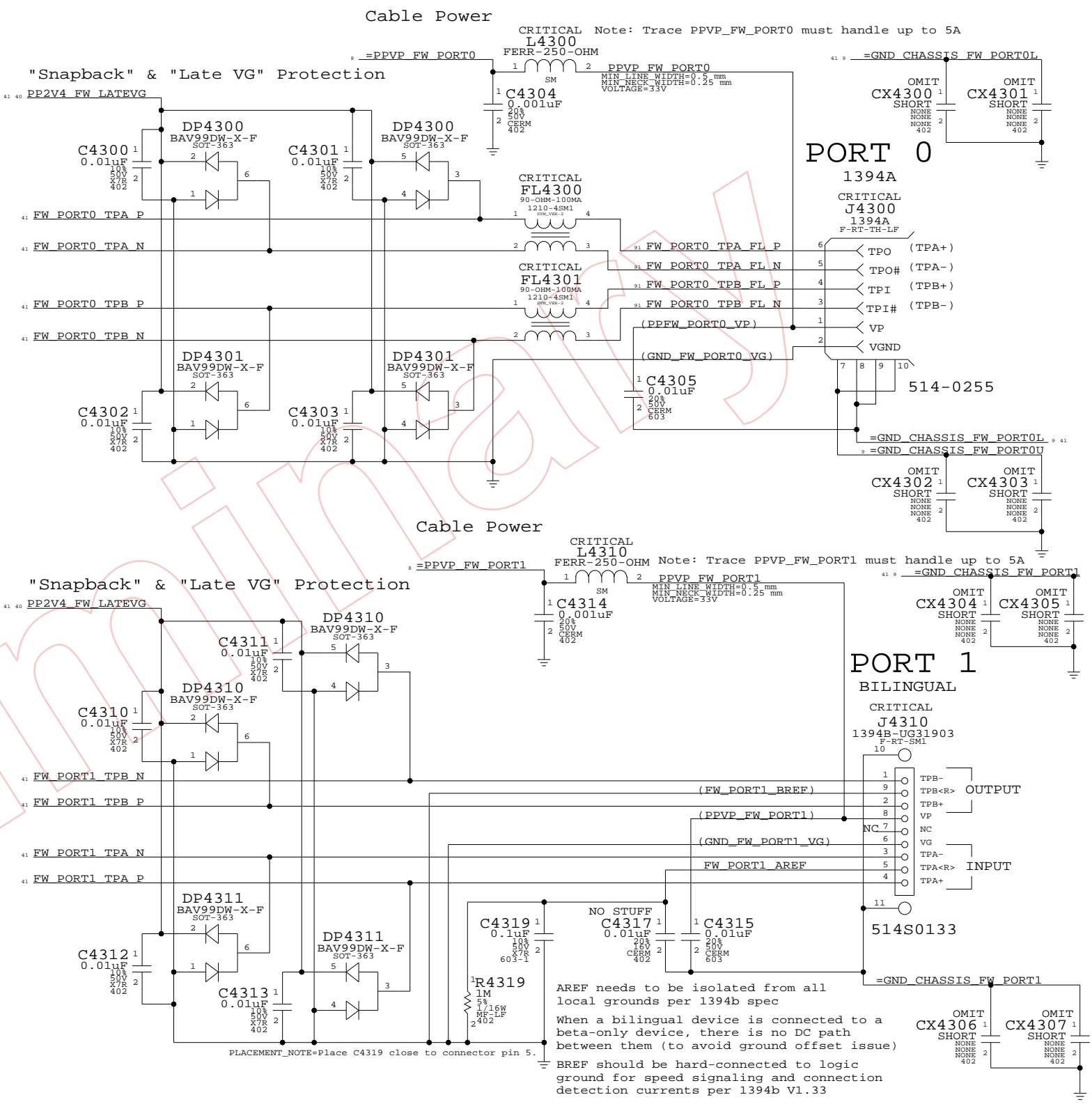
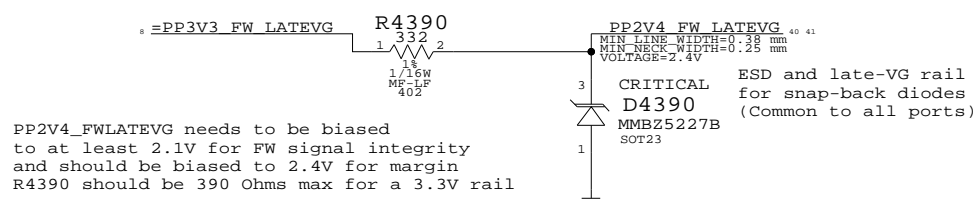


## Termination

Place close to FireWire PHY



## Late-VG Protection Power

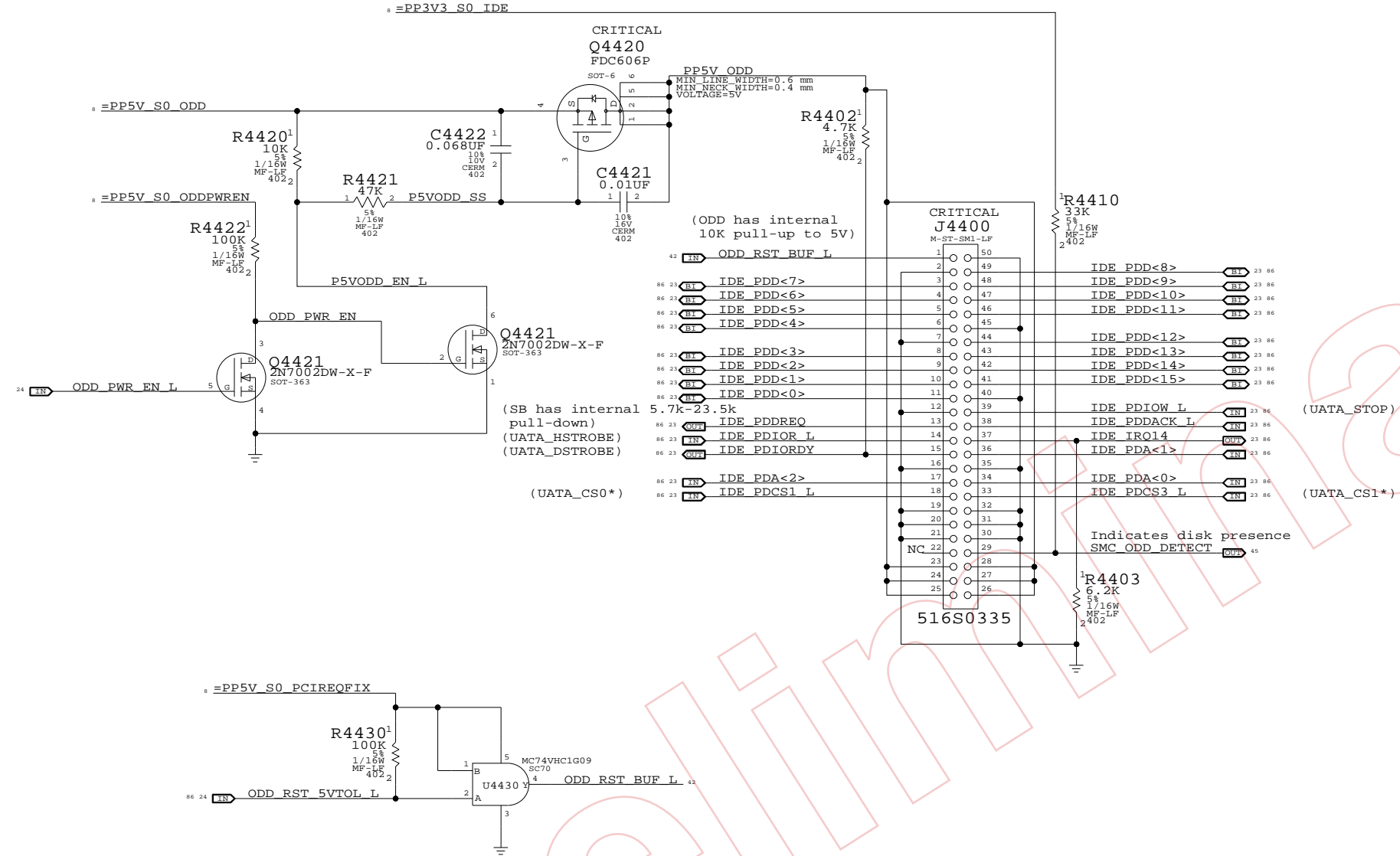


FireWire Ports		
SYNC_MASTER=M75_MLB	SYNC_DATE=12/04/2006	
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	109
NONE	43		

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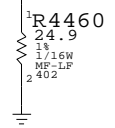
# IDE (ODD) Connector



## Unused SATA Ports

- 86 23 SATA B R2D C P == TP SATA B R2DP  
MAKE\_BASE=TRUE
- 86 23 SATA B R2D C N == TP SATA B R2DN  
MAKE\_BASE=TRUE
- 86 23 SATA B D2R P == TP SATA B D2RP  
MAKE\_BASE=TRUE
- 86 23 SATA B D2R N == TP SATA B D2RN  
MAKE\_BASE=TRUE
- 86 23 SATA C R2D C P == TP SATA C R2DP  
MAKE\_BASE=TRUE
- 86 23 SATA C R2D C N == TP SATA C R2DN  
MAKE\_BASE=TRUE
- 86 23 SATA C D2R P == TP SATA C D2RP  
MAKE\_BASE=TRUE
- 86 23 SATA C D2R N == TP SATA C D2RN  
MAKE\_BASE=TRUE
- 23 SATA RBIAS P == SATA RBIAS  
MAKE\_BASE=TRUE
- 23 SATA RBIAS N == SATA RBIAS  
MAKE\_BASE=TRUE

Placement note  
Place within 12.7mm  
from ball of SB

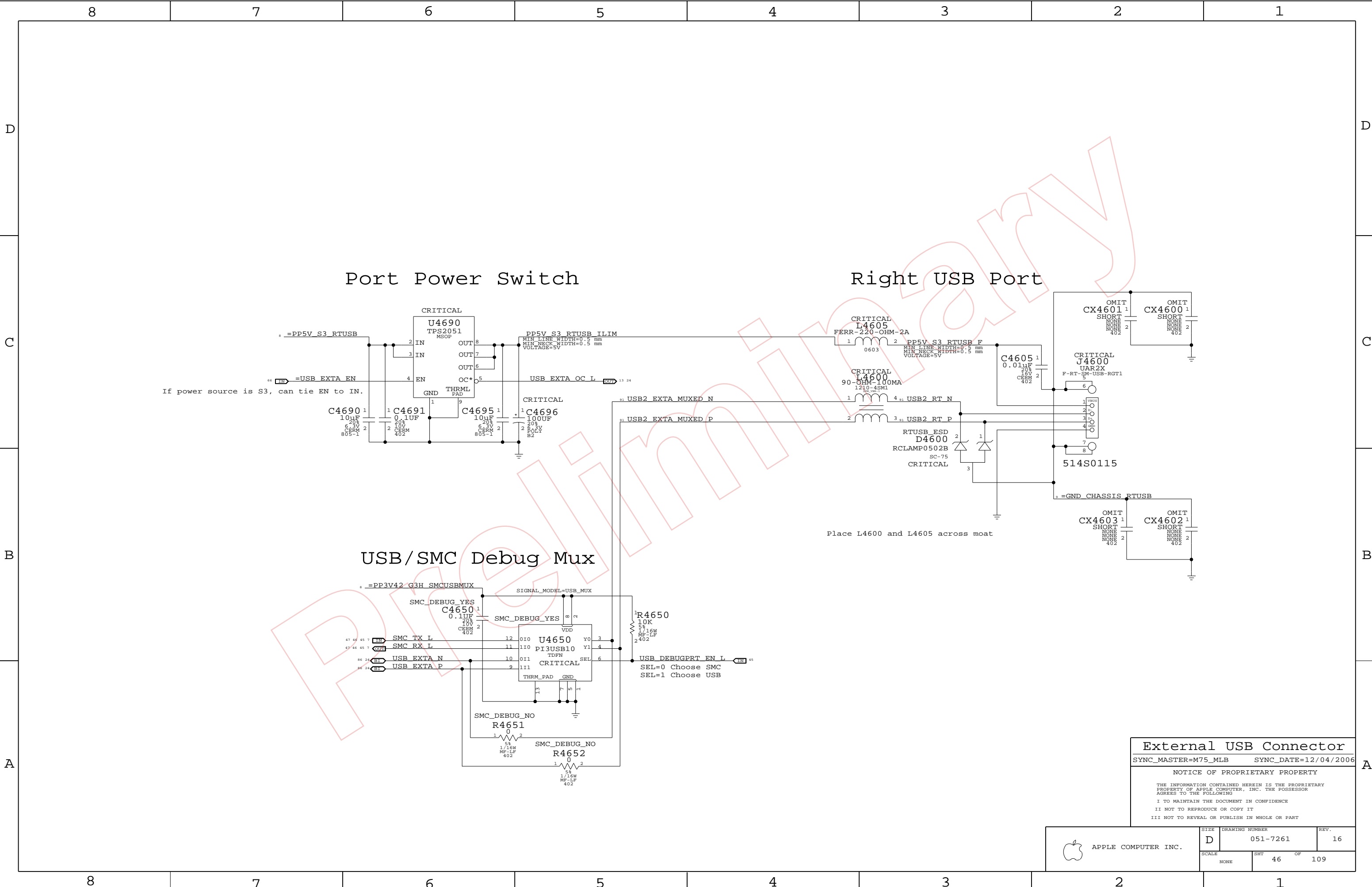


## PATA Connector

SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/07/2006

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	SCALE: NONE	SHT: 44	OF: 109



If power source is S3, can tie EN to IN.

Place L4600 and L4605 across moat

**External USB Connector**

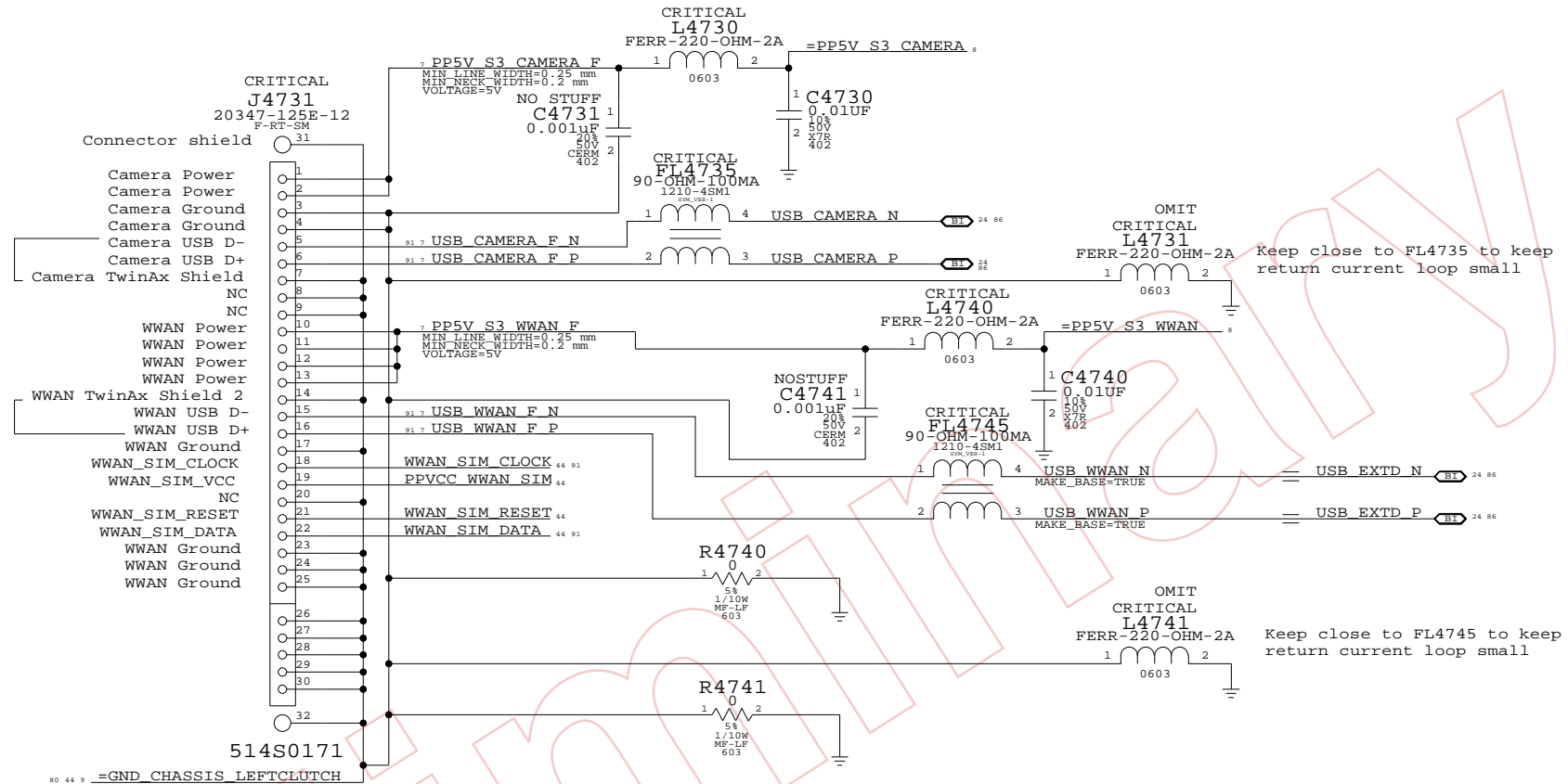
SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006

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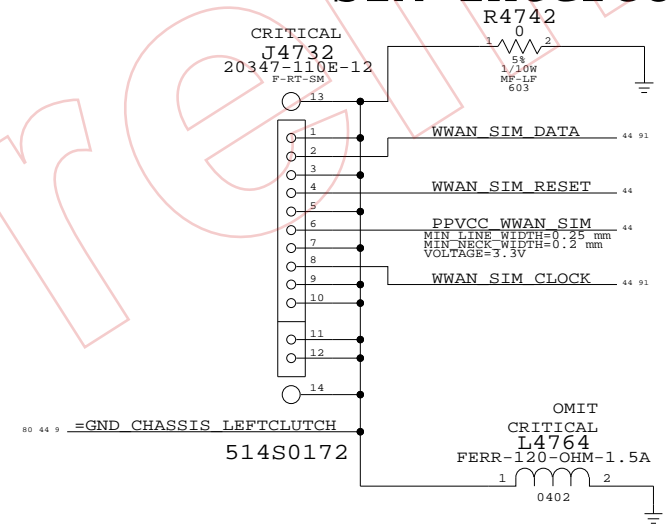
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT		OF
NONE	46		109

# Left Clutch Barrel Interconnect



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
113S0022	2	RES, MF, 1/10W, 00HM, 5, 0603, SM, LF	L4731, L4741	CRITICAL	
116S0004	1	RES, MF, 1/16W, 00HM, 5, 0402, SM, LF	L4764	CRITICAL	

## SIM Interconnect



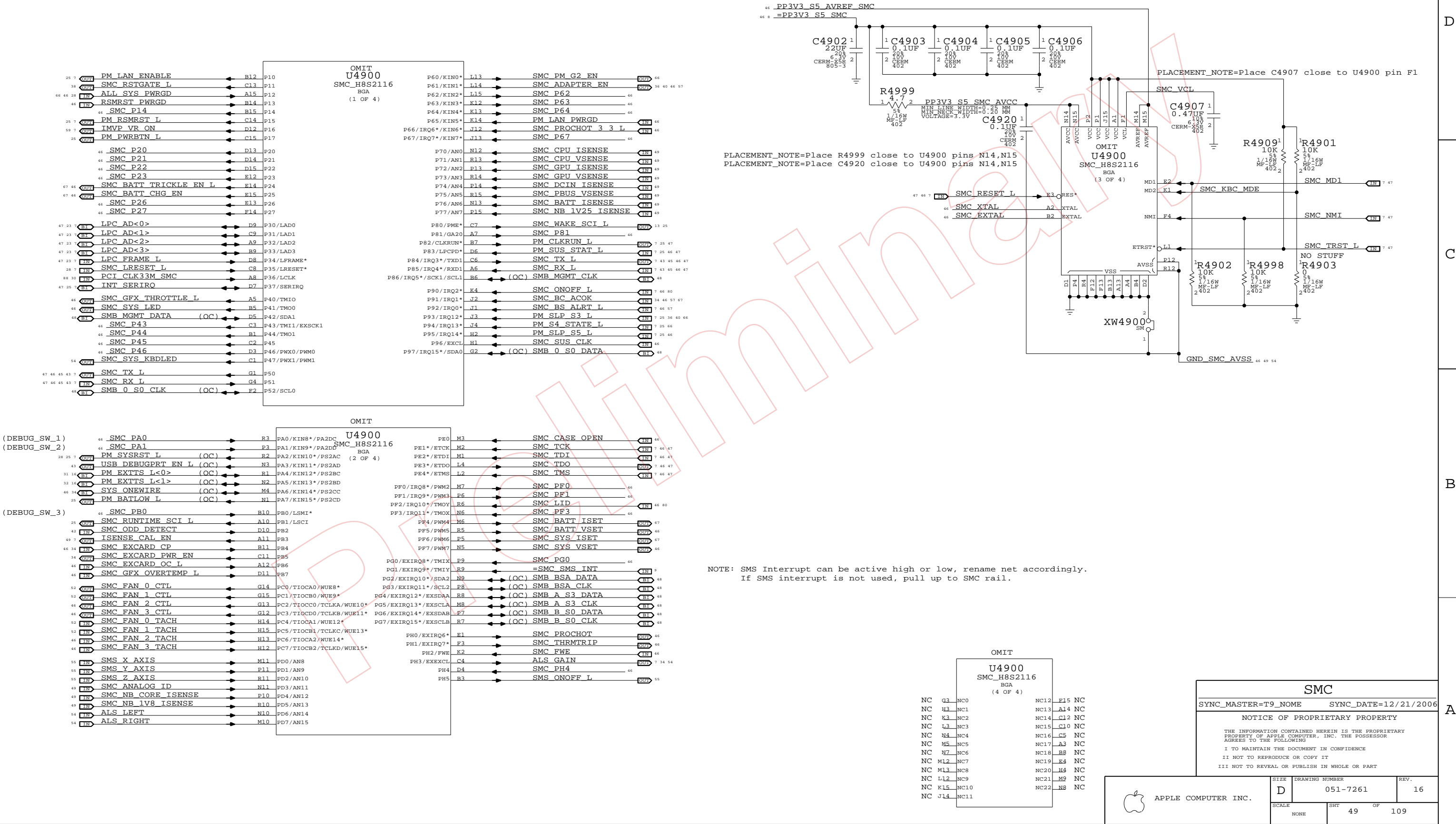
Left Clutch Barrel Interconnect  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/21/2006

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	D	051-7261	16
SCALE		SHT	OF
NONE		47	109



NOTE: Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



PLACEMENT\_NOTE=Place R4999 close to U4900 pins N14,N15  
 PLACEMENT\_NOTE=Place C4920 close to U4900 pins N14,N15

PLACEMENT\_NOTE=Place C4907 close to U4900 pin F1

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

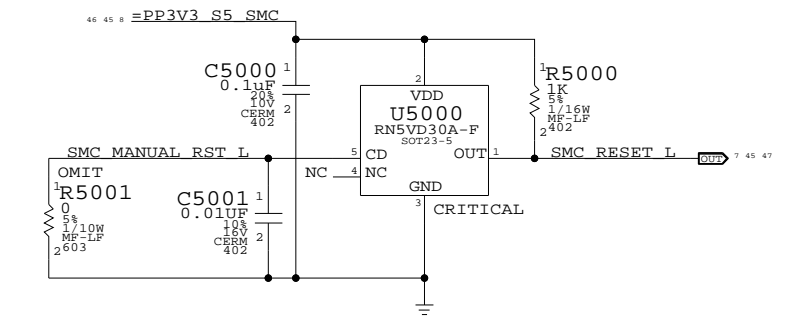
NC G3 NC0		NC12 E15 NC	
NC H3 NC1	NC13 A14 NC	NC14 C12 NC	
NC K3 NC2	NC15 C10 NC	NC16 C5 NC	
NC L3 NC3	NC17 A3 NC	NC18 BB NC	
NC M4 NC4	NC19 E4 NC	NC20 H4 NC	
NC N5 NC5	NC21 M9 NC	NC22 NB NC	
NC N7 NC6			
NC ML2 NC7			
NC ML3 NC8			
NC L12 NC9			
NC K15 NC10			
NC J14 NC11			

SMC  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=12/21/2006  
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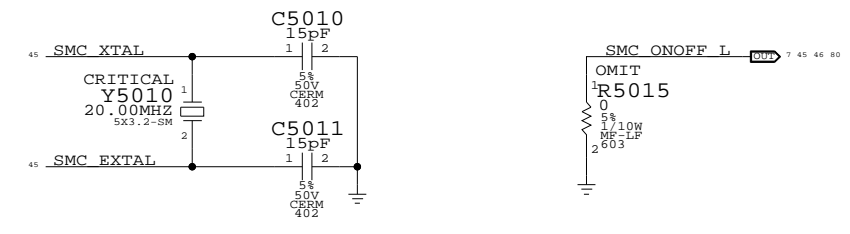
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	49	109	

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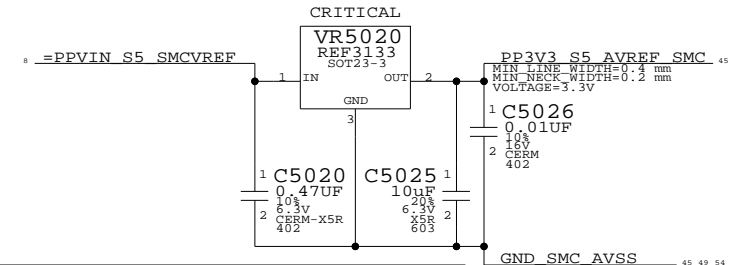
### SMC Reset "Button" / Brownout Detect



### SMC Crystal Circuit Debug Power "Button"

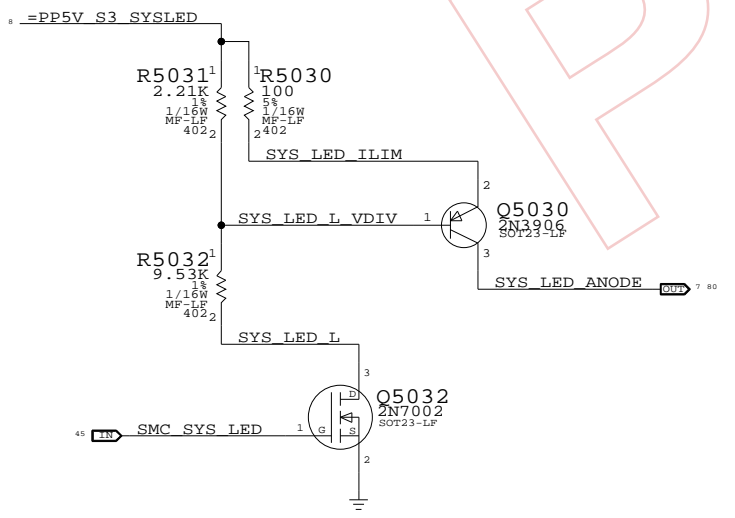


### SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Interail ISL60002-33

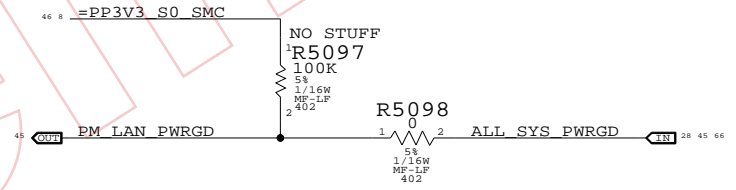
### System (Sleep) LED Circuit



- SMC\_FAN\_2\_CTL == TP\_SMC\_FAN\_2\_CTL
- SMC\_FAN\_2\_TACH == TP\_SMC\_FAN\_2\_TACH
- SMC\_FAN\_3\_CTL == TP\_SMC\_FAN\_3\_CTL
- SMC\_FAN\_3\_TACH == TP\_SMC\_FAN\_3\_TACH
- SMC\_GFX\_OVERTEMP\_L == TP\_SMC\_GFX\_OVERTEMP\_L
- SMC\_GFX\_THROTTLE\_L == TP\_SMC\_GFX\_THROTTLE\_L
- SMC\_BATT\_VSET == TP\_SMC\_BATT\_VSET
- SMC\_SYS\_VSET == TP\_SMC\_SYS\_VSET
- SMC\_P14 == TP\_SMC\_P14
- SMC\_P20 == TP\_SMC\_P20
- SMC\_P21 == TP\_SMC\_P21
- SMC\_P22 == TP\_SMC\_P22
- SMC\_P23 == TP\_SMC\_P23
- SMC\_P26 == TP\_SMC\_P26
- SMC\_P27 == TP\_SMC\_P27
- SMC\_P43 == TP\_SMC\_P43
- SMC\_P44 == TP\_SMC\_P44
- SMC\_P46 == TP\_SMC\_P46
- SMC\_P62 == TP\_SMC\_P62
- SMC\_P63 == TP\_SMC\_P63
- SMC\_P64 == TP\_SMC\_P64
- SMC\_P81 == TP\_SMC\_P81
- SMC\_PFO == TP\_SMC\_PFO
- SMC\_PF1 == TP\_SMC\_PF1

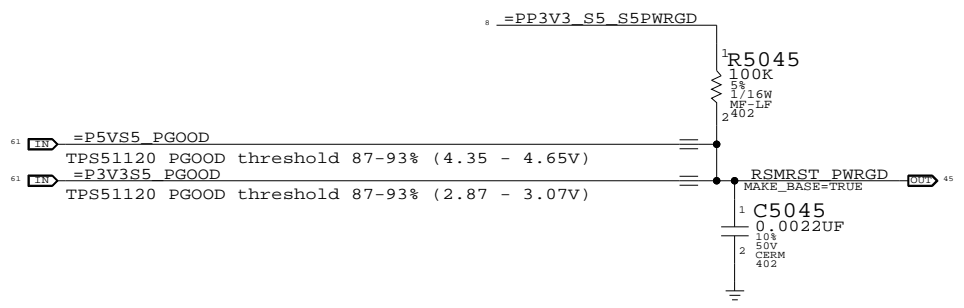
- SMC\_EXCARD\_OC\_L == EXCARD\_OC\_L
- SMC\_SUS\_CLK == SUS\_CLK\_SB
- SMC\_P45 == SMC\_ENRGYSTR\_LDO\_EN

### LAN PWRGD Circuit

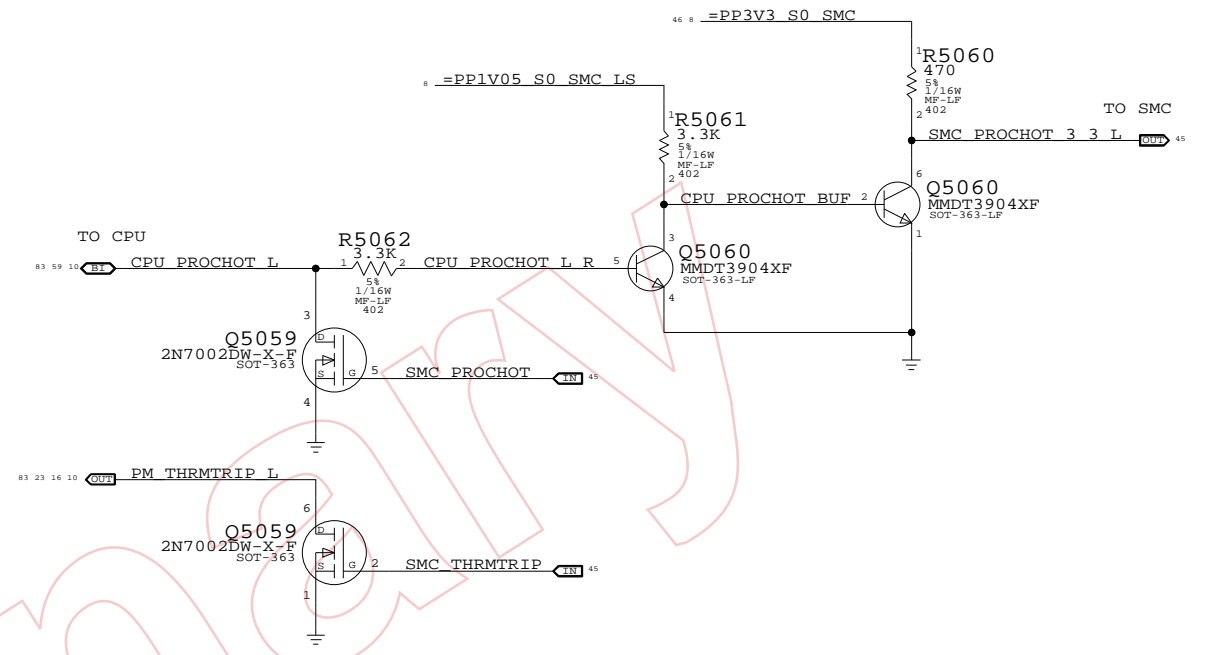


### S5 Rail PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



### SMC FSB to 3.3V Level Shifting

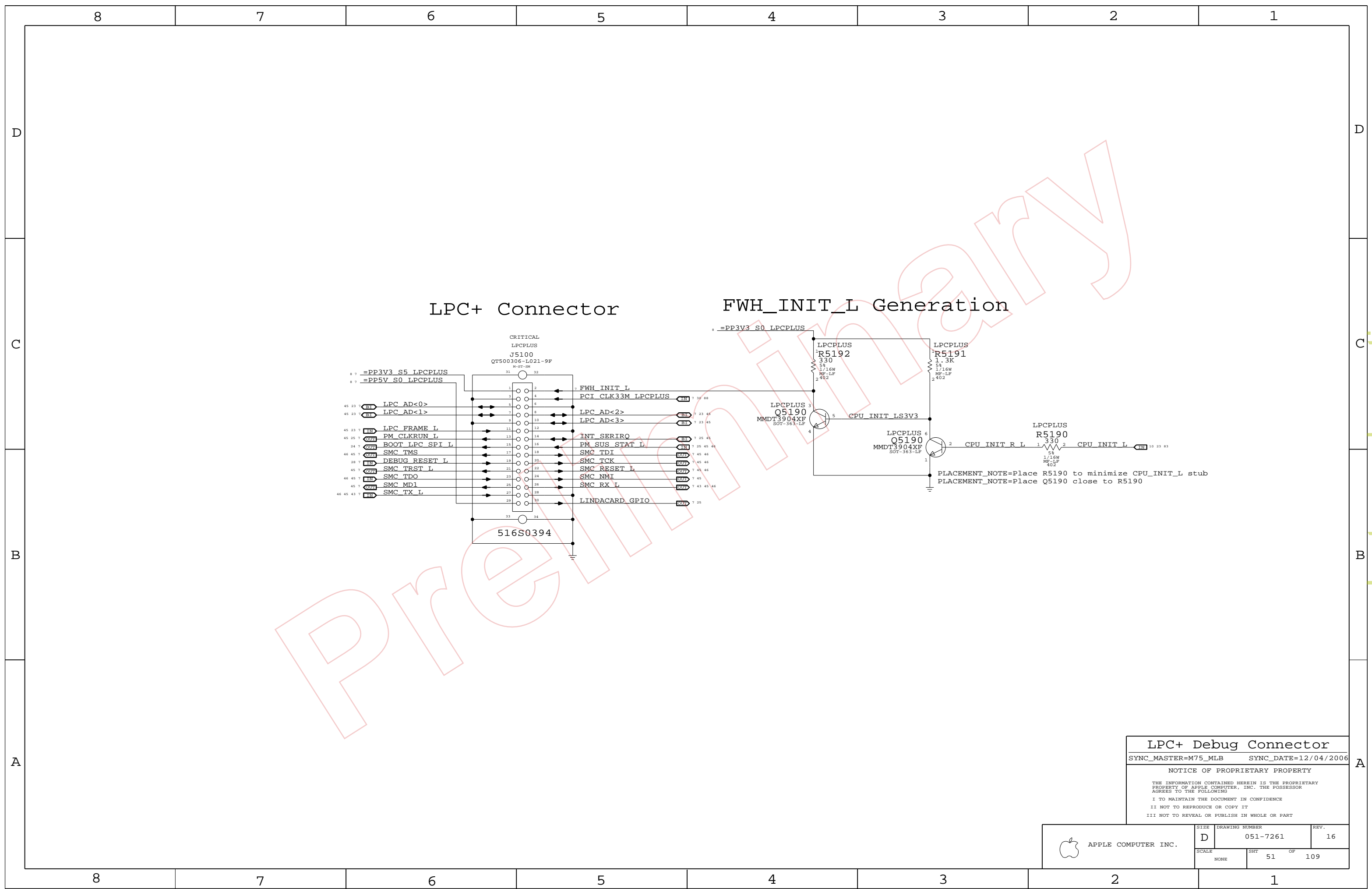


- SMC\_PA0 == R5091 100K
- SMC\_PA1 == R5092 100K
- SMC\_PB0 == R5093 100K
- SMC\_ONOFF\_L == R5070 10K
- SMC\_LID == R5071 100K
- SMC\_FWE == R5072 10K
- SMC\_TX\_L == R5073 10K
- SMC\_RX\_L == R5074 10K
- SMC\_P67 == R5094 10K
- SMC\_P63 == R5081 10K
- SMC\_PG0 == R5096 10K
- SMC\_PH4 == R5082 10K
- SMC\_BATT\_TRICKLE\_EN\_L == R5083 10K
- SMC\_BATT\_CHG\_EN == R5084 10K
- SMC\_ADAPTER\_EN == R5085 10K
- SMC\_CASE\_OPEN == R5086 10K
- SMC\_BC\_ACOK == R5087 470K
- SMC\_EXCARD\_CP == R5088 10K
- PM\_SUS\_STAT\_L == R5089 100K
- PM\_SLP\_S5\_L == R5090 100K

SMC Support  
SYNC\_MASTER=M75\_MLB SYNC\_DATE=04/02/2007

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	D	051-7261	16
SCALE	SHT	OF	
NONE	50	109	



LPC+ Connector

FWH\_INIT\_L Generation

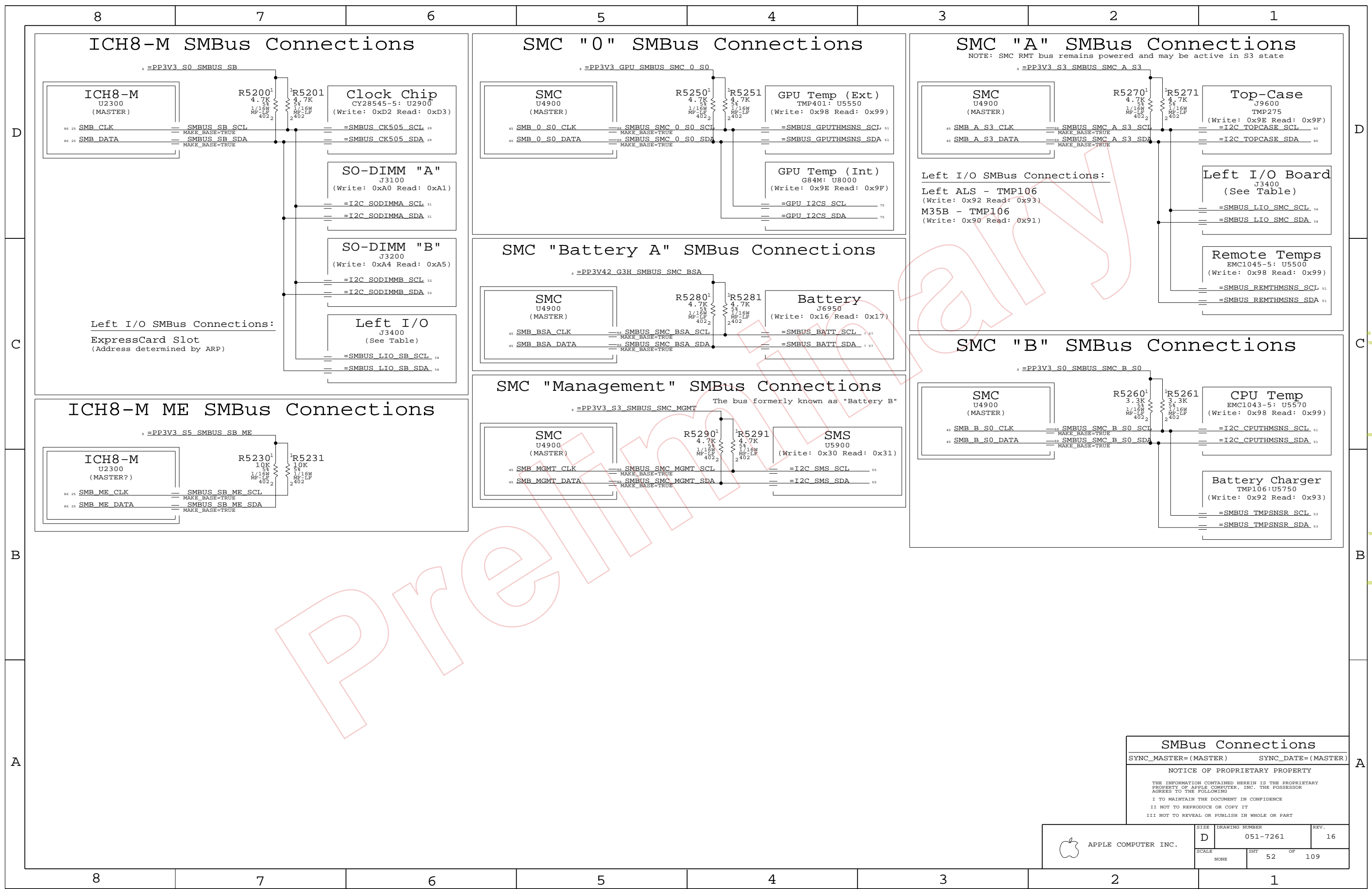
LPC+ Debug Connector

SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006

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	D	051-7261	16
SCALE	SHT	OF	
NONE	51	109	



**SMBus Connections**

SYNC\_MASTER=(MASTER)      SYNC\_DATE=(MASTER)

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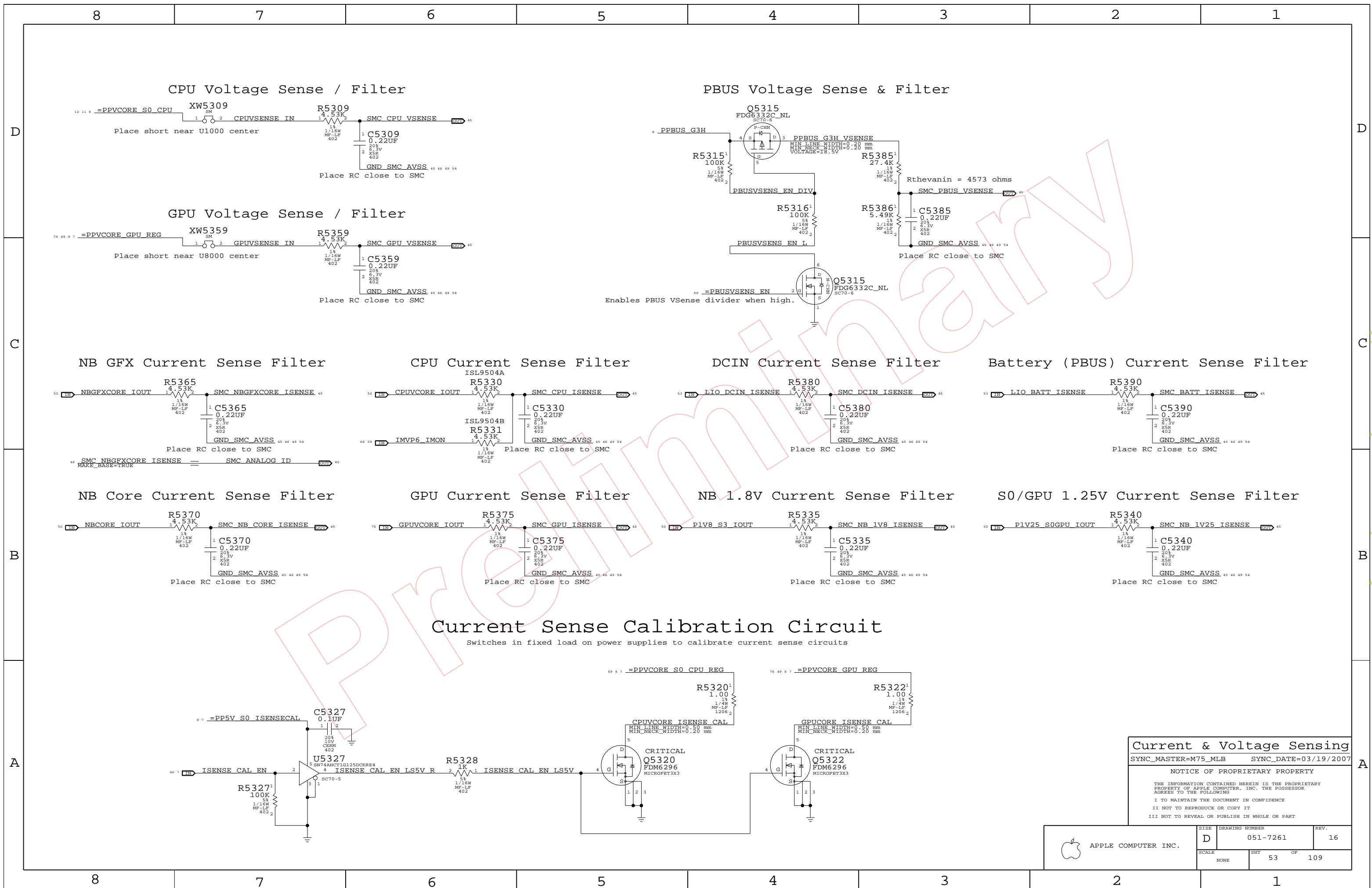
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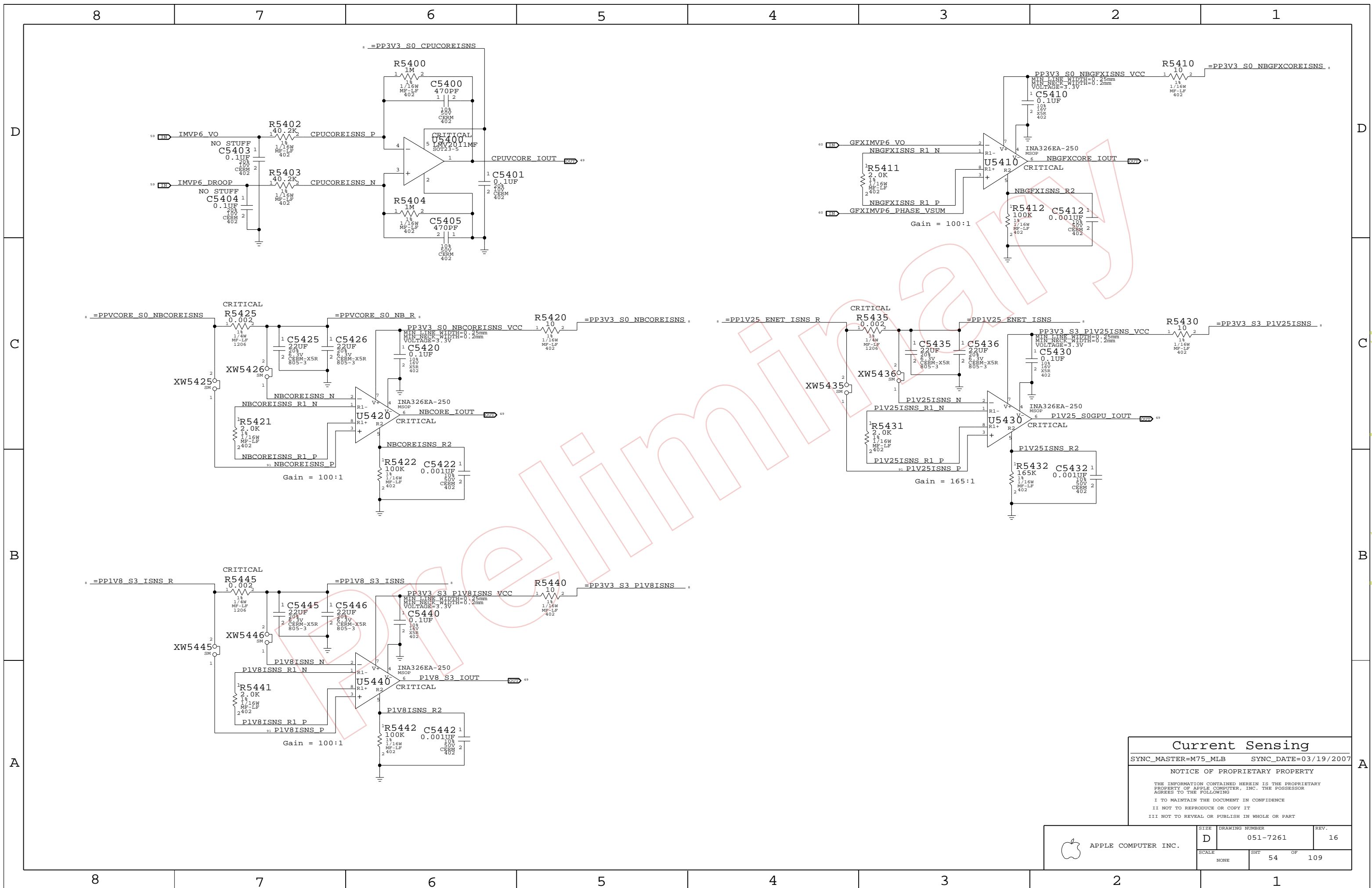
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

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	D	051-7261	16
SCALE	SHT	OF	REV.
NONE	52	109	





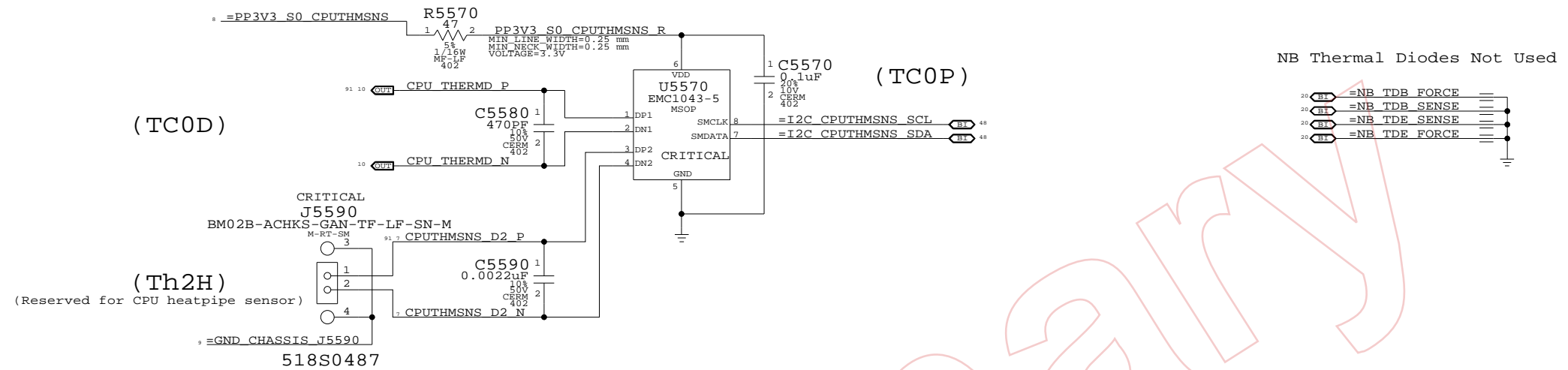
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	53	109	



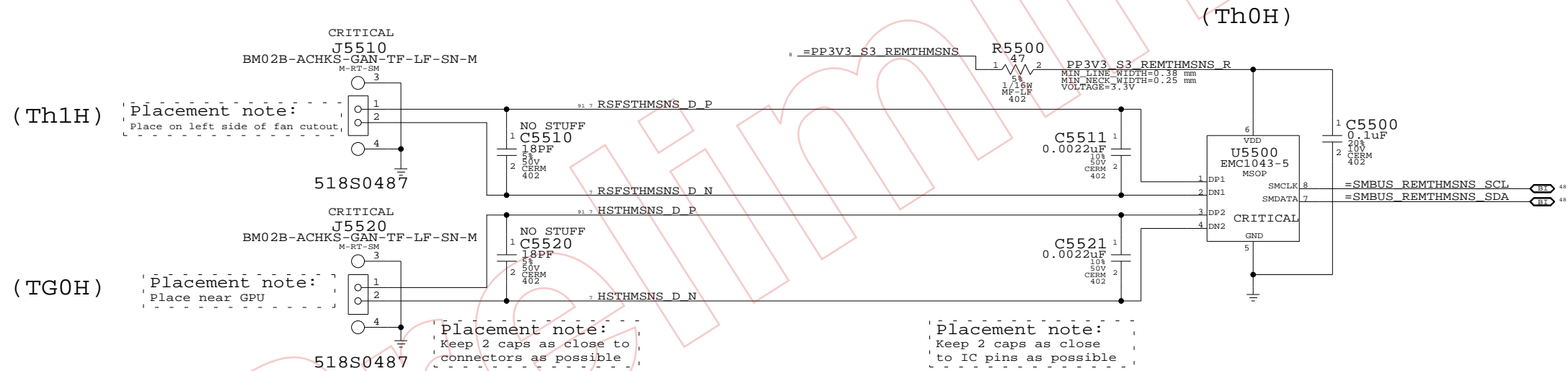
**Current Sensing**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007  
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	D	051-7261	16
SCALE	SHT	OF	
NONE	54	109	

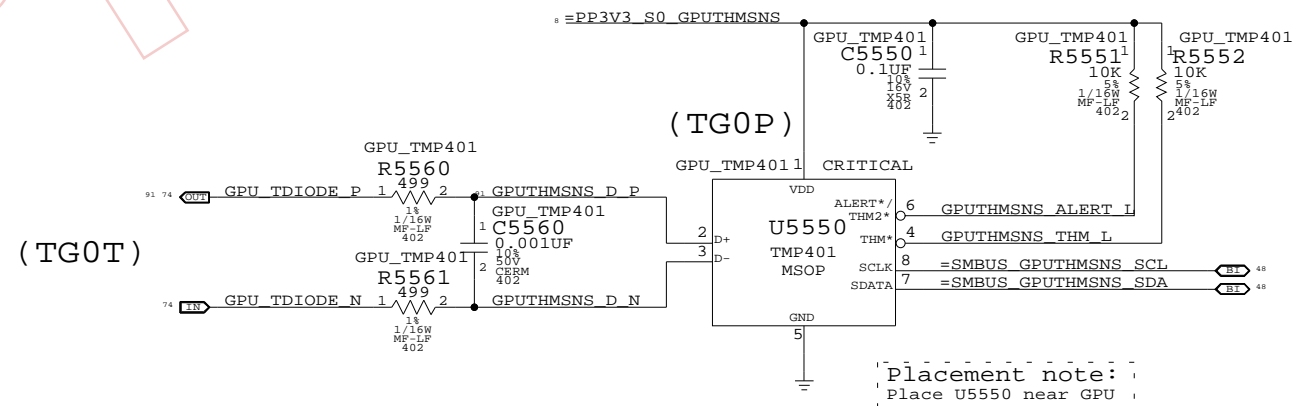
# CPU T-Diode Thermal Sensor



# GPU/Heat Pipe & Bottom Case Skin Thermal Sensor

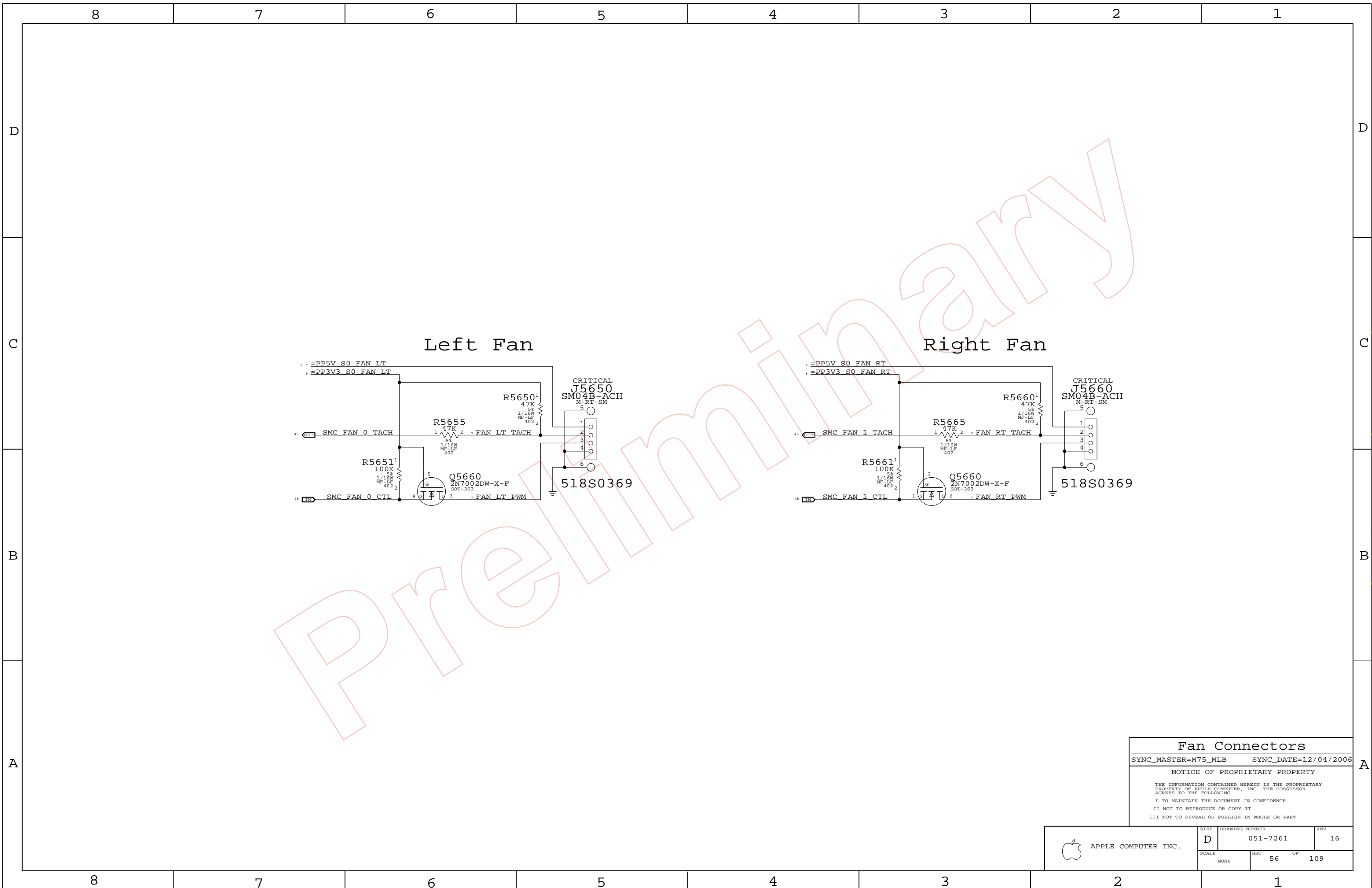


# GPU Die Thermal Sensor



Thermal Sensors		
SYNC_MASTER=M75_MLB	SYNC_DATE=03/19/2007	
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SCALE	SHT	OF	
NONE	55	109	



**Fan Connectors**

SYNC\_MASTER=M75\_MLB      SYNC\_DATE=12/04/2006

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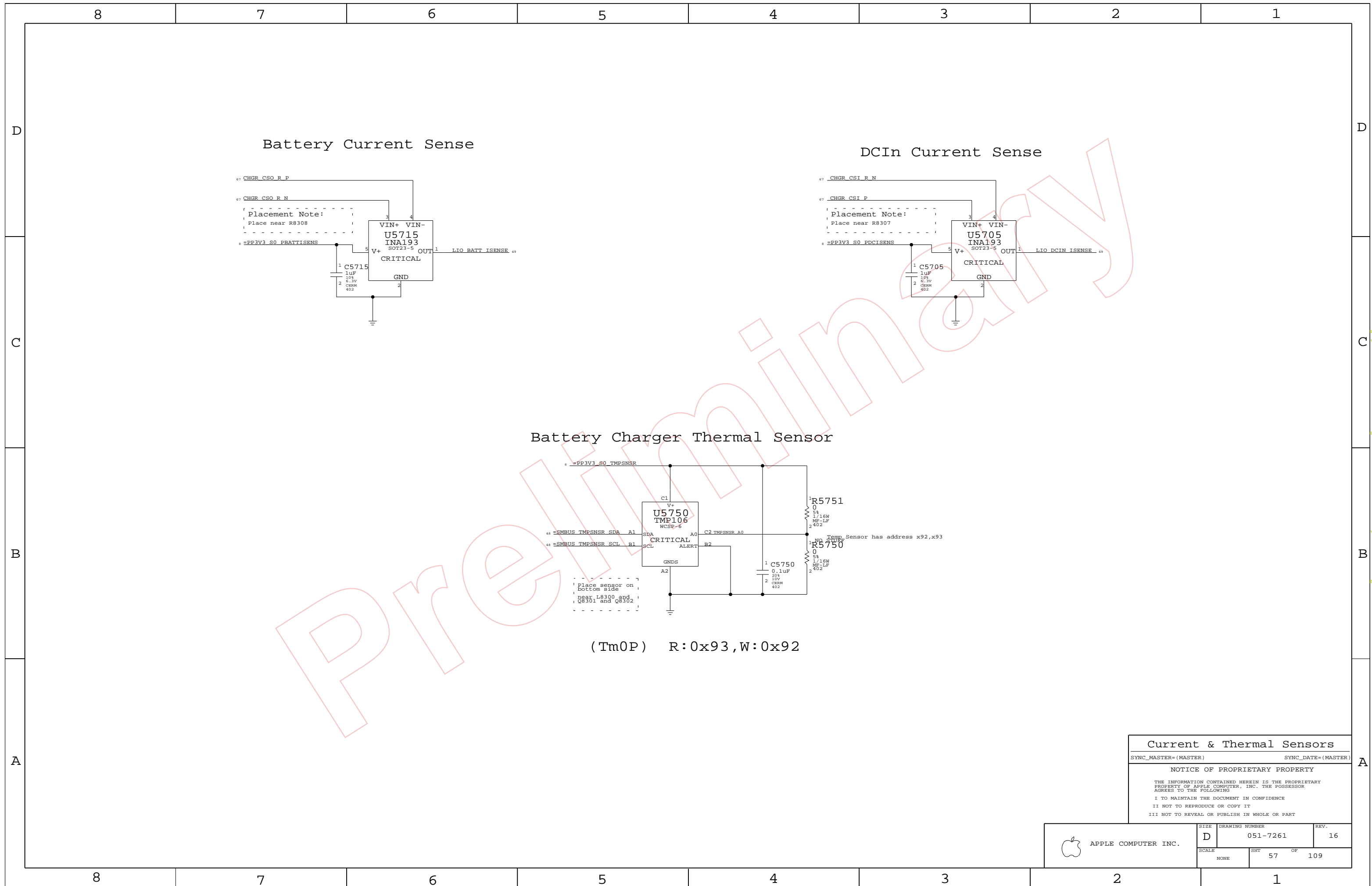
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II NOT TO REPRODUCE OR COPY IT

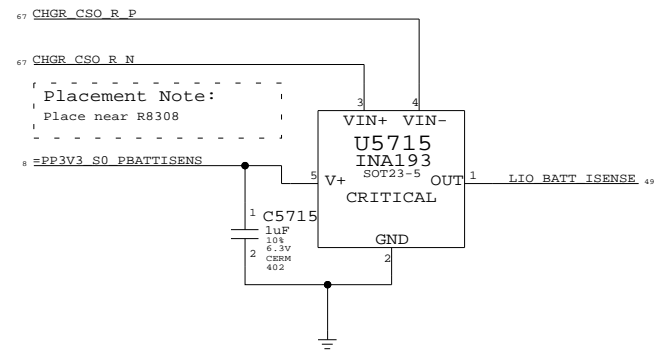
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHT 56	OF 109

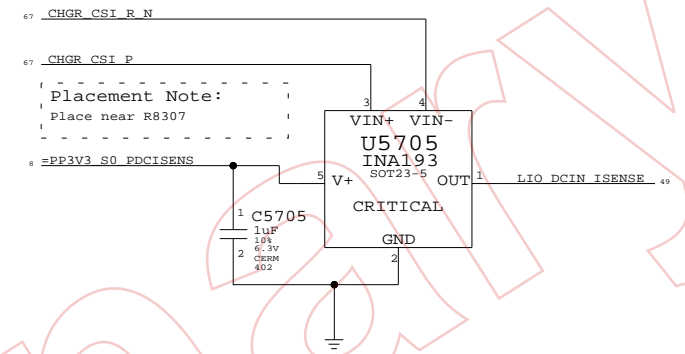




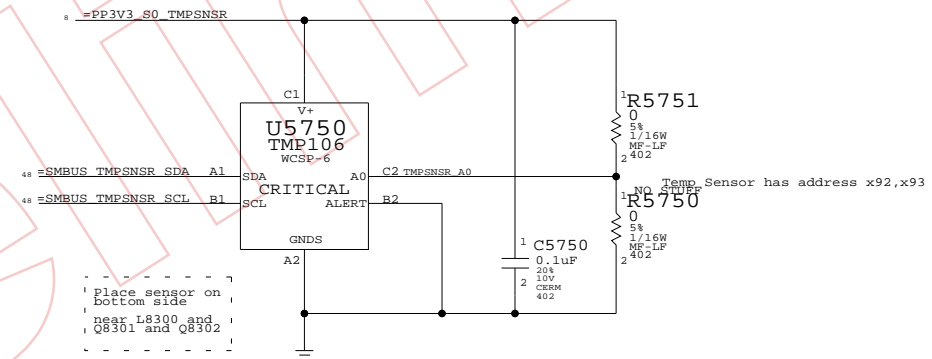
Battery Current Sense



DCIn Current Sense



Battery Charger Thermal Sensor



(Tm0P) R:0x93,W:0x92

Current & Thermal Sensors

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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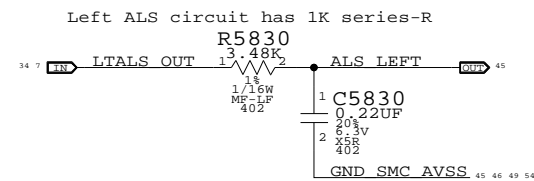
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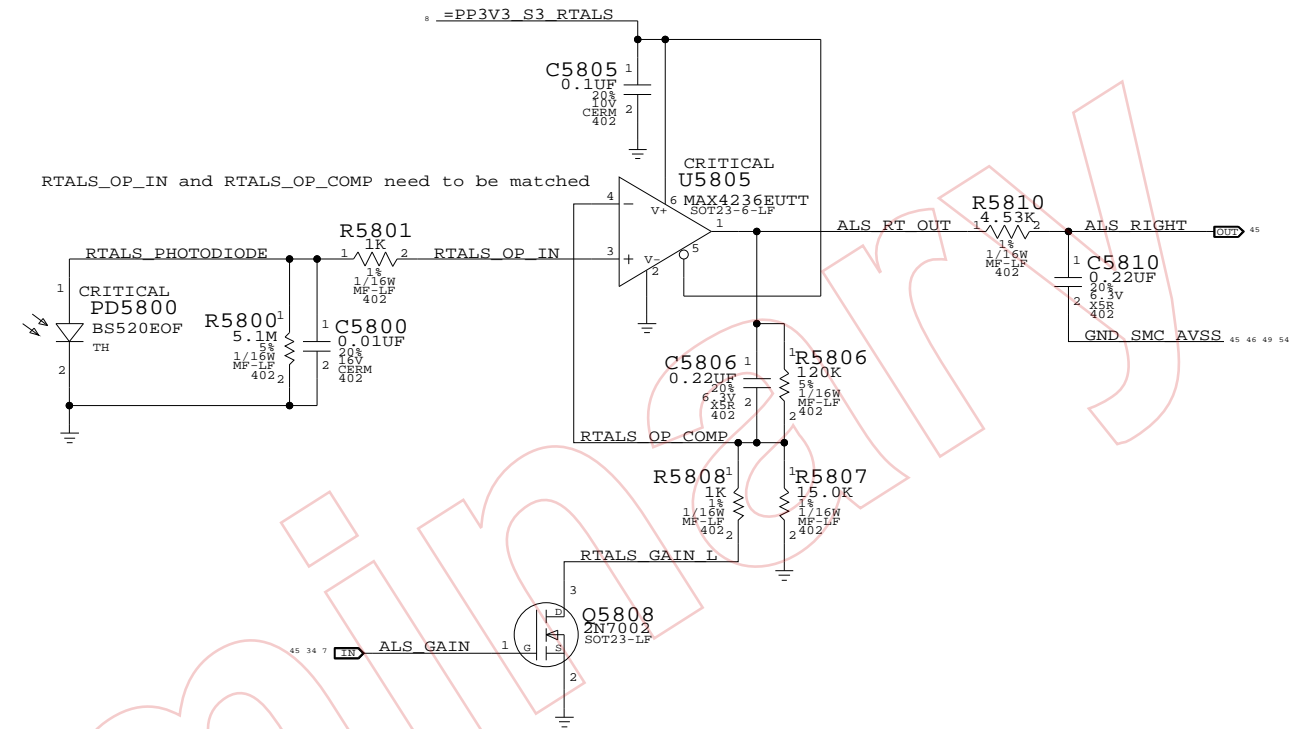
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	REV.
NONE	57	109	

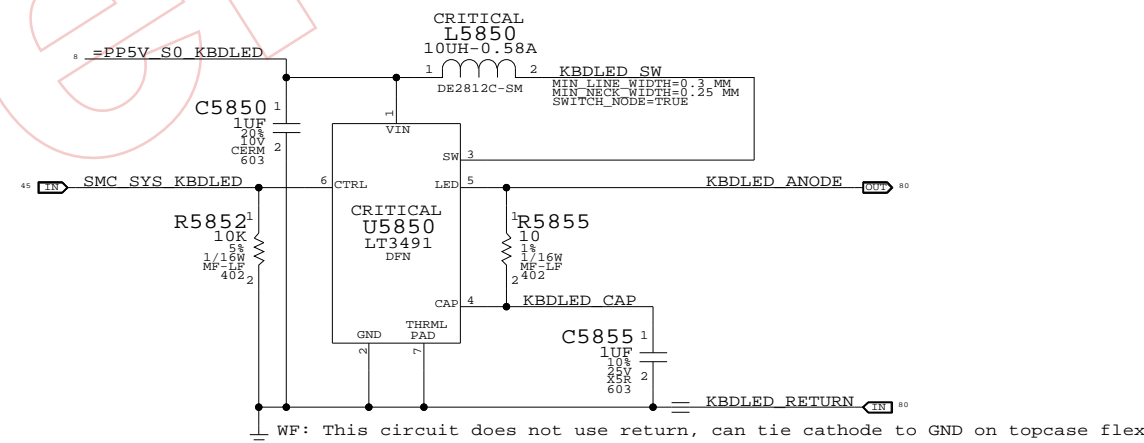
### Left ALS Filter



### Right ALS Circuit

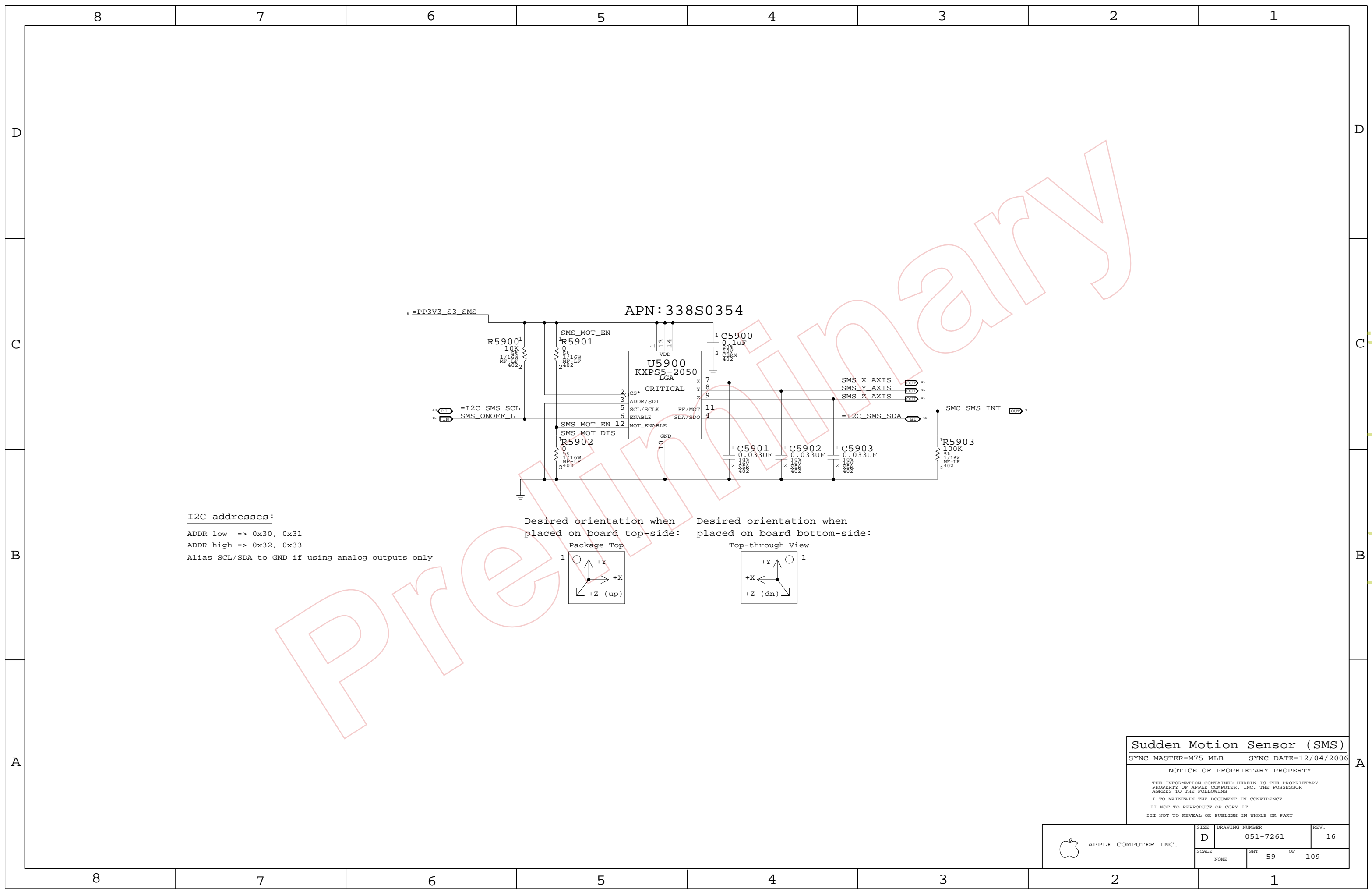


### Keyboard LED Driver



**ALS Support**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	REV.
NONE	58	109	



PREVIEW


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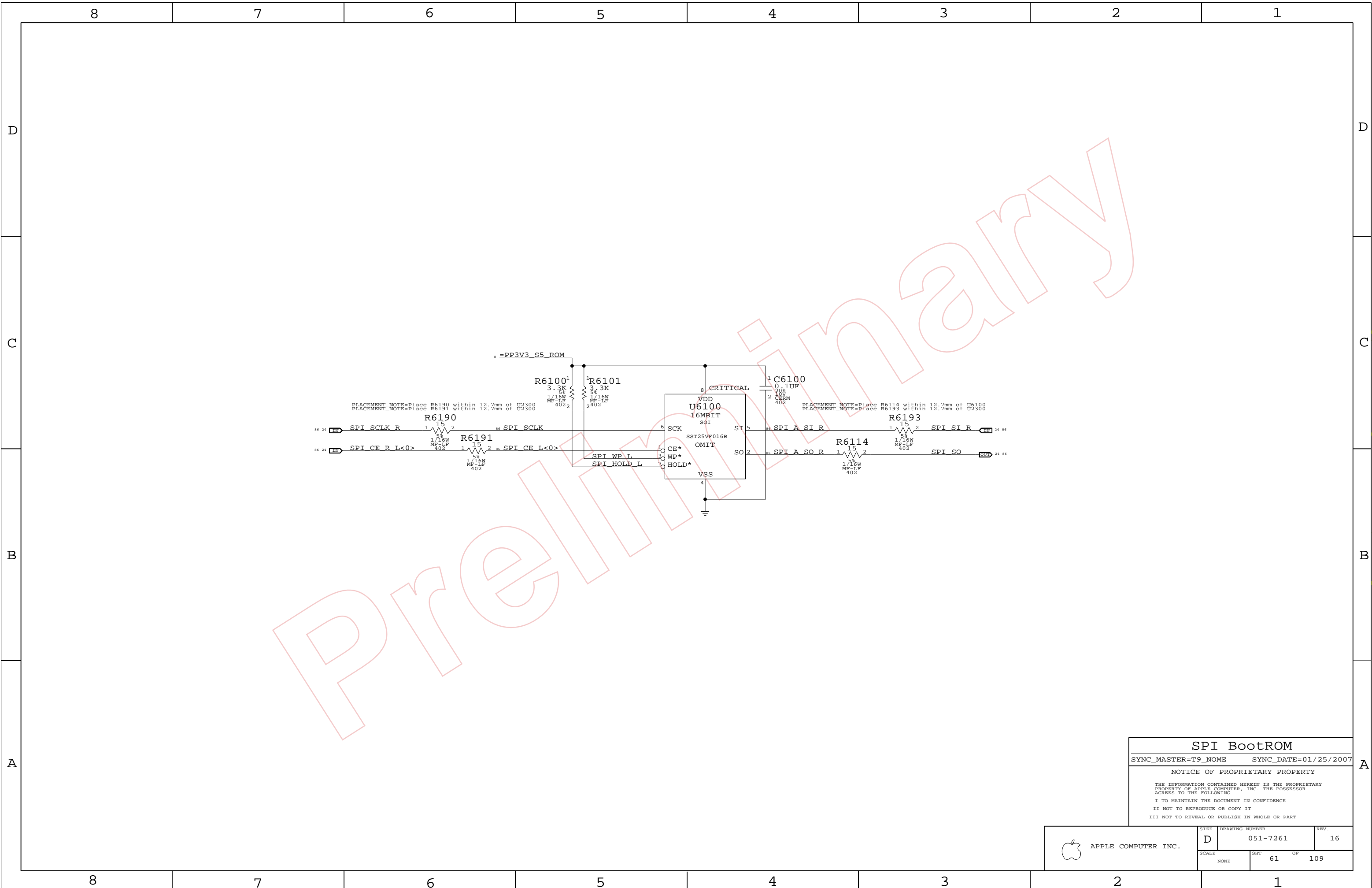
**Sudden Motion Sensor (SMS)**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006

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SCALE	SHT	OF	
NONE	59	109	



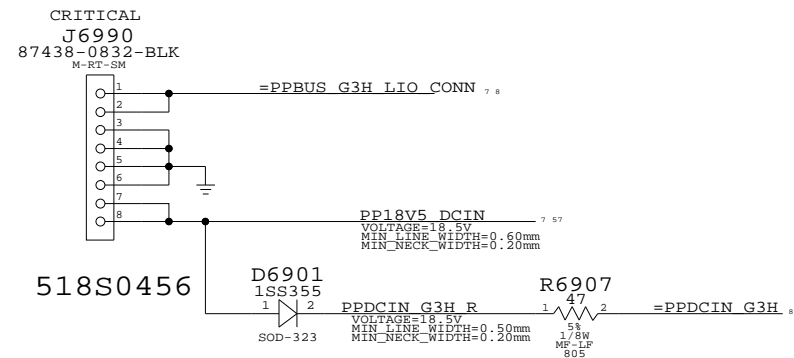
Preliminary

**SPI BootROM**  
 SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007  
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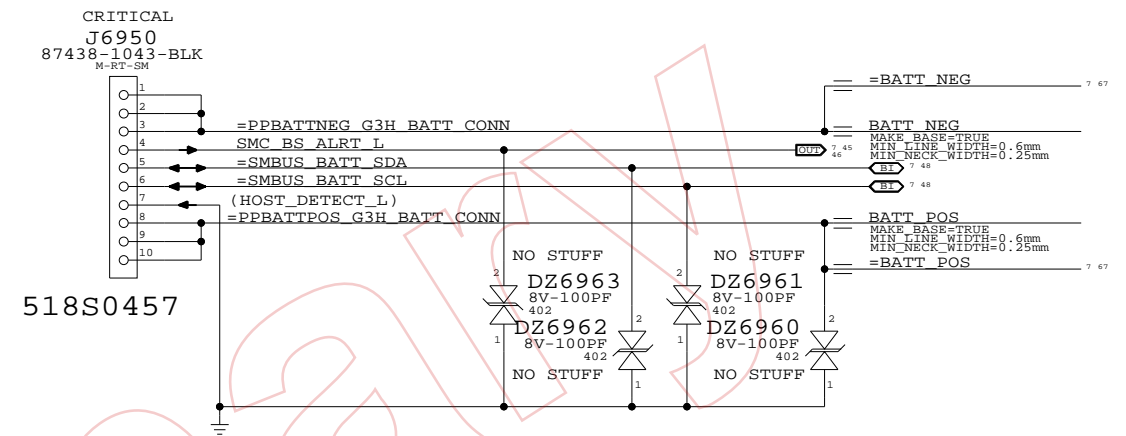
APPLE COMPUTER INC.	SIZE <b>D</b>	DRAWING NUMBER 051-7261	REV. 16
	SCALE NONE	SHEET 61	OF 109



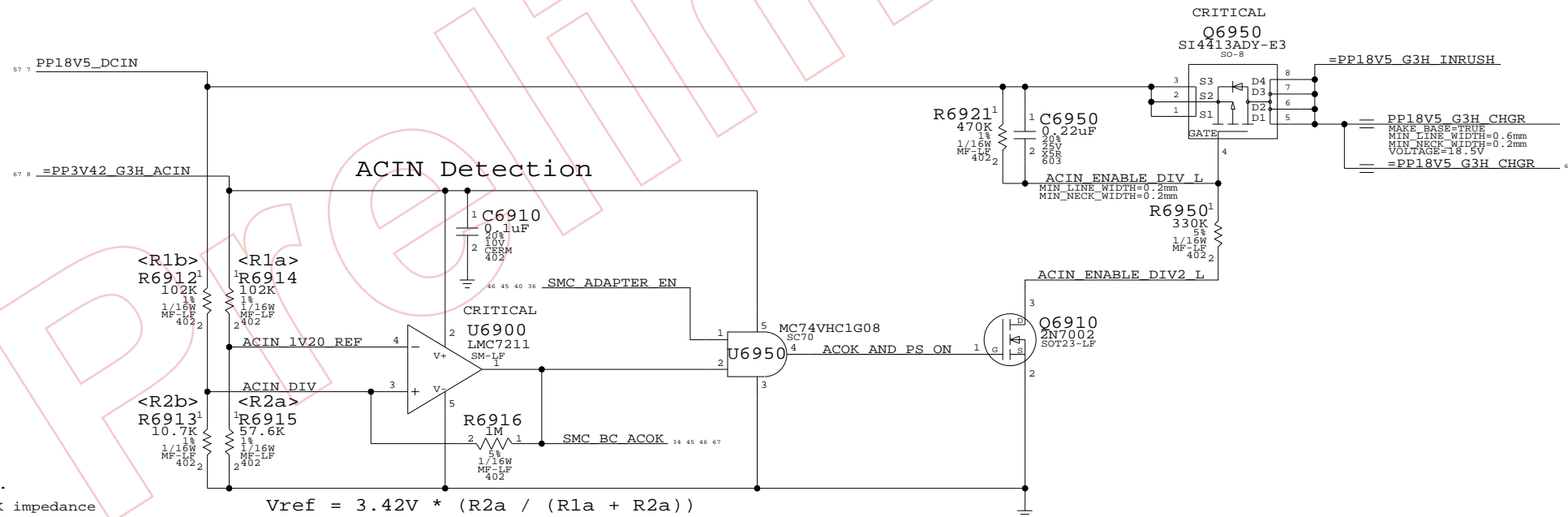
## DC-In Connector



## Battery Connector



## Inrush Limiter



NOTE: R6910 is on LIO.  
System must provide 10K-70K impedance to A52 adapter for system load detection.  
REQ of R6910 (on LIO), R6912, & R6913 is 36.9K.

$$V_{ref} = 3.42V * (R2a / (R1a + R2a))$$

$$V_{th} = (V_{ref} / (R2b / (R1b + R2b)))$$

$$V_{ref} = 1.23V$$

$$V_{th} = 13.0V$$

Assuming 1% variance for R6910-R6915 and 3.42V:  
Worst case Vth: min:12.47V, max: 13.54V

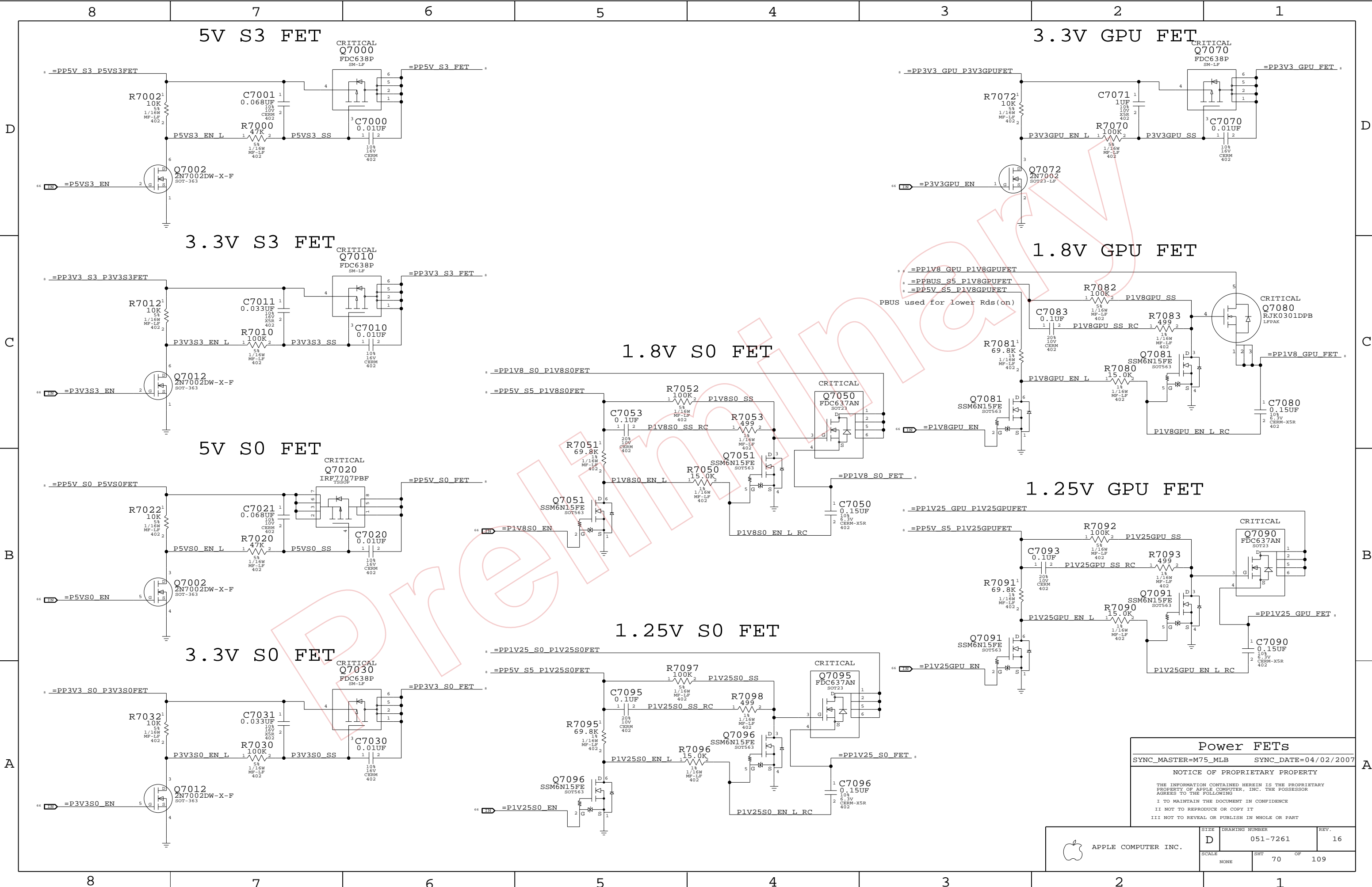
### DC-In & Battery Connectors

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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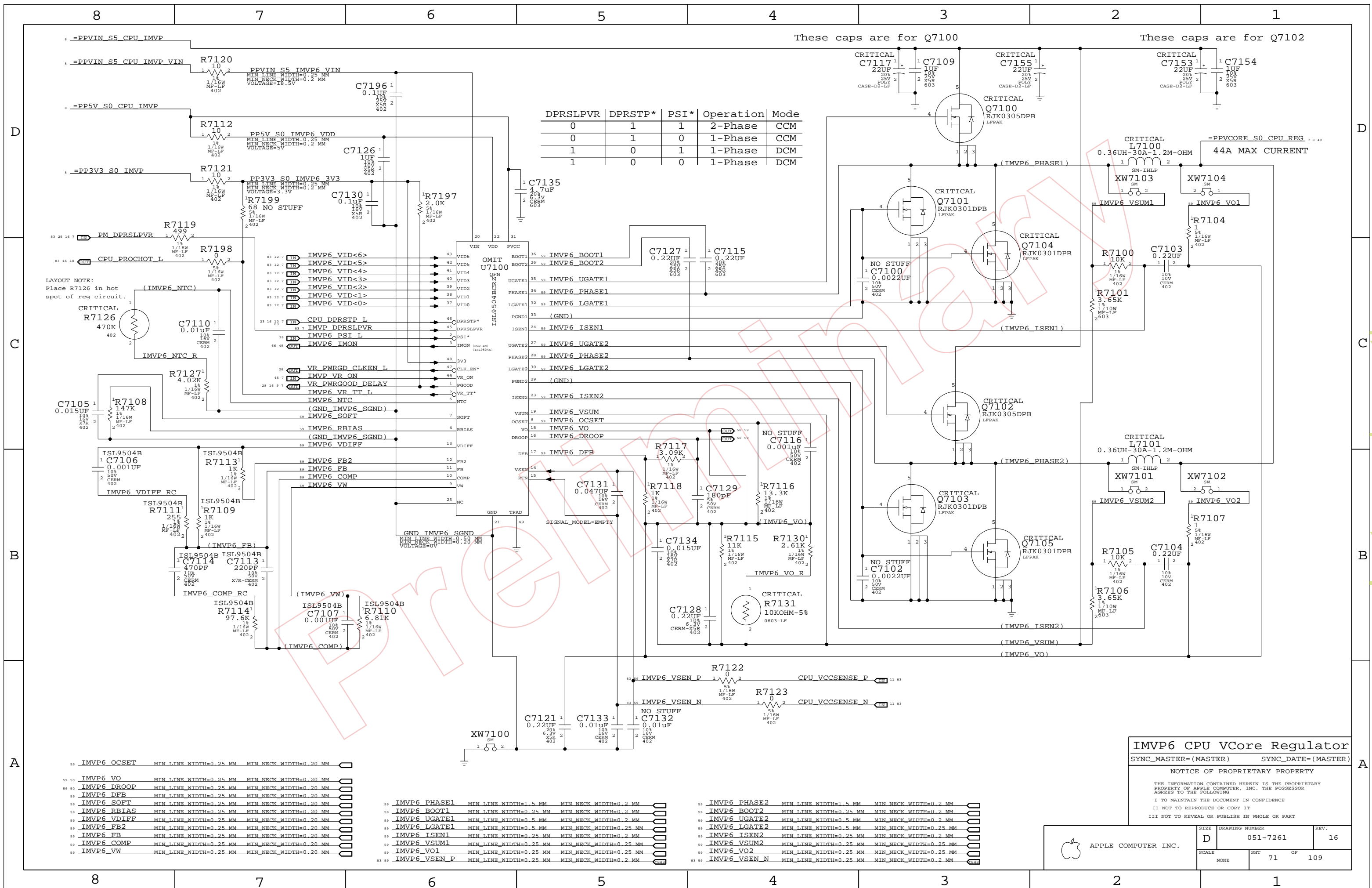
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	109
NONE	69		



**Power FETs**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=04/02/2007  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	NONE	SHT	70 OF 109

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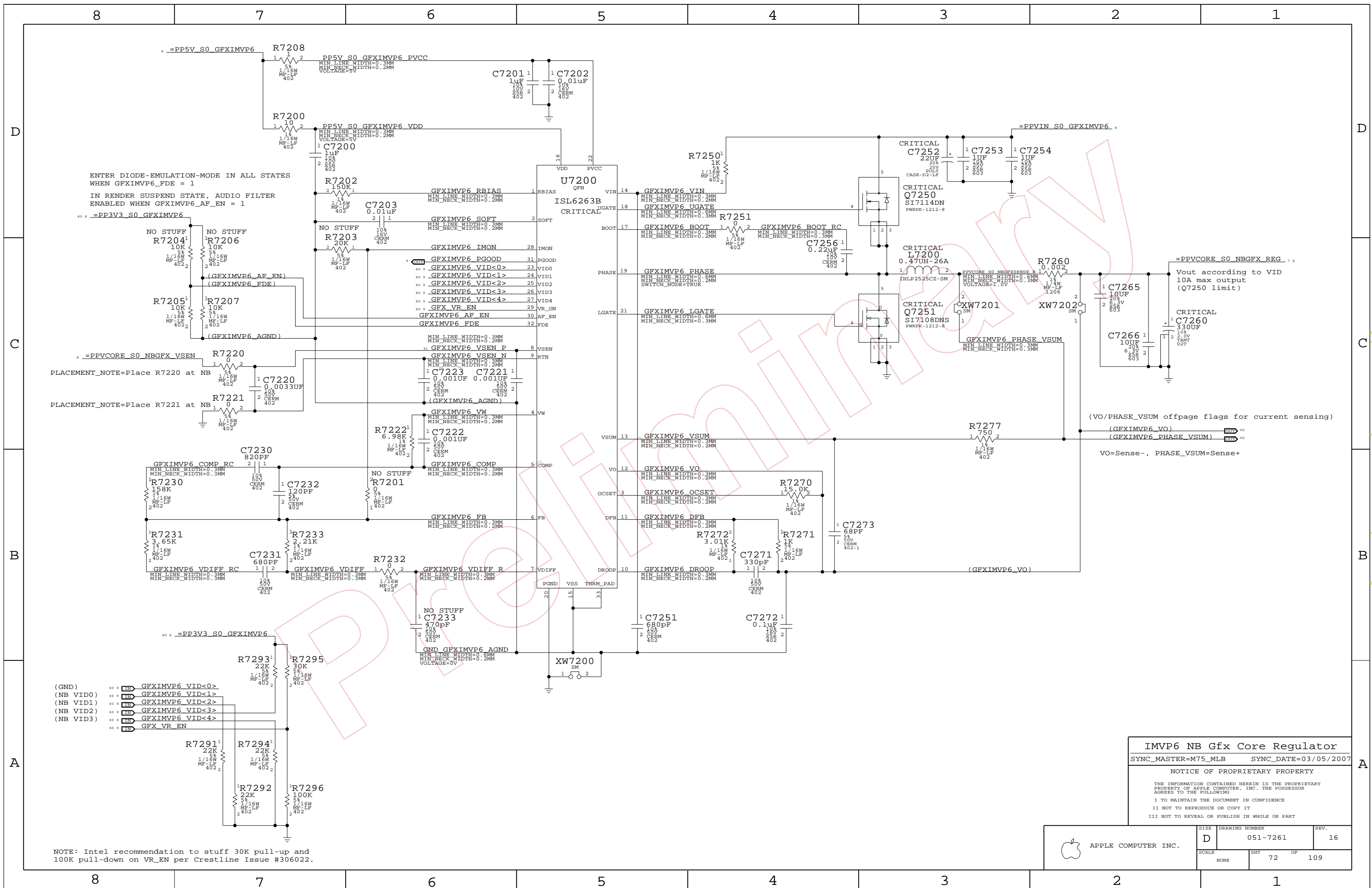


DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

**IMVP6 CPU VCore Regulator**  
 SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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	D	051-7261	16
SCALE	SHEET	OF	
NONE	71	OF	109



ENTER DIODE-EMULATION-MODE IN ALL STATES  
WHEN GFXIMVP6\_FDE = 1  
IN RENDER SUSPEND STATE, AUDIO FILTER  
ENABLED WHEN GFXIMVP6\_AF\_EN = 1

NO STUFF R7204 10K  
NO STUFF R7206 10K  
(GFXIMVP6\_AF\_EN)  
(GFXIMVP6\_FDE)  
R7205 10K  
R7207 10K  
(GFXIMVP6\_AGND)

PPVCORE\_S0\_NBGFX\_VSEN R7220  
PLACEMENT\_NOTE=Place R7220 at NB  
R7221  
PLACEMENT\_NOTE=Place R7221 at NB

GFXIMVP6\_COMP\_RC C7230 820PF  
R7230 15K  
C7232 20PF  
R7231 3.65K  
R7233 2.21K  
GFXIMVP6\_VDIFF\_RC C7231 680PF  
R7232  
GFXIMVP6\_VDIFF R

PP3V3\_S0\_GFXIMVP6 R7293 22K  
R7295 30K  
R7291 22K  
R7294 22K  
R7292 22K  
R7296 100K

NOTE: Intel recommendation to stuff 30K pull-up and 100K pull-down on VR\_EN per Crestline Issue #306022.

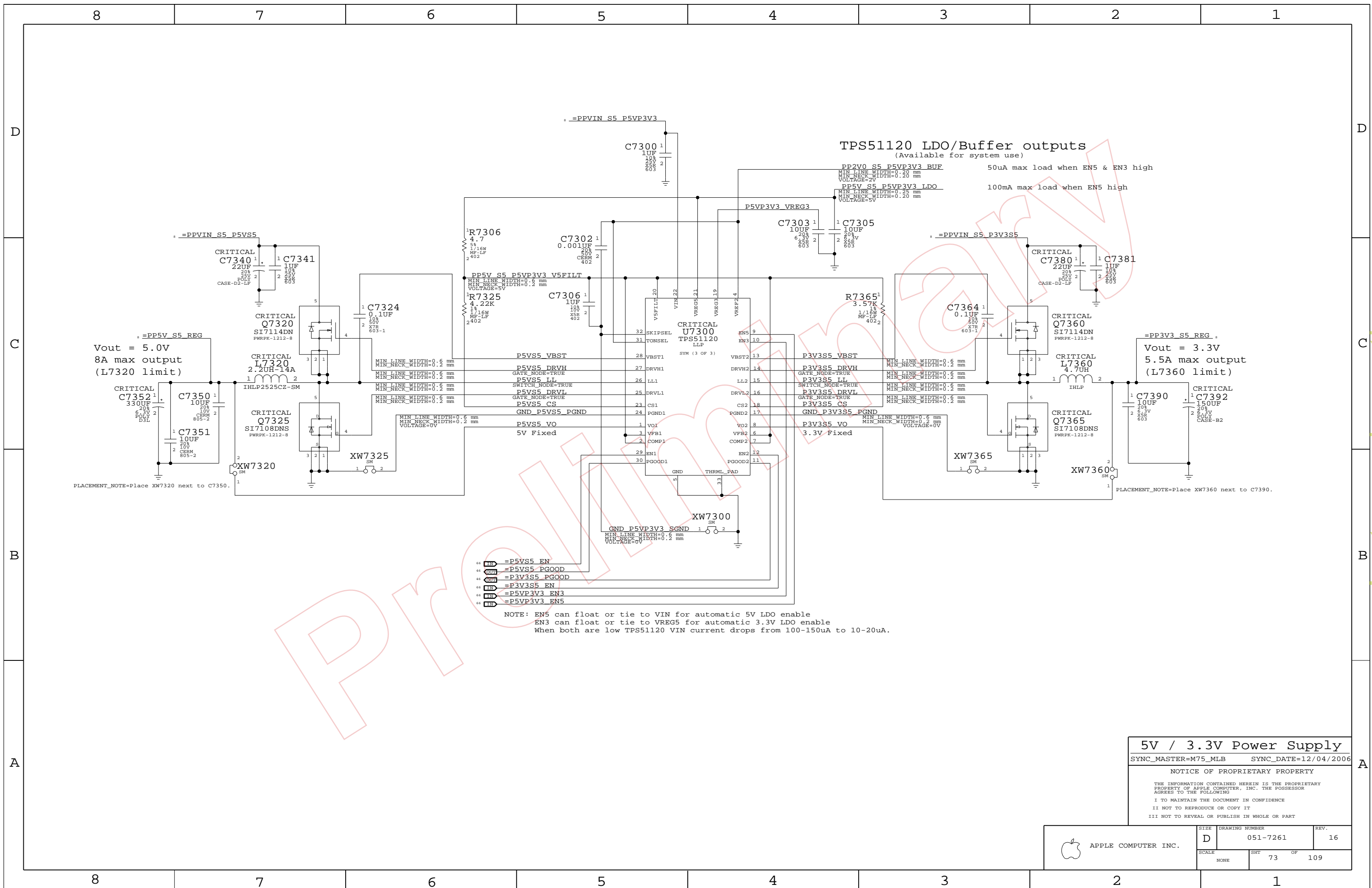
IMVP6 NB Gfx Core Regulator  
SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/05/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	72	109	

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**TPS51120 LDO/Buffer outputs**  
(Available for system use)

PP2V0 S5 P5VP3V3 BUF 50uA max load when EN5 & EN3 high  
 MIN\_LINE\_WIDTH=0.20 mm  
 MIN\_NECK\_WIDTH=0.20 mm  
 VOLTAGE=2V  
 P5V S5 P5VP3V3 LDO 100mA max load when EN5 high  
 MIN\_LINE\_WIDTH=0.25 mm  
 MIN\_NECK\_WIDTH=0.20 mm  
 VOLTAGE=5V

Vout = 5.0V  
8A max output  
(L7320 limit)

Vout = 3.3V  
5.5A max output  
(L7360 limit)

- 65 =P5VS5\_EN
- 66 =P5VS5\_PGOOD
- 67 =P3V3S5\_PGOOD
- 68 =P3V3S5\_EN
- 69 =P5VP3V3\_EN3
- 70 =P5VP3V3\_EN5

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable  
 EN3 can float or tie to VREG5 for automatic 3.3V LDO enable  
 When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

**5V / 3.3V Power Supply**

SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006

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SCALE	SHT	OF	REV.
NONE	73	109	

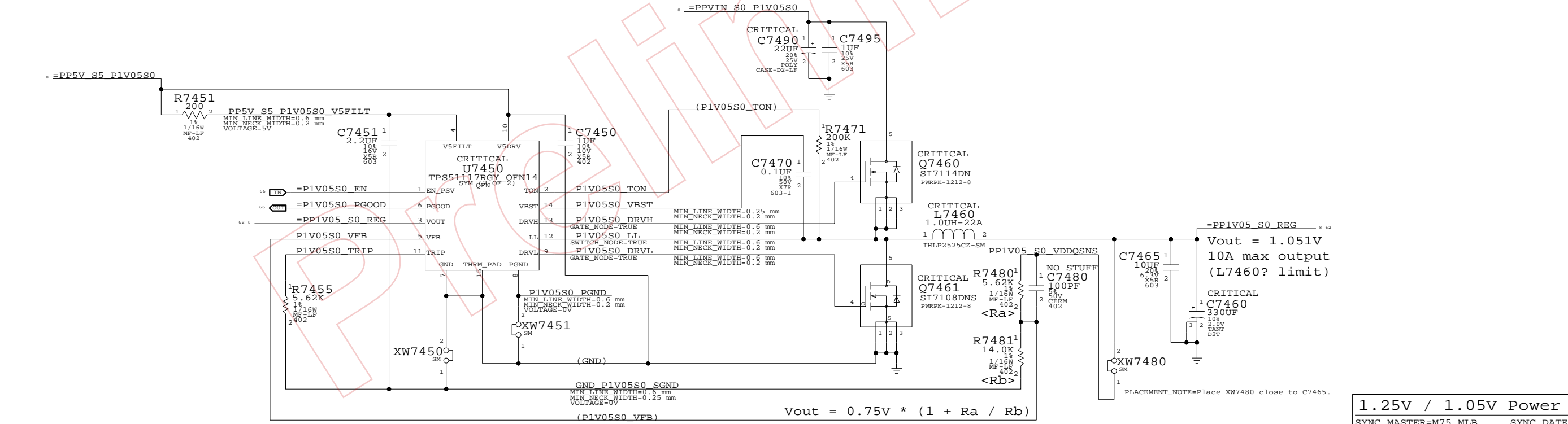
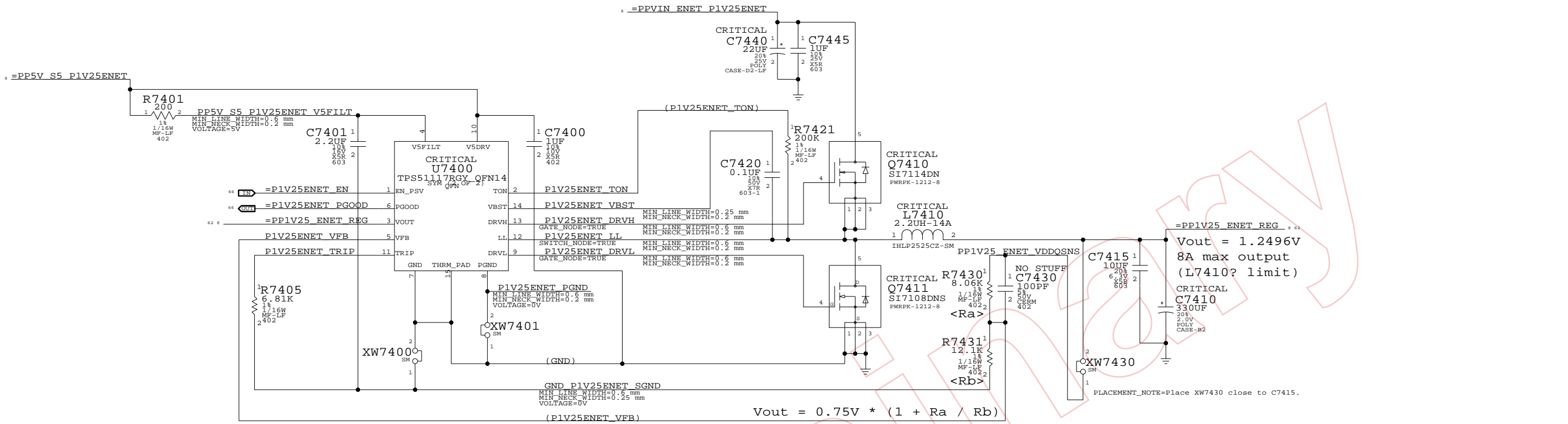
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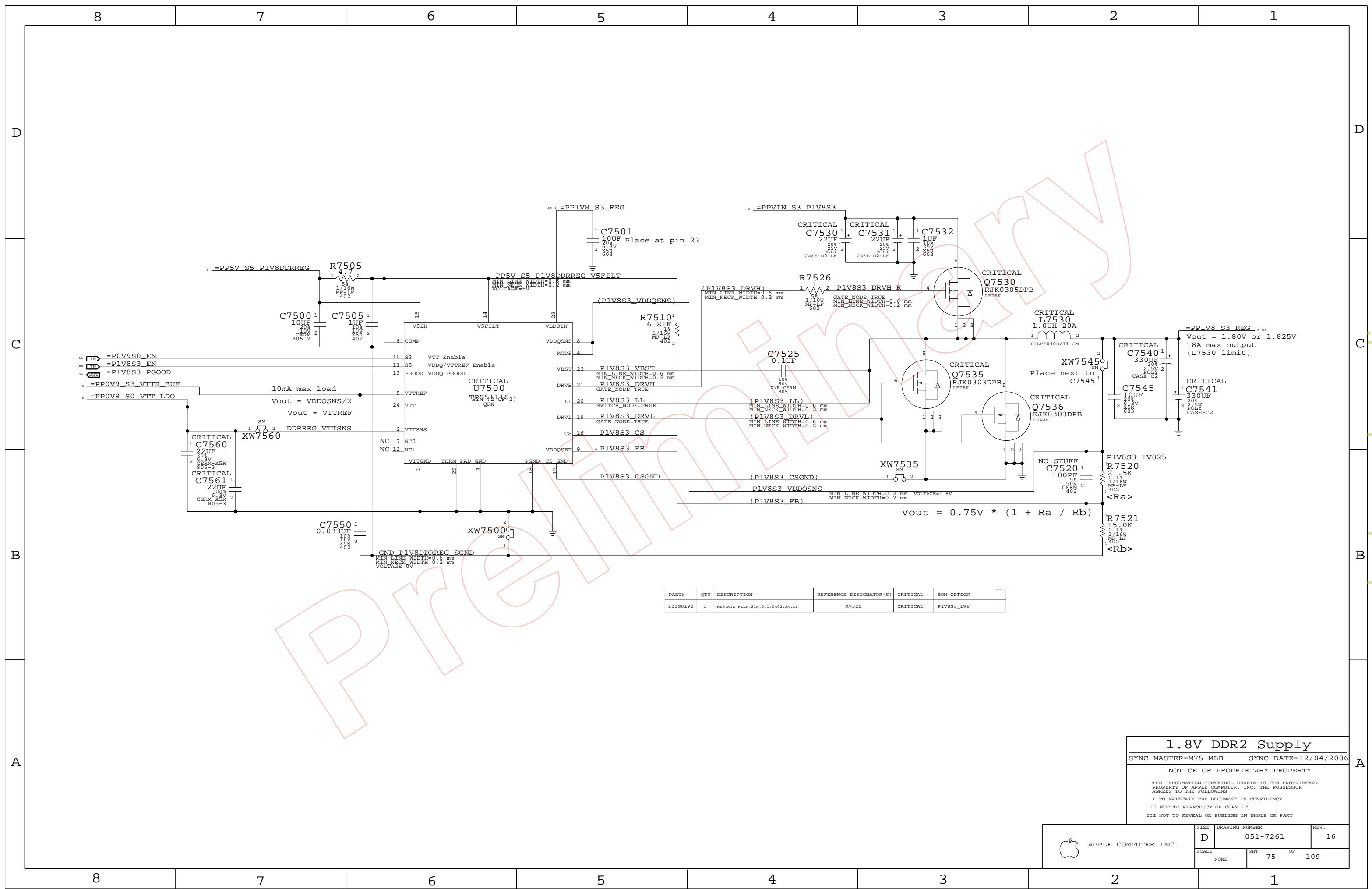
A



1.25V / 1.05V Power Supply  
SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/05/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	74	109	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10380192	1	RES,MTL FILM,21K,0.1,0402,SM,LF	R7520	CRITICAL	P1V8S3_LV8

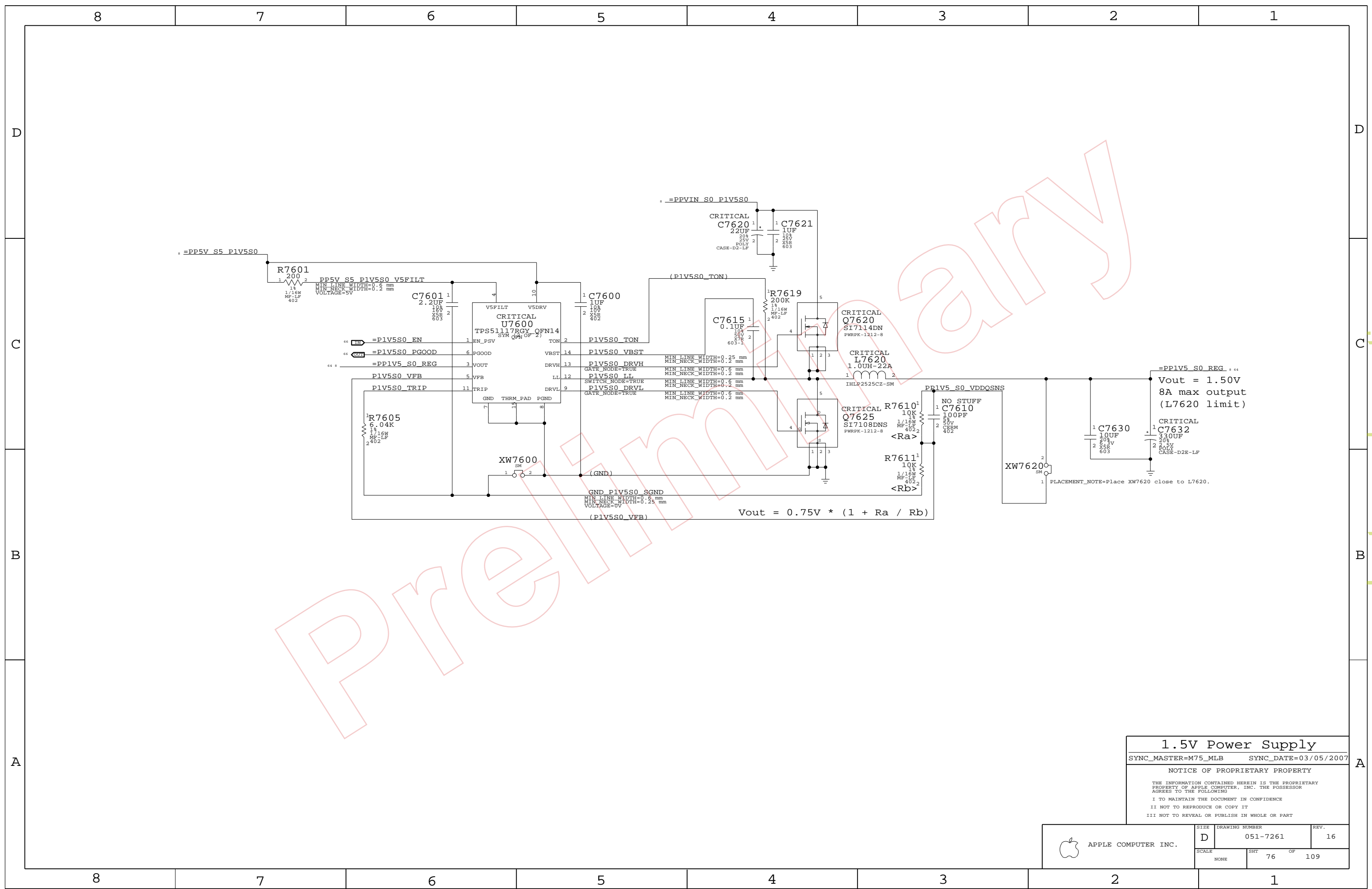
**1.8V DDR2 Supply**  
 SYNC\_MASTER=M75\_MLB    SYNC\_DATE=12/04/2006

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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF	
NONE	75	109	



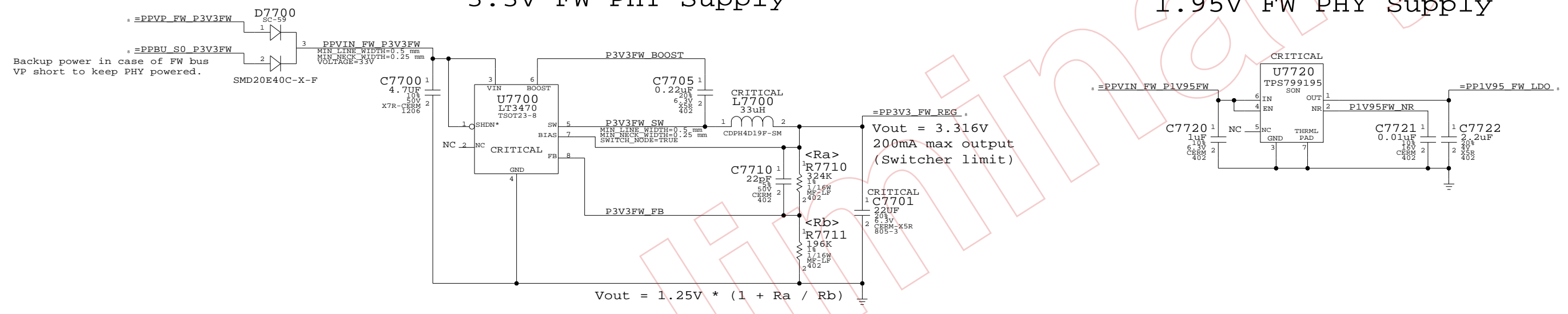
**1.5V Power Supply**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/05/2007  
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT		OF
NONE	76		109



### 3.3V FW PHY Supply

### 1.95V FW PHY Supply



#### FW PHY Power Supplies

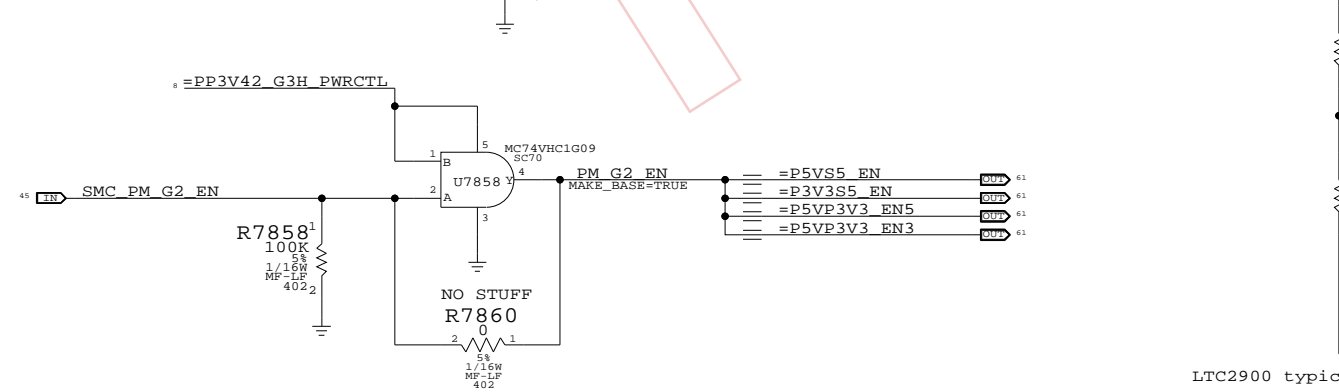
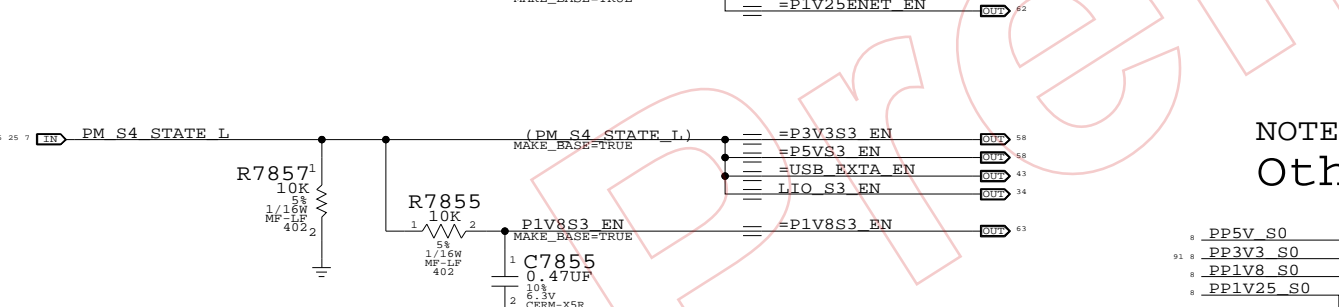
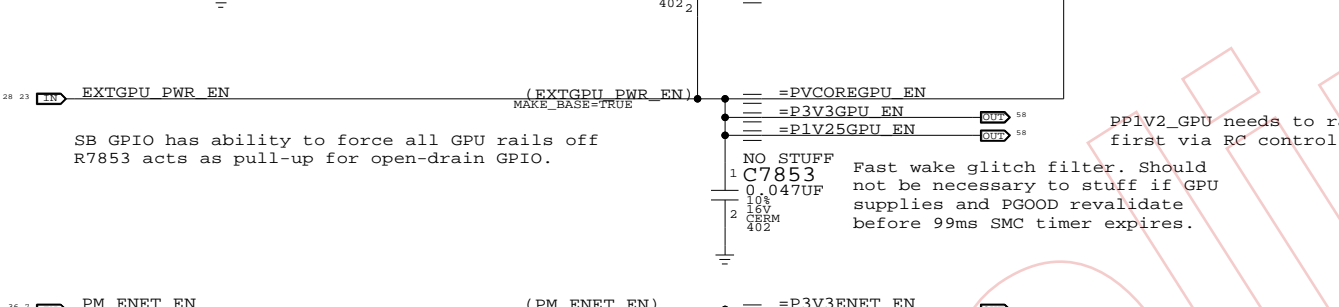
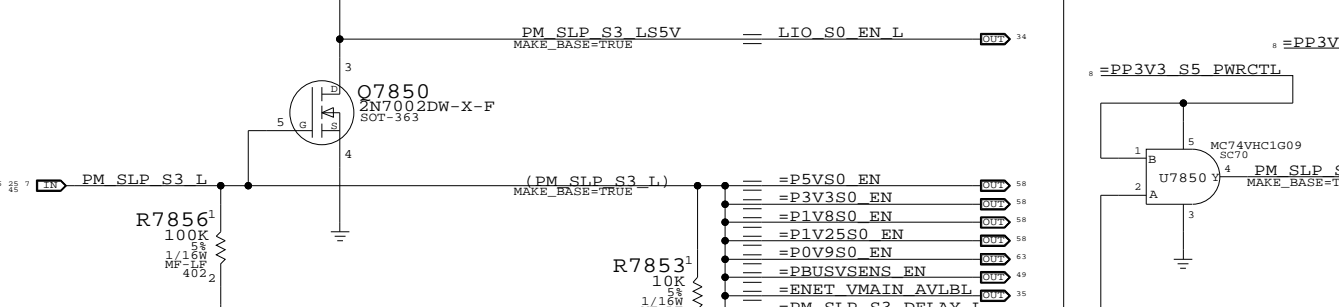
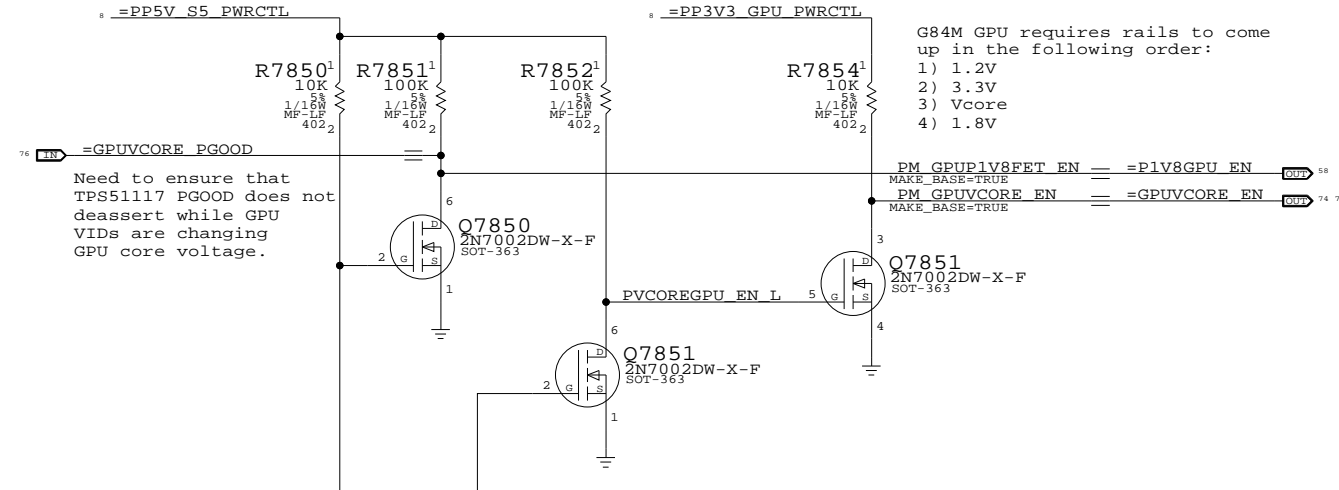
SYNC\_MASTER=M75\_MLB SYNC\_DATE=12/04/2006

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE		SHT	OF
NONE		77	109

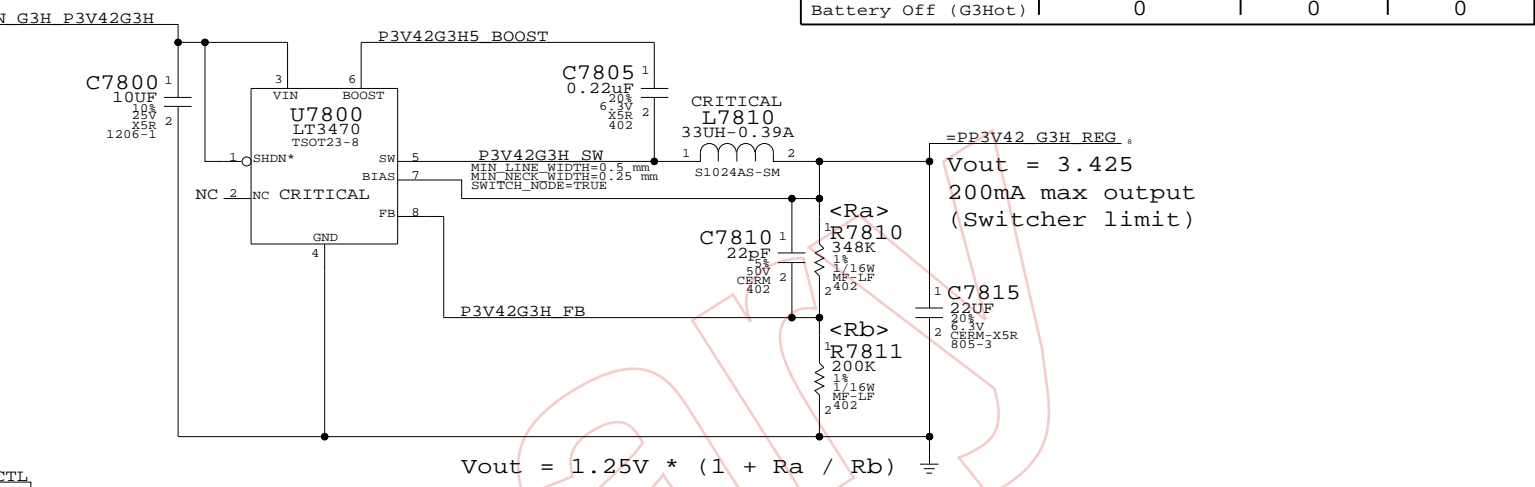
# Power Control Signals



# 3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

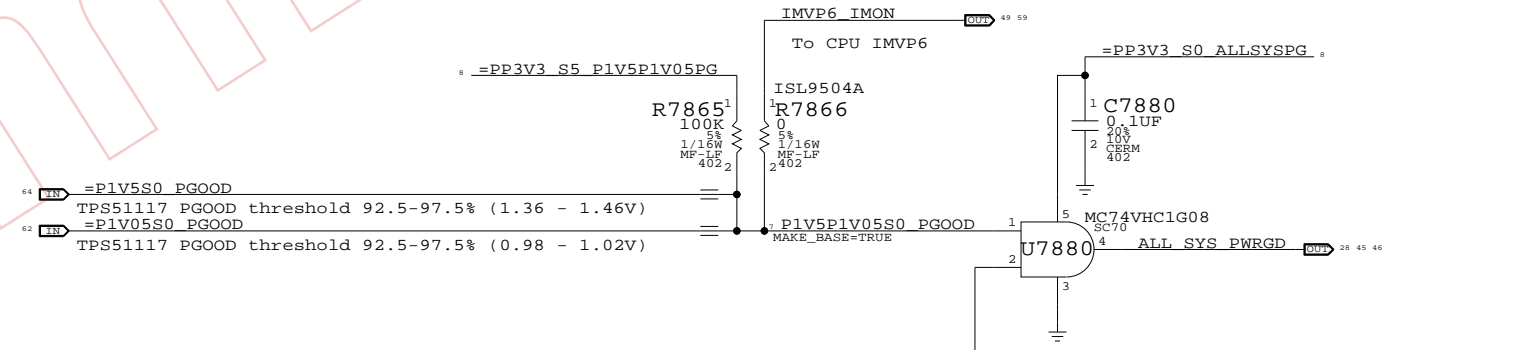


# Unused PGOOD Signals

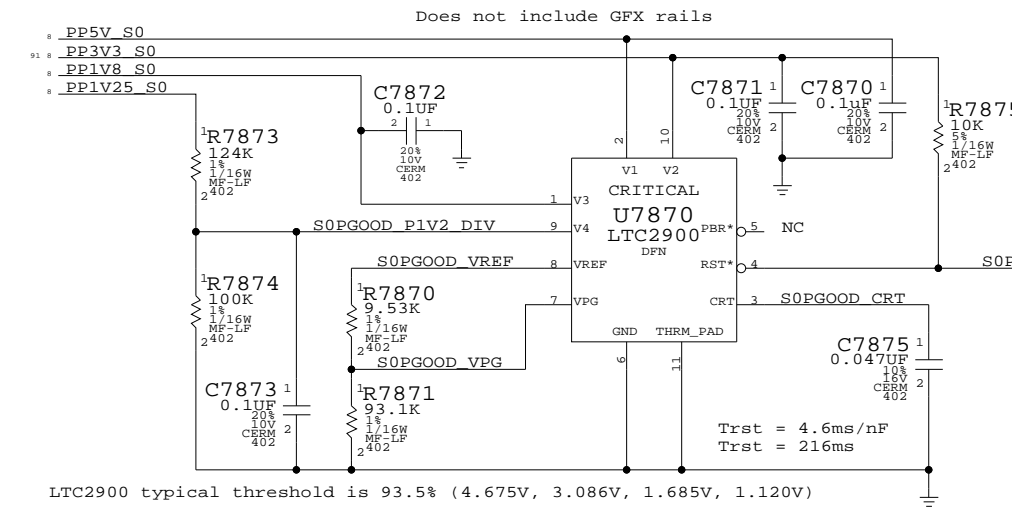
- =P1V25ENET PGOOD = TP P1V25ENET PGOOD
- =P1V8S3 PGOOD = TP P1V8S3 PGOOD

# 1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



# NOTE: 0.9V/2.5V is not checked! Other S0 Rails PWRGD Circuit

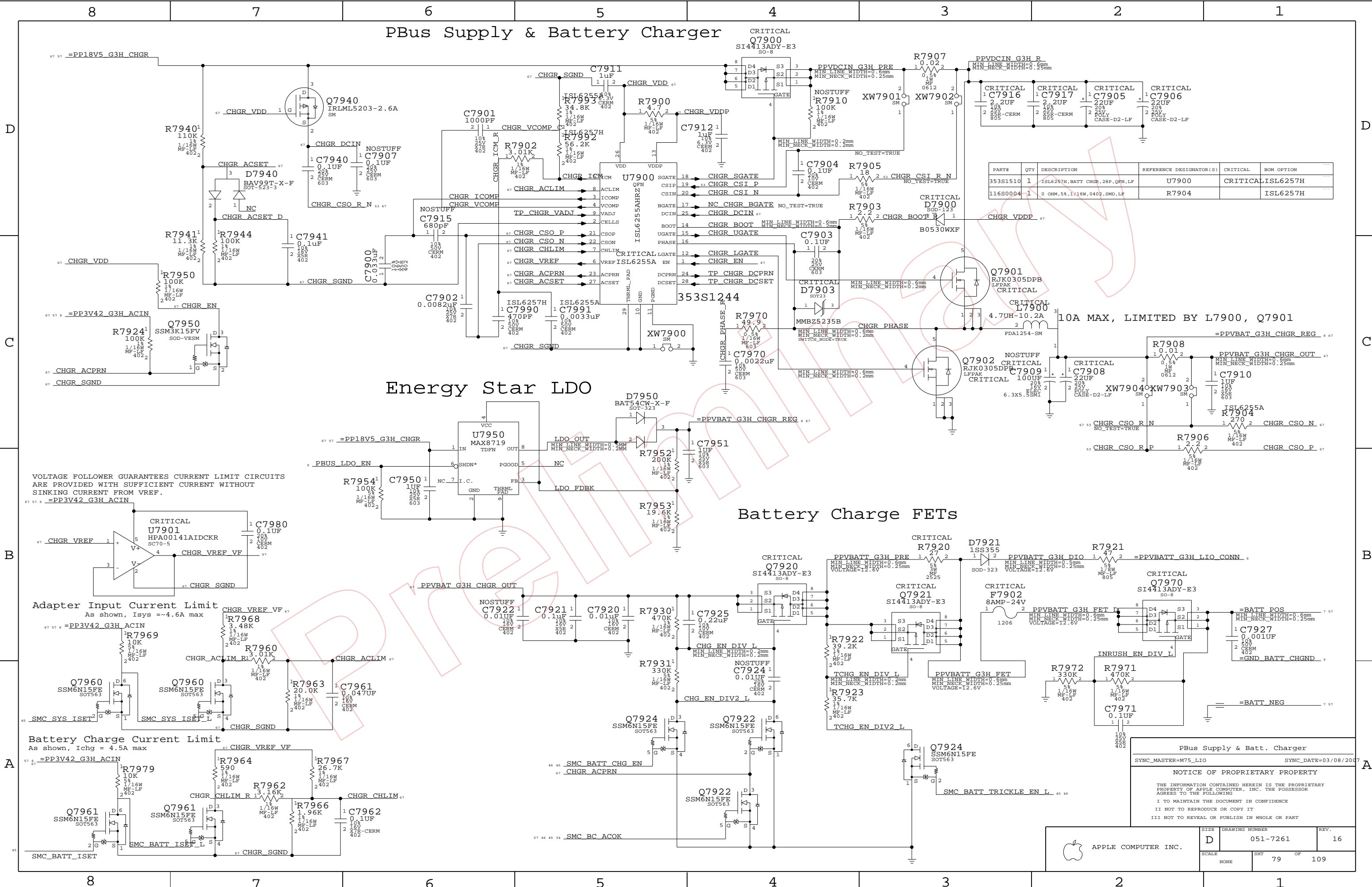


3.425V G3Hot Supply & Power Control  
SYNC\_MASTER=M75\_MLB SYNC\_DATE=04/02/2007

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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7261	16
SCALE	SHT	OF	
NONE	78	109	

# PBus Supply & Battery Charger



## Energy Star LDO

VOLTAGE FOLLOWER GUARANTEES CURRENT LIMIT CIRCUITS ARE PROVIDED WITH SUFFICIENT CURRENT WITHOUT SINKING CURRENT FROM VREF.

## Battery Charge FETs

### Adapter Input Current Limit

As shown,  $I_{syt} \approx -4.6A$  max

### Battery Charge Current Limit

As shown,  $I_{chg} = 4.5A$  max

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1510	1	ISL6257H, BATT CHGR, 28P, QFN, LF	U7900	CRITICAL	ISL6257H
116S0004	1	0 OHM, 5%, 1/16W, 0402, SMD, LF	R7904		ISL6257H

10A MAX, LIMITED BY L7900, Q7901

PBus Supply & Batt. Charger  
 SYNC\_MASTER=M75\_LIO SYNC\_DATE=03/08/2007

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	D	051-7261	16
SCALE	SHEET	OF	
NONE	79	109	

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# Page Notes

Power aliases required by this page:

- =PPIV2\_GPU\_PEX\_PLLXVDD
- =PPIV2\_GPU\_PEX\_IOVDDQ
- =PPIV2\_GPU\_PEX\_IOVDD

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

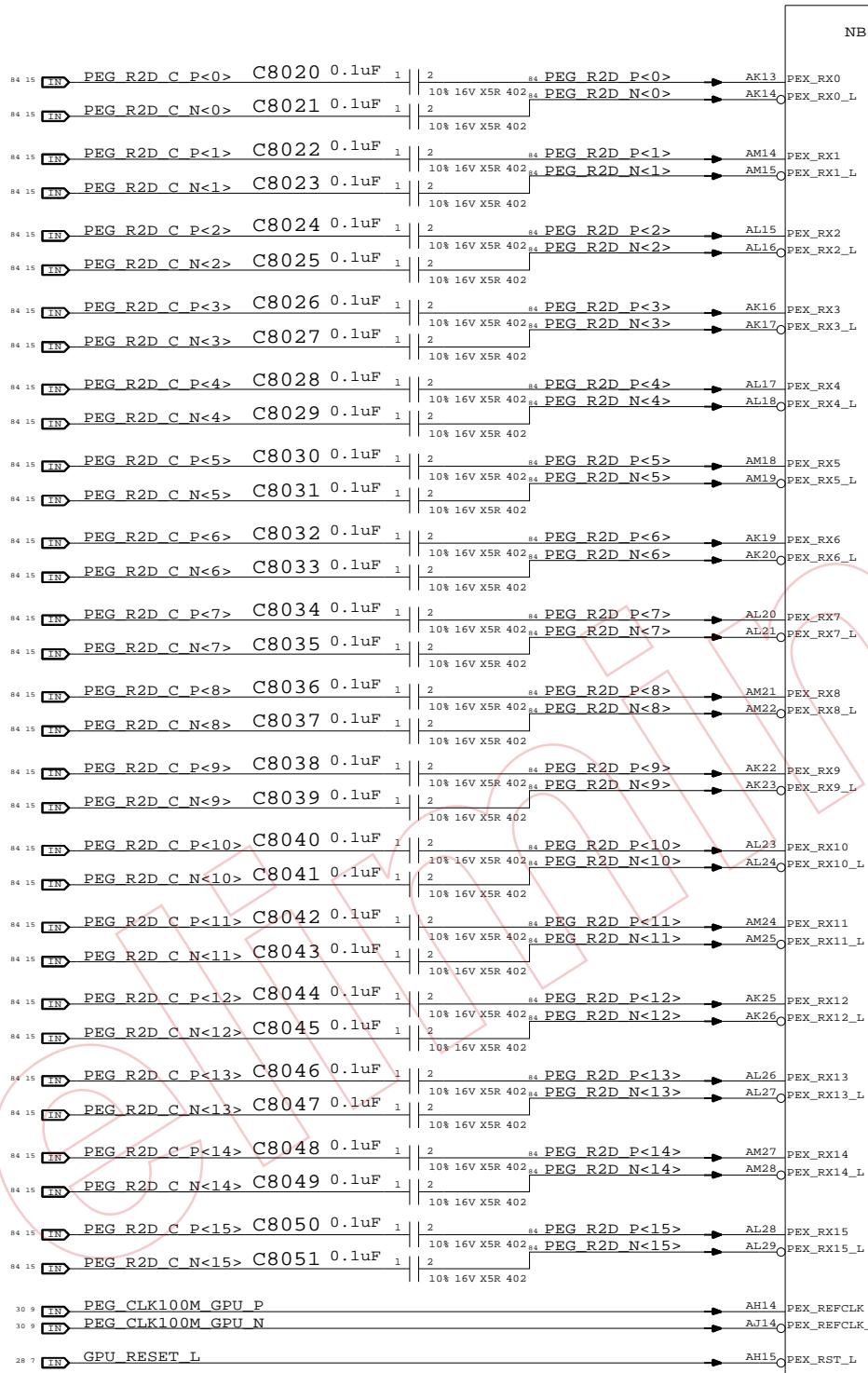
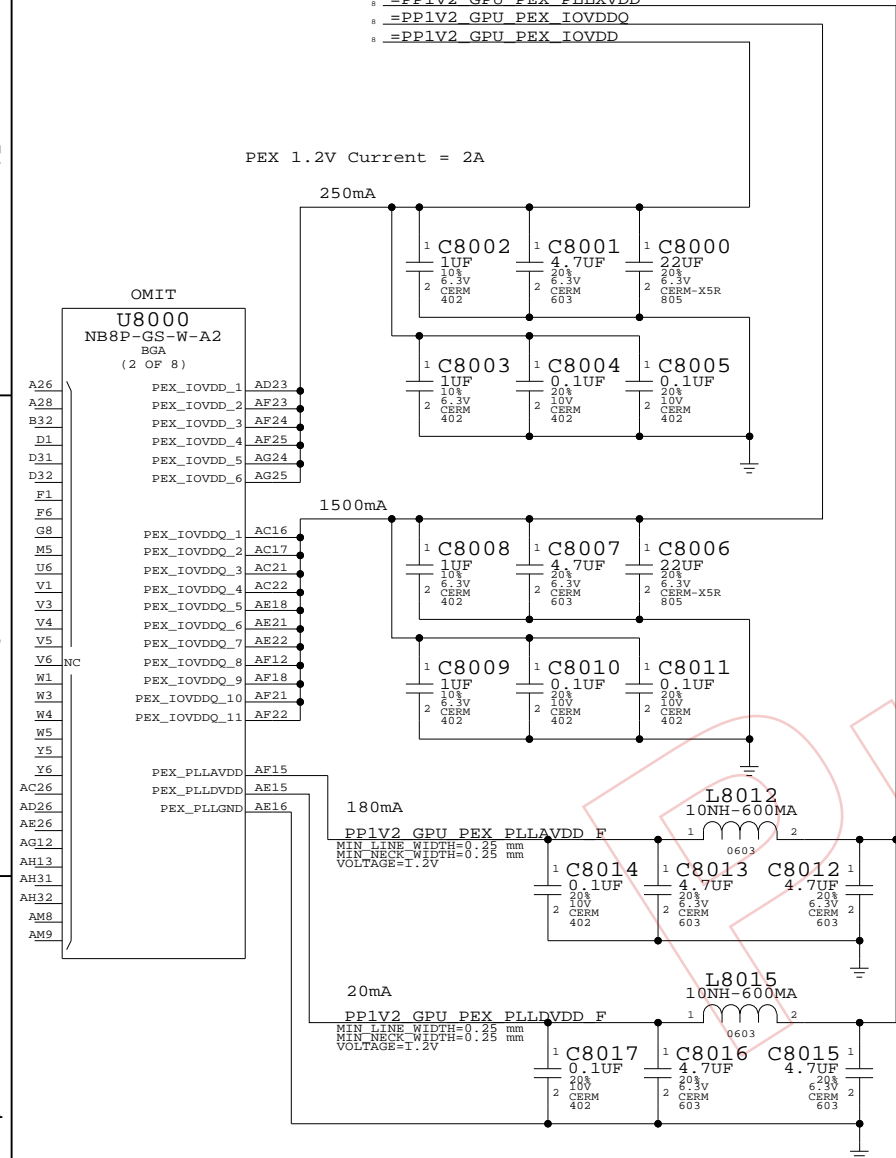
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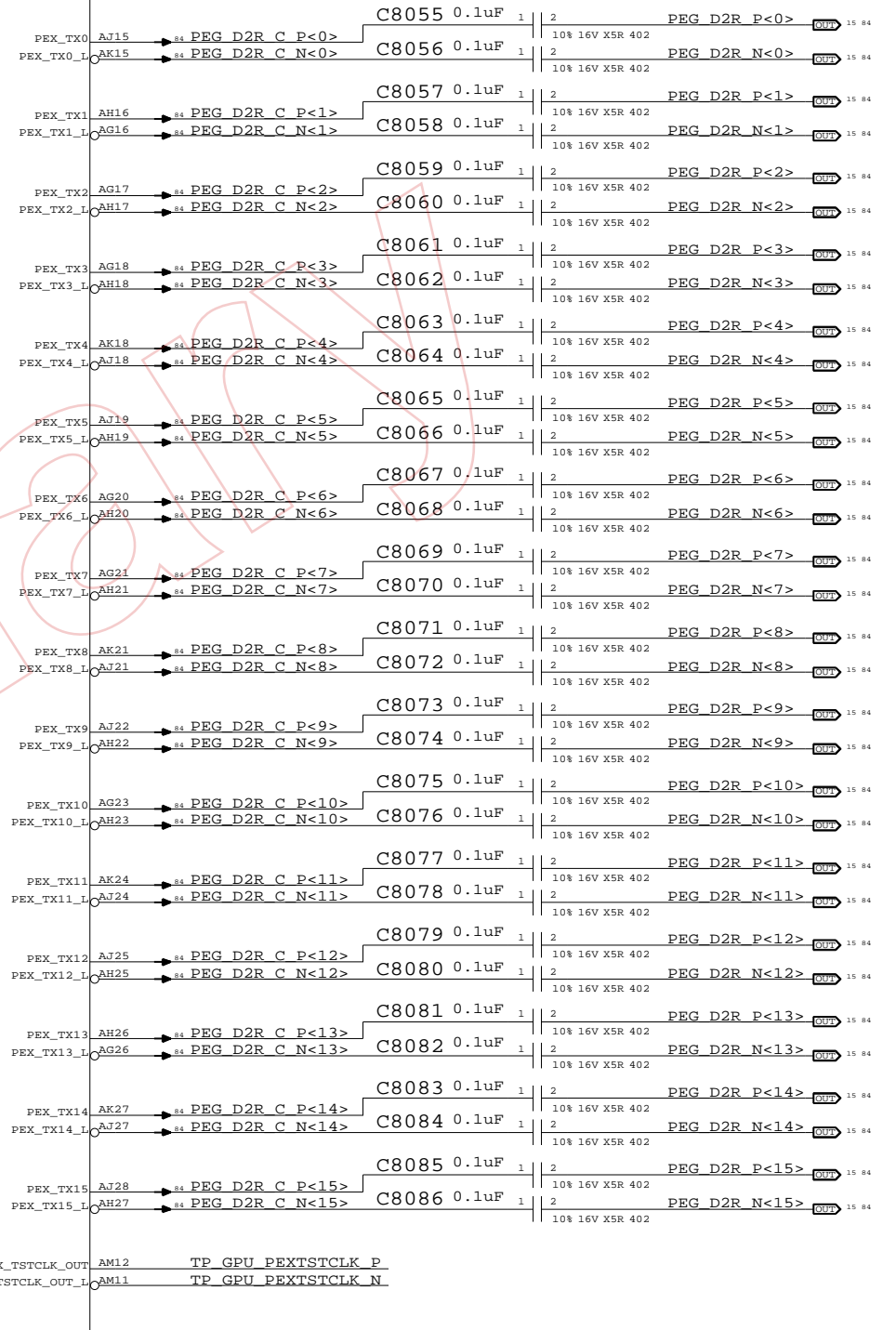
A



OMIT

U8000 NB8P-GS-W-A2 BGA (1 OF 8)

PCI EXPRESS BUS INTERFACE



NV G84M PCI-E

SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007

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SCALE	SHT	OF	
NONE	80	109	

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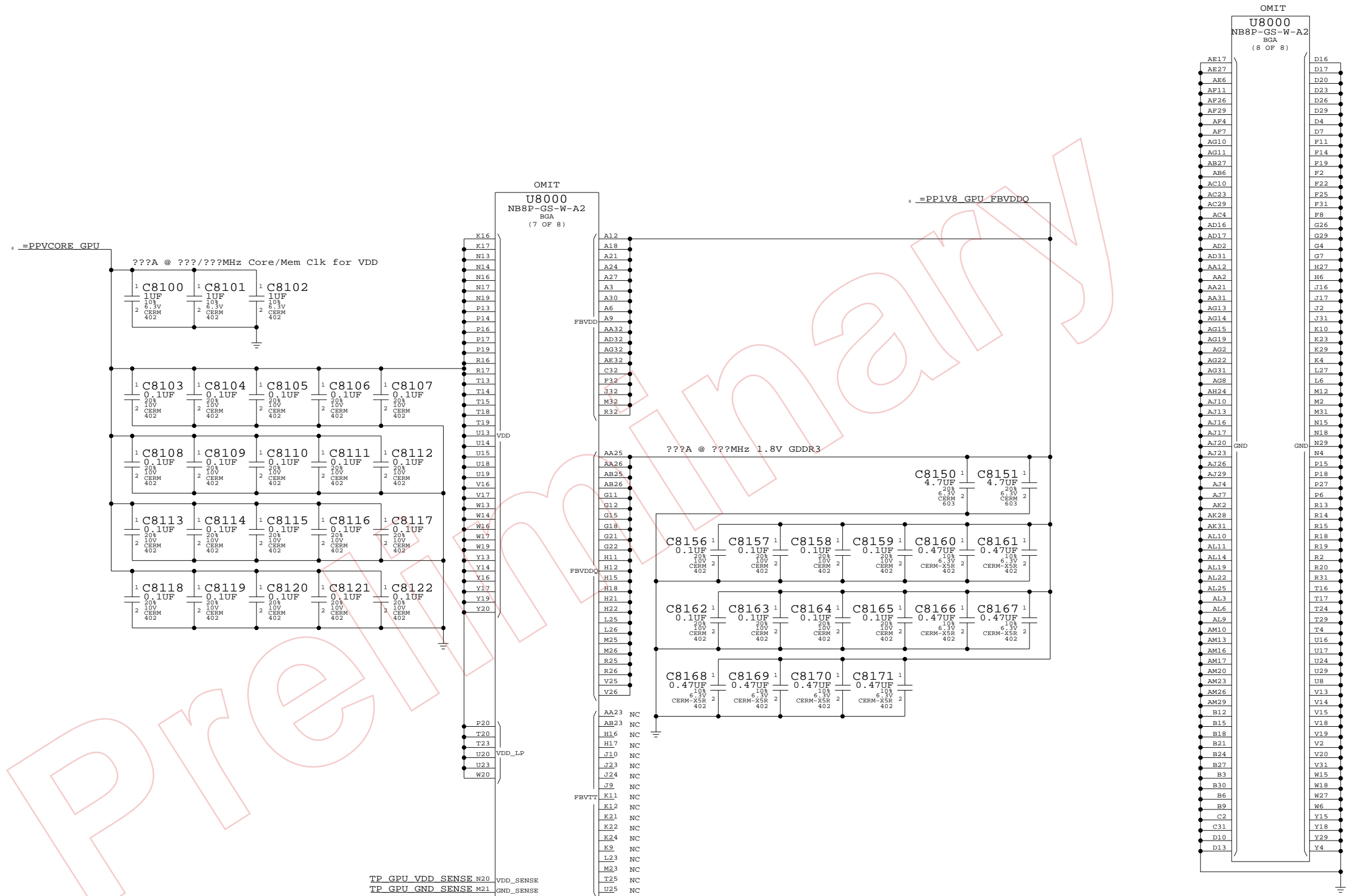
# Page Notes

Power aliases required by this page:

- =PPVCORE\_GPU
- =PP1V8\_GPU\_FBVDDQ

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)



## NV G84M Core/FB Power

SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007

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SCALE	SHT	OF	
NONE	81	109	

# Page Notes

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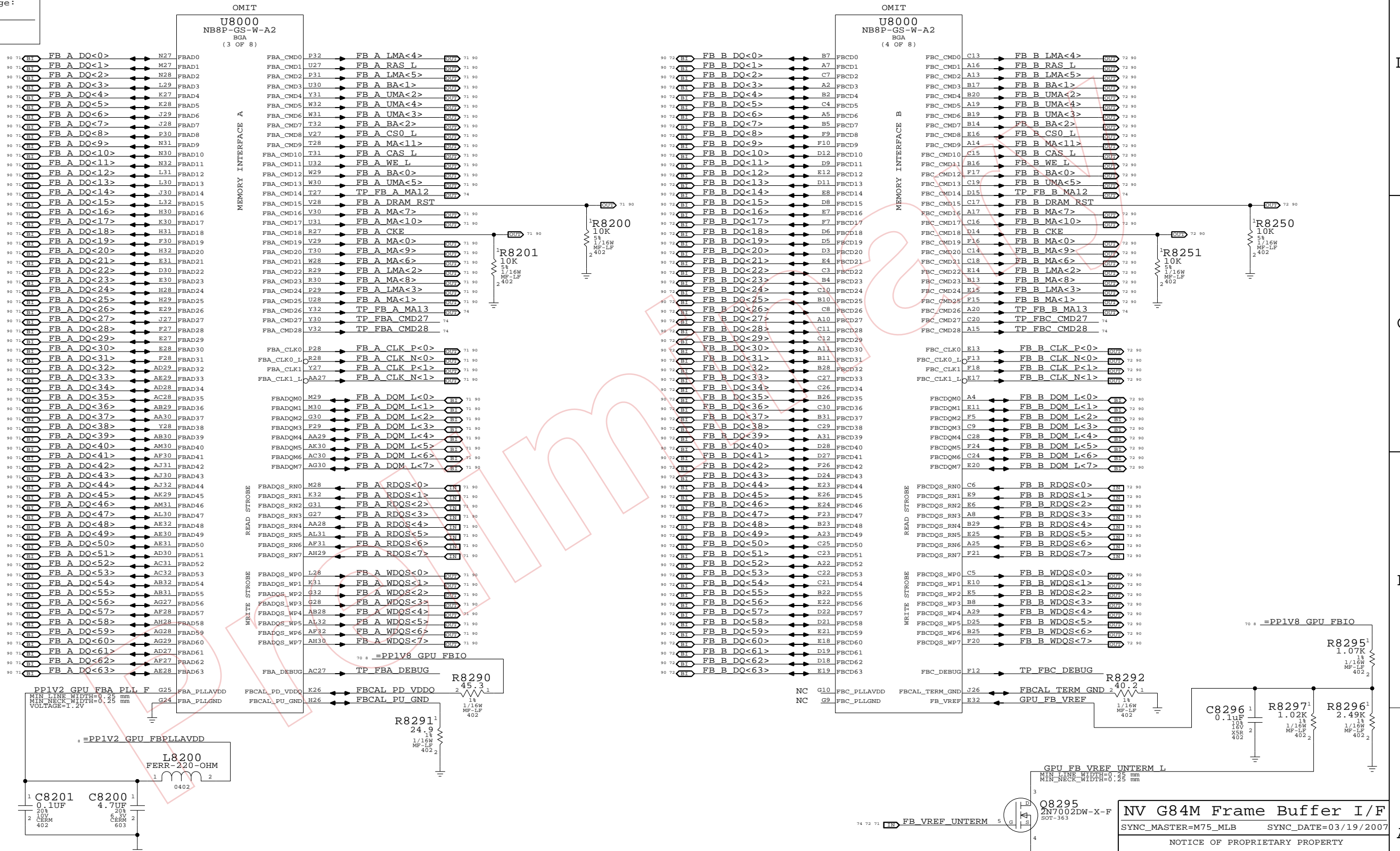
- =PP1V2\_GPU\_FBLLAVDD
- =PP1V8\_GPU\_FBIO

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)



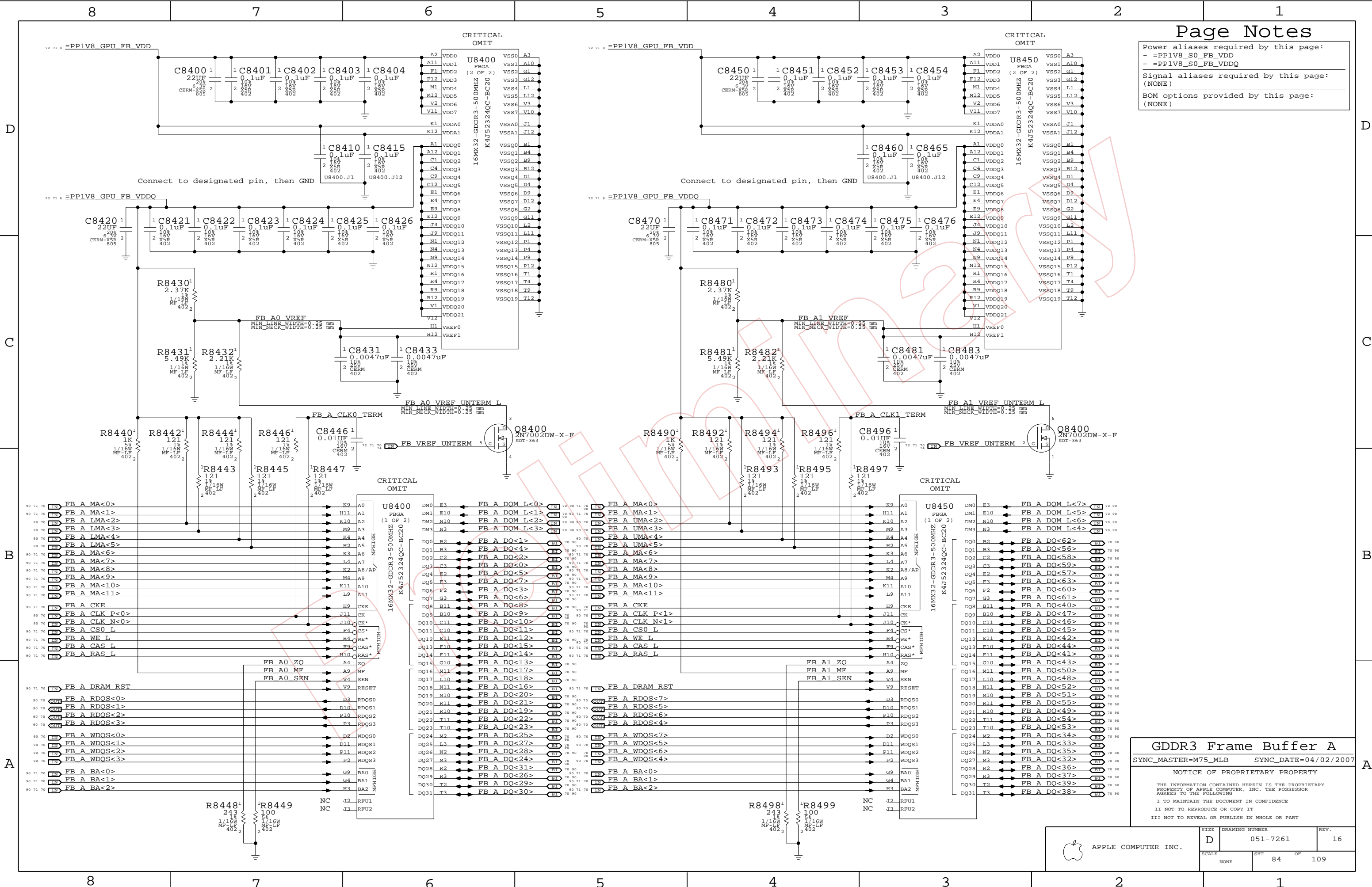
NV G84M Frame Buffer I/F  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007

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SCALE	SHT	OF	
NONE	82	OF	109

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Power aliases required by this page:  
- =PP1V8\_S0\_FB\_VDD  
- =PP1V8\_S0\_FB\_VDDQ  
Signal aliases required by this page:  
(NONE)  
BOM options provided by this page:  
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GDDR3 Frame Buffer A

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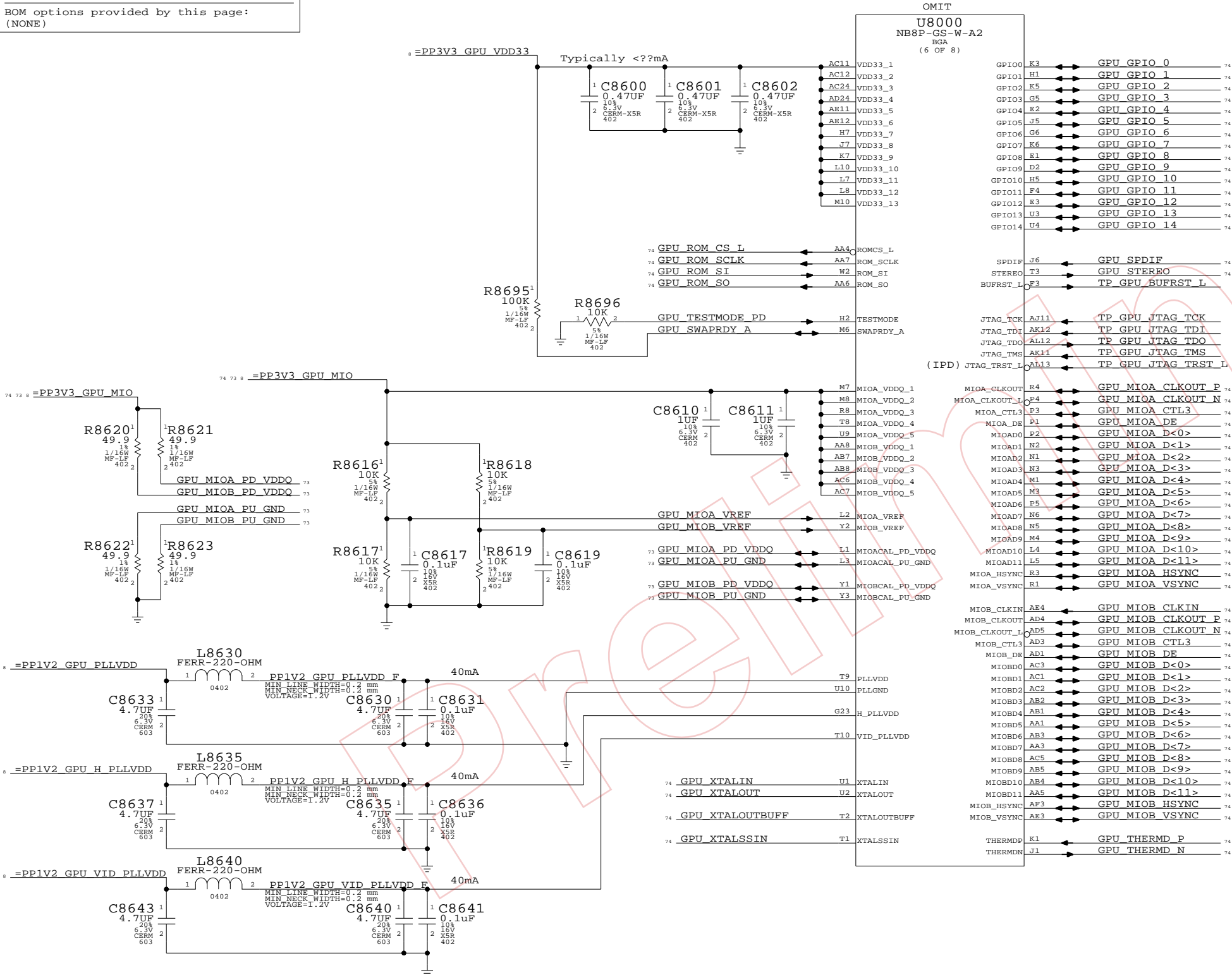


# Page Notes

Power aliases required by this page:  
 - =PP3V3\_GPU\_VDD33  
 - =PP3V3\_GPU\_MIO  
 - =PP1V2\_GPU\_PLLVDD  
 - =PP1V2\_GPU\_H\_PLLVDD  
 - =PP1V2\_GPU\_VID\_PLLVDD

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



OMIT

U8000  
NB8P-GS-W-A2  
BGA  
(6 OF 8)

GPIO0	K3	GPU GPIO 0	74
GPIO1	H1	GPU GPIO 1	74
GPIO2	K5	GPU GPIO 2	74
GPIO3	G5	GPU GPIO 3	74
GPIO4	E2	GPU GPIO 4	74
GPIO5	J5	GPU GPIO 5	74
GPIO6	G6	GPU GPIO 6	74
GPIO7	K6	GPU GPIO 7	74
GPIO8	E1	GPU GPIO 8	74
GPIO9	D2	GPU GPIO 9	74
GPIO10	H5	GPU GPIO 10	74
GPIO11	F4	GPU GPIO 11	74
GPIO12	E3	GPU GPIO 12	74
GPIO13	U3	GPU GPIO 13	74
GPIO14	U4	GPU GPIO 14	74
SPDIP	J6	GPU SPDIF	74
STEREO	T3	GPU STEREO	74
BUFRST_L	F3	TP GPU BUFRST L	74
JTAG_TCK	AJ11	TP GPU JTAG TCK	74
JTAG_TDI	AK12	TP GPU JTAG TDI	74
JTAG_TDO	AL12	TP GPU JTAG TDO	74
JTAG_TMS	AK11	TP GPU JTAG TMS	74
(IPD) JTAG_TRST_L	AL13	TP GPU JTAG TRST L	74
MIOA_CLKOUT	R4	GPU MIOA CLKOUT P	74
MIOA_CLKOUT_N	P4	GPU MIOA CLKOUT N	74
MIOA_CTL3	P3	GPU MIOA CTL3	74
MIOA_DE	P1	GPU MIOA DE	74
MIOAD0	P2	GPU MIOA D<0>	74
MIOAD1	N2	GPU MIOA D<1>	74
MIOAD2	N1	GPU MIOA D<2>	74
MIOAD3	N3	GPU MIOA D<3>	74
MIOAD4	M1	GPU MIOA D<4>	74
MIOAD5	M3	GPU MIOA D<5>	74
MIOAD6	P5	GPU MIOA D<6>	74
MIOAD7	N6	GPU MIOA D<7>	74
MIOAD8	N5	GPU MIOA D<8>	74
MIOAD9	M4	GPU MIOA D<9>	74
MIOAD10	L4	GPU MIOA D<10>	74
MIOAD11	L5	GPU MIOA D<11>	74
MIOA_HSYNC	R3	GPU MIOA HSYNC	74
MIOA_VSYNC	R1	GPU MIOA VSYNC	74
MIOB_CLKIN	AE4	GPU MIOB CLKIN	74
MIOB_CLKOUT	AD4	GPU MIOB CLKOUT P	74
MIOB_CLKOUT_N	AD5	GPU MIOB CLKOUT N	74
MIOB_CTL3	AD3	GPU MIOB CTL3	74
MIOB_DE	AD1	GPU MIOB DE	74
MIOBD0	AC3	GPU MIOB D<0>	74
MIOBD1	AC1	GPU MIOB D<1>	74
MIOBD2	AC2	GPU MIOB D<2>	74
MIOBD3	AB2	GPU MIOB D<3>	74
MIOBD4	AB1	GPU MIOB D<4>	74
MIOBD5	AA1	GPU MIOB D<5>	74
MIOBD6	AB3	GPU MIOB D<6>	74
MIOBD7	AA3	GPU MIOB D<7>	74
MIOBD8	AC5	GPU MIOB D<8>	74
MIOBD9	AB5	GPU MIOB D<9>	74
MIOBD10	AB4	GPU MIOB D<10>	74
MIOBD11	AA5	GPU MIOB D<11>	74
MIOB_HSYNC	AF3	GPU MIOB HSYNC	74
MIOB_VSYNC	AE3	GPU MIOB VSYNC	74
THERMDP	K1	GPU THERMD P	74
THERMDN	J1	GPU THERMD N	74

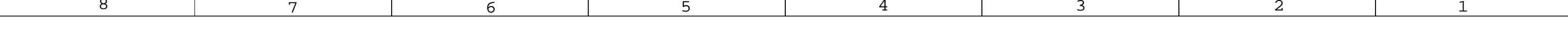
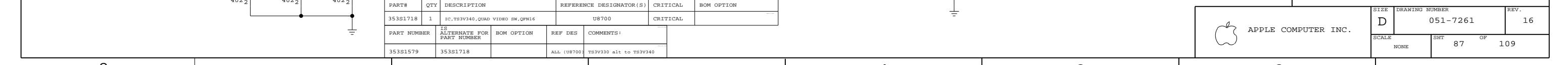
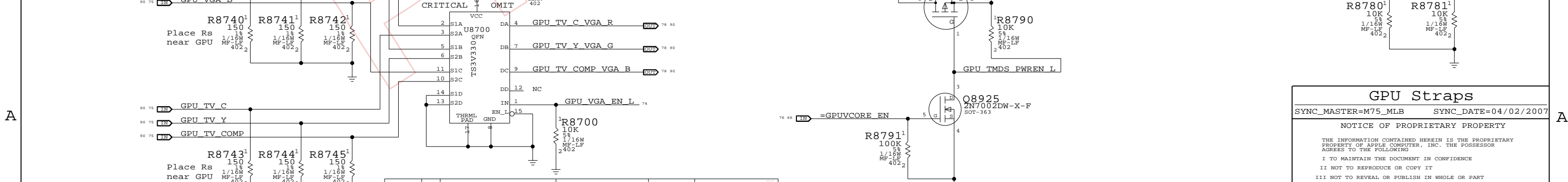
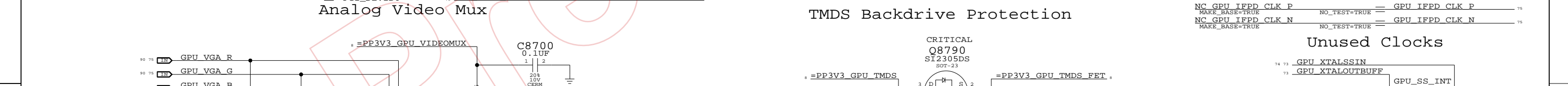
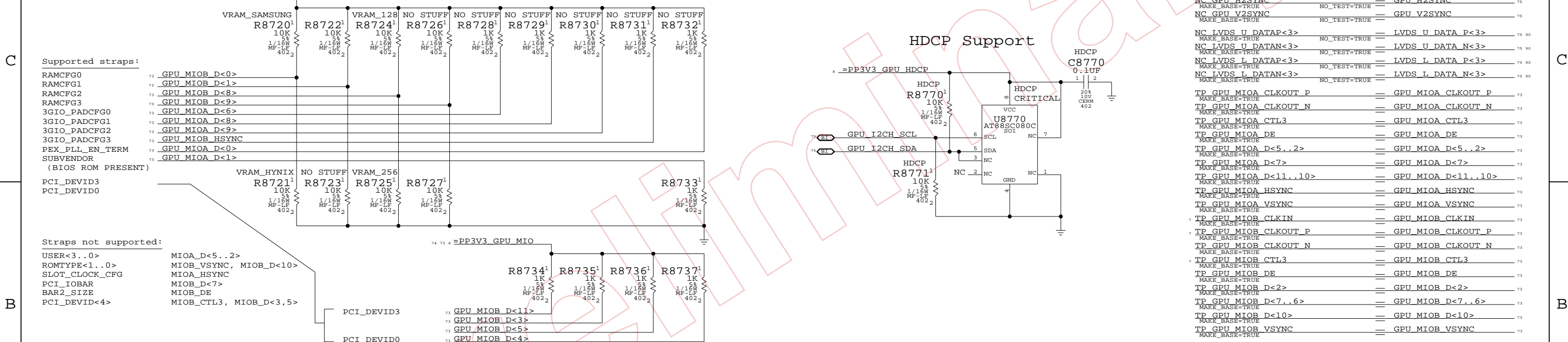
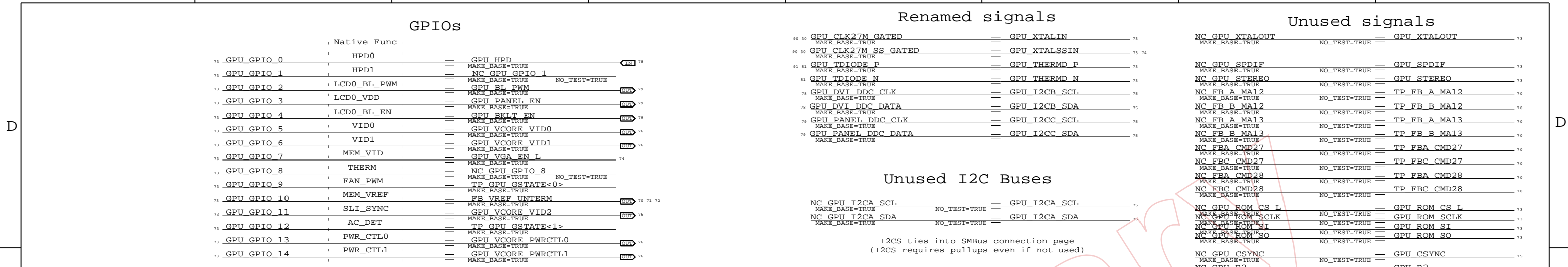
## NV G84M GPIO/MIO/Misc

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NONE	86	109	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35381718	1	IC,TS3V330,QUAD VIDEO SW,QFN16	U8700	CRITICAL	
		ALTERNATE FOR PART NUMBER	REF DES	COMMENTS:	
35381579		35381718	ALL (U8700)	TS3V330 alt to TS3V340	

**GPU Straps**

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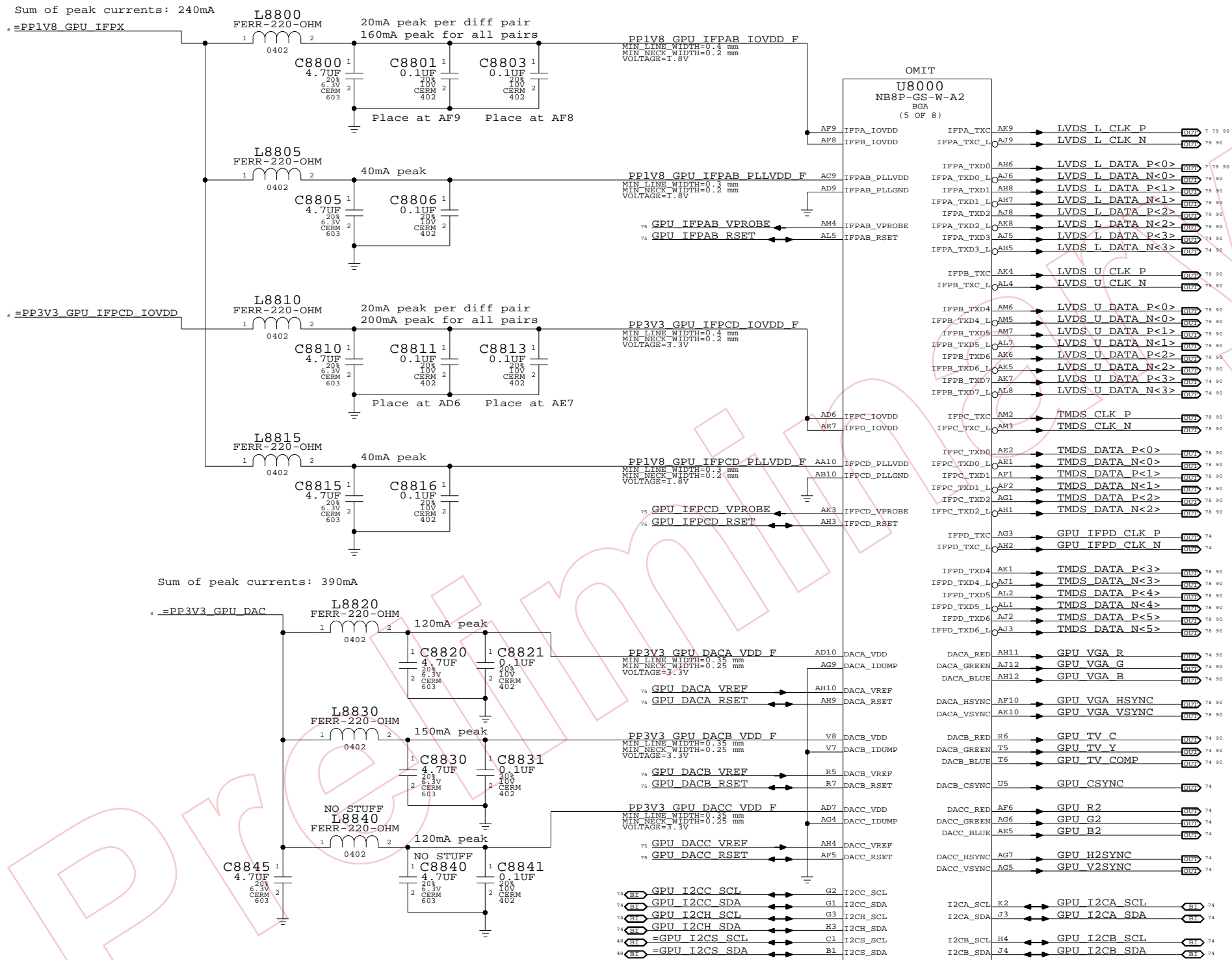
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# Page Notes

Power aliases required by this page:  
 - =PP1V8\_GPU\_IFPX  
 - =PP3V3\_GPU\_IFPCD\_IOVDD  
 - =PP3V3\_GPU\_DAC

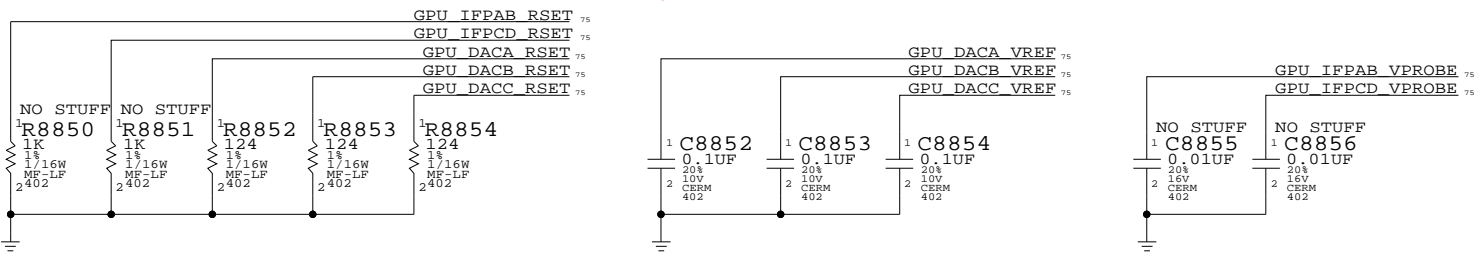
Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



I2CS must be pulled up if not used  
 I2CS addr fixed at 0x9E,0x9F

Composite/S-Video	VGA	Component
C	R	Pr
Y	G	Y
Comp	B	Pb



NV G84M Video Interfaces  
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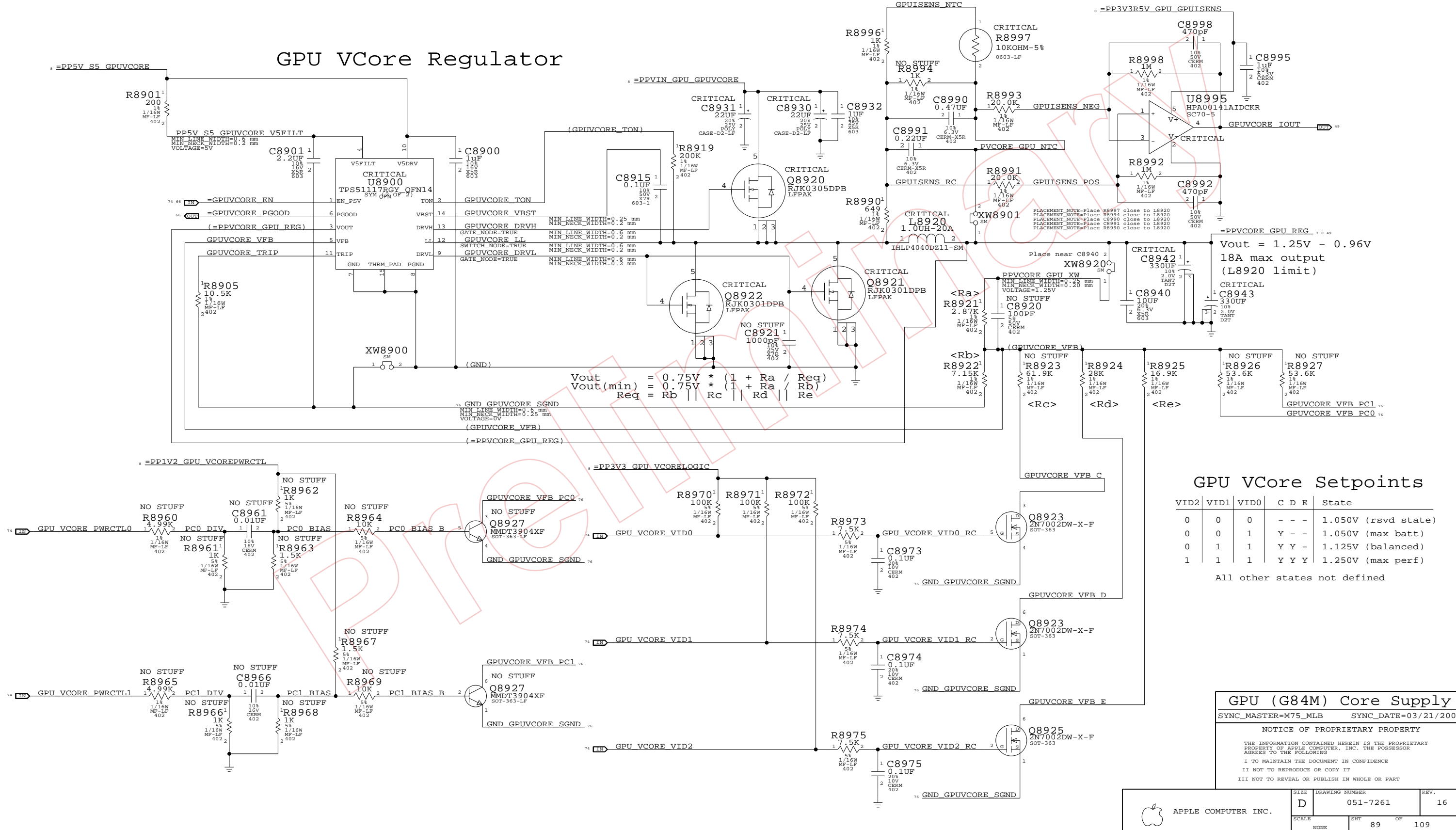
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NONE	88	109	

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# GPU VCore Regulator

# GPU VCore Current Sense



$$V_{out} = 0.75V * (1 + R_a / R_{eq})$$

$$V_{out(min)} = 0.75V * (1 + R_a / R_b)$$

$$R_{eq} = R_b || R_c || R_d || R_e$$

## GPU VCore Setpoints

VID2	VID1	VID0	C	D	E	State
0	0	0	-	-	-	1.050V (rsvd state)
0	0	1	Y	-	-	1.050V (max batt)
0	1	1	Y	Y	-	1.125V (balanced)
1	1	1	Y	Y	Y	1.250V (max perf)

All other states not defined

## GPU (G84M) Core Supply

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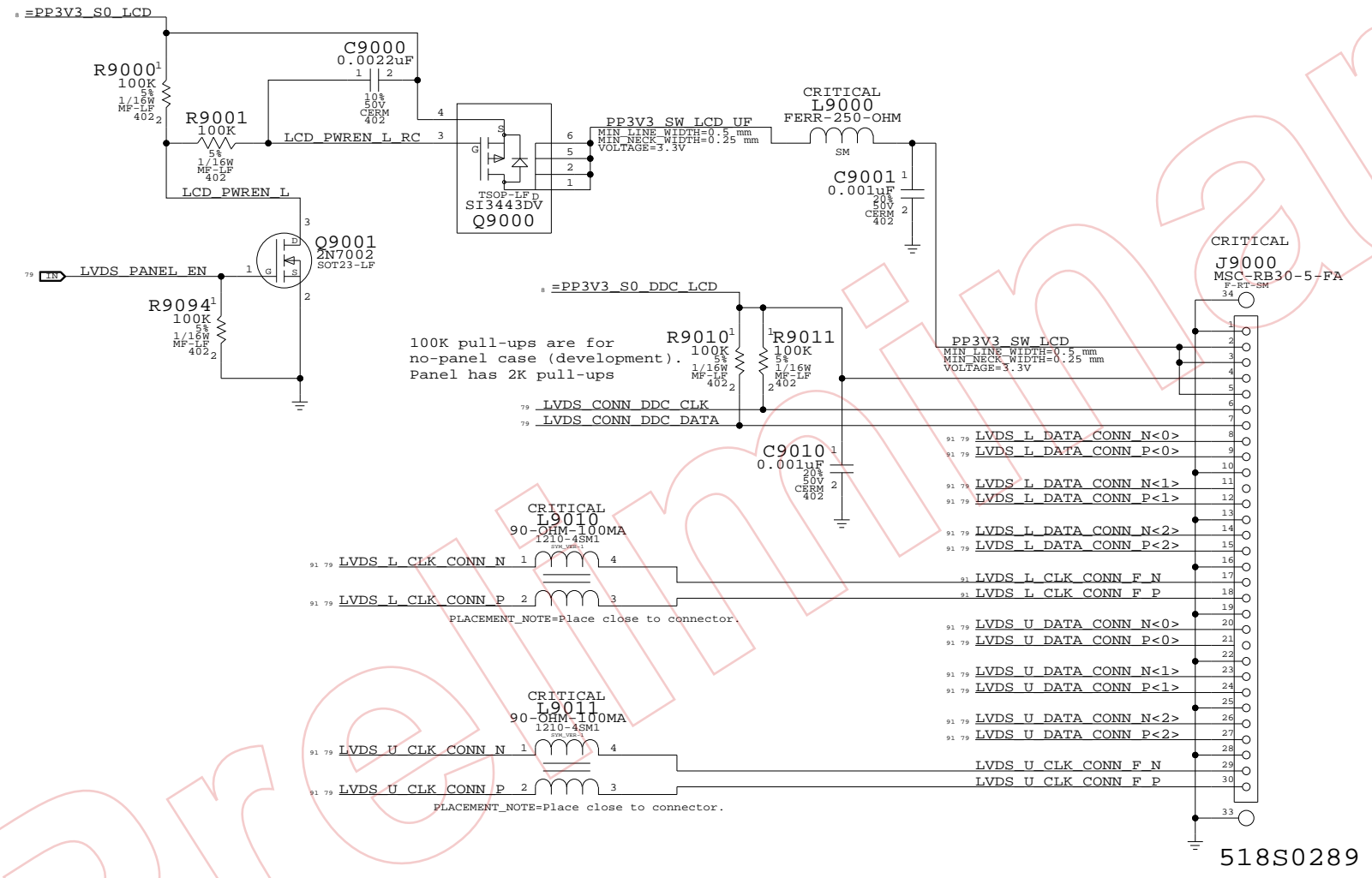
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NONE	89	109	



# LCD (LVDS) INTERFACE

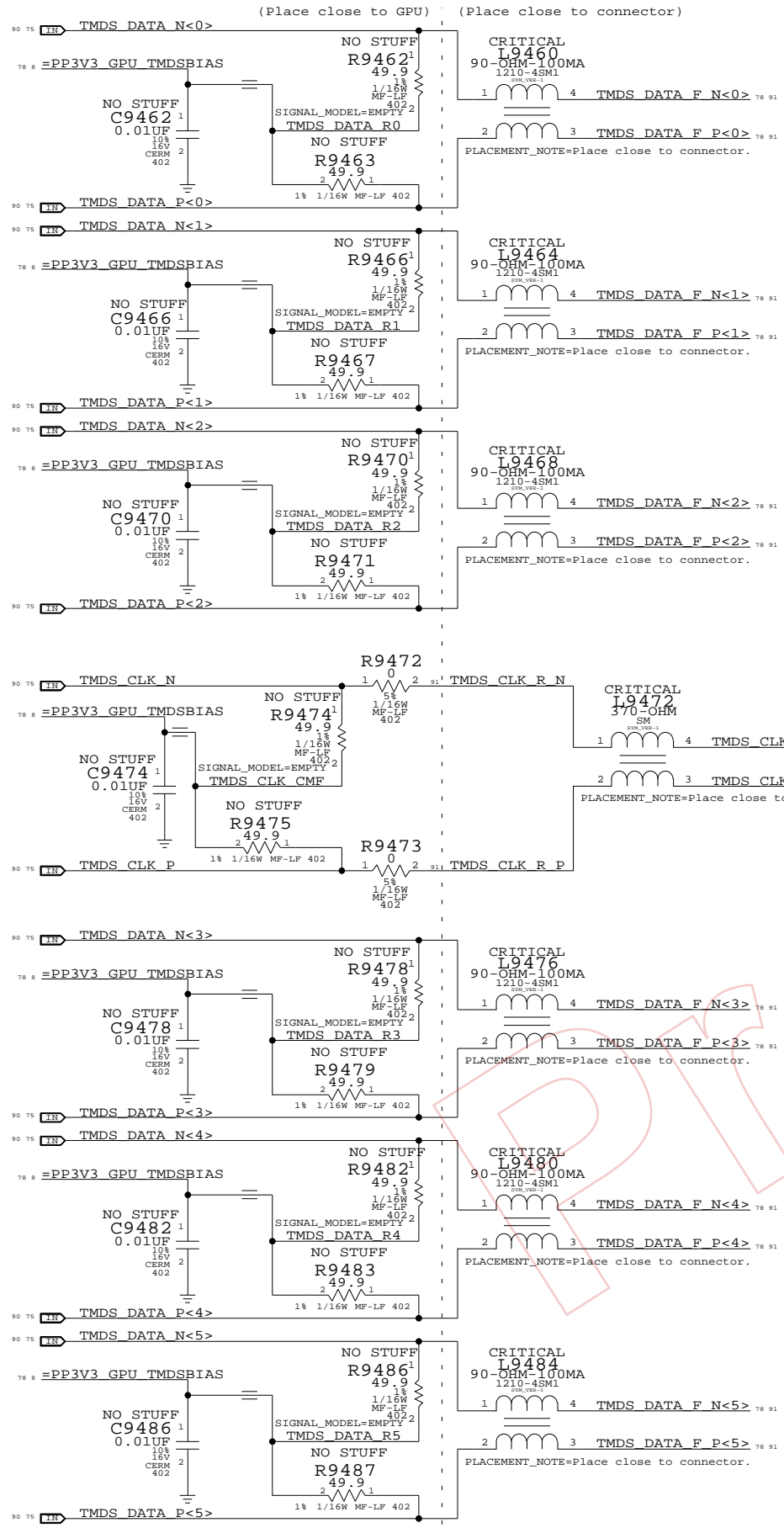


518S0289

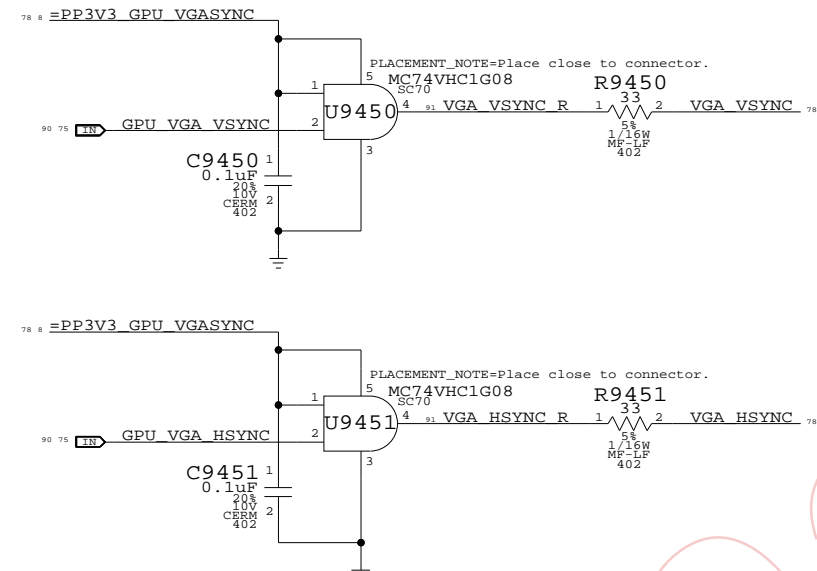
**LVDS Display Connector**  
 SYNC\_MASTER=M75\_MLB SYNC\_DATE=03/19/2007  
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NONE		90	109

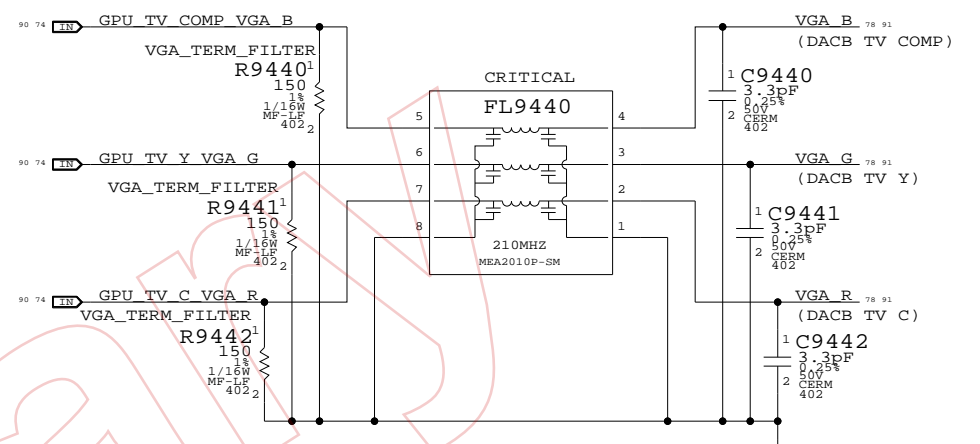
# TMDS Filtering



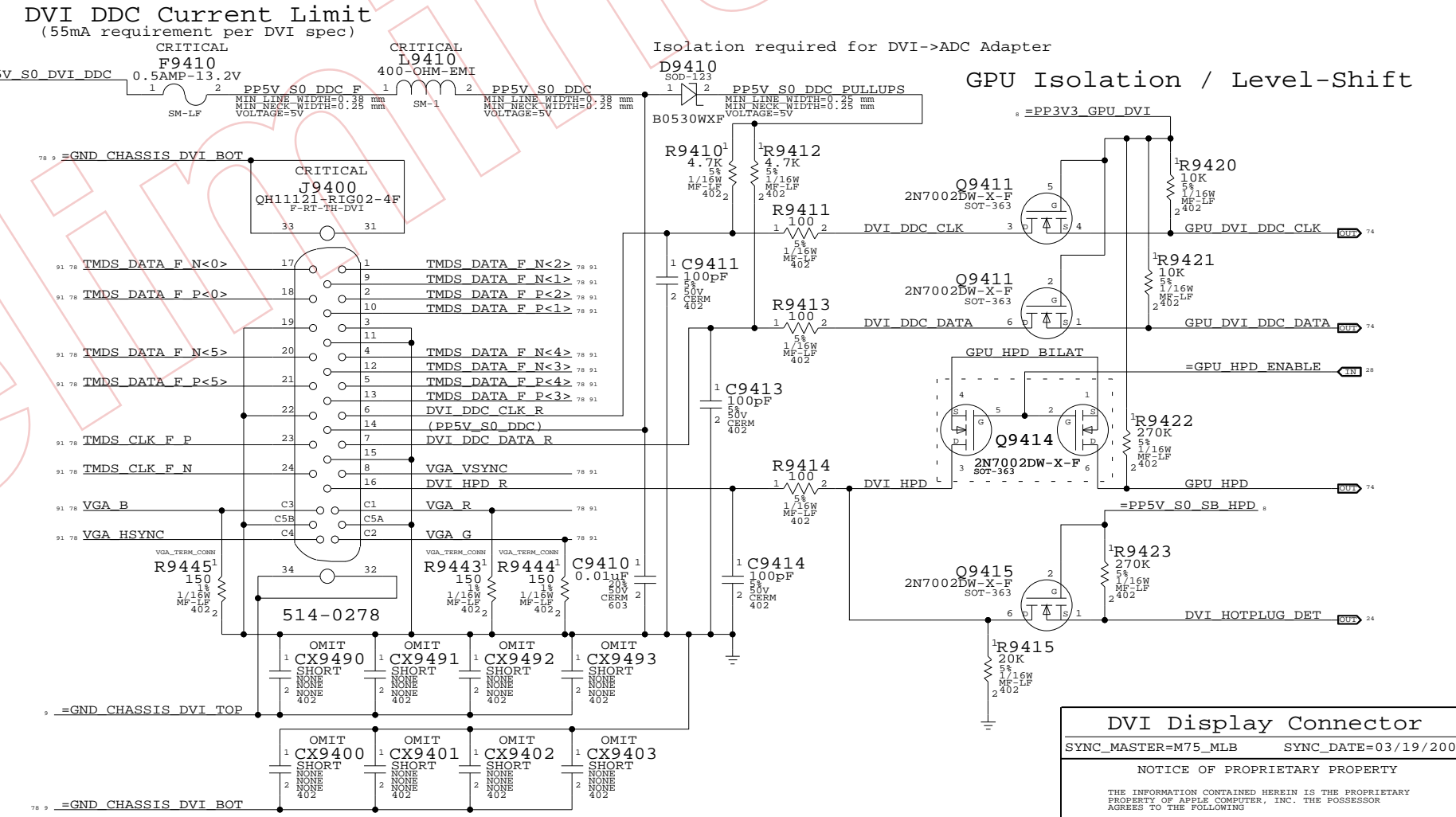
# VGA SYNC Buffers



# ANALOG FILTERING PLACE CLOSE TO CONNECTOR



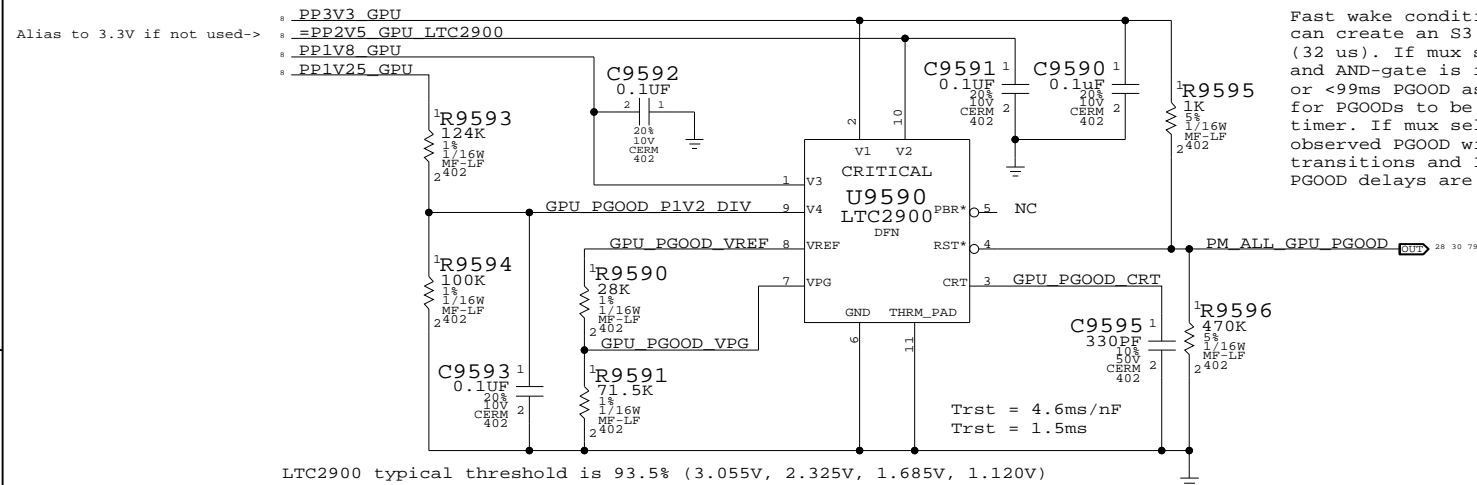
# DVI INTERFACE



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# PGOOD Monitor for GPU Rails

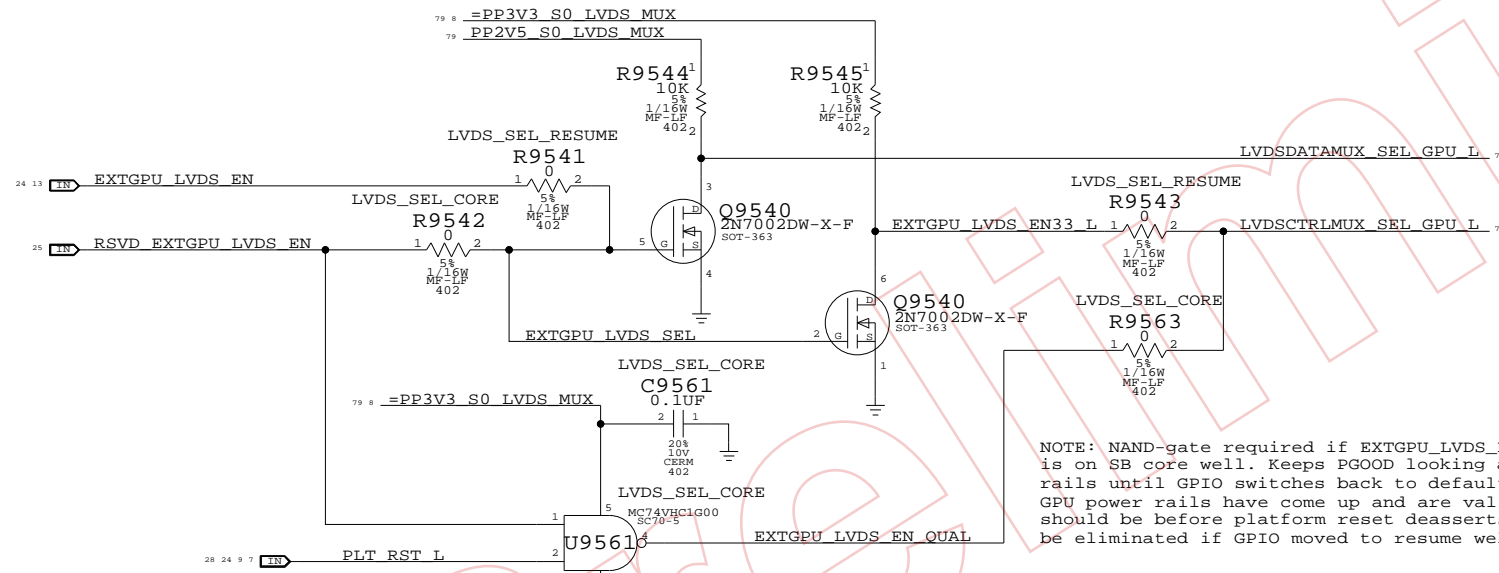
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit



Fast wake condition is worst case. ICHx can create an S3 duration of 1 RTC clock (32 us). If mux select is on core well and AND-gate is implemented, glitch filter or <99ms PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If mux select on resume well, then observed PGOOD will not change during S3 transitions and ICHx will honor whatever PGOOD delays are provided.

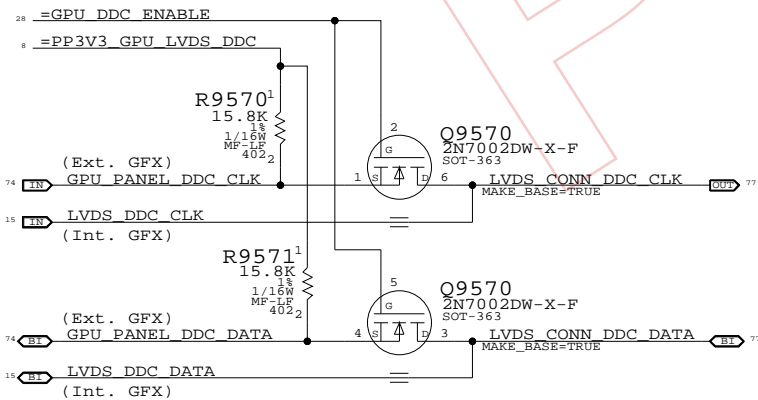
LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

# Mux Select Conditioning

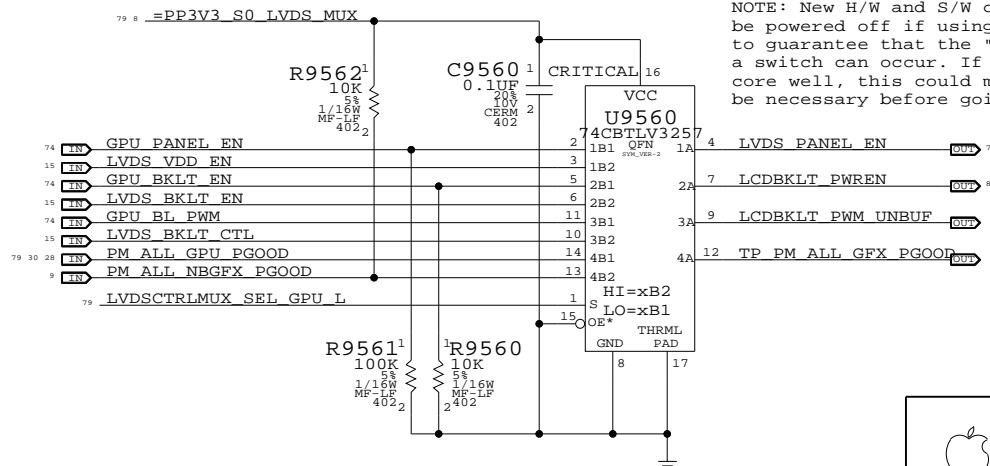


NOTE: NAND-gate required if EXTGPU LVDS\_EN GPIO is on SB core well. Keeps PGOOD looking at non-GPU rails until GPIO switches back to default state and GPU power rails have come up and are valid (which should be before platform reset deasserts). Could be eliminated if GPIO moved to resume well.

# GPU DDC Pass FETs

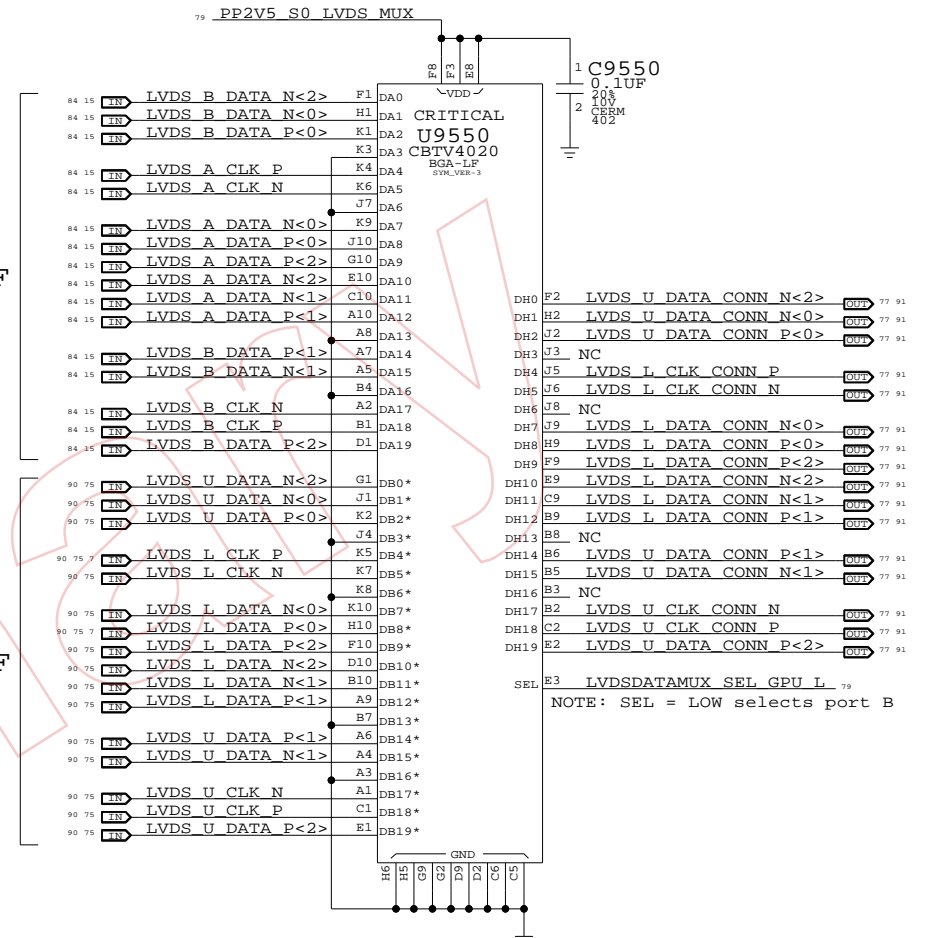


# Panel/Backlight Control Mux

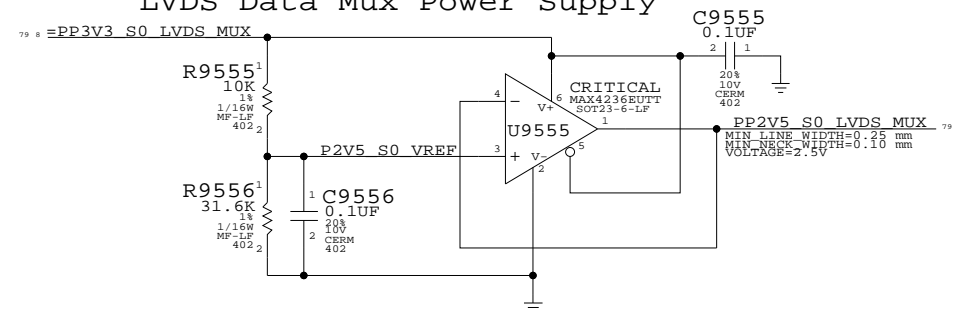


NOTE: New H/W and S/W challenge since NB gfx might be powered off if using external GPU. S/W will have to guarantee that the "other" device is ready before a switch can occur. If mux select GPIO is still on a core well, this could mean powering up IG supply will be necessary before going to sleep to keep PGOODs valid.

# LVDS I/F Mux



# LVDS Data Mux Power Supply



# LVDS Interface Mux

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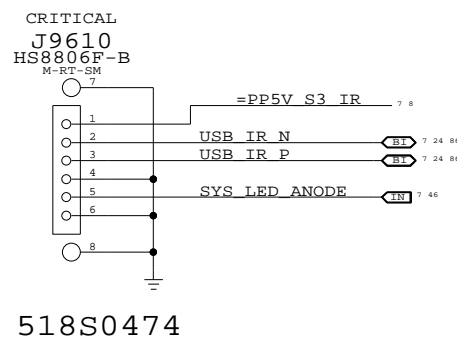
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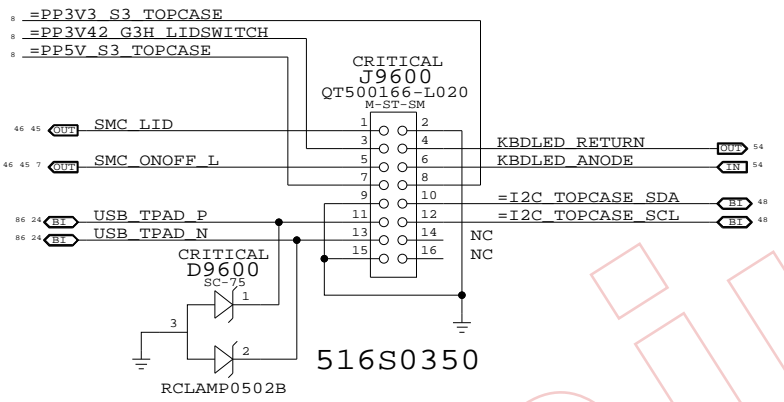
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### IR & Sleep LED Connector



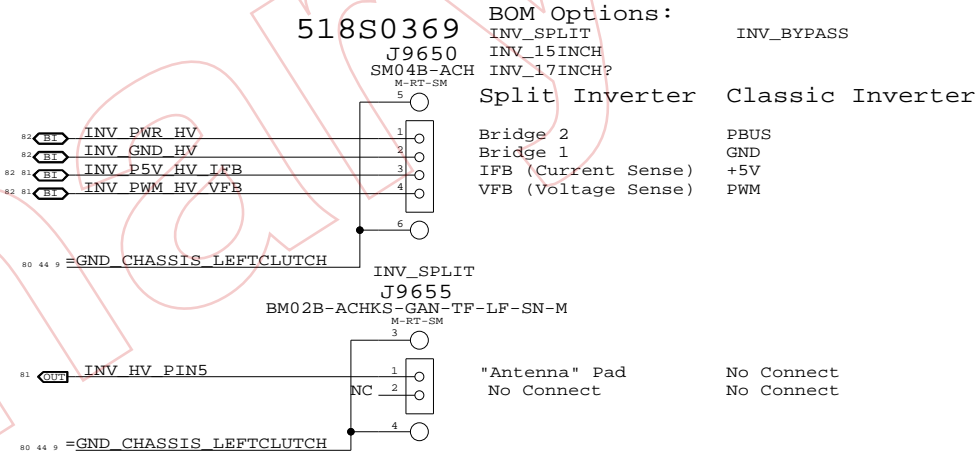
518S0474

### Top-Case Connector



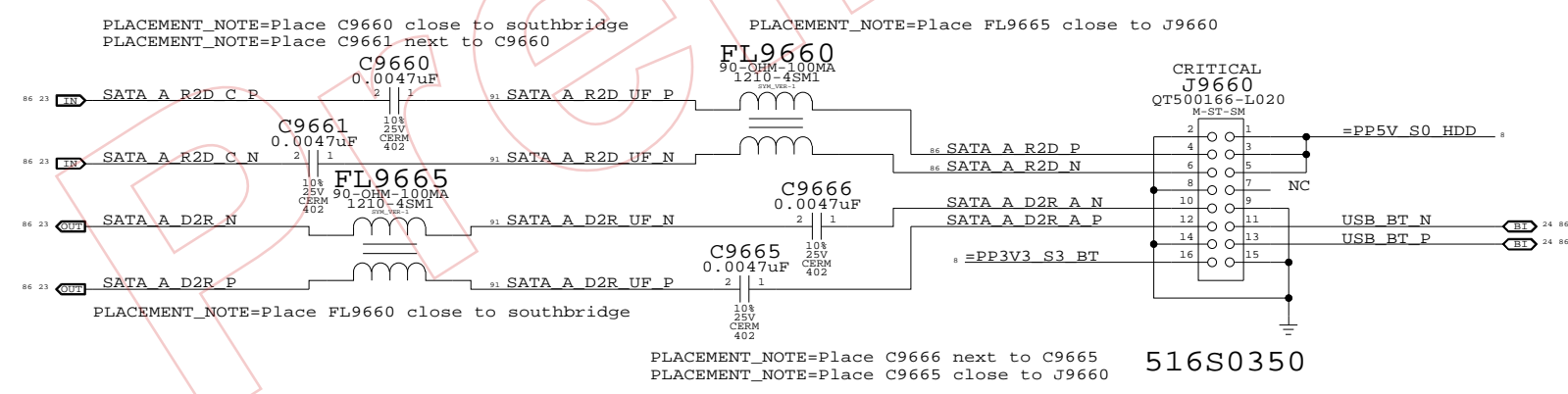
516S0350

### Inverter Connectors



518S0487

### Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

#### M76 Specific Connectors

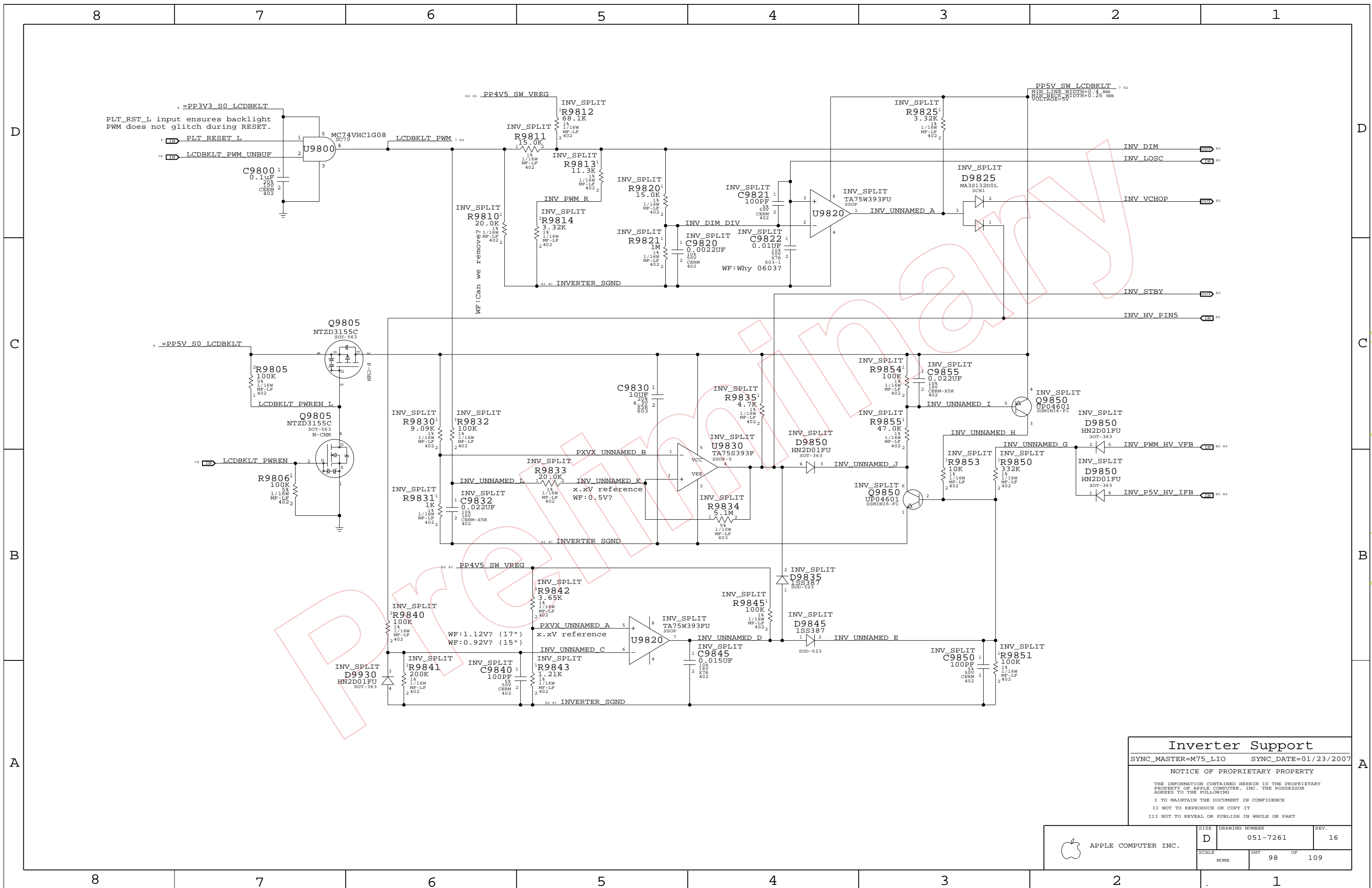
SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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SCALE	SHT	OF	REV.
NONE	96	109	





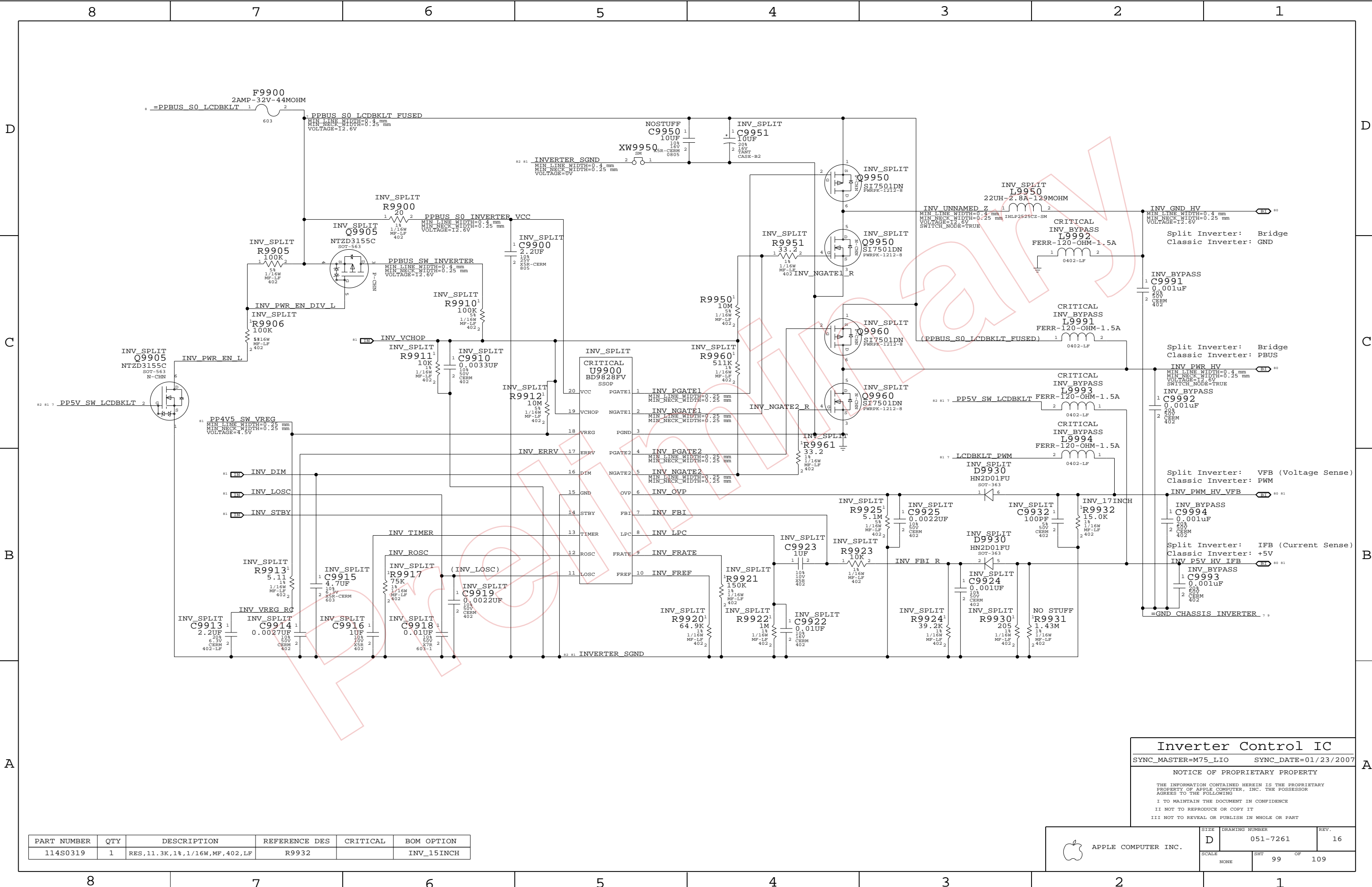
**Inverter Support**  
 SYNC\_MASTER=M75\_LIO SYNC\_DATE=01/23/2007

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### Inverter Control IC

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0319	1	RES, 11.3K, 1%, 1/16W, MF, 402, LF	R9932		INV_15INCH

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
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SCALE	SHT 99 OF 109		
NONE			

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### FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended. Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs. Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs. DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer. Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1. NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

### CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2T01	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended. Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

### CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB ADS L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BNR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BPRI L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB BRQ0 L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DBSY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DEFER L	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DPWR L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB DRDY L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HIT L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB HITM L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB LOCK L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB RS L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB TRDY L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB CPURST L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB D L<15..0>	7 10 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB DINV L<0>	7 10 14
FSB_DSTR0	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<0>	7 10 14
FSB_DSTR0	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB D L<31..16>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB DINV L<1>	7 10 14
FSB_DSTR1	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<1>	7 10 14
FSB_DSTR1	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB D L<47..32>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB DINV L<2>	7 10 14
FSB_DSTR2	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<2>	7 10 14
FSB_DSTR2	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB D L<63..48>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB DINV L<3>	7 10 14
FSB_DSTR3	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L P<3>	7 10 14
FSB_DSTR3	FSB_DSTR_55S	FSB_DSTR	FSB DSTB L N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB A L<16..3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB REQ L<4..0>	7 10 14
FSB_ADSTR0	FSB_55S	FSB_ADSTR	FSB ADSTB L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB A L<35..17>	7 10 14
FSB_ADSTR1	FSB_55S	FSB_ADSTR	FSB ADSTB L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU IERR L	10
CPU_FERR_L	CPU_55S		CPU FERR L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2T01	CPU PROCHOT L	10 46 59
CPU_PWRGD	CPU_55S		CPU PWRGD	7 10 13 23
CPU_FROM_SB	CPU_55S		CPU INTR	10 23
CPU_FROM_SB	CPU_55S		CPU NMI	10 23
CPU_FROM_SB	CPU_55S		CPU A20M L	10 23
CPU_FROM_SB	CPU_55S		CPU DPSTP L	7 10 23
CPU_FROM_SB	CPU_55S		CPU IGNE L	10 23
CPU_INIT_L	CPU_55S		CPU INIT L	10 23 47
CPU_FROM_SB	CPU_55S		CPU SMI L	10 23
CPU_FROM_SB	CPU_55S		CPU STPCLK L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2T01	PM THRMTRIP L	10 16 23 46
FSB_CPUSLP_L	CPU_55S		FSB CPUSLP L	7 10 14
PM_DPRSLEVR	CPU_55S	CPU_2T01	PM DPRSLPVR	7 16 25 59
(See above)	CPU_55S	CPU_2T01	IMVP DPRSLPVR	7 59
CPU_BSEL0	CPU_55S	CPU_2T01	CPU BSEL<0>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2T01	CPU BSEL<1>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2T01	CPU BSEL<2>	10 30
(See above)	CPU_55S	CPU_2T01	NB BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2T01	CPU DPRSTP L	7 10 16 23 59
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP TCK	10 13
XDP_TEST_L	CPU_55S	CPU_ITP	XDP TRST L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP BPM L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP BPM L<5>	10 13
CLK_FSB_100D	CLK_FSB	CLK_FSB	XDP CLK P	13 30 88
CLK_FSB_100D	CLK_FSB	CLK_FSB	XDP CLK N	13 30 88
(FSB_CPURST_L)	CPU_55S	CPU_ITP	XDP CPURST L	13
CPU_55S	CPU_2T01		CPU VID<6..0>	11 12
CPU_55S	CPU_2T01		IMVP6 VID<6..0>	7 12 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11 59
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11 59
CPU_27P4S	CPU_VCCSENSE		IMVP6 VSEN P	59
CPU_27P4S	CPU_VCCSENSE		IMVP6 VSEN N	59

### CPU/FSB Constraints

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007

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NONE	100	109

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	20 MIL	?
CRT	*	25 MIL	?
CRT_2CRT	*	20 MIL	?
CRT_SYNC	*	25 MIL	?
CRT_SYNC2SYNC	*	20 MIL	?
TVDAC	*	25 MIL	?
TVDAC_2TVDAC	*	20 MIL	?

DG Says 40 mil spacing minimum

DG Says 30 mil spacing minimum

DG Says 40 mil spacing minimum

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC


LVDS signals are 100-ohm +/- 20% differential impedance.  
 CRT & TVDAC signal single-ended impedance varies by location:  
 - 37.5-ohm +/- 15% from GMCH to first termination resistor.  
 - 50-ohm +/- 15% from first to second termination resistor.  
 - 55-ohm +/- 15% from second termination resistor to connector.  
 CRT\_HSYNC/CRT\_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG R2D P<15..0>
	PCIE_100D	PCIE	PEG R2D N<15..0>
	PCIE_100D	PCIE	PEG R2D C P<15..0>
	PCIE_100D	PCIE	PEG R2D C N<15..0>
PEG_D2R	PCIE_100D	PCIE	PEG D2R P<15..0>
	PCIE_100D	PCIE	PEG D2R N<15..0>
	PCIE_100D	PCIE	PEG D2R C P<15..0>
	PCIE_100D	PCIE	PEG D2R C N<15..0>
DMI_N2S	DMI_100D	DMI	DMI N2S P<3..0>
	DMI_100D	DMI	DMI N2S N<3..0>
DMI_S2N	DMI_100D	DMI	DMI S2N P<3..0>
	DMI_100D	DMI	DMI S2N N<3..0>
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK P
LVDS_A_CLK	LVDS_100D	LVDS	LVDS A CLK N
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA P<2..0>
LVDS_A_DATA	LVDS_100D	LVDS	LVDS A DATA N<2..0>
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA P<3>
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS A DATA N<3>
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK P
LVDS_B_CLK	LVDS_100D	LVDS	LVDS B CLK N
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA P<2..0>
LVDS_B_DATA	LVDS_100D	LVDS	LVDS B DATA N<2..0>
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA P<3>
LVDS_B_DATA3	LVDS_100D	LVDS	LVDS B DATA N<3>
LVDS_IBG		LVDS	LVDS IBG
CRT_TVO_IREF		CRT	CRT TVO IREF
CRT_RED	CRT_50S	CRT	CRT RED
CRT_GREEN	CRT_50S	CRT	CRT GREEN
CRT_BLUE	CRT_50S	CRT	CRT BLUE
CRT_SYNC	CRT_55S	CRT_SYNC	CRT HSYNC_R
CRT_SYNC	CRT_55S	CRT_SYNC	CRT VSYNC_R
TV_A_DAC	CRT_50S	TVDAC	TV A DAC
TV_B_DAC	CRT_50S	TVDAC	TV B DAC
TV_C_DAC	CRT_50S	TVDAC	TV C DAC

Preliminary

NB Constraints		
SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	
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SCALE	SHT	OF	
NONE	101	109	



## DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Need to support MEM\*-style wildcards!

## Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK P<2..0>
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK N<2..0>
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_CS L<1..0>
MEM_A_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A A<14..0>
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A BS<2..0>
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A RAS L
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A CAS L
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A WE L
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM A DQ<7..0>
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM A DQ<15..8>
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM A DQ<23..16>
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM A DQ<31..24>
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM A DQ<39..32>
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM A DQ<47..40>
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM A DQ<55..48>
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM A DQ<63..56>
MEM_A_DM0	MEM_55S	MEM_DATA	MEM A DM<0>
MEM_A_DM1	MEM_55S	MEM_DATA	MEM A DM<1>
MEM_A_DM2	MEM_55S	MEM_DATA	MEM A DM<2>
MEM_A_DM3	MEM_55S	MEM_DATA	MEM A DM<3>
MEM_A_DM4	MEM_55S	MEM_DATA	MEM A DM<4>
MEM_A_DM5	MEM_55S	MEM_DATA	MEM A DM<5>
MEM_A_DM6	MEM_55S	MEM_DATA	MEM A DM<6>
MEM_A_DM7	MEM_55S	MEM_DATA	MEM A DM<7>
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS P<0>
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM A DQS N<0>
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS P<1>
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM A DQS N<1>
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS P<2>
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM A DQS N<2>
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS P<3>
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM A DQS N<3>
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS P<4>
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM A DQS N<4>
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS P<5>
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM A DQS N<5>
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS P<6>
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM A DQS N<6>
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS P<7>
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM A DQS N<7>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK P<5..3>
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK N<5..3>
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_CS L<3..2>
MEM_B_CNTRL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B A<14..0>
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B BS<2..0>
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B RAS L
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B CAS L
MEM_B_CMD	MEM_55S	MEM_CMD	MEM B WE L
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM B DQ<7..0>
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM B DQ<15..8>
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM B DQ<23..16>
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM B DQ<31..24>
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM B DQ<39..32>
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM B DQ<47..40>
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM B DQ<55..48>
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM B DQ<63..56>
MEM_B_DM0	MEM_55S	MEM_DATA	MEM B DM<0>
MEM_B_DM1	MEM_55S	MEM_DATA	MEM B DM<1>
MEM_B_DM2	MEM_55S	MEM_DATA	MEM B DM<2>
MEM_B_DM3	MEM_55S	MEM_DATA	MEM B DM<3>
MEM_B_DM4	MEM_55S	MEM_DATA	MEM B DM<4>
MEM_B_DM5	MEM_55S	MEM_DATA	MEM B DM<5>
MEM_B_DM6	MEM_55S	MEM_DATA	MEM B DM<6>
MEM_B_DM7	MEM_55S	MEM_DATA	MEM B DM<7>
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS P<0>
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM B DQS N<0>
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS P<1>
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM B DQS N<1>
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS P<2>
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM B DQS N<2>
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS P<3>
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM B DQS N<3>
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS P<4>
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM B DQS N<4>
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS P<5>
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM B DQS N<5>
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS P<6>
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM B DQS N<6>
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS P<7>
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM B DQS N<7>

### Memory Constraints

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007

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SCALE	SHT	OF
NONE	102	109

### Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

### HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

### USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

### Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE PDD<15..0> 23 42
IDE_PDA	IDE_55S	IDE	IDE PDA<2..0> 23 42
IDE_PDCS	IDE_55S	IDE	IDE PDCS1 L 23 42
IDE_PDCS	IDE_55S	IDE	IDE PDCS3 L 23 42
IDE_PDIOW	IDE_55S	IDE	IDE PDIOW L 23 42
IDE_PDIOR	IDE_55S	IDE	IDE PDIOR L 23 42
IDE_PDDACK	IDE_55S	IDE	IDE PDDACK L 23 42
IDE_PDDREQ	IDE_55S	IDE	IDE PDDREQ 23 42
IDE_PDIORDY	IDE_55S	IDE	IDE PDIORDY 23 42
IDE_IRQ14	IDE_55S	IDE	IDE IRQ14 23 42
IDE_RST_L	IDE_55S	IDE	ODD RST 5VTOL L 24 42
SATA_A_R2D	SATA_100D	SATA	SATA A R2D C P 23 80
SATA_100D	SATA	SATA	SATA A R2D C N 23 80
SATA_100D	SATA	SATA	SATA A R2D P 80
SATA_100D	SATA	SATA	SATA A R2D N 80
SATA_A_D2R	SATA_100D	SATA	SATA A D2R P 23 80
SATA_100D	SATA	SATA	SATA A D2R N 23 80
SATA_100D	SATA	SATA	SATA A D2R C P 80
SATA_100D	SATA	SATA	SATA A D2R C N 80
SATA_B_R2D	SATA_100D	SATA	SATA B R2D C P 23 42
SATA_100D	SATA	SATA	SATA B R2D C N 23 42
SATA_100D	SATA	SATA	SATA B R2D P 23 42
SATA_100D	SATA	SATA	SATA B R2D N 23 42
SATA_B_D2R	SATA_100D	SATA	SATA B D2R P 23 42
SATA_100D	SATA	SATA	SATA B D2R N 23 42
SATA_100D	SATA	SATA	SATA B D2R C P 23 42
SATA_100D	SATA	SATA	SATA B D2R C N 23 42
SATA_C_R2D	SATA_100D	SATA	SATA C R2D C P 23 42
SATA_100D	SATA	SATA	SATA C R2D C N 23 42
SATA_100D	SATA	SATA	SATA C R2D P 23 42
SATA_100D	SATA	SATA	SATA C R2D N 23 42
SATA_C_D2R	SATA_100D	SATA	SATA C D2R P 23 42
SATA_100D	SATA	SATA	SATA C D2R N 23 42
SATA_100D	SATA	SATA	SATA C D2R C P 23 42
SATA_100D	SATA	SATA	SATA C D2R C N 23 42
SATA_RBIAS	SATA_55S	SATA	SATA RBIAS 42
HDA_BIT_CLK	HDA_55S	HDA	HDA BIT CLK 23 34
HDA_55S	HDA	HDA	HDA BIT CLK R 23 34
HDA_SYNC	HDA_55S	HDA	HDA SYNC 23 34
HDA_55S	HDA	HDA	HDA SYNC R 23 34
HDA_RST_L	HDA_55S	HDA	HDA RST L 23 34
HDA_55S	HDA	HDA	HDA RST L R 23 34
HDA_SDIN0	HDA_55S	HDA	HDA SDIN0 23 34
HDA_55S	HDA	HDA	HDA SDIN CODEC 23 34
HDA_SDOUT	HDA_55S	HDA	HDA SDOUT 23 34
HDA_55S	HDA	HDA	HDA SDOUT R 23 34
USB_EXT_A	USB_90D	USB	USB EXT_A P 24 43
USB_90D	USB	USB	USB EXT_A N 24 43
USB_90D	USB	USB	USB EXT_A MUXED P 24 43
USB_90D	USB	USB	USB EXT_A MUXED N 24 43
USB_MINI	USB_90D	USB	USB MINI P 24 34
USB_90D	USB	USB	USB MINI N 24 34
USB_EXTD	USB_90D	USB	USB EXT_D P 24 44
USB_90D	USB	USB	USB EXT_D N 24 44
USB_CAMERA	USB_90D	USB	USB CAMERA P 24 44
USB_90D	USB	USB	USB CAMERA N 24 44
USB_BT	USB_90D	USB	USB BT P 24 80
USB_90D	USB	USB	USB BT N 24 80
USB_TPAD	USB_90D	USB	USB TPAD P 24 80
USB_90D	USB	USB	USB TPAD N 24 80
USB_IR	USB_90D	USB	USB IR P 7 24 80
USB_90D	USB	USB	USB IR N 7 24 80
USB_EXTB	USB_90D	USB	USB EXTB P 24 34
USB_90D	USB	USB	USB EXTB N 24 34
USB_EXCARD	USB_90D	USB	USB EXCARD P 24 34
USB_90D	USB	USB	USB EXCARD N 24 34
USB_EXTC	USB_90D	USB	USB EXTC P 24 34
USB_90D	USB	USB	USB EXTC N 24 34
USB_RBIAS	USB_60S	USB	USB RBIAS 24
SMB_SB_SCL	SMB_55S	SMB	SMB CLK 25 48
SMB_SB_SDA	SMB_55S	SMB	SMB DATA 25 48
SMB_SB_ME_SCL	SMB_55S	SMB	SMB ME CLK 25 48
SMB_SB_ME_SDA	SMB_55S	SMB	SMB ME DATA 25 48
SPI_SCLK	SPI_55S	SPI	SPI SCLK R 24 56
SPI_55S	SPI	SPI	SPI SCLK 56
SPI_55S	SPI	SPI	SPI A SCLK R 56
SPI_55S	SPI	SPI	SPI B SCLK R 56
SPI_SI	SPI_55S	SPI	SPI SI R 24 56
SPI_55S	SPI	SPI	SPI SI 56
SPI_55S	SPI	SPI	SPI A SI R 56
SPI_55S	SPI	SPI	SPI B SI R 56
SPI_SO	SPI_55S	SPI	SPI SO 24 56
SPI_55S	SPI	SPI	SPI A SO R 56
SPI_55S	SPI	SPI	SPI B SO 56
SPI_55S	SPI	SPI	SPI B SO R 56
SPI_CE_L0	SPI_55S	SPI	SPI CE R L<0> 24 56
SPI_55S	SPI	SPI	SPI CE L<0> 56
SPI_CE_L1	SPI_55S	SPI	SPI CE R L<1> 24 56
SPI_55S	SPI	SPI	SPI CE L<1> 56

### SB Constraints (1 of 2)

SYNC\_MASTER=T9\_NOME SYNC\_DATE=01/25/2007

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	D	051-7261	16
SCALE	SHT	OF	
NONE	103	109	

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### PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

### Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	=STANDARD	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

### Ethernet (Yukon) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MILS	?

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	24 38
PCI_AD19	PCI_55S	PCI	PCI AD<19>	24 38
PCI_AD20	PCI_55S	PCI	PCI AD<20>	24 38
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	24 38
PCI_AD	PCI_55S	PCI	PCI PAR	24 38
PCI_C_BE_L	PCI_55S	PCI	PCI C BE L<3..0>	24 38
PCI_CNTRL	PCI_55S	PCI	PCI IRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI DEVSEL_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI PERR_L	24 38
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	24
PCI_CNTRL	PCI_55S	PCI	PCI SERR_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI STOP_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI TRDY_L	24 38
PCI_CNTRL	PCI_55S	PCI	PCI FRAME_L	24 38
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW REQ_L	24 38
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW GNT_L	24 38
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	24 38
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	24
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	24
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	24
INT_PIRQA_L	PCI_55S	PCI	INT PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT PIROC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT PIROD_L	24 38
INT_PIRQE_L	PCI_55S	PCI	INT PIRQE_L	24
INT_PIRQF_L	PCI_55S	PCI	INT PIROF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C P	
PCIE_A_R2D	PCIE_100D	PCIE	PCIE A R2D C N	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R P	
PCIE_A_D2R	PCIE_100D	PCIE	PCIE A D2R N	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C P	
PCIE_B_R2D	PCIE_100D	PCIE	PCIE B R2D C N	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R P	
PCIE_B_D2R	PCIE_100D	PCIE	PCIE B D2R N	
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C P	34
PCIE_EXCARD_R2D	PCIE_100D	PCIE	PCIE EXCARD R2D C N	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R P	34
PCIE_EXCARD_D2R	PCIE_100D	PCIE	PCIE EXCARD D2R N	34
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C P	
PCIE_FW_R2D	PCIE_100D	PCIE	PCIE FW R2D C N	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R P	
PCIE_FW_D2R	PCIE_100D	PCIE	PCIE FW D2R N	
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C P	24 34
PCIE_MINI_R2D	PCIE_100D	PCIE	PCIE MINI R2D C N	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R P	24 34
PCIE_MINI_D2R	PCIE_100D	PCIE	PCIE MINI D2R N	24 34
GLAN_COMP			GLAN COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK NB CLK	16 25
CLINK_NB	CLINK_55S	CLINK	CLINK NB DATA	16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK NB RESET_L	16 25
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN CLK	
CLINK_WLAN	CLINK_55S	CLINK	CLINK WLAN DATA	
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK WLAN RESET_L	
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB CLINK VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB CLINK VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB CLINK VREF1	25
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C P	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D C N	24 35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D P	35
PCIE_ENET_R2D	PCIE_100D	PCIE	PCIE ENET R2D N	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R P	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R N	24 35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C P	35
PCIE_ENET_D2R	PCIE_100D	PCIE	PCIE ENET D2R C N	35
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<0>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<1>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<2>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI P<3>	35 37
ENET_MDI	ENET_100D	ENET_MDI	ENET MDI N<3>	35 37

### SB Constraints (2 of 2)

SYNC\_MASTER=T9\_NAME SYNC\_DATE=01/25/2007

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D	051-7261	16
SCALE	SHT	OF
NONE	104	109

### Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

### Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CK505_CPU0	CLK_FSB_100D	CLK_FSB	CK505_CPU0 P	29 30
CK505_CPU0	CLK_FSB_100D	CLK_FSB	CK505_CPU0 N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1 P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1 N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2 ITP_SRC10 P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2 ITP_SRC10 N	29 30
CK505_PCIE0	CLK_MED_55S	CLK_MED	CK505_PCIE0 CLK ITPEN	29 30
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1 CLK	29 30
CK505_PCIE1	CLK_MED_55S	CLK_MED	CK505_PCIE1 CLK	29 30
CK505_PCIE2	CLK_MED_55S	CLK_MED	CK505_PCIE2 CLK	29 30
CK505_PCIE3	CLK_MED_55S	CLK_MED	CK505_PCIE3 CLK	29 30
CK505_PCIE4	CLK_MED_55S	CLK_MED	CK505_PCIE4 CLK	29 30
CK505_PCIE5	CLK_MED_55S	CLK_MED	CK505_PCIE5 CLK FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96 27M P	29 30
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96 27M N	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS P	29 30
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1 P	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1 N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2 P	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2 N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3 P	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3 N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4 P	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4 N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5 P	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5 N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6 P	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6 N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7 P	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7 N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8 P	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8 N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU P	7 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU N	7 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK P	13 30 83
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK N	13 30 83
(CK505_PCIE0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 47
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	24 30
(CK505_PCIE1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	30 38
(CK505_PCIE2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	30 45
(CK505_PCIE3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	30 45
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTRL	25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT P	7
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT N	7
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS P	7 22 30
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS N	7 22 30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M P	9
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M N	9
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI P	24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI N	24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD P	30 34
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD N	30 34
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA P	23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA N	23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI N	30 34
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET P	30 35
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET N	30 35

### SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48

### Clock & SMC Constraints

SYNC\_MASTER=T9\_NAME SYNC\_DATE=01/25/2007

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	D	051-7261	16
SCALE	SHT	OF	
NONE	105	109	



### FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

### FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
EW_D_CTL	EW_55S	FW	FW LINK<7..0>
EW_D_CTL	EW_55S	FW	FW CTL<1..0>
EW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_LCLK
EW_L_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_LCLK 38 39
EW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW LINK_PCLK 38 39
EW_P_CLK	CLK_MED_55S	CLK_MED	CLKFW PHY_PCLK 38 39
EW_LKON	EW_55S	FW	FW LKON
EW_LKON	EW_55S	FW	FW LKON R 38 39
EW_LPS	EW_55S	FW	FW LPS 38 39
EW_LREQ	EW_55S	FW	FW LREQ 38 39
EW_PINT	EW_55S	FW	FW PINT 38 39
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW_XI_R
EWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M FW_XI
EW_0_TPA	EW_110D	EW_TP	FW_0 TPA_P 39 41
EW_0_TPA	EW_110D	EW_TP	FW_0 TPA_N 39 41
EW_0_TPB	EW_110D	EW_TP	FW_0 TPB_P 39 41
EW_0_TPB	EW_110D	EW_TP	FW_0 TPB_N 39 41
EW_1_TPA	EW_110D	EW_TP	FW_1 TPA_P 39 41
EW_1_TPA	EW_110D	EW_TP	FW_1 TPA_N 39 41
EW_1_TPB	EW_110D	EW_TP	FW_1 TPB_P 39 41
EW_1_TPB	EW_110D	EW_TP	FW_1 TPB_N 39 41
Port 2 Not Used			

Preliminary

FireWire Constraints		
SYNC_MASTER=T9_NOME	SYNC_DATE=01/25/2007	
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	D	051-7261	16
SCALE	SHT	OF	
NONE	106	109	

GDDR3 Frame Buffer Signal Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include GDDR3\_40R50SE, GDDR3\_50SE, and GDDR3\_80D.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include GDDR3\_CLK, GDDR3\_CMD, GDDR3\_DATA, and GDDR3\_DQS.

Video Signal Constraints

Table with 8 columns: PHYSICAL\_RULE\_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include TMDS\_100D, VGA\_50S, and VGA\_55S.

Table with 4 columns: SPACING\_RULE\_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include TMDS, VGA, and VGA\_SYNC.

GDDR3 FB A/B Net Properties

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, SPACING, and a net name. Lists various net types like FB\_A\_CLK\_P, FB\_AB\_CMD, FB\_AB\_CMD\_PD, FB\_A\_CMD, FB\_A\_WDQS0, etc.

GDDR3 FB C/D Net Properties

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, SPACING, and a net name. Lists various net types like FB\_C\_CLK\_P, FB\_CD\_CMD, FB\_CD\_CMD\_PD, FB\_C\_CMD, FB\_C\_WDQS0, etc.

G84M Net Properties

Table with 4 columns: ELECTRICAL\_CONSTRAINT\_SET, PHYSICAL, SPACING, and a net name. Lists various net types like GPU\_CLK27M, LVDS\_L\_CLK\_P, TMDS\_CLK\_P, GPU\_VGA\_R, etc.

GPU (G84M) Constraints

SYNC\_MASTER=M75\_MLB SYNC\_DATE=01/26/2007

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Table with 3 columns: SIZE, DRAWING NUMBER, REV. Row 1: D, 051-7261, 16. Row 2: SCALE NONE, SHEET 107 OF 109.



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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1T01_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V8_MEM	*	PWR_P2MM
MEM_CMD	PP1V8_MEM	*	PWR_P2MM
MEM_CTRL	PP1V8_MEM	*	PWR_P2MM
MEM_DATA	PP1V8_MEM	*	PWR_P2MM
MEM_DQS	PP1V8_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
DMI	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

### Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM	2.54 MM	OVERRIDE	OVERRIDE
MEM_70D	ISL10			0.100 MM	2.54 MM		
MEM_85D	ISL4, ISL10			0.100 MM	2.54 MM		

### Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_100D	*	100_DIFF_BGA
LVDS_100D	*	100_DIFF_BGA
TMDS_100D	*	100_DIFF_BGA

### SIM Card Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WWAN_SIM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
WWAN_SIM	*	=2:1_SPACING	?

### M76 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_P
(PCIE_EXCARD)	PCIE_100D	PCIE	PCIE_EXCARD_R2D_N
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_P
(PCIE_MINI)	PCIE_100D	PCIE	PCIE_MINI_R2D_N
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3..0>
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3..0>
	ENET_100D	ENETCONN	ENETCONN_P<3..0>
	ENET_100D	ENETCONN	ENETCONN_N<3..0>
	FW_110D	FW_TP	FW_PORT0_TPA_FL_P
	FW_110D	FW_TP	FW_PORT0_TPA_FL_N
	FW_110D	FW_TP	FW_PORT0_TPB_FL_P
	FW_110D	FW_TP	FW_PORT0_TPB_FL_N
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_P
(SATA_A_R2D)	SATA_100D	SATA	SATA_A_R2D_UF_N
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_P
(SATA_A_D2R)	SATA_100D	SATA	SATA_A_D2R_UF_N
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_P
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_N
(USB_EXT_A)	USB_90D	USB	USB2_RT_P
(USB_EXT_A)	USB_90D	USB	USB2_RT_N
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_P
(USB_EXT_D)	USB_90D	USB	USB_WWAN_F_N
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_P
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_F_N
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	GFXIMVP6_VSEN_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	NBCOREISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V8ISNS_P
SENSE_DIFFPAIR	SENSE_1T01_55S	SENSE	P1V25ISNS_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THERMSNS_D2_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	CPU_THERMD_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_THERMSNS_D_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	GPU_TDIODE_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	HSTHERMSNS_D_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	REMTHERMSNS_DX_P
THERM_DIFFPAIR	THERM_1T01_55S	THERM	RSF_THERMSNS_D_P
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_P
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_F_N
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_P
	LVDS_100D	LVDS	LVDS_L_CLK_CONN_N
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_P<3..0>
	LVDS_100D	LVDS	LVDS_L_DATA_CONN_N<3..0>
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_P
	LVDS_100D	LVDS	LVDS_U_CLK_CONN_N
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_P<3..0>
	LVDS_100D	LVDS	LVDS_U_DATA_CONN_N<3..0>
	TMDS_100D	TMDS	TMDS_CLK_R_P
	TMDS_100D	TMDS	TMDS_CLK_R_N
	TMDS_100D	TMDS	TMDS_CLK_F_P
	TMDS_100D	TMDS	TMDS_CLK_F_N
	TMDS_100D	TMDS	TMDS_DATA_F_P<5..0>
	TMDS_100D	TMDS	TMDS_DATA_F_N<5..0>
(VGA_R_TV_Y)	VGA_50S	VGA	VGA_R
(VGA_G_TV_C)	VGA_50S	VGA	VGA_G
(VGA_B_TV_COMP)	VGA_50S	VGA	VGA_B
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC_R
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC_R
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_HSYNC
(VGA_SYNC)	VGA_55S	VGA_SYNC	VGA_VSYNC
	PP1V8_MEM		=PP1V8_S3M_MEM_A
	PP1V8_MEM		=PP1V8_S3M_MEM_B
	GND		GND
	SB_POWER		PP3V3_S5
	SB_POWER		PP3V3_S0
	SB_POWER		PP1V5_S0
WWAN_SIM	WWAN_SIM		WWAN_SIM_CLOCK
WWAN_SIM	WWAN_SIM		WWAN_SIM_DATA

### M76 Specific Constraints

SYNC\_MASTER=M76\_MLB SYNC\_DATE=02/02/2007

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	D	051-7261	16
SCALE	NONE	SHT	108 OF 109

# M75/M76 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA			MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	ISL2, ISL11	Y	0.250 MM	0.076 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.125 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.149 MM	0.149 MM		0.125 MM	0.125 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.115 MM	0.115 MM		0.125 MM	0.125 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3, ISL4	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL9, ISL10	Y	0.101 MM	0.101 MM		0.125 MM	0.125 MM
85_OHM_DIFF	ISL2, ISL11	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM
85_OHM_DIFF	TOP, BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y		0.075 MM			0.125 MM
100_DIFF_BGA	ISL2, ISL11	Y		0.085 MM			0.140 MM
100_DIFF_BGA	TOP, BOTTOM	Y		0.085 MM			0.140 MM

NOTE: 100\_DIFF\_BGA is for select 100-ohm differential pairs with routing difficulties through BGAs. Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.

## M75/M76 Rule Definitions

SYNC\_MASTER=M76\_MLB SYNC\_DATE=02/02/2007

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