3. All crystals & oscillator values are in hertz.

2. All capacitance values are in microfarads.
### Schematic / PCB #s

<table>
<thead>
<tr>
<th>Schematic / PCB #s</th>
<th>Description</th>
<th>Revision Level</th>
<th>PCB Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>SILENT, SERIAL, MLR</td>
<td>03A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>POST-RAMP-DIMM35</td>
<td>07A</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### BOARD STACK-UP AND CONSTRUCTION

#### Top

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>Layer</th>
<th>Thickness (mil)</th>
<th>Trace Width (mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GROUND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SIGNAL (High Speed)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>POWER</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GROUND</td>
<td></td>
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<tr>
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</tbody>
</table>

#### Bottom

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>Layer</th>
<th>Thickness (mil)</th>
<th>Trace Width (mil)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIGNAL</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### MLB STACKUP

- **Layer**: CONFORMAL_COAT, GROUND, SIGNAL, POWER
- **Thickness (mil)**: 0.018, 0.07, 0.076, 0.076, 0.076, 0.076, 0.076, 0.076, 0.076, 0.076
- **Trace Width (mil)**: 0.1, 0.07, 0.076, 0.076, 0.07, 0.07, 0.076, 0.076, 0.076, 0.076

### TOTAL

Total thickness: 1.276 mils

### SIGNAL ALIASES

- **Signal Aliases**: M42B, M42A, 5V3V3S3_SKIP, 5V3V3S3_CONT, 1V51V05S0_SKIP, 1V51V05S0_CONT, BETTER-KIONIX, BEST-KIONIX, GOOD, BETTER, POST-RAMP-DIMM35, CONFORMAL_COAT, POWER, SIGNAL

### CONFORMAL COAT

- **Layer**: MLB STACKUP
- **Thickness (mil)**: 0.018
- **Trace Width (mil)**: 0.1

### CONFIGURATION OPTIONS

- **Sync Date**: 07/18/2005
- **Configuration Options**: SMC, USB, PSOC+W/USB, 56P, MLF, CY8C24794

---

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SO THE TDI PULL UP THROUGH 54.9 OHM, TMS PULL UP THROUGH 54.9 OHM
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD—ECM*50

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9
LAYOUT NOTE: CONNECT R0803

YONAH

CPU

VSSSENSE

VCCP_1

VCCP_9

VCCP_6

VCCP_5

VCCP_4

VCCP_1

VCC_98

VCC_92

VCC_91

VCC_86

VCC_83

VCC_81

VCC_80

VCC_79

VCC_78

VCC_76

VCC_70

VCC_69

VID3

VID1

B26

W21

T21

R21

AF9

AE9

AC9

AC7

AE7

AF2

AF5

N21

M21

T6

N6

J6

AF18

AF17

AF12

AF10

AE20

AE17

AE15

AE13

AE12

AD14

AD10

AC18

AC17

AF20

=PP1V5_S0_CPU

CPU_VID<6>

CPU_VID<5>

CPU_VID<3>

CPU_VID<1>

2

R0803

100

402

1%

(CPU IO POWER 1.05V)

(CPU CORE POWER)

OUT

OUT

OUT

OUT

9C3

9C3

7B5

8B5

7B6

VCCA=1.5 ONLY

=PPVCORE_S0_CPU

2

1

1/16W

1%

RESISTORS TERMINATE THE 55 OHM BETWEEN VCCSENSE AND VSSSENSE AT THE LOCATION WHERE THE TWO 54.9 OHM TO CONNECT A DIFFERENTIAL PROBE

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CPU 2 OF 2-PWR/GND

REV. D

SHT 051-7370

OF 98

C

A

D
# CPU DECAPS & VID<>

**CPU CORE VID<> SETTINGs**

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dual Core</td>
<td>VCCFM 1.1625</td>
<td>1.30</td>
<td></td>
</tr>
<tr>
<td>Single Core</td>
<td>VCCFM 1.1625</td>
<td>1.30</td>
<td></td>
</tr>
<tr>
<td>UltraLow Voltage</td>
<td>VCCFM 1.0</td>
<td>1.1625</td>
<td></td>
</tr>
</tbody>
</table>

**CPU DECAPS & VID<>**

- **ALL PROCESSOR DEFAULT VCORE FOR INITIAL POWER UP IS 1.2V**
- **TWO PROCESSORS AT THE SAME FREQUENCY MAY HAVE DIFFERENT SETTING WITH THE VID RANGE(VCORE VOLTAGE)**
- **REFER TO YONAH PROCESSOR EMTS REV 1.0**
- **VCCFM: VCORE AT HIGHEST FREQUENCY MODE**
- **VCCFLM: VCORE AT LOWEST FREQUENCY MODE**

---

**VCCA DECOUPLING**

(CPU INTERNAL PLL POWER 1.5V)

PLACE NEAR THE NORTH BRIDGE

VCCP CORE DECOUPLING

(CPU IO POWER 1.05V)

PLACE NEAR THE NORTH BRIDGE ON BOTTOM SIDE

---

**VCC CORE DECOUPLING**

(CPU CORE POWER)

PLACE NEAR THE CPU ON BOTTOM SIDE

10 PCS ON NORTH SIDE

10 PCS ON SOUTH SIDE

---

**IF WE USE LOW ESL CAP, THEN WE CAN USE 20 PCS 22UF CAP**

---

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CPU ZONE THERMAL SENSOR

CPU_MISC1-TEMP SENSOR

PLACE XX WUT TWO XX WUT

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ITP TCK SIGNAL LAYOUT NOTE:

路由TCK信号从ITP700FLEX连接器的TCK引线到CPU的TCK引线，并将信号从CPU TCK引线返回到ITP700FLEX连接器的TCK引线。

CPU ITP700FLEX DEBUG SUPPORT

注意：确保ITP在使用CPU时，CPU在debug接口。

debug port active Torque to CPU TCK pin and route back to ITP700FLEX.

CRITICAL SM1

3029 2827 2625 2423 2221 2019 1817 1615 1413 1211 10 9 8 7 6 5 4 3 2 1

CPU ITP700FLEX DEBUG SUPPORT

SYNC_DATE=5/23/05
SYNC_MASTER=MASTER

XDP_DBRESET_L
CPU_XDP_CLK_N
CPU_XDP_CLK_P
XDP_BPM_L<3>=PP1V05_S0_CPU

XDP_BPM_L<1>=PP3V3_S5_SB_PM

XDP_BPM_L<2>=PP1V05_S0_CPU

XDP_TDI
XDP_TCK
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_BPM_L<0>
XDP_BPM_L<2>

XDP_TMS
XDP_TRST_L
ITPRESET_L

64D6 11C5 9C8 8C7 7D5 64A3 11B3 64C6 33D3 33D2 7B6 7B5 7C6 11B2 64D5 26C6 26C5 7B6 7B8 7C6 7A8 7C6 7B6 7B5 12C4 7D5 23D1 26C5 23D1 7B5 7D6 7C6 7C6 7B8 7C6 7B8 7C6 7C6

051-7370

APPLE INC.
connect to GND through 75-ohm resistors.

VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.
This is the best part to use? SC70-5

RTC Battery Connector

SB RTC Crystal Circuit

Platform Reset Connections

Unbuffered

Buffered

Gated

Initial resistor values are based on CMB, but may change after characterization.
SB_GPIO5 IS PULLED HIGH

ODD detect need less than 100ms include OS latency

MAKE_BASE=TRUE

ODD_PWR_EN_L

2N7002DW-X-F  SOT-363

C3875 0.47UF 402 10%

CERM-X5R

C3876 0.1uF 10V 402 20%

CERM

C3804 603 X5R 20% 6.3V NOSTUFF

C3805 21

NOSTUFF  MF-LF 1/16W 10K

C3806 603 X5R 20% 6.3V NOSTUFF

R3853 33K 5% 402 MF-LF 1/16W

Indicates disk presence, to SMC

Per ATA Spec

Per ATA7 Spec

NC

NC

NC

NC

VOLTAGE=5V

MIN_LINE_WIDTH=0.35MM

APPLY A WIDE TRACE SHAPE FROM JC901 TO C3805/C3806.

PLACE C3805/C3806 CLOSE TO JC901 FOR PP5V_PATA.

MIN_NECK & MIN_LINE WIDTH

ARE CONTROLLED BY PP5V_RUN 1MM / 0.6MM.

SCM_ODD_DETECT

IDE_PDDACK_L

IDE_PDCS3_L

IDE_PDIOR_L

IDE_PDD<14>

IDE_PDD<13>

IDE_PDD<11>

IDE_PDD<10>

IDE_PDD<9>

IDE_PDD<8>

IDE_PDD<7>

IDE_PDD<6>

IDE_PDD<5>

IDE_PDD<4>

IDE_PDD<3>

IDE_PDD<2>

IDE_PDD<1>

IDE_PDD<0>

IDE_PDDREQ

IDE_IRQ14

IDE_PDA<0>

IDE_PDD<0>

IDE_PDD<1>

IDE_PDD<2>

IDE_PDD<3>

IDE_PDD<4>

IDE_PDD<5>

IDE_PDD<6>

IDE_PDD<7>
PORT POWER CLASS

LATE-VO PROTECTION POWER

Cable Power

*Snapback* & "Late VO" Protection

SYNC=SYNC_MASTER=ENET

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FIREWIRE PORT

DESCRIPTION

SYMBOL

START

END

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PHOTO

DRAWING NUMBER

SHEET

OF

SIZE

PLACE L5400 NEAR J5400
PLACE L5411 NEAR J5400
PLACE L5410 NEAR J5400

TO MIDI SLIT

518S0334
SB HAS INTERNAL 15K PULL-DOWNS

0.1UF
402
20%
10V
CERM
NOSTUFF
2
1
C5498
C5499 NEAR L5410

90-OHM
CRITICAL
SM
4
32
1
L5400

10UF
X5R
20%
603
6.3V
NOSTUFF
2
1
C5499

OMIT
F-ST-SM
88611-04001
CRITICAL
4
3
2
1
6
5
J5400

120-OHM-0.3A-EMI
0402-LF
21
L5410
120-OHM-0.3A-EMI
0402-LF
21
L5411

CRITICAL M42B518S0486
IMPROVED ACES CONNECTOR
J5400
BLUETOOTH INTERFACE

C
051-7370
54
98
6C2
64B3
6B2

=USB2_BT_P
=USB2_BT_N
=USB2_BT_F_P
=PP3V3_S3_BT
=PP3V3_S3_BT_F
=GND_BT_F
=USB2_BT_F_P

VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.2MM

PP3V3_S3_BT_F
USB2_BT_F_P
GND_BT_F
USB2_BT_N
USB2_BT_P

6C2
64B3
6B2
Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits

CPU Voltage Sense

Place RC filter close to SMC
NOTE: REPLACE J6250 AND J6251 FROM 518S0332 TO 518S0487
AFTER THIS CHANGE, THE PCB WILL USE 518S0332 LANDPATTERN, BUT BOM WILL STUFF 518S0487 PART
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA (LAN CHIP).
R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M.
R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM.
YUKON POWER CONTROL

2.5V REGULATORS

1.2V REGULATOR

Vout = 0.5V * (1 + Ra / Rb)
1.5V/1.05V POWER SUPPLY

Vout = 0.8V * (1 + R_c / R_d)

R_c = 20kΩ
R_d = 17.8kΩ

D104C/2.8uH

1.5V / 1.05V Power Supply

[Diagram of 1.5V/1.05V Power Supply]