### BOARD STACK-UP AND CONSTRUCTION

#### Top SIGNAL

<table>
<thead>
<tr>
<th>Layer</th>
<th>SIGNAL</th>
<th>MLB STACKUP</th>
<th>TRACE WIDTH (MM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SIGNAL/TOP</td>
<td>CONFORMAL_COAT</td>
<td>0.016</td>
</tr>
<tr>
<td>2</td>
<td>L1-L2</td>
<td>L1-L2</td>
<td>0.07</td>
</tr>
<tr>
<td>3</td>
<td>GROUND</td>
<td>L2-GROUND</td>
<td>0.014</td>
</tr>
<tr>
<td>4</td>
<td>SIGNAL(High Speed)</td>
<td>L2-L3</td>
<td>0.076</td>
</tr>
<tr>
<td>5</td>
<td>POWER</td>
<td>L3-SIGNAL</td>
<td>0.014</td>
</tr>
<tr>
<td>6</td>
<td>GROUND</td>
<td>L3-L4</td>
<td>0.156</td>
</tr>
<tr>
<td>7</td>
<td>SIGNAL(High Speed)</td>
<td>L4-L5</td>
<td>0.076</td>
</tr>
<tr>
<td>8</td>
<td>POWER</td>
<td>L5-GND</td>
<td>0.014</td>
</tr>
<tr>
<td>9</td>
<td>GROUND</td>
<td>L5-L6</td>
<td>0.07</td>
</tr>
<tr>
<td>10</td>
<td>SIGNAL(High Speed)</td>
<td>L6-POWER</td>
<td>0.031</td>
</tr>
<tr>
<td>11</td>
<td>POWER</td>
<td>L6-L7</td>
<td>0.076</td>
</tr>
<tr>
<td>12</td>
<td>GROUND</td>
<td>L7-L8</td>
<td>0.07</td>
</tr>
<tr>
<td>13</td>
<td>SIGNAL(High Speed)</td>
<td>L8-GROUND</td>
<td>0.014</td>
</tr>
<tr>
<td>14</td>
<td>POWER</td>
<td>L8-L9</td>
<td>0.076</td>
</tr>
<tr>
<td>15</td>
<td>GROUND</td>
<td>L9-SIGNAL</td>
<td>0.014</td>
</tr>
<tr>
<td>16</td>
<td>SIGNAL(High Speed)</td>
<td>L9-L10</td>
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<tr>
<td>17</td>
<td>POWER</td>
<td>L10-L11</td>
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<tr>
<td>18</td>
<td>GROUND</td>
<td>L10-L11</td>
<td>0.014</td>
</tr>
<tr>
<td>19</td>
<td>SIGNAL(High Speed)</td>
<td>L11-L12</td>
<td>0.07</td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>L11-L12</td>
<td>0.014</td>
</tr>
<tr>
<td>21</td>
<td></td>
<td>L12-SIGNAL(BOTTOM)</td>
<td>0.047</td>
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</table>

#### Bottom SIGNAL

<table>
<thead>
<tr>
<th>Layer</th>
<th>SIGNAL</th>
<th>MLB STACKUP</th>
<th>TRACE WIDTH (MM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SIGNAL</td>
<td>CONFORMAL_COAT</td>
<td>0.016</td>
</tr>
<tr>
<td>2</td>
<td>L3-L4</td>
<td>L3-L4</td>
<td>0.156</td>
</tr>
<tr>
<td>3</td>
<td>POWER</td>
<td>L4-L5</td>
<td>0.076</td>
</tr>
<tr>
<td>4</td>
<td>GROUND</td>
<td>L5-GND</td>
<td>0.014</td>
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<tr>
<td>5</td>
<td>SIGNAL(High Speed)</td>
<td>L5-L6</td>
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<tr>
<td>6</td>
<td>POWER</td>
<td>L6-POWER</td>
<td>0.031</td>
</tr>
<tr>
<td>7</td>
<td>GROUND</td>
<td>L6-L7</td>
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</tr>
<tr>
<td>8</td>
<td>SIGNAL(High Speed)</td>
<td>L7-L8</td>
<td>0.07</td>
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<tr>
<td>9</td>
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<tr>
<td>10</td>
<td>GROUND</td>
<td>L8-GROUND</td>
<td>0.014</td>
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<tr>
<td>11</td>
<td>SIGNAL(High Speed)</td>
<td>L8-L9</td>
<td>0.156</td>
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<tr>
<td>12</td>
<td>POWER</td>
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<td>13</td>
<td>GROUND</td>
<td>L9-SIGNAL</td>
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<td>14</td>
<td>SIGNAL(High Speed)</td>
<td>L9-L10</td>
<td>0.076</td>
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<td>15</td>
<td>POWER</td>
<td>L10-L11</td>
<td>0.076</td>
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<tr>
<td>16</td>
<td>GROUND</td>
<td>L10-L11</td>
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<td>17</td>
<td>SIGNAL(High Speed)</td>
<td>L11-L12</td>
<td>0.07</td>
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<td>18</td>
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<td>L11-L12</td>
<td>0.014</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>L12-SIGNAL(BOTTOM)</td>
<td>0.047</td>
</tr>
</tbody>
</table>

**TOTAL**: 1.276

---

**Power aliases required by this page**: (NONE)

**Signal aliases required by this page**: 337S3561, 337S3587, 337S3586, 337S3592

**Part Numbers**

- 337S3599: THERMTRIP SCREENED
- 337S3598: THERMTRIP SCREENED
- 826-4393
- 341S2274: LOCKED BOOTROM
- 341S2275: IC,SMC,HS8/2116
- 338S0434

---

**BOM OPTION**

<table>
<thead>
<tr>
<th>COMMON</th>
<th>ALTERNATE</th>
<th>K36 GOOD</th>
<th>K36 BAD</th>
<th>K36 BEST</th>
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<td>COMMON</td>
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<td>V</td>
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<td>PART</td>
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<td>337S3587</td>
<td>337S3586</td>
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**BOM Table for HF POSCAPS**

<table>
<thead>
<tr>
<th>PLAYER</th>
<th>DESCRIPTION</th>
<th>UNIT</th>
<th>PART NUMBER</th>
<th>TERMINAL CONNECTION</th>
<th>TERMINAL CONNECTION</th>
<th>TERMINAL CONNECTION</th>
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</tbody>
</table>

**Configuration Options**

<table>
<thead>
<tr>
<th>CONFIGURATION OPTIONS</th>
<th>K36 GOOD</th>
<th>K36 BAD</th>
<th>K36 BEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sync Master = SMC</td>
<td>common</td>
<td>common</td>
<td>common</td>
</tr>
<tr>
<td>Sync Date</td>
<td>07/17/2022</td>
<td>07/17/2022</td>
<td>07/17/2022</td>
</tr>
</tbody>
</table>

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---

**Author**

Apple Inc.

**Date**

05/17/2012

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**Notes**

- Page borders are required by this page.
- The revision provided by this page.
- The image contains a diagram of the board stack-up and construction, with specific layers, signals, and thicknesses. The BOM table lists parts and their descriptions, with details such as part numbers and terminal connections. Configuration options are also provided.
B - SIZING DOWN R2205 FROM 0603 TO 0402 FOR PLACEMENT.
- FIX MOJO-CARD SMC TX, RX REVERSAL - RADAR: 4910888
3/12/2007
- CHANGE J2800 FROM 518S0487 TO 518S0519.
- CHANGE J3900 FROM 514S0143 TO 514-0443.
- MOVE SMC RESET BUTTON PAD TO TOP SIDE OF MLB - RADAR: 4920913
- CHANGED ALL TRANSIENT SUPPRESSORS TO 6.8V/100PF DEVICES (WERE ORIGINALLY 8V/100PF DEVICES).
- RENAME CPU_VID_R<6:0> TO CPU_VID<6:0>.
- REMOVE R1290 TO R1296 ON CPU_VID<0:6>.
- ADD R1600 (0OHM, 0402) TO CONNECT GFX_VID<4> TO GND.
- 4986074 CHANGE L2205 TO R2205(100OHM,5%,1/10W,0603).
- ADD FUNC_TEST=TRUE FOR THRM_FINSTACK_P/N.
- WAKE-ON-WIRELESS SUPPORT - RADAR: 4954357
- CHANGE 10UF, 16V CPU VCORE CAPS TO 10UF, 6.3V CAPS - RADAR: 4952553
- ADD 270K PULL-DOWN RESISTOR ON HTPLG - RADAR: 4888755
- CHANGE R2900, R2901 FROM 2.2OHM TO 0OHM.
- ADD FUNC_TEST=TRUE FOR PP1V05_S0_R.
- CHANGE C2700 FROM 128S0051 TO 128S0113 PER CE.
- CHANGE C2173 FROM 128S0051 TO 128S0113 PER CE.
- DELETE LVDS_VREFH AND LVDS_VREFL TO GROUND TO FIX LVDS GLITCH.
- LOWER RDS(ON) MOSFET (FDC606P - APN: 376S0552) FOR ODD AND LCD POWER - RADAR: TBD
- REMOVE NO_TEST=TRUE FOR 1V8S3_COMP, 1V8S3_FSET, 3V3S5_COMP, 3V3S5_FSET, 1V05S0_COMP, 1V05S0_FSET, IMVP6_RBIAS, IMVP6_COMP, 5VS5_RUNSS, 1V5S0_RUNSS.

M70 PROTO TO EVT CHANGES
- ADD 2ND SMS (U5930).
- CHANGE U1400 FROM 343S0448 TO 338S0516(NB667, PRQ).
- CHANGE L7900 FROM 152S0302 TO 152S0670 FOR CORRECT AVL.
- ALL 128S0111 BECOME 128S0169.
- ALL 128S0057 BECOME 128S0147.
- ADD OMIT TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.

M70 EVT TO DVT CHANGES
- NOSTUFF C0930.
- ADD 10K PULL-UP RESISTOR (R5232 & R5233) TO =PP3V3_S3_SMBUS_SMC_MGMT.
- UPDATE BOM OPTION TABLE FOR J4300.
- ADD BOM TABLE TO CHANGE L9405, L9406 AND L9407 FROM 155S0303 TO 155S0371.
- ADD ALTERNATE TABLE TO MAKE 155S0310 ALTERNATE OF 155S0322.
- ADD CRITICAL TO U4401.
- ADD OMIT TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.

M70 DVT TO K36 CHANGES
- ADD 155S0303 TO 155S0371.
- ADD 155S0310 TO 155S0322.
- ADD CRITICAL TO U4401.
- ADD OMIT TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.

K36 DVT1 TO DVT2 CHANGES
- NOSTUFF C9401 FOR EMC (RDAR:5475926).
- CHANGE R7210 FROM 2.94K TO 499 OHM 1%.
- IN BOM TABLE, CHANGE PART NUMBER OF Z0903,Z0904,Z0905 AND Z0921 FROM 860-0876 TO 860-0964.

K36 EVT TO DVT1 CHANGES
- ADD CRITICAL TO U4401.
- ADD OMIT TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.

K36 DVT1 TO K36 CHANGES
- ADD CRITICAL TO U4401.
- ADD OMIT TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.

M70 PROTO TO EVT CHANGES
- MANUFACTURING ENTRIES: REMOVED ALL.
- ADD FUNCTIONAL TESTS FOR ALL NEW NETS.
- ADD LAYOUT CHANGES FOR ALL NEW NETS.
- ADD PAYLOAD CHANGES FOR ALL NEW NETS.
- ADD NO_TEST=TRUE FOR ALL NEW NETS.
- ADD ADDITIONAL NOTES FOR ALL NEW NETS.
- ADD ADDITIONAL PAGES FOR ALL NEW NETS.
- ADD ADDITIONAL IMAGES FOR ALL NEW NETS.
- ADD ADDITIONAL TABLES FOR ALL NEW NETS.
Referenced to ground.
CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S TCK PIN.
NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

CRT Disable / TV-Out Enable

S-Video: DACB & DACC only

Leave GFX_VID<3..0> and GFX_VR_EN as NC.

VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VSYNC and CRT_TVO_IREF to GND.

Composite: DACA only

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

Tie VCC_TX_LVDS and VCCA_LVDS to GND.

omit filtering components. Unused DAC outputs TVD_DAC to GND.

Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and follow instructions for LVDS and CRT & TV-Out Disable above.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

All CRT/TVDAC rails must be powered. All decoupling. Otherwise, tie VCCD_LVDS to GND also.
Current numbers from Crestline EDS, doc #21749.

8 7 6 5 4 3 2 1

550 mA (533MHz DDR)
640 mA (667MHz DDR)

0.4 mA
250 mA
100 mA
150 mA
100 mA
60 mA
40 mA
40 mA
80 mA

21C3
20A6
21B5
20B2
21B3
20D1
21D6
21C1
20B5
21B3
18B3
20C1
20D1
21A3
21A3
21B1
21D1
21B1
7C4
7C4
PP1V25_S0_NB_PEGPLL
PP1V5_S0_NB_VCCD_QDAC
PP1V25_S0M_NB_VCCA_SM
PP3V3_S0_NB_VCCA_TVDACA
PP3V3_S0_NB_VCCA_TVDACB
PP3V3_S0_NB_VCCA_TVDACC
PP1V25_S0M_NB_VCCA_HPLL
PP1V25_S0_NB_VCCA_DPLLB
PP1V25_S0_NB_VCCA_DPLLA
PP3V3_S0_NB_VCCA_DAC_BG
PP3V3_S0_NB_VCCA_CRTDAC
=PP1V25_S0M_NB_VCCD_HPLL
PP1V25_S0M_NB_VCCA_SM_CK
=PP3V3_S0_NB_VCCSYNC
=PP1V8_S0_NB_VCCD_LVDS

=VCCD_LVDS2
=VCCD_LVDS1
=VCCD_PEG_PLL
=VCCD_QDAC
=VCCD_TVDAC
=VCCD_CRT

=VCCA_TVC_DAC2
=VCCA_TVB_DAC2
=VCCA_TVA_DAC2
=VCCA_SM_CK1
=VCCA_SM_NCTF2
=VCCA_SM10
=VCCA_SM7
=VCCA_SM5
=VCCA_SM4
=VCCA_SM3
=VCCA_SM2
=VCCA_PEG_PLL
=VSSA_PEG_BG

=VCCA_HPLL
=VTT16
=VCCA_DPLLB
=VCCA_DPLLA
=VSSA_DAC_BG
=VCCA_DAC_BG
=VCCA_CRT_DAC1
=VCC_SYNC

D1 PEG
PLL
A SMA
CK
(8 OF 10)

FCBGA
DMI

www.laptop-schematics.com
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: TDE = _P

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NOT TO ARRIVE IN FRANCE OR SWITZERLAND
PLACE CAP < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN A24

PLACE CAPS < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AE29

PLACE CAP UNDER SB NEAR PINS F19 AND G20

PLACE CAPS AT EDGE OF SB

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PINS AA3...Y7

PLACEMENT NOTE:

PLACE < 2.54MM OF SB ON SECONDARY OR 3.56MM ON PRIMARY NEAR PIN AE7..AJ7

PLACE CAP AT EDGE OF SB

PLACEMENT NOTE:

MIN_LINE_WIDTH=0.3MM

MIN_LINE_WIDTH=0.5MM

MIN_NECK_WIDTH=0.25MM

VOLTAGE=5V

VOLTAGE=1.5V

VOLTAGE=6.3V

VOLTAGE=10V

VOLTAGE=16V

VOLTAGE=5V

CRITICAL

NOSTUFF

SYNC_MASTER=WFERRY

SYNC_DATE=06/01/2006
In CLOSE=12.5pF

It may take a few days before this is done through
2-input NAND gate-APN:311S0304
Pulled a new APN for U2803(0.6mm max

This part is never stuffed,
on the board to short or

Initial resistor values are based on CRB,
but may change after characterization.
B

A

7C4

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

28D3

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)

FERR-120-OHM-1.5A

USE 2.2OHM FOR R2900, R2901 AND 1OHM FOR R2902

402

0

10K

402

MIN_LINE_WIDTH=0.5mm

MIN_NECK_WIDTH=0.2mm

U2900 HAS INTERNAL PU ON PGMODE

STUFF R2905 FOR CK410M MODE

(PORT80 LPC 33MHZ)

Y2901

CRITICAL

18PF

VOLTAGE=3.3V

0.1UF

75D3 29B2

75D3 29A6

75D3

C2903

OUT

CK505_PCI5_FCTSEL1

= SMBUS_CK505_SDA

= SMBUS_CK505_SCL

R2905

6.3V20%

NOSTUFF

X5R402

10%

X5R2

10%

X402

10%

DOT_96/27M

SCL

SRC_1*

SRC_7

SRC_6*

SRC_5

SRC_2

SRC_0*/LCD_CLK*

SCL

PP3V3_S0_CK505_VDD_PCI

PP3V3_S0_CK505_VDD_REF

SYNC_MASTER=DSIMON

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APPLE INC.
- FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS
- FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
- PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
- INPUT/OUTPUT

6/21/2005 - CHANGED INT* TO INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
- PCI_RST_L - PCI RESET FROM SB

6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE

PCI_AD<0..31>, PCI_C_BE_L<0..3>, PCI_FRAME_L, PCI_IRDY_L, PCI_TRDY_L
- FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
Bleed circuit to discharge ODD power rail when ODD is disabled.
Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits.
HEAT-PIPE/FIN-STACK TEMPERATURE ZONE

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GAURD

CPU TEMPERATURE ZONE

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GAURD

WRITE: 0x98 READ: 0x99
IMVP6 CPU VCore Regulator

LATEST ISSUE: 2007/01/23
5V/3.3V POWER SUPPLY

PWM FREQ. = 280 kHz
MAX CURRENT = 7.5A

PWM FREQ. = 430 kHz
MAX CURRENT = 5A

LATEST ISSUE: 2006/12/22
3.425V G3H SUPPLY

Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

1.25V S0 REGULATOR

Vout = 0.85V * (1 + Ra / (Rb + Rc))
PBUS SUPPLY / BATTERY CHARGER
Some signals require 27.4-ohm single-ended impedance.

DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

All FSB signals with impedance requirements are 55-ohm single-ended.

Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.

NOTE: Design Guide recommends at least 25 mils, >50 mils preferred.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.
- 55-ohm +/- 15% from second termination resistor to connector.
- 50-ohm +/- 15% from first to second termination resistor.

CRT & TVDAC signal single-ended impedence varies by location:

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5
### Disk Interface Constraints

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### HD Audio Interface Constraints

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### USB 2.0 Interface Constraints

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### Internal Interface Constraints

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### SPACING RULE SET

- SMB_55S
- USB_60S

### smb_me_SDa

- SPI_55S
- USB_3G

### hda_sync

- SPI_55S
- USB_90D

### spicentle gap

- STANDARD
- 100_OHM_DIFF

### Table Spacing Rule Item

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### Table Physical Rule Item

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### Apple Inc.

- D 051-7559
- A 103 106

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<table>
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<th>Platform LAN (Nineveh) Constraints</th>
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<tbody>
<tr>
<td>PCI Bus Constraints</td>
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- **CLINK_55S**: ENET_MDI
- **ENET_MDI**: 8 7 6 5 4 3 2 1
- **LINE-TO-LINE SPACING**: ALLOW ROUTE = 1.5:1_SPACING
- **MINIMUM LINE WIDTH**: 12 MILS
- **WEIGHT**: ?
- **TABLE_SPACING_RULE_ITEM**: TABLE_SPACING_RULE_ITEM
- **MINIMUM NECK WIDTH**: 300 MILS
- **DIFFPAIR PRIMARY GAP**: STANDARD
- **DIFFPAIR NECK GAP**: PHYSICAL_RULE_SET
- **CB: CLINK_WLAN_RESET_L**
- **LAN_55S**: PCI_CNTL
- **PCI_GNT1_L**: PCI_LOCK_L
- **CLINK_NB**: ENET_LAN
- **PCI_REQ2_L**: PCI_FW_GNT_L
- **PCIE**: PCI_FW_REQ_L
- **CLINK_NB_CLK**: CLINK_NB_DATA
- **ENET_MDI_P**: ENET_MDI_P
- **ENET_GLAN_CLK_R**: SB_CLINK_VREF1
- **INT_PIRQD_L**: PCI_REQ2_L
- **INT_PIRQF_L**: PCI_REQ2_L
- **PCI_AD<31..21>:**: PCI_AD<31..21>
- **PCI_AD<19>:**: PCI_AD<19>
- **PCI_AD<19>:**: PCI_AD<19>
- **PCI_AD<31..21>:**: PCI_AD<31..21>

*Property of Apple Computer, Inc., the possessor.*

Sync Date: 06/12/2006

**APPENDIX B**

*Apple Inc. agrees to the following.*