1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
S		636816	PRODUCTION RELEASED	10/08/08	

K36A MLB SCHEMATIC

10/08/2008

Page (.csa)		Contents		Sync	Date
1	1	Table of Contents	RX	USB	09/05/2006
2	2	System Block Diagram	RX	WFERRY-WF	05/11/2006
3	3	Power Block Diagram	MK	POWER	06/30/2005
4	4	CONFIGURATION OPTIONS	RX	SMC	07/18/2005
5	5	L	RX	N/A	N/A
6	7	FUNC TEST 1 OF 2	RX	TP	07/25/2005
7	8	Power Aliases	MK	WFERRY	06/15/2006
8	9	SIGNAL ALIAS /RESET	RX	GPU	07/17/2006
9	10	CPU FSB	RX	T9_MLB_NOME	11/12/2006
10	11	CPU Power & Ground	RX	T9_MLB_NOME	11/12/2006
11	12	CPU Decoupling & VID	RX	MSARWAR	04/26/2006
12	13	CPU ITP700FLEX DEBUG	ES	MASTER	5/23/05
13	14	NB CPU Interface	ES	T9_MLB	10/30/2006
14	15	NB PEG / Video Interfaces	ES	T9_MLB	10/30/2006
15	16	NB Misc Interfaces	ES	T9_MLB	10/30/2006
16	17	NB DDR2 Interfaces	ES	T9_MLB	10/30/2006
17	18	NB Power 1	ES	T9_MLB	10/30/2006
18	19	NB Power 2	ES	T9_MLB	10/30/2006
19	20	NB Grounds	ES	T9_MLB	10/30/2006
20	21	NB Standard Decoupling	ES	WFERRY	06/15/2006
21	22	NB Graphics Decoupling	ES	WFERRY	06/15/2006
22	23	SB Enet, Disk, FSB, LPC	RX	T9_MLB	10/30/2006
23	24	SB PCI, PCIe, DMI, USB	RX	T9_MLB	10/30/2006
24	25	SB Pwr Mgt, GPIO, Clink	RX	T9_MLB	10/30/2006
25	26	SB Power & Ground	RX	T9_MLB	10/30/2006
26	27	SB Decoupling	RX	WFERRY	06/01/2006
27	28	SB Misc	RX	NB	07/26/2005
28	29	Clock (CK505)	DK	DSIMON	06/06/2006
29	30	Clock Termination	DK	DSIMON-WF	06/06/2006
30	31	DDR2 SO-DIMM Connector A	LD	MEMORY	06/20/2005
31	32	DDR2 SO-DIMM Connector B	LD	MEMORY	06/20/2005
32	33	Memory Active Termination	LD	MEMORY	06/20/2005
33	34	AIRPORT CONNECTOR	LT	ENET	08/19/2005
34	37	Ethernet (Yukon)	LT	USB	10/07/2006
35	38	Yukon Power Control	LT	USB	10/07/2006
36	39	ETHERNET CONNECTOR	LT	USB	09/14/2006
37	40	FIREWIRE CONTROLLER	LT	ENET	08/30/2005
38	43	FIREWIRE PORT	LT	GPU	07/17/2006
39	44	PATA CONNECTOR	DK	GPU	07/17/2006
40	45	SATA CONNECTOR	RX	GPU	07/17/2006
41	46	USB EXTERNAL CONNECTORS	LT	USB	06/30/2006
42	47	CONNECTOR MISC	LT	USB	06/29/2006
43	48	IR CONTROLLER & BT INTERFACE	LT	USB	09/05/2006
44	49	SMC	LD	T9_MLB	10/30/2006
45	50	SMC SUPPORT	LD	GPU	07/17/2006
46	51	LPC+ Debug Connector	LD	WFERRY	06/01/2006
47	52	SMBUS CONNECTIONS	LD	WFERRY	06/01/2006
48	53	CPU Current & Voltage Sense	ES	GPU	07/17/2006
49	55	TEMPERATURE SENSE	ES	GPU	06/21/2006
50	56	Fan	LD	ENET	11/10/2005
51	59	SMS	MK	SMC	08/23/2005
52	61	SPI ROMs	RX	WFERRY	04/26/2006
53	62	AUDIO: CODEC	RX	M70AUDIO	03/12/2007
54	66	AUDI0: SPEAKER AMP	RX	M70AUDIO	03/12/2007
55	67	AUDIO: JACK	RX	M70AUDIO	03/12/2007
56	68	AUDIO: JACK TRANSLATORS	RX	M70AUDIO	03/12/2007
57	69	DC-In & Battery Connectors	RX	POWER	07/13/2005
58	70	S0 FETS & Power Sequencing	MK	DSIMON-WF	05/31/2006
59	71	IMVP6 CPU VCore Regulator	MK	POWER	07/13/2005
60	72	Render VCore Supplies	MK	GPU	06/29/2006
61	73	1.5V / 1.05V Supplies	MK	POWER	07/13/2005
62	75	1.8V/0.9V Supplies	MK	POWER	07/13/2005
63	76	5V/3.3V Supplies	MK	POWER	07/13/2005
64	77	3.42V/1.25V Switcher	MK	ENET	12/06/2005
65	78	S3 FET & S3/S5 Control	MK	DSIMON-WF	06/12/2006
66	79	PBUS Supply/Battery Charger	MK	SMC	08/19/2005
67	90	INVERTER,LVDS,TMDS	MK	GPU	06/23/2006
68	92	EXTERNAL TMDS	ES	GRAPHIC	06/06/2005
69	94	MINI-DVI CONNECTOR	ES	EUGENE	05/21/05
70	100	CPU/FSB Constraints	ES	WFERRY	06/08/2006
71	101	NB Constraints	RX	WFERRY	06/12/2006
72	102	Memory Constraints	ES	WFERRY	06/08/2006
73	103	SB Constraints (1 of 2)	LD	WFERRY	06/12/2006
74	104	SB Constraints (2 of 2)	RX	WFERRY	06/12/2006
75	105	Clock Constraints	RX	WFERRY	06/12/2006
76	106	FireWire & SMC Constraints	DK	WFERRY	06/12/2006

K36A EE DRIS:

DK-DINESH KUMAR

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7559	1	SCHEM,MLB,K36A	SCH	CRITICAL	
820-2279	1	PCBF,MLB,K36	PCB	CRITICAL	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

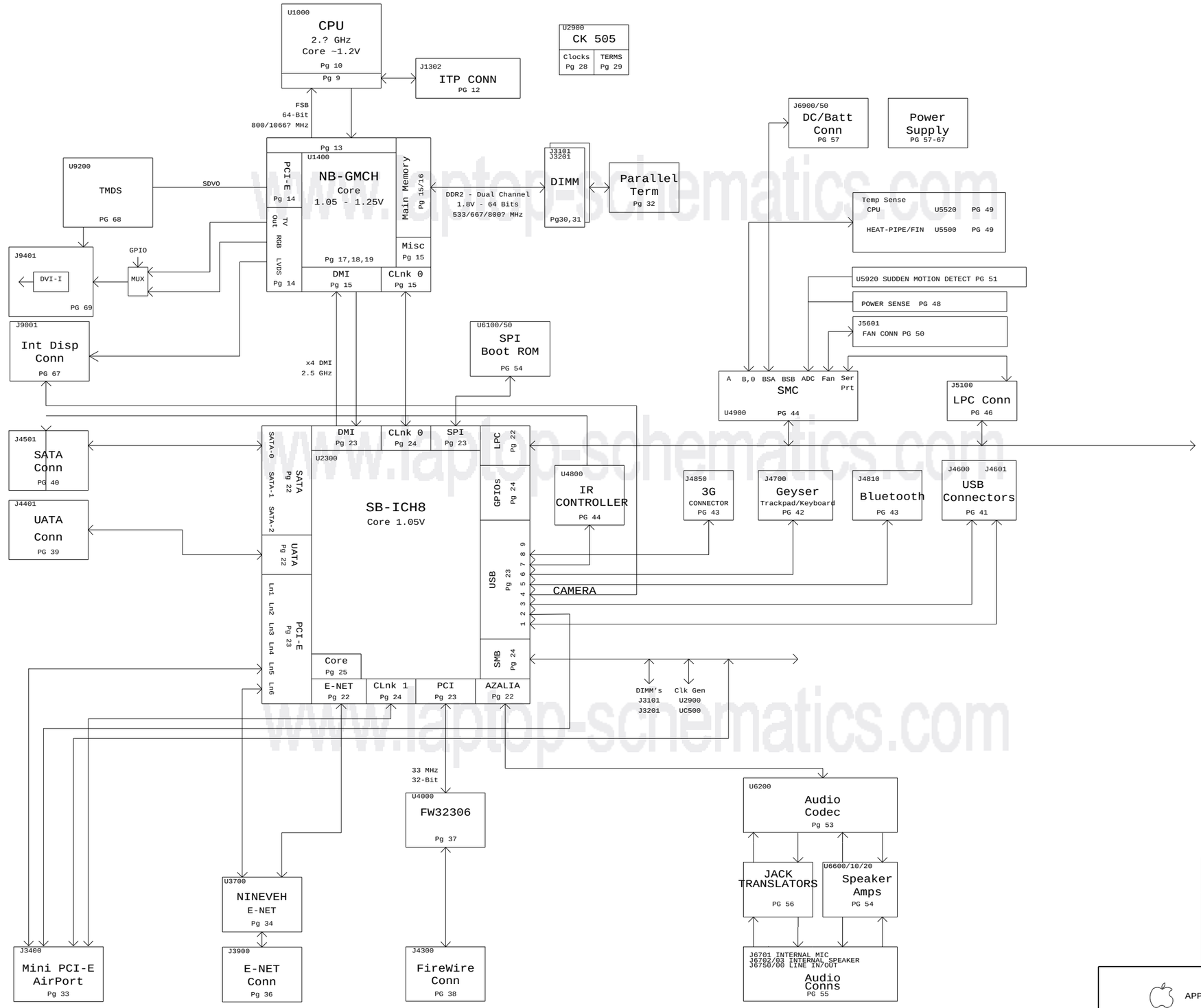
SIZE D

APPLE INC.

TITLE
SCHEM,MLB,K36A

DRAWING NUMBER 051-7559 REV. S

SHT 1 OF 106



System Block Diagram

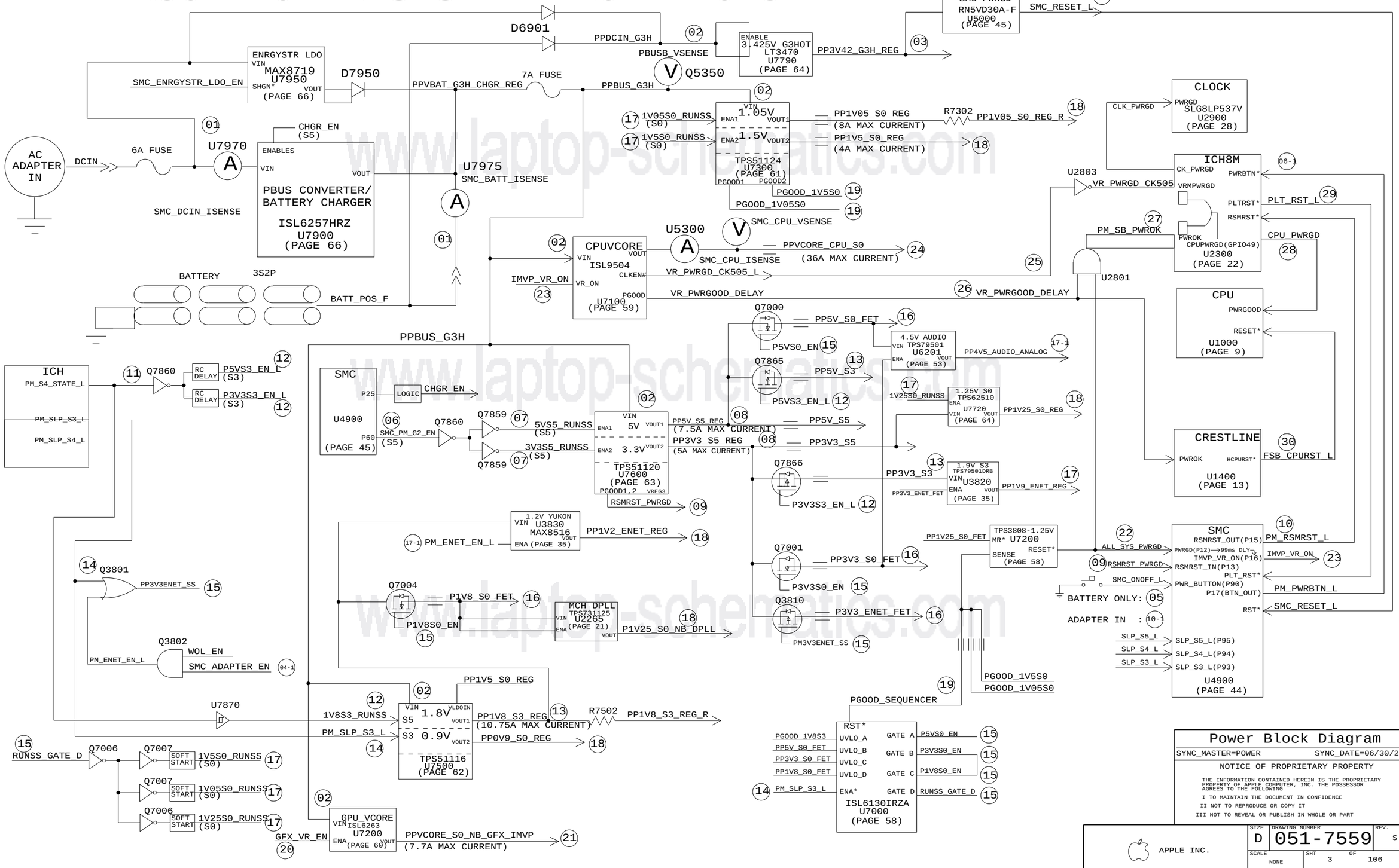
SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	2	106

K36A POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=POWER SYNC_DATE=06/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	3	106

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

BOARD STACK-UP AND CONSTRUCTION

Top		SIGNAL
2		GROUND
3		SIGNAL(High Speed)
4		SIGNAL(High Speed)
5		GROUND
6		POWER
7		POWER
8		GROUND
9		SIGNAL(High Speed)
10		SIGNAL(High Speed)
11		GROUND
BOTTOM		SIGNAL

MLB STACKUP

LAYER	THICKNESS (MM)	TRACE WIDTH (MM)
CONFORMAL_COAT	0.018	
L1 SIGNAL(TOP)	0.047	0.1
L1-L2	0.07	
L2 GROUND	0.014	---
L2-L3	0.076	
L3 SIGNAL	0.014	0.079
L3-L4	0.156	
L4 SIGNAL	0.014	0.079
L4-L5	0.076	
L5 GND	0.014	---
L5-L6	0.07	
L6 POWER	0.031	---
L6-L7	0.076	
L7 POWER	0.031	---
L7-L8	0.07	
L8 GROUND	0.014	---
L8-L9	0.076	
L9 SIGNAL	0.014	0.1
L9-L10	0.156	
L10 SIGNAL	0.014	0.1
L10-L11	0.076	
L11 GROUND	0.014	0.1
L11-L12	0.07	
L12 SIGNAL(BOTTOM)	0.047	0.1
CONFORMAL_COAT	0.018	
TOTAL	1.276	---

BOM OPTION

BOMOPTION	K36 GOOD 630-9104 PVT	K36 BETTER 630-9105 PVT	K36 BEST 630-9106 PVT	M70 GOOD 630-7935 CONCEPT
COMMON	V	V	V	V
ALTERNATE	V	V	V	V
ARB_ONLY				
K36	V	V	V	V
LPCPLUS				V
INVERTER_BUF	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V
INVERTER_UNBUF	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	
ITP				V
NO_REBOOT_MODE				
NBCFG_DMI_REVERSE				
NBCFG_DMI_X2				
NBCFG_DYN_ODT_DISABLE				
NBCFG_PEG_REVERSE				
NBCFG_SDVO_AND_PCIE				
GOOD	V			V
BETTER		V		
BEST			V	
K36_PGM	V	V	V	V
YUKON_EC				
YUKON_ULTRA	V	V	V	V
NORMAL	V	V		V
FANCY			V	
STANDOFF	V	V	V	V
ODD_PWR_CORE	V	V	V	V
ODD_PWR_RESUME				
ISL6126	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	
ISL6130	BOM OPTION REMOVED	BOM OPTION REMOVED	BOM OPTION REMOVED	V

BOM TABLE FOR HF POSCAPS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
128S0147	4	HF VERSION OF 128S0057	C4610,C4611,C6830,C6831	CRITICAL	K36
128S0164	3	HF VERSION OF 128S0073	C2130,C2716,C7543	CRITICAL	K36
128S0148	1	HF VERSION OF 128S0085	C6605	CRITICAL	K36
128S0169	3	HF VERSION OF 128S0111	C7220,C7352,C7542	CRITICAL	K36
128S0160	2	HF VERSION OF 128S0113	C2173,C2700	CRITICAL	K36
128S0150	6	HF VERSION OF 128S0115	C6204 C6205,C7651,C7652,C7691,C7692	CRITICAL	K36
128S0157	1	HF VERSION OF 128S0122	C2220	CRITICAL	K36
128S0162	1	HF VERSION OF 128S0123	C2140	CRITICAL	K36
128S0135	2	HF VERSION OF 128S0129	C6601,C6603	CRITICAL	K36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3592	1	IC,PDC,SLAPS,PRQ,M0/3M,2.1/0.8G,479FCBGA	U1000	CRITICAL	GOOD
337S3576	1	IC,PDC,SLAPR,PRQ,M0/3M,2.4/0.8G,479FCBGA	U1000	CRITICAL	BETTER
337S3576	1	IC,PDC,SLAPR,PRQ,M0/3M,2.4/0.8G,479FCBGA	U1000	CRITICAL	BEST
337S3586	1	IC,PDC,Q72F,Q5,C0,2.1/0.8G,3M,479FCBGA	U1000	CRITICAL	GOOD_FUSED
337S3587	1	IC,PDC,Q72F,Q5,NON-DTS,M0,2.1/0.8G,3M,479FCBGA	U1000	CRITICAL	GOOD_NON_DTS
337S3561	1	IC,PDC,Q72F,Q5,C0,2.4/0.8G,3M,479FCBGA	U1000	CRITICAL	BETTER_FUSED
337S3561	1	IC,PDC,Q72F,Q5,C0,2.4/0.8G,3M,479FCBGA	U1000	CRITICAL	BEST_FUSED

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3598	337S3592	?	U1000	THERMTRIP SCREENED
337S3599	337S3586	?	U1000	THERMTRIP SCREENED
337S3600	337S3576	?	U1000	THERMTRIP SCREENED
337S3604	337S3561	?	U1000	THERMTRIP SCREENED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0516	1	IC,CRESTLINE,GM965,667	U1400	CRITICAL	K36
338S0434	1	IC,ICH8,BGA	U2300	CRITICAL	K36
516-0162	2	IN-LINE SODIMM CONNECTOR	J3101,J3201	CRITICAL	K36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2273	1	IC,16MBIT SPIN SPI FLASH ROM,FOR K36A	U6100	CRITICAL	K36_PGM
341S2060	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U3780	CRITICAL	K36_PGM
341S2275	1	IC,SMC,HS8/2116 FOR K36A	U4900	CRITICAL	K36_PGM
341S2093	1	IC,CYPRESS,CY7C63833,ENCORE_II,USB_CONTR	U4800	CRITICAL	K36_PGM

LOCKED BOOTROM PN 341S2274 FOR K36A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:0PH	CRITICAL	GOOD
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:0PJ	CRITICAL	BETTER
826-4393	1	LBL,P/N LABEL,PCB,28MMX6MM	EEE:0PK	CRITICAL	BEST

CONFIGURATION OPTIONS

SYNC_MASTER=SMC SYNC_DATE=07/18/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	4	106

Revision History

M70 PROTO TO EVT CHANGES

- WAKE-ON-WIRELESS SUPPORT - RADAR: 4954357
- ADD ISOLATION BUFFER FOR ODD_RESET_L SIGNAL, ADD 100K PULL-DOWN TO ODD_PWR_EN_L, ADD ‘DRAG’ CIRCUIT TO PROPERLY DISCHARGE ODD POWER WHEN IT’S TURNED OFF - RADAR: 4923903
- ADD 270K PULL-DOWN RESISTOR ON HTPLG - RADAR: 4888755
- LOWER RDS(ON) MOSFET (FDC606P - APN: 376S0552) FOR ODD AND LCD POWER - RADAR: TBD
- HIGH-PRECISION 0.1% RESISTORS TO INCREASE OUTPUT VOLTAGE REGULATION (5V, 3.3V, PBUS_LDO) ACCURACY - RADAR:4972500
- FIX LINDA CARD POWER ALIAS (NEED TO CONNECT TO PP3V42_G3HOT INSTEAD OF PP3V3_S5) - RADAR: 4927858
- FIX MOJO-CARD SMC TX, RX REVERSAL - RADAR: 4910888
- NO STUFF 3G CONNECTOR CIRCUITRY
- CHANGE BOM STUFFING TO SPEED UP PORT POWER SHUT-OFF RESPONSE TIME DURING ACTIVE LATE-VG EVENT (RADAR: 4985252)
- CHANGE BOM STUFFING TO ENABLE ON-BOARD MICROPHONE CONNECTOR (M42/M42A SOLUTION) INSTEAD OF ROUTING MICROPHONE THROUGH LVDS CABLE
- CHANGE LOAD CAP STUFFING OPTION FOR RTC AND ETHERNET CRYSTALS TO MEET 5XESR (-R) REQUIREMENT
- CHANGE 10UF, 16V CPU VCORE CAPS TO 10UF, 6.3V CAPS - RADAR: 4952553
- MOVE SMC RESET BUTTON PAD TO TOP SIDE OF MLB - RADAR: 4920913
- MODIFY FIREWIRE CONNECTOR SYMBOL TO SUPPORT MINI-DVI CONNECTOR WITH TAB
- TEST POINT MOVEMENTS REQUESTED BY ICT AND MAC-1 GROUPS - RADAR: 4924481

M70 EVT TO DVT CHANGES

3/5/2007

CSA PAGE 8:
- 4954357 ADD =PP3V3_S3_AIRPORT_AUX BACK TO PP3V3_S3 ALIAS.
CSA PAGE 34:
- 4954357 BREAK OUT =PP3V3_S3_AIRPORT_AUX(J3400_PIN 24) FROM PP3V3_S3_AP_AUX_AGAIN.
- 4954357 MOVE C3409 AND C3410 FROM PP3V3_S3_AP_AUX RAIL TO =PP3V3_S3_AIRPORT_AUX RAIL.
CSA PAGE 49:
- 5040728 STUFF C9421 FOR EMI.
CSA PAGE 62,66,67,68:
- SYNC FROM AUDIO TEAM.
CSA PAGE 67:
- 4999533 SWAP PIN 2 AND PIN 3 OF MIC CONNECTOR, BACK TO M42 PIN OUT.
CSA PAGE 78:
- 5029811 CHANGE Q7940 FROM 376S0326 TO 376S0558.

3/8/2007

CSA PAGE 22:
- 4986074 CHANGE L2205 TO R2205(100OHM,5%,1/10W,0603).
CSA PAGE 25:
- 4924143 CHANGE R2514 FROM 100K PULL-DOWN TO 10K PULL-UP TO 3.3V_S5.
CSA PAGE 77:
- 5040847 SYNC 1P25V REGULATOR CIRCUIT FROM M82. CHANGE R_AND C_TO 0402. CHANGE =PP3V3_S5_P1V25S0 TO =PP3V3_S5_1V25S0, C7723 FROM 2.2NF TO 10000PF, C7724 FROM 22PF TO 100PF, C7728 FROM 2.2NF TO 10000PF, AND REVERT REFERENCE DESIGNATORS. (CHANGE FROM TPS62510 TO LTC3412A)

3/12/2007

CSA PAGE 25:
- 4924143 CHANGE R2514 FROM 100K PULL-UP TO 47K PULL-UP.
CSA PAGE 45:
- UPDATE SYMBOL FOR J4501.
CSA PAGE 62,66,67,68:
- SYNC FROM AUDIO TEAM.
CSA PAGE 94:
- 4986074 CHANGE R9469 FOR CRT_TVO_IREF FROM 1.3K TO 1.21K.

3/14/2007

CSA PAGE 47:
- ADD TEXT NOTE TO UPDATE J4700 FROM 516S0251 TO 516S0588 WHEN SYMBOL IS READY.
CSA PAGE 69:
- ADD TEXT NOTE TO UPDATE J6900 FROM 518S0287 TO 518S0526 WHEN SYMBOL IS READY.
CSA PAGE 90:
- DELETE LVDS_VREFH AND LVDS_VREFL TO GROUND TO FIX LVDS GLITCH.
CSA PAGE 94:
- ADD TEXT NOTE TO CHANGE L9404 FROM 155S0303 TO 155S0348 WHEN SYMBOL IS READY.

M70 DVT TO K36 CHANGES

6/29/2007

CSA PAGE 4:
- CHANGE GOOD CPU FROM 337S3471(1.8G) TO 337S3463(2.0G).
- CHANGE BETTER CPU FROM 337S3470(2.0G) TO 337S3464(2.2G).
- CHANGE BEST CPU FROM 337S3469(2.2G) TO 337S3465(2.4G).
- CHANGE U8 FROM 338S0428(800M) TO 343S0448(667M).
- CHANGE U6 FROM 338S0427 TO 338S0434.
CSA PAGE 16:
- DISCONNECT GFX_VID<0> TO GND.
- CONNECT GFX_VID<0:3> TO GFX_VID0:3 ON NB.
- ADD R1600 (00HM, 0402) TO CONNECT GFX_VID<4> TO GND.
CSA PAGE 22:
- 5209756 ADD C2207 (0.1UF, 0402).
- SIZING DOWN R2205 FROM 0603 TO 0402 FOR PLACEMENT.
- CHANGE GFX_VID<1:2> TO GFX_VID<0:3>.
- CHANGE STRAPPING FROM 0010 ON GFX_VID<1:4> TO 0001 ON GFX_VID<0:3>.
CSA PAGE 39:
- CHANGE J3900 FROM 514S0143 TO 514-0443.
- EDVT BOM OPTION TABLE.
CSA PAGE 46:
- CHANGE U4600 FROM 353S1245 TO 353S1728.
- REMOVE MIN_NECK_WIDTH=0.3MM FROM PP5V_S3_USB2_EXTA/B.
- ADD NOSTUFF R4660 AND R4661.
CSA PAGE 47:
- CHANGE J4700 FROM 516S0251 TO 516S0588.
CSA PAGE 69:
- CHANGE J6900 FROM 518S0287 TO 518S0526.
- REPLACE BATTERY INTERFACE CIRCUIT WITH THE ONE ON M42B ESTAR.
CSA PAGE 94:
- 5040728 CHANGE L9404 FROM 155S0303 TO 155S0348.

7/5/2006

CSA PAGE 4:
- REPLACE ALL M70 WITH K36 (TEXT, BOM OPTIONS, 630 NUMBERS).
CSA PAGE 21:
- CHANGE C2173 FROM 128S0051 TO 128S0113 PER CE.
CSA PAGE 27:
- CHANGE C2700 FROM 128S0051 TO 128S0113 PER CE.
CSA PAGE 28:
- CHANGE J2800 FROM 518S0487 TO 518S0519.
CSA PAGE 45:
- REMOVE R4660 AND R4601 (U4675 BYPASS RESISTORS).
CSA PAGE 46:
- CHANGE J4810 FROM 518S0369 TO 518S0521.
CSA PAGE 55:
- CHANGE D5500 FROM M70 EMC1033 CIRCUIT TO M71 EMC1043 CIRCUIT.
- 15528 CHANGES FROM 2PIN TO 4PIN.
CSA PAGE 56:
- CHANGE J5601 FROM 518S0369 TO 518S0521.
CSA PAGE 67:
- CHANGE J6702 FROM 518S0487 TO 518S0519.
- CHANGE J6703 FROM 518S0369 TO 518S0521.
CSA PAGE 68:
- CHANGE J9000 FROM 518S0369 TO 518S0521.

7/6/2006

CSA PAGE 8:
- REMOVE NO_TEST=TRUE FOR 1V8S3_COMP, 1V8S3_FSET, 3V3S5_COMP, 3V3S5_FSET, 1V05S0_COMP, 1V05S0_FSET, IMVP6_RBIAS, IMVP6_COMP, 5VS5_RUNSS, 1V5S0_RUNSS.
- REMOVE NO_TEST=TRUE FOR CK505_SRC14_CLK_SPN, CK505_SRC1_N/P_SPN, CK505_SRC3_N/P_SPN, CK505_SRC7_N/P_SPN, CK505_SRC_CLKREQ1/3_L_SPN.
- ADD FUNC_TEST=TRUE FOR THRM_FINSTACK_P/N.
- ADD FUNC_TEST=TRUE FOR PP1V05_S0_R.
CSA PAGE 9:
- REMOVE ALIASES FOR GND_CHASSIS_AUDIO_SPKRCONN,GND_CHASSIS_AUDIO_SHIELD1,GND_CHASSIS_AUDIO_SHIELD2,GND_CHASSIS_AUDIO_SHIELD3,MIC_SHIELD_LVDS_R,MIC_SHLD_CONN.
- REMOVE ALIAS FOR =PWRBT_CNRDN.
- ADD SPN ALIASES FOR TP_CK505_SRC7_N/P.
- ADD SPN ALIASES FOR CK505_PCI2/4_CLK.
CSA PAGE 12:
- REMOVE R1290 TO R1296 ON CPU_VID<0:6>.
CSA PAGE 14:
- DELETE TEXT NOTE AND WITH RESET BUTTON.
CSA PAGE 15:
- RENAME LVDS_VREFH/L TO TP_LVDS_VREFH/L.
CSA PAGE 25:
- ADD R2507 AND R2506 FOR 10K PU ON GPIO6 AND GPIO17(EXTGPU_RST_L).
- CHANGE R2514 TO 100K.
CSA PAGE 28:
- CHANGE L2902 AND L2903 FROM 155S0302 TO 0OHM R2906 AND R2907.
- NOSTUFF C2807, C2810, C2916, C2911, C2914.
- CHANGE R2900, R2901 FROM 2.2OHM TO 0OHM.
- CHANGE R2902 FROM 10HM TO 0OHM.
CSA PAGE 44:
- REMOVE TEXT NOTE WILL CHANGE TO 606P.
CSA PAGE 45:
- RE-DRAW CPU VOLTAGE SENSE RC FILTERING.
CSA PAGE 62:
- RE-CONNECTED (SHDN_INPUT OF U6801 SO THAT IT’S CONTROLLED BY U6200 PORTA VREF. - DISCONNECTED GPIO1 AND TERMINATED IT WITH A 10K PULL DOWN.
- ADDED A NO STUFF ENABLE PULLDOWN TO GND ON U6200 A7 GPIO2.
- ADDED SMALL 15PF COMPENSATION CAP. TO U6201 FEEDBACK NETWORK (C6224).
CSA PAGE 67:
- CHANGED ALL TRANSIENT SUPPRESSORS TO 6.8V/100PF DEVICES (WERE ORIGINALLY 8V/100PF DEVICES).
- ADDED L6771 AND L6773 TO MIC INPUT EMI FILTER.
- REMOVED DZ6772.
- ADDED R6740 NO STUFF.
CSA PAGE 68:
- CONNECTED MIC_SHLD_CONN TO GND_CHASSIS_AUDIO_MIC THROUGH R6854.
- ADDED R6856 NO STUFF.
CSA PAGE 71:
- RENAME CPU_VID_R<6:0> TO CPU_VID<6:0>.

7/10/2007

CSA PAGE 4:
- BOOTROM PART NUMBER CHANGES FROM 341S2085 TO 341S2196.
- EMC PART NUMBER CHANGES FROM 341S2088 TO 341S2198.
- UPDATE EEE CODES, Z9S FOR GOOD, Z58 FOR BETTER, Z57 FOR BEST.
CSA PAGE 15:
- ADD ALIAS =PP3V3_S3_SMBUS_SMC_MGMT TO PP3V3_S3.
CSA PAGE 29:
- ADD CRITICAL TO U2900.
CSA PAGE 44:
- ADD CRITICAL TO U4401.
CSA PAGE 46:
- CHANGE U4675 FROM APN 353S1505 TO APN 353S1742. (SMALL PACKAGE)
- ADD R4670 & R4671. (USB BYPASS ROUTING).
CSA PAGE 49:
- REMOVE ALIAS FOR =SMC_SMS_INT TO SMC_PG1 - SIGNAL SHOULD JUST BE CALLED SMC_SMS_INT.
CSA PAGE 50:
- CHANGE R5077 FROM PULL-UP TO A PULL-DOWN RESISTOR AND NAME IT SMC_SMS_INT.
CSA PAGE 52:
- I2C@3.3V BE SMBUS.
- SMB_ME_CLK AND SMB_ME_DATA ON SOUTHBRIDGE DISCONNECTED FROM SMB_MGMT_CLK AND SMB_MGMT_DATA FROM SMC.
- THE 10K PULL-UP RESISTORS (R5230 AND R5231), AND STILL REMAIN CONNECTED TO PP3V3_S5_SMBUS_SB_ME AND STAY ON THE SB SIDE.
- SMC MANAGEMENT SMBUS CONNECTION:
- ADD TWO NEW 10K PULL-UP RESISTOR (R5232 & R5233) TO =PP3V3_S3_SMBUS_SMC_MGMT.
- THE PULL-UP RESISTORS SHOULD BE CONNECTED BETWEEN SMB_MGMT_CLK AND SMB_MGMT_DATA TO =I2C_SMS_SCL AND =I2C_SMS_SDA OF THE NEW ACCELEROMETER.
CSA PAGE 59:
- ADD 2ND SMS (U5930).
CSA PAGE 62:
- CHANGED C6210 FROM A CASE-R 10UF TANT. CAP. TO A SMA-LE 3.3UF TANT. CAP.
- MADE NO TEST ATTRIBUTE VISIBLE FOR NET NC_VRP CONNECTED TO PIN 37 OF U6200.
CSA PAGE 67:
- REMOVED NO STUFF RESISTORS R6730, R6731, AND R6732. ALSO REMOVED L6774.
- STUFFED R6740.
- MADE DZ6702, DZ6703, DZ6704, DZ6705, DZ6752, DZ6753, DZ6754, DZ6755, DZ6770, DZ6771´ CRITICAL.
CSA PAGE 68:
- NO STUFFED R6854
CSA PAGE 75:
- CHANGE R7208 FROM 8.66K TO 15.8K.

7/11/2007

CSA PAGE 9:
- CHANGE Z0901 AND Z0906 FROM 998-1178 TO 998-1186 (NON-PLATED).
CSA PAGE 31:
- STUFF C3110 AND C3111.
CSA PAGE 32:
- STUFF C3210 AND C3211.
CSA PAGE 39:
- UPDATE BOM FOR FANCY RJ45 CONNECTOR, 514-0475.
CSA PAGE 50:
- REMOVE R5077 (BECOMES R5931).
CSA PAGE 59:
- ADD U5930. 10K PU ON SMC_SMS_INT.
- ADD R5931 (WAS R5077 BEFORE), 10K PD ON SMC_SMS_INIT.
- STUFF U5930 (DIGITAL ACCELEROMETER) CIRCUIT.

7/12/2007

CSA PAGE 43:
- CHANGE J4300 FROM 514-0289 TO 514-0456 (SAME JEDEC).
- UPDATE BOM OPTION TABLE FOR J4300.
- NORMAL CHANGES FROM 514-0359 TO 514-0456, FANCY CHANGES FROM 514-0316 TO 514-0476.
CSA PAGE 46:
- CHANGE J4800 AND J4801 FROM 514-0288 TO 514-0457 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J4800 AND J4801.
- NORMAL CHANGES FROM 514-0288 TO 514-0457, FANCY CHANGES FROM 514-0315 TO 514-0477.
CSA PAGE 62:
- ADD PAGE TITLE AUDIO: CODEC.
CSA PAGE 67:
- CHANGE J6700 FROM 514-0409 TO 514-0459 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J6700.
- NORMAL CHANGES FROM 514-0409 TO 514-0459, FANCY CHANGES FROM 514-0411 TO 514-0479.
- CHANGE J6750 FROM 514-0408 TO 514-0458 (DIFFERENT JEDEC, SAME LANDPATTERN).
- UPDATE BOM OPTION TABLE FOR J6750.
- NORMAL CHANGES FROM 514-0408 TO 514-0458, FANCY CHANGES FROM 514-0410 TO 514-0478.
CSA PAGE 78:
- CHANGE L7900 FROM 152S0302 TO 152S0670 FOR CORRECT AVL.
CSA PAGE 94:
- UPDATE BOM OPTION TABLE FOR J9401.
- NORMAL CHANGES FROM 514-0375 TO 514-0480, FANCY CHANGES FROM 514-0376 TO 514-0481.

7/13/2007

CSA PAGE 4:
- CHANGE BEST CPU FROM 337S3465(2.4GHZ) TO 337S3464(2.2GHZ).
CSA PAGE 45:
- CHANGE C3831 AND C3832 FROM 138S0582 TO 138S0554 (DON’T NEED LOW-PROFILE PARTS).

7/17/2007

CSA PAGE 59:
- UPDATE SYMBOL FOR U5930, VENDOR PART NUMBER CHANGES FROM SMB380 TO BMA150.

7/24/2007

CSA PAGE 4:
- CHANGE BETTER AND BEST CPU TO G0 STEPPING PARTS (FROM 337S3464 TO 337S3500).
CSA PAGE 42:
- STUFF R2242 AND NOSTUFF R2247.
CSA PAGE 52:
- CHANGE R9201 AND R9202 FROM 5.23K TO 2.94K.
- CHANGE R9211 AND R9212 FROM 16.5K TO 9.09K.

K36 EVT TO DVT1 CHANGES

8/9/2007

PER CE, ALL SANYO POSCAPS HAVE NEW HF PART NUMBERS.
- ALL 128S0057 BECOME 128S0147.
- ALL 128S0073 BECOME 128S0164.
- ALL 128S0095 BECOME 128S0148.
- ALL 128S0111 BECOME 128S0169.
- ALL 128S0113 BECOME 128S0166.
- ALL 128S0115 BECOME 128S0150.
- ALL 128S0122 BECOME 128S0157.
- ALL 128S0123 BECOME 128S0162.
- ALL 128S0129 BECOME 128S0135.
- ADD QTY1 TO ALL ABOVE PARTS SO THE HF PARTS IN BOM TABLE TAKE OVER.
CSA PAGE 4:
- ADD BOM OPTION TABLE FOR ALL SANYO POSCAP TO USE HF PARTS.

8/10/2007

CSA PAGE 12:
- C1235 SYMBOL CORRECTED TO REFLECT 20% TOLERANCE.
CSA PAGE 79:
- CHANGE U7920 FROM 107S0077(EOL) TO 107S0110.
- CHANGE R7952 FROM 103S0189 TO 103S0200 FOR HF.

8/13/2007

CSA PAGE 34:
- CHANGE J3400 FROM 516S0406 TO 516S0635 TO ADD ACON AS 2ND SOURCE.

K36 DVT1 TO DVT2 CHANGES

8/30/2007

CHANGE ALL 138S0578 TO 138S0614 FOR ADDITIONAL VENDORS.
(C2205,C4800,C4804,C7305,C7508,C7605,C7902,C7911,C7912)
CSA PAGE 43:
- ADD ALTERNATE TABLE TO MAKE 155S0369 ALTERNATE OF 155S0326.
CSA PAGE 46:
- ADD ALTERNATE TABLE TO MAKE 155S0310 ALTERNATE OF 155S0322.
CSA PAGE 72:
- CHANGE C7210 FROM 150pF(1.21%)(1) TO 220pF(1%)(2)(3).
- CHANGE R7208 FROM 0.0010UF(1325400) TO 0.001UF(1323045).
CSA PAGE 94:
- ADD CR1 TO L9405, L9406 AND L9407.
- ADD BOM TABLE TO CHANGE L9405, L9406 AND L9407 FROM 155S0303 TO 155S0371.
- ADD ALTERNATE TABLE TO MAKE 155S0376 ALTERNATE OF 155S0348.

9/3/2007

CSA PAGE 9:
- NOSTUFF C0930.

K36 DVT2 TO PVT CHANGES

9/3/2007

CSA PAGE 73:
- DELETE =PP1V5_S0_REG_P BECOMES =PP1V5_S0_REG.
CSA PAGE 76:
- DELETE =PP3V3_S5_REG_P BECOMES =PP3V3_S5_REG.
- DELETE =PP5V_S5_REG_P BECOMES =PP5V_S5_REG.

9/7/2007

CSA PAGE 4:
- CHANGE U1400 FROM 343S0448 TO 338S0516(NB667, PRQ).
- CHANGE U7400 FROM 337S3468 TO 337S3502 (2.2GHZ CPU, PRQ).
- UNCHECK BOM OPTIONS ITP AND LPCPLUS IN TABLE.
CSA PAGE 38:
- ADD BOM OPTION ITP TO R3004 AND R3005.
CSA PAGE 46:
- NOSTUFF U4675,C4675.
- STUFF R4670 AND R4671.
CSA PAGE 59:
- NOSTUFF U5930,C5931,C5932.
- NOSTUFF R5931 AND STUFF R5930.

9/13/2007

CSA PAGE 52:
- CHANGE R5280 AND R5281 TO 1K (RDAR:5188703).
CSA PAGE 92:
- NOSTUFF C9401 FOR EMC (RDAR:5475926).

9/25/2007

CSA PAGE 9:
- IN BOM TABLE, CHANGE PART NUMBER OF Z0903,Z0904,Z0905 AND Z0921 FROM 860-0876 TO 860-0964.
CSA PAGE 73:
- CHANGE C7320 AND L7360 FROM 152S0432 TO 152S0685 TO ADD TDK.
CSA PAGE 79:
- CHANGE L7520 FROM 152S0432 TO 152S0685 TO ADD TDK.

9/27/2007

CSA PAGE 22:
- UNSTUFF R2242 AND STUFF R2247.

10/1/2007

CSA PAGE 72:
- CHANGE R7208 FROM 15.8K TO 4.99K 1%.
- CHANGE R7210 FROM 2.94K TO 499 OHM 1%.

L

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 5 OF 106	

Functional Test Points

Power Supply NO_TESTs

NO_TEST

L93		IMVP6_RBIAS	59A4 59B7
L94		IMVP6_COMP	59A4 59B7
L95		5VS5_RUNSS	63B5 65C5
L96		1V5S0_RUNSS	58B1 61B5

CLOCK NO_TESTS

NO_TEST

L11	TRUE	CK505_CPU0_N	28C4 29D6 75D3
L11	TRUE	CK505_CPU0_P	28C4 29D6 75D3
L11	TRUE	CK505_CPU1_N	28C4 29D6 75D3
L11	TRUE	CK505_CPU1_P	28C4 29D6 75D3
L11	TRUE	CK505_CPU2_ITP_SRC10_N	28C4 29D6 75D3
L11	TRUE	CK505_CPU2_ITP_SRC10_P	28C4 29D6 75D3
L11	TRUE	CK505_DOT96_27M_N	28A4 29B6 75D3
L11	TRUE	CK505_DOT96_27M_P	28A4 29B6 75D3
L11	TRUE	CK505_LVDS_N	28B4 29C6 75C3
L11	TRUE	CK505_LVDS_P	28B4 29C6 75D3
L11	TRUE	CK505_PCIF1_CLK	28B6 29B6 75D3
L11	TRUE	CK505_SRC2_N	28B4 29C6 75C3
L11	TRUE	CK505_SRC2_P	28B4 29C6 75C3
L11	TRUE	CK505_SRC4_N	28B4 29C6 75C3
L11	TRUE	CK505_SRC4_P	28B4 29C6 75C3
L11	TRUE	CK505_SRC5_N	28B4 29C6 75C3
L11	TRUE	CK505_SRC5_P	28B4 29C6 75C3
L11	TRUE	CK505_SRC6_N	28B4 29B6 75C3
L11	TRUE	CK505_SRC6_P	28B4 29C6 75C3
L11	TRUE	CK505_SRC8_N	28A4 29B6 75C3
L11	TRUE	CK505_SRC8_P	28A4 29B6 75C3

FIREWARE NO_TESTS

NO_TEST

L11	TRUE	FW_B_TPA_N_SPN	8D1
L12	TRUE	FW_B_TPA_P_SPN	8D1
L12	TRUE	FW_B_TPBIAS_SPN	8D1
L12	TRUE	FW_B_TPB_N_SPN	8D1
L12	TRUE	FW_B_TPB_P_SPN	8D1
L12	TRUE	FW_C_TPA_N_SPN	8D1
L12	TRUE	FW_C_TPA_P_SPN	8D1
L12	TRUE	FW_C_TPBIAS_SPN	8D1
L12	TRUE	FW_C_TPB_N_SPN	8D1
L12	TRUE	FW_C_TPB_P_SPN	8D1

LVDS NO_TESTS

NO_TEST

L12	TRUE	LVDS_B_CLK_N_SPN	8D5
L12	TRUE	LVDS_B_CLK_P_SPN	8D5
L12	TRUE	LVDS_B_DATA_N0_SPN	8D5
L12	TRUE	LVDS_B_DATA_N1_SPN	8D5
L12	TRUE	LVDS_B_DATA_N2_SPN	8D5
L12	TRUE	LVDS_B_DATA_P1_SPN	8D5
L12	TRUE	LVDS_B_DATA_P2_SPN	8D5

NO_TEST

L21	TRUE	SMC_FAN_3_TACH	44A4 44A8

Fan Connectors

FUNC_TEST

L12	TRUE	=PP5V_S0_FAN_RT	7A7 50C4
L15	TRUE	FAN_RT_PWM	50B3
L16	TRUE	FAN_RT_TACH	50C3
L15	TRUE	=PP3V3_S0_FAN_RT	7C4 50C4
L15	TRUE	SMC_FAN_1_CTL	44A8 50B4
L15	TRUE	SMC_FAN_1_TACH	44A8 50C4

LPC+ Debug Connector

FUNC_TEST

L20	TRUE	=PP3V42_G3H_LPCPLUS	7B1 46C6
L20	TRUE	=PP5V_S0_LPCPLUS	7A7 46C6
L18	TRUE	LPC_AD<0>	22D4 44C8 46C6
L17	TRUE	LPC_AD<1>	22D4 44C8 46C6
L17	TRUE	LPC_FRAME_L	22D4 44C8 46B6
L17	TRUE	PM_CLKRUN_L	24C8 37A5 44C5 46B6
L17	TRUE	BOOT_LPC_SPI_L	23B5 46B6
L17	TRUE	SMC_TMS	44B5 45C5 46B6
L17	TRUE	DEBUG_RESET_L	27D1 46B6
L17	TRUE	SMC_TRST_L	44C1 46B6
L17	TRUE	SMC_TDO	44B5 45C5 46B6
L17	TRUE	SMC_MD1	44D1 46B6
L17	TRUE	SMC_TX_L	41A8 44B8 44C5 45D5 46B6
L18	TRUE	FWH_INIT_L	46C5
L18	TRUE	PCI_CLK33M_LPCPLUS	29B3 46C4 75C3
L18	TRUE	LPC_AD<2>	22D4 44C8 46C4
L18	TRUE	LPC_AD<3>	22D4 44C8 46C4
L18	TRUE	INT_SERIRQ	24C8 44C8 46B4
L18	TRUE	PM_SUS_STAT_L	24D5 44C5 46B4
L18	TRUE	SMC_TDI	44B5 45C5 46B4
L18	TRUE	SMC_TCK	44B5 45C5 46B4
L18	TRUE	SMC_RESET_L	44C3 45D7 46B4
L18	TRUE	SMC_NMI	44C1 46B4
L17	TRUE	SMC_RX_L	41A8 44B8 44C5 45D5 46B4
L19	TRUE	LINDACARD_GPIO	24A7 24D5 46B4

Other Func Test Points

FUNC_TEST

L19	TRUE	=PP1V05_S0_REG	7D8 61B8

SMBus FUNC_TEST

I182

	TRUE	SMBUS_SMC_B_S0_SCL	47C5 76C3
L15	TRUE	SMBUS_SMC_B_S0_SDA	47C5 76C3

FIREWIRE FUNC_TEST

L15	TRUE	PPFW_SWITCH	38D3

SLEEP LED FUNC_TEST

L15	TRUE	SYS_LED_ANODE	40C5 45A3

SMC FUNC_TEST

L15	TRUE	SMC_LID	42C3 44B5 45C5 57A8
L15	TRUE	SMC_MANUAL_RST_L	45D8
L16	TRUE	SMC_CPU_VSENSE	44C5 48B1

Power Supply FUNC_TEST

L16	TRUE	ALL_SYS_PWRGD	27A5 44D8 58A3
L16	TRUE	PPVCORE_S0_CPU	7D7
L20	TRUE	PP1V05_S0_R	7D7
L16	TRUE	PP1V05_S0	7D7 45D2
L16	TRUE	PP1V5_S0	7C7
L16	TRUE	PP1V8_S0	7B7
L16	TRUE	PP3V3_S0	7D4 45D1
L16	TRUE	PP5V_S0	7A7
L16	TRUE	PP1V2_ENET_S0	7B5
L16	TRUE	PP1V8_S3	7B4
L17	TRUE	PP3V3_S3	7A4
L17	TRUE	PP5V_S3	7A4
L17	TRUE	PP3V3_S5	7D1
L17	TRUE	PP5V_S5	7C1
L17	TRUE	PP3V42_G3H	7C1
L17	TRUE	PPBUS_G3H	7B1
L17	TRUE	PP18V5_G3H	7B1
L18	TRUE	PP0V9_S0	7D7
L22	TRUE	PP3V3_S3_BT_F	43D2
L23	TRUE	GND_BT_F	43C2

Battery Digital Connector

FUNC_TEST

L1	TRUE	SMC_BS_ALRT_L	44C5 45C5 57A2
L3	TRUE	SMBUS_BATT_SCL_F	57A5
L4	TRUE	SMBUS_BATT_SDA_F	57A5
L17	TRUE	BATT_POS	57B5
L18	TRUE	BATT_NEG	57A5

Audio FUNC_TEST

L9	TRUE	=PP5V_S0_AUDIO_AMP	7A7 54B8 54C8 54D8
L11	TRUE	=PP5V_S0_AUDIO	7A7 53A7 56C4
L19	TRUE	GND_AUDIO_AMP	8A4
L21	TRUE	GND_AUDIO_CODEC	8B4
L22	TRUE	ACZ_SDATAIN<0>	8A5 53C7
L24	TRUE	ACZ_SDATAOUT	8A5 53C7
L25	TRUE	ACZ_BITCLK	8A5 53C7
L26	TRUE	ACZ_RST_L	8A5 53B7
L45	TRUE	ACZ_SYNC	8A5 53C7

Battery FUNC_TEST

L29	TRUE	SMC_BATT_ISET	44B5 66A8
L32	TRUE	SMC_BATT_CHG_EN	44C8 45B6 66A4
L34	TRUE	SMC_BC_ACOK	66A6 44C5 45B6 57C3 57C7
L33	TRUE	SMC_ADAPTER_EN	45B3 57C4 43C7 35C7 38C6 44D5
L36	TRUE	SMC_BATT_TRICKLE_EN_L	44C8 45B6 66A3
L38	TRUE	SYS_ONEWIRE	44B8 45D5 57C8

USB FUNC_TEST

L44	TRUE	TP_USB_EXCARD_P	8B2
L47	TRUE	TP_USB_EXCARD_N	8B2
L46	TRUE	TP_USB_EXTC_P	8B2
L48	TRUE	TP_USB_EXTC_N	8B2
L22	TRUE	USB2_BT_F_P	43C2
L22	TRUE	USB2_BT_F_N	43C2
L24	TRUE	USB2_3G_F_N	43A4
L24	TRUE	USB2_3G_F_P	43A4

DC-JACK FUNC_TEST

L57	TRUE	ACIN_ENABLE_GATE	57C3 66A6

Battery charger FUNC_TEST

L58	TRUE	PPVBAT_G3H_CHGR_OUT	66B5 66C2

INVERTER CONNECTOR FUNC_TEST

L60	TRUE	PPBUS_ALL_INV_CONN	67D3
L59	TRUE	INV_GND	67D2
L61	TRUE	PP5V_INV_F	67D3
L63	TRUE	INV_BKLIGHT_PWM_L	67D2

MIC FUNC_TEST

L22	TRUE	MIC_HI	55B3 56A6
L22	TRUE	MIC_LO	55B3 56A6
L22	TRUE	MIC_SHIELD	
L23	TRUE	MIC_HI_CONN	55B1 55D3
L23	TRUE	MIC_LO_CONN	55B1 55D3
L23	TRUE	MIC_SHLD_CONN	55A1 55D3 56A6

SPEAKER FUNC_TEST

L22	TRUE	SPKRCONN_L_N_OUT	54C1 55C2
L22	TRUE	SPKRCONN_L_P_OUT	54C1 55C2
L22	TRUE	SPKRCONN_R_N_OUT	54C1 55C2
L22	TRUE	SPKRCONN_R_P_OUT	54D1 55C2
L24	TRUE	SPKRCONN_SUB_N_OUT	54B1 55C2
L24	TRUE	SPKRCONN_SUB_P_OUT	54B1 55C2

THERMAL FUNC_TEST

L20	TRUE	THRM_HEATPIPE_P	49D6
L20	TRUE	THRM_HEATPIPE_N	49D6
L20	TRUE	THRM_DIMM_DX_F_N	49B6
L20	TRUE	THRM_DIMM_DX_F_P	49B6
L24	TRUE	THRM_FINSTACK_P	49C6
L24	TRUE	THRM_FINSTACK_N	49C6

FUNC TEST 1 OF 2

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 7 OF 106

"S0,S0M" RAILS

(REGULATOR OUTPUT CPU VCORE PWR)

59D1 =PPVORE_S0_CPU_REG → PPVCORE_S0_CPU (6B2)
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.3 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE

(CPU VCOR PWRE) → =PPVCORE_S0_CPU (10B5 10D7 11D7 48B3 48B5)

(REGULATOR OUTPUT CPU 0.90V PWR)

62B8 =PP0V9_S0_REG → PP0V9_S0 (6A2)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE

(DDR2 TERMINATION 0.9V PWR) → =PP0V9_S3M_MEM_TERM (32D4)

61B8 6B2 =PP1V05_S0_REG → PP1V05_S0 (6B2 45D2)
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V05_S0_SB_CPU_IO (22D2 25C3 26C4)
- =PPVCORE_S0_SB (25D3 26D2)

61C7 =PP1V05_S0_REG_R → PP1V05_S0_R (6B2)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- =PP1V05_S0_CPU (9B5 9B6 9C5 9D5 10C7 11A3 12B3 12C5)
- =PP1V05_S0_NB_PCIE (20D5)
- =PPVCORE_S0_NB (17D3 17D7 20B4 20D8)
- =PP1V25R1V05_S0_FSB_NB (13B7 29B6 29C6)
- =PP1V25R1V05_S0_NB_VTT (18D3 20C8)
- =PP1V05_S0M_NB_VCCAXM (17B3 17C1 20D8)

64B2 =PP1V25_S0_REG → PP1V25_S0 (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.25V, MAKE_BASE=TRUE)

- =PP1V25_S0_NB_PLL (7C7 20B4 20D3)
- =PP1V25_S0_NB_VCCDMI (18C3 20A8)
- =PP1V25_S0_SB_DMI (25C3 26A6)
- =PP1V25_S0_NB_VCCAXF (20D4)
- =PP1V25_S0_NB_PLL (7C7 20B4 20D3)
- =PP1V25_S0_NB_VCC (20A8)
- =PP1V25_S0_NB_VCCA (20B8)
- =PP1V25_S0_FET (58A3)

62C5 61B1 =PP1V5_S0_REG → PP1V5_S0 (6B2)
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE

- =PP1V5_S0_CPU (10B7 11B3)
- =PP1V5_S0_NB_TVDAC (21D8)
- =PP1V5_S0_SB (26A8 26C8 26D6)
- =PP1V5_S0_SB_VCC1_5_A_ARX (25B6 26D5)
- =PP1V5_S0_SB_VCC1_5_A_ATX (25B6 26C6)
- =PP1V5_S0_SB_VCC1_5_A (25B6 26C2)
- =PP1V5_S0_SB_VCCUSBPLL (25A6 26B6)
- =PP1V5_S0_SB_VCC1_5_A_USB_CORE (25B6 26C2)
- =PP1V5_S0_AIRPORT (33D2)
- =PP1V5_S0_NB_FOLLOW (21D5)

58C4 58B8 =PP1V8_S0_FET → PP1V8_S0 (6B2)
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8_S0_NB_LVDS (21C5)
- =PP1V8_S0_NB_DPLL (21A7)
- =PP1V8_S0_TMDS (68D6)

66C2 =PPVCORE_S0_NB_GFX_IMVP → PPVCORE_S0_NB_GFX (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=1.25V, MAKE_BASE=TRUE)

- =PPVCORE_S0_NB_GFX (17B7 17D5 21C5 48B3)

58D4 58C8 =PP5V_S0_FET → PP5V_S0 (6A2)
MIN_LINE_WIDTH=0.30 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=5V
MAKE_BASE=TRUE

- =PP5V_S0_SB (26D8)
- =PP5V_S0_SATA (40C6)
- =PP5V_S0_3G (43B5)
- =PP5V_S0_LPCPLUS (6D2 46C6)
- =PP5V_S0_ISENSECAL (48B8)
- =PP5V_S0_FAN_RT (6D2 50C4)
- =PP5V_S0_AUDIO (6D1 53A7 56C4)
- =PP5V_S0_AUDIO_AMP (6D1 54B8 54C8 54D8)
- =PP5V_S0_CPU_IMVP (59D8)
- =PP5V_S0_NB_GFX_IMVP (60D2)
- =PP5V_S0_LCD (67D7)
- =PP5V_S0_TMDS (69D7)
- =PP5V_S0_NB_TVDAC (21D6)
- =PP5V_S0_IDE_RESET (39B7)

58D3 58C4 58C3 58B8 58B3 58A3 =PP3V3_S0_FET → PP3V3_S0 (6A2 45D1)
MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S0_NB_VCCHV (15B7 15C7 18B3 20A8 21B7)
- =PP3V3_S0_NB_FOLLOW (20B2)
- =PP3V3_S0_SB_GPIO (22D2 22D7 24B3 24D8)
- =PP3V3_S0_SB_VCCGLAN3_3 (25A6)
- =PP3V3_S0_SB_VCC3_3_PCI (25B3 26B4)
- =PP3V3_S0_SB_VCC3_3_IDE (25C3 26B4)
- =PP3V3_S0_SB_VCC3_3_VCCPCORE (25C3 26A6 26C6)
- =PP3V3_S0_SB_VCC3_3_SATA (25C3 26B8)
- =PP3V3_S0_SB_VCC3_3_DMI (25C3 26A8)
- =PP3V3_S0_SB (26D8 39C8)
- =PP3V3_S0_SB_PM (27B6 27B8)
- =PP3V3_S0_RSTBUF (27D4)
- =PP3V3_S0_AIRPORT (33C6)
- =PP3V3_S0_FW (38C6)
- =PP3V3_S0_PATA (39C2)
- =PP3V3_S0_SMC_LS (45D4)
- =PP3V3_S0_LPCPLUS (46C4)
- =PP3V3_S0_SMBUS_SB (47D8)
- =PP3V3_S0_SMBUS_SMC_0_S0 (47D5)
- =PP3V3_S0_SMBUS_SMC_B_S0 (47C5)
- =PP3V3_S0_THRM_SNR (49C2 49D2)
- =PP3V3_S0_FAN_RT (6D2 50C4)
- =PP3V3_S0_ENET (8A4)
- =PP3V3_S0_AUDIO (53A7 53D7 55D8 56B5)
- =PP3V3_S0_IMVP (59D8)
- =PP3V3_S0_NB_GFX_IMVP (60C7)
- =PP3V3_S0_PDCISENS (60C2 61C5 66C3)
- =PP3V3_S0_LCD (67B5 67B7 67C6)
- =PP3V3_S0_TMDS (7C4 68B1 68B2 68B7 68C8 68D8 69B7 69C2 69C8)
- =PP3V3_S0_CPUPOWER (48D2)
- =PP3V3_S0_PBATTISENS (66B3)
- =PP3V3R1V5_S0_SB_VCCHDA (25B3 26C4)
- =PP3V3_S0_SB_PCI (23A3)
- =PP3V3_S0_NB_VCCA_PEG_BG (18C6 20A6)
- =PPSPD_S0_MEM (30A7 31A3 31A7)
- =PP3V3_S0MWOL_SB_VCCCL3_3 (25A6 26B2)
- =PP3V3_S0MWOL_SB_VCCLAN3_3 (25A3 26D3)
- =PP3V3_S0MWOL_SB_CLINK0 (24C1)
- =PP3V3_S0_CK505 (28C8 28D3 28D8 29B2 29D2)
- =PP3V3_S0_NB_VCCSYNC (18D6 21B5)
- =PP3V3_S0_NB (69C8)
- =PP3V3_S0_TMDS (7C4 68B1 68B2 68B7 68C8 68D8 69B7 69C2 69C8)

35C1 =PP1V2_ENET_REG → PP1V2_ENET_S0 (6A2)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE

- =PP1V2_ENET_PHY (34D6)

35D4 =PP3V3_ENET_FET → =PP3V3_ENET_PHY (34D6)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

35D1 35B2 =PP1V9_ENET_REG → PP1V9_ENET_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE

- =PP1V8_S0_YUKON (36D8)
- =PP1V8R2V5_ENET_PHY (34C7)

"S3" RAILS

62B2 =PP1V8_S3_REG → PP1V8_S3 (6A2)
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8_S3_FET (58C5)
- =PP1V8_S3_MEMVREF (20A5 20A6)
- =PP1V8_S3_MEM (30B2 30D4 30D6 31B2 31D4 31D6)
- =PP1V8_ENET_P1V8ENETFET (35C3)

62C4 =PP1V8_S3_REG_R → PP1V8_S3_MEM_NB
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE

- =PP1V8_S3M_MEM_NB (15D2 17D7 20C8 30D2 31D2)
- =PP1V8_S3_NB_VCC (20A4)

65C3 65A4 =PP3V3_S3_FET → PP3V3_S3 (6A2)
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S3_AIRPORT_AUX (33C2)
- =PP3V3_S3_FW (37D5)
- =PP3V3_S3_PCI (37C5)
- =PP3V3_S3_BT (43D3)
- =PP3V3_S3_SMS (51C7)
- =PP3V3_S3_SMBUS_SMC_A_S3 (47D3)
- =PP3V3_S3_PDCISENS (62A2 62C2)
- =PP3V3_S3_ENETPWRCTL (35D7)
- =PP3V3_S3_SMBUS_SMC_MGMT (47C3 51B6)
- =PP3V3_ENET_P3V3ENETFET (35D3)

65B4 =PP5V_S3_FET → PP5V_S3 (6A2)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

- =PP5V_S3_SYSLED (40B6 45A4)
- =PP5V_S3_GEYSER (42D6)
- =PP5V_S3_IR (43D8)
- =PP5V_S3_CAMERA (67A5)

"S5" RAILS

63B1 =PP3V3_S5_REG → PP3V3_S5 (6A2)
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S5_SB_PM (27C5)
- =PP3V3_S5_SB_USB (23C8)
- =PP3V3_S5_SB_GPIO (24D8)
- =PP3V3_S5_SB (24A3 24A8 26D8 35C7)
- =PP3V3_S5_FET (58C5 65A5 65C4)
- =PP3V3_S5_SB_VCCSUS3_3_USB (25A3 26D2)
- =PP3V3_S5_SB_VCCSUS3_3 (25A3 26B6 26D2)
- =PP3V3_S5_SB_3V3_VCCSUSHDA (25B3 26B2)
- =PP3V3_S5_FWLATEVG (38A6 38A8)
- =PP3V3_S5_SMBUS_SB_ME (47A7)
- =PP3V3_S5_ROM (52C6)
- =PP3V3_S5_LCD (67C7)
- =PP3V3_S5_SB_CLINK1 (24B1)
- =PP3V3_S5_1V25S0 (64B6)
- =PP3V3_S5_AIRPORT_AUX (33C7 33D6 33D7)

63B8 =PP5V_S5_REG → PP5V_S5 (6A2)
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE

- =PP5V_S5_SB (26D8)
- =PP5V_S5_PATA (39D6)
- =PP5V_S5_USB (41C8)
- =PP5V_S5_1V51V05S0 (61C4)
- =PP5V_S5_1V8S30V9S0 (62C5)
- =PP5V_S5_PWRCTL (65B6)
- =PP5V_S5_FET (58B3 58C6 58D5 65B5)

"G3H" RAILS

64C4 =PP3V42_G3H_REG → PP3V42_G3H (6A2)
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE

- =PP3V42_G3H_SMC (44D4 45C1 45D4 45D8 51B8)
- =PP3V42_G3H_SMCVREF (45C8)
- =PP3V42_G3H_SMBUS_SMC_BSA (47C3)
- =PP3V42_G3H_ACIN (57C4 66A5 66A8 66B8)
- =PP3V42_G3H_LIDSWITCH (57A8)
- =PP3V42_G3H_PWRCTL (65C7)
- =PP3V42_G3H_SB_RTC (27D7)
- =PP3V42_G3H_SMCUSBMUX (41A6)
- =PP3V42_G3H_LPCPLUS (6D2 46C6)

57D1 =PP18V5_G3H_INRUSH → PP18V5_G3H (6A2)
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

- =PP18V5_G3H_CHGR (66D8)

57D3 =PPDCIN_G3H → PPDCIN_G3H (MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=18.5V, MAKE_BASE=TRUE)

- =PPVIN_G3H_P3V42G3H (64C6)

66C2 =PPBUSA_G3H → PPBUS_G3H (6A2)
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE

- =PPVIN_S0_NB_DPLL
- =PPBUS_S5_FWPWRSW (38D5)
- =PPVIN_S5_CPU_IMVP (48D7 59C2 59D4 59D8)
- =PPVIN_S5_NB_GFX_IMVP (60C2)
- =PPBUS_S5_INV (67D4)
- =PPVIN_S5_1V8S30V9S0 (62B3)
- =PPVIN_S5_5VS5 (63A6 63B6)
- =PPVIN_S5_3V3S5 (63B3)
- =PPVIN_S5_1V5S0 (61B3)
- =PPVIN_S5_1V05S0 (61B5)
- =PPVIN_S5_IMVP (45A6)

66C2 =PPBUSB_G3H

Power Aliases

SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	8	106

(EMI PAD FOR INVERTER GONNECTOR)

INVT_CHGND — VOLTAGE=0V, MAKE_BASE=TRUE — ZS0920 EMI-SPRING CLIP-SM-M42

=GND_CHASSIS_3GPOWER

CHASSIS GND

BATTERY,AUDIO,DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_IO Z0906 OMIT 5R2P3-7SQBNP

=GND_BATT_CHGND
=GND_CHASSIS_AUDIO_JACK
=GND_CHASSIS_AUDIO_MIC
=GND_CHASSIS_DIPDIMM_LEFT

SATA,LVDS CONNECTOR CHASSIS GND

GND_CHASSIS_SATA Z0907 OMIT 6P5R2P6-7SQB — VOLTAGE=0V, MAKE_BASE=TRUE

=GND_CHASSIS_LVDS

C0907 0.1UF 10% 16V X5R 402
C0908 0.01UF 10% 16V CERM 402

DCIN CONNECTOR CHASSIS GND

GND_CHASSIS_DCIN Z0902 OMIT 7X7R2P3-5B — VOLTAGE=0V, MAKE_BASE=TRUE

=GND_DCIN_CHGND
=GND_CHASSIS_RJ45
=GND_CHASSIS_TMDS_UPPER

C0930 0.1UF 10% 16V X5R 402 — NOSTUFF

I/O CONNECTOR CHASSIS GND

GND_CHASSIS_IO Z0908 OMIT 5P0R2P3-7BLB — VOLTAGE=0V, MAKE_BASE=TRUE

=GND_CHASSIS_FW_DOWN
=GND_CHASSIS_USB

C0910 0.1UF 10% 16V X5R 402
C0911 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_CENTER Z0910 OMIT 5R2P3-7SQB — VOLTAGE=0V, MAKE_BASE=TRUE

=GND_CHASSIS_DIPDIMM_CENTER

C0916 0.1UF 10% 16V X5R 402
C0917 0.01UF 10% 16V CERM 402

DIP DIMM CONNECTOR CHASSIS GND

GND_CHASSIS_RIGHT Z0909 OMIT 5R2P3-7SQB — VOLTAGE=0V, MAKE_BASE=TRUE

=GND_CHASSIS_DIPDIMM_RIGHT

C0914 0.1UF 10% 16V X5R 402
C0915 0.01UF 10% 16V CERM 402

Z0901 OMIT 5R2P3-7SQBNP — GND_CHASSIS_CPU

C0912 0.1UF 10% 16V X5R 402
C0913 0.01UF 10% 16V CERM 402

Z0911 OMIT 5R2P3-7B — GND_CHASSIS_FANSCREW

C0918 0.1UF 10% 16V X5R 402
C0919 0.01UF 10% 16V CERM 402

CPU HEATSINK STANDOFF SCREW HOLE

Z0903 OMIT — STDOFF-4.2OD3.95H-5.52R3.37-6B — NB_RIGHT_DOWN_SCREW

R0912 0 5% 1/16W MF-LF 402

Z0904 OMIT — STDOFF-4.2OD3.95H-5.52R3.37-7SQB — CPU_THERMAL_SCREW_UP

R0910 0 5% 1/16W MF-LF 402

Z0903 USE SAME Z0913 NON SHAPE OF A HOOF SYMBOL FOR LAYOUT PLACEMENT
BUT, NEED CHANGE TO HIGH STANDOFF SYMBOL

Z0905 OMIT — STDOFF-4.5OD3.95H-1.1-3.2-TH — CPU_THERMAL_SCREW_DOWN

R0911 0 5% 1/16W MF-LF 402

Z0921 OMIT — STDOFF-4.5OD3.95H-1.1-3.2-TH — CPU_THERMAL_SCREW_RIGHT

R0921 0 5% 1/16W MF-LF 402

LVDS ALIASES

NO-CONNECT UNUSED LVDS INTERFACE PORTS

LVDS_B_CLK_N	LVDS_B_CLK_N_SPN
LVDS_B_CLK_P	LVDS_B_CLK_P_SPN
LVDS_B_DATA_N<0>	LVDS_B_DATA_N0_SPN
LVDS_B_DATA_N<1>	LVDS_B_DATA_N1_SPN
LVDS_B_DATA_N<2>	LVDS_B_DATA_N2_SPN
TP_LVDS_B_DATAN3	LVDS_B_DATA_N3_SPN
LVDS_B_DATA_P<0>	LVDS_B_DATA_P0_SPN
LVDS_B_DATA_P<1>	LVDS_B_DATA_P1_SPN
LVDS_B_DATA_P<2>	LVDS_B_DATA_P2_SPN
TP_LVDS_B_DATAP3	LVDS_B_DATA_P3_SPN
TP_LVDS_A_DATAP3	LVDS_A_DATA_P3_SPN
TP_LVDS_A_DATAN3	LVDS_A_DATA_N3_SPN

PCI_EXPRESS GRAPHICS ALIASES

NO-CONNECT UNUSED SDVO INTERFACE PORTS

PEG_D2R_N<0>	PEG_D2R_N0_SPN
PEG_D2R_N<2>	PEG_D2R_N2_SPN
PEG_D2R_N<3>	PEG_D2R_N3_SPN
PEG_D2R_N<4>	PEG_D2R_N4_SPN
PEG_D2R_N<5>	PEG_D2R_N5_SPN
PEG_D2R_N<6>	PEG_D2R_N6_SPN
PEG_D2R_N<7>	PEG_D2R_N7_SPN
PEG_D2R_N<8>	PEG_D2R_N8_SPN
PEG_D2R_N<9>	PEG_D2R_N9_SPN
PEG_D2R_N<10>	PEG_D2R_N10_SPN
PEG_D2R_N<11>	PEG_D2R_N11_SPN
PEG_D2R_N<12>	PEG_D2R_N12_SPN
PEG_D2R_N<13>	PEG_D2R_N13_SPN
PEG_D2R_N<14>	PEG_D2R_N14_SPN
PEG_D2R_N<15>	PEG_D2R_N15_SPN
PEG_D2R_P<0>	PEG_D2R_P0_SPN
PEG_D2R_P<2>	PEG_D2R_P2_SPN
PEG_D2R_P<3>	PEG_D2R_P3_SPN
PEG_D2R_P<4>	PEG_D2R_P4_SPN
PEG_D2R_P<5>	PEG_D2R_P5_SPN
PEG_D2R_P<6>	PEG_D2R_P6_SPN
PEG_D2R_P<7>	PEG_D2R_P7_SPN
PEG_D2R_P<8>	PEG_D2R_P8_SPN
PEG_D2R_P<9>	PEG_D2R_P9_SPN
PEG_D2R_P<10>	PEG_D2R_P10_SPN
PEG_D2R_P<11>	PEG_D2R_P11_SPN
PEG_D2R_P<12>	PEG_D2R_P12_SPN
PEG_D2R_P<13>	PEG_D2R_P13_SPN
PEG_D2R_P<14>	PEG_D2R_P14_SPN
PEG_D2R_P<15>	PEG_D2R_P15_SPN
PEG_R2D_C_N<4>	PEG_R2D_C_N4_SPN
PEG_R2D_C_N<5>	PEG_R2D_C_N5_SPN
PEG_R2D_C_N<6>	PEG_R2D_C_N6_SPN
PEG_R2D_C_N<7>	PEG_R2D_C_N7_SPN
PEG_R2D_C_N<8>	PEG_R2D_C_N8_SPN
PEG_R2D_C_N<9>	PEG_R2D_C_N9_SPN
PEG_R2D_C_N<10>	PEG_R2D_C_N10_SPN
PEG_R2D_C_N<11>	PEG_R2D_C_N11_SPN
PEG_R2D_C_N<12>	PEG_R2D_C_N12_SPN
PEG_R2D_C_N<13>	PEG_R2D_C_N13_SPN
PEG_R2D_C_N<14>	PEG_R2D_C_N14_SPN
PEG_R2D_C_N<15>	PEG_R2D_C_N15_SPN
PEG_R2D_C_P<4>	PEG_R2D_C_P4_SPN
PEG_R2D_C_P<5>	PEG_R2D_C_P5_SPN
PEG_R2D_C_P<6>	PEG_R2D_C_P6_SPN
PEG_R2D_C_P<7>	PEG_R2D_C_P7_SPN
PEG_R2D_C_P<8>	PEG_R2D_C_P8_SPN
PEG_R2D_C_P<9>	PEG_R2D_C_P9_SPN
PEG_R2D_C_P<10>	PEG_R2D_C_P10_SPN
PEG_R2D_C_P<11>	PEG_R2D_C_P11_SPN
PEG_R2D_C_P<12>	PEG_R2D_C_P12_SPN
PEG_R2D_C_P<13>	PEG_R2D_C_P13_SPN
PEG_R2D_C_P<14>	PEG_R2D_C_P14_SPN
PEG_R2D_C_P<15>	PEG_R2D_C_P15_SPN

HDA ALIASES

HDA_BIT_CLK	ACZ_BITCLK
HDA_SYNC	ACZ_SYNC
HDA_RST_L	ACZ_RST_L
HDA_SDIN0	ACZ_SDATAIN<0>
HDA_SDOUT	ACZ_SDATAOUT
TP_HDA_SDIN1	HDN_SDIN1_SPN
TP_HDA_SDIN2	HDN_SPIN2_SPN
TP_HDA_SDIN3	HDN_SPIN3_SPN

NB CFG ALIASES

NB_CFG<3>	TP_NB_CFG<3>
NB_CFG<4>	TP_NB_CFG<4>
NB_CFG<6>	TP_NB_CFG<6>
NB_CFG<7>	TP_NB_CFG<7>
NB_CFG<8>	TP_NB_CFG<8>

GND_CHASSIS_IO1 — VOLTAGE=0V, MAKE_BASE=TRUE

=GND_CHASSIS_TMDS_DOWN
=GND_CHASSIS_FW_UPPER

SATA ALIASES

NO-CONNECT UNUSED SATA INTERFACE PORTS

SATA_B_D2R_N	SATA_B_D2R_N_SPN
SATA_B_D2R_P	SATA_B_D2R_P_SPN
SATA_B_R2D_C_N	SATA_B_R2D_C_N_SPN
SATA_B_R2D_C_P	SATA_B_R2D_C_P_SPN
SATA_C_D2R_N	SATA_C_D2R_N_SPN
SATA_C_D2R_P	SATA_C_D2R_P_SPN
SATA_C_R2D_C_N	SATA_C_R2D_C_N_SPN
SATA_C_R2D_C_P	SATA_C_R2D_C_P_SPN

PCI_EXP ALIASES

NO-CONNECT UNUSED PCI_EXP INTERFACE PORTS

TP_PCIE_A_D2R_N	PCIE_A_D2R_N_SPN
TP_PCIE_A_D2R_P	PCIE_A_D2R_P_SPN
TP_PCIE_A_R2D_C_N	PCIE_A_R2D_C_N_SPN
TP_PCIE_A_R2D_C_P	PCIE_A_R2D_C_P_SPN
TP_PCIE_B_D2R_N	PCIE_B_D2R_N_SPN
TP_PCIE_B_D2R_P	PCIE_B_D2R_P_SPN
TP_PCIE_B_R2D_C_N	PCIE_B_R2D_C_N_SPN
TP_PCIE_B_R2D_C_P	PCIE_B_R2D_C_P_SPN
TP_PCIE_EXCARD_D2R_N	PCIE_C_D2R_N_SPN
TP_PCIE_EXCARD_D2R_P	PCIE_C_D2R_P_SPN
TP_PCIE_EXCARD_R2D_C_N	PCIE_C_R2D_C_N_SPN
TP_PCIE_EXCARD_R2D_C_P	PCIE_C_R2D_C_P_SPN
TP_PCIE_FW_D2R_N	PCIE_D_D2R_N_SPN
TP_PCIE_FW_D2R_P	PCIE_D_D2R_P_SPN
TP_PCIE_FW_R2D_C_N	PCIE_D_R2D_C_N_SPN
TP_PCIE_FW_R2D_C_P	PCIE_D_R2D_C_P_SPN

CLOCK ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

TP_CK505_SRC1_N	CK505_SRC1_N_SPN
TP_CK505_SRC1_P	CK505_SRC1_P_SPN
TP_CK505_SRC3_N	CK505_SRC3_N_SPN
TP_CK505_SRC3_P	CK505_SRC3_P_SPN
TP_CK505_SRC7_N	CK505_SRC7_N_SPN
TP_CK505_SRC7_P	CK505_SRC7_P_SPN
CK505_PCI2_CLK	CK505_PCI2_CLK_SPN
CK505_PCI4_CLK	CK505_PCI4_CLK_SPN
=ENET_CLKREQ_L	ENET_CLKREQ_L

SB ALIASES

NO-CONNECT UNUSED CLOCK INTERFACE PORTS

VR_PWRGD_CLKEN	VR_PWRGD_CK505
=SB_CLINK_MPWROK	CLINK_MPWROK
=SB_SATA_CLKREQ_L	SB_CLK100M_SATA_OE_L
EXTGPU_RST_L	TP_SB_GPIO17

SO-DIMM ALIASES

NO-CONNECT UNUSED ADDRESS INTERFACE PORTS

MEM_A_A<15>	MEM_A_A15_SPN
MEM_B_A<15>	MEM_B_A15_SPN
TP_MEM_CLKP2	MEM_CLK_P_2_SPN
TP_MEM_CLKN2	MEM_CLK_N_2_SPN
TP_MEM_CLKP5	MEM_CLK_P_5_SPN
TP_MEM_CLKN5	MEM_CLK_N_5_SPN

=GND_AUDIO_CODEC — GND_AUDIO_CODEC — XW0801 SM
=GND_AUDIO_AMP — GND_AUDIO_AMP — XW0802 SM

Ethernet ALIASES

=PP3V3_S0_ENET — =ENET_VMAIN_AVLBL
=YUKON_EC_PP2V5_ENET

AIRPORT CARD STANDOFF SCREW HOLE

Z0912 OMIT — STDOFF-4.2OD2.15H-1.2-3.2-TH — NC

Z0913 OMIT — STDOFF-4.2OD3.95H-5.52R3.37-6B — NC

FIREWIRE ALIASES

NO-CONNECT UNUSED FIREWIRE INTERFACE PORTS

FW_B_TPBIAS	FW_B_TPBIAS_SPN
FW_B_TPA_P	FW_B_TPA_P_SPN
FW_B_TPA_N	FW_B_TPA_N_SPN
FW_B_TPB_P	FW_B_TPB_P_SPN
FW_B_TPB_N	FW_B_TPB_N_SPN
FW_C_TPBIAS	FW_C_TPBIAS_SPN
FW_C_TPA_P	FW_C_TPA_P_SPN
FW_C_TPA_N	FW_C_TPA_N_SPN
FW_C_TPB_P	FW_C_TPB_P_SPN
FW_C_TPB_N	FW_C_TPB_N_SPN

USB PORT [0] = External USB2.0 Port A

=USB2_EXTA_P — USB2_EXTA_P — USB_EXTA_P
=USB2_EXTA_N — USB2_EXTA_N — USB_EXTA_N
=EXTAUSB_OC_L — EXTAUSB_OC_L — USB_EXTA_OC_L

USB PORT [1] = PCI-E Mini Card

=USB2_AIRPORT_P — USB2_AIRPORT_P — USB_MINI_P
=USB2_AIRPORT_N — USB2_AIRPORT_N — USB_MINI_N

USB PORT [2] = 3G USB

=USB2_3G_P — USB2_3G_P — USB_EXTD_P
=USB2_3G_N — USB2_3G_N — USB_EXTD_N

USB PORT [3] = CAMERA

=USB2_CAMERA_P — USB2_CAMERA_P — USB_CAMERA_P
=USB2_CAMERA_N — USB2_CAMERA_N — USB_CAMERA_N

USB PORT [4] = IR CONTROLLER

=USB2_IR_P — USB_IR_P
=USB2_IR_N — USB_IR_N

USB PORT [5] = Trackpad(Geyser)

=USB2_GEYSER_P — USB2_GEYSER_P — USB_TPAD_P
=USB2_GEYSER_N — USB2_GEYSER_N — USB_TPAD_N

USB PORT [6] = BLUETOOTH

=USB2_BT_P — USB_BT_P
=USB2_BT_N — USB_BT_N

USB PORT [7] = External USB2.0 Port B

=USB2_EXTB_P — USB2_EXTB_P — USB_EXTB_P
=USB2_EXTB_N — USB2_EXTB_N — USB_EXTB_N
=EXTBUSB_OC_L — EXTBUSB_OC_L — USB_EXTB_OC_L

USB PORT [8] = Unused

TP_USB_EXCARD_P — USB_EXCARD_P
TP_USB_EXCARD_N — USB_EXCARD_N

USB PORT [9] = Unused

TP_USB_EXTC_P — USB_EXTC_P
TP_USB_EXTC_N — USB_EXTC_N

ANALOG SWITCH GPIO

PM_EXTTS_L<0> — DIMM_OVERTEMPA_L
PM_EXTTS_L<1> — DIMM_OVERTEMPB_L

NB ALIASES

=GFX_VR_EN	GFX_VR_EN
=NB_CLINK_MPWROK	CLINK_MPWROK
=NB_CLK96M_DOT_P	NB_CLK96M_DOT_P
=NB_CLK96M_DOT_N	NB_CLK96M_DOT_N
=NB_CLK100M_DPLLSS_P	NB_CLK100M_DPLLSS_P
=NB_CLK100M_DPLLSS_N	NB_CLK100M_DPLLSS_N
=NB_TDE_SENSE	
=NB_TDE_FORCE	
=NB_TDB_EORCE	
=NB_TDB_SENSE	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
860-0964	4	THERMAL STANDOFF	Z0903,Z0904,Z0905,Z0921	STANDOFF
860-0723	1	STANDOFF WIRELESS	Z0912	STANDOFF
860-0749	1	STANDOFF W/THRU HOLES,WIRELESS	Z0913	STANDOFF

SIGNAL ALIAS /RESET

SYNC_MASTER=GPU — SYNC_DATE=07/17/2006

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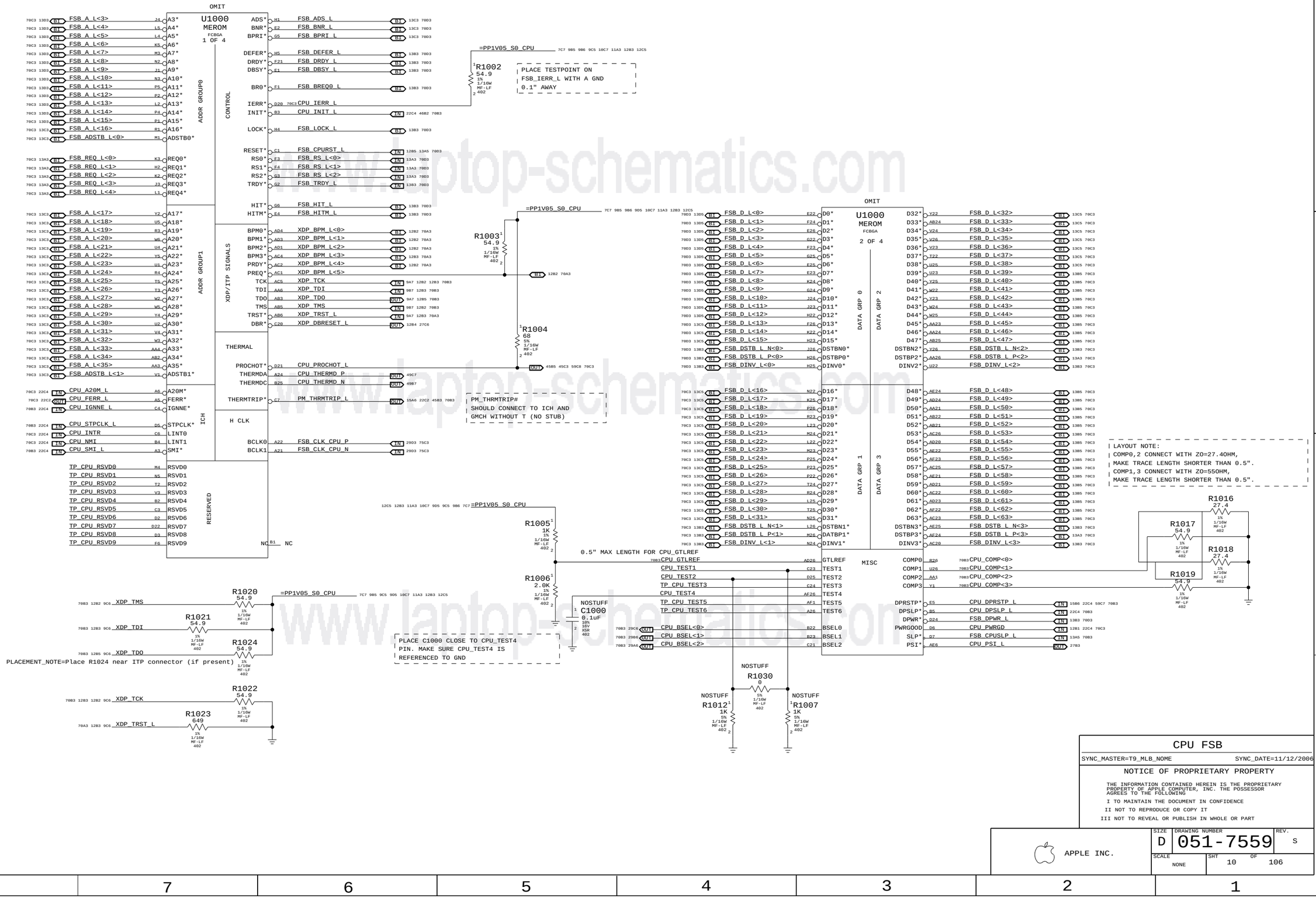
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE — SHT 9 OF 106



CPU FSB

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	10	106

(CPU CORE POWER)

=PPVCORE_S0_CPU 7D7 10B5 11D7 48B3 48B5

Standard Voltage:

44.0 A (Design Target)

41.0 A (HFM)
30.4 A (LFM)
25.5 A (SuperLFM)

27.4 A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)

27.4 A (Sleep HFM)
16.8 A (Sleep SuperLFM)

25.0 A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)

11.5 A (Deeper Sleep)

9.4 A (Enhanced Deeper Sleep)

Low Voltage:

23.0 A (Design Target)

21.0 A (HFM)
18.7 A (LFM)
TBD A (SuperLFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant SuperLFM)

TBD A (Sleep HFM)
TBD A (Sleep SuperLFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep SuperLFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

17.0 A (Design Target)

TBD A (HFM)
TBD A (LFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant LFM)

TBD A (Sleep HFM)
TBD A (Sleep LFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep LFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

OMIT
U1000
MEROM
FCBGA
3 OF 4

VCC
VCCP
VCCA
VSS

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 7C7 9B5 9B6 9C5 9D5 11A3 12B3 12C5

4500 mA (before VCC stable)
2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 7C7 11B3

130 mA

VID0 CPU_VID<0> OUT 59C7 70A3
VID1 CPU_VID<1> OUT 59C7 70A3
VID2 CPU_VID<2> OUT 59C7 70A3
VID3 CPU_VID<3> OUT 59C7 70A3
VID4 CPU_VID<4> OUT 59C7 70A3
VID5 CPU_VID<5> OUT 59C7 70A3
VID6 CPU_VID<6> OUT 59C7 70A3

VCCSENSE CPU_VCCSENSE_P OUT 59A4 59A5 70A3

VSSSENSE CPU_VCCSENSE_N OUT 59A4 59A5 70A3

=PPVCORE_S0_CPU 7D7 10D7 11D7 48B3 48B5

R1100
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1%
1/16W
MF-LF
402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
MEROM
FCBGA
4 OF 4

VSS

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

CPU Power & Ground

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/12/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 11 OF 106

CPU VCORE HF AND BULK DECOUPLING

4x 330uF. 20x 10uF 0805

4885 4883 16D7 10B5 7D7 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

CRITICAL C1200 10UF 20% 6.3V X5R 805-2	CRITICAL C1201 10UF 20% 6.3V X5R 805-2	CRITICAL C1202 10UF 20% 6.3V X5R 805-2	CRITICAL C1203 10UF 20% 6.3V X5R 805-2	CRITICAL C1204 10UF 20% 6.3V X5R 805-2	CRITICAL C1205 10UF 20% 6.3V X5R 805-2	CRITICAL C1206 10UF 20% 6.3V X5R 805-2	CRITICAL C1207 10UF 20% 6.3V X5R 805-2	CRITICAL C1208 10UF 20% 6.3V X5R 805-2	CRITICAL C1209 10UF 20% 6.3V X5R 805-2

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

CRITICAL C1210 10UF 20% 6.3V X5R 805-2	CRITICAL C1211 10UF 20% 6.3V X5R 805-2	CRITICAL C1212 10UF 20% 6.3V X5R 805-2	CRITICAL C1213 10UF 20% 6.3V X5R 805-2	CRITICAL C1214 10UF 20% 6.3V X5R 805-2	CRITICAL C1215 10UF 20% 6.3V X5R 805-2	CRITICAL C1216 10UF 20% 6.3V X5R 805-2	CRITICAL C1217 10UF 20% 6.3V X5R 805-2	CRITICAL C1218 10UF 20% 6.3V X5R 805-2	CRITICAL C1219 10UF 20% 6.3V X5R 805-2

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CRITICAL C1250 330UF 10% 2.0V TANT D2T	CRITICAL C1251 330UF 10% 2.0V TANT D2T
CRITICAL C1252 330UF 10% 2.0V TANT D2T	CRITICAL C1253 330UF 10% 2.0V TANT D2T

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

C1250, C1251, C1252 AND C1253 NEED TO USE 6mOHM CAPS.

VCCA (CPU AVdd) DECOUPLING

1087 7C7 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

C1280 10uF 20% 6.3V X5R 603

C1281 0.01UF 10% 16V CERM 402

LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

12C5 12B3 10C7 9D5 9C5 9B6 9B5 7C7 =PP1V05_S0_CPU

1X 330UF, 6X 0.1UF

CRITICAL C1235 330UF 20% 2.5V TANT D2T	C1236 0.1UF 20% 10V CERM 402	C1237 0.1UF 20% 10V CERM 402	C1238 0.1UF 20% 10V CERM 402	C1239 0.1UF 20% 10V CERM 402	C1240 0.1UF 20% 10V CERM 402	C1241 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

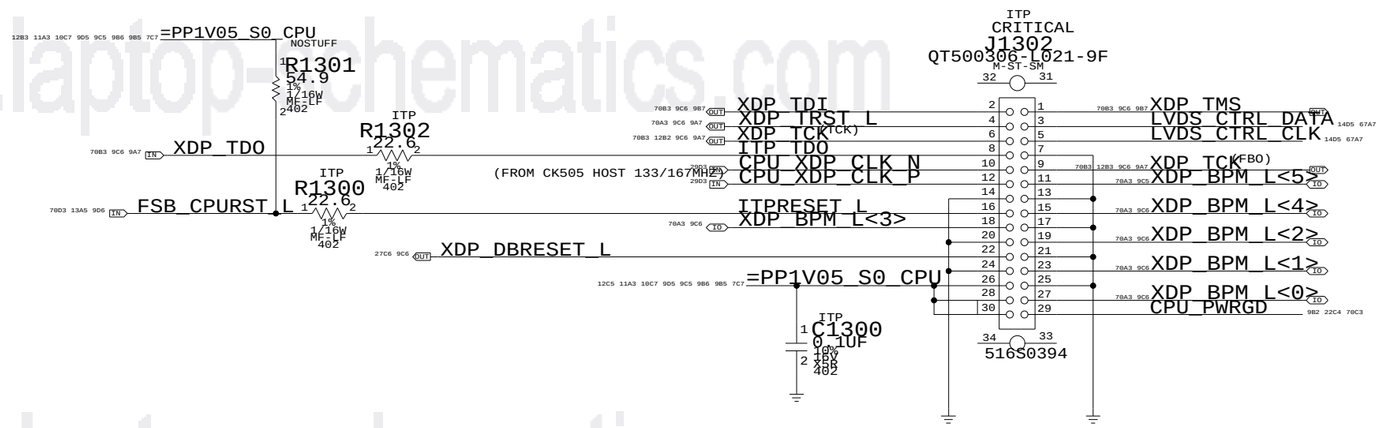
SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE SHT 12 OF 106

CPU ITP700FLEX DEBUG SUPPORT



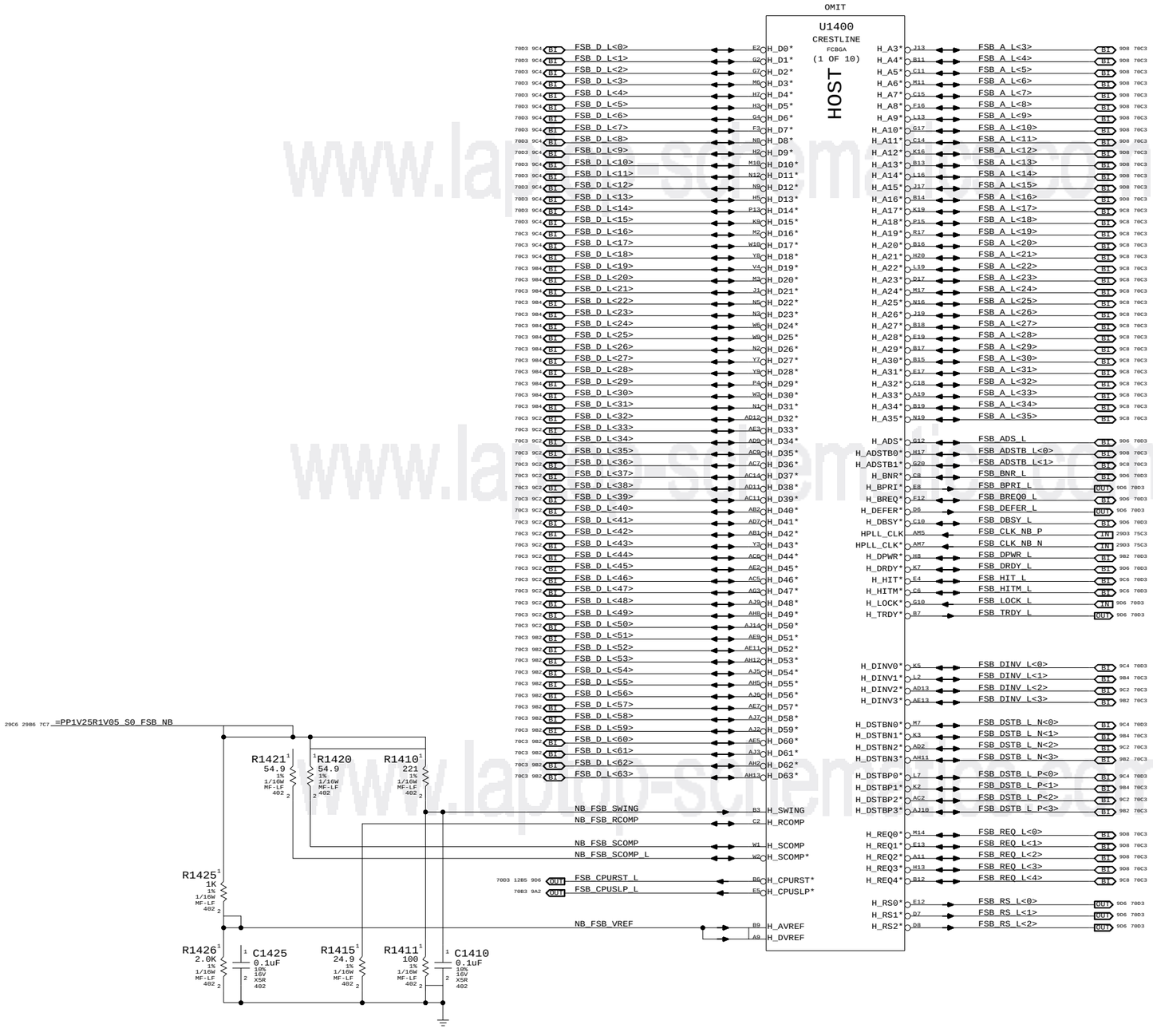
(DBA#)INDICATE THAT ITP IS USING TAP I/F, NC IN 965GM CHIPSET SYSTEM.
(DEBUG PORT ACTIVE)
(DBR#)TO ICH8M SYS_RST*, AND WITH SYSTEM RESET LOGIC
(DEBUG PORT RESET)

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG
SYNC_MASTER=MASTER SYNC_DATE=5/23/05

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 13 OF 106	



NB CPU Interface

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	14	106

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND.
All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

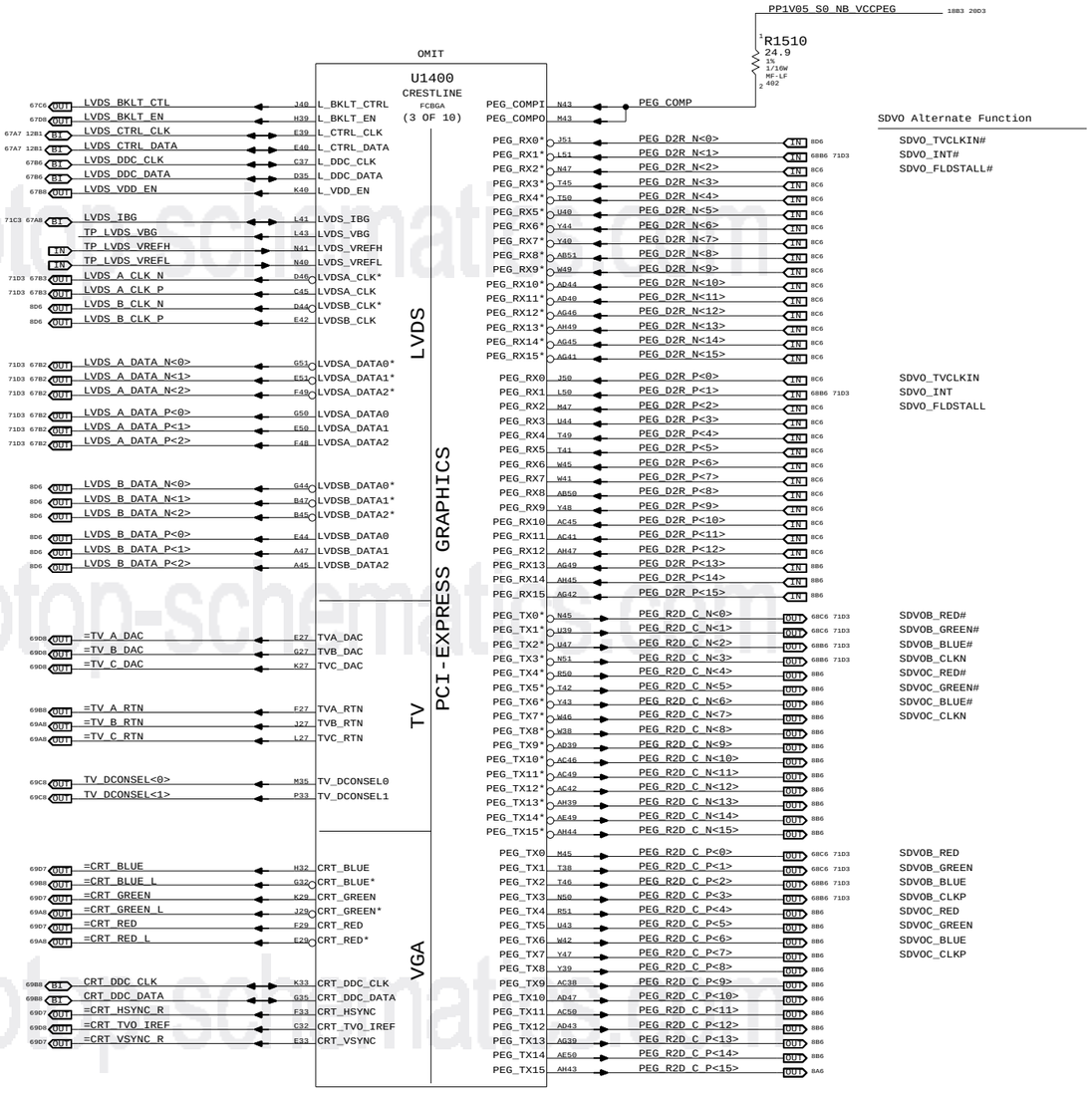
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	15	106

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

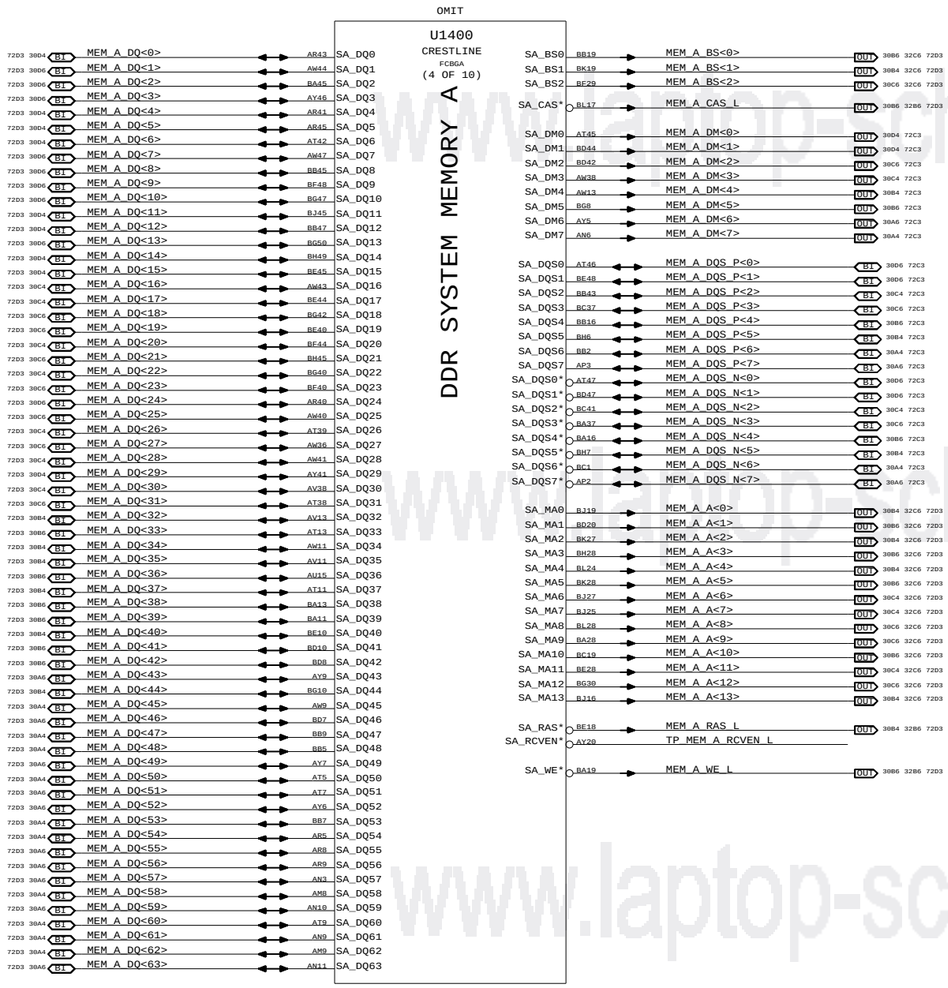
Clk used for PEG and DMI

NB Misc Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 16 OF 106	



NB DDR2 Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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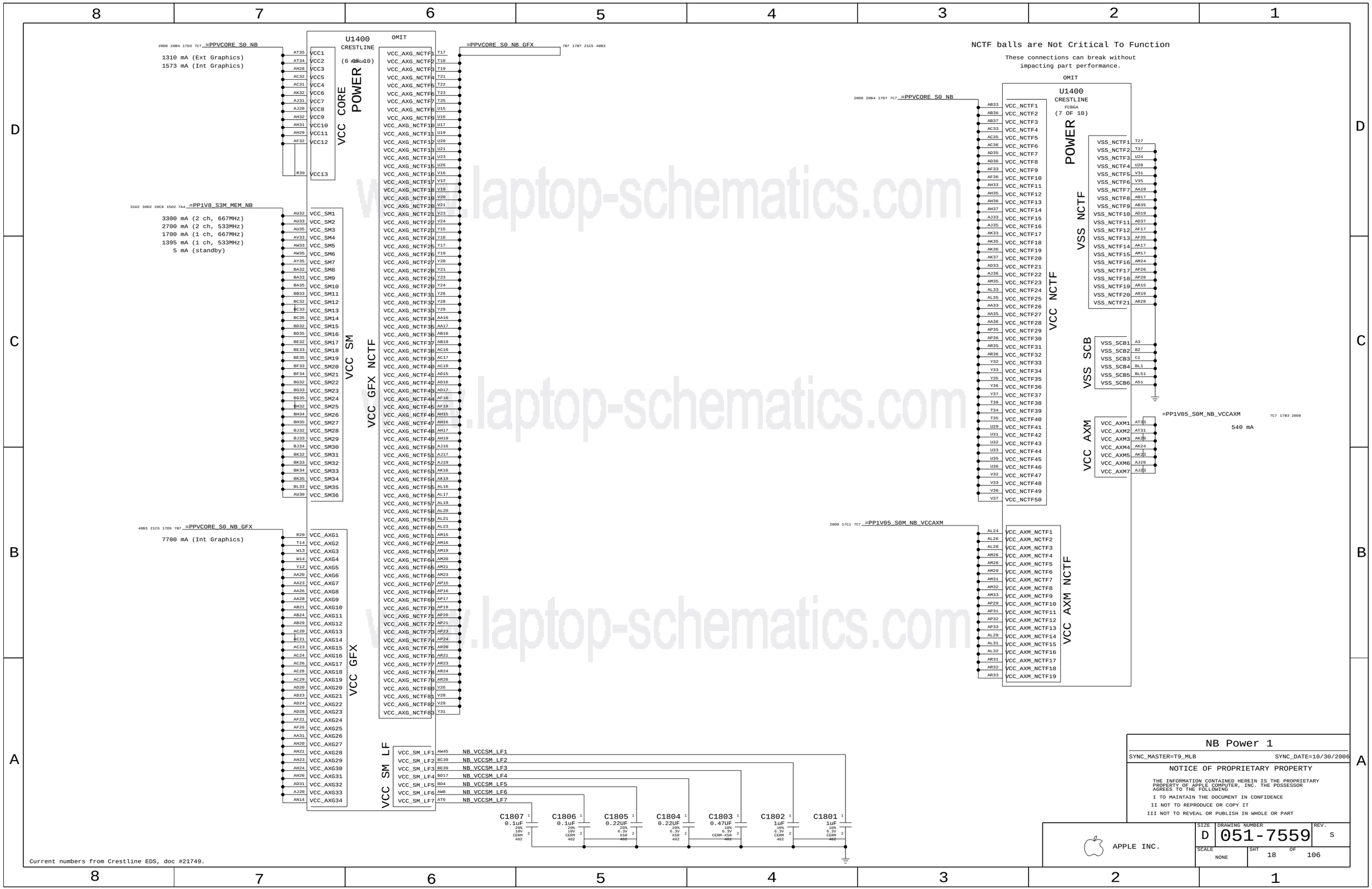
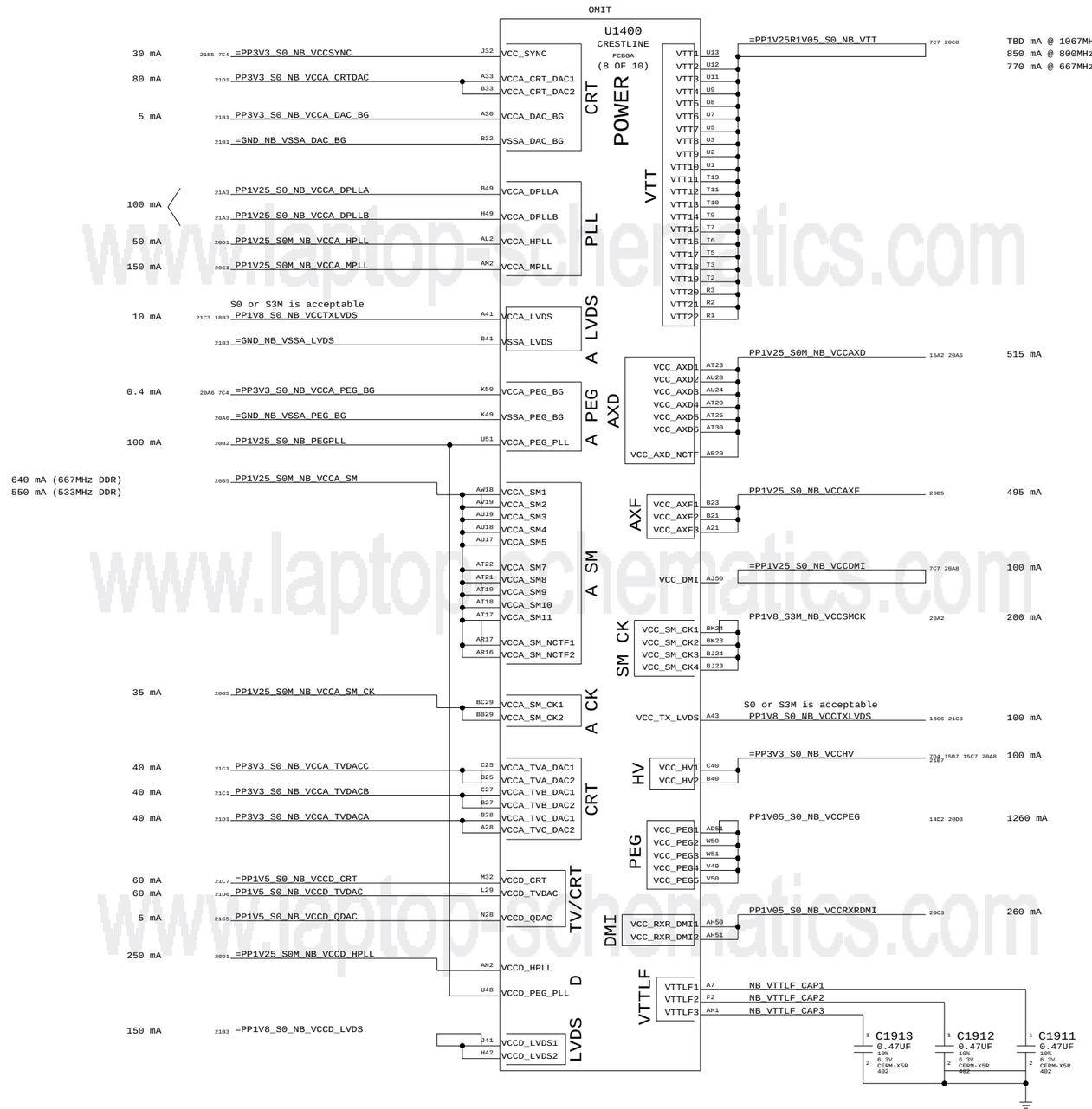
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	17	106





Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	19	106

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE	VSS302 T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE	VSS303 T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE	VSS304 T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE	VSS305 R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

=NB_TDE_SENSE 8A2

NOTE: TDE = _P

=NB_TDE_FORCE 8A2

=NB_TDB_FORCE 8A2

NOTE: TDB = _N

=NB_TDB_SENSE 8A2

NB Grounds

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	20	106

GMCH Core Power

=PPVCORE_S0_NB

CRITICAL
C2100 470UF 20% 2.5V POLY TANT D2T

C2101 22UF 20% 6.3V CERM 805
C2102 0.22UF 20% 6.3V X5R 402
C2103 0.22UF 20% 6.3V X5R 402
C2104 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place in GMCH cavity

GMCH ME Core Power

=PP1V05_S0M_NB_VCCAXM

540 mA

C2110 22UF 20% 6.3V CERM 805
C2111 0.22UF 20% 6.3V X5R 402
C2112 0.22UF 20% 6.3V X5R 402
C2113 0.1UF 20% 10V CERM 402
C2114 0.1UF 20% 10V CERM 402
C2115 0.1UF 20% 10V CERM 402

GMCH FSB I/O Rail

=PP1V25R1V05_S0_NB_VTT

850 mA

C2121 4.7uF 20% 6.3V CERM 603
C2122 4.7uF 20% 6.3V CERM 603
C2123 2.2uF 20% 6.3V CERM1 603
C2124 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place close to U1400

WF: Matanzas has 270uF

GMCH Memory I/O Rail

=PP1V8_S3M_MEM_NB

2400 mA

this is "1 of 2" 1.8V bulk decoupling caps.

OMIT
CRITICAL
C2130 330UF 20% 2.5V POLY CASE-C2

C2135 0.1UF 20% 10V CERM 402
C2131 22UF 20% 6.3V CERM 805
C2132 22UF 20% 6.3V CERM 805

PLACEMENT_NOTE=Place close to U1400

WF: "Place where LVDS and DDR2 taps." (C2125)

I/O voltage Supply

=PP1V25_S0_NB_VCCAXF

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.25V

=PP1V25_S0_NB_VCCAXF

350 mA

C2170 10uF 20% 6.3V X5R 603
C2171 1UF 10% 6.3V CERM 402

CRITICAL
L2173 91NH 1210

=PP1V05_S0_NB_PCIE

1450 mA

Layout Note:
Place L and C
close to MCH

Analog,I/O logic,and Term Voltage for PCI-E Graphics

PP1V05_S0_NB_VCCPEG

MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

1200 mA

OMIT
CRITICAL
C2173 220UF 20% 2.5V POLY CASE-B2

C2174 10uF 20% 6.3V X5R 603

Layout Note:
10uF caps should
be close to MCH
on opposite side.

RX and I/O Logic for DMI

PP1V05_S0_NB_VCCRXRDMI

MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

250 mA

C2177 10uF 20% 6.3V X5R 603

Layout Note:
10uF caps should
be close to MCH
on opposite side.

Host PLL Digital Supply

=PP1V25_S0M_NB_VCCD_HPLL

250 mA

C2180 0.1UF 20% 10V CERM 402

=PP1V25_S0_NB_PLL

450 mA

250mA,0.5ohm
L2181 120-OHM-0.3A-EMI 0402-LF

Host PLL Analog Supply

PP1V25_S0M_NB_VCCA_HPLL

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

50 mA

C2181 22UF 20% 6.3V CERM 805

C2182 0.1UF 20% 10V CERM 402

250mA,0.5ohm
L2183 120-OHM-0.3A-EMI 0402-LF

MPLL Analog Supply

PP1V25_S0M_NB_VCCA_MPLL

MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

150 mA

R2183 0.51 1% 1/10W MF-LF 402

C2184 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2184 by U1400.AM2

PP1V25_S0M_NB_MPLL_RC

MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2183 22UF 20% 6.3V CERM 805

These supplies are still needed even using external GPU

spec requires "3.9uH ferrite,1A,32mohm max". Memory I/O logic and DLL voltage.

=PP1V25_S0_NB_VCCA

??? mA

R2141 0 5% 1/16W MF-LF 402

OMIT
CRITICAL
C2140 330UF 20% 2.0V POLY CASE-B2

C2142 22UF 20% 6.3V CERM 805
C2143 4.7UF 10% 6.3V X5R-CERM 603
C2144 1UF 10% 6.3V CERM 402

PP1V25_S0M_NB_VCCA_SM

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

??? mA

Memory clock logic voltage.

R2145 0 5% 1/16W MF-LF 402

C2145 22UF 20% 6.3V CERM 805
NOSTUFF
C2147 2.2UF 20% 6.3V CERM 402-LF
C2148 0.1UF 20% 10V CERM 402

PP1V25_S0M_NB_VCCA_SM_CK

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

??? mA

5.6nH,0.9A,45mohm max.no bigger than 0603

Memory voltage supply.

=PP1V25_S0_NB_VCC

200 mA

R2109 0 5% 1/16W MF-LF 402

NOSTUFF
C2150 10uF 20% 6.3V X5R 603

C2151 1UF 10% 6.3V CERM 402

PP1V25_S0M_NB_VCCAXD

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

200 mA

=PP1V8_S3_MEMVREF

R2112 1K 1% 1/10W MF-LF 402

PP0V9_S3M_MEM_NBVREFA

MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V

=PP0V9_S3M_MEM_NBVREFA

R2113 1K 1% 1/10W MF-LF 402

=PP1V8_S3_MEMVREF

R2110 1K 1% 1/10W MF-LF 402

PP0V9_S3M_MEM_NBVREFB

MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V

=PP0V9_S3M_MEM_NBVREFB

R2111 1K 1% 1/10W MF-LF 402

LAYOUT NOTE: PLACE THOSE COMPONENT CLOSE TO GMCH

D2186 1SS418 SOD-723

=PPVCORE_S0_NB

PP3V3_S0_NBCORE_FOLLOW_R

MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

R2186 10 1% 1/16W MF-LF 402

=PP3V3_S0_NB_FOLLOW

NOTE: This follower is redundant if VCORE is always 1.05V.

WF: 220-ohm

L2190 FERR-220-OHM-2.5A 0603

=PP1V25_S0_NB_PLL

100 mA

R2190 1.1 1% 1/16W MF-LF 402

WF: Should be 1.0, 1%

Analog PLL Voltage for PCI-E GPU

PP1V25_S0_NB_PEGPLL

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

100 mA

C2191 0.1UF 20% 10V CERM 402

C2192 0.1UF 20% 10V CERM 402

PP1V25_S0_NB_PEGPLL_RC

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2190 10uF 20% 6.3V X5R 603

need to find "1uH,220mA,150mohm max"

=PP1V8_S3_NB_VCC

200 mA

L2195 1.0UH-0.23A 0603

R2195 1.1 1% 1/16W MF-LF 402

WF: Should be 1.0, 1%

PP1V8_S3_NB_VCCSMCK

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

200 mA

C2196 22UF 20% 6.3V CERM 805

C2197 0.1UF 20% 10V CERM 402

PP1V8_S3_NB_VCCSMCK_RC

MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

C2195 10UF 20% 6.3V X5R 603

100 mA =PP3V3_S0_NB_VCCHV

100 mA =PP1V25_S0_NB_VCCDMI

C2160 0.1UF 20% 10V CERM 402

C2161 0.1UF 20% 10V CERM 402

=PP3V3_S0_NB_VCCA_PEG_BG

C2165 0.1UF 20% 10V CERM 402

5 mA

=GND_NB_VSSA_PEG_BG

Layout Note: Route to caps, then GND

Current numbers from Crestline EDS Addendum, doc #20127.

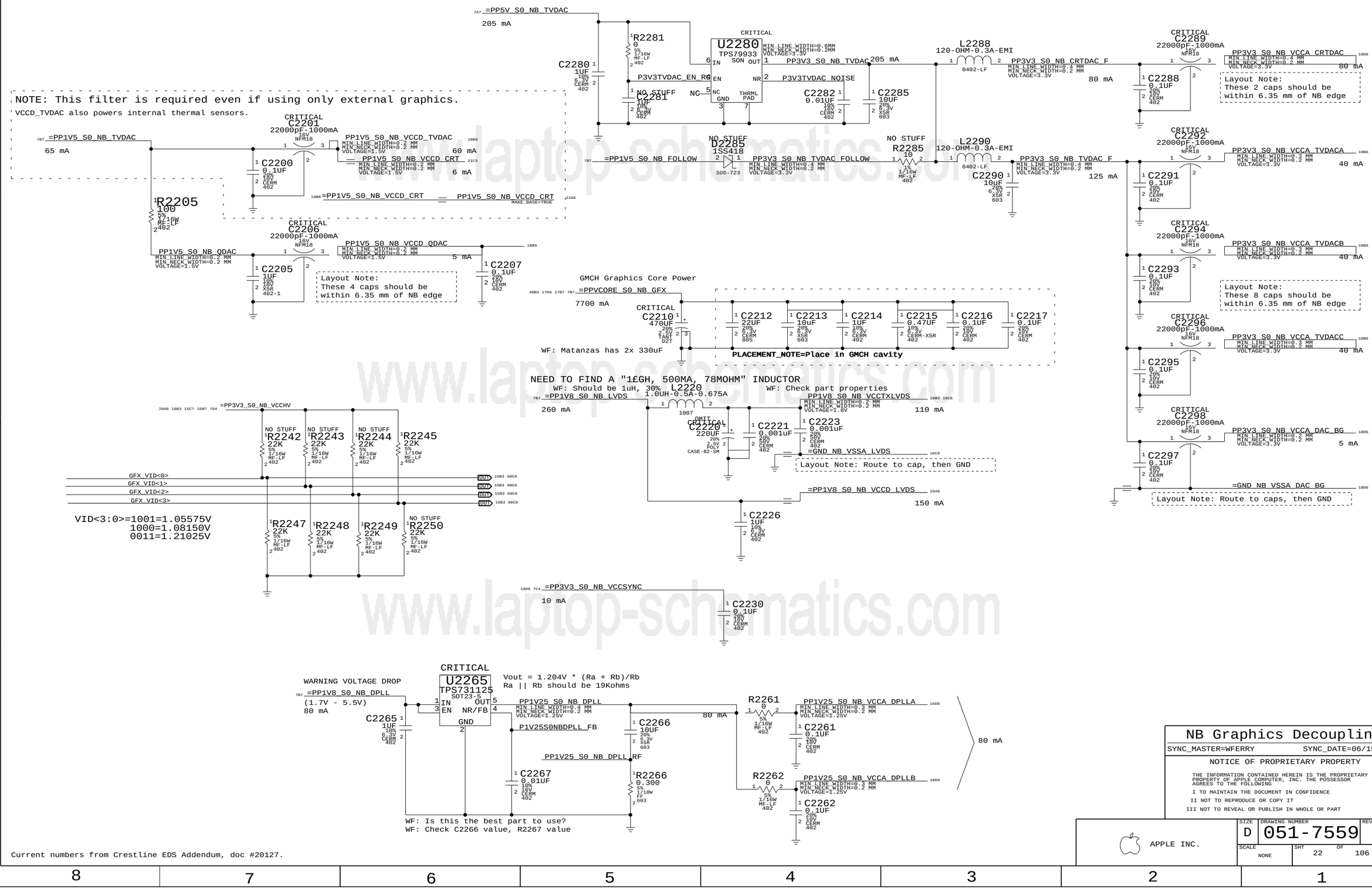
NB Standard Decoupling

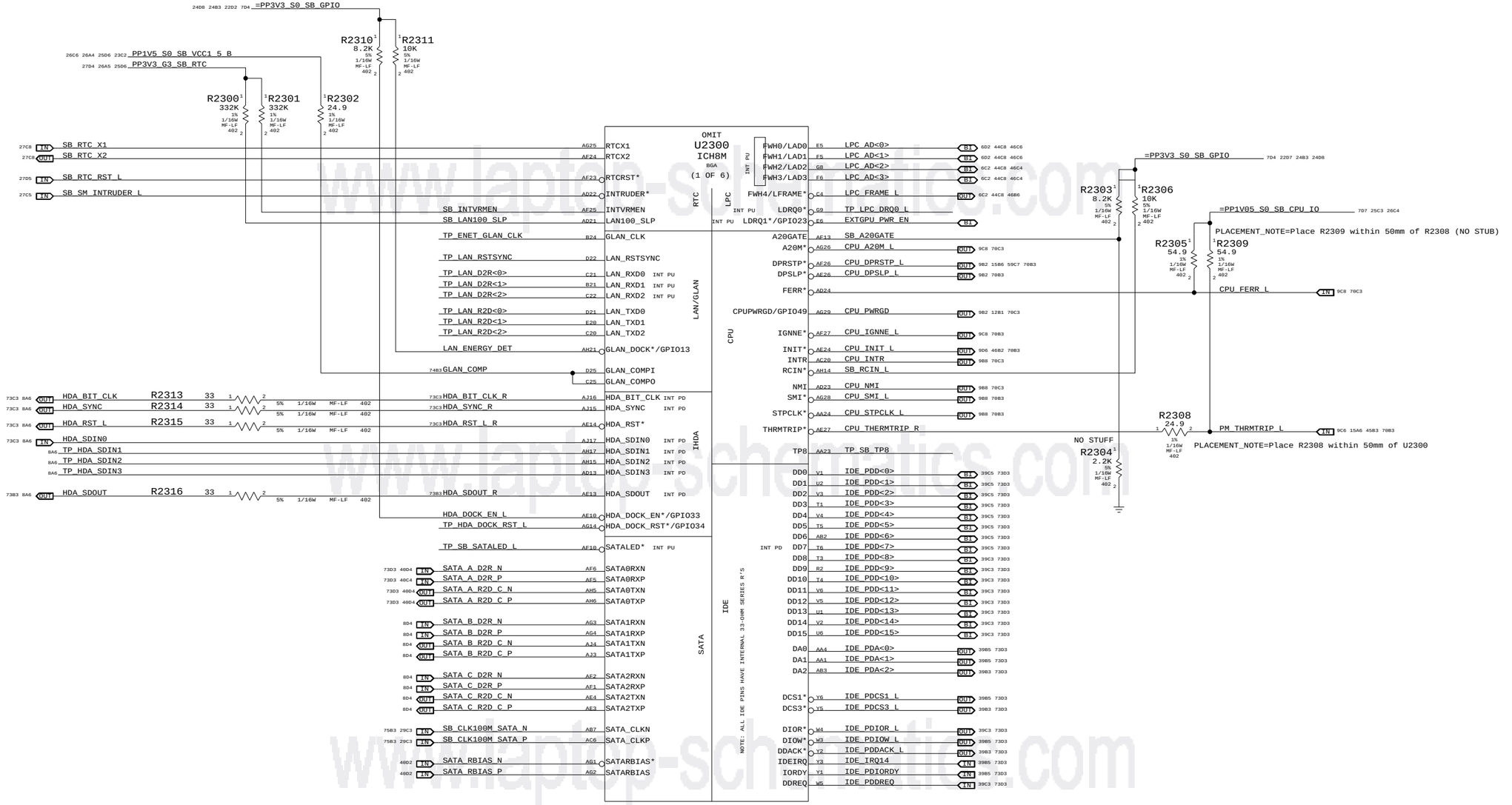
SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 21 OF 106





	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 23 OF 106	

OMIT

U2300
ICH8M
BGA
(2 OF 6)

PCI_EXPRESS

Spares

(x2-capable, pull HDA_SYNC high for x2)

8D4	TP_PCIE_A_D2R_N	P27	PERN1
8D4	TP_PCIE_A_D2R_P	P26	PERP1
8D4	TP_PCIE_A_R2D_C_N	N29	PETN1
8D4	TP_PCIE_A_R2D_C_P	N28	PETP1
8D4	TP_PCIE_B_D2R_N	M27	PERN2
8D4	TP_PCIE_B_D2R_P	M26	PERP2
8C4	TP_PCIE_B_R2D_C_N	L29	PETN2
8C4	TP_PCIE_B_R2D_C_P	L28	PETP2

ExpressCard

8C4	TP_PCIE_EXCARD_D2R_N	K27	PERN3
8C4	TP_PCIE_EXCARD_D2R_P	K26	PERP3
8C4	TP_PCIE_EXCARD_R2D_C_N	J29	PETN3
8C4	TP_PCIE_EXCARD_R2D_C_P	J28	PETP3

FireWire

8C4	TP_PCIE_FW_D2R_N	H27	PERN4
8C4	TP_PCIE_FW_D2R_P	H26	PERP4
8C4	TP_PCIE_FW_R2D_C_N	G29	PETN4
8C4	TP_PCIE_FW_R2D_C_P	G28	PETP4

PCIe Mini Card (AirPort)

33B6 IN	PCIE_MINI_D2R_N	F27	PERN5
33B6 IN	PCIE_MINI_D2R_P	F26	PERP5
33B6 OUT	PCIE_MINI_R2D_C_N	E29	PETN5
33B6 OUT	PCIE_MINI_R2D_C_P	E28	PETP5

Ethernet Yukon-PCIE Nineveh-GLCI

34C8 IN	PCIE_ENET_D2R_N	D27	PERN6/GLAN_RXN
34C8 IN	PCIE_ENET_D2R_P	D26	PERP6/GLAN_RXP
34C8 OUT	PCIE_ENET_R2D_C_N	C29	PETN6/GLAN_TXN
34C8 OUT	PCIE_ENET_R2D_C_P	C28	PETP6/GLAN_TXP

SPI

	SPI_CLK	C23	SPI_CLK INT PU
73A3 52C7 B1	SPI_CE_R_L<0>	B23	SPI_CS0*
	TP_SPI_CE_R_L<1>	E22	SPI_CS1* INT PU
73A3 52C3 B1	SPI_SI_R	D23	SPI_MOSI INT PU
73A3 52C3 B1	SPI_SO	F21	SPI_MISO INT PU

DIRECT MEDIA INTERFACE

DMI0RXN	V27	DMI_N2S_N<0>	IN 15B3 71D3
DMI0RXP	V26	DMI_N2S_P<0>	IN 15B3 71D3
DMI0TXN	U29	DMI_S2N_N<0>	OUT 15C3 71D3
DMI0TXP	U28	DMI_S2N_P<0>	OUT 15B3 71D3
DMI1RXN	Y27	DMI_N2S_N<1>	IN 15B3 71D3
DMI1RXP	Y26	DMI_N2S_P<1>	IN 15B3 71D3
DMI1TXN	W29	DMI_S2N_N<1>	OUT 15C3 71D3
DMI1TXP	W28	DMI_S2N_P<1>	OUT 15B3 71D3
DMI2RXN	AB26	DMI_N2S_N<2>	IN 15B3 71D3
DMI2RXP	AB25	DMI_N2S_P<2>	IN 15B3 71D3
DMI2TXN	AA29	DMI_S2N_N<2>	OUT 15B3 71D3
DMI2TXP	AA28	DMI_S2N_P<2>	OUT 15B3 71D3
DMI3RXN	AD27	DMI_N2S_N<3>	IN 15B3 71D3
DMI3RXP	AD26	DMI_N2S_P<3>	IN 15B3 71D3
DMI3TXN	AC29	DMI_S2N_N<3>	OUT 15B3 71D3
DMI3TXP	AC28	DMI_S2N_P<3>	OUT 15B3 71D3
DMI_CLKN	T26	SB_CLK100M_DMI_N	IN 29C3 75B3
DMI_CLKP	T25	SB_CLK100M_DMI_P	IN 29C3 75B3
DMI_ZCOMP	Y23		
DMI_IRCOMP	Y24	DMI_IRCOMP_R	

R2413 24.9 1% 1/10W MF-LF 402 — PP1V5_S0_SB_VCC1_5_B 22D7 25D6 26A4 26C6

USB

EHCI0

INT PD	USBP0N	G3	USB_EXTA_N
INT PD	USBP0P	G2	USB_EXTA_P
INT PD	USBP1N	H5	USB_MINI_N
INT PD	USBP1P	H4	USB_MINI_P
INT PD	USBP2N	H2	USB_EXTD_N
INT PD	USBP2P	H1	USB_EXTD_P
INT PD	USBP3N	J3	USB_CAMERA_N
INT PD	USBP3P	J2	USB_CAMERA_P
INT PD	USBP4N	K5	USB_IR_N
INT PD	USBP4P	K4	USB_IR_P
INT PD	USBP5N	K2	USB_TPAD_N
INT PD	USBP5P	K1	USB_TPAD_P

EHCI1

INT PD	USBP6N	L3	USB_BT_N
INT PD	USBP6P	L2	USB_BT_P
INT PD	USBP7N	M5	USB_EXTB_N
INT PD	USBP7P	M4	USB_EXTB_P
INT PD	USBP8N	M2	USB_EXCARD_N
INT PD	USBP8P	M1	USB_EXCARD_P
INT PD	USBP9N	N3	USB_EXTC_N
INT PD	USBP9P	N2	USB_EXTC_P

USBRBIAS*	F2		
USBRBIAS	F3	73B3 USB_RBIAS	

R2414 22.6 1% 1/10W MF-LF 402

USB_EXTA_N	External A
USB_EXTA_P	
USB_MINI_N	AirPort (PCIe Mini-Card)
USB_MINI_P	
USB_EXTD_N	External D / WWAN
USB_EXTD_P	
USB_CAMERA_N	Camera
USB_CAMERA_P	
USB_IR_N	IR
USB_IR_P	
USB_TPAD_N	Geyser Trackpad/Keyboard
USB_TPAD_P	
USB_BT_N	Bluetooth
USB_BT_P	
USB_EXTB_N	External B
USB_EXTB_P	
USB_EXCARD_N	ExpressCard
USB_EXCARD_P	
USB_EXTC_N	External C
USB_EXTC_P	

NOTE: USBP[0-9]P/N have internal 15K pull-downs.

7D1 =PP3V3_S5_SB_USB

R2400 10K 5% 1/16W MF-LF 402
R2402 10K 5% 1/16W MF-LF 402
R2404 10K 5% 1/16W MF-LF 402
R2408 10K 5% 1/16W MF-LF 402
R2401 10K 5% 1/16W MF-LF 402
R2403 10K 5% 1/16W MF-LF 402
R2405 10K 5% 1/16W MF-LF 402
R2407 10K 5% 1/16W MF-LF 402
R2409 10K 5% 1/16W MF-LF 402

8C1 IN	USB_EXTA_OC_L	AJ19 OC0*
39B8 OUT	SB_GPIO40	AG16 OC1*/GPIO40
IN	USB_EXTD_OC_L	AG15 OC2*/GPIO41
33B8 OUT	SB_GPIO42	AE15 OC3*/GPIO42
OUT	PM_LATRIGGER_L	AF15 OC4*/GPIO43
OUT	EXTGPU_LVDS_EN	AG17 OC5*/GPIO29
OUT	SB_GPIO30	AD17 OC6*/GPIO30
8B1 IN	USB_EXTB_OC_L	AJ18 OC7*/GPIO31
IN	EXCARD_OC_L	AD14 OC8*
IN	USB_EXTC_OC_L	AH18 OC9*

NOSTUFF R2406 100K 5% 1/16W MF-LF 402

NOTE: GNT[0-3]# have internal 20K pull-ups enabled only when PCIRST# = 0 and PWROK = 1

If used, ensure GNT2# is not low when PWROK rises, or PCIe ports 5 & 6 will be disabled.

OMIT

U2300
ICH8M
BGA
(3 OF 6)

PCI

74D3 37C5 B1	PCI_AD<0>	D20	AD0
74D3 37C5 B1	PCI_AD<1>	E19	AD1
74D3 37C5 B1	PCI_AD<2>	D19	AD2
74D3 37C5 B1	PCI_AD<3>	A20	AD3
74D3 37C5 B1	PCI_AD<4>	D17	AD4
74D3 37C5 B1	PCI_AD<5>	A21	AD5
74D3 37C5 B1	PCI_AD<6>	A19	AD6
74D3 37C5 B1	PCI_AD<7>	C19	AD7
74D3 37C5 B1	PCI_AD<8>	A18	AD8
74D3 37C5 B1	PCI_AD<9>	B16	AD9
74D3 37C5 B1	PCI_AD<10>	A12	AD10
74D3 37C5 B1	PCI_AD<11>	E16	AD11
74D3 37B5 B1	PCI_AD<12>	A14	AD12
74D3 37B5 B1	PCI_AD<13>	G16	AD13
74D3 37B5 B1	PCI_AD<14>	A15	AD14
74D3 37B5 B1	PCI_AD<15>	B6	AD15
74D3 37B5 B1	PCI_AD<16>	C11	AD16
74D3 37B5 B1	PCI_AD<17>	A9	AD17
74D3 37B5 B1	PCI_AD<18>	D11	AD18
74D3 37B6 B1	PCI_AD<19>	B12	AD19
74D3 37B5 B1	PCI_AD<20>	C12	AD20
74D3 37B5 B1	PCI_AD<21>	D10	AD21
74D3 37B5 B1	PCI_AD<22>	C7	AD22
74D3 37B5 B1	PCI_AD<23>	F13	AD23
74D3 37B5 B1	PCI_AD<24>	E11	AD24
74D3 37B5 B1	PCI_AD<25>	E13	AD25
74D3 37B5 B1	PCI_AD<26>	E12	AD26
74D3 37B5 B1	PCI_AD<27>	D8	AD27
74D3 37B5 B1	PCI_AD<28>	A6	AD28
74D3 37B5 B1	PCI_AD<29>	E8	AD29
74D3 37B5 B1	PCI_AD<30>	D6	AD30
74D3 37B5 B1	PCI_AD<31>	A3	AD31

	REQ0*	A4	PCI_FW_REQ_L IN 23A4 37A5 74D3
	GNT0*	D7	PCI_FW_GNT_L MAKE_BASE=TRUE OUT 37A5 74D3
	REQ1*/GPIO50	E18	PCI_REQ1_L IN 23A4 74D3
INT PU	GNT1*/GPIO51	C18	TP_SB_GPIO51 BOOT_LPC_SPI_L OUT 6C2 46B6
	REQ2*/GPIO52	B19	PCI_REQ2_L IN 23A4 74D3
INT PU	GNT2*/GPIO53	F18	TP_SB_GPIO53
	REQ3*/GPIO54	A11	ODD_RST_5VTOL_L OUT 39A8 73D3
INT PU	GNT3*/GPIO55	C10	TP_SB_GPIO55

R2415 1K 5% 1/16W MF-LF 402

R2415 pull-down on GNT0# selects SPI ROM by default.

	C/BE0*	C17	PCI_C_BE_L<0> B1 37B5 74D3
	C/BE1*	E15	PCI_C_BE_L<1> B1 37B5 74D3
	C/BE2*	F16	PCI_C_BE_L<2> B1 37B5 74D3
	C/BE3*	E17	PCI_C_BE_L<3> B1 37B5 74D3
	IRDY*	C8	PCI_IRDY_L B1 23A4 37A5 74D3
	PAR	D9	PCI_PAR B1 37B5 74D3
	PCIRST*	G6	PCI_RST_L OUT 37A6
	DEVSEL*	D16	PCI_DEVSEL_L B1 23A4 37A5 74D3
	PERR*	A7	PCI_PERR_L B1 23A4 37A5 74D3
	PLOCK*	B7	PCI_LOCK_L B1 23A4 74D3
	SERR*	F10	PCI_SERR_L B1 23A4 37A5 74D3
	STOP*	C16	PCI_STOP_L B1 23A4 37A5 74D3
	TRDY*	C9	PCI_TRDY_L B1 23A4 37A5 74D3
	FRAME*	A17	PCI_FRAME_L B1 23A4 37A5 74D3
	PLTRST*	AG24	PLT_RST_L OUT 27D4 67C6
	PCICLK	B10	PCI_CLK33M_SB IN 29A5 29B3 75B3
INT PU	PME*	G7	TP_PCI_PME_L

INTERRUPT I/F

74C3 23A4 B1	INT_PIRQA_L	F9	PIRQA*
74C3 23A4 B1	INT_PIRQB_L	B5	PIRQB*
74C3 23A4 B1	INT_PIRQC_L	C5	PIRQC*
74C3 37A5 23A4 B1	INT_PIRQD_L	A10	PIRQD*
	PIRQE*/GPIO2	E8	INT_PIRQE_L B1 23A4 74C3
	PIRQF*/GPIO3	G11	INT_PIRQF_L B1 23A4 74C3
	PIRQG*/GPIO4	E12	DVI_HOTPLUG_DET IN 68A4 68B8
	PIRQH*/GPIO5	B3	ODD_PWR_EN_L OUT 23A4 39C8

FireWire INT*

Provide a pull-down on this GPIO if not used.

SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

7C4 =PP3V3_S0_SB_PCI

74D3 37A5 23A6	PCI_FRAME_L	R2423	8.2K
74D3 37A5 23A6	PCI_IRDY_L	R2424	8.2K
74D3 37A5 23A6	PCI_TRDY_L	R2425	8.2K
74D3 37A5 23A6	PCI_STOP_L	R2426	8.2K
74D3 37A5 23A6	PCI_SERR_L	R2427	8.2K
74D3 37A5 23A6	PCI_DEVSEL_L	R2428	8.2K
74D3 37A5 23A6	PCI_PERR_L	R2430	8.2K
74D3 23A6	PCI_LOCK_L	R2429	8.2K
74D3 37A5 23B6	PCI_FW_REQ_L	R2432	8.2K
74D3 23B6	PCI_REQ1_L	R2431	8.2K
74D3 23B6	PCI_REQ2_L	R2433	8.2K
74C3 23A8	INT_PIRQA_L	R2437	8.2K
74C3 23A8	INT_PIRQB_L	R2436	8.2K
74C3 23A8	INT_PIRQC_L	R2438	8.2K
74C3 37A5 23A8	INT_PIRQD_L	R2439	8.2K
74C3 23A6	INT_PIRQE_L	R2440	8.2K
74C3 23A6	INT_PIRQF_L	R2441	8.2K
39C8 23A6	ODD_PWR_EN_L	R2442	8.2K

SB PCI, PCIe, DMI, USB

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE NONE SHT 24 OF 106

24B3 22D7 22D2 7D4 =PP3V3_S0_SB_GPIO
7D1 =PP3V3_S5_SB_GPIO

R2500 1K 5% 1/16W MF-LF 402
R2551 8.2K 5% 1/16W MF-LF 402
R2553 8.2K 5% 1/16W MF-LF 402
R2504 10K 5% 1/16W MF-LF 402
R2506 10K 5% 1/16W MF-LF 402
R2510 1K 5% 1/16W MF-LF 402
NO_REBOOT_MODE

R2502 10K 5% 1/16W MF-LF 402
R2550 10K 5% 1/16W MF-LF 402
R2552 10K 5% 1/16W MF-LF 402
R2547 10K 5% 1/16W MF-LF 402
R2505 8.2K 5% 1/16W MF-LF 402
R2507 8.2K 5% 1/16W MF-LF 402

OMIT

U2300 ICH8M BGA (4 OF 6)

73A3 47D8 BI	SMB_CLK	AJ26	SMBCLK	SMB	
73A3 47D8 BI	SMB_DATA	AD19	SMBDATA	SMB	
74A3 BI	CLINK_WLAN_RESET_L	AG21	CLINKALERT*	SMB	
73A3 47A8 BI	SMB_ME_CLK	AC17	SMLINK0	SMB	
73A3 47A8 BI	SMB_ME_DATA	AE19	SMLINK1	SMB	
24A5 IN	PM_RI_L	AF17	RI*	CLOCKS	
46B4 44C5 6C2 OUT	PM_SUS_STAT_L	F4	SUS_STAT*/LPCPD*	CLOCKS	
44B8 27C5 IN	PM_SYSRST_L	AD15	SYS_RESET*	CLOCKS	
15B6 IN	PM_BMBUSY_L	AG12	BMBUSY*/GPIO0	SYS GPIO	
46B4 24A7 6C2 IN	LINDACARD_GPIO	AG22	SMBALERT*/GPIO11	SYS GPIO	
29C2 28C4 OUT	PM_STPPCI_L	AE20	STP_PCI*/GPIO15	SYS GPIO	
29C2 28C4 OUT	PM_STPCPU_L	AG18	STP_CPU*/GPIO25	SYS GPIO	
46B6 44C5 37A5 6C2 BI	PM_CLKRUN_L	AH11	CLKRUN*/GPIO32	SYS GPIO	
34B8 33C5 IN	PCIE_WAKE_L	AE17	WAKE*	SYS GPIO	
46B4 44C8 6C2 BI	INT_SERIRQ	AF12	SERIRQ	SYS GPIO	
PM_THRM_L		AC13	THRM*	SYS GPIO	
8B4 IN	VR_PWRGD_CLKEN	AJ20	VRMPWRGD	SYS GPIO	
TP_SB_TP7		AJ22	TP7	SYS GPIO	
37A5 24A5 IN	PCI_PME_FW_L	AJ8	TACH1/GPIO1 INT PU	GPIO	
24B5 IN	TP_SB_GPIO6	AJ9	TACH2/GPIO6 INT PU	GPIO	
		AH9	TACH3/GPIO7 INT PU	GPIO	
		AE16	GPIO8	GPIO	
24A5 OUT	LAN_PHYPC	AC19	GPIO12	GPIO	
24B5 8B4 OUT	EXTGPU_RST_L	AG8	TACH0/GPIO17 INT PU	GPIO	
SB_GPIO18		AH12	GPIO18	GPIO	
TP_SB_GPIO20		AE11	GPIO20 INT PD	GPIO	
SB_SCLOCK		AG10	SCLOCK/GPIO22	GPIO	
24A5 SATA_B_PWR_EN_L		AH25	QRT_STATE0/GPIO27	GPIO	
24A7 FWH_MFG_MODE		AD16	QRT_STATE1/GPIO28	GPIO	
8B4 OUT SB_SATA_CLKREQ_L		AG13	SATACLKREQ*/GPIO35	GPIO	
SB_SLOAD		AF9	SLOAD/GPIO38	GPIO	
SB_SDATAOUT<0>		AJ11	SDATAOUT0/GPIO39	GPIO	
SB_SDATAOUT<1>		AD10	SDATAOUT1/GPIO48	GPIO	
SB_SPKR		AD9	SPKR INT PD	MISC	
15A3 IN NB_SB_SYNC_L		AJ13	MCH_SYNC*	MISC	
TP_SB_TP3		AJ21	TP3 INT PU	MISC	

Test access required for XOR chain testing.

		AJ12	SATA0GP/GPIO21	SATA GPIO	
		AJ10	SATA1GP/GPIO19	SATA GPIO	
		AF11	SATA2GP/GPIO36	SATA GPIO	
		AG11	SATA3GP/GPIO37	SATA GPIO	
	CLK14	AG9	SB_CLK14P3M_TIMER	IN 29A5 29D6 75B3	
	CLK48	G5	SB_CLK48M_USBCTLR	IN 29A5 29D6 75B3	
	SUSCLK	D3	SUS_CLK_SB	OUT 45A8	
	SLP_S3*	AG23	PM_SLP_S3_L	OUT 33C7 35C7 44C5 45A6 58B7 62B8	
	SLP_S4*	AF21	TP_PM_SLP_S4_L		
	SLP_S5*	AD18	PM_SLP_S5_L	OUT 44C5 45C3	
	S4_STATE*/GPIO26	AH27	PM_S4_STATE_L	OUT 33B7 44C5 65A6 65C4	
	PWROK	AE23	PM_SB_PWROK	IN 27A6	
	DPRSLPVR/GPIO16	AJ14	PM_DPRSLPVR	OUT 15A6 59D8 70B3	
	BATLOW*	AE21	PM_BATLOW_L	IN 24A5 44B8	
INT PU	PWRBTN*	C2	PM_PWRBTN_L	IN 44C8	
	LAN_RST*	AH20	PM_LAN_ENABLE	IN 44D8	
	RSMRST*	AG27	PM_RSMRST_L	IN 44C8	
	CK_PWRGD	E1	CLK_PWRGD	OUT 28A4	
	CLPWROK	E3	See note below =SB_CLINK_MPWROK	IN 8B4	
	SLP_M*	AJ25	TP_PM_SLP_M_L		
	CL_CLK0	F23	CLINK_NB_CLK	BI 15A3 74A3	
	CL_CLK1	AE18	CLINK_WLAN_CLK	BI 74A3	
	CL_DATA0	F22	CLINK_NB_DATA	BI 15A3 74A3	
	CL_DATA1	AF19	CLINK_WLAN_DATA	BI 74A3	
	CL_VREF0	D24 74A3	SB_CLINK_VREF0		
	CL_VREF1	AH23 74A3	SB_CLINK_VREF1		
INT PU	CL_RST*	AJ23	CLINK_NB_RESET_L	OUT 15A3 74A3	
	MEM_LED/GPIO24	AJ27	ARB_DETECT_L	BI 24A7	
	ME_EC_ALERT/GPIO10	AJ24	SB_GPIO10_CL1	24A5	
	EC_ME_ALERT/GPIO14	AF22	SB_GPIO14_CL2	24A5	
	WOL_EN/GPIO9	AG19 35B7	WOL_EN		

NOTE: ICH CLPWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M. If ME/AMT is not used, short CLPWROK to PWROK.

R2532 10K 5% 1/16W MF-LF 402
R2535 10K 5% 1/16W MF-LF 402
R2533 10K 5% 1/16W MF-LF 402
R2534 10K 5% 1/16W MF-LF 402
RSVD_EXTGPU_LVDS_EN OUT
SATA_B_DET_L
SB_GPIO36
SB_CRT_TVOUT_MUX_L OUT 69A6

NOTE: DPRSLPVR HAS INT 20K PD ENABLED AT BOOT/RESET FOR STRAPPING FUNCTION

PM_LAN_ENABLE must remain deasseted until VccCL3_3, VccLAN3_3 and VccLAN1_05 have been up for at least 1ms.

R2524 100K 5% 1/16W MF-LF 402
R2525 10K 5% 1/16W MF-LF 402

=PP3V3_S0MWOL_SB_CLINK0 7C4
R2526 3.24K 1% 1/16W MF-LF 402
R2527 453 1% 1/16W MF-LF 402
C2500 0.1uF 10% 16V X5R 402

=PP3V3_S5_SB_CLINK1 7C1
R2528 3.24K 1% 1/16W MF-LF 402
C2501 0.1uF 10% 16V X5R 402
R2529 453 1% 1/16W MF-LF 402

NOSTUFF
R2523 100K 5% 1/16W MF-LF 402

44B8 IN SMC_RUNTIME_SCI_L
44C5 IN SMC_WAKE_SCI_L

LAYOUT NOTE:
PLACE R2511-16 WHERE PHYSICALLY ACCESSIBLE

35C7 26D8 24A3 7D1 =PP3V3_S5_SB
R2511 10K 5% 1/16W MF-LF 402
R2514 100K 5% 1/16W MF-LF 402
R2515 10K 5% 1/16W MF-LF 402
FWH_MFG_MODE 24C5
LINDACARD_GPIO 6C2 24D5 46B4
ARB_DETECT_L 24B3
NOSTUFF
R2512 0 5% 1/16W MF-LF 402
ARB_ONLY
R2516 0 5% 1/16W MF-LF 402

=PP3V3_S0_SB_GPIO 7D4 22D2 22D7 24D8
24C5 TP_SB_GPIO6 — R2597 10K 1% 1/16W MF-LF 402
24C5 8B4 EXTGPU_RST_L — R2596 10K 1% 1/16W MF-LF 402
24C5 SATA_B_PWR_EN_L — R2530 10K 1% 1/16W MF-LF 402
37A5 24C5 PCI_PME_FW_L — R2531 10K 1% 1/16W MF-LF 402

=PP3V3_S5_SB 7D1 24A8 26D8 35C7
24D5 PM_RI_L — R2536 10K 1% 1/16W MF-LF 402
44B8 24C3 PM_BATLOW_L — R2544 8.2K 5% 1/16W MF-LF 402
24C5 LAN_PHYPC — R2545 10K 1% 1/16W MF-LF 402
24B3 SB_GPIO10_CL1 — R2598 10K 1% 1/16W MF-LF 402
24B3 SB_GPIO14_CL2 — R2546 10K 1% 1/16W MF-LF 402

SB Pwr Mgt, GPIO, Clink

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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SIZE	DRAWING NUMBER	REV.
D	051-7559	S

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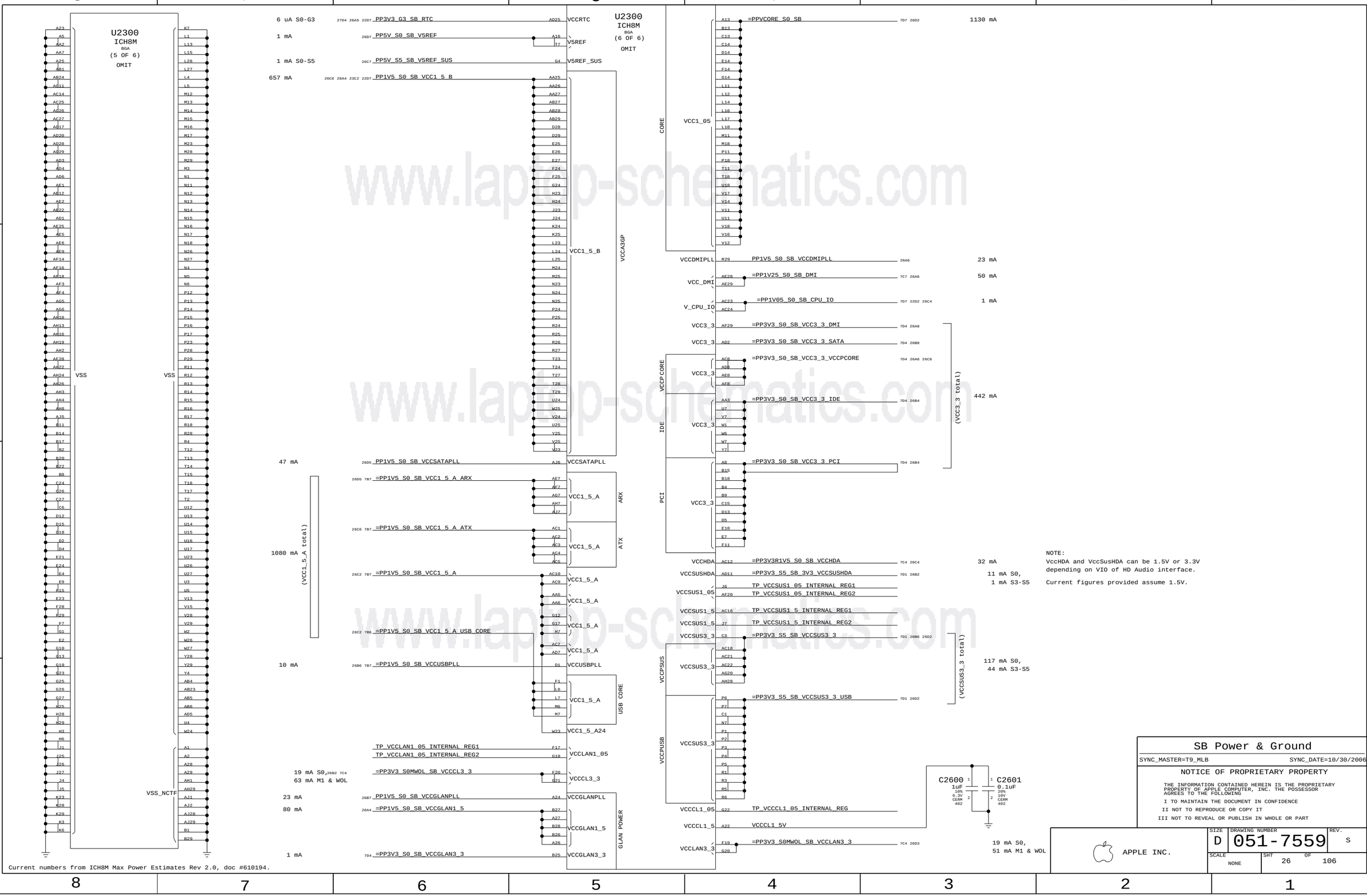


ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)

=PP3V3_S0_SB
=PP5V_S0_SB
R2702 100 1/16W MF-LF 402 5%
D2702 HN2S02JE SOT-665
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2703 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)

=PP3V3_S5_SB
=PP5V_S5_SB
R2701 10 1/16W MF-LF 402 5%
D2702 HN2S02JE SOT-665
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2704 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

=PP1V5_S0_SB
L2700 MAY HAVE CHANGE TO 0.5UH PART
ICH VCCA3GP(VCC1_5_B BYPASS
FERR-330-OHM-1.5A (ICH IO,LOGIC 1.5V PWR)
0805-1
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
OMIT
CRITICAL
NOSTUFF
C2700 220UF 20% 2.5V POLY CASE-B2
C2705 22UF 20% 6.3V CERM 805
C2706 22UF 20% 6.3V CERM 805
C2707 2.2UF 20% 6.3V CERM1 603

PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23

M70 DOES NOT USE GIGABIT IN SB, SO NO NEED FOR PLL FILTERING

VOLTAGE=1.5V
MIN_LINE_WIDTH=1.5 mm
MIN_NECK_WIDTH=0.25 mm
PP1V5_S0_SB_VCCGLANPLL
NOSTUFF
C2742 10UF 20% 6.3V X5R 603
C2732 2.2UF 20% 6.3V CERM1 603

PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24

=PP3V3_S0_SB_VCC3_3_SATA

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2

C2738 0.1UF 10% 16V X5R 402

=PP1V5_S0_SB
L2703 NEED CHANGE TO 1UH PART
L2703 1.0UH-0.5A-0.675A 1007
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
R2700 1 1/10W 5% MF-LF 402
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2701 0.01UF 10% 16V CERM 402
C2708 10UF 20% 6.3V X5R 603

PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

=PP3V3_S0_SB_VCC3_3_DMI

PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29

C2737 0.1UF 10% 16V X5R 402

=PP1V25_S0_SB_DMI

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29

C2739 22UF 20% 6.3V CERM 805

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7

C2711 1UF 10% 6.3V CERM 402

L2702 MAY HAVE CHANGE TO 1.0UH PART
L2702 10UH-100MA 0805
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
=PP1V5_S0_SB
PP1V5_S0_SB_VCCSATAPLL
C2735 10UF 20% 6.3V X5R 603
C2717 1UF 10% 6.3V CERM 402

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AJ6

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_VCCPCORE

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11

C2713 0.1UF 10% 16V X5R 402

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5

C2714 1UF 10% 6.3V CERM 402

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3

PLACEMENT NOTE:
PLACE CAPS NEAR PIN C2..AH28

C2720 0.1UF 10% 16V X5R 402
C2743 0.1UF 10% 16V X5R 402

ICH VCCSUSPLL BYPASS
(ICH USB PLL 1.5V PWR)
=PP1V5_S0_SB_VCCUSBPLL

PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB

C2715 0.1UF 10% 16V X5R 402

ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_VCCPCORE

PLACEMENT NOTE:
PLACE C2709 NEAR PIN B27 OF SB

C2709 0.1UF 10% 16V X5R 402

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
=PP3V3_G3_SB_RTC
C2730 0.1UF 10% 16V X5R 402
C2729 0.1UF 10% 16V X5R 402

PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB

PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
=PPVCORE_S0_SB
C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402
OMIT
CRITICAL
C2716 330UF 20% 2.5V POLY CASE-C2

PLACEHOLDER
FOR 270UF

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
=PP3V3_S0MWOL_SB_VCCLAN3_3

PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20

C2719 0.1UF 10% 16V X5R 402

ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
=PP3V3R1V5_S0_SB_VCCHDA

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12

C2721 0.1UF 10% 16V X5R 402

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
=PP1V05_S0_SB_CPU_IO

PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB

C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402
C2724 4.7UF 20% 6.3V CERM 603

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7

C2725 0.1UF 10% 16V X5R 402

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI

PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11

NOSTUFF
C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402

PP1V5_S0_SB_VCC1_5_B
MAKE_BASE=TRUE
=PP1V5_S0_SB_VCCGLAN1_5

PLACEMENT NOTE:
PLACE CAP NEAR PIN B27..A26

C2736 4.7UF 20% 6.3V CERM 603

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3

PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AC18..AH28

C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB

PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6

C2733 4.7UF 20% 6.3V CERM 603

ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A

PLACEMENT NOTE:
PLACE CAP NEAR PINS
AC10..AD7 OF SB

C2710 0.1UF 10% 16V X5R 402

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7

C2712 0.1UF 10% 16V X5R 402

ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
=PP3V3_S5_SB_3V3_VCCSUSHDA

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11

C2741 0.1UF 10% 16V X5R 402

=PP3V3_S0MWOL_SB_VCCCL3_3

PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F20,G21

C2740 0.1UF 10% 16V X5R 402

SB Decoupling

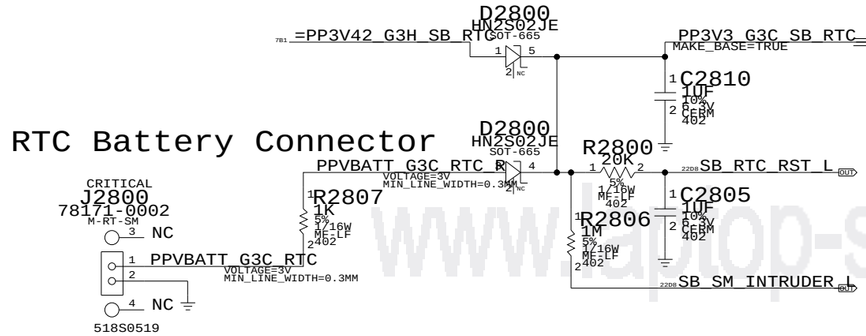
SYNC_MASTER=WFERRY SYNC_DATE=06/01/2006

APPLE INC.

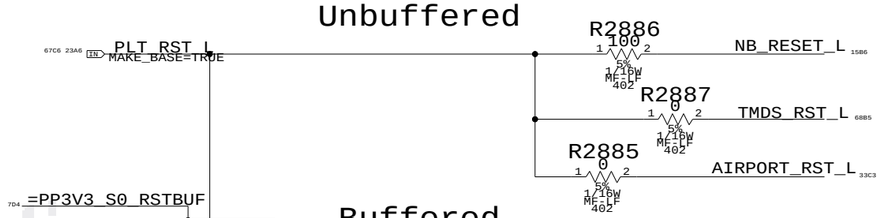
SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 27 OF 106	

Platform Reset Connections

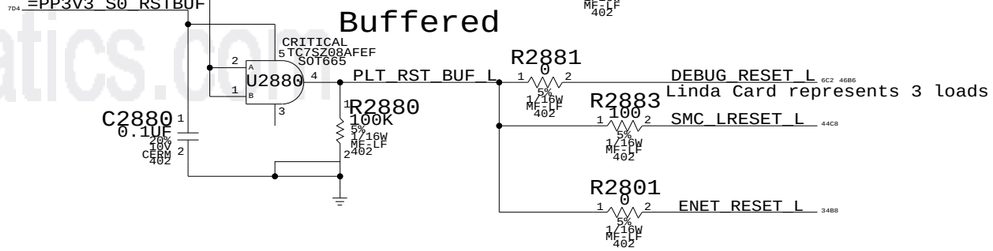
RTC Battery Connector



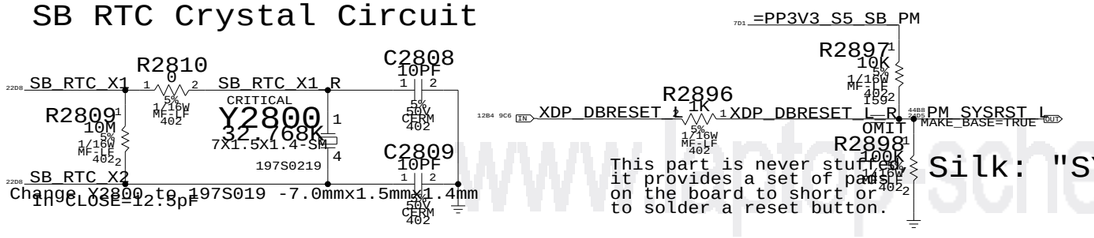
Unbuffered



Buffered



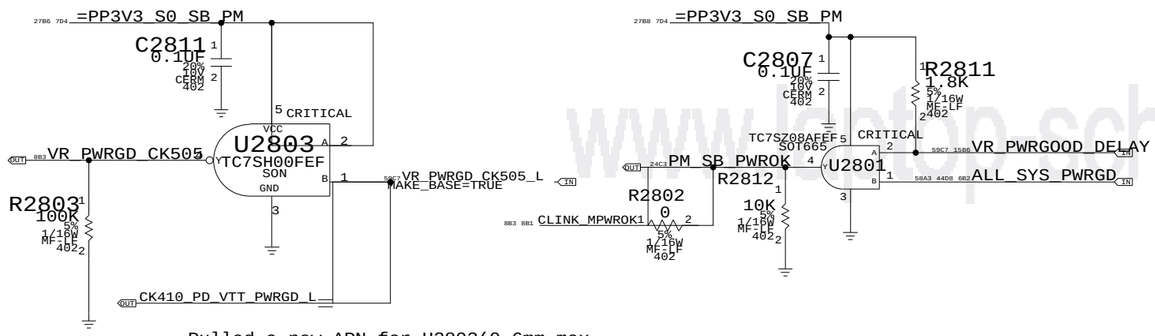
SB RTC Crystal Circuit



This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Silk: "SYS RST"

CPU VCORE PSI



Pulled a new APN for U2803(0.6mm max
2-input NAND gate-APN:311S0304
It may take a few days before this is done through
This will allow us to sequence this part under wireless card

Initial resistor values are based on CRB, but may change after characterization.

SB Misc

SYNC_MASTER=NB SYNC_DATE=07/26/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	28	106

SELIGO RECOMMEND TO REMOVE L2903,R2900,C2907,C2910
R2901,L2902,C2916,C2911,C2914 and R2902

ORIGINAL DESIGN:
USE 155S0302 FOR L2902(R2906) AND L2903(R2907)
STUFF C2907,C2910,C2916,C2911,C2914
USE 2.2OHM FOR R2900,R2901 AND 1OHM FOR R2902

=PP3V3_S0_CK505

L2901
FERR-120-OHM-1.5A
0402-LF

PP3V3_S0_CK505_VDD_CPU_SRC
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

C2900 1UF 10% 6.3V CERM 402
C2901 10UF 20% 6.3V X5R 603
C2902 0.1UF 10% 16V X5R 402
C2903 0.1UF 10% 16V X5R 402
C2904 0.1UF 10% 16V X5R 402
C2905 0.1UF 10% 16V X5R 402
C2906 0.1UF 10% 16V X5R 402

R2907 0 5% 1/16W MF-LF 402
PP3V3_S0_CK505_VDDA_R
MIN_LINE_WIDTH=0.5mm
VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2mm

R2900 0 5% 1/16W MF-LF 402
PP3V3_S0_CK505_VDDA
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm

NOSTUFF C2907 10UF 20% 6.3V X5R 603
C2908 0.1UF 10% 16V X5R 402

NEED TO CHECK CAP VALUE

CRITICAL
Y2901
14.31818
5X3.2-SM
C2989 18PF 5% 50V CERM 402
C2990 18PF 5% 50V CERM 402

PP3V3_S0_CK505_VDD48
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

C2909 0.1UF 10% 16V X5R 402
NOSTUFF C2910 10UF 20% 6.3V X5R 603

R2901 0 5% 1/16W MF-LF 402

R2906 0 5% 1/16W MF-LF 402

=PP3V3_S0_CK505
NOSTUFF C2911 1UF 10% 6.3V CERM 402

PP3V3_S0_CK505_VDD_PCI
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

C2912 0.1UF 10% 16V X5R 402
C2913 0.1UF 10% 16V X5R 402
NOSTUFF C2914 10UF 20% 6.3V X5R 603

PP3V3_S0_CK505_VDD_REF
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

C2915 0.1UF 10% 16V X5R 402
NOSTUFF C2916 10UF 20% 6.3V X5R 603

R2902 0 5% 1/16W MF-LF 402

VDD_48 3
VDD_CPU 43
VDD_PCI 61 67
VDD_REF 49
VDD_SRC 12 17 28 35

(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

CRITICAL
U2900
SLG2AP101
QFN

38	VDD_A			
39	VSS_A			
51	XTAL_IN	CK505_XTAL_IN		
50	XTAL_OUT	CK505_XTAL_OUT		
8	FS_B/TEST_MODE	CK505_FSB_TEST_MODE	IN	29B8
57	PCI_1	CK505_PCI1_CLK	OUT	75D3 29B6
58	PCI_2	CK505_PCI2_CLK	OUT	75D3 8C4
63	PCI_3	CK505_PCI3_CLK	OUT	75D3 29A6
64	PCI_4	CK505_PCI4_CLK	OUT	75D3 8C4
65	PCI_5/FCT_SEL	CK505_PCI5_FCTSEL1	BI	75D3 29B2
68	PCIF_0/ITP_EN	(NO INT PD) (NO INT PU)		
1	PCIF_1	CK505_PCIF1_CLK	OUT	75D3 29B6 6C7
47	SCL	=SMBUS_CK505_SCL	IN	47D6
48	SDA	=SMBUS_CK505_SDA	BI	47D6
		CK505_PGMODE		28A4
5	VSS_48			
46	VSS_CPU			
62				
66	VSS_PCI			
52	VSS_REF			
31	VSS_SRC			
69	THRM_PAD			

PCI_STOP*	56	PM_STPPCI_L	IN	24C8 29C2
CPU_STOP*	55	PM_STPCPU_L	IN	24C8 29C2
CPU_0*	44	CK505_CPU0_N	OUT	6C7 29D6 75D3
CPU_0	45	CK505_CPU0_P	OUT	6C7 29D6 75D3
CPU_1_MCH*	41	CK505_CPU1_N	OUT	6C7 29D6 75D3
CPU_1_MCH	42	CK505_CPU1_P	OUT	6C7 29D6 75D3
CPU_ITP*/SRC_10*	36	CK505_CPU2_ITP_SRC10_N	OUT	6C7 29D6 75D3
CPU_ITP/SRC_10	37	CK505_CPU2_ITP_SRC10_P	OUT	6C7 29D6 75D3
SRC_0*/LCD_CLK*	11	CK505_LVDS_N	OUT	6C7 29C6 75C3
SRC_0/LCD_CLK	10	CK505_LVDS_P	OUT	6C7 29C6 75D3
SRC_1*	14	TP_CK505_SRC1_N	OUT	8C4
SRC_1	13	TP_CK505_SRC1_P	OUT	8C4
CLKREQ_1*	9	CK505_SRC_CLKREQ1_L	IN	29C2
SRC_2*	16	CK505_SRC2_N	OUT	6C7 29C6 75C3
SRC_2	15	CK505_SRC2_P	OUT	6C7 29C6 75C3
SRC_3*	19	TP_CK505_SRC3_N	OUT	8C4
SRC_3	18	TP_CK505_SRC3_P	OUT	8C4
CLKREQ_3*	59	CK505_SRC_CLKREQ3_L	IN	29C2
SRC_4*	22	CK505_SRC4_N	OUT	6C7 29C6 75C3
SRC_4	21	CK505_SRC4_P	OUT	6C7 29C6 75C3
CLKREQ_4*	20	SB_CLK100M_SATA_OE_L	IN	8B3
SRC_5*	24	CK505_SRC5_N	OUT	6C7 29C6 75C3
SRC_5	23	CK505_SRC5_P	OUT	6C7 29C6 75C3
CLKREQ_5*	60	NB_CLKREQ_L	IN	15A3
SRC_6*	27	CK505_SRC6_N	OUT	6C7 29B6 75C3
SRC_6	26	CK505_SRC6_P	OUT	6C7 29C6 75C3
CLKREQ_6*	25	CK505_SRC_CLKREQ6_L	IN	33C5
SRC_7*	30	TP_CK505_SRC7_N	OUT	8C4
SRC_7	29	TP_CK505_SRC7_P	OUT	8C4
CLKREQ_7*	40	CK505_PGMODE		28B5
SRC_8*	32	CK505_SRC8_N	OUT	6B7 29B6 75C3
SRC_8	33	CK505_SRC8_P	OUT	6B7 29B6 75C3
CLKREQ_8*	34	=ENET_CLKREQ_L	IN	8C4 34B8
DOT_96*/27M_SS	7	CK505_DOT96_27M_N	OUT	6C7 29B6 75D3
DOT_96/27M	6	CK505_DOT96_27M_P	OUT	6C7 29B6 75D3
CKPWRGD/PD*	2	CLK_PWRGD	IN	24C3
48M/FS_A	4	CK505_USB48_FSA	OUT	29D8 75D3
REF_0/FS_C/TEST_SEL	54	CK505_CLK14P3M_TIMER	OUT	29D8 75D3
GPU_STOP*	53	CK505_REF1	BI	

(FROM ICH8M GPIO15 STPPCI*)
(FROM ICH8M GPIO25 STPCPU*)
(CPU HOST 133/167MHZ)
(GMCH HOST 133/167MHZ)
(ITP HOST 133/167MHZ)
(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
(SLOT F - GPU PCI-E 100 MHZ)
(ICH8M DMI 100 MHZ)
(SLOT D - 4 LANE PCI-E FOR EXPRESSCARD)
(ICH SATA 100 MHZ)
(FROM ICH8M GPIO35)
(GMCH G_CLKIN 100 MHZ)
(FROM GMCH CLK_REQ*)
(WIRELESS PCI-E 100 MHZ)
(DB400 SRC)
(SLOT E)
(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
(FROM ICH8M)
(ICH8M USB 48MHZ)
(ICH8M,SIO,LPC REF. 14.318MHZ)

=PP3V3_S0_CK505
R2903 10K 5% 1/16W MF-LF 402
(FW PCI 33MHZ)
(TPM LPC 33MHZ)
(SMC LPC 33MHZ)
(PCI SLOT)
(PORT80 LPC 33MHZ)

CK505_PCIF0_CLK
(ICH8M PCI 33MHZ)

(PULL UP PIN 68 TO ENABLE ITP HOST CLK)

(ICH SM BUS)

0 = VTT_PWRGD#/PD
1 = CKPWRGD/PD#

U2900 HAS INTERNAL PU ON PGMODE

475 OHM FOR CK410M
COMPATIBILITY
STUFF R2905 FOR CK410M MODE

NOSTUFF R2905 475 1% 1/16W MF-LF 402

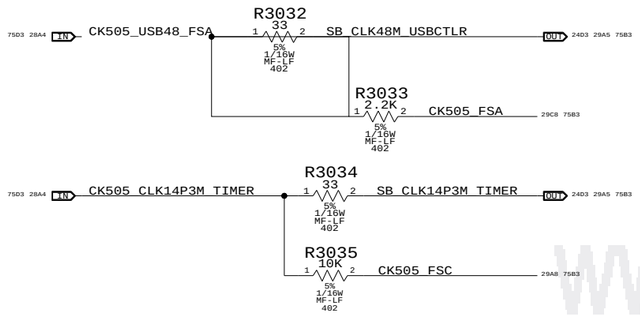
FCTSEL1	PIN 6	PIN 7	PIN 10	PIN 11
0	DOT96T	DOT96C	100MT_SST	100MC_SST
1	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0

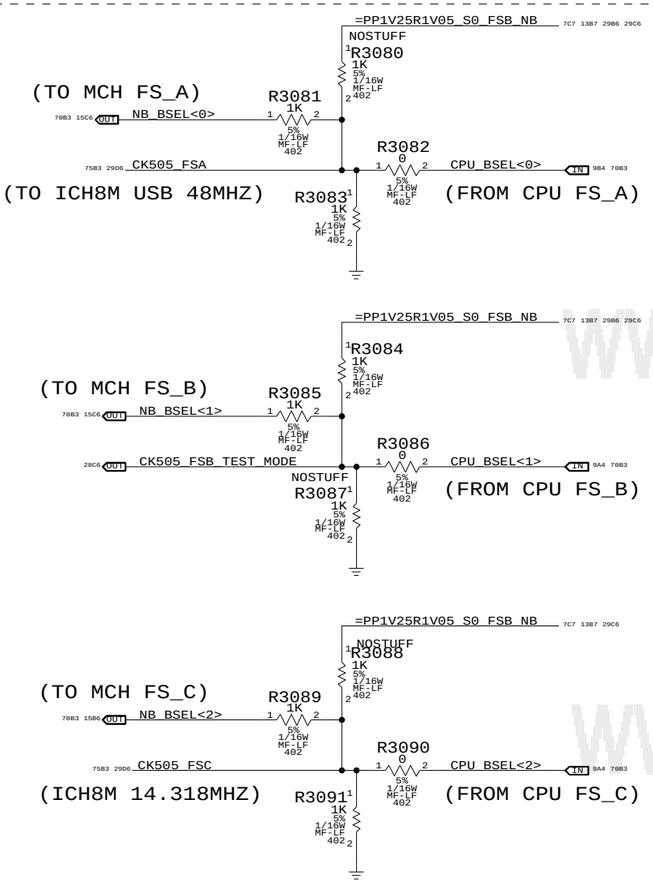
* FOR INT. GRAPHIC SYSTEM
* FOR EXT. GRAPHIC SYSTEM

Clock (CK505)
SYNC_MASTER=DSIMON SYNC_DATE=06/06/2006

APPLE INC.
SIZE D | DRAWING NUMBER 051-7559 | REV. S
SCALE NONE | SHT 29 OF 106

CLK Termination

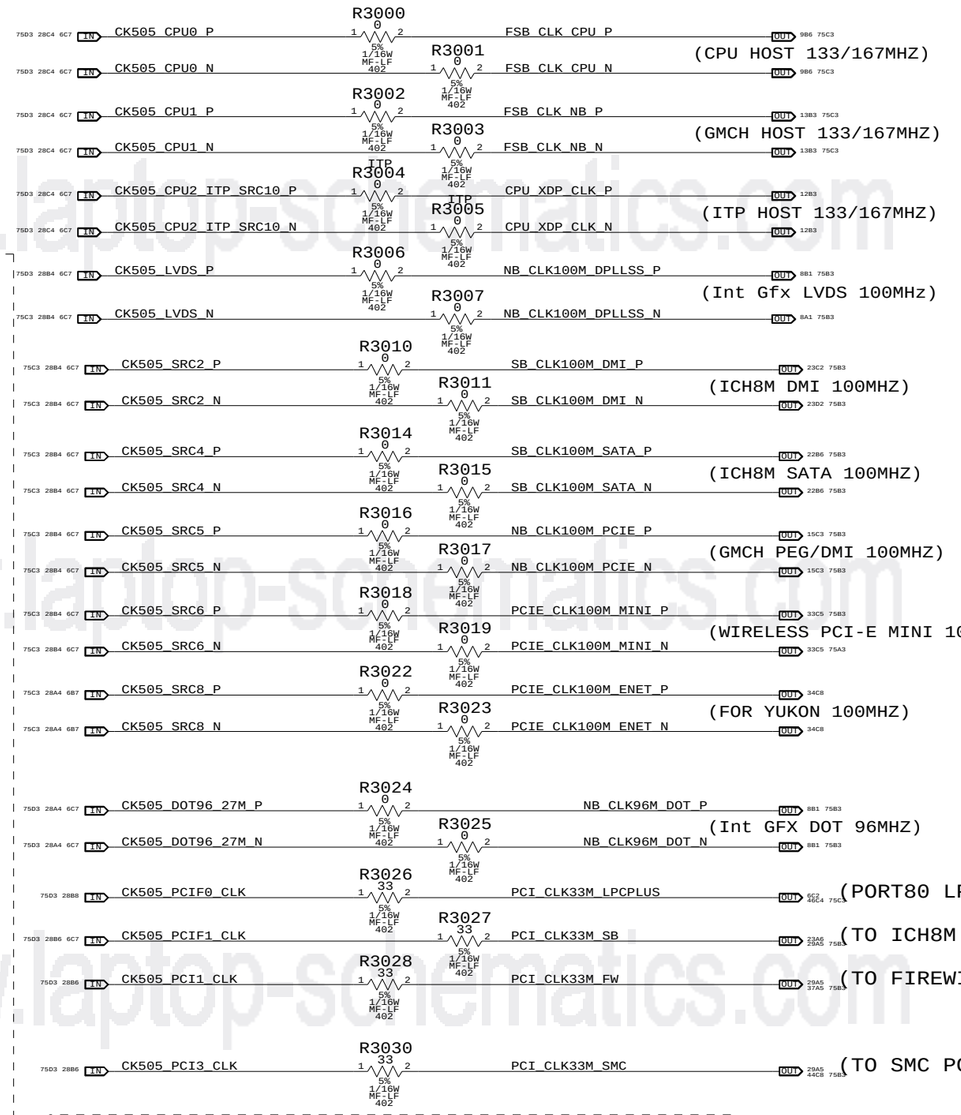




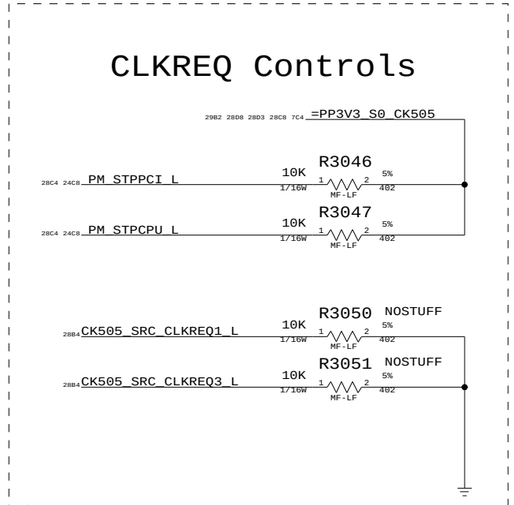
FS_C	FS_B	FS_A	CPU
0	0	0	266M
0	0	1	133M
0	1	1	166M
* 0	1	0	200M
1	1	0	400M
1	1	1	Resrvd
1	0	1	100M
1	0	0	333M

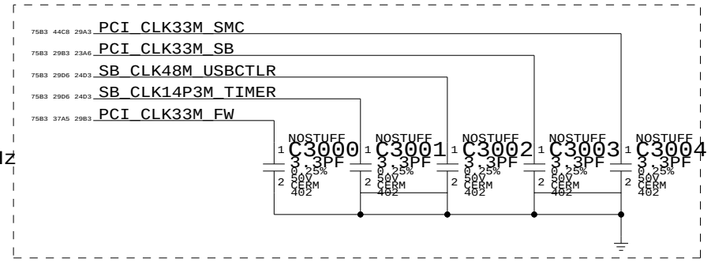
NOSTUFF R3082, R3086, R3090
FOR MANUAL CPU FREQUENCY

CPU speed is currently set to 200MHz



CLKREQ Controls





Place close to CLK Gen
For reducing noise coupling to wireless frequencies

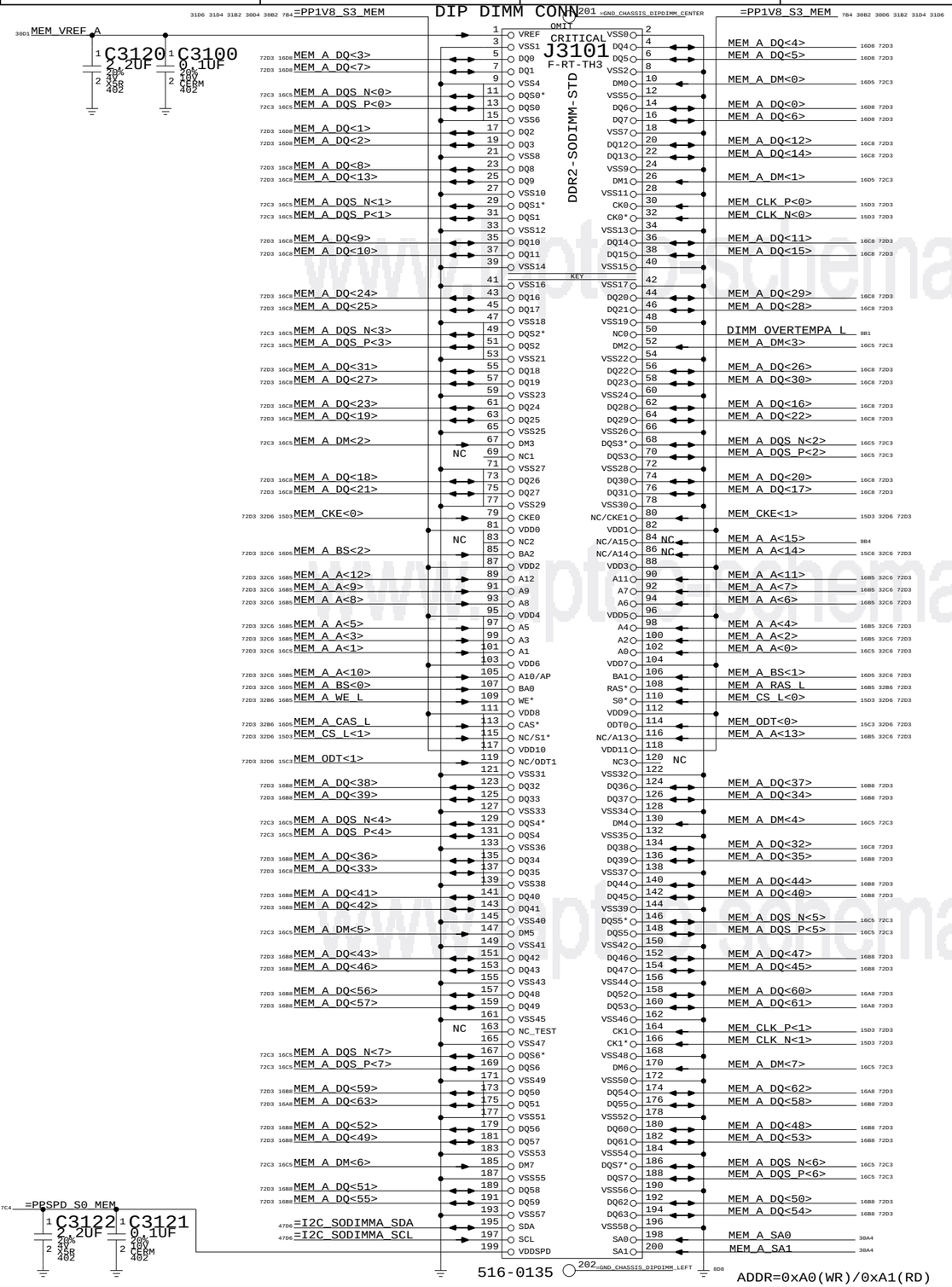
Clock Termination

SYNC_MASTER=DSIMON-WF SYNC_DATE=06/06/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 30 OF 106



DDR2 VREF (FOR CONNECTOR B)

One 0.1uF per connector

30D2 20C8 17D7 15D2 7A4 =PP1V8_S3M_MEM_NB

R3201 1K 1% 1/16W MF-LF 402

MEM_VREF_B 31D7
VOLTAGE=0.9V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

R3202 1K 1% 1/16W MF-LF 402

Yellow uses 10K divider and TLV2463 to drive MCH and DIMM connectors. (See Capell Valley pg 47)

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

DDR2 Bypass Caps

(For return current)

31D6 31D4 30D6 30D4 30B2 7B4 =PP1V8_S3_MEM

C3209 4.7uF 20% 6.3V CERM 603

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402

C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 2.2UF 20% 6.3V CERM 402-LF
C3217 2.2UF 20% 6.3V CERM 402-LF

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 2.2UF 20% 6.3V CERM 402-LF
C3232 2.2UF 20% 6.3V CERM 402-LF

The 4.7uF and 1.0uF caps can be changed to 5x 2.2uF caps, when they get cheaper.

31D1 MEM_VREF_B

C3220 2.2UF 20% 4V X5R 402
C3200 0.1UF 20% 10V CERM 402

31D4 31B2 30D6 30D4 30B2 7B4 =PP1V8_S3_MEM

DIP DIMM CONN

J3201 CRITICAL F-RT-TH3 (OMIT) — DDR2-SODIMM-STD

1	VREF		2	VSS0	
3	VSS1		4	DQ4	MEM_B_DQ<5>
5	DQ0		6	DQ5	MEM_B_DQ<0>
7	DQ1		8	VSS2	
9	VSS4		10	DM0	MEM_B_DM<0>
11	DQS0*		12	VSS5	
13	DQS0		14	DQ6	MEM_B_DQ<6>
15	VSS6		16	DQ7	MEM_B_DQ<2>
17	DQ2		18	VSS7	
19	DQ3		20	DQ12	MEM_B_DQ<15>
21	VSS8		22	DQ13	MEM_B_DQ<11>
23	DQ8		24	VSS9	
25	DQ9		26	DM1	MEM_B_DM<1>
27	VSS10		28	VSS11	
29	DQS1*		30	CK0	MEM_CLK_P<3>
31	DQS1		32	CK0*	MEM_CLK_N<3>
33	VSS12		34	VSS13	
35	DQ10		36	DQ14	MEM_B_DQ<9>
37	DQ11		38	DQ15	MEM_B_DQ<14>
39	VSS14		40	VSS15	
	KEY				
41	VSS16		42	VSS17	
43	DQ16		44	DQ20	MEM_B_DQ<21>
45	DQ17		46	DQ21	MEM_B_DQ<16>
47	VSS18		48	VSS19	
49	DQS2*		50	NC0	DIMM_OVERTEMPB_L (BB1)
51	DQS2		52	DM2	MEM_B_DM<2>
53	VSS21		54	VSS22	
55	DQ18		56	DQ22	MEM_B_DQ<23>
57	DQ19		58	DQ23	MEM_B_DQ<19>
59	VSS23		60	VSS24	
61	DQ24		62	DQ28	MEM_B_DQ<25>
63	DQ25		64	DQ29	MEM_B_DQ<28>
65	VSS25		66	VSS26	
67	DM3		68	DQS3*	MEM_B_DQS_N<3>
NC	NC1		70	DQS3	MEM_B_DQS_P<3>
71	VSS27		72	VSS28	
73	DQ26		74	DQ30	MEM_B_DQ<24>
75	DQ27		76	DQ31	MEM_B_DQ<26>
77	VSS29		78	VSS30	
79	CKE0		80	NC/CKE1	MEM_CKE<4>
81	VDD0		82	VDD1	
NC	NC2		84	NC/A15	NC — MEM_B_A<15> (8B4)
85	BA2		86	NC/A14	NC — MEM_B_A<14> (15C6 32A5 72B3)
87	VDD2		88	VDD3	
89	A12		90	A11	MEM_B_A<11>
91	A9		92	A7	MEM_B_A<7>
93	A8		94	A6	MEM_B_A<6>
95	VDD4		96	VDD5	
97	A5		98	A4	MEM_B_A<4>
99	A3		100	A2	MEM_B_A<2>
101	A1		102	A0	MEM_B_A<0>
103	VDD6		104	VDD7	
105	A10/AP		106	BA1	MEM_B_BS<1>
107	BA0		108	RAS*	MEM_B_RAS_L
109	WE*		110	S0*	MEM_CS_L<2>
111	VDD8		112	VDD9	
113	CAS*		114	ODT0	MEM_ODT<2>
115	NC/S1*		116	NC/A13	MEM_B_A<13>
117	VDD10		118	VDD11	
119	NC/ODT1		120	NC3	NC
121	VSS31		122	VSS32	
123	DQ32		124	DQ36	MEM_B_DQ<36>
125	DQ33		126	DQ37	MEM_B_DQ<37>
127	VSS33		128	VSS34	
129	DQS4*		130	DM4	MEM_B_DM<4>
131	DQS4		132	VSS35	
133	VSS36		134	DQ38	MEM_B_DQ<34>
135	DQ34		136	DQ39	MEM_B_DQ<33>
137	DQ35		138	VSS37	
139	VSS38		140	DQ44	MEM_B_DQ<43>
141	DQ40		142	DQ45	MEM_B_DQ<42>
143	DQ41		144	VSS39	
145	VSS40		146	DQS5*	MEM_B_DQS_N<5>
147	DM5		148	DQS5	MEM_B_DQS_P<5>
149	VSS41		150	VSS42	
151	DQ42		152	DQ46	MEM_B_DQ<41>
153	DQ43		154	DQ47	MEM_B_DQ<46>
155	VSS43		156	VSS44	
157	DQ48		158	DQ52	MEM_B_DQ<53>
159	DQ49		160	DQ53	MEM_B_DQ<49>
161	VSS45		162	VSS46	
NC	NC_TEST		164	CK1	MEM_CLK_P<4>
165	VSS47		166	CK1*	MEM_CLK_N<4>
167	DQS6*		168	VSS48	
169	DQS6		170	DM6	MEM_B_DM<6>
171	VSS49		172	VSS50	
173	DQ50		174	DQ54	MEM_B_DQ<51>
175	DQ51		176	DQ55	MEM_B_DQ<54>
177	VSS51		178	VSS52	
179	DQ56		180	DQ60	MEM_B_DQ<60>
181	DQ57		182	DQ61	MEM_B_DQ<62>
183	VSS53		184	VSS54	
185	DM7		186	DQS7*	MEM_B_DQS_N<7>
187	VSS55		188	DQS7	MEM_B_DQS_P<7>
189	DQ58		190	VSS56	
191	DQ59		192	DQ62	MEM_B_DQ<58>
193	VSS57		194	DQ63	MEM_B_DQ<59>
195	SDA		196	VSS58	
197	SCL		198	SA0	MEM_B_SA0 (31A3)
199	VDDSPD		200	SA1	J3201_SA1

MEM_B_DQ<1> 72B3 16D4; MEM_B_DQ<4> 72B3 16D4
MEM_B_DQS_N<0> 72A3 16C1; MEM_B_DQS_P<0> 72A3 16C1
MEM_B_DQ<7> 72B3 16D4; MEM_B_DQ<3> 72B3 16D4
MEM_B_DQ<13> 72B3 16C4; MEM_B_DQ<12> 72B3 16C4
MEM_B_DQS_N<1> 72A3 16C1; MEM_B_DQS_P<1> 72A3 16C1
MEM_B_DQ<10> 72B3 16C4; MEM_B_DQ<8> 72B3 16C4
MEM_B_DQ<17> 72B3 16C4; MEM_B_DQ<20> 72B3 16C4
MEM_B_DQS_N<2> 72A3 16C1; MEM_B_DQS_P<2> 72A3 16C1
MEM_B_DQ<22> 72B3 16C4; MEM_B_DQ<18> 72B3 16C4
MEM_B_DQ<29> 72B3 16C4; MEM_B_DQ<27> 72B3 16C4
MEM_B_DM<3> 72B3 16C1
MEM_B_DQ<30> 72B3 16C4; MEM_B_DQ<31> 72B3 16C4
MEM_CKE<3> 72B3 32D6 15D3
MEM_B_BS<2> 72B3 32A6 16D1
MEM_B_A<12> 72B3 32A5 16B1; MEM_B_A<9> 72B3 32B5 16B1; MEM_B_A<8> 72B3 32B5 16B1
MEM_B_A<5> 72B3 32B5 16B1; MEM_B_A<3> 72B3 32B5 16B1; MEM_B_A<1> 72B3 32B5 16C1
MEM_B_A<10> 72B3 32B5 16B1; MEM_B_BS<0> 72B3 32A6 16D1; MEM_B_WE_L 72B3 32A6 16B1
MEM_B_CAS_L 72B3 32A6 16D1; MEM_CS_L<3> 72B3 32D6 15C3
MEM_ODT<3> 72B3 32D6 15C3
MEM_B_DQ<38> 72B3 16B4; MEM_B_DQ<32> 72B3 16C4
MEM_B_DQS_N<4> 72A3 16C1; MEM_B_DQS_P<4> 72A3 16C1
MEM_B_DQ<39> 72B3 16B4; MEM_B_DQ<35> 72B3 16B4
MEM_B_DQ<47> 72B3 16B4; MEM_B_DQ<45> 72B3 16B4
MEM_B_DM<5> 72B3 16C1
MEM_B_DQ<44> 72B3 16B4; MEM_B_DQ<40> 72B3 16B4
MEM_B_DQ<48> 72B3 16B4; MEM_B_DQ<52> 72B3 16B4
MEM_B_DQS_N<6> 72A3 16C1; MEM_B_DQS_P<6> 72A3 16C1
MEM_B_DQ<50> 72B3 16B4; MEM_B_DQ<55> 72B3 16B4
MEM_B_DQ<56> 72B3 16B4; MEM_B_DQ<57> 72B3 16B4
MEM_B_DM<7> 72A3 16C1
MEM_B_DQ<61> 72B3 16A4; MEM_B_DQ<63> 72B3 16A4
=I2C_SODIMMB_SDA 47C6; =I2C_SODIMMB_SCL 47C6

=GND_CHASSIS_DIPDIMM_RIGHT 201

=PP1V8_S3_MEM 7B4 30B2 30D4 30D6 31B2 31D6

DIMM_OVERTEMPB_L BB1
MEM_B_DM<2> 16C1 72B3
MEM_B_DQ<23> 16C4 72B3; MEM_B_DQ<19> 16C4 72B3
MEM_B_DQ<25> 16C4 72B3; MEM_B_DQ<28> 16C4 72B3
MEM_B_DQS_N<3> 16C1 72A3; MEM_B_DQS_P<3> 16C1 72A3
MEM_B_DQ<24> 16C4 72B3; MEM_B_DQ<26> 16C4 72B3
MEM_CKE<4> 15D3 32D5 72B3
MEM_B_A<15> 8B4; MEM_B_A<14> 15C6 32A5 72B3
MEM_B_A<11> 16B1 32A5 72B3; MEM_B_A<7> 16B1 32B5 72B3; MEM_B_A<6> 16B1 32B5 72B3
MEM_B_A<4> 16B1 32B5 72B3; MEM_B_A<2> 16B1 32B5 72B3; MEM_B_A<0> 16C1 32B5 72B3
MEM_B_BS<1> 16D1 32A6 72B3; MEM_B_RAS_L 16B1 32A6 72B3; MEM_CS_L<2> 15D3 32D6 72B3
MEM_ODT<2> 15C3 32D6 72B3; MEM_B_A<13> 16B1 32A5 72B3
MEM_B_DQ<36> 16B4 72B3; MEM_B_DQ<37> 16B4 72B3
MEM_B_DM<4> 16C1 72B3
MEM_B_DQ<34> 16B4 72B3; MEM_B_DQ<33> 16C4 72B3
MEM_B_DQ<43> 16B4 72B3; MEM_B_DQ<42> 16B4 72B3
MEM_B_DQS_N<5> 16C1 72A3; MEM_B_DQS_P<5> 16C1 72A3
MEM_B_DQ<41> 16B4 72B3; MEM_B_DQ<46> 16B4 72B3
MEM_B_DQ<53> 16B4 72B3; MEM_B_DQ<49> 16B4 72B3
MEM_CLK_P<4> 15D3 72B3; MEM_CLK_N<4> 15D3 72B3
MEM_B_DM<6> 16C1 72A3
MEM_B_DQ<51> 16B4 72B3; MEM_B_DQ<54> 16B4 72B3
MEM_B_DQ<60> 16A4 72B3; MEM_B_DQ<62> 16A4 72B3
MEM_B_DQS_N<7> 16C1 72A3; MEM_B_DQS_P<7> 16C1 72A3
MEM_B_DQ<58> 16B4 72B3; MEM_B_DQ<59> 16B4 72B3
MEM_B_SA0 31A3

516-0135

202 =GND_CHASSIS_DIPDIMM_CENTER

ADDR=0xA4(WR)/0xA5(RD)

31A4 MEM_B_SA0 — R3203 10K 5% 1/16W MF-LF 402

31A3 30A7 7C4 =PPSPD_S0_MEM

C3222 2.2UF 20% 4V X5R 402
C3221 0.1UF 20% 10V CERM 402

=PPSPD_S0_MEM 7C4 30A7 31A7

R3200 10K 5% 1/10W MF-LF 402

Resistor prevents pwr-gnd short

DDR2 SO-DIMM Connector B		
SYNC_MASTER=MEMORY	SYNC_DATE=06/20/2005	
NOTICE OF PROPRIETARY PROPERTY		
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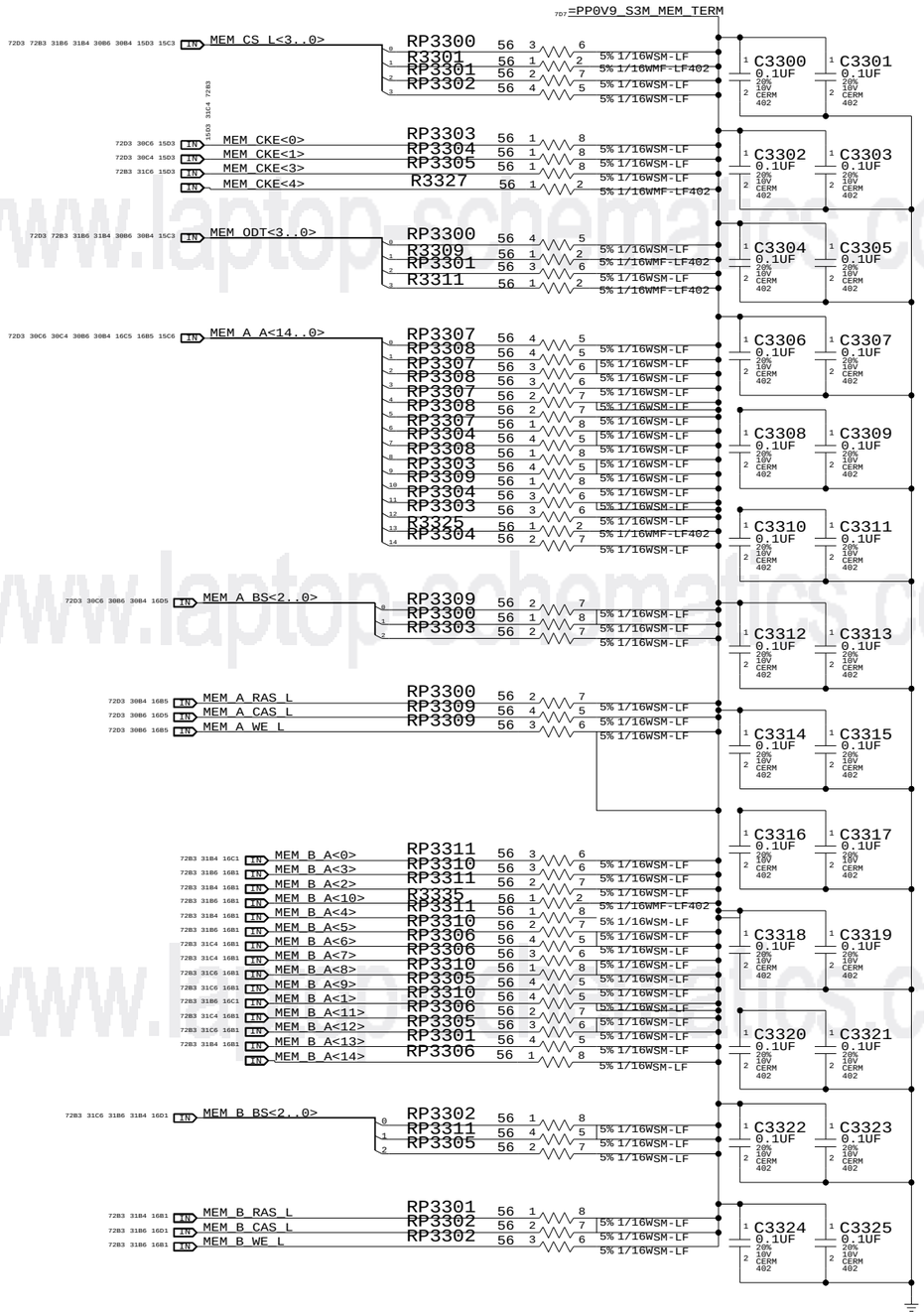
APPLE INC.	SIZE D	DRAWING NUMBER 051-7559 REV. S
	SCALE NONE	SHT 32 OF 106

One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



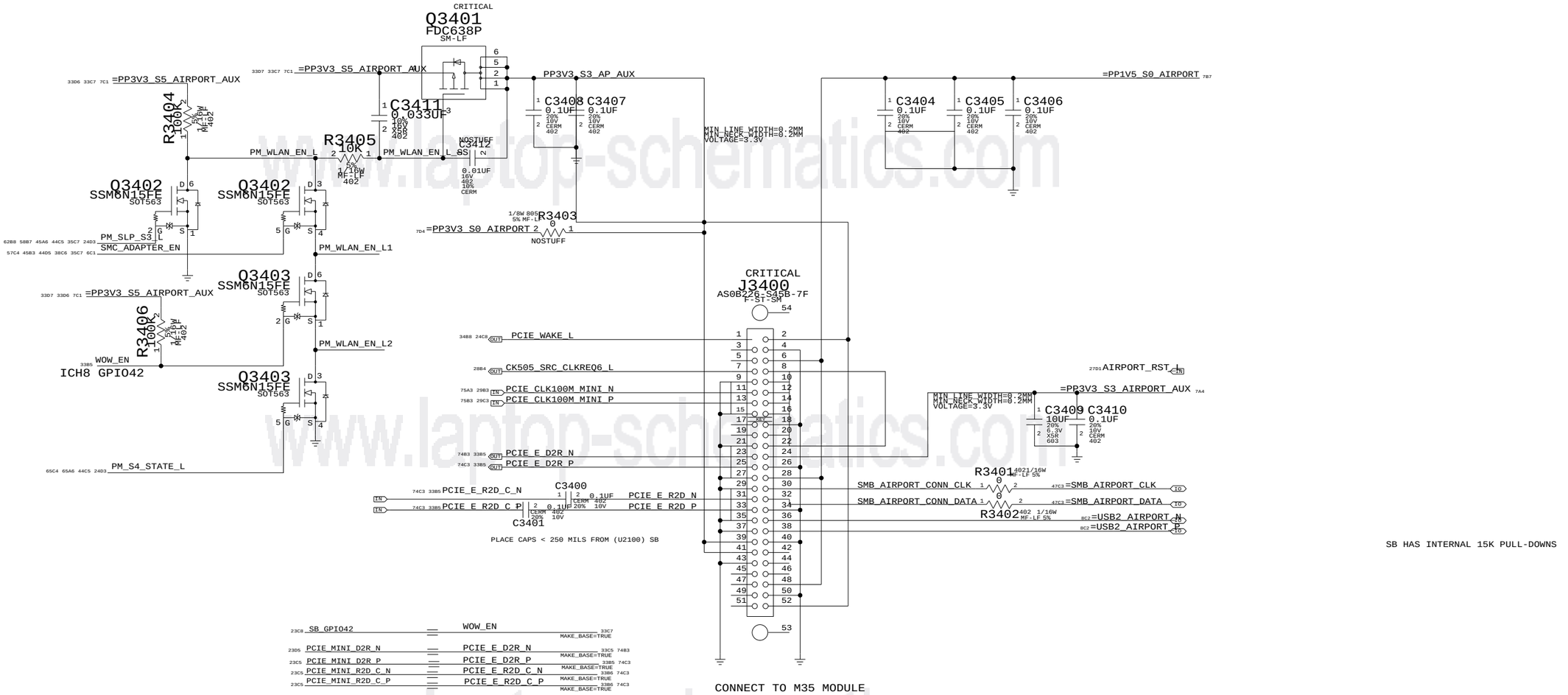
LAYOUT NOTE:PLACE ONE CAP CLOSE TO EVERY TWO PULLUP RESISTORS TERMINATED TO PP0V9_S0_MEM_TERM

Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	33	106



AIRPORT CONNECTOR

SYNC_MASTER=ENET SYNC_DATE=08/19/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	34	106

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V8R2V5_ENET_PHY (2.5V / 1.8V)
- =YUKON_EC_PP2V5_ENET (2.5V / GND)
- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL

BOM options provided by this page:
YUKON_EC - Selects Yukon EC RSET value.
YUKON_ULTRA - Selects Yukon Ultra RSET.

NOTE: Yukon IC and EEPROM are OMITted on this page. Proper part numbers must be called out elsewhere.

NOTE: See bottom of page for instructions for dual Yukon EC / Yukon Ultra schematic support.

=PP1V2_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	171 mA	No link:	130 mA
10 Mbps:	179 mA	10 Mbps:	130 mA
100 Mbps:	203 mA	100 Mbps:	150 mA
1000 Mbps:	426 mA	1000 Mbps:	290 mA

C3700 4.7UF 20% 6.3V CERM 603; C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 0.1UF 10% 16V X5R 402

=PP3V3_ENET_PHY

Yukon EC		Yukon Ultra	
No link:	4 mA	No link:	60 mA
10 Mbps:	4 mA	10 Mbps:	70 mA
100 Mbps:	4 mA	100 Mbps:	70 mA
1000 Mbps:	4 mA	1000 Mbps:	80 mA

C3710 4.7UF 20% 6.3V CERM 603; C3711 C3712 C3713 0.1UF 10% 16V X5R 402; C3714 0.001UF 10% 50V CERM 402; C3715 0.001UF 10% 50V CERM 402

L3720 FERR-120-OHM-1.5A 0402-LF

=PP1V8R2V5_ENET_PHY — PP1V8R2V5_ENET_PHY_AVDD (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.22 mm, VOLTAGE=1.8V)

Yukon EC (2.5V)		Yukon Ultra (1.8V)	
No link:	82 mA	No link:	0 mA
10 Mbps:	108 mA	10 Mbps:	30 mA
100 Mbps:	126 mA	100 Mbps:	40 mA
1000 Mbps:	218 mA	1000 Mbps:	150 mA

(EC:2.5V)

C3720 4.7UF 20% 6.3V CERM 603; C3721 C3722 C3723 0.1UF 10% 16V X5R 402; C3724 0.001UF 10% 50V CERM 402

=YUKON_EC_PP2V5_ENET

Yukon EC: Alias to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF & 1x 0.001uF caps
Yukon Ultra: Alias to GND

PCIE_ENET_D2R_P
PCIE_ENET_D2R_N
PCIE_ENET_R2D_C_P — C3730 0.1UF 10% 16V X5R 402 — PLACEMENT_NOTE=Place C3730 close to southbridge.
PCIE_ENET_R2D_C_N — C3731 0.1UF 10% 16V X5R 402 — PLACEMENT_NOTE=Place C3731 close to southbridge.
C3735 0.1UF 10% 16V X5R 402
C3736 0.1UF 10% 16V X5R 402

PCIE_ENET_D2R_C_P
PCIE_ENET_D2R_C_N
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N

PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
=ENET_CLKREQ_L
PCIE_WAKE_L
ENET_RESET_L

Yukon EC: Pin 42 should be NC (or TP) net.

ENET_MDI_P<0>
ENET_MDI_N<0>
ENET_MDI_P<1>
ENET_MDI_N<1>
ENET_MDI_P<2>
ENET_MDI_N<2>
ENET_MDI_P<3>
ENET_MDI_N<3>

SIGNAL_MODEL=EMPTY
R3740 R3741 R3742 R3743 R3744 R3745 R3746 R3747 49.9 1% 1/16W MF-LF 402
ENET_MDI0 ENET_MDI1 ENET_MDI2 ENET_MDI3
C3740 C3742 C3744 C3746 0.001UF 10% 50V CERM 402

CRITICAL
Y3750 SM-3.2X2.5MM 25.0000M 16pF
C3750 C3751 15PF 5% 50V CERM 402 NC NC

ENET_CLK25M_XTALI
ENET_CLK25M_XTALO

U3700 88E8058 QFN CRITICAL

NC_32		AVDD0	19
NC_51		AVDD1	22
NC_52		AVDD2	23
NC_57		AVDD3	28
NC_64			

EC:AVDD 2.5

VDDO_TTL0	1	AVDDH	8
VDDO_TTL1	40	VDD0	2
VDDO_TTL2	45	VDD1	7
VDDO_TTL3	61	VDD2	13
		VDD3	33
		VDD4	39
		VDD5	44
		VDD6	48
		VDD7	58

PCI EXPRESS
TX_P 49 PCIE_ENET_D2R_C_P
TX_N 50 PCIE_ENET_D2R_C_N
RX_P 54 PCIE_ENET_R2D_P
RX_N 53 PCIE_ENET_R2D_N
REFCLKP 55
REFCLKN 56
CLKREQ* 42 EC:NO CONNECT
WAKE* 6
PERST* 5
MDIP0 17
MDIN0 18
MDIP1 20
MDIN1 21
MDIP2 26
MDIN2 27
MDIP3 30
MDIN3 31
XTALI 15
XTALO 14
THRML_PAD 65

ANALOG
EC:CTRL25
LOM_DISABLE* 10 — ENET_LOM_DIS_L
VAUX_AVLBL 12
SWITCH_VAUX 9 NC
VMAIN_AVLBL 47 — Must be high in S0 state (can use PP3V3_S0 as input) =ENET_VMAIN_AVLBL
SWITCH_VCC 11 NC
CTRL18 4 — TP_YUKON_CTRL18
CTRL12 3 — TP_YUKON_CTRL12
RSET 16 — YUKON_RSET

LED
LED_ACT* 59 NC
LED_LINK10/100* 60 NC
LED_LINK1000* 62 NC
LED_DUPLEX* 63 NC

SPI
(IPU) SPI_DO 34 NC
(IPU) SPI_DI 35 NC
(IPU) SPI_CLK 37 NC
(IPU) SPI_CS 36 NC

MEDIA

TWSI
(IPU) VPD_CLK 38 — YUKON_VPD_CLK
(IPU) VPD_DATA 41 — YUKON_VPD_DATA

TEST/RSVD
(IPD) TESTMODE 46
RSVD_24 24 NC
RSVD_25 25 NC
RSVD_29 29 NC
RSVD_43 43 NC

MAIN CLK

R3760 4.7K 5% 1/10W MF-LF 402 — EC:AVDD 2.5

YUKON_ULTRA
R3765 4.99K 1% 1/16W MF-LF 402 — If characterization shows eye height is too small, make R3765 smaller

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/10W MF-LF 402
R3781 4.7K 5% 1/10W MF-LF 402
U3780 M24C08 SO8 CRITICAL
E2 NC1 NC0 WC* VCC VSS SDA SCL
OMIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0285	1	RES,4.87K,1%,1/16W,0402,LF	R3760		YUKON_EC

To support Yukon EC and Ultra on the same board:
- Alias =YUKON_EC_PP2V5_ENET to PP1V8R2V5_ENET_PHY_AVDD, add 1x 0.1uF and 1x 0.001uF caps
- Use 0-ohm resistors or variable supply to provide 1.8V or 2.5V to =PP1V8R2V5_ENET_PHY
- Connect =ENET_CLKREQ_L to clock generator via 0-ohm resistor (BOMOPTION: YUKON_ULTRA)
- Use YUKON_EC and YUKON_ULTRA BOMOPTIONs to select stuffed part

Ethernet (Yukon)

SYNC_MASTER=USB SYNC_DATE=10/07/2006

APPLE INC.

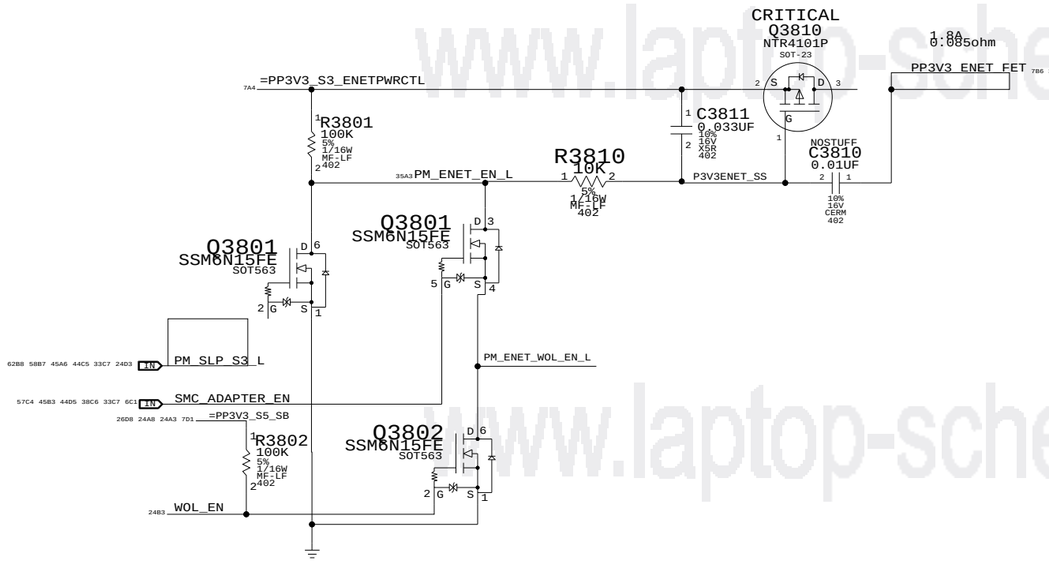
SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 37 OF 106

ENET Enable Generation

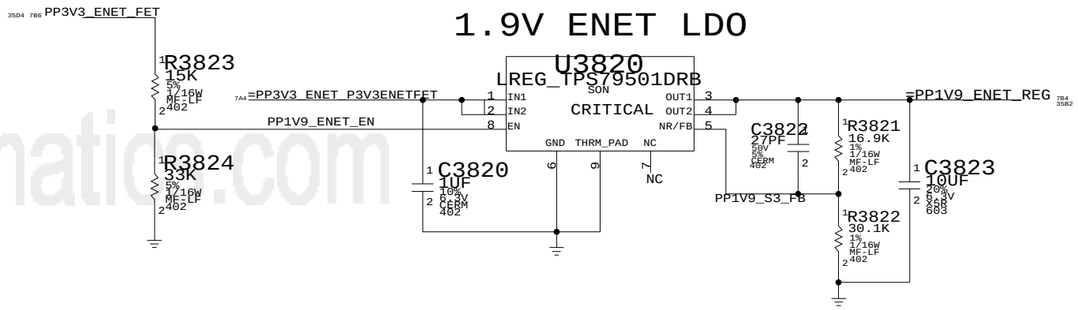
"ENET" = "S0" || AC

3.3V ENET FET



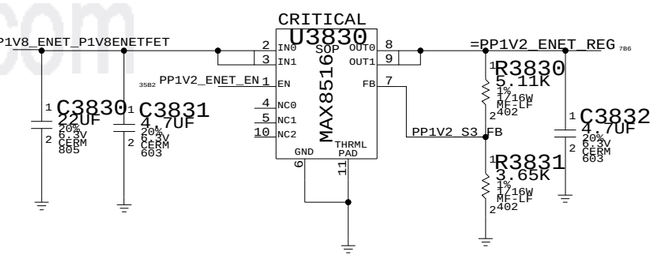
Name	PM_SLP_S3_L	SMC_ADAPTER_EN	PM_ENET_EN_L	PM_ENET_EN	Yukon Power
Logic	S0	AC			Powered by S3
S0 on Battery	High (3.3V)	Low (0V)	Low (0V)	High (3.3V)	Power
S3 on Battery	Low (0V)	Low (0V)	High (3.3V)	Low (0V)	Power
S0 on AC	High (3.3V)	High (3.3V)	Low (0V)	High (3.3V)	Power
S3 on AC	Low (0V)	High (3.3V)	Low (0V)	High (3.3V)	Power
S5 on anything	N/A	N/A	N/A	N/A	No Power

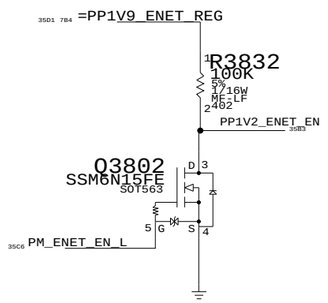
1.9V ENET LDO



Vout = 1.2246V * (1 + R3821 / R3822)

1.2V ENET LDO





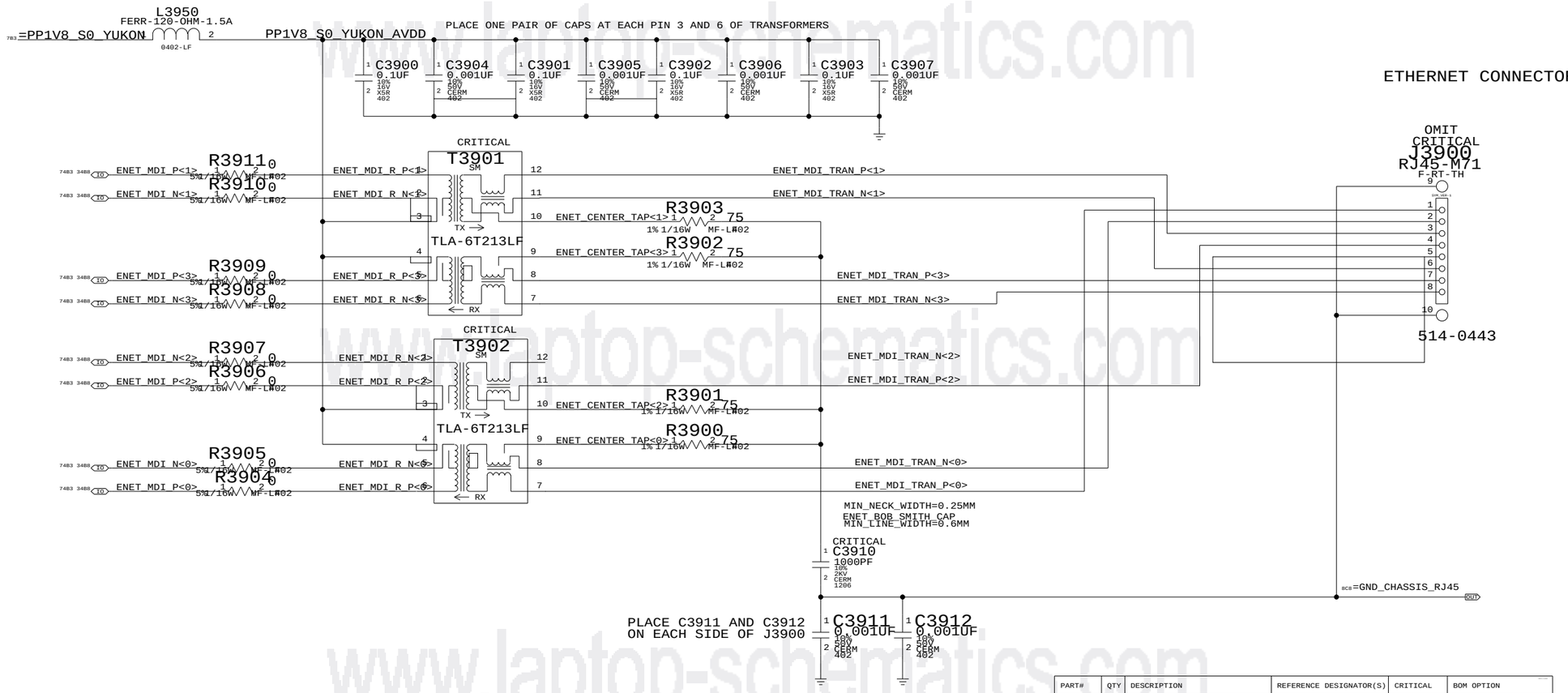
Yukon Power Control

SYNC_MASTER=USB SYNC_DATE=10/07/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	38	106



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0443	1	CONN,8P RJ-45 JACK,TH,MG3,LF	J3900	CRITICAL	NORMAL
514-0475	1	CONN,8P RJ-45 JACK,TH,BLACK,LF	J3900	CRITICAL	FANCY

ETHERNET CONNECTOR

SYNC_MASTER=USB SYNC_DATE=09/14/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	39	106

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW323-06 ADDED
6/21/2005 - CHANGED INT_IO_INT_PIRQD_L (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_ID TO AD16 (PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ3_L TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST_L AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_PME DIFF PAIR NAMES TO BE BE-DSE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PCA CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

=PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4024 ON VDD0

C4024 10UF 20% 6.3V X5R 603
C4018 0.1UF 10% 10V CERM 402
C4022 0.1UF 10% 10V CERM 402
C4026 0.1UF 10% 10V CERM 402
C4028 0.1UF 10% 10V CERM 402
C4030 0.1UF 10% 10V CERM 402
C4032 0.1UF 10% 10V CERM 402

L4000 600-OHM-300MA 0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4016 ON VDDA0

C4016 10UF 20% 6.3V X5R 603
C4017 0.1UF 10% 10V X5R 402
C4029 0.1UF 10% 10V X5R 402
C4025 0.1UF 10% 10V X5R 402

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

=PP3V3_S3_PCI

VDD0 G4, VDD1 N1, VDD2 N2, VDD3 K5, VDD4 K6, VDD5 K7, VDD6 L13, VDD7 H13, VDD9 A2
VDDA0 D10, VDDA1 A13, VDDA2 B13, VDDA3 A7, VDDA4 A8, VDDA5 D6

CONNECT TO VDD FOR 3.3V OPERATION

PCI_VIOS G13

PCI_AD<0>	F10	PCI_AD0
PCI_AD<1>	G10	PCI_AD1
PCI_AD<2>	H10	PCI_AD2
PCI_AD<3>	H12	PCI_AD3
PCI_AD<4>	J13	PCI_AD4
PCI_AD<5>	J12	PCI_AD5
PCI_AD<6>	K13	PCI_AD6
PCI_AD<7>	K10	PCI_AD7
PCI_AD<8>	L12	PCI_AD8
PCI_AD<9>	M13	PCI_AD9
PCI_AD<10>	L11	PCI_AD10
PCI_AD<11>	M12	PCI_AD11
PCI_AD<12>	M11	PCI_AD12
PCI_AD<13>	N12	PCI_AD13
PCI_AD<14>	M10	PCI_AD14
PCI_AD<15>	N11	PCI_AD15
PCI_AD<16>	M4	PCI_AD16
PCI_AD<17>	N5	PCI_AD17
PCI_AD<18>	N4	PCI_AD18
	M3	PCI_AD19
PCI_AD<19>		
PCI_AD<20>	M2	PCI_AD20
PCI_AD<21>	N3	PCI_AD21
PCI_AD<22>	K4	PCI_AD22
PCI_AD<23>	M1	PCI_AD23
PCI_AD<24>	K2	PCI_AD24
PCI_AD<25>	J4	PCI_AD25
PCI_AD<26>	K1	PCI_AD26
PCI_AD<27>	J2	PCI_AD27
PCI_AD<28>	J1	PCI_AD28
PCI_AD<29>	H2	PCI_AD29
PCI_AD<30>	H4	PCI_AD30
PCI_AD<31>	H1	PCI_AD31

PCI_C_BE_L<0>	K12	PCI_CBE0*
PCI_C_BE_L<1>	M9	PCI_CBE1*
PCI_C_BE_L<2>	L3	PCI_CBE2*
PCI_C_BE_L<3>	L1	PCI_CBE3*
PCI_PAR	N10	PCI_PAR
PCI_FRAME_L	N6	PCI_FRAME*
PCI_IRDY_L	M6	PCI_IRDY*
PCI_TRDY_L	N7	PCI_TRDY*
PCI_DEVSEL_L	N8	PCI_DEVSEL*
PCI_STOP_L	M7	PCI_STOP*
FW_PCI_IDSEL	L2	PCI_IDSEL
PCI_FW_REQ_L	E2	PCI_REQ*
PCI_FW_GNT_L	E1	PCI_GNT*
PCI_PERR_L	M8	PCI_PERR*
PCI_SERR_L	N9	PCI_SERR*
PCI_CLK33M_FW	G2	PCI_CLK
PM_CLKRUN_L	D1	CLKRUN*
FW_PCI_RST_L	F1	PCI_RST*
INT_PIRQD_L	D2	PCI_INTA*
PCI_PME_FW_L	F2	PCI_PME*

R4031 22 5% 1/16W MF-LF 402
R4032 100 1% 1/16W MF-LF 402
PCI_RST_L
THIS IS FROM ICH-8
PLACE R4032 VERY CLOSE TO SB

CRITICAL
U4000
FW32306
BGA

VSS0 A1, VSS1 B2, VSS2 C3, VSS3 D4, VSS4 E4, VSS5 E5, VSS6 F4, VSS7 F6, VSS8 F7, VSS9 F8, VSS10 G1, VSS11 G6, VSS12 G7, VSS13 G8, VSS14 H6, VSS15 H7, VSS16 H8, VSS17 J5, VSS18 J9, VSS19 J10, VSS20 K8, VSS21 K9, VSS22 N13
VSSA0 E13, VSSA1 E9, VSSA2 D9, VSSA3 D7, VSSA4 D5

197S0030 3.2MMX2.5MM
CRITICAL
Y4003
SM-3.2X2.5MM
24.576MHZ
R4000 390 5% 1/16W MF-LF 402
C4011 15PF 5% 50V CERM 402
C4012 15PF 5% 50V CERM 402
NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI A5 FW_XI
XO B5 FW_XO
RESET* B4 FW_PWRON_RST_L
R1 A6 FW_R1
R0 B7 FW_R0
SPEC RECOMMENDS 2.49K

R4052 2.1K 1% 1/16W MF-LF 402
C4020 0.1UF 10% 10V X5R 402
R4020 510K 5% 1/16W MF-LF 402

TPBIAS0	B8	FW_A_TPBIAS
TPA0_P	A9	FW_A_TPA_P
TPA0_N	B9	FW_A_TPA_N
TPB0_P	B10	FW_A_TPB_P
TPB0_N	A10	FW_A_TPB_N
TPBIAS1	D8	FW_B_TPBIAS
TPA1_P	A11	FW_B_TPA_P
TPA1_N	B11	FW_B_TPA_N
TPB1_P	B12	FW_B_TPB_P
TPB1_N	A12	FW_B_TPB_N
TPBIAS2	C13	FW_C_TPBIAS
TPA2_P	C11	FW_C_TPA_P
TPA2_N	C12	FW_C_TPA_N
TPB2_P	D13	FW_C_TPB_P
TPB2_N	D12	FW_C_TPB_N

MODE_420 M5, MODE_A B6 — MODE FOR EXTERNAL LINK
PC0 E12 FW_PC0
PC1 F13
PC2 F12
CONTENDER G12 — LOW = NOT BUS MANAGER
CARDBUSN B1 — LOW = PCI OPERATION
MPCI_ACTN_323 E10

DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’)
SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)

MANUFACTURING TEST PINS
TEST0 C2 FW_TEST0
TEST1 C1 FW_TEST1
PTEST A4 FW_PTEST
SE A3 FW_SE
SM B3 FW_SM

R4033 47 5% 1/16W MF-LF 402
R4034 47 5% 1/16W MF-LF 402
R4035 47 5% 1/16W MF-LF 402
R4036 47 5% 1/16W MF-LF 402
R4037 47 5% 1/16W MF-LF 402

FIREWIRE CONTROLLER

SYNC_MASTER=ENETSYNC_DATE=08/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE
SHT 40 OF 106

Page Notes

INPUT:

=PPBUS_FW - PORT POWER

=PP3V3_S5_FW - DIGITAL POWER

=GND_CHASSIS_FW_PORT0 - CHASSIS GROUND

=FWPWR_PWRON - ADDITIONAL POWER CONTROL

INPUT/OUTPUT:

FW_TPA0_P/N,FW_TPB0_P/N,FW_TPBIAS0 - FIREWIRE DIFF PAIRS

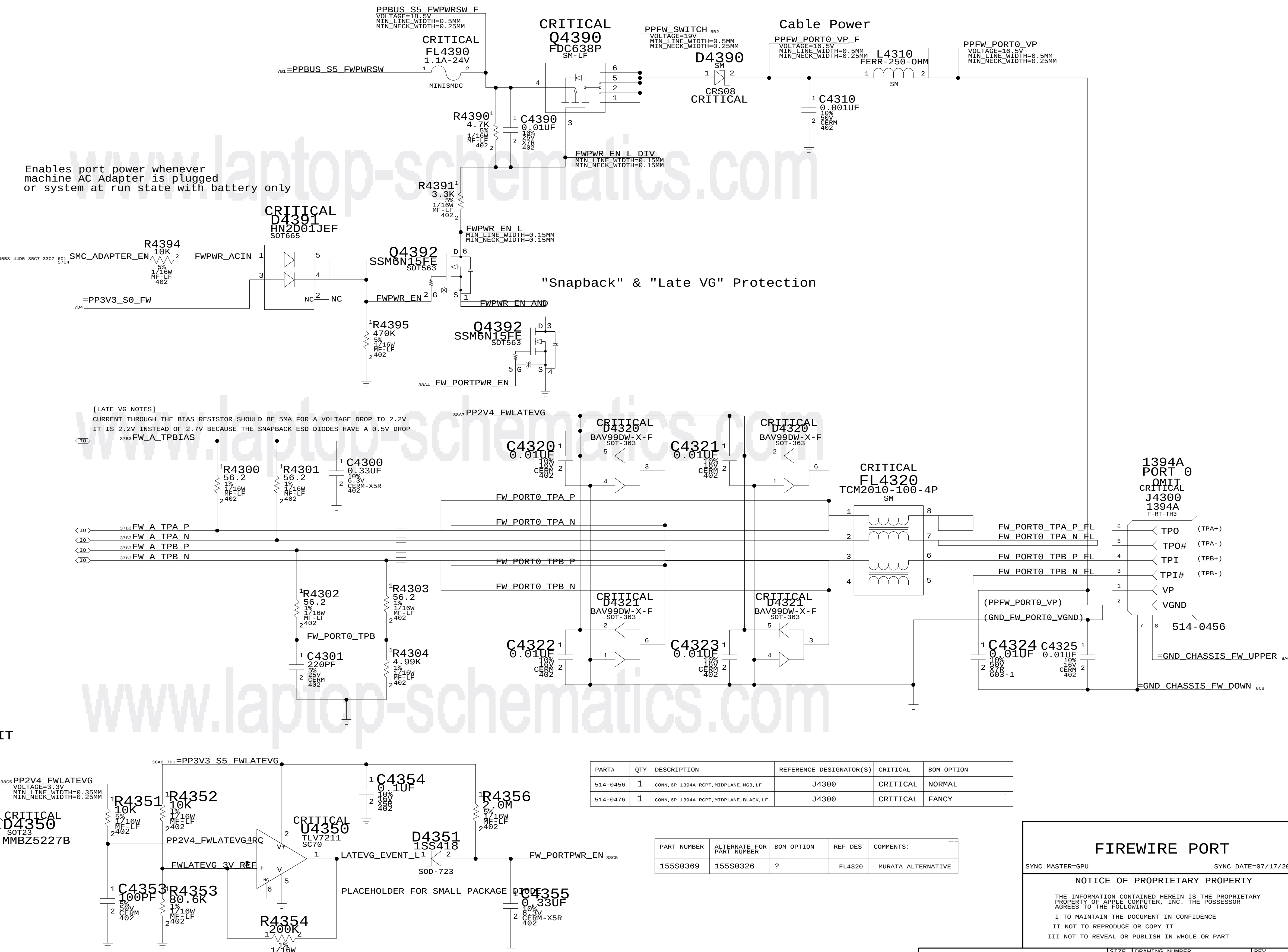
OUTPUT:

FW_PC0 - POWER CLASS IDENTIFIER (SINGLE PORT - TIE LOW)

PAGE HISTORY

5/19/05 - INITIAL REVISION
6/22/05 - CHANGED DIFF PAIR NAMES TO MATCH REUSE
6/22/05 - REMOVED CONSTRAINTS BECAUSE USING ALLEGRO CONST MANAGER
6/22/05 - CONNECTED FW_PC0 FOR SINGLE PORT
7/26/05 - UPDATED LATE-VG POWER RAIL CIRCUIT FROM M1
7/26/05 - CHANGED CONNECTOR PORT NAMING TO PORT0
7/26/05 - SWITCHED TO 514-0124 FOR PRE-PROTO CONNECTOR
7/26/05 - REMOVED R4520 - IT HASN'T BEEN STUFFED FOR MANY PRODUCTS
7/26/05 - CHANGED FL4590 TO 1.1A VERSION
7/26/05 - REMOVED ETHERNET LOW-POWER MODE CIRCUIT
7/26/05 - UPDATED SIGNAL NAMES FOR FW PORT POWER ENABLE

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)



Enables port power whenever machine AC Adapter is plugged or system at run state with battery only
PPBUS_S5_FWPWRSW_F
VOLTAGE=18.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
=PPBUS_S5_FWPWRSW
CRITICAL FL4390 1.1A-24V MINISMDC
CRITICAL Q4390 FDC638P SM-LF
PPFW_SWITCH
VOLTAGE=19V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
D4390 SM CRS08 CRITICAL
Cable Power
PPFW_PORT0_VP_F
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
L4310 FERR-250-OHM SM
PPFW_PORT0_VP
VOLTAGE=16.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C4310 0.001UF 10% 50V CERM 402
R4390 4.7K 5% 1/16W MF-LF 402
C4390 0.01UF 10% 25V X7R 402
FWPWR_EN_L_DIV
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.15MM
R4391 3.3K 5% 1/16W MF-LF 402
FWPWR_EN_L
MIN_LINE_WIDTH=0.15MM
MIN_NECK_WIDTH=0.15MM
CRITICAL D4391 HN2D01JEF SOT665
R4394 10K 5% 1/16W MF-LF 402
SMC_ADAPTER_EN
FWPWR_ACIN
=PP3V3_S0_FW
NC
Q4392 SSM6N15FE SOT563
FWPWR_EN
FWPWR_EN_AND
"Snapback" & "Late VG" Protection
R4395 470K 5% 1/16W MF-LF 402
Q4392 SSM6N15FE SOT563
FW_PORTPWR_EN
PORT POWER CLASS
0 FOR SINGLE PORT
1 FOR DUAL PORT
FW_PC0
[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A 0.5V DROP
FW_A_TPBIAS
FW_A_TPA_P
FW_A_TPA_N
FW_A_TPB_P
FW_A_TPB_N
R4300 56.2 1% 1/16W MF-LF 402
R4301 56.2 1% 1/16W MF-LF 402
C4300 0.33UF 10% 6.3V CERM-X5R 402
PP2V4_FWLATEVG
CRITICAL D4320 BAV99DW-X-F SOT-363
C4320 0.01UF 10% 16V CERM 402
C4321 0.01UF 10% 16V CERM 402
FW_PORT0_TPA_P
FW_PORT0_TPA_N
FW_PORT0_TPB_P
FW_PORT0_TPB_N
CRITICAL FL4320 TCM2010-100-4P SM
R4302 56.2 1% 1/16W MF-LF 402
R4303 56.2 1% 1/16W MF-LF 402
FW_PORT0_TPB
C4301 220PF 5% 25V CERM 402
R4304 4.99K 1% 1/16W MF-LF 402
CRITICAL D4321 BAV99DW-X-F SOT-363
C4322 0.01UF 10% 16V CERM 402
C4323 0.01UF 10% 16V CERM 402
1394A PORT 0 OMIT CRITICAL J4300 1394A F-RT-TH3
FW_PORT0_TPA_P_FL
FW_PORT0_TPA_N_FL
FW_PORT0_TPB_P_FL
FW_PORT0_TPB_N_FL
TPO (TPA+)
TPO# (TPA-)
TPI (TPB+)
TPI# (TPB-)
VP
VGND
514-0456
(PPFW_PORT0_VP)
(GND_FW_PORT0_VGND)
C4324 0.01UF 10% 50V X7R 603-1
C4325 0.01UF 10% 16V CERM 402
=GND_CHASSIS_FW_UPPER
=GND_CHASSIS_FW_DOWN
LATE-VG DETECTION CIRCUIT
R4350 330 5% 1/16W MF-LF 402
=PP3V3_S5_FWLATEVG
NO STUFF C4352 0.001UF 10% 50V CERM 402
CRITICAL D4350 SOT23 MMBZ5227B
PP2V4_FWLATEVG
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM
R4351 10K 5% 1/16W MF-LF 402
R4352 10K 1% 1/16W MF-LF 402
=PP3V3_S5_FWLATEVG
C4354 0.1UF 10% 16V X5R 402
R4356 2.0M 5% 1/16W MF-LF 402
CRITICAL U4350 TLV7211 SC70
FWLATEVG_3V_REF
LATEVG_EVENT_L
D4351 1SS418 SOD-723
FW_PORTPWR_EN
C4353 100PF 5% 50V CERM 402
R4353 80.6K 1% 1/16W MF-LF 402
R4354 200K 1% 1/16W MF-LF 402
PLACEHOLDER FOR SMALL PACKAGE DIODE
C4355 0.33UF 10% 6.3V CERM-X5R 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0456	1	CONN,6P 1394A RCPT,MIDPLANE,MG3,LF	J4300	CRITICAL	NORMAL
514-0476	1	CONN,6P 1394A RCPT,MIDPLANE,BLACK,LF	J4300	CRITICAL	FANCY

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0369	155S0326	?	FL4320	MURATA ALTERNATIVE

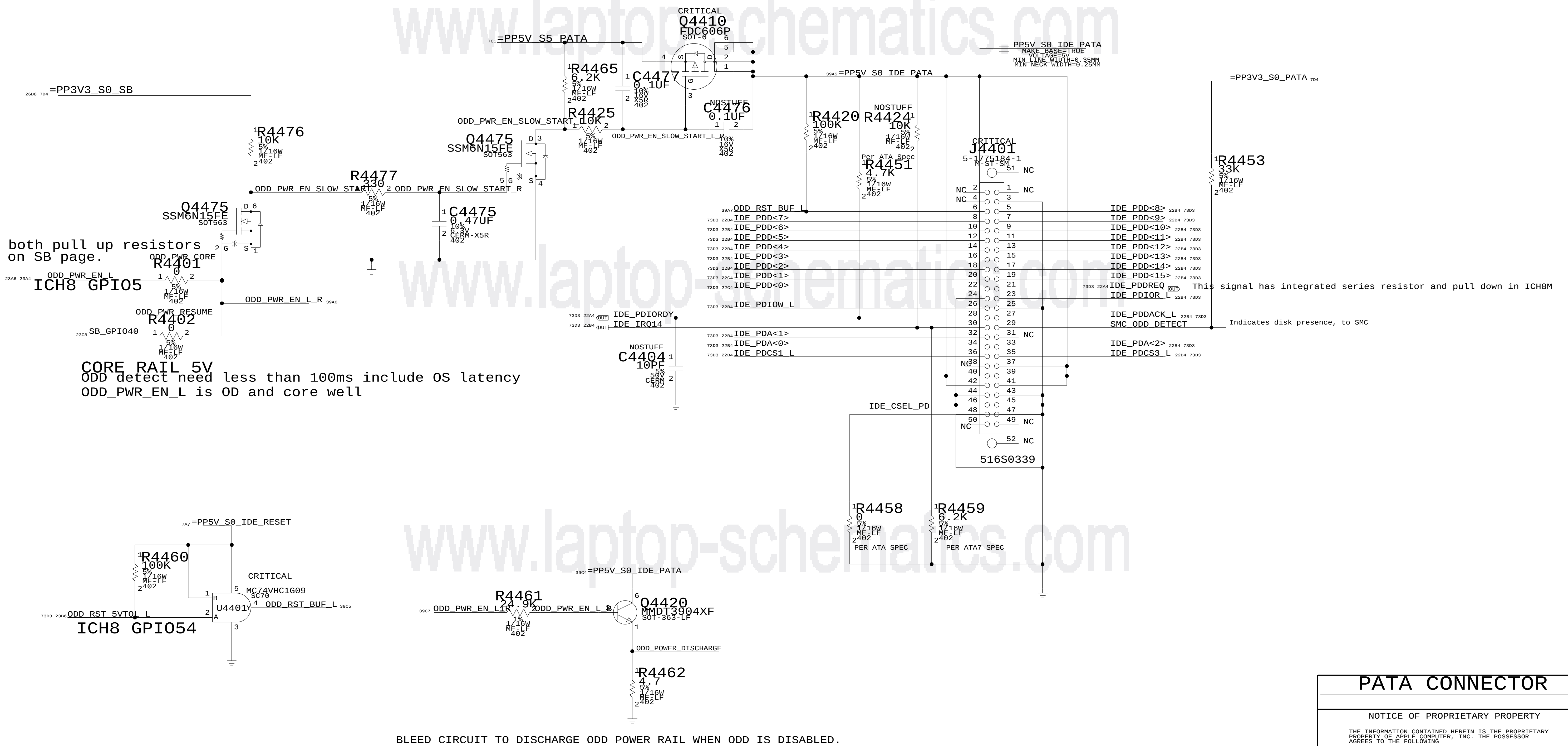
FIREWIRE PORT

SYNC_MASTER=GPU SYNC_DATE=07/17/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 43 OF 106



=PP5V_S5_PATA
CRITICAL
Q4410
FDC606P
SOT-6
=PP3V3_S0_SB
R4476
10K
5%
1/16W
MF-LF
402
R4465
6.2K
C4477
0.1UF
10%
16V
X5R
402
R4425
10K
ODD_PWR_EN_SLOW_START
ODD_PWR_EN_SLOW_START_L_R
NOSTUFF
C4476
0.1UF
Q4475
SSM6N15FE
SOT563
R4477
330
ODD_PWR_EN_SLOW_START_R
C4475
0.47UF
6.3V
CERM-X5R
both pull up resistors
on SB page.
ODD_PWR_CORE
R4401
0
ODD_PWR_EN_L
ICH8 GPIO5
ODD_PWR_EN_L_R
ODD_PWR_RESUME
R4402
0
SB_GPIO40
CORE RAIL 5V
ODD detect need less than 100ms include OS latency
ODD_PWR_EN_L is OD and core well
PP5V_S0_IDE_PATA
MAKE_BASE=TRUE
VOLTAGE=5V
MIN_LINE_WIDTH=0.35MM
MIN_NECK_WIDTH=0.25MM
=PP5V_S0_IDE_PATA
R4420
100K
NOSTUFF
R4424
10K
Per ATA Spec
R4451
4.7K
CRITICAL
J4401
5-1775184-1
M-ST-SM
516S0339
=PP3V3_S0_PATA
R4453
33K
ODD_RST_BUF_L
IDE_PDD<7>
IDE_PDD<6>
IDE_PDD<5>
IDE_PDD<4>
IDE_PDD<3>
IDE_PDD<2>
IDE_PDD<1>
IDE_PDD<0>
IDE_PDIOW_L
IDE_PDIORDY
IDE_IRQ14
IDE_PDA<1>
IDE_PDA<0>
IDE_PDCS1_L
IDE_PDD<8>
IDE_PDD<9>
IDE_PDD<10>
IDE_PDD<11>
IDE_PDD<12>
IDE_PDD<13>
IDE_PDD<14>
IDE_PDD<15>
IDE_PDDREQ
This signal has integrated series resistor and pull down in ICH8M
IDE_PDIOR_L
IDE_PDDACK_L
SMC_ODD_DETECT
Indicates disk presence, to SMC
IDE_PDA<2>
IDE_PDCS3_L
NOSTUFF
C4404
10PF
5%
50V
CERM
402
IDE_CSEL_PD
NC
R4458
0
PER ATA SPEC
R4459
6.2K
PER ATA7 SPEC
=PP5V_S0_IDE_RESET
R4460
100K
CRITICAL
MC74VHC1G09
SC70
U4401
ODD_RST_5VTOL_L
ICH8 GPIO54
ODD_RST_BUF_L
=PP5V_S0_IDE_PATA
R4461
24.9K
1%
ODD_PWR_EN_L_R
ODD_PWR_EN_L_B
Q4420
MMDT3904XF
SOT-363-LF
ODD_POWER_DISCHARGE
R4462
4.7
BLEED CIRCUIT TO DISCHARGE ODD POWER RAIL WHEN ODD IS DISABLED.

PATA CONNECTOR

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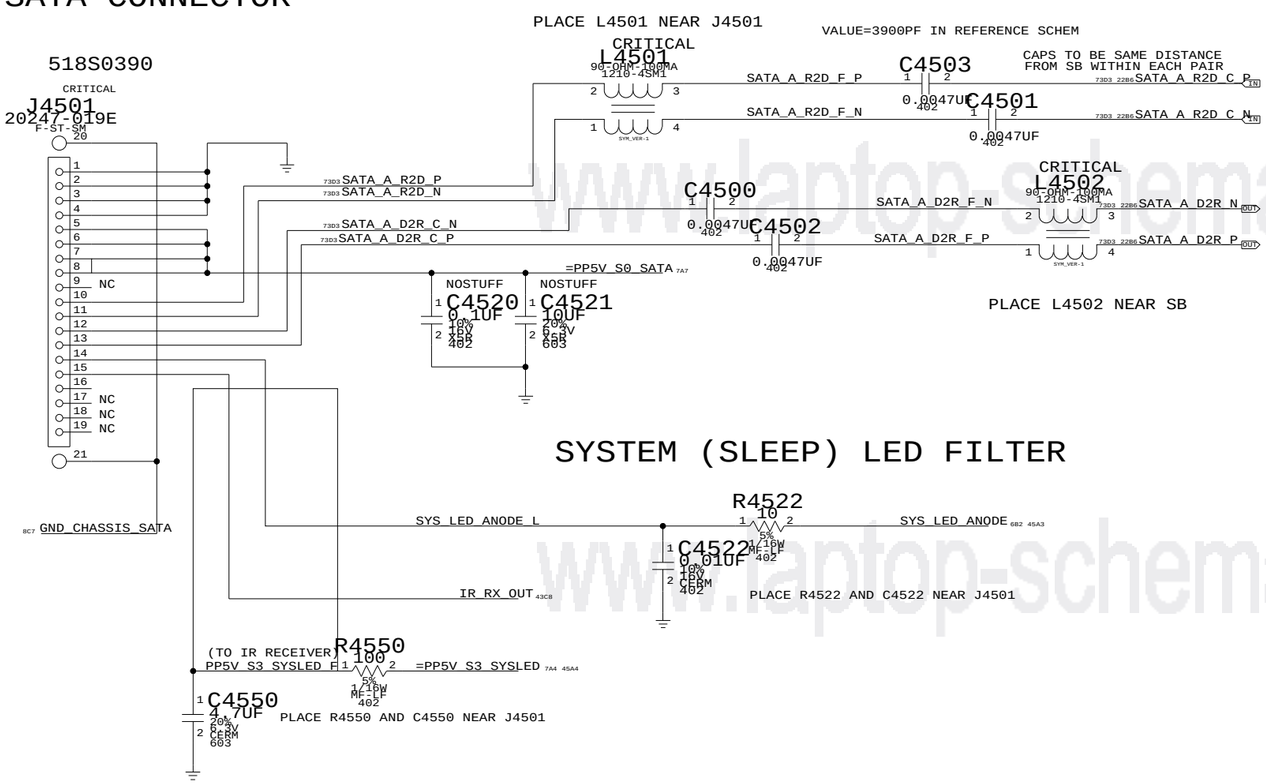
APPLE INC.

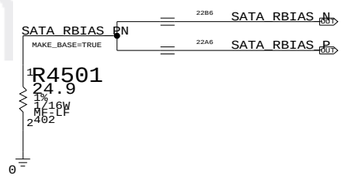
SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE NONE	SHT 44	OF 106

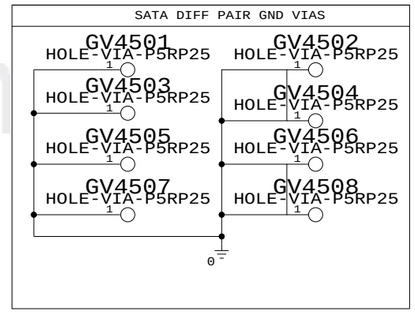
SATA CONNECTOR



SYSTEM (SLEEP) LED FILTER

PLACE NEAR ICH8 PIN





SATA CONNECTOR

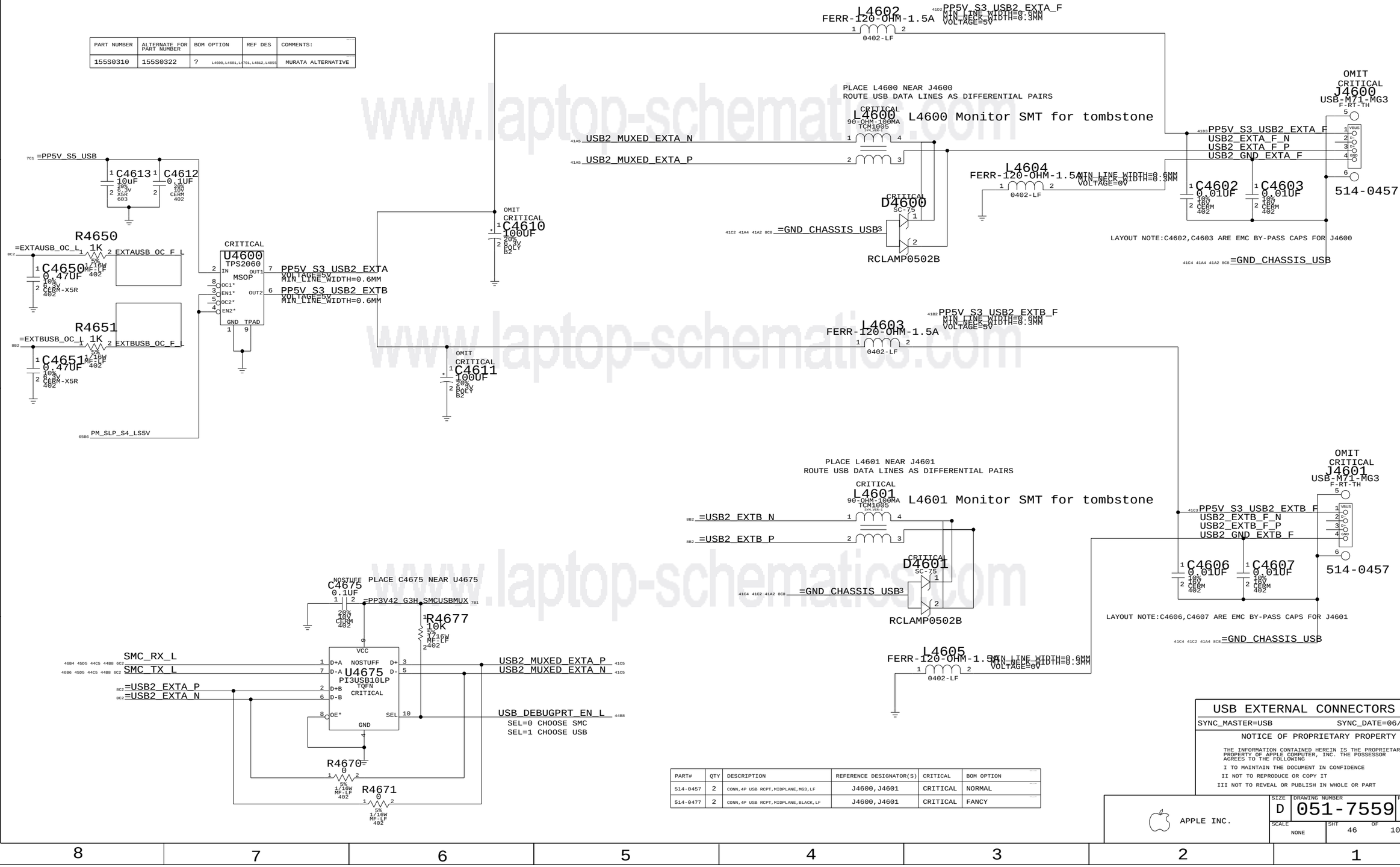
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	45	106

USB 2.0 CONNECTORS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0310	155S0322	?	L4600,L4601,L4701,L4812,L4855	MURATA ALTERNATIVE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0457	2	CONN,4P USB RCPT,MIDPLANE,MG3,LF	J4600,J4601	CRITICAL	NORMAL
514-0477	2	CONN,4P USB RCPT,MIDPLANE,BLACK,LF	J4600,J4601	CRITICAL	FANCY

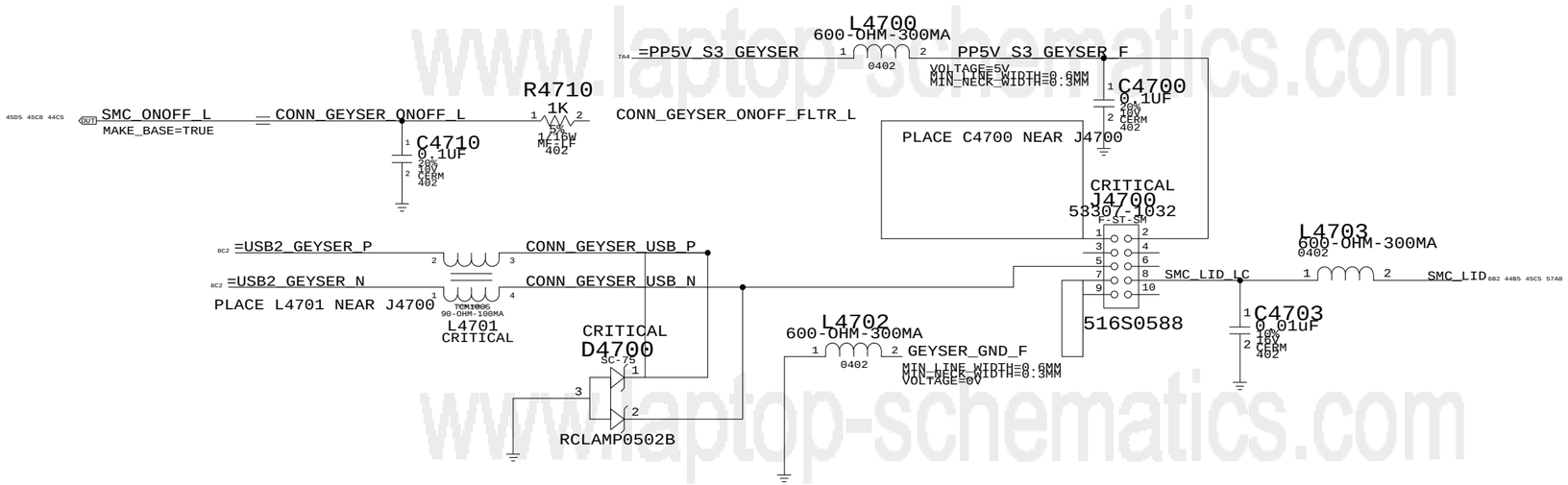
USB EXTERNAL CONNECTORS

SYNC_MASTER=USB SYNC_DATE=06/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 46 OF 106	

GEYSER AND DIMM0 REMOTE TEMP SENSORS



CONNECTOR MISC

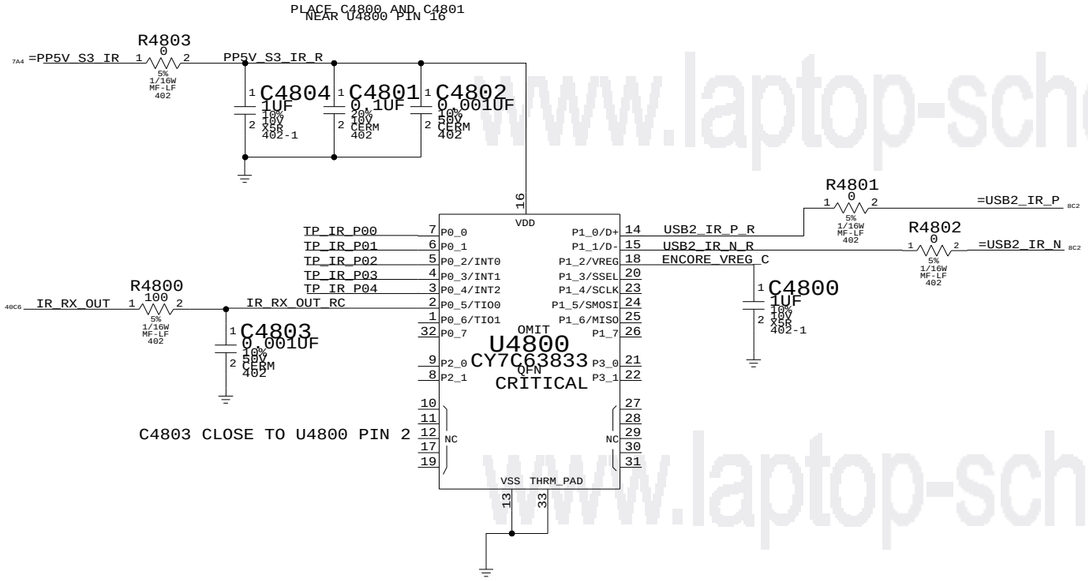
SYNC_MASTER=USB SYNC_DATE=06/29/2006

APPLE INC.

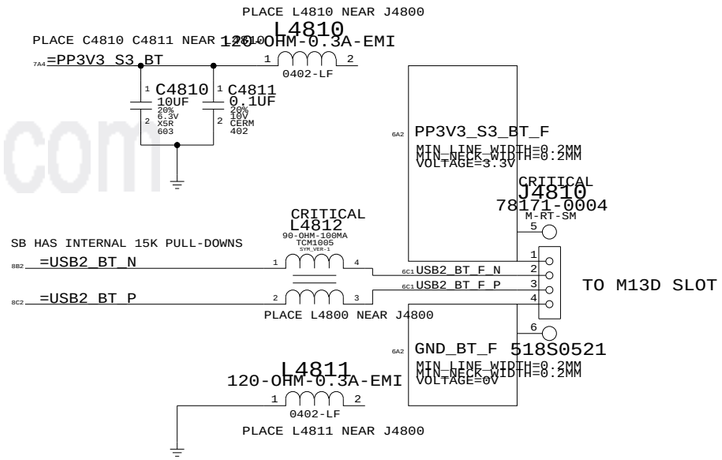
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	47	106

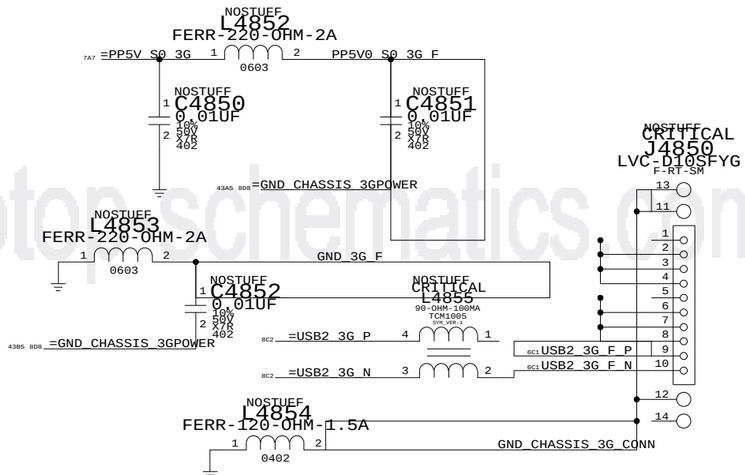
IR CYPRESS ENCORE II USB CONTROLLER



BLUETOOTH



3G CONNECTOR



IR CONTROLLER & BT INTERFACE

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	48	106

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

OMIT
U4900
SMC_H8S2116
BGA
(1 OF 4)

24C2	OUT	PM_LAN_ENABLE	B12	P10		
44A4	OUT	SMC_RSTGATE_L	C13	P11		
58A3 27A5 6B2	IN	ALL_SYS_PWRGD	A15	P12		
63B5 63B4 45D5	IN	RSMRST_PWRGD	B14	P13		
44B4		SMC_P14	B15	P14		
24C2	OUT	PM_RSMRST_L	C14	P15		
59C7	OUT	IMVP_VR_ON	D12	P16		
24C5	OUT	PM_PWRBTN_L	C15	P17		
44B4		SMC_P20	D13	P20		
44B4		SMC_P21	D14	P21		
44B4		SMC_P22	D15	P22		
44B4		SMC_P23	E12	P23		
66A3 45B6 6C1	OUT	SMC_BATT_TRICKLE_EN_L	E14	P24		
66A4 45B6 6C1	OUT	SMC_BATT_CHG_EN	E15	P25		
44B4		SMC_P26	E13	P26		
44B4		SMC_P27	E14	P27		
46C6 22D4 6D2	BI	LPC_AD<0>	D9	P30/LAD0		
46C6 22D4 6D2	BI	LPC_AD<1>	C9	P31/LAD1		
46C4 22D4 6C2	BI	LPC_AD<2>	A9	P32/LAD2		
46C4 22D4 6C2	BI	LPC_AD<3>	B9	P33/LAD3		
46B6 22D4 6C2	IN	LPC_FRAME_L	D8	P34/LFRAME*		
27C1	IN	SMC_LRESET_L	C8	P35/LRESET*		
75B3 29A5 29A3	IN	PCI_CLK33M_SMC	A8	P36/LCLK		
46B4 24C8 6C2	BI	INT_SERIRQ	D7	P37/SERIRQ		
44A4	OUT	SMC_GFX_THROTTLE_L	A5	P40/TMI0		
45A6	OUT	SMC_SYS_LED	B5	P41/TMO0		
47B3	BI	SMB_MGMT_DATA	(OC)	D5	P42/SDA1	
44B4		SMC_P43	C3	P43/TMI1/EXSCK1		
44B4		SMC_P44	B1	P44/TMO1		
44A4		SMC_P45	C2	P45		
44B4		SMC_P46	D3	P46/PWX0/PWM0		
44B4	OUT	SMC_SYS_KBDLED	C1	P47/PWX1/PWM1		
46B6 45D5 44C5 41A8 6C2	OUT	SMC_TX_L	G1	P50		
46B4 45D5 44C5 41A8 6C2	IN	SMC_RX_L	G4	P51		
47D6	BI	SMB_0_S0_CLK	(OC)	F2	P52/SCL0	

P60/KIN0*	L13	SMC_PM_G2_EN	OUT	65C6		
P61/KIN1*	L14	SMC_ADAPTER_EN	OUT	6C1 33C7 35C7 38C6 45B3 57C4		
P62/KIN2*	L15	SMC_P62		44B4		
P63/KIN3*	K12	SMC_P63		44B4		
P64/KIN4*	K13	SMC_P64		44B4		
P65/KIN5*	K14	PM_LAN_PWRGD	IN	45C5		
P66/IRQ6*/KIN6*	J12	SMC_PROCHOT_3_3_L	IN	45D1		
P67/IRQ7*/KIN7*	J13	SMC_P67		45C5		
P70/AN0	N12	SMC_CPU_ISENSE	IN	48C1 59C7		
P71/AN1	R13	SMC_CPU_VSENSE	IN	6B2 48B1		
P72/AN2	P13	SMC_GPU_ISENSE	IN	44A4		
P73/AN3	R14	SMC_GPU_VSENSE	IN	44A4		
P74/AN4	P14	SMC_DCIN_ISENSE	IN	66C2		
P75/AN5	R15	SMC_PBUS_VSENSE	IN	48D6		
P76/AN6	N13	SMC_BATT_ISENSE	IN	66B1		
P77/AN7	P15	SMC_NB_1V25_ISENSE	IN	45B3		
P80/PME*	C7	SMC_WAKE_SCI_L	OUT	24C8		
P81/GA20	A7	SMC_P81		44B4		
P82/CLKRUN*	B7	PM_CLKRUN_L	OUT	6C2 24C8 37A5 46B6		
P83/LPCPD*	D6	PM_SUS_STAT_L	IN	6C2 24D5 46B4		
P84/IRQ3*/TXD1	C6	SMC_TX_L	OUT	6C2 41A8 44B8 45D5 46B6		
P85/IRQ4*/RXD1	A6	SMC_RX_L	IN	6C2 41A8 44B8 45D5 46B4		
P86/IRQ5*/SCK1/SCL1	B6	(OC)	SMB_MGMT_CLK	BI	47B3	
P90/IRQ2*	K4	SMC_ONOFF_L	IN	42C8 45C8 45D5		
P91/IRQ1*	J2	SMC_BC_ACOK	IN	6C1 45B6 57C3 57C7 66A6		
P92/IRQ0*	J1	SMC_BS_ALRT_L	IN	6D1 45C5 57A2		
P93/IRQ12*	J3	PM_SLP_S3_L	IN	24D3 33C7 35C7 45A6 58B7 62B8		
P94/IRQ13*	J4	PM_S4_STATE_L	IN	24D3 33B7 65A6 65C4		
P95/IRQ14*	H2	PM_SLP_S5_L	IN	24D3 45C3		
P96/EXCL	H1	SMC_SUS_CLK	IN	45A7		
P97/IRQ15*/SDA0	G2	(OC)	SMB_0_S0_DATA	BI	47D6	

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(2 OF 4)

(DEBUG_SW_1)	45C5	SMC_PA0		R3	PA0/KIN8*/PA2DC	
(DEBUG_SW_2)	45C5	SMC_PA1		P3	PA1/KIN9*/PA2DD	
27C5 24D5	OUT	PM_SYSRST_L	(OC)	R2	PA2/KIN10*/PS2AC	
41A5	OUT	USB_DEBUGPRT_EN_L	(OC)	N3	PA3/KIN11*/PS2AD	
15B7 88Z	BI	PM_EXTTS_L<0>	(OC)	R1	PA4/KIN12*/PS2BC	
15B7 88Z	BI	PM_EXTTS_L<1>	(OC)	N2	PA5/KIN13*/PS2BD	
57C8 45D5 6C1	BI	SYS_ONEWIRE	(OC)	M4	PA6/KIN14*/PS2CC	
24C3 24A5	OUT	PM_BATLOW_L	(OC)	N1	PA7/KIN15*/PS2CD	
(DEBUG_SW_3)	45C5	SMC_PB0		B10	PB0/LSMI*	
24C8	OUT	SMC_RUNTIME_SCI_L		A10	PB1/LSCI	
39B2	IN	SMC_ODD_DETECT		D10	PB2	
48A8	OUT	ISENSE_CAL_EN		A11	PB3	
45C3	IN	SMC_EXCARD_CP		B11	PB4	
44B4	OUT	SMC_EXCARD_PWR_EN		C11	PB5	
45D5	IN	SMC_EXCARD_OC_L		A12	PB6	
45D5	IN	SMC_GFX_OVERTEMP_L		D11	PB7	
44B4	OUT	SMC_FAN_0_CTL		G14	PC0/TIOCA0/WUE8*	
50B4 6D2	OUT	SMC_FAN_1_CTL		G15	PC1/TIOCB0/WUE9*	
44B4	OUT	SMC_FAN_2_CTL		G13	PC2/TIOCC0/TCLKA/WUE10*	
44B4	OUT	SMC_FAN_3_CTL		G12	PC3/TIOCD0/TCLKB/WUE11*	
44B4	IN	SMC_FAN_0_TACH		H14	PC4/TIOCA1/WUE12*	
50C4 6D2	IN	SMC_FAN_1_TACH		H15	PC5/TIOCB1/TCLKC/WUE13*	
44B4	IN	SMC_FAN_2_TACH		H13	PC6/TIOCA2/WUE14*	
44A4 6A7	IN	SMC_FAN_3_TACH		H12	PC7/TIOCB2/TCLKD/WUE15*	
51C2	IN	SMS_X_AXIS		M11	PD0/AN8	
51C2	IN	SMS_Y_AXIS		P11	PD1/AN9	
51C2	IN	SMS_Z_AXIS		R11	PD2/AN10	
45C6	IN	SMC_ANALOG_ID		N11	PD3/AN11	
61C5	IN	SMC_NB_CORE_ISENSE		P10	PD4/AN12	
62C2	IN	SMC_NB_1V8_ISENSE		R10	PD5/AN13	
44A4	IN	ALS_LEFT		N10	PD6/AN14	
44A4	IN	ALS_RIGHT		M10	PD7/AN15	

PE0	M3	SMC_CASE_OPEN	IN	45B3		
PE1*/ETCK	M2	SMC_TCK	IN	6C2 45C5 46B4		
PE2*/ETDI	M1	SMC_TDI	IN	6C2 45C5 46B4		
PE3*/ETDO	L4	SMC_TDO	OUT	6C2 45C5 46B6		
PE4*/ETMS	L2	SMC_TMS	IN	6C2 45C5 46B6		
PF0/IRQ8*/PWM2	M7	SMC_PF0		44A4		
PF1/IRQ9*/PWM3	P6	SMC_PF1		44B4		
PF2/IRQ10*/TMOY	R6	SMC_LID	IN	6B2 42C3 45C5 57A8		
PF3/IRQ11*/TMOX	N6	SMC_PF3		45C1		
PF4/PWM4	M6	SMC_BATT_ISET	OUT	6C1 66A8		
PF5/PWM5	R5	SMC_BATT_VSET	OUT	44A4		
PF6/PWM6	P5	SMC_SYS_ISET	OUT	66B8		
PF7/PWM7	N5	SMC_SYS_VSET	OUT	44A4		
PG0/EXIRQ8*/TMIX	P9	SMC_PG0		45C5		
PG1/EXIRQ9*/TMIY	R9	SMC_SMS_INT	IN	51A8		
PG2/EXIRQ10*/SDA2	N9	(OC)	SMB_BSA_DATA	BI	47C3	
PG3/EXIRQ11*/SCL2	P8	(OC)	SMB_BSA_CLK	BI	47C3	
PG4/EXIRQ12*/EXSDAA	R8	(OC)	SMB_A_S3_DATA	BI	47D3	
PG5/EXIRQ13*/EXSCLA	M8	(OC)	SMB_A_S3_CLK	BI	47D3	
PG6/EXIRQ14*/EXSDAB	P7	(OC)	SMB_B_S0_DATA	BI	47C6	
PG7/EXIRQ15*/EXSCLB	R7	(OC)	SMB_B_S0_CLK	BI	47C6	
PH0/EXIRQ6*	E1	SMC_PROCHOT	OUT	45B6		
PH1/EXIRQ7*	F3	SMC_THRMTRIP	OUT	45B5		
PH2/FWE	K2	SMC_FWE	IN	45C5		
PH3/EXEXCL	C4	ALS_GAIN	OUT	44B4		
PH4	D4	SMC_PH4		44A4		
PH5	B3	SMC_ONOFF_L	OUT	51C7		

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

45C6 PP3V3_S5_AVREF_SMC
51B8 45D8 45D4 45C1 7C1 =PP3V42_G3H_SMC

C4902 22UF 20% 6.3V CERM 805
C4903 0.1UF 20% 10V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402
R4999 4.7 5% 1/16W MF-LF 402
PP3V3_S5_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
C4920 0.1UF 20% 10V CERM 402
PLACEMENT_NOTE=Place R4999 close to U4900 pins N14,N15
PLACEMENT_NOTE=Place C4920 close to U4900 pins N14,N15

PLACEMENT_NOTE=Place C4907 close to U4900 pin F1
SMC_VCL
C4907 0.47UF 10% 6.3V CERM-X5R 402

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AVCC	N14					
AVCC	N15					
VCC	P2					
VCC	P1					
VCC	J15					
VCC	A1					
VCL	F1					
AVREF	M14					
AVREF	M15					
		MD1	E2			SMC_MD1 IN 6C2 46B6
		MD2	K1			SMC_KBC_MDE
46B4 45D7 6C2	IN	SMC_RESET_L	E3	RES*		
45C7		SMC_XSTAL	A2	XTAL		
45C7		SMC_EXTAL	B2	EXTAL		
		NMI	F4			SMC_NMI IN 6C2 46B4
		ETRST*	L1			SMC_TRST_L IN 6C2 46B6
						NO STUFF
		AVSS	P12			
		VSS	R12			
		D1 P4 R4 F12 F13 B13 A13 A4 B4 D2				

R4909 10K 5% 1/16W MF-LF 402
R4901 10K 5% 1/16W MF-LF 402
R4902 10K 5% 1/16W MF-LF 402
R4998 10K 5% 1/16W MF-LF 402
R4903 0 5% 1/16W MF-LF 402
XW4900 SM
GND_SMC_AVSS 45B6 48A1 48B1 48C1 48C6 60B2 61C5 62C2 66B1 66C2

44D8	SMC_P14	MAKE_BASE=TRUE	NC_SMC_P14	
44C8	SMC_P20	MAKE_BASE=TRUE	NC_SMC_P20	
44C8	SMC_P21	MAKE_BASE=TRUE	NC_SMC_P21	
44C8	SMC_P22	MAKE_BASE=TRUE	NC_SMC_P22	
44C8	SMC_P23	MAKE_BASE=TRUE	NC_SMC_P23	
44C8	SMC_P26	MAKE_BASE=TRUE	NC_SMC_P26	
44C8	SMC_P27	MAKE_BASE=TRUE	NC_SMC_P27	
44B8	SMC_P46	MAKE_BASE=TRUE	NC_SMC_P46	
44C8	SMC_P44	MAKE_BASE=TRUE	NC_SMC_P44	
44C8	SMC_P43	MAKE_BASE=TRUE	NC_SMC_P43	
44D5	SMC_P62	MAKE_BASE=TRUE	NC_SMC_P62	
44D5	SMC_P63	MAKE_BASE=TRUE	NC_SMC_P63	
44D5	SMC_P64	MAKE_BASE=TRUE	NC_SMC_P64	
44C5	SMC_P81	MAKE_BASE=TRUE	NC_SMC_P81	
44B5	SMC_PF1	MAKE_BASE=TRUE	NC_SMC_PF1	
44B8	SMC_SYS_KBDLED	MAKE_BASE=TRUE	NC_SMC_SYS_KBDLED	
44A5	ALS_GAIN	MAKE_BASE=TRUE	NC_ALS_GAIN	
44B8	SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	NC_SMC_EXCARD_PWR_EN	
44A8	SMC_FAN_0_CTL	MAKE_BASE=TRUE	NC_SMC_FAN_0_CTL	
44A8	SMC_FAN_2_CTL	MAKE_BASE=TRUE	NC_SMC_FAN_2_CTL	
44A8	SMC_FAN_3_CTL	MAKE_BASE=TRUE	NC_SMC_FAN_3_CTL	
44A8	SMC_FAN_0_TACH	MAKE_BASE=TRUE	NC_SMC_FAN_0_TACH	
44A8	SMC_FAN_2_TACH	MAKE_BASE=TRUE	NC_SMC_FAN_2_TACH	
44A8 6A7	SMC_FAN_3_TACH	MAKE_BASE=TRUE	NC_SMC_FAN_3_TACH	
44A8	ALS_LEFT	MAKE_BASE=TRUE	NC_ALS_LEFT	
44A8	ALS_RIGHT	MAKE_BASE=TRUE	NC_ALS_RIGHT	
44B5	SMC_PF0	MAKE_BASE=TRUE	NC_SMC_PF0	
44B5	SMC_BATT_VSET	MAKE_BASE=TRUE	NC_SMC_BATT_VSET	
44B5	SMC_SYS_VSET	MAKE_BASE=TRUE	NC_SMC_SYS_VSET	
44D8	SMC_RSTGATE_L	MAKE_BASE=TRUE	NC_SMC_RSTGATE_L	
44C8	SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	NC_SMC_GFX_THROTTLE_L	
44C5	SMC_GPU_ISENSE	MAKE_BASE=TRUE	SMC_GPU1_ISENSE	60B2 60C7
44C5	SMC_GPU_VSENSE	MAKE_BASE=TRUE	SMC_GPU1_VSENSE	48B1
44C8	SMC_P45	MAKE_BASE=TRUE	SMC_ENRGYSTR_LDO_EN	66D3
44A5	SMC_PH4	MAKE_BASE=TRUE	SMC_ENRGYSTR_LDO_PGOOD	

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U4900
SMC_H8S2116
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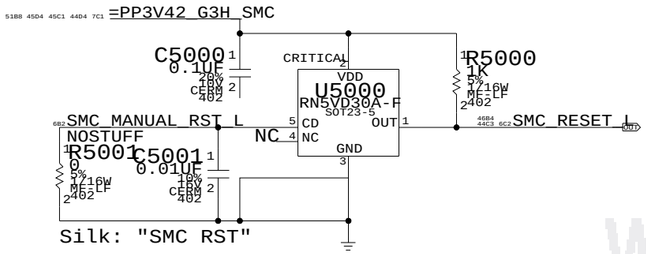
NC	G3	NC0		NC12	F15	NC
NC	H3	NC1		NC13	A14	NC
NC	K3	NC2		NC14	C12	NC
NC	L3	NC3		NC15	C10	NC
NC	N4	NC4		NC16	C5	NC
NC	M5	NC5		NC17	A3	NC
NC	N7	NC6		NC18	B8	NC
NC	M12	NC7		NC19	E4	NC
NC	M13	NC8		NC20	H4	NC
NC	L12	NC9		NC21	M9	NC
NC	K15	NC10		NC22	N8	NC
NC	J14	NC11				

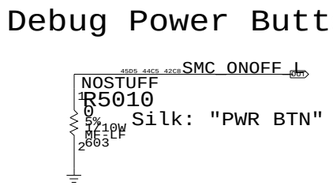
SMC
45C5 66C1
SYNC_MASTER=T9_MLB
SYNC_DATE=10/30/2006

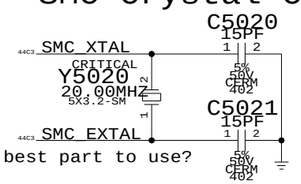
APPLE INC.

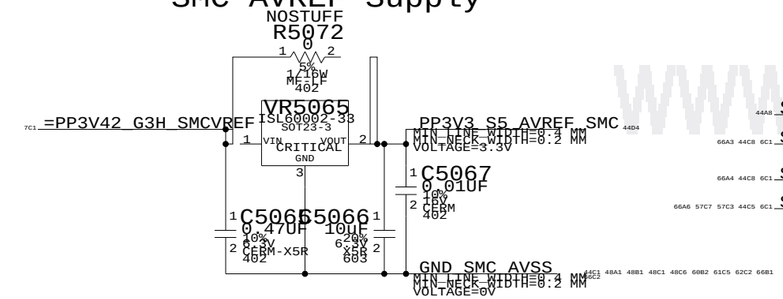
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE
SHT 49 OF 106

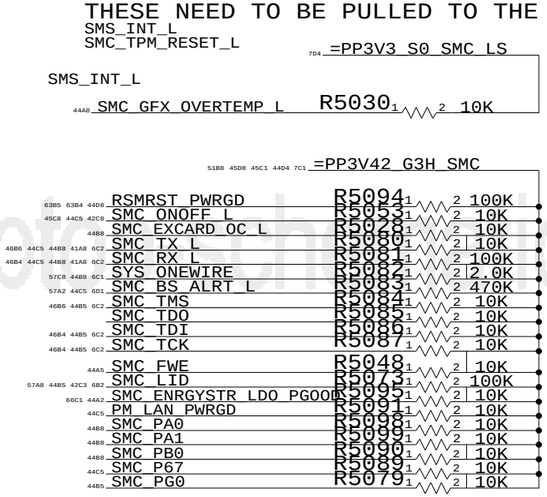


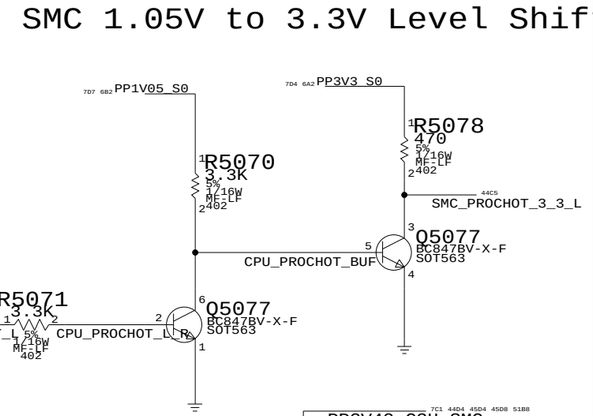


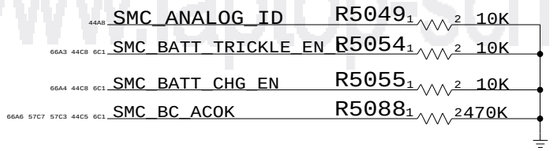


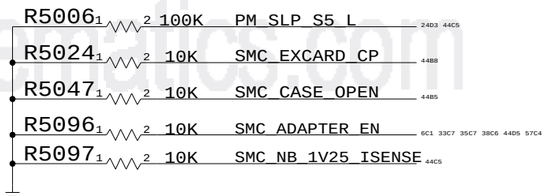


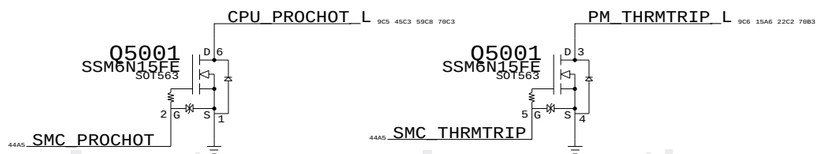
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1278	353S1381	?	VR5065	TI REF3133

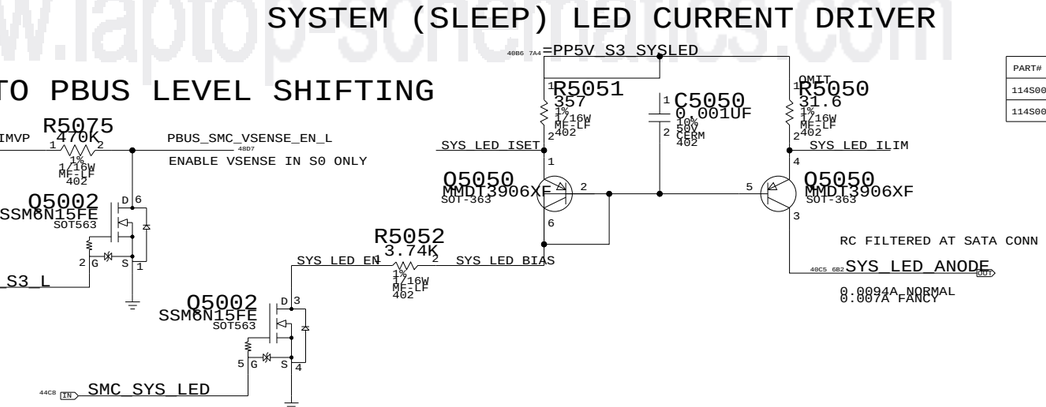












PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0071	1	31.6, 1%, 1/16W, MF-LF, 402	R5050	NORMAL
114S0086	1	44.2, 1%, 1/16W, MF-LF, 402	R5050	FANCY

SMC SUPPORT

SYNC_MASTER=GPU SYNC_DATE=07/17/2006

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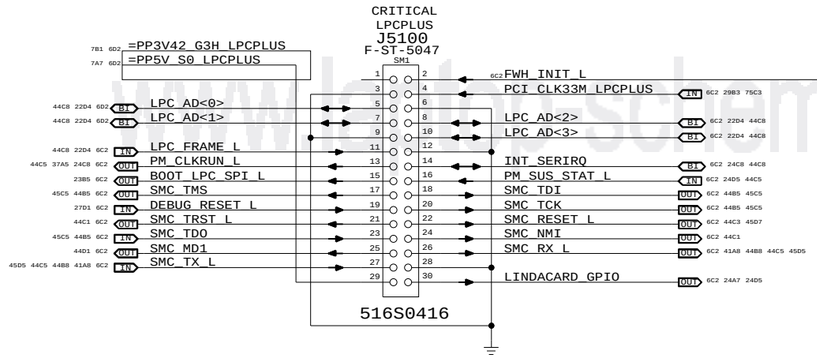
APPLE INC.

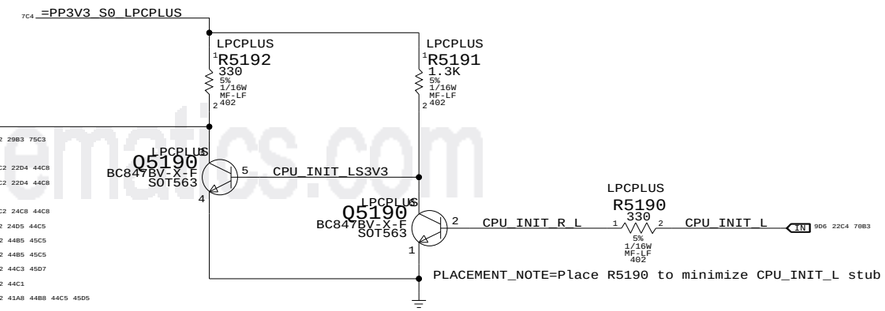
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	50	106

LPC+ Connector



FWH_INIT_L Generation



LPC+ Debug Connector

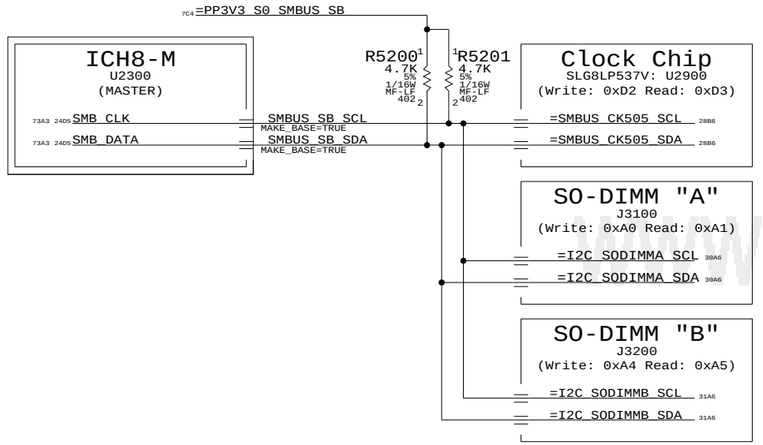
SYNC_MASTER=WFERRY SYNC_DATE=06/01/2006

APPLE INC.

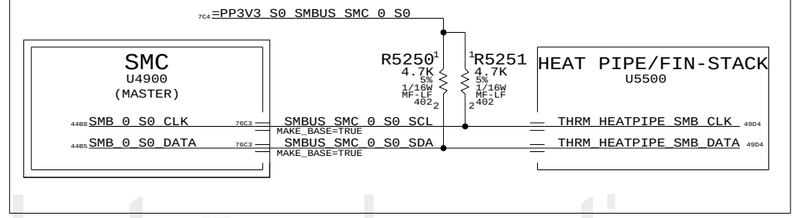
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	51	106

ICH8-M SMBus Connections

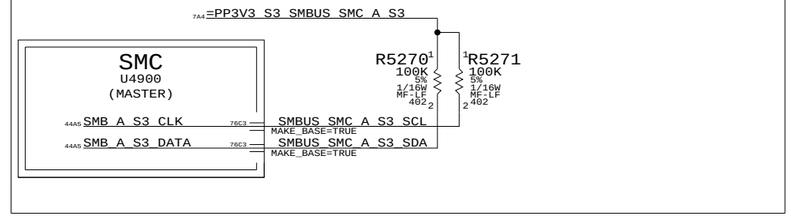


SMC "0" SMBus Connections

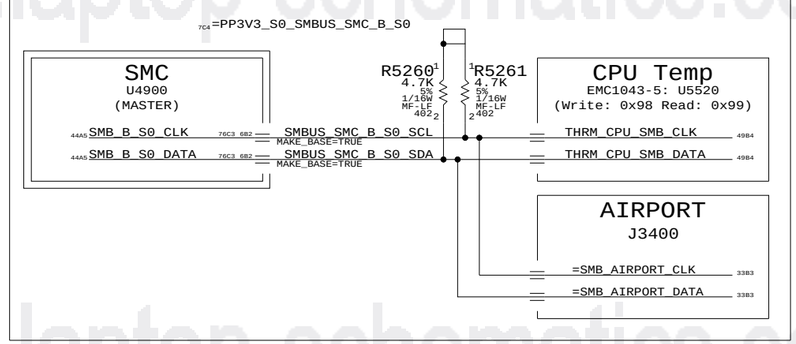


SMC "A" SMBus Connections

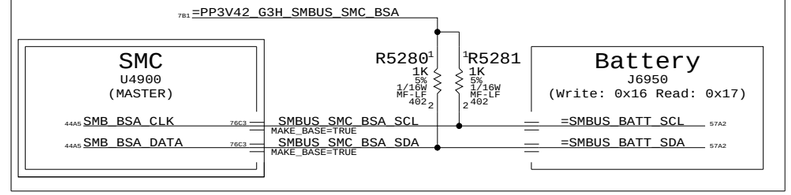
NOTE: SMC RMT bus remains powered and may be active in S3 state



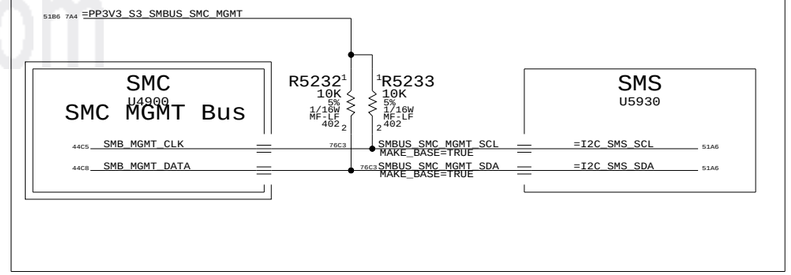
SMC "B" SMBus Connections



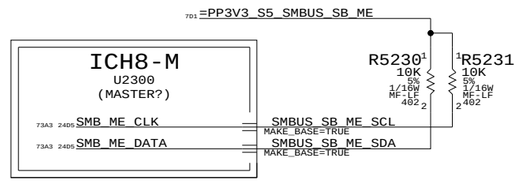
SMC "Battery A" SMBus Connections



SMC "MANAGEMENT" SMBUS CONNECTIONS



ICH8-M ME SMBus Connections



SMBUS CONNECTIONS

SYNC_MASTER=WFERRY SYNC_DATE=06/01/2006

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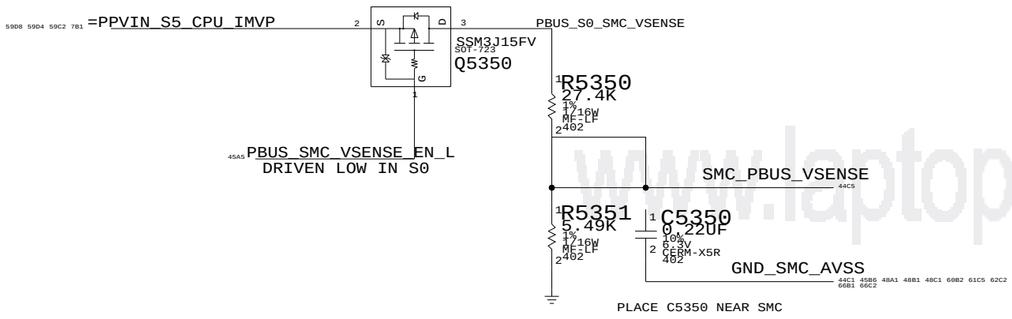
APPLE INC.

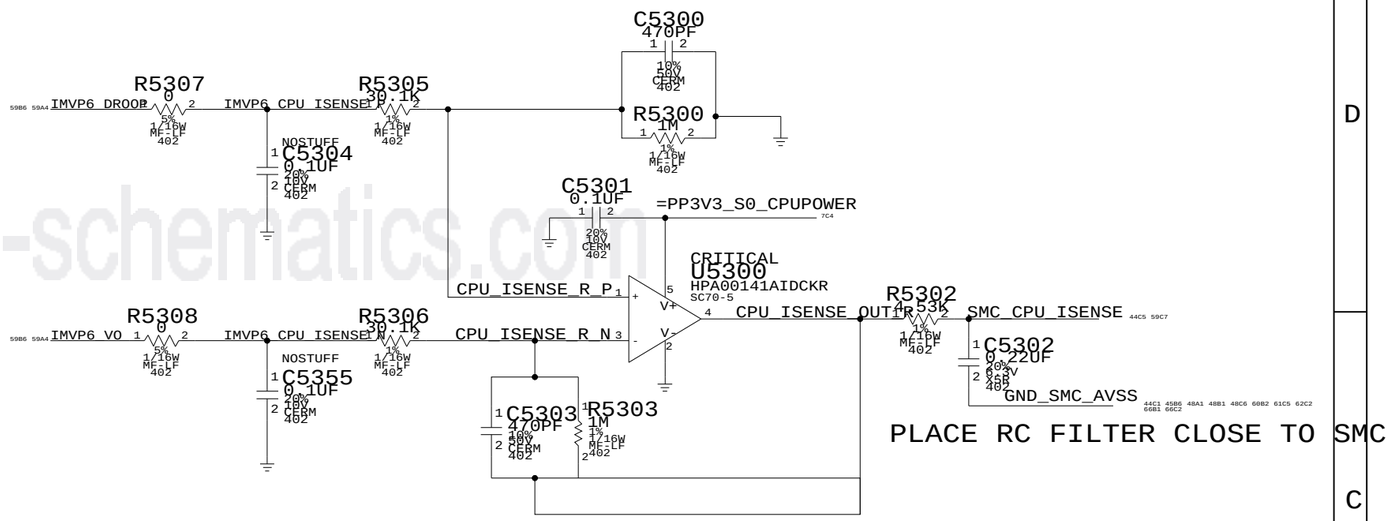
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE SHT 52 OF 106

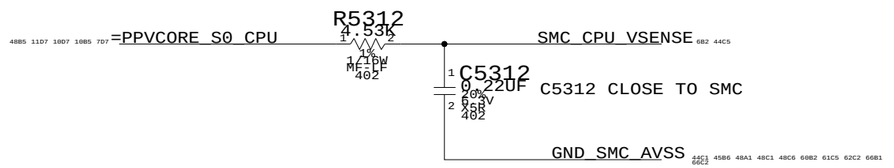
PROCESSOR DCIN VOLTAGE SENSE



CPU CURRENT SENSE

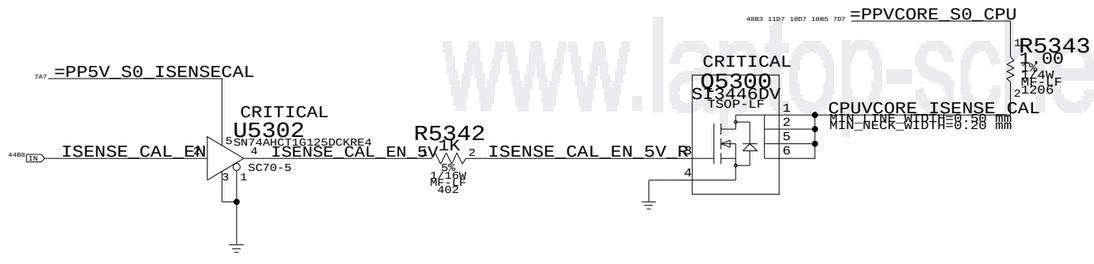


CPU VOLTAGE SENSE

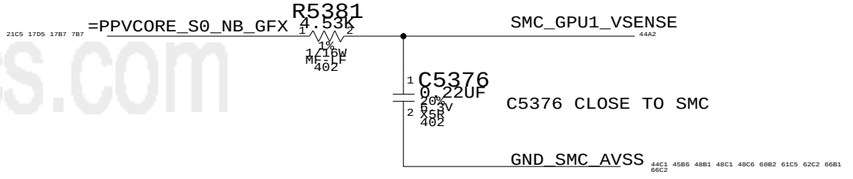


Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



GPU VOLTAGE SENSE



CPU Current & Voltage Sense

SYNC_MASTER=GPU SYNC_DATE=07/17/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 53 OF 106

HEAT-PIPE/FIN-STACK TEMPERATURE ZONE

CRITICAL
J5550
78171-0004
M-RT-SM
518S0521

CONNECTOR DRIVES TWO TEMP DIODE JUNCTIONS

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GAURD

6A1 THRM_HEATPIPE_P
PLACE C5510 NEXT TO U5500
C5510 0.0022UF 10% 50V CERM 402
6A1 THRM_HEATPIPE_N

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GAURD

6A1 THRM_FINSTACK_P
C5511 0.0022UF 10% 50V CERM 402 PLACE C5511 NEXT TO U5500
6A1 THRM_FINSTACK_N

CRITICAL
U5500
EMC1043-5
MSOP
PP3V3_S0_THRM_HEATPIPE_F
PLACE C5501 NEXT TO U5500 VDD
C5501 0.1UF 10% 16V X5R 402
C5502 1UF 10% 6.3V CERM 402
R5501 33 5% 1/16W MF-LF 402 =PP3V3_S0_THRM_SNR 7C4 49C2
PLACE C5501 NEAR U5500 VDD
VDD DP1 DN1 DP2 DN2 GND SMCLK SMDATA
47D3 THRM_HEATPIPE_SMB_CLK TO
47D3 THRM_HEATPIPE_SMB DATA TO
ADDR= 1001 100B

(WRITE: 0X98 READ: 0X99)

LAYOUT NOTE:
ADD GND GUARD TRACE FOR CPU_THERMD_P AND CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND CPU_THERMD_N ON SAME LAYER.
10 MIL TRACE
10 MIL SPACING

CPU TEMPERATURE ZONE

OUT 9C6 CPU_THERMD_P
C5520 0.0022UF 10% 50V CERM 402
(TO CPU INTERNAL THERMAL DIODE)
IN 9C6 CPU_THERMD_N

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GAURD

6A1 THRM_DIMM_DX_F_P
R5522 10 1% 1/16W MF-LF 402
THRM_DIMM_DX_P
THRM_DIMM_DX_N
C5521 0.0022UF 10% 50V CERM 402
CRITICAL
Q5520
BC846BM3T5G
SOT732-3
PLACE UNDER J3101
NOSTUFF
C5524 0.0022UF 10% 50V CERM 402 PLACE C5524 NEXT TO Q5520
R5523 10 1% 1/16W MF-LF 402
6A1 THRM_DIMM_DX_F_N

1. ROUTE DXP AND DXN DIFFERENTIALLY
2. ROUTE GROUNDED GAURD TRACES AROUND THE DXP/DXN DIFF PAIR
3. 10 MIL TRACE WIDTHS AND 10MIL SPACING BETWEEN THE GAURD

CRITICAL
U5520
EMC1043-5
MSOP
PP3V3_S0_THRM_CPU_F
C5522 0.1UF 10% 16V X5R 402
C5523 1UF 10% 6.3V CERM 402
R5524 33 5% 1/16W MF-LF 402 =PP3V3_S0_THRM_SNR 7C4 49D2
PLACE C5522 NEAR U5520 VDD
VDD DP1 DN1 DP2 DN2 GND SMCLK SMDATA
47C3 THRM_CPU_SMB_CLK TO
47C3 THRM_CPU_SMB_DATA TO
ADDR= 1001 100B

(Write: 0x98 Read: 0x99)

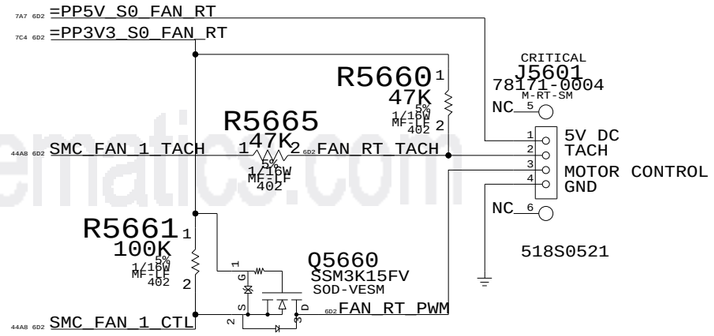
TEMPERATURE SENSE

SYNC_MASTER=GPU SYNC_DATE=06/21/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE SHT 55 OF 106



Fan

SYNC_MASTER=ENES SYNC_DATE=11/10/2005

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	56	106

PAGE NOTES

INPUT

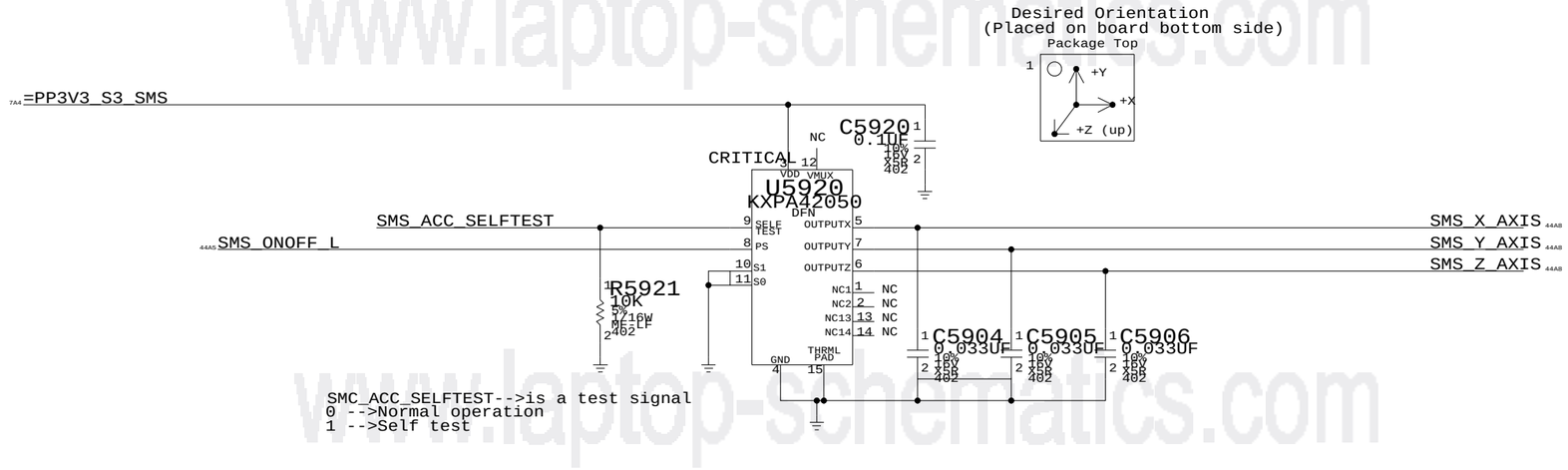
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

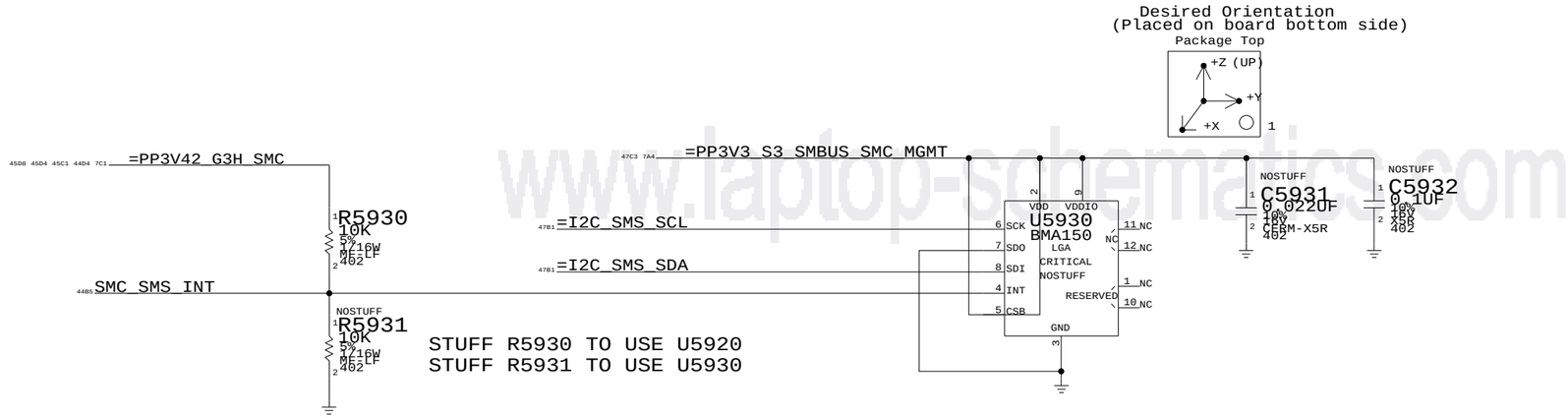
OUTPUT

SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION_OE PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -





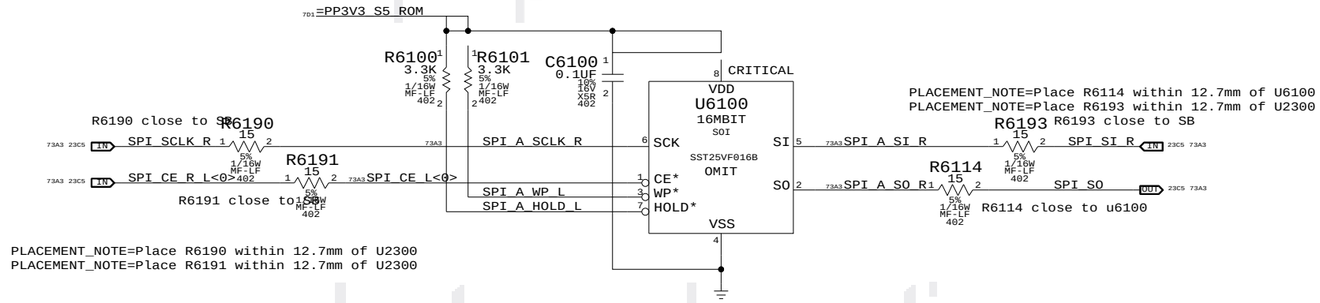
SMS

SYNC_MASTER=SMC SYNC_DATE=08/23/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	59	106



SPI ROMs

SYNC_MASTER=WFERRY SYNC_DATE=04/26/2006

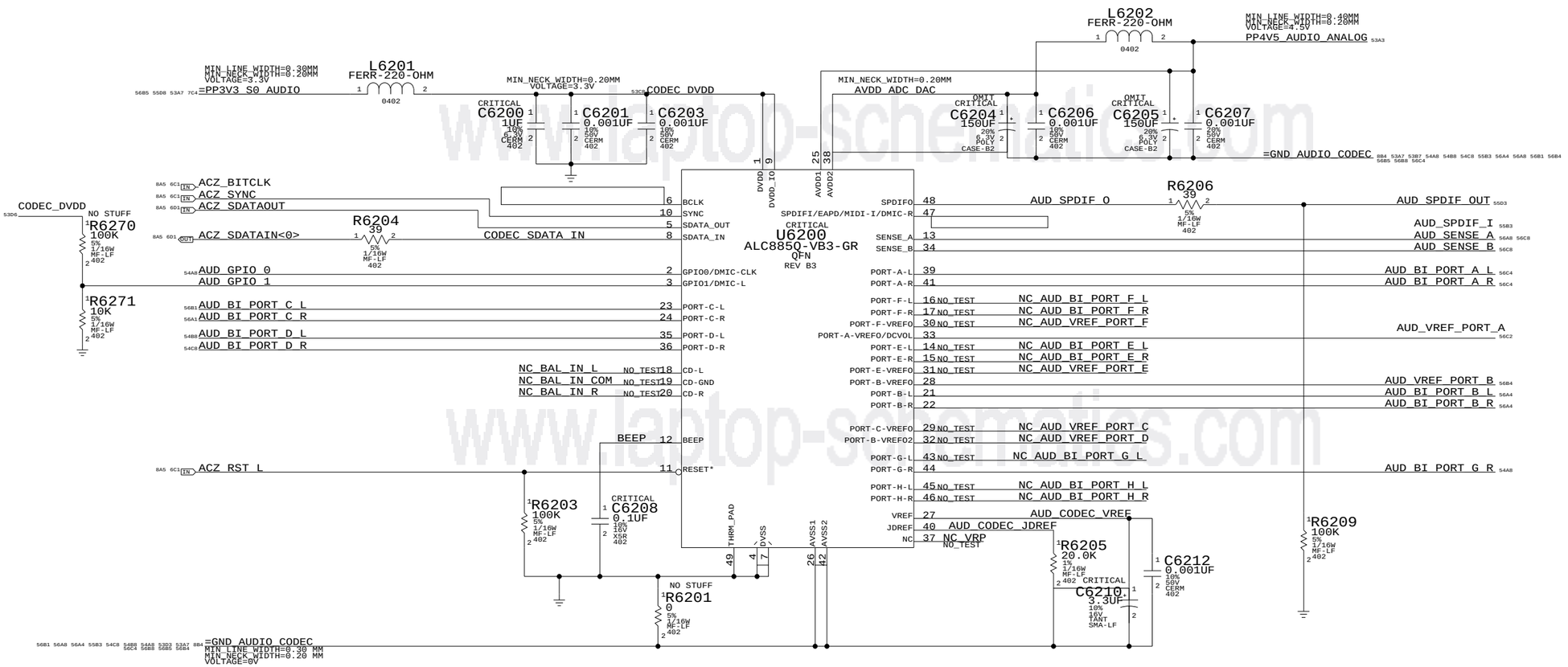
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	61	106

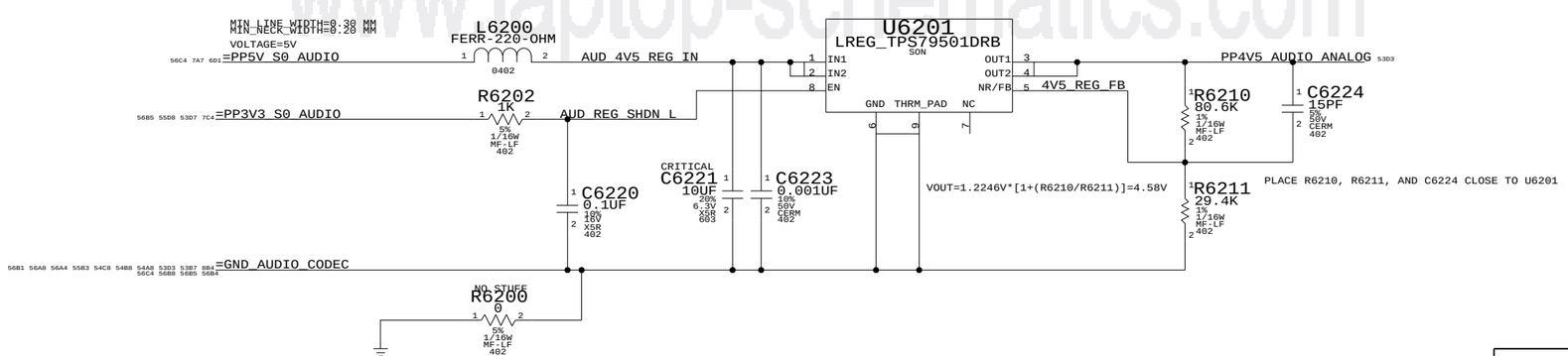
AUDIO CODEC

APPLE P/N 353S1538



AUDIO 4.5V REGULATOR

APPLE P/N 353S1576



AUDIO: CODEC

SYNC_MASTER=M70AUDIO

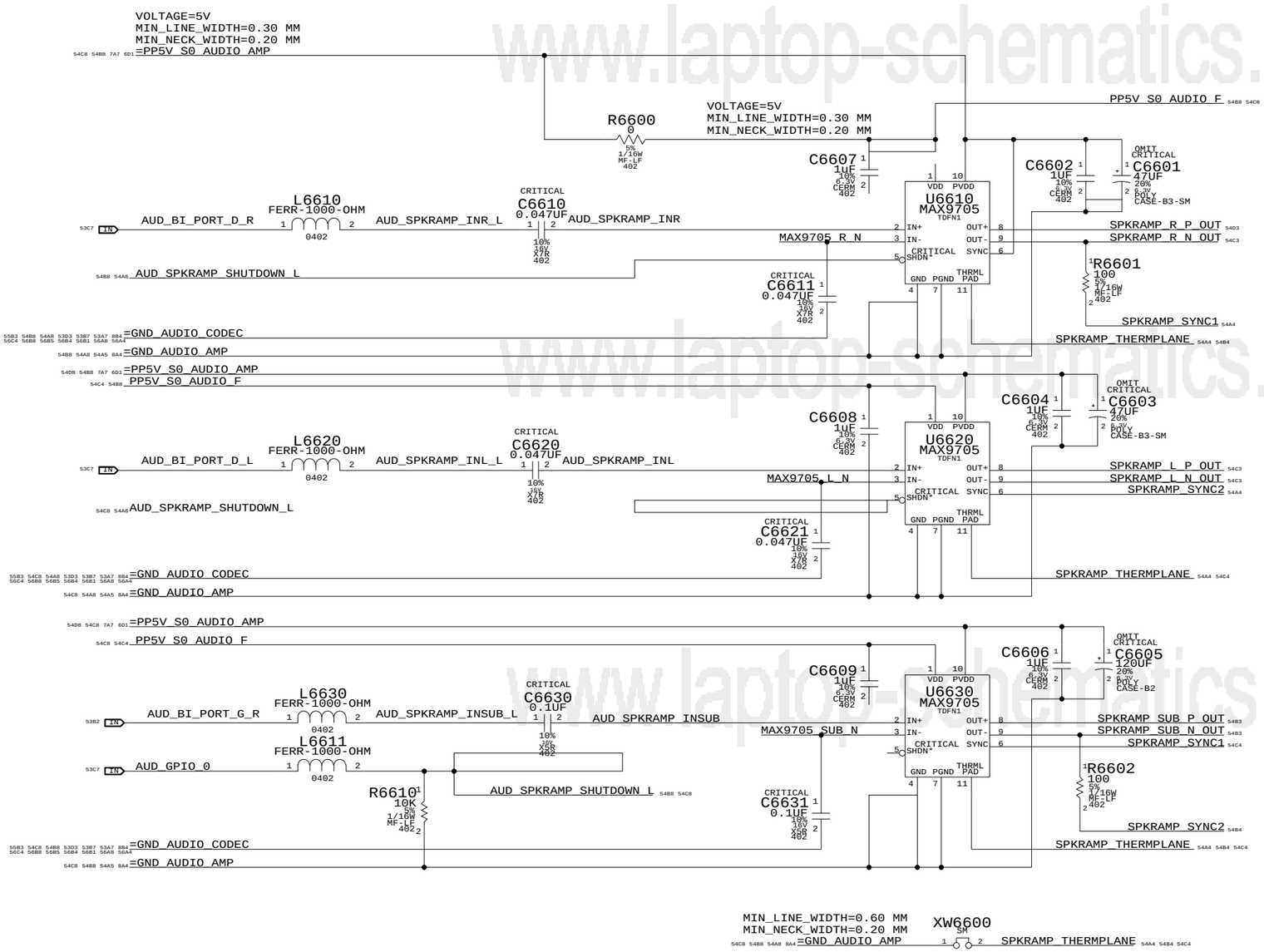
APPLE INC.

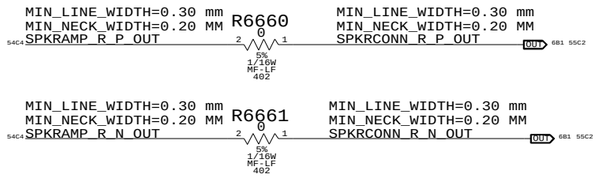
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	62	106

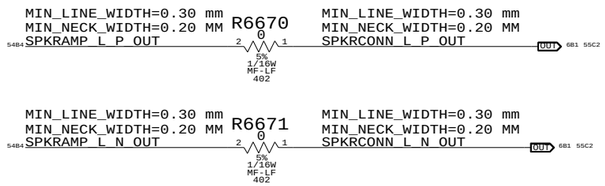
SATELLITE & SUB TWEETER AMPLIFIER APN:353S1595

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	12DB

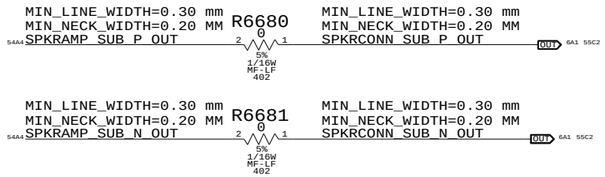




RIGHT SATELLITE



LEFT SATELLITE



SUB-TWEETER

AUDIO: SPEAKER AMP

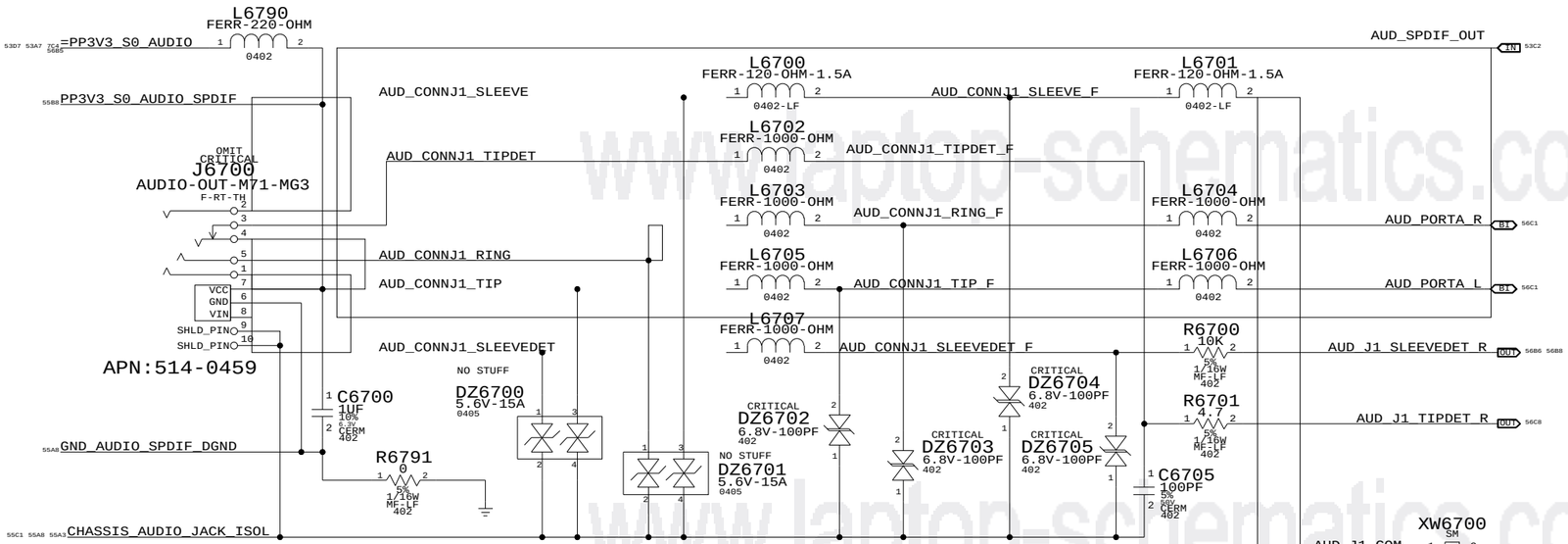
SYNC_MASTER=M70AUDIO SYNC_DATE=03/12/2007

APPLE INC.

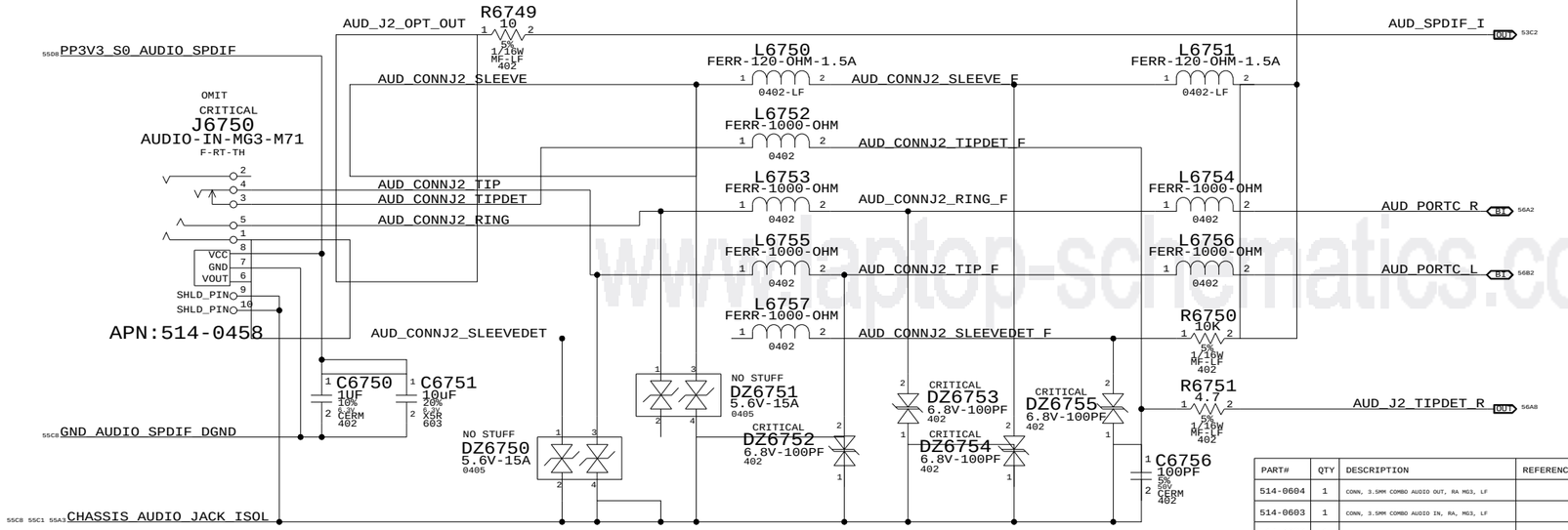
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	66	106

AUDIO JACK 1: LO/HP CONNECTOR, SPDIF TX

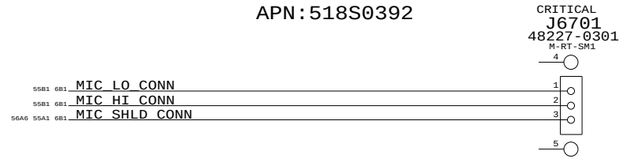


AUDIO JACK 2: LINE IN CONNECTOR, SPDIF RX



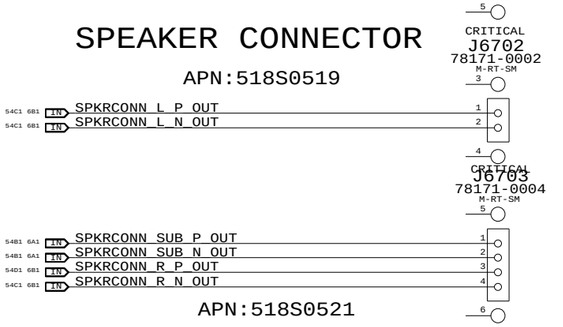
MIC CONNECTOR

APN:518S0392



SPEAKER CONNECTOR

APN:518S0519

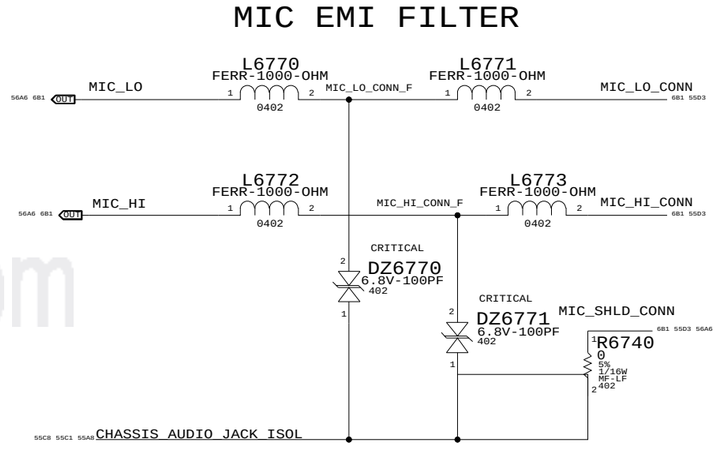


APN:518S0521

XW6705

=GND_CHASSIS_AUDIO_JACK
CHASSIS_AUDIO_JACK_ISOL

MIC EMI FILTER



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0604	1	CONN, 3.5MM COMBO AUDIO OUT, RA MG3, LF	J6700	CRITICAL	NORMAL
514-0603	1	CONN, 3.5MM COMBO AUDIO IN, RA, MG3, LF	J6750	CRITICAL	NORMAL
514-0602	1	CONN, 3.5MM COMBO AUDIO OUT, RA, BLACK, LF	J6700	CRITICAL	FANCY
514-0601	1	CONN, 3.5MM COMBO AUDIO IN, RA, BLACK, LF	J6750	CRITICAL	FANCY

AUDIO: JACK

SYNC_MASTER=M70AUDIO SYNC_DATE=03/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	67	106

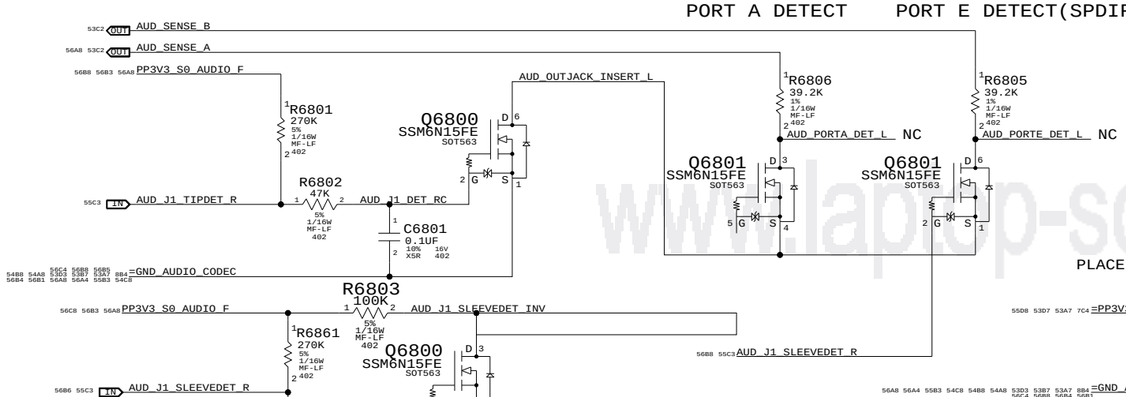
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP OUT	0X0F (15)	0X05 (5)	0X15 (21,PORTA)	VREF_A(100%)	0X15 (21,PORTA)
SAT SPKR	0X26 (38)	0X25 (37)	0X14 (20,PORTD)	GPIO 0	N/A
SUB SPKR	0X0E (14)	0X04 (4)	0X16 (22,PORTG)	GPIO 0	N/A
SPDIF OUT	N/A	0X06 (6)	0X1E (30,SPDIF OUT)	N/A	0X1B (27,PORTE)

CODEC INPUT SIGNAL PATHS

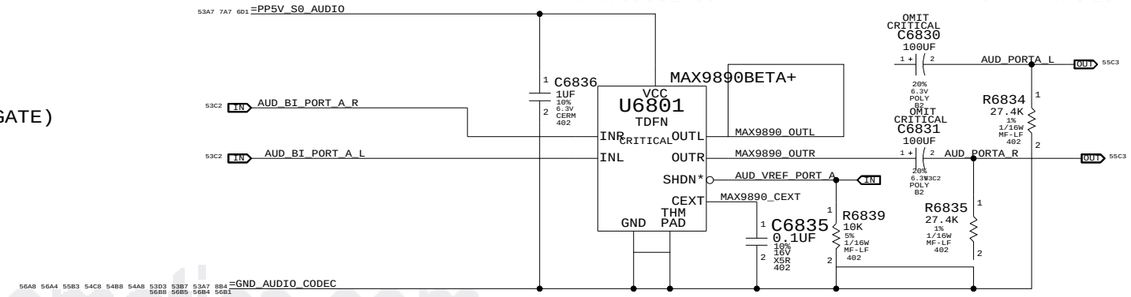
FUNCTION	MIXER	VOLUME	MUTE CONTROL	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X08 (8)	0X08 (8)	0X1A (26,PORTC)	N/A	0X1A (26,PORTC)
MIC IN	0X24 (36)	0X07 (7)	0X07 (7)	0X07 (7)	0X18 (24,PORTB)	VREF_B (80%)	N/A
SPDIF IN	N/A	N/A	N/A	0X0A (10)	0X1F (31,SPDIF IN)	N/A	N/A

PORT A DETECT PORT E DETECT(SPDIF DELEGATE)

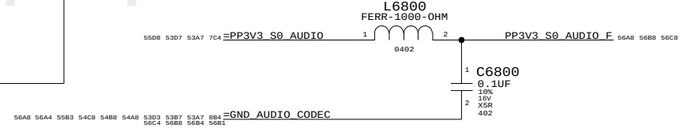


HP/LO DE-POP SWITCH
APN:353S1459

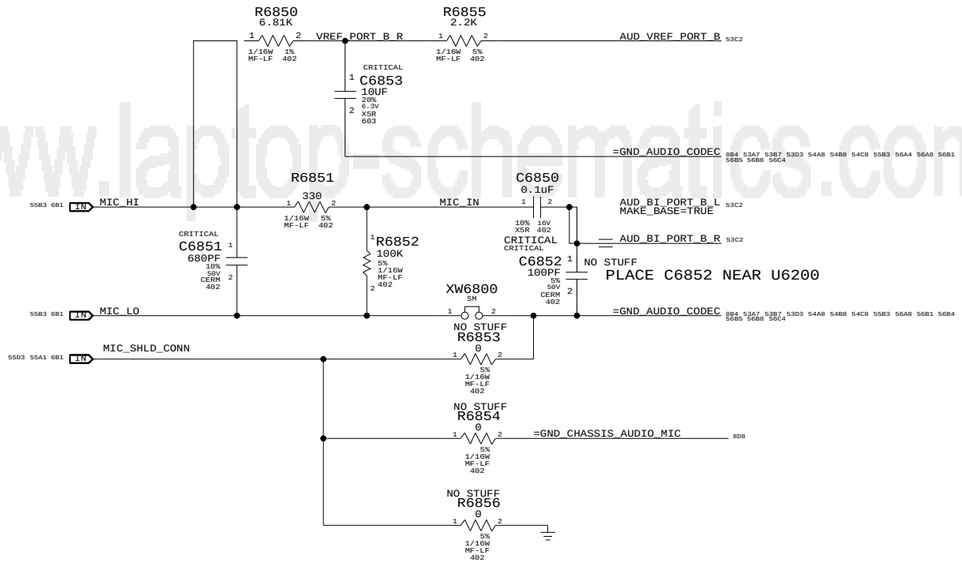
PORT A HP/LO



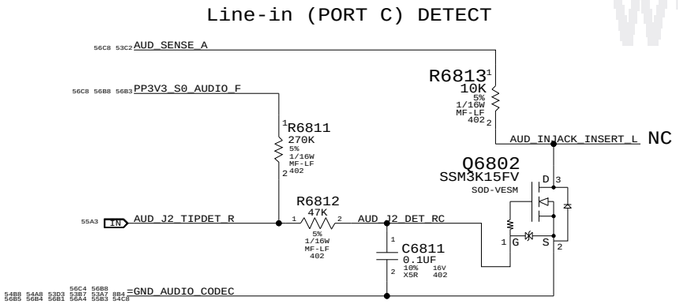
PLACE L6800/C6800 CLOSE TO Q6800



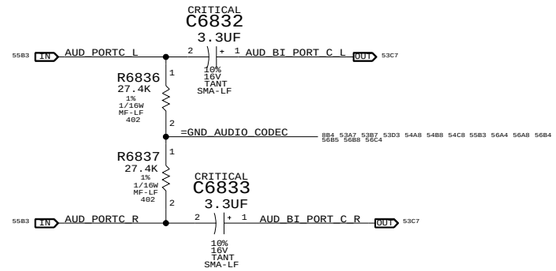
MIC INPUT CIRCUITRY



Line-in (PORT C) DETECT



PORT C LI



AUDIO: JACK TRANSLATORS

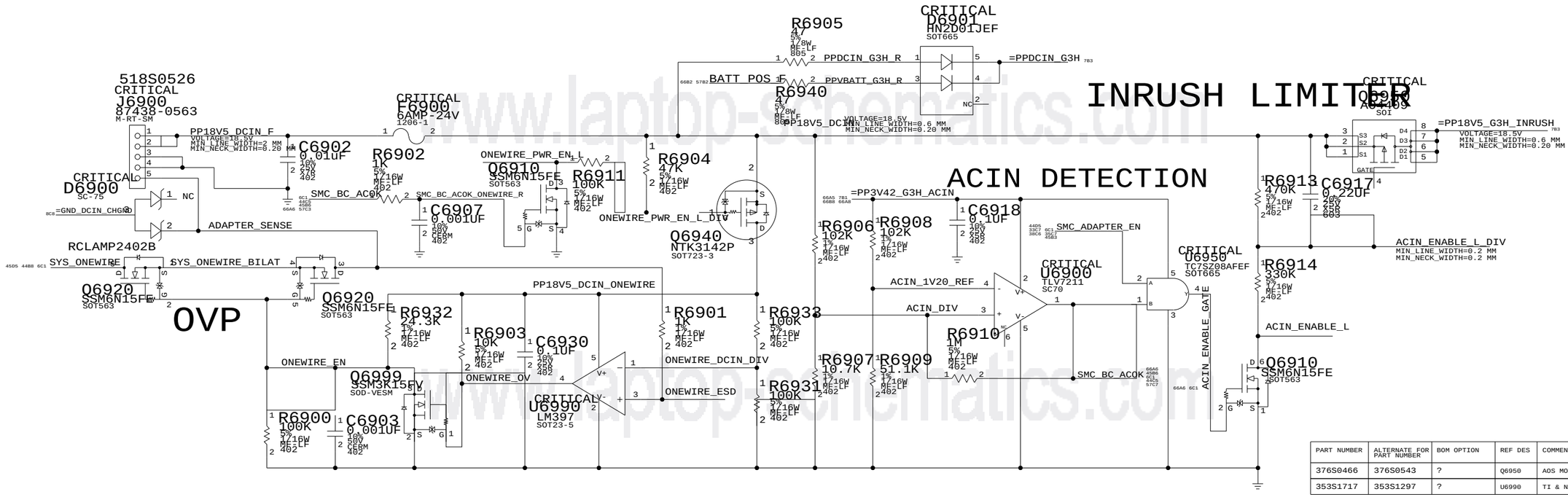
SYNC_MASTER=M70AUDIO SYNC_DATE=03/12/2007

APPLE INC.

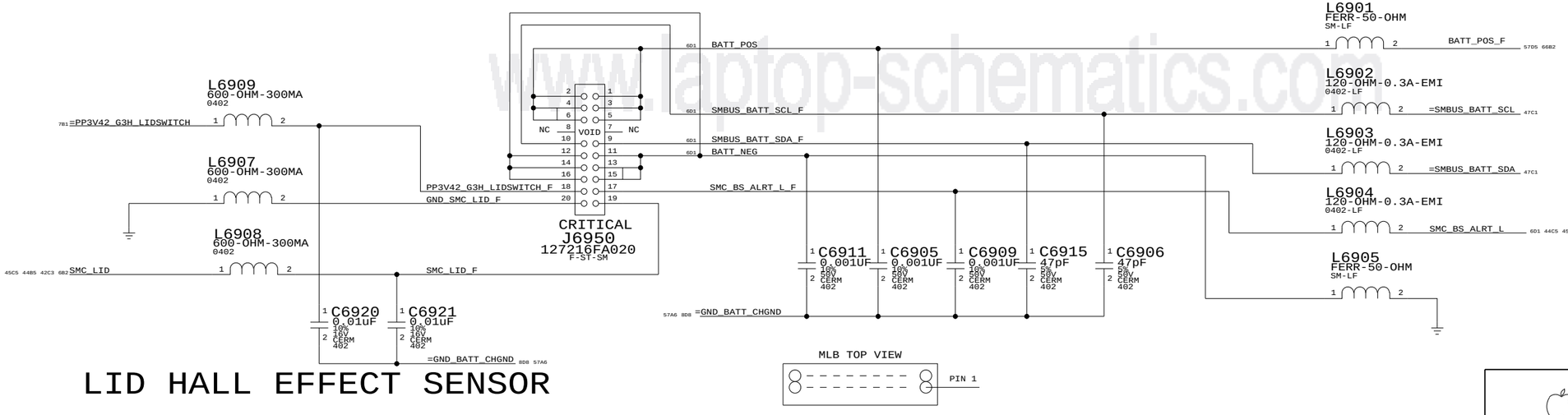
SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE SHT 68 OF 106

DC-JACK INTERFACE



BATTERY INTERFACE



LID HALL EFFECT SENSOR

DC-In & Battery Connectors

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE

SHT 69 OF 106

S0 FETS & POWER SEQUENCING

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q7000	

5V S0 FET

MOSFET	FDM6296
CHANNEL	N-TYPE
RDS(ON)	15 mOhm @4.5V
LOADING	4.348 A

3.3V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	1.810 A

1.8V S0 FET

MOSFET	FDC655BN
CHANNEL	N-TYPE
RDS(ON)	33 mOhm @4.5V
LOADING	0.260 A

1.05V S0 RUN/SS CONTROL

1.25V S0 RUN/SS CONTROL

1.5V S0 RUN/SS CONTROL

DEASSERTED 160MS
AFTER UVLO_D VALID

~26MS

MAKEBASE=TRUE
U7002.3 has int 90K pull-up

LATEST ISSUE: 2007/01/02

S0 FETS & Power Sequencing
SYNC_MASTER=DSIMON-WF SYNC_DATE=05/31/2006

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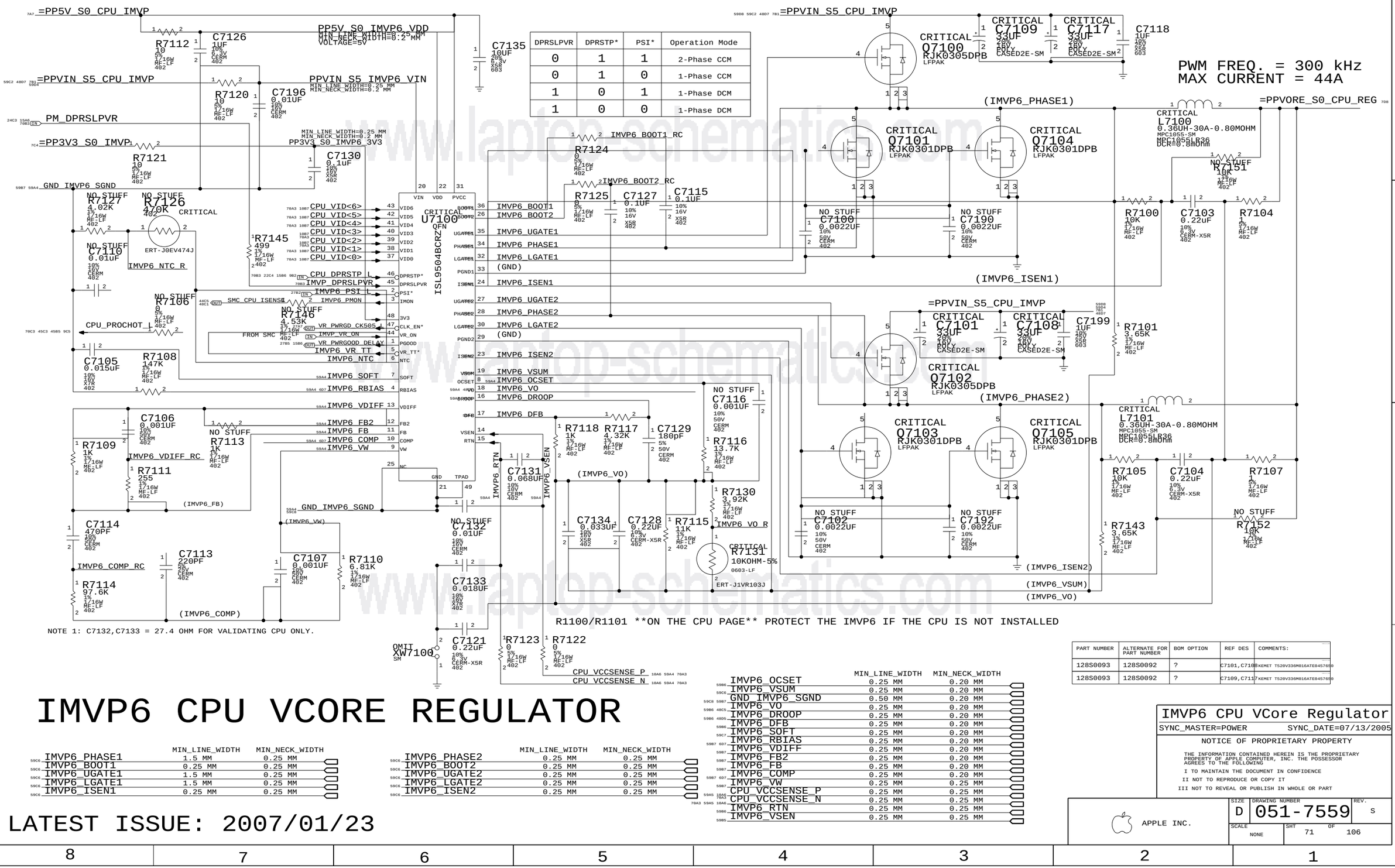
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	70	106



DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7101,C7108	KEMET T520V336M016ATE045/650
128S0093	128S0092	?	C7109,C7117	KEMET T520V336M016ATE045/650

IMVP6 CPU VCORE REGULATOR

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE1	1.5 MM	0.25 MM
IMVP6_BOOT1	0.25 MM	0.25 MM
IMVP6_UGATE1	1.5 MM	0.25 MM
IMVP6_LGATE1	1.5 MM	0.25 MM
IMVP6_ISEN1	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE2	0.25 MM	0.25 MM
IMVP6_BOOT2	0.25 MM	0.25 MM
IMVP6_UGATE2	0.25 MM	0.25 MM
IMVP6_LGATE2	0.25 MM	0.25 MM
IMVP6_ISEN2	0.25 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB2	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.25 MM
CPU_VCCSENSE_P	0.25 MM	0.25 MM
CPU_VCCSENSE_N	0.25 MM	0.25 MM
IMVP6_RTN	0.25 MM	0.25 MM
IMVP6_VSEN	0.25 MM	0.25 MM

LATEST ISSUE: 2007/01/23

IMVP6 CPU VCore Regulator

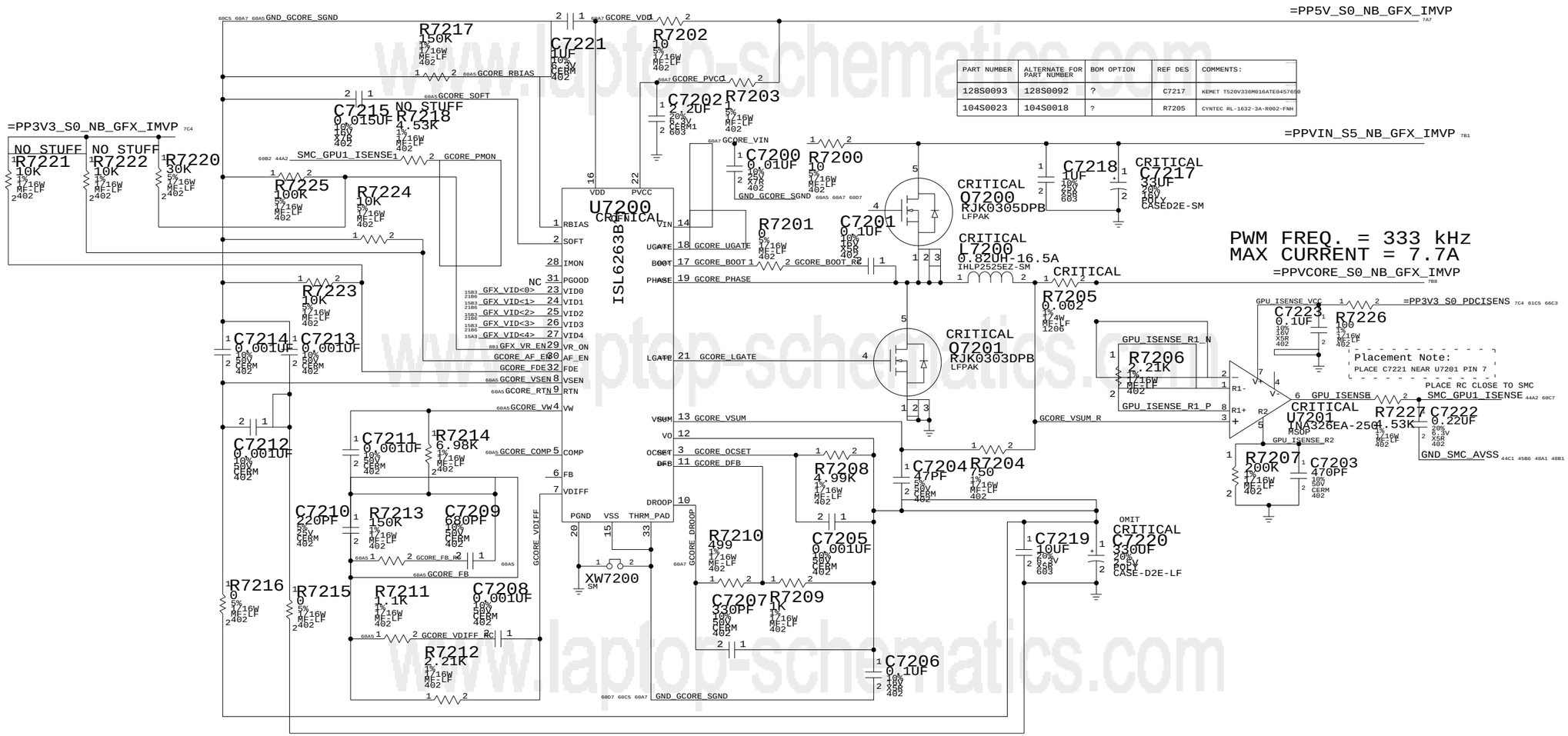
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 71 OF 106

RENDER VCORE POWER SUPPLY



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7217	KEMET T520V336M016ATE0457600
104S0023	104S0018	?	R7205	CYNTEC RL-1632-3A-R002-FNH

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GCORE_PHASE	1 MM	0.25 MM
GCORE_BOOT	0.3 MM	0.25 MM
GCORE_UGATE	1 MM	0.25 MM
GCORE_LGATE	1 MM	0.25 MM
GCORE_BOOT_RC	0.3 MM	0.25 MM
GND_GCORE_SGND	0.6 MM	0.25 MM
GCORE_VDD	0.3 MM	0.25 MM
GCORE_PVCC	0.3 MM	0.25 MM
GCORE_VIN	0.3 MM	0.25 MM
GCORE_DROOP	0.3 MM	0.25 MM
GCORE_VSUM	0.3 MM	0.25 MM
GCORE_DFB	0.3 MM	0.25 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
GCORE_OCSET	0.3 MM	0.25 MM
GCORE_VW	0.3 MM	0.25 MM
GCORE_RTN	0.3 MM	0.25 MM
GCORE_VSEN	0.3 MM	0.25 MM
GCORE_RBIAS	0.3 MM	0.25 MM
GCORE_SOFT	0.3 MM	0.25 MM
GCORE_COMP	0.3 MM	0.25 MM
GCORE_FB	0.3 MM	0.25 MM
GCORE_VDIFF	0.3 MM	0.25 MM
GCORE_FB_RC	0.3 MM	0.25 MM
GCORE_VDIFF_RC	0.3 MM	0.25 MM

Render VCore Supplies

SYNC_MASTER=GPU SYNC_DATE=06/29/2006

APPLE INC.

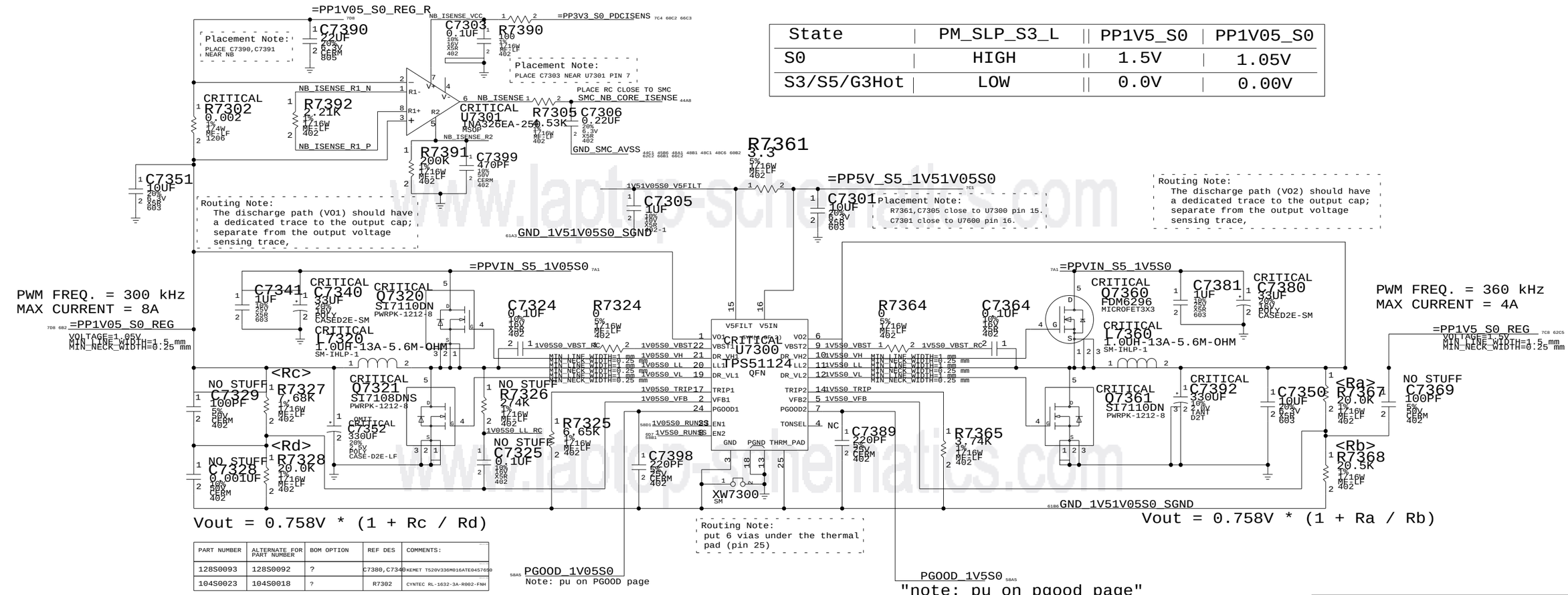
SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 72 OF 106

LATEST ISSUE: 2006/12/22

1.5V/1.05V POWER SUPPLY

State	PM_SLP_S3_L	PP1V5_S0	PP1V05_S0
S0	HIGH	1.5V	1.05V
S3/S5/G3Hot	LOW	0.0V	0.00V



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7380,C7340	KEMET T520V336M016ATE045/7650
104S0023	104S0018	?	R7302	CYNTEC RL-1632-3A-R002-FNH

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0448	376S0445	?	Q7360	

LATEST ISSUE: 2006/12/22

1.5V / 1.05V Supplies

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

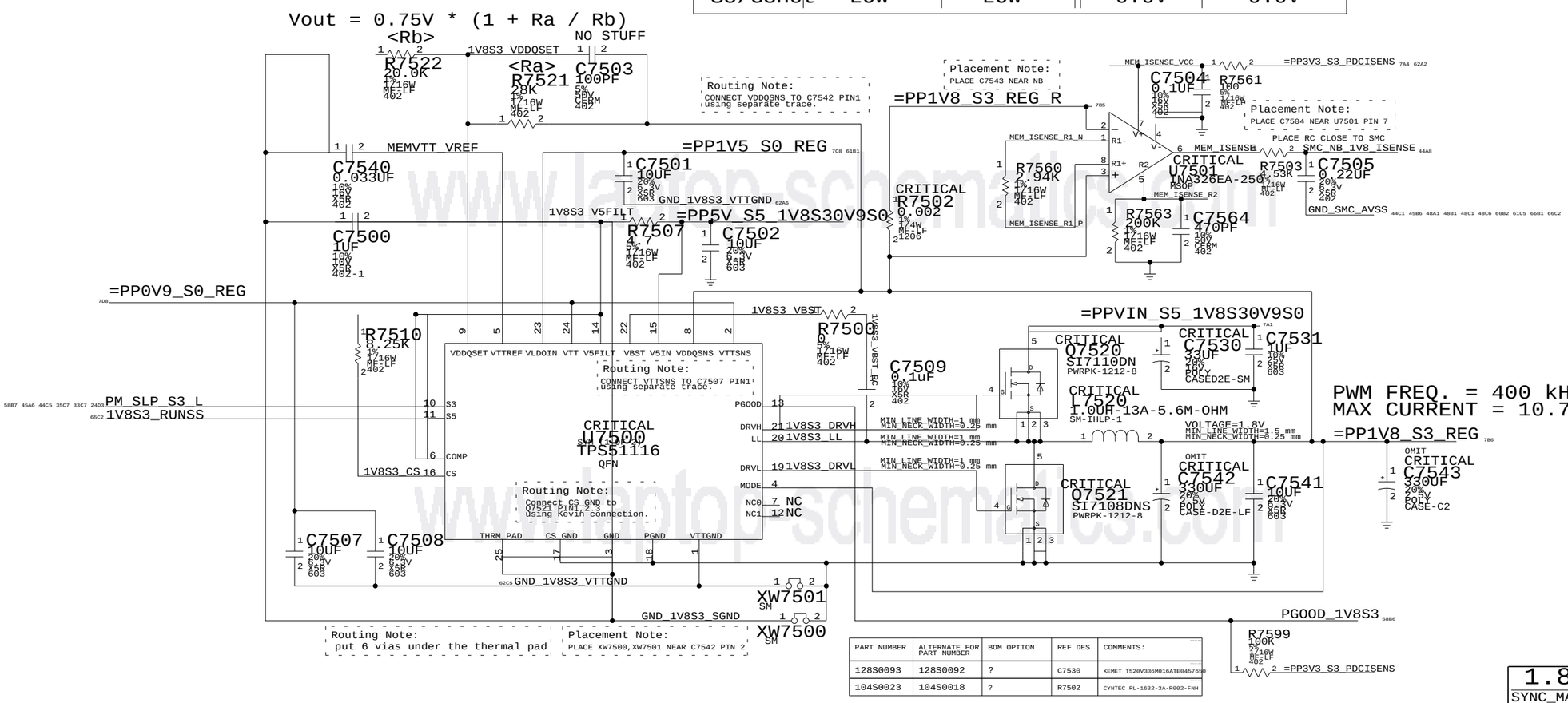
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	73	106

1.8V/0.9V POWER SUPPLY

State	PM_SLP_S4_L	PM_SLP_S3_L	PP1V8_S3	PP0V9_S0
S0	HIGH	HIGH	1.8V	0.9V
S3	HIGH	LOW	1.8V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7530	KEMET T520V336M016ATE0457600
104S0023	104S0018	?	R7502	CYNTEC RL-1632-3A-R002-FNH

LATEST ISSUE: 2006/12/22

1.8V/0.9V Supplies

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

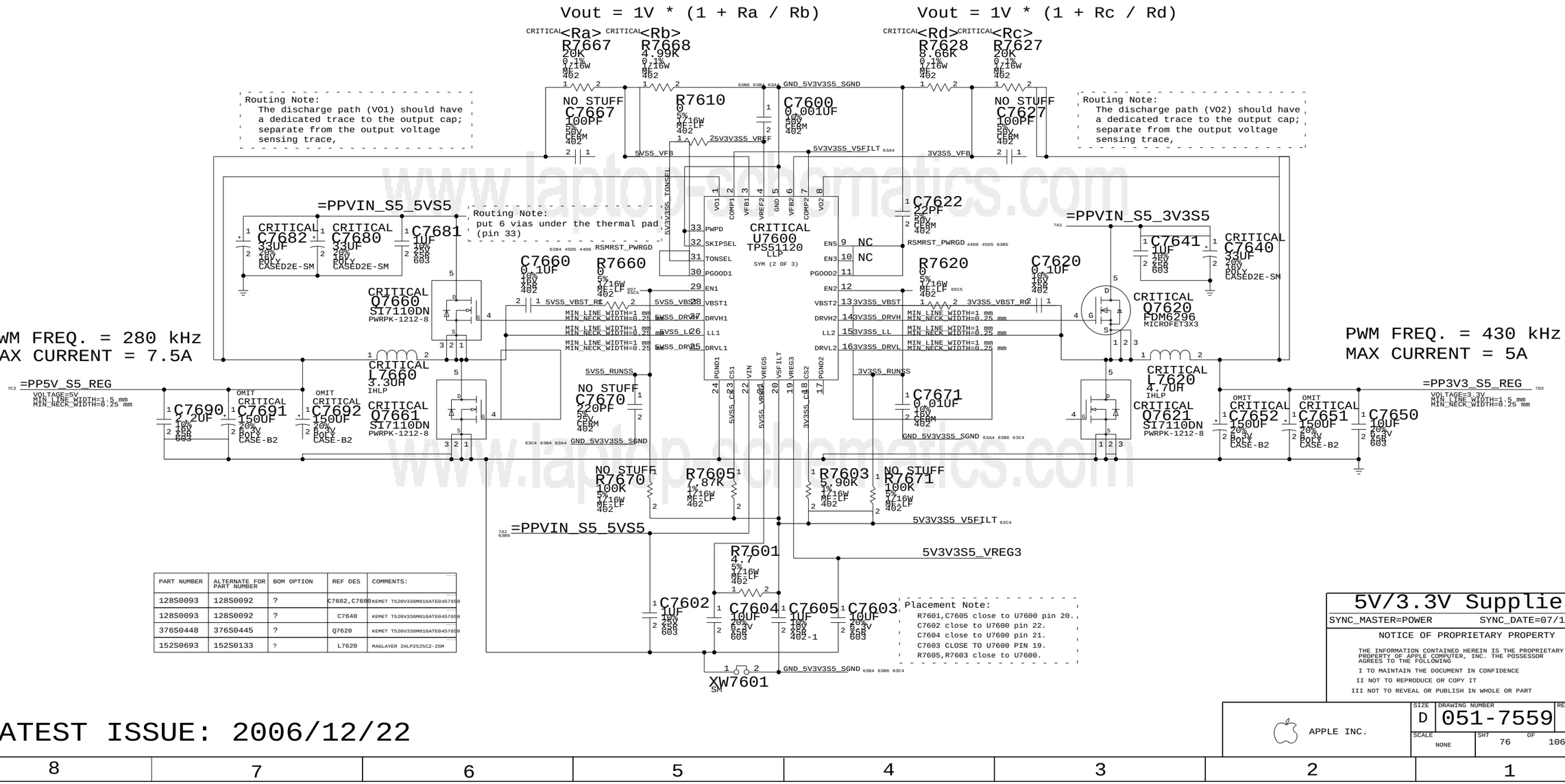
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	75	106

5V/3.3V POWER SUPPLY

State	SMC_PM_G2_EN	PP3V3_G3H	PP5V_S5	PP3V3_S5
G3H	LOW	3.3V	0.0V	0.0V
S0/S3/S5	HIGH	3.3V	5.0V	3.3V



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7682,C7680	KEMET T520V336M016ATE045/E60
128S0093	128S0092	?	C7640	KEMET T520V336M016ATE045/E60
376S0448	376S0445	?	Q7620	KEMET T520V336M016ATE045/E60
152S0693	152S0133	?	L7620	MAGLAYER IHLP2525CZ-2SM

5V/3.3V Supplies

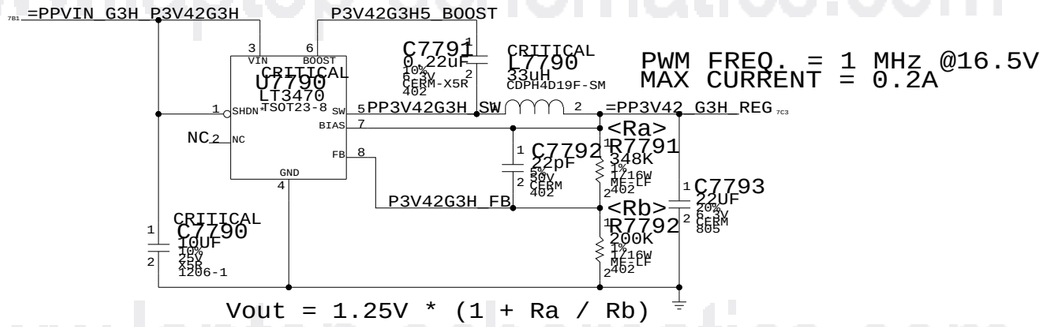
SYNC_MASTER=POWER SYNC_DATE=07/13/2005

APPLE INC.

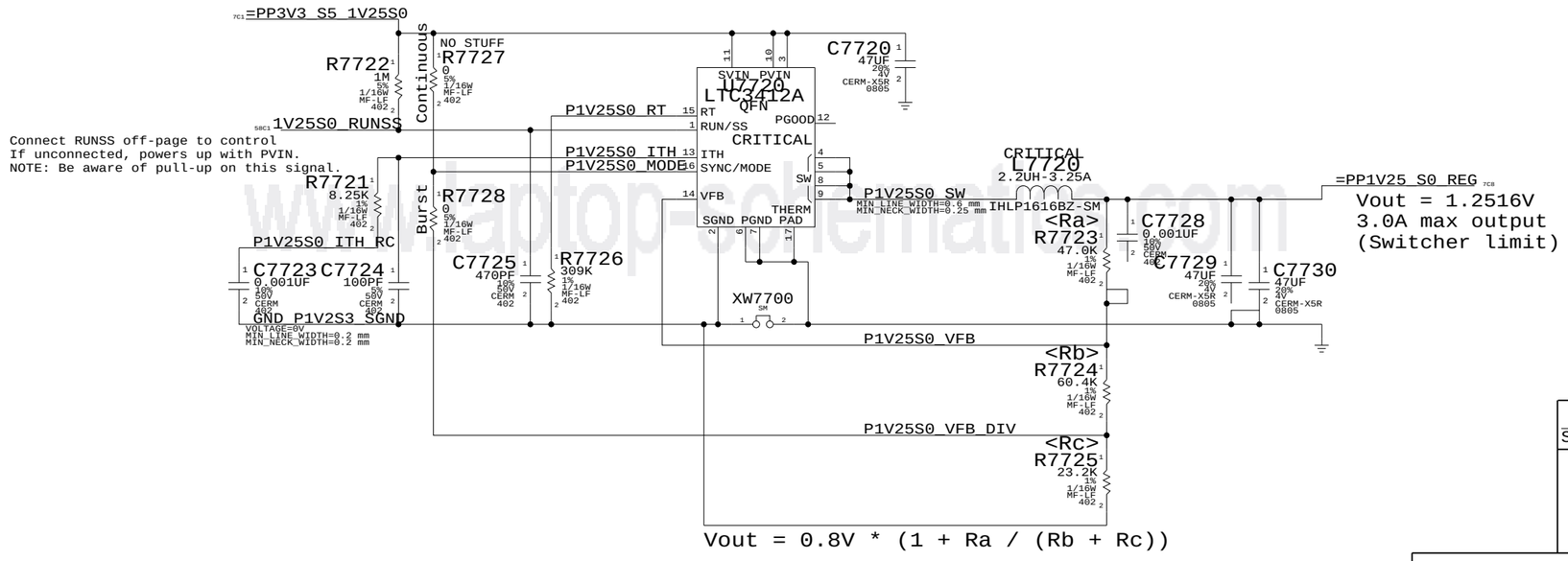
SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 76 OF 106	

LATEST ISSUE: 2006/12/22

3.425V G3H SUPPLY



1.25V S0 REGULATOR



LATEST ISSUE: 2007/3/8

3.42V/1.25V Switcher			
SYNC_MASTER=ENETSYNC_DATE=12/06/2005			
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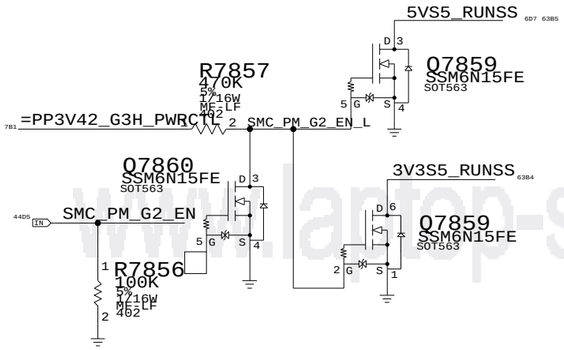
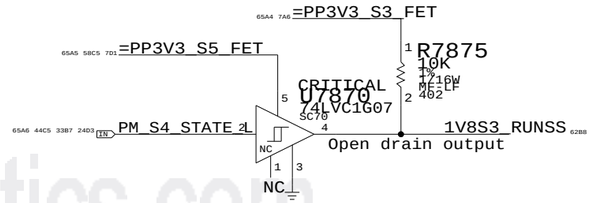
APPLE INC.	SIZE D	DRAWING NUMBER 051-7559	REV. S
	SCALE NONE	SHT 77	OF 106

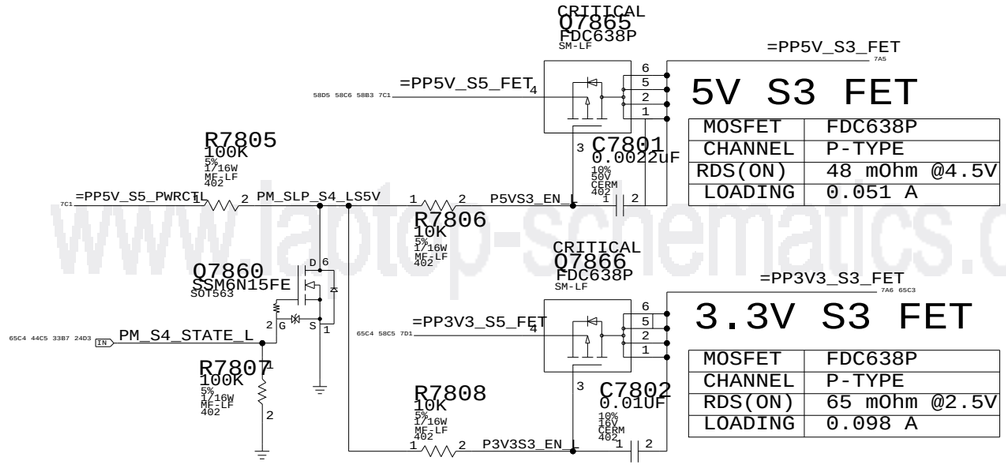
S3 FETS & S3/S5 CONTROL

5V/3.3V S5 RUN/SS CONTROL



1.8V S3 RUN/SS CONTROL





5V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.051 A

3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	65 mOhm @2.5V
LOADING	0.098 A

LATEST ISSUE: 2006/12/22

S3 FET & S3/S5 Control

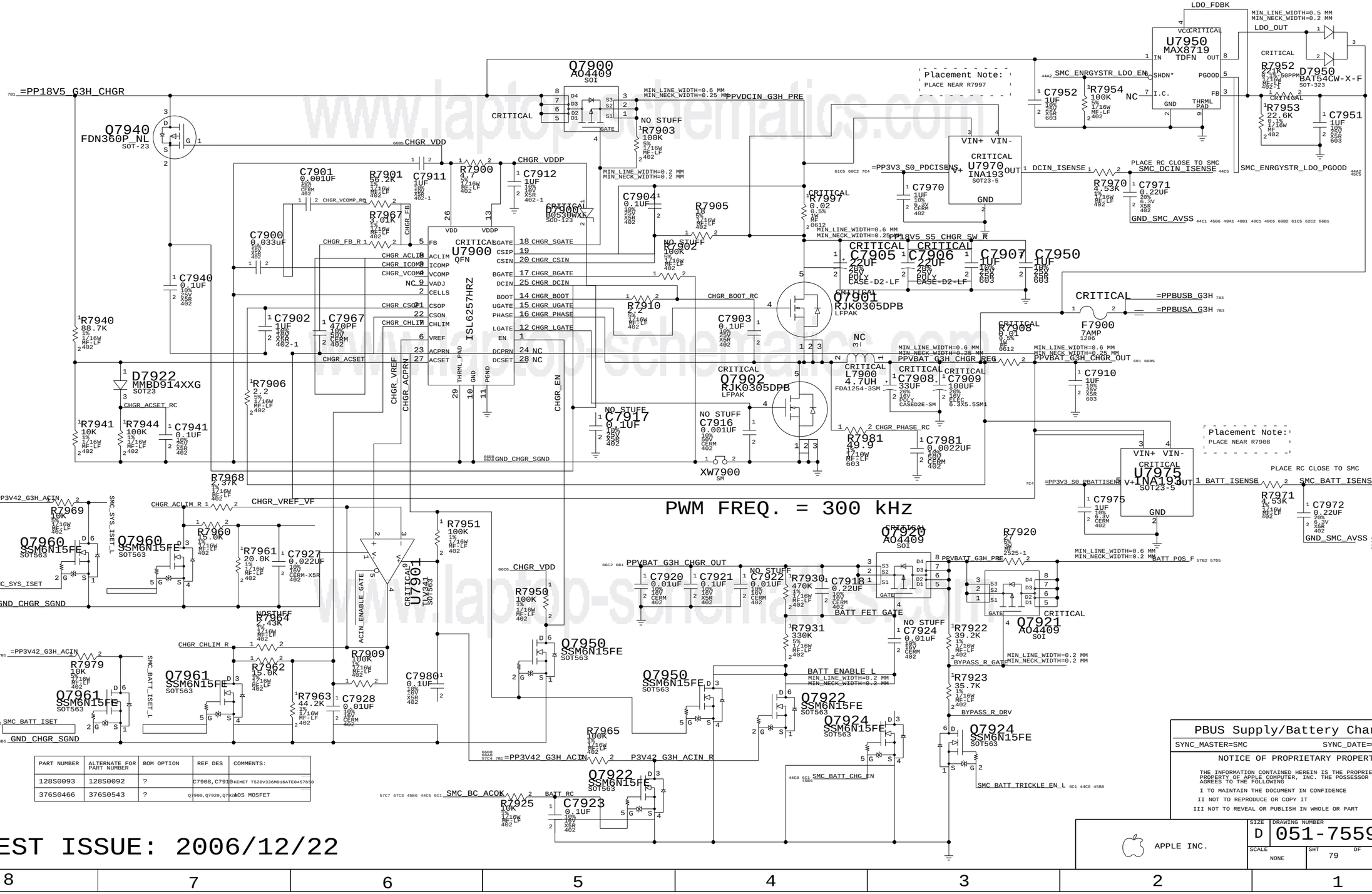
SYNC_MASTER=DSIMONWD SYNC_DATE=06/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	78	106

PBUS SUPPLY / BATTERY CHARGER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0093	128S0092	?	C7908,C7910	KEMET T520V336M016ATE045760
376S0466	376S0543	?	Q7900,Q7920,Q7922	AOS MOSFET

LATEST ISSUE: 2006/12/22

PBUS Supply/Battery Charger

SYNC_MASTER=SMC SYNC_DATE=08/19/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S
SCALE: NONE	SHT 79 OF 106	

INVERTER CONNECTOR

=PP5V_S0_LCD
R9000 100K 5% 1/16W MF-LF 402
R9001 100K 1% 1/16W MF-LF 402
INV_PWREN_F
INV_PWREN_L
Q9006 SSM3K15FV SOD-VESM
LVDS_BKLT_EN
Q9005 NTK3142P SOT723-3
PP5V_INV MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=5V
C9014 0.0022UF 10% 50V CERM 402
L9003 FERR-120-OHM-1.5A 0402-LF
=PPBUS_S5_INV
PPBUS_ALL_INV_CONN VOLTAGE=12.6V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM
R9003 0 5% 1/16W MF-LF 402
L9000 120-OHM-0.3A-EMI 0402-LF
PP5V_INV_F VOLTAGE=5V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM
L9001 120-OHM-0.3A-EMI 0402-LF
CRITICAL J9000 78171-0004 M-RT-SM 518S0521
INV_GND
INV_BKLIGHT_PWM
=PP3V3_S0_LCD
CRITICAL U9053 TC7SZ08AFEF SOT665
PLT_RST_L
LVDS_BKLT_CTL
BKLIGHT_CTL
C9059 0.1UF 10% 16V X5R 402
C9001 100PF 5% 50V CERM 402
C9002 0.001UF 10% 50V CERM 402
R9004 0 5% 1/16W MF-LF 402
C9000 0.001UF 10% 50V CERM 402
INVT_CHGND
THIS GND CONECTS TO CHASSIS GND

LCD + CAMERA CONNECTOR

=PP3V3_S5_LCD
R9002 100K 5% 1/16W MF-LF 402
R9023 10K 5% 1/16W MF-LF 402
LCDVDD_PWREN
LCDVDD_PWREN_L_R
CRITICAL Q9003 FDC606P SOT-6
C9013 0.0033UF 10% 50V CERM 402
PP3V3_LCDVDD_SW VOLTAGE=3.3V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM
C9011 0.1UF 10% 16V X5R 402
C9012 10UF 20% 6.3V X5R 603
Q9004 SSM3K15FV SOD-VESM
LVDS_VDD_EN
R9014 100K 1% 1/16W MF-LF 402
=PP3V3_S0_LCD
R9008 10K 5% 1/16W MF-LF 402
R9009 10K 5% 1/16W MF-LF 402
L9004 FERR-120-OHM-1.5A 0402-LF
L9008 120-OHM-0.3A-EMI 0402-LF
PP3V3_LCDVDD_SW_F VOLTAGE=3.3V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM
PP3V3_S0_LCD_F (LVDS DDC POWER) VOLTAGE=3.3V MIN_LINE_WIDTH=0.25 MM MIN_NECK_WIDTH=0.20 MM
LVDS_DDC_CLK
LVDS_DDC_DATA
C9009 0.001UF 10% 50V CERM 402
CRITICAL J9001 S-05016 2B F-RT-SM
=GND_CHASSIS_LVDS
LVDS_A_DATA_N<0>
LVDS_A_DATA_P<0>
LVDS_A_DATA_N<1>
LVDS_A_DATA_P<1>
LVDS_A_DATA_N<2>
LVDS_A_DATA_P<2>
LVDS_A_CLK_F_N
LVDS_A_CLK_F_P
CRITICAL L9006 90-OHM-200MA SM SYM_VER-1
LVDS_A_CLK_N
LVDS_A_CLK_P
CRITICAL L9007 90-OHM-200MA SM SYM_VER-1
=USB2_CAMERA_P
=USB2_CAMERA_N
USB2_CAMERA_CONN_P
USB2_CAMERA_CONN_N
L9005 FERR-120-OHM-1.5A 0402-LF
=PP5V_S3_CAMERA
PP5V_S3_CAMERA_F VOLTAGE=5V MIN_NECK_WIDTH=0.20 MM MIN_LINE_WIDTH=0.30 MM
MIC_LO_LVDS_CONN
MIC_HI_LVDS_CONN
LCD I/F
CAMERA I/F
C9016 0.001UF 10% 50V CERM 402
C9015 0.001UF 10% 50V CERM 402
C9010 0.001UF 10% 50V CERM 402
C9008 0.001UF 10% 50V CERM 402
Plexi: 516S0212
*Enclosure: 518S0364

LVDS REFERENCE CURRENT,2.37K OHM PULL DOWN RESISTOR NEEDED
R9013 2.37K 1% 1/16W MF-LF 402
LVDS_IBG
L9010 NOSTUFF FERR-1000-OHM 0402
MIC_LO_LVDS
L9011 NOSTUFF FERR-1000-OHM 0402
MIC_HI_LVDS
L9012 NOSTUFF FERR-1000-OHM 0402
MIC_SHIELD_LVDS
CRITICAL DZ9000 NOSTUFF 8V-100PF 402-1
CRITICAL DZ9001 NOSTUFF 8V-100PF 402-1
=GND_CHASSIS_LVDS
R9015 NOSTUFF 10K 5% 1/16W MF-LF 402
R9016 NOSTUFF 10K 5% 1/16W MF-LF 402
LVDS_CTRL_CLK
LVDS_CTRL_DATA

INVERTER,LVDS,TMDS

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

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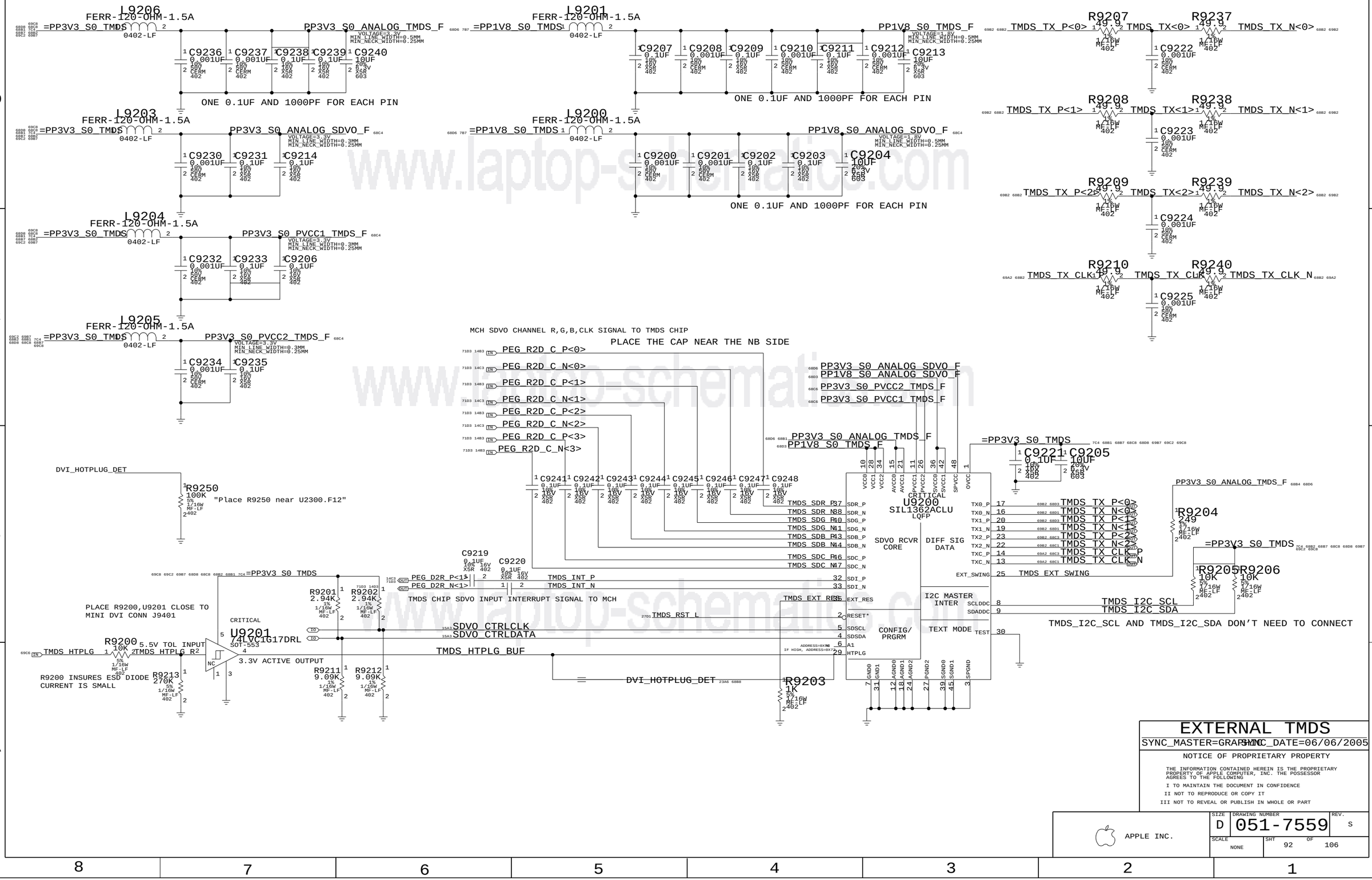
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	90	106


L9206
FERR-120-OHM-1.5A
=PP3V3_S0_TMDS
0402-LF
PP3V3_S0_ANALOG_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9236 0.001UF
C9237 0.001UF
C9238 0.1UF
C9239 0.1UF
C9240 10UF
ONE 0.1UF AND 1000PF FOR EACH PIN
L9201
FERR-120-OHM-1.5A
=PP1V8_S0_TMDS
PP1V8_S0_TMDS_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9207 0.1UF
C9208 0.001UF
C9209 0.1UF
C9210 0.001UF
C9211 0.1UF
C9212 0.001UF
C9213 10UF
ONE 0.1UF AND 1000PF FOR EACH PIN
L9203
FERR-120-OHM-1.5A
=PP3V3_S0_TMDS
PP3V3_S0_ANALOG_SDVO_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9230 0.001UF
C9231 0.1UF
C9214 0.1UF
L9200
FERR-120-OHM-1.5A
=PP1V8_S0_TMDS
PP1V8_S0_ANALOG_SDVO_F
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C9200 0.001UF
C9201 0.001UF
C9202 0.1UF
C9203 0.1UF
C9204 10UF
ONE 0.1UF AND 1000PF FOR EACH PIN
L9204
FERR-120-OHM-1.5A
=PP3V3_S0_TMDS
PP3V3_S0_PVCC1_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9232 0.001UF
C9233 0.1UF
C9206 0.1UF
L9205
FERR-120-OHM-1.5A
=PP3V3_S0_TMDS
PP3V3_S0_PVCC2_TMDS_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C9234 0.001UF
C9235 0.1UF
MCH SDVO CHANNEL R,G,B,CLK SIGNAL TO TMDS CHIP
PLACE THE CAP NEAR THE NB SIDE
PEG_R2D_C_P<0>
PEG_R2D_C_N<0>
PEG_R2D_C_P<1>
PEG_R2D_C_N<1>
PEG_R2D_C_P<2>
PEG_R2D_C_N<2>
PEG_R2D_C_P<3>
PEG_R2D_C_N<3>
PP3V3_S0_ANALOG_SDVO_F
PP1V8_S0_ANALOG_SDVO_F
PP3V3_S0_PVCC2_TMDS_F
PP3V3_S0_PVCC1_TMDS_F
PP3V3_S0_ANALOG_TMDS_F
PP1V8_S0_TMDS_F
C9241 0.1UF
C9242 0.1UF
C9243 0.1UF
C9244 0.1UF
C9245 0.1UF
C9246 0.1UF
C9247 0.1UF
C9248 0.1UF
U9200
SIL1362ACLU
LQFP
CRITICAL
SDVO RCVR CORE
DIFF SIG DATA
I2C MASTER INTER
CONFIG/ PRGRM
TEXT MODE
TMDS_SDR_P
TMDS_SDR_N
TMDS_SDG_P
TMDS_SDG_N
TMDS_SDB_P
TMDS_SDB_N
TMDS_SDC_P
TMDS_SDC_N
TMDS_INT_P
TMDS_INT_N
TMDS_EXT_RES
TMDS_RST_L
SDVO_CTRLCLK
SDVO_CTRLDATA
TMDS_HTPLG_BUF
DVI_HOTPLUG_DET
TMDS_TX_P<0>
TMDS_TX_N<0>
TMDS_TX_P<1>
TMDS_TX_N<1>
TMDS_TX_P<2>
TMDS_TX_N<2>
TMDS_TX_CLK_P
TMDS_TX_CLK_N
TMDS_EXT_SWING
TMDS_I2C_SCL
TMDS_I2C_SDA
R9207 49.9
R9237 49.9
R9222 0.001UF
R9208 49.9
R9238 49.9
R9223 0.001UF
R9209 49.9
R9239 49.9
R9224 0.001UF
R9210 49.9
R9240 49.9
R9225 0.001UF
R9204 249
R9205 10K
R9206 10K
C9221 0.1UF
C9205 10UF
C9219 0.1UF
C9220 0.1UF
R9250 100K
"Place R9250 near U2300.F12"
R9200 10K
R9213 270K
R9201 2.94K
R9202 2.94K
R9211 9.09K
R9212 9.09K
R9203 1K
U9201
74LVC1G17DRL
SOT-553
CRITICAL
PLACE R9200,U9201 CLOSE TO MINI DVI CONN J9401
R9200 INSURES ESD DIODE CURRENT IS SMALL
5.5V TOL INPUT
3.3V ACTIVE OUTPUT
TMDS_I2C_SCL AND TMDS_I2C_SDA DON'T NEED TO CONNECT
EXTERNAL TMDS
SYNC_MASTER=GRAPHIC SYNC_DATE=06/06/2005
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APPLE INC.
SIZE D
DRAWING NUMBER 051-7559
REV. S
SCALE NONE
SHT 92 OF 106

NB VIDEO ALIASES

=CRT_TVO_IREF	CRT_TVO_IREF		
=TV_A_DAC	TV_A_DAC	MAKE_BASE=TRUE	69B8 71C3
=TV_B_DAC	TV_B_DAC	MAKE_BASE=TRUE	69B8 71C3
=TV_C_DAC	TV_C_DAC	MAKE_BASE=TRUE	69A8 71C3
=CRT_BLUE	CRT_BLUE	MAKE_BASE=TRUE	69B8 71C3
=CRT_GREEN	CRT_GREEN	MAKE_BASE=TRUE	69A8 71C3
=CRT_RED	CRT_RED	MAKE_BASE=TRUE	69A8 71C3
=CRT_HSYNC_R	CRT_HSYNC_R	MAKE_BASE=TRUE	69C3 71C3
=CRT_VSYNC_R	CRT_VSYNC_R	MAKE_BASE=TRUE	69C3 71C3

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

Isolation required for DVI power switch

TMDS(MINI DVI) INTERFACE

A 1.3K OHM 1% RESISTOR IS REQUIRED BETWEEN CRT_IREF AND GROUND

R9469 1.21K 1% 1/16W MF-LF 402

CRT_TVO_IREF

F9404 0.5AMP-13.2V SM-LF CRITICAL

=PP5V_S0_TMDS VOLTAGE=5V MIN_LINE_WIDTH=0.30 MM MIN_NECK_WIDTH=0.20 MM

PP5V_S0_TMDS_FUSE VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

D9401 1SS418 SOD-723

L9444 600-OHM-300MA 0402

PP5V_S0_DVIPORT VOLTAGE=5V MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM

C9404 0.1UF 20% 16V CERM 402

=GND_CHASSIS_TMDS_UPPER

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
740S0044	740S0028	?	F9404	

PP5V_S0_DVIPORT_D

DVI power DIODE on page 95 (D9500)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0370	155S0348	?	L9404	MURATA ALTERNATIVE

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR CONNECTOR

=PP3V3_S0_TMDS

C9460 0.1UF 20% 16V CERM 402

CRITICAL U9404 SN74LVC2G125DCU

R9460 39 5% 1/16W MF-LF 402 — CRT_HSYNC_R — CRT_HSYNC_LS_R

R9470 39 5% 1/16W MF-LF 402 — CRT_HSYNC_LS — VGA_HSYNC

NOSTUFF C9442 33PF 5% 50V CERM 402

PLACE THE RESISTOR CLOSE TO GMCH AND THE CAP NEAR THE CONNECTOR

R9461 39 5% 1/16W MF-LF 402 — CRT_VSYNC_R — CRT_VSYNC_LS_R

R9471 39 5% 1/16W MF-LF 402 — CRT_VSYNC_LS — VGA_VSYNC

NOSTUFF C9443 33PF 5% 50V CERM 402

=PP3V3_S0_NB

R9466 2.2K 5% 1/16W MF 402 — TV_DCONSEL<0>

R9467 2.2K 5% 1/16W MF 402 — TV_DCONSEL<1>

R9462 2.2K 5% 1/16W MF 402

R9463 2.2K 5% 1/16W MF 402

TMDS_HTPLG

C9410 0.001UF 10% 50V CERM 402

=PP3V3_S0_TMDS

R9421 2.2K 5% 1/16W MF 402 — CRT_DDC_CLK

R9422 2.2K 5% 1/16W MF 402 — CRT_DDC_DATA

NOTE: CRT_DDC_* ARE NOT 5V COMPLIANT

Q9401 SSM6N15FE SOT563

GPU_CRT_DDC_CLK

GPU_CRT_DDC_DATA

C9411 100PF 5% 50V CERM 402

C9412 100PF 5% 50V CERM 402

OMIT CRITICAL J9401 MINI-DVI-M42-BLK F-RT-TH

PP5V_S0_DVIPORT

TMDS_TX_CONN_P<2>
TMDS_TX_CONN_N<2>
TMDS_TX_CONN_P<1>
TMDS_TX_CONN_N<1>
TMDS_TX_CONN_P<0>
TMDS_TX_CONN_N<0>
TMDS_TX_CONN_CLK_P
TMDS_TX_CONN_CLK_N

NC NC VGA_B VGA_HSYNC VGA_G VGA_VSYNC VGA_R

514-0376

=GND_CHASSIS_TMDS_UPPER — =GND_CHASSIS_TMDS_DOWN

NOSTUFF C9421 0.1UF 10% 16V CER 402

OMIT CRITICAL L9405 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<2> — TMDS_TX_N<2>

OMIT CRITICAL L9407 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<1> — TMDS_TX_N<1>

OMIT CRITICAL L9406 90-OHM-100MA 1210-4SM1 — TMDS_TX_P<0> — TMDS_TX_N<0>

CRITICAL L9404 300-OHM-100MA 1210-4SM — TMDS_TX_CLK_P — TMDS_TX_CLK_N

PLACE R9450 R9451 CLOSE TO GMCH

TV_A_DAC — CRT_BLUE

R9450 75 1% 1/16W MF-LF 402 — =CRT_BLUE_L

R9451 75 1% 1/16W MF-LF 402 — =TV_A_RTN

PLACE R9452 R9453 CLOSE TO GMCH

TV_B_DAC — CRT_GREEN

R9452 75 1% 1/16W MF-LF 402 — =CRT_GREEN_L

R9453 75 1% 1/16W MF-LF 402 — =TV_B_RTN

PLACE R9454 R9455 CLOSE TO GMCH

TV_C_DAC — CRT_RED

R9454 75 1% 1/16W MF-LF 402 — =CRT_RED_L

R9455 75 1% 1/16W MF-LF 402 — =TV_C_RTN

=PP3V3_S0_TMDS

C9439 0.1UF 10% 16V X5R 402

CRITICAL U9401 TS3V330 SOP

EXT_COMPVID_B

EXT_Y_G

EXT_C_R

SB_CRT_TVOUT_MUX_L

FL9400 210MHZ MEA2010P-SM CRITICAL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0371	3	TDK AND MURATA	L9405,L9406,L9407	CRITICAL	K36

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0480	1	CONN,REC,MINI-DVI,32P,RA,TABS,MG3	J9401	CRITICAL	NORMAL
514-0481	1	CONN,REC,MINI-DVI,32P,RA,TABS,BLK	J9401	CRITICAL	FANCY

MINI-DVI CONNECTOR

SYNC_MASTER=EUGENE SYNC_DATE=05/21/05

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE — SHT 94 OF 106

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	?
FSB_ADDR2ADDR	*	=2:1_SPACING	?
FSB_ADSTB	*	=3:1_SPACING	?
FSB_ADDR2ADSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	?
FSB_DATA2DATA	*	=2:1_SPACING	?
FSB_DSTB	*	=3:1_SPACING	?
FSB_DATA2DSTB	*	=3:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	9D6 13C3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BNR_L	9D6 13C3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	9D6 13C3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BREQ0_L	9D6 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DBSY_L	9D6 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	9D6 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DPWR_L	9B2 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	9D6 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HIT_L	9C6 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_HITM_L	9C6 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_LOCK_L	9D6 13B3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	9D6 13A3
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	9D6 13B3
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	9D6 12B5 13A5
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..0>	9C4 13C5 13D5
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_DINV_L<0>	9C4 13B3
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	9C4 13B3
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	9C4 13B3
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..16>	9B4 9C4 13C5
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_DINV_L<1>	9B4 13B3
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	9B4 13B3
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	9B4 13B3
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..32>	9C2 13B5 13C5
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_DINV_L<2>	9C2 13B3
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	9C2 13A3
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	9C2 13B3
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..48>	9B2 9C2 13B5
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_DINV_L<3>	9B2 13B3
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	9B2 13A3
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	9B2 13B3
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..3>	9D8 13C3 13D3
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	9C8 9D8 13A3
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	9D8 13C3
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..17>	9C8 13C3
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	9C8 13C3
CPU_IERR_L	CPU_55S		CPU_IERR_L	9D6
CPU_FERR_L	CPU_55S		CPU_FERR_L	9C8 22C2
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	9C5 45B5 45C3 59C8
CPU_PWRGD	CPU_55S		CPU_PWRGD	9B2 12B1 22C4
CPU_FROM_SB	CPU_55S		CPU_INTR	9B8 22C4
CPU_FROM_SB	CPU_55S		CPU_NMI	9B8 22C4
CPU_FROM_SB	CPU_55S		CPU_A20M_L	9C8 22C4
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	9B2 22C4
CPU_FROM_SB	CPU_55S		CPU_IGNNE_L	9C8 22C4
CPU_INIT_L	CPU_55S		CPU_INIT_L	9D6 22C4 46B2
CPU_FROM_SB	CPU_55S		CPU_SMI_L	9B8 22C4
CPU_FROM_SB	CPU_55S		CPU_STPCLK_L	9B8 22C4
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	9C6 15A6 22C2 45B3
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	9A2 13A5
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	15A6 24C3 59D8
(See above)	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	59C7
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	9B4 29C6
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<0>	15C6 29C8
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	9A4 29B6
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<1>	15C6 29B8
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	9A4 29A6
(See above)	CPU_55S	CPU_2TO1	NB_BSEL<2>	15B6 29B8
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	9B2 15B6 22C4 59C7
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	9B4
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	9B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9B3
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	9B3
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9B3
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	9B7 9C6 12B3
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	9A7 9C6 12B5
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	9B7 9C6 12B2
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	9A7 9C6 12B2 12B3
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	9A7 9C6 12B3
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	9C6 12B2 12B3
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	9C5 12B2
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	75C3
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	75C3
(FSB_CPURST_L)	CPU_55S	CPU_ITP	ITP_CPURST_L	
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	10B7 59C7
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10A6 59A4 59A5
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10A6 59A4 59A5
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	

CPU/FSB Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/08/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE SHT 100 OF 106

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	?
DMI	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CRT_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CRT_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	
LVDS	*	20 MIL	?	
CRT	*	25 MIL	?	DG Says 40 mil spacing minimum
CRT_2CRT	*	20 MIL	?	
CRT_SYNC	*	25 MIL	?	DG Says 30 mil spacing minimum
CRT_SYNC2SYNC	*	20 MIL	?	
TVDAC	*	25 MIL	?	DG Says 40 mil spacing minimum
TVDAC_2TVDAC	*	20 MIL	?	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT
CRT_SYNC	CRT_SYNC	*	CRT_SYNC2SYNC
TVDAC	TVDAC	*	TVDAC_2TVDAC

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.

CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
PEG_R2D	PCIE_100D	PCIE	PEG_D2R_N<1> 14D3 68B6
	PCIE_100D	PCIE	PEG_D2R_P<1> 14C3 68B6
	PCIE_100D	PCIE	PEG_R2D_C_P<3..0> 14B3 68B6 68C6
	PCIE_100D	PCIE	PEG_R2D_C_N<3..0> 14B3 14C3 68B6 68C6
DMI_N2S	DMI_100D	DMI	DMI_N2S_P<3..0> 15B3 23D2
	DMI_100D	DMI	DMI_N2S_N<3..0> 15B3 23D2
DMI_S2N	DMI_100D	DMI	DMI_S2N_P<3..0> 15B3 23D2
	DMI_100D	DMI	DMI_S2N_N<3..0> 15B3 15C3 23D2
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P 14C5 67B3
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N 14C5 67B3
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0> 14C5 67B2
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0> 14C5 67B2
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_P<3>
LVDS_A_DATA3	LVDS_100D	LVDS	LVDS_A_DATA_N<3>
LVDS_IBG		LVDS	LVDS_IBG 14D5 67A8
CRT_TVO_IREF		CRT	CRT_TVO_IREF 69D7 69D8
CRT_RED	CRT_50S	CRT	CRT_RED 69A8 69D5
CRT_GREEN	CRT_50S	CRT	CRT_GREEN 69A8 69D5
CRT_BLUE	CRT_50S	CRT	CRT_BLUE 69B8 69D5
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_HSYNC_R 69C3 69D5
CRT_SYNC	CRT_55S	CRT_SYNC	CRT_VSYNC_R 69C3 69D5
TV_A_DAC	CRT_50S	TVDAC	TV_A_DAC 69B8 69D7
TV_B_DAC	CRT_50S	TVDAC	TV_B_DAC 69A8 69D7
TV_C_DAC	CRT_50S	TVDAC	TV_C_DAC 69A8 69D7

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NB Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 101 OF 106

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=3:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<2..0>	15D3 30A4 30D4
	MEM_70D	MEM_CLK	MEM_CLK_N<2..0>	15D3 30A4 30D4
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	15D3 30C4 30C6 32D6
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	15D3 30B4 30B6 32D6
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	15C3 30B4 30B6 32D6
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	15C6 16B5 16C5 30B4 30B6 30C4 30C6 32C6
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	16D5 30B4 30B6 30C6 32C6
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	16B5 30B4 32B6
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	16D5 30B6 32B6
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	16B5 30B6 32B6
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<7..0>	16D8 30D4 30D6
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15..8>	16C8 30D4 30D6
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..16>	16C8 30C4 30C6
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..24>	16C8 30C4 30C6 30D4 30D6
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<39..32>	16B8 16C8 30B4 30B6
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<47..40>	16B8 30A4 30A6 30B4 30B6
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55..48>	16B8 30A4 30A6
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..56>	16A8 16B8 30A4 30A6
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	16D5 30D4
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	16D5 30D4
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	16C5 30C6
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	16C5 30C4
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	16C5 30B4
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	16C5 30B6
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	16C5 30A6
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	16C5 30A4
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	16C5 30D6
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	16C5 30D6
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	16C5 30D6
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	16C5 30D6
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	16C5 30C4
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	16C5 30C4
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	16C5 30C6
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	16C5 30C6
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	16C5 30B6
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	16C5 30B6
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	16C5 30B4
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	16C5 30B4
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	16C5 30A4
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	16C5 30A4
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	16C5 30A6
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	16C5 30A6
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<5..3>	15D3 31A4 31D4
	MEM_70D	MEM_CLK	MEM_CLK_N<5..3>	15D3 31A4 31D4
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	15D3 31C4 31C6 32D5 32D6
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	15C3 15D3 31B4 31B6 32D6
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	15C3 31B4 31B6 32D6
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	15C6 16B1 16C1 31B4 31B6 31C4 31C6 32A5 32B5
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	16D1 31B4 31B6 31C6 32A6
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	16B1 31B4 32A6
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	16D1 31B6 32A6
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	16B1 31B6 32A6
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7..0>	16D4 31D4 31D6
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..8>	16C4 31D4 31D6
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<23..16>	16C4 31C4 31C6
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..24>	16C4 31C4 31C6
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39..32>	16B4 16C4 31B4 31B6
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..40>	16B4 31A4 31A6 31B4 31B6
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..48>	16B4 31A4 31A6
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63..56>	16A4 16B4 31A4 31A6
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	16D1 31D4
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	16D1 31D4
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	16C1 31C4
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	16C1 31C6
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	16C1 31B4
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	16C1 31A6
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	16C1 31A4
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	16C1 31A6
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	16C1 31D6
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	16C1 31D6
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	16C1 31D6
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	16C1 31D6
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	16C1 31C6
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	16C1 31C6
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	16C1 31C4
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	16C1 31C4
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	16C1 31B6
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	16C1 31B6
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	16C1 31A4
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	16C1 31B4
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	16C1 31A6
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	16C1 31A6
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	16C1 31A4
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	16C1 31A4

Memory Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/08/2006

APPLE INC.

SIZE D | DRAWING NUMBER 051-7559 | REV. S

SCALE NONE | SHT 102 OF 106

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	?
SATA	*	20 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=1.8:1_SPACING	?

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_60S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
USB_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	20 MIL	?
USB_2CLK	*	25 MIL	?

DG says minimum spacing 50 mils to clocks

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	?
SPI	*	=1.8:1_SPACING	?

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..0> 22B4 22C4 39C3 39C5
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0> 22B4 39B3 39B5
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L 22B4 39B5
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L 22B4 39B3
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L 22B4 39B5
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L 22B4 39C3
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L 22B4 39B3
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ 22A4 39C3
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY 22A4 39B5
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14 22B4 39B5
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L 23B6 39A8
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P 22B6 40D4
	SATA_100D	SATA	SATA_A_R2D_C_N 22B6 40D4
	SATA_100D	SATA	SATA_A_R2D_P 40D7
	SATA_100D	SATA	SATA_A_R2D_N 40D7
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P 22B6 40C4
	SATA_100D	SATA	SATA_A_D2R_N 22B6 40D4
	SATA_100D	SATA	SATA_A_D2R_C_P 40C7
	SATA_100D	SATA	SATA_A_D2R_C_N 40D7
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 8A6 22C8
	HDA_55S	HDA	HDA_BIT_CLK_R 22C6
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 8A6 22C8
	HDA_55S	HDA	HDA_SYNC_R 22C6
HDA_RST_L	HDA_55S	HDA	HDA_RST_L 8A6 22C8
	HDA_55S	HDA	HDA_RST_L_R 22C6
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 8A6 22C8
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 8A6 22B8
	HDA_55S	HDA	HDA_SDOUT_R 22B6
USB_EXTA	USB_90D	USB	USB_EXTA_P 8C1 23C2
	USB_90D	USB	USB_EXTA_N 8C1 23C2
	USB_90D	USB	USB_EXTA_MUXED_P
	USB_90D	USB	USB_EXTA_MUXED_N
USB_MINI	USB_90D	USB	USB_MINI_P 8C1 23C2
	USB_90D	USB	USB_MINI_N 8C1 23C2
USB_3G	USB_90D	USB	USB_3G_P
	USB_90D	USB	USB_3G_N
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 8C1 23C2
	USB_90D	USB	USB_CAMERA_N 8C1 23C2
USB_BT	USB_90D	USB	USB_BT_P 8C1 8C2 23C2
	USB_90D	USB	USB_BT_N 8B1 8B2 23C2
USB_TPAD	USB_90D	USB	USB_TPAD_P 8C1 23C2
	USB_90D	USB	USB_TPAD_N 8C1 23C2
USB_IR	USB_90D	USB	USB_IR_P 8C1 8C2 23C2
	USB_90D	USB	USB_IR_N 8C1 8C2 23C2
USB_EXTB	USB_90D	USB	USB_EXTB_P 8B1 23C2
	USB_90D	USB	USB_EXTB_N 8B1 23C2
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 8B1 23C2
	USB_90D	USB	USB_EXCARD_N 8B1 23C2
USB_EXTC	USB_90D	USB	USB_EXTC_P 8B1 23C2
	USB_90D	USB	USB_EXTC_N 8B1 23C2
USB_RBIAS	USB_60S		USB_RBIAS 23B3
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK 24D5 47D8
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA 24D5 47D8
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK 24D5 47A8
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA 24D5 47A8
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R 23C5 52C7
	SPI_55S	SPI	SPI_A_SCLK_R 52C5
SPI_SI	SPI_55S	SPI	SPI_SI_R 23C5 52C3
	SPI_55S	SPI	SPI_A_SI_R 52C4
SPI_SO	SPI_55S	SPI	SPI_SO 23C5 52C3
	SPI_55S	SPI	SPI_A_SO_R 52C4
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0> 23C5 52C7
	SPI_55S	SPI	SPI_CE_L<0> 52C6
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>

SB Constraints (1 of 2)

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE SHT 103 OF 106

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Platform LAN (Nineveh) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LAN_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
GLAN_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CLK	*	=2.5:1_SPACING	?
ENET_GLAN	*	20 MILS	?
ENET_LAN	*	=1.5:1_SPACING	?
ENET_MDI	*	25 MILS	?

DG says 30 mils min separation.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Controller Link (AMT) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLINK_12MIL	*	Y	12 MILS	5 MILS	300 MILS	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLINK	*	=1.8:1_SPACING	?
CLINK_VREF	*	12 MILS	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCI_AD	PCI_55S	PCI	PCI AD<18..0>	23A8 23B8 37B5 37C5
PCI_AD19	PCI_55S	PCI	PCI AD<19>	23A8 37B6
PCI_AD20	PCI_55S	PCI	PCI AD<20>	23A8 37B5
PCI_AD	PCI_55S	PCI	PCI AD<31..21>	23A8 37B5
PCI_AD	PCI_55S	PCI	PCI PAR	23A6 37B5
PCI_C_BE_L	PCI_55S	PCI	PCI C_BE_L<3..0>	23B6 37B5
PCI_CNTL	PCI_55S	PCI	PCI IRDY_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI DEVSEL_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI PERR_L	23A4 23A6 37A5
PCI_LOCK_L	PCI_55S	PCI	PCI LOCK_L	23A4 23A6
PCI_CNTL	PCI_55S	PCI	PCI SERR_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI STOP_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI TRDY_L	23A4 23A6 37A5
PCI_CNTL	PCI_55S	PCI	PCI FRAME_L	23A4 23A6 37A5
PCI_FW_REQ_L	PCI_55S	PCI	PCI FW_REQ_L	23A4 23B6 37A5
PCI_FW_GNT_L	PCI_55S	PCI	PCI FW_GNT_L	23B5 37A5
PCI_REQ1_L	PCI_55S	PCI	PCI REQ1_L	23A4 23B6
PCI_GNT1_L	PCI_55S	PCI	PCI GNT1_L	
PCI_REQ2_L	PCI_55S	PCI	PCI REQ2_L	23A4 23B6
PCI_GNT2_L	PCI_55S	PCI	PCI GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	23A4 23A8
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	23A4 23A8
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	23A4 23A8
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	23A4 23A8 37A5
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	23A4 23A6
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	23A4 23A6
PCIE_E_R2D	PCIE_100D	PCIE	PCIE_E_R2D_C_P	33B5 33B6
	PCIE_100D	PCIE	PCIE_E_R2D_C_N	33B5 33B6
PCIE_E_D2R	PCIE_100D	PCIE	PCIE_E_D2R_P	33B5
	PCIE_100D	PCIE	PCIE_E_D2R_N	33B5 33C5
GLAN_COMP			GLAN_COMP	22C6
ENET_LAN	LAN_55S	ENET_LAN	LAN_RSTSYNC	
ENET_LAN	LAN_55S	ENET_LAN	LAN_R2D<2..0>	
ENET_LAN	LAN_55S	ENET_LAN	LAN_D2R<2..0>	
ENET_GLAN_CLK	LAN_55S	ENET_CLK	ENET_GLAN_CLK_R	
	LAN_55S	ENET_CLK	ENET_GLAN_CLK	
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>	34B8 36B7
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	34B8 36B7
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>	34B8 36C7
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	34B8 36C7
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>	34B8 36B7
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	34B8 36C7
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>	34B8 36C7
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	34B8 36C7
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	15A3 24C3
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	15A3 24C3
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	15A3 24C3
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_CLK	24C3
CLINK_WLAN	CLINK_55S	CLINK	CLINK_WLAN_DATA	24C3
CLINK_WLAN_RESET_L	CLINK_55S	CLINK	CLINK_WLAN_RESET_L	24D5
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	15A4
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	24C3
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	24C3

SB Constraints (2 of 2)

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE	SHT	OF
NONE	104	106

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	?
CLK_PCIE	*	20 MIL	?
CLK_MED	*	20 MIL	?
CLK_SLOW	*	10 MIL	?

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	6C7 28C4 29D6
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	6C7 28C4 29D6
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	6C7 28C4 29D6
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	6C7 28C4 29D6
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	6C7 28C4 29D6
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	6C7 28C4 29D6
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK	28B8 29B6
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	6C7 28B6 29B6
CK505_PCI1	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	28B6 29B6
CK505_PCI2	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	8C4 28B6
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	28B6 29A6
CK505_PCI4	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	8C4 28B6
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_FCTSEL1	28B6 29B2
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_USB48_FSA	28A4 29D8
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_CLK14P3M_TIMER	28A4 29D8
CK505_DOT96	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	6C7 28A4 29B6
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	6C7 28A4 29B6
CK505_LVDS	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	6C7 28B4 29C6
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	6C7 28B4 29C6
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	6C7 28B4 29C6
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	6C7 28B4 29C6
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	6C7 28B4 29C6
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	6C7 28B4 29C6
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	6C7 28B4 29C6
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	6C7 28B4 29C6
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	6C7 28B4 29C6
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	6C7 28B4 29B6
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	6B7 28A4 29B6
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	6B7 28A4 29B6
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9B6 29D3
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9B6 29D3
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	13B3 29D3
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	13B3 29D3
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	70A3
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	70A3
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	6C2 29B3 46C4
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	23A6 29A5 29B3
(CK505_PCI1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_FW	29A5 29B3 37A5
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	29A3 29A5 44C8
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	24D3 29A5 29D6
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	24D3 29A5 29D6
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	29C8 29D6
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	29A8 29D6
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_P	8B1 29B3
(CK505_DOT96)	CLK_PCIE_100D	CLK_PCIE	NB_CLK96M_DOT_N	8B1 29B3
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_P	8B1 29C3
(CK505_LVDS)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_DPLLSS_N	8A1 29C3
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	23C2 29C3
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	23D2 29C3
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	22B6 29C3
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	22B6 29C3
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	15C3 29C3
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	15C3 29C3
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	29C3 33C5
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	29B3 33C5
			CK505 SRC7 is project-specific	
			CK505 SRC8 is project-specific	

Clock Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7559	S

SCALE: NONE SHT 105 OF 106

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW	*	=2:1_SPACING	?
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
FW_D_CTL	FW_55S	FW	FW_LINK<7..0>
FW_D_CTL	FW_55S	FW	FW_CTL<1..0>
FW_LCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_LCLK
	CLK_MED_55S	CLK_MED	CLKFW_PHY_LCLK
FW_PCLK	CLK_MED_55S	CLK_MED	CLKFW_LINK_PCLK
	CLK_MED_55S	CLK_MED	CLKFW_PHY_PCLK
FW_LKON	FW_55S	FW	FW_LKON
	FW_55S	FW	FW_LKON_R
FW_LPS	FW_55S	FW	FW_LPS
FW_LREQ	FW_55S	FW	FW_LREQ
FW_PINT	FW_55S	FW	FW_PINT
FWPHY_CLK98P304M_XI	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI_R
	CLK_MED_55S	CLK_MED	CLK98P304M_FW_XI
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_P
FW_0_TPA	FW_110D	FW_TP	FW_0_TPA_N
FW_0_TPB	FW_110D	FW_TP	FW_0_TPB_P
	FW_110D	FW_TP	FW_0_TPB_N
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_P
FW_1_TPA	FW_110D	FW_TP	FW_1_TPA_N
FW_1_TPB	FW_110D	FW_TP	FW_1_TPB_P
	FW_110D	FW_TP	FW_1_TPB_N

Port 2 Not Used

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	47D2
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	47D2
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	68Z 47C5
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	68Z 47C5
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	47D5
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	47D5
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	47C2
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	47C2
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	47B2
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	47B2

FireWire & SMC Constraints

SYNC_MASTER=WFERRY SYNC_DATE=06/12/2006

APPLE INC.

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SCALE NONE | SHT 106 OF 106