### BOM Groups

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<td>338S0600</td>
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<td>335S0610</td>
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### Module Parts

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<td>M97_COMMON,CPU_2_4GHZ</td>
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<td>CPU_2_4GHZ</td>
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<td>CPU_2_0GHZ</td>
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### Programmable Parts

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<tr>
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<td>IC,RTL8211CL,GIGE TRANSCEIVER,48P,TQFP</td>
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<td>IC,CY7C63833,ENCORE II,USB CONTROLLER</td>
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<td>IC,PSOC+ W/ USB,56 PIN,MLF,CY8C24794</td>
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<td>PDC,SLB4N,PRQ,2.4,25W,1066,M0,3M,BGA</td>
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<td>PDC,QDYD,QS,2.26,25W,1066,M0,3M,BGA</td>
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<td>PDC,QJGL,QS,2.0,25W,1066,M0,3M,BGA</td>
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<td>IC,FLASH,SPI,32MBIT,3.3V,86MHZ,8-SOP</td>
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<td>IC,GMCP,MCP79,35X35MM,BGA1437,A01Q</td>
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<td>PDC,QDYJ,QS,2.4,25W,1066,M0,3M,BGA</td>
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<td>IC,PRGRM,EFI BOOTROM,UNLOCK,M97</td>
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<td>IC,SMC,HS8/2117,9X9MM,TLP,HF</td>
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<td>IC,IR CONTROLLER,M97</td>
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<td>IC,GMCP,MCP79,35X35MM,BGA1437,A01Q</td>
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### Alternate Parts

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### M97 BOARD STACK-UP

#### Top

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>2</th>
<th>GROUND</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIGNAL(High Speed)</td>
<td>3</td>
<td>GROUND</td>
</tr>
<tr>
<td>SIGNAL(High Speed)</td>
<td>4</td>
<td>GROUND</td>
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</table>

#### Bottom

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>9</th>
<th>SIGNAL(High Speed)</th>
</tr>
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<td>SIGNAL(High Speed)</td>
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<td>SIGNAL(High Speed)</td>
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<th>CRITICAL</th>
<th>ONEWIRE_PU</th>
<th>BKLT_PLL_NOT</th>
<th>DP_ESD</th>
<th>ENG_BMON</th>
<th>MIKEY</th>
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<td>U5701</td>
<td>U6100</td>
<td>U1400</td>
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### Notes

- Preliminary
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![Diagram](www.laptop-schematics.com)
1.05V TO 3.3V LEVEL TRANSLATOR (M97: ON ICT FIXTURE)

From XDP connector
U1000 CPU
To XDP connector and/or level translator.

From XDP connector
or via level translator
U1400 MCP

To XDP connector

JTAG_MCP_TDI
JTAG_MCP_TCK
JTAG_MCP_TMS
JTAG_MCP_TDO
JTAG_MCP_TDO_CONN
JTAG_MCP_TRST_L

XDP_TDI
XDP_TDO
XDP_TDO_CONN
XDP_TRST_L
XDP_TMS
XDP_TCK

JTAG_LVL_TRANS_EN_L

Preliminary
"S0, S0M" RAILS

"S3" RAILS

"G3H" RAILS

"S5" RAILS

"ENET" RAILS

PEX & SATA AVDD/VDVI D aliases

Power Aliases

SCALE

SHT

www.laptop-schematics.com
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CHANGE C1240-C1243 AND C1260 FROM 128S0241(9 MILLI-OHM) TO 128S0231(6 MILLI-OHM)

SYNC FROM T18

REMOVE NO STUFF CAPS C1220 TO C1231

REMOVE C1244 & C1245

PLACEMENT NOTE (C1200-C1219):
1x 10uF, 1x 0.01uF
Place on secondary side.
Place inside socket cavity on secondary side.

VCCA (CPU AVdd) DECOUPLING
1x 330uF, 6x 0.1uF 0402

VCCP (CPU I/O) DECOUPLING

SYNC_DATE=03/31/2008

CPU Decoupling

APPLE INC.

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I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

www.laptop-schematics.com
SYNC FROM T18
CHANGE STANDARD XDP CONNECTOR TO SMALLER ONE 516S0625
RENAME JTAG_MCP_TDO TO JTAG_MCP_TDO_CONN
RENAME XDP_TDO TO XDP_TDO_CONN
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

<table>
<thead>
<tr>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

#### PCI EXPRESS

- PEG_PRESENT_L
- PE0_RX6_N
- PE0_RX3_N
- PE0_RX11_P
- PE0_TX14_P
- PE0_TX12_N
- PE0_TX11_N
- PE0_TX9_N
- PE0_TX7_P
- PE0_TX1_P
- PE1_TX1_N
- PEX_RST0#
- +AVDD0_PEX5
- +AVDD0_PEX1
- PE0_TX10_P
- PE0_TX8_P
- PE0_TX1_P
- PE0_TX10_P

#### MCP PCIe Interfaces

- TP_PCIE_CLK100M_PE5N
- TP_PCIE_CLK100M_PE5P
- TP_PCIE_PE4_R2D_CN
- PCIE_EXCARD_R2D_C_P

---

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Apple Inc.
3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.

MCP_SAFE_MODE SIGNAL TO SUPPORT ROM FAILURE OVERRIDE

Preliminary
NOTE: If CPU_VLD deasserts during S0, MCP79 will take system to S5 immediately.

This results in earlier ROMSIP and MCP FSB I/O interface initialization.

CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

MCPSEQ_MIX is cross between MLB and internal power sequencing, which VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPU_VDD_EN (which is 40-100ms after PS_PWRGD assertion).

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Sync from T18
Change reset button to reset pads
Remove unused PCIe reset signals
Remove R2824 and net PCI_CLK33M_SLOT_A
Change RTC coin cell to LDO & supercap
Alias MEM_VTEN to -DDRVTEN
Change Y2810 and U2850 to smaller parts

Platform reset connections
LPC Reset (Unbuffered)

RTC power sources

RTC crystal

MCP 25MHz crystal

MCP S0 PWRGD & CPU_VLD

Reset button

Sync from T18
Change reset button to reset pads
Remove unused PCIe reset signals
Remove R2824 and net PCI_CLK33M_SLOT_A
Change RTC coin cell to LDO & supercap
Alias MEM_VTEN to -DDRVTEN
Change Y2810 and U2850 to smaller parts
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TP55116 regulator.
DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MEM# rails are not powered in sleep.

DDR3 Reset Support

1) To prevent the incorrect generation of signal to avoid glitch on MEM_RESET_L.

Before 1.5V starts to rise to 3.3V input must be stable before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

MCP79 cannot control this signal directly since it must be high in sleep and MEM# rails are not powered in sleep.
ENET_RESET_L IS NOT ASSERTED WHEN WOL IS ACTIVE.
HENCE, RC (C3725 AND R3725) ARE NOT STUFFED.

IN ENET_CLK125M_TXCLK

PLACE R3796 CLOSE TO U1400, PIN D24
IN ENET_RESET_L

(19mA typ - Energy Detect)
(43mA typ - 1000base-T)

R3725
2.49K
1/16W
5%

R3795
R3793
22
22
22
22
22
1 2
1 2
1 2
1 2
1 2
1 2

1/16W
402
1%

C3705
C3700
0.1UF
10V

C3706
C3701
0.1UF
X5R
16V
10%

CERM
402
50V

CRITICAL

BI
BI
BI
BI
BI
BI

BI
BI
BI
BI
BI
BI

C3710
C3711
0.1UF
0.1UF

C3716

16V
10%

AVDD33

15
MANAGEMENT

RESET

CRITICAL

16V

GND

41

45

36

35

34

33

12

11

9

4

2

1

2

1

1

2

1

8B1

AVDD12

10%

AVDD12

10%

FERR-120-OHM-1.5A

R3750
4.7K
402

X5R

4.7K

MF-LF

1/16W

AVDD12

16V

10%

16V

10%

X5R

X5R

1/16W

MF-LF

1/16W

MF-LF

1/16W

MF-LF
WLAN Enable Generation

NOTE: 21C3 is guaranteed by 23 pull up or open-drain 82_PM4B9 signal.

NOTE: 21C3 is guaranteed by 23 pull up or open-drain 82_PM4B9 signal.

1.05V ENET FET

NOTE: 18C3 can provide 25MHz clock. See clock notes elsewhere. 82_PM4B9 is preserved.

NOTE: 18C3 can provide 25MHz clock. See clock notes elsewhere. 82_PM4B9 is preserved.

RTL8211 25MHz Clock

NOTE: 25MHz clock can be 25MHz clock. See clock notes elsewhere. 82_PM4B9 is preserved.

NOTE: 25MHz clock can be 25MHz clock. See clock notes elsewhere. 82_PM4B9 is preserved.
NOTE: Unused pins have "SMC_Pxx" names.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

NOTE: P94 and P95 are shorted, P95 could be spare.

SMC_PB3:

SMC_TX_L

LPC_AD<3>

LPC_AD<1>

ALS_LEFT

ALS_RIGHT

LPC_FRAME_L

LPC_SERIRQ

SMS_ONOFF_L

SMS_Z_AXIS

SMS_Y_AXIS

SMS_X_AXIS

LPC_CLK33M_SMC

IMVP_VR_ON

SMC_FAN_2_TACH

SMC_FAN_1_TACH

SMC_FAN_0_TACH

SMC_GFX_OVERTEMP_L

SMC_ANALOG_ID

SMC_FAN_2_CTL

SMC_EXCARD_CP

SMC_EXCARD_PWR_EN

SMC_ADAPTER_EN

SMC_KBC_MDE

SMC_ODD_DETECT

SMC_NDB_DDR_ISENSE

SMC_NB_CORE_ISENSE

SMC_NB_DDR_ISENSE

SMC_PBUS_VSENSE

SMC_GPU_VSENSE

SMC_GPU_ISENSE

PM_SLP_S5_L

PM_CLKRUN_L

SMB_A_S3_DATA

SMB_B_S0_CLK

SMB_A_S3_CLK

SMB_MGMT_CLK

SMC_PH2

SMC_TDO

SMC_TDI

SMC_TCK

MIN_NECK_WIDTH=0.20 MM

VOLTAGE=3.3V
DETECT FIN-STACK TEMPERATURE

REPLACED 518S0521 WITH 518S0519

Preliminary
78171-0002
CRITICAL
J5590
M-RT-SM

DETECT HEAT-PIPE TEMPERATURE

DETECT CPU DIE TEMPERATURE

DETECT MCP DIE TEMPERATURE

CPU T-Diode Thermal Sensor

MCP T-Diode Thermal Sensor

REPLACED 518S0521 WITH 518S0519

www.laptop-schematics.com
PSOC USB CONTROLLER

KEYBOARD CONNECTOR

PSOC PROGRAMMING CONNECTOR

ISOLATION CIRCUIT

SMC_MANUAL_RESET LOGIC

TPAD BUTTONS DISABLE

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

WELLSPRING 1

www.laptop-schematics.com
To detect Keyboard backlight, SMC will
BOM OPTION: KBDLED_YES
R5853 ALWAYS PRESENT
LOW = keyboard backlight present
PLACEMENT_NOTE=NEAR J5800
CRITICAL
SYM_VER-1
SM-HF
1 2
MF-LF
1/10W
603
0
4
21
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
VOLTAGE=3V3
VOLTAGE=0V
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM
7C5
48B6
8B5
48A4

SHORTING_HEADER=TOPSIDE
CRITICAL
APN 152S0504
CRITICAL
TPS61045
U5805
NO STUFF
=PP5V_S0_KBDLED
APN 353S1401
5%
402
2.2UF
603
16V
10%
1%

BOOSTER +18.5VDC FOR SENSORS
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- CHOPP CURE REDUCTION
- ADAP TO NEXT SN
- 150-250 KHZ CLEAN SPECTRUM
- Ipst, NM, CDAD ADAPTED

R5800
R5801
R5811
1%
1/16W
402
7A5
KBDLED_ANODE
MIN_NECK_WIDTH=0.25 MM
MIN_LINE_WIDTH=0.50MM

3V3 LDO FOR IPD
PP3V3_S3_LDO_R
PSOC_SCLK
PSOC_MOSI
PSOC_F_CS_L
SHT
Z2_BOOT_CFG1
Z2_HOST_INTN
Z2_CLKIN
Z2_MOSI
SYNC_DATE=05/09/2008
SYNC_MASTER=YUAN.MA
APPLD INC.
16 15
14 13
12 11
10
9
8 7

3V3 LDG FOR IPD
R5873
R5874
R5875

KEYBOARD BACKLIGHT DRIVING AND DETECTION
KBD BACKLIGHT CONNECTOR
IPD FLEX CONNECTOR
WELLSPRING 2
Digital SMS

Pull-up required if SMS_INT_L is not used.

Pull-up required if SMS_PWRDN is not used.

Desired orientation when placed on board top-side:

Analog SMS

Pull-up required if SMS_PWRDN is not used.

Desired orientation when placed on board top-side:

 поверка

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Sync Date = 05/02/2008
Sync Master = Changzheng

SPI ROM

MCP79 SPI Frequency Select

<table>
<thead>
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<th>Frequency</th>
<th>SPI_MOSI_MUX</th>
<th>SPI_CLK_MUX</th>
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<tr>
<td>42 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>25 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>32 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1 MHz</td>
<td>1</td>
<td>1</td>
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</table>
PLACE R6301, R6305, R6306, R6307, AND R6308 OUTSIDE AUDIO SECTION TO CONSERVE AUDIO AREA

<table>
<thead>
<tr>
<th>PART#</th>
<th>REFERENCE DESIGNATOR(S)</th>
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<tbody>
<tr>
<td></td>
<td>MIKEY</td>
</tr>
<tr>
<td></td>
<td>CRITICAL</td>
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5V_RT/3.3V POWER SUPPLY

VOUT = (2 * RA / RB) + 2
VOUT = (2 * RC / RD) + 2

PWM FREQ. = 300 KHZ
MAX CURRENT = 4A

PWM FREQ. = 375 KHZ
MAX CURRENT = 4A

PLACE XW7204 BY PIN 2 OF L7220.
MCP 1.05V_S5 AUXC SUPPLY

\[ V_{OUT} = 0.6V \times (1 + \frac{Ra}{Rb}) \]

MCP79 Rev A01 requires higher voltage

\[ V_{OUT} = 1.102V \]

Max Current = 1.5A

Freq = 1Mhz

Max Current = 200mA

Input Rail is 3.3V So

1.8V S0 SWITCHER

SYNC_DATE=01/23/2008
SYNC_MASTER=RAYMOND

MISC POWER SUPPLIES

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D C B A

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Display Port Interoperability spec says that sources or sinks which do both DP and DVI must depend on the external adapter for pull ups on DDC lines (since DP or sinks which do both DP and DVI has the pull option on the external adapter).
### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
<th>MEM_DQS</th>
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<th>MEM_CLK</th>
<th>MEM_CLK</th>
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<tr>
<td>MEM_DQS2MEM</td>
<td>MEM_70D_VDD</td>
<td>MEM_2OTHER</td>
<td>MEM_CTRL</td>
<td>MEM_CTRL</td>
<td>MEM_CTRL</td>
</tr>
<tr>
<td></td>
<td>MEM_DATA</td>
<td>MEM_CMD</td>
<td>MEM_DATA2MEM</td>
<td>MEM_DQS</td>
<td>MEM_DQS</td>
</tr>
<tr>
<td>SPACING_RULE_SET</td>
<td>SPACING_RULE_SET</td>
<td>SPACING_RULE_SET</td>
<td>SPACING_RULE_SET</td>
<td>SPACING_RULE_SET</td>
<td>SPACING_RULE_SET</td>
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<td>MEM_DQS</td>
<td>MEM_DQS</td>
<td>MEM_DATA</td>
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<td>MEM_DQS</td>
<td>MEM_DQS</td>
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### Memory Net Properties

<table>
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<tr>
<th>DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.</th>
<th>DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.</th>
</tr>
</thead>
<tbody>
<tr>
<td>All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).</td>
<td>DDR3: DDR2:</td>
</tr>
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### Memory Constraints

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<tr>
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<th>MEM_B_DQS7</th>
<th>MEM_B_DQS6</th>
<th>MEM_B_DQS5</th>
<th>MEM_B_DQS4</th>
<th>MEM_B_DQS3</th>
<th>MEM_B_DQS2</th>
<th>MEM_B_DQS1</th>
<th>MEM_B_DQS0</th>
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<tbody>
<tr>
<td>MEM_B_CNTL</td>
<td>MEM_B_CLK</td>
<td>MEM_B_DQ&lt;15..8&gt;</td>
<td>MEM_B_DQS_P&lt;2&gt;</td>
<td>MEM_B_DQS_N&lt;1&gt;</td>
<td>MEM_B_DQS_N&lt;0&gt;</td>
<td>MEM_B_DQS_P&lt;1&gt;</td>
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<td>MEM_B_DQ&lt;14..8&gt;</td>
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<tr>
<td>MEM_A_DQ_BYTE7</td>
<td>MEM_70D</td>
<td>MEM_A_DQ_BYTE6</td>
<td>MEM_A_DQ_BYTE5</td>
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<td>MEM_A_CMD</td>
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Digital Video Signal Constraints

SATA Interface Constraints

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

**Digital Video Signal Constraints**

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<tr>
<th>Source</th>
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<th>Cryptic</th>
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**SATA Interface Constraints**

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### Table: Physical Rules

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<th>Minimum Line Width</th>
<th>Allow Route on Layer?</th>
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### Table: Physical Rules

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<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
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### Table: Physical Rule Set

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### Table: Physical Rule Item

<table>
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### Table: M97 Sensor Net Properties

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<th>Spacing</th>
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### Table: M97 Special Constraints

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<th>MCPTHMSNS_D2_P</th>
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### Table: M97 Special Constraints

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### Table: M97 Special Constraints

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<th>44A8</th>
<th>21C3</th>
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