3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.
### BOM Configuration

#### BOARD STACK-UP

<table>
<thead>
<tr>
<th>TOP SIGNAL</th>
<th>BOTTOM SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

#### BOARD GROUPS

**CPU**

- **BOM NUMBER**: 607-4701
- **BOM GROUPS**
  - **CPUS**
  - **BOTTOM BOARD STACK-UP**
  - **TOP**

#### CRITICAL BOM OPTION

- **TABLE_5_ITEM**
  - **REFERENCE DESIGNATOR(S)**
  - **TABLE_BOMGROUP_ITEM**
  - **BOM OPTIONS**
  - **TABLE_5_ITEM**
  - **R5400**
  - **L7530**
  - **MSQ-1211-1R5L-F**

#### COMMON

- **PART#**
  - **152-0105**
  - **132S0082**
  - **132S0205**
  - **338S0570**
  - **511S0038**

- **DESCRIPTION**
  - **CONN, INTEL SKT-P, BGA, 26X26-479**
  - **EFI ROM, K50A/K51A/K50E**
  - **PCB, FAB, MLB, K50, HF**
  - **CAP, CER, 0.068UF, 10%, 10V, 0402**
  - **IC, FW643-06, 1394B, REV-E**
  - **CAP, CER, 270PF, 10%, 50V, 0402**
  - **RES, 7.87K, 0402, 1%, 1/16W, LF**

- **USE 20MOHM AS 0R**
  - **U1000**
  - **U4100**
  - **U1400**

#### TABLE_5_HEAD

- **20_INCH_LCD**
- **MCP_B02**

---

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

II NOT TO REPRODUCE OR COPY IT

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
CPU FSB Frequency Straps

NOTE: () values not supported by MCP79.

Merom/Penryn do not officially support PECI, but it’s not clear whether PECI interface is present or not. T12 used pin F6.

Extra FSB Pull-ups

Exist in SSE but not Intel designs. Here for CYA.

Extra FSB Pull-ups

Exist in SSE but not Intel designs. Here for CYA.

Debug: CPU

CPU FSB Frequency Straps

NOTE: () values not supported by MCP79.

Merom/Penryn do not officially support PECI, but it’s not clear whether PECI interface is present or not. T12 used pin F6.

Extra FSB Pull-ups

Exist in SSE but not Intel designs. Here for CYA.

Debug: CPU
Page Notes

MEM A VREF SQ  MEM A VREF CA  MEM B VREF SQ  MEM B VREF CA  CPU FIB VREF

<table>
<thead>
<tr>
<th>DAC channel</th>
<th>A</th>
<th>B</th>
<th>A</th>
<th>B</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min DAC code</td>
<td>0x67</td>
<td>0x67</td>
<td>0x67</td>
<td>0x67</td>
<td>0x55</td>
</tr>
<tr>
<td>Vref Stepping</td>
<td>6.5 mV</td>
<td>6.5 mV</td>
<td>6.5 mV</td>
<td>6.5 mV</td>
<td>11.2 mV</td>
</tr>
<tr>
<td>Nominal Vref</td>
<td>0.75 V</td>
<td>0.75 V</td>
<td>0.75 V</td>
<td>0.75 V</td>
<td>0.70 V</td>
</tr>
<tr>
<td>Min Vref</td>
<td>0.375 V</td>
<td>0.375 V</td>
<td>0.375 V</td>
<td>0.375 V</td>
<td>0.091 V</td>
</tr>
<tr>
<td>Max source I</td>
<td>5 mA</td>
<td>5 mA</td>
<td>5 mA</td>
<td>5 mA</td>
<td>0.52 mA</td>
</tr>
<tr>
<td>Max sink I</td>
<td>-3.75 mA</td>
<td>-3.75 mA</td>
<td>-3.75 mA</td>
<td>-3.75 mA</td>
<td>-0.91 mA</td>
</tr>
</tbody>
</table>

DAC channel:

- A
- B
- A
- B
- C

Max DAC code:

- 0x87
- 0x87
- 0x87
- 0x87
- 0x55

Vref Stepping:

- 6.5 mV
- 6.5 mV
- 6.5 mV
- 6.5 mV
- 11.2 mV

Nominal Vref:

- 0.75 V
- 0.75 V
- 0.75 V
- 0.75 V
- 0.70 V

Min Vref:

- 0.375 V
- 0.375 V
- 0.375 V
- 0.375 V
- 0.091 V

Max source I:

- 5 mA
- 5 mA
- 5 mA
- 5 mA
- 0.52 mA

Max sink I:

- -3.75 mA
- -3.75 mA
- -3.75 mA
- -3.75 mA
- -0.91 mA

Note:

- SO-DIMM A and SO-DIMM B Vref settings should be margin separately
  (i.e. not simultaneously) due to current limitation of TP55116 regulator.

- VREFMRGN

- PLACE close to U1000.1D
- PLACE close to J3100.1
- PLACE close to J3200.1
- PLACE close to J3100.1
- PLACE close to J3100.126
- PLACE close to J3200.1
- PLACE close to J3100.1
- PLACE close to J3100.126
- PLACE close to J3200.1

Required zero ohm resistors when no VREF margining circuit stuffed

<table>
<thead>
<tr>
<th>Type</th>
<th>Description</th>
<th>Resistor Required</th>
<th>Voltage</th>
<th>Value</th>
<th>Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTICE OF PROPRIETARY PROPERTY

The information contained herein is the property of Apple Inc. and is to be used only in connection with our products. No portion of this document may be reproduced or transmitted in any form without the express written permission of Apple Inc.
CAPS TO COUPLE MCP 1V5_S0_MEM AND DIMMS 1V5_S3

CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM A (FURTHER FROM MCP)

CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM B (CLOSER TO MCP)

EXTRA DECOUPLING CAPS FOR MCP MEM RAIL

MEMORY COUPLING CAPS

www.laptop-schematics.com
DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and the MEM rail is not powered in sleep.

3.3V input must be stable before 1.5V starts to rise to avoid glitch on MEM_RESET_L.
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE

NOTICE OF PROPRIETARY PROPERTY

PORT 0
1394B

12 VOLTS
7 WATTS MAX PER PORT

"Snapback" & "Late VG" Protection

ESD Rail

IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1
CAMERA POWER FILTERING

K37L (BLUETOOTH) CONNECTOR

CAMERA CONNECTOR

IR RECEIVER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:
I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE
SMC_PB3:

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
Alternate SPI ROM Support

SPI Bus Series Resistance Option

MCP79 Internal SPI MUX Support

LPC+SPI Debug Connector
REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)

CPU T-Diode Thermal Sensor

DIGITAL LCD TEMP SENSOR

REMOTE THERMAL SENSORS

PLACE SNS_T_DN4_DP5

PLACE SNS_T_DP4_DN5

PLACE SNS_T_DN1_DP6

PLACE SNS_T_DP2_DN3

PLACE SNS_T_DP1_DN6

SIGNAL_MODEL=EMPTY

DIFFERENTIAL_PAIR=SNS_T3

DIFFERENTIAL_PAIR=SNS_T1

=PP3V3_S0_MCPTHMSNS

FERR-220-OHM

0402

21C3

VOLTAGE=3.3V

CERM

50V

10%

5%

1/16W

MF-LF

0.0022UF

L5513

L5512

R5538

0402

L5536

SIGNAL_MODEL=EMPTY

DIFFERENTIAL_PAIR=SNS_T3

0402

1UF

X5R

10V

21

1

1/16W

MF-LF

0.0022UF

C5501

GND

5%
FROM COMPARATOR

PPDDR REGULATOR HAS NOT COME UP, PPDDR REGULATOR HAS NOT COME UP.

PLACE SHORTS CLOSE TO PLANE CUTS

PART# HYSTERESIS NUMBERS CALCULATED BASED ON OUTPUT PULL UP OF 3.3V

DESCRIPTION

REFERENCE DESIGNATOR(S)

ENABLE FET

ENABLE REGULATOR

DELAY OF ~16MS FROM PM_SLP_S3_L

PM_MXM_PGOOD IS OPEN DRAIN SIGNAL, IT'S PULLED UP TO ALL_SYS_PWRGD

CAN I USE ALIAS OR DO I NEED INLINE RESISTOR?

PM_MXM_PGOOD IS PULLED UP TO IT AND GATE BY THE FACT THAT

PLACE RESISTORS CLOSE TO U7020

R7098

IRF6402

IRF7410

1.6A

5.8A

8.8A

13A

SYNC_DATE=01/07/2009

REV. D

SCALE

D C B A

NOTE: TO PRODUCE THE DOCUMENT IN CONFORMITY TO THE

TABLE_5_HEAD

OUT

OUT

OUT

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

AGREES TO THE FOLLOWING

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

PROPERTY OF INTEL CORPORATION, AND ITS USE OR DISSEMINATION

IS LIMITED TO THE CONTENT OF THIS DOCUMENT.

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
1.5 V DDR SUPPLY

PPDDR_S3_REG
VOUT = 1.5V
PEAR = 34.73A
AVG = 8.33A

PPVTT_S0_DDR_LDO
PPVTT_S3_DDR_BUF
TP_PGOOD_DDRREG_S3
=DDRREG_EN
DDRVTT_EN

LO
HI ON
S3
S5

C7560
CERM-X5R
ON
OFF OFF
6.3V
20%
1

VTTREF
ON
OFF

C7550
CERM-X5R
6.3V
603
1

1.5 V DDR SUPPLY

CAUTION: THIS DRAWING IS PROVIDED FOR REFERENCE ONLY. IT IS NOT TO BE USED IN CONSTRUCTION OR PRODUCTION. IT IS PROPRIETARY AND CONFIDENTIAL. APPRECIATION IS EXPRESSED TO THE RECIPIENT OF THIS DOCUMENT.

PEAK  = 14.75A
VOUT  = 1.5V
PPDDR_S3_REG

330UF-0.009OHM

R7562
0.499
1000PF
402
NP0-C0G

L7530
20%
MCP 1.05V_S5 AUXC SUPPLY

VOUT = 0.6V * (1 + Ra / Rb)

VOUT = 1.05V

MAX Current = 1.5A

FREQ = 1Mhz
PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

R9124
R9125

R9124
R9125

R9124
R9125
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

Intel Design Guide recommends FSB signals be routed only on internal layers.
Memory Bus Constraints

- **A/BA/cmd signals** should be matched within 5 ps of CLK pairs.
- **All DQS pairs** should be matched within 100 ps of clocks.
- **DQ signals** should be matched within 5 ps of associated DQS pair.

**SPACING_RULE_SET**

```
NET_SPACING_TYPE1 NET_SPACING_TYPE2
NET_SPACING_TYPE1 NET_SPACING_TYPE2
MEM_CTRL2CTRL
MCP_MEM_COMP
MEM_CLK2MEM
MEM_70D_VDD
MEM_70D
MEM_CTRL
MEM_CLK
```

**Area Type**

```
MINIMUM LINE WIDTH
```

**Layer**

```
LAYER
LAYER
LAYER
LAYER
LAYER
```

**Weight**

```
WEIGHT
```

**Allow Route**

```
=3:1_SPACING
```

**Table Spacing Rule Item**

```
TABLE_SPACING_RULE_ITEM
TABLE_SPACING_ASSIGNMENT_ITEM
TABLE_SPACING_ASSIGNMENT_ITEM
TABLE_SPACING_ASSIGNMENT_ASSIGNMENT_ITEM
```

**Electrical Constraint Set**

```
ELECTRICAL_CONSTRAINT_SET
```

**Property of Apple Computer, Inc. The Possessor Notice of Proprietary Property**

**Memory Net Properties**

**Memory Bus Spacing Group Assignments**

** MCP MEM COMP Signal Constraints**
MCP Constraints 1

SOURCE: MCP Interface DG (DG-03328-001_v0D), Section 2.7.1.

SATA Interface Constraints

PCIE

SPACING RULE SET

CLK_PCIE_100D = 100_OHM_DIFF = 100_OHM_DIFF

MCP_PEX_COMP

CLK_PCIE

PCIE_90D

SATA

PCIE

SIZE

NONE

DRAWING NUMBER

SHT

109102

A

C

B

D
**RTL8211CLGR (ETHERNET PHY) CONSTRAINTS**

**MCP RGMII (Ethernet) Constraints**

**SOURCE:** MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

**SPANING RULE SET**

- ENET_MDI_100D
- MCP_BUF0_CLK
- ENET_MII_55S
- MCP_MII_COMP

**LINE-TO-LINE SPACING**

<table>
<thead>
<tr>
<th><strong>SPACING</strong></th>
<th><strong>RULE</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.6 MM</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

**DIFFPAIR NECK GAP**

<table>
<thead>
<tr>
<th><strong>GAP</strong></th>
<th><strong>RULE</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0.2 MM</td>
<td>STAND</td>
</tr>
</tbody>
</table>

**MAXIMUM NECK LENGTH**

<table>
<thead>
<tr>
<th><strong>LENGTH</strong></th>
<th><strong>RULE</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>STAND</td>
</tr>
</tbody>
</table>

**DIFFPAIR PRIMARY GAP**

<table>
<thead>
<tr>
<th><strong>GAP</strong></th>
<th><strong>RULE</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>STAND</td>
</tr>
</tbody>
</table>

**PHYSICAL RULE SET**

- ENET_MDI
- ENET_TXD
- ENET_TXCLK
- ENET_RXCLK
- ENET_MDI_100D
- ENET_MII_55S
- MCP_MII_COMP
- MCP_BUF0_CLK

**SCALE SIZE FIT:**

- A
- B
- C
- D

**SYNC DATE:** 01/07/2009
## FireWire Interface Constraints

<table>
<thead>
<tr>
<th>Port</th>
<th>Voltage</th>
<th>Current</th>
<th>Clock</th>
<th>Clock Spread</th>
<th>Clock Phase</th>
<th>Clock Skew</th>
<th>Data 1</th>
<th>Data 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port 1</td>
<td>1.2 V</td>
<td>20 mA</td>
<td>50 MHz</td>
<td>0.5 ns</td>
<td>1.0 ns</td>
<td>0.1 ns</td>
<td>1.0 A</td>
<td>1.0 A</td>
</tr>
<tr>
<td>Port 2</td>
<td>3.3 V</td>
<td>15 mA</td>
<td>48 MHz</td>
<td>0.4 ns</td>
<td>0.9 ns</td>
<td>0.1 ns</td>
<td>1.5 A</td>
<td>1.5 A</td>
</tr>
</tbody>
</table>

## FireWire Net Properties

<table>
<thead>
<tr>
<th>Net</th>
<th>SPACING</th>
<th>NET_TYPE</th>
<th>Layer</th>
<th>Min Width</th>
<th>Max Length</th>
<th>Gap</th>
<th>Neck Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>FW_0_TPB</td>
<td>0.1 mm</td>
<td>1.0 mm</td>
<td>P</td>
<td>0.1 mm</td>
<td>0.5 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>FW_TP</td>
<td>0.1 mm</td>
<td>1.0 mm</td>
<td>P</td>
<td>0.1 mm</td>
<td>0.5 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>FW_PORT0_TPB_P</td>
<td>0.1 mm</td>
<td>1.0 mm</td>
<td>P</td>
<td>0.1 mm</td>
<td>0.5 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>FW_PORT0_TPB_N</td>
<td>0.1 mm</td>
<td>1.0 mm</td>
<td>P</td>
<td>0.1 mm</td>
<td>0.5 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>FW_PORT0_TPA_P</td>
<td>0.1 mm</td>
<td>1.0 mm</td>
<td>P</td>
<td>0.1 mm</td>
<td>0.5 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
</tr>
<tr>
<td>FW_PORT0_TPA_N</td>
<td>0.1 mm</td>
<td>1.0 mm</td>
<td>P</td>
<td>0.1 mm</td>
<td>0.5 mm</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
</tr>
</tbody>
</table>

## FireWire Constraints

- Port 1 & 2 NOT USED
- * = 3:1 SPACING
- FW_TP
- FW_PORT0_TPB_P
- FW_PORT0_TPB_N
- FW_PORT0_TPA_P
- FW_PORT0_TPA_N
- FW_0_TPB
- FW_TP
- FW_110D
- FW_PORT0_TPA_N
- FW_0_TPB
- FW_TP
- FW_PORT0_TPA_P
- FW_110D

---

The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. Not to reproduce or copy it
II. Not to reveal or publish in whole or part
III. To maintain the document in confidence

Notices of Proprietary Property

This information is the property of Apple Computer, Inc. and is protected by copyright and confidentiality agreements. It is not to be reproduced or published in whole or part without the express written consent of Apple Computer, Inc.
Digital Video Signal Constraints

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

GRAPHICS CONSTRAINTS

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

NET_TYPE

GRAPHICS CONSTRAINTS

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.
**PCI, LPC, SMB, HDA, SPI, RGMII, SMBUS ARE ROUTED AS 55 OHM SE SIGNALS**

**K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS**

<table>
<thead>
<tr>
<th>SPACING RULE SET</th>
<th>CLK_SPACING_0.6MM</th>
<th>1:1_DIFFPAIR</th>
<th>110_OHM_DIFF</th>
<th>4:1_SPACING</th>
<th>3:1_SPACING</th>
<th>2:1_SPACING</th>
<th>90_OHM_DIFF</th>
<th>90_OHM_DIFF</th>
<th>70_OHM_DIFF</th>
<th>70_OHM_DIFF</th>
<th>27P4_OHM_SE</th>
</tr>
</thead>
</table>

- **STANDARD**
- **DEFAULT**

<table>
<thead>
<tr>
<th>8 7 6 5 4 3 2 1</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP, BOTTOM</td>
</tr>
</tbody>
</table>

- **ISL3, ISL6**

<table>
<thead>
<tr>
<th>LAYER</th>
</tr>
</thead>
<tbody>
<tr>
<td>LAYER</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TABLE_SPACING_RULE_HEAD</th>
<th>TABLE_SPACING_RULE_ITEM</th>
</tr>
</thead>
<tbody>
<tr>
<td>LINE-TO-LINE SPACING allow route on layer?</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>Y</td>
<td>Y</td>
</tr>
</tbody>
</table>

- **MINIMUM LINE WIDTH**
  - **STANDARD**
  - **0.085 MM**
  - **0.085 MM**
  - **0.099 MM**

- **MAXIMUM NECK LENGTH**
  - **STANDARD**
  - **0.1 MM**

- **DIFFPAIR PRIMARY GAP**
  - **0.400 MM**
  - **0.320 MM**
  - **0.240 MM**
  - **0.160 MM**
  - **0.150 MM**

- **MINIMUM NECK WIDTH**
  - **STANDARD**
  - **0.085 MM**
  - **0.085 MM**
  - **0.085 MM**
  - **0.085 MM**
  - **0.085 MM**
  - **0.085 MM**

- **AREA TYPE**
  - **BGA_P2MM**
  - **BGA_P1MM**

- **DRAWING NUMBER**
  - **051-7973**

- **SCALE**
  - **A**

- **SYNC MASTER**
  - **K50**

- **NOT TO REVEAL OR PUBLISH IN WHOLE OR PART**

- **NOT TO REPRODUCE OR COPY IT**

- **AGREES TO THE FOLLOWING**

- **APPENDIX INC.**