### Bar Code Label / EEE #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>REFERENCE ORG</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AS-5523</td>
<td>PCBA,MLB,2.13GHZ,MI 2GB,HY 2GB,SS CAP,M96A</td>
<td>CRITICAL</td>
<td>BOM_5523</td>
</tr>
<tr>
<td>AS-5524</td>
<td>PCBA,MLB,1.86GHZ,HY 2GB,SS CAP,M96A</td>
<td>CRITICAL</td>
<td>BOM_5524</td>
</tr>
<tr>
<td>AS-5525</td>
<td>PCBA,MLB,1.83GHZ,M96A_COMMON,M96A_MICRON,M96A_MU_CAP,CPU_2_13GHZ</td>
<td>CRITICAL</td>
<td>BOM_5525</td>
</tr>
<tr>
<td>AS-5526</td>
<td>PCBA,MLB,1.86GHZ,HYNIX,TY 2GB,SS CAP,M96A</td>
<td>CRITICAL</td>
<td>BOM_5526</td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>338S0563</td>
<td>IC,GMCP,MCP79U-A01Q,27MMX27MM,BGA1588</td>
<td>CRITICAL</td>
<td>BOM_338S0563</td>
</tr>
<tr>
<td>338S0637</td>
<td>IC,GMCP,MCP79U-B01,27MMX27MM,BGA1588</td>
<td>CRITICAL</td>
<td>BOM_338S0637</td>
</tr>
<tr>
<td>338S0604</td>
<td>IC,GMCP,MCP79U-B02,27MMX27MM,BGA1588</td>
<td>CRITICAL</td>
<td>BOM_338S0604</td>
</tr>
<tr>
<td>333S0475</td>
<td>IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M96</td>
<td>CRITICAL</td>
<td>BOM_333S0475</td>
</tr>
<tr>
<td>335S0615</td>
<td>MICRON,DDR3,128M16,9x11.5</td>
<td>CRITICAL</td>
<td>BOM_335S0615</td>
</tr>
<tr>
<td>337S3758</td>
<td>HYNIX,DDR3,128M16,9x11.5</td>
<td>CRITICAL</td>
<td>BOM_337S3758</td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>Referenced Parts</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>U3100</td>
<td>IC,EFI,BOOTROM FINAL (LOCKED),M96</td>
<td>104S0018</td>
<td>CRITICAL</td>
<td>BOM_U3100</td>
</tr>
<tr>
<td>U1400</td>
<td>IC,32MBIT 8-PIN SERIAL FLASH, WSON8</td>
<td>1206 1/4W .002 OHM</td>
<td>CRITICAL</td>
<td>BOM_U1400</td>
</tr>
<tr>
<td>U6100</td>
<td>IC,SMC,HS8/2117</td>
<td>33UF 20% 16V DCASE</td>
<td>CRITICAL</td>
<td>BOM_U6100</td>
</tr>
</tbody>
</table>

### Configuration Options

- **SECTION A**
  - Option 1: SELECTED MOVEMENT MODES
  - Option 2: SELECTED MOVEMENT MODES

- **SECTION B**
  - Option 1: SELECTED MOVEMENT MODES
  - Option 2: SELECTED MOVEMENT MODES

- **SECTION C**
  - Option 1: SELECTED MOVEMENT MODES
  - Option 2: SELECTED MOVEMENT MODES

- **SECTION D**
  - Option 1: SELECTED MOVEMENT MODES
  - Option 2: SELECTED MOVEMENT MODES
## 1UF 0402 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>QTY</th>
<th>Description</th>
<th>Reference DC</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td>SS_CAP_2_2UF</td>
<td>Critical</td>
<td>BOM Option</td>
</tr>
<tr>
<td>10</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td>SS_CAP_10UF</td>
<td>Critical</td>
<td>BOM Option</td>
</tr>
</tbody>
</table>

## 2.2UF 0402 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>QTY</th>
<th>Description</th>
<th>Reference DC</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td>SS_CAP_2_2UF</td>
<td>Critical</td>
<td>BOM Option</td>
</tr>
<tr>
<td>7</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td>SS_CAP_10UF</td>
<td>Critical</td>
<td>BOM Option</td>
</tr>
</tbody>
</table>

## 10UF 0603 Capacitor Vendor Tables for Acoustics

<table>
<thead>
<tr>
<th>QTY</th>
<th>Description</th>
<th>Reference DC</th>
<th>Critical</th>
<th>BOM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>CAP, 10UF, 6.3V, 20%, 0603</td>
<td>SS_CAP_10UF</td>
<td>Critical</td>
<td>BOM Option</td>
</tr>
<tr>
<td>4</td>
<td>CAP, 2.2UF, 6.3V, 20%, 0402</td>
<td>SS_CAP_2_2UF</td>
<td>Critical</td>
<td>BOM Option</td>
</tr>
</tbody>
</table>

---

**Vendor Tables for Acoustics**

- **SAMSUNG**: Capacitor 1UF 0402, Capacitor 2.2UF 0402, Capacitor 10UF 0603
- **MURATA**: Capacitor 2.2UF 0402, Capacitor 10UF 0603
- **TAIYO YUDEN**: Capacitor 2.2UF 0402, Capacitor 10UF 0603
MCP79-specific pinout

From XDP connector

U1000 CPU

To XDP connector
and/or level translator

U1400 MCP

XDP connector

extended Debug Port (XDP)
3.3V input must be stable before avoid glitch on MEM_RESET_L.

MCP79 cannot control this signal directly since it must be high in sleep and MEM rails are not powered in sleep.

**DDR3 RESET Support**

MCP_MEM_RESET_L = PP3V3_S5_MEMRESET

MEM_RESET_RC_L = PP1V5_S3_MEMRESET

**DDR3 Support**

SYNC_DATE=01/30/2008
SYNC_MASTER=T18_MLB
Micro-DisplayPort / USB to RIO Hatch Assembly

Audio Connector

516S0350

516S0710

Hatch and Audio Connectors

APPENDIX A

Notice of Proprietary Property

This information is the proprietary of APPLE COMPUTER, INC. and may be protected by one or more U.S. and foreign patents. einmal herin: the information contained herein is the proprietary property of Apple Computer, Inc. the possessor agrees to the following:

I To maintain the document in confidence
II Not to reproduce or copy it
III Not to reveal or publish in whole or part

Scale

Size

Drawn Number

Sheet

Of

Notice of Proprietary Property

Audio Connector
SATA HDD PORT

516S0678

SATA Connectors

PLACEMENT_NOTE=Place FL4501 close to J4501
PLACEMENT_NOTE=Place FL4502 close to MCP79
PLACEMENT_NOTE=PLACE C4501 CLOSE TO J4500
PLACEMENT_NOTE=PLACE C4502 CLOSE TO J4500
PLACEMENT_NOTE=PLACE L4500 CLOSE TO J4501
PLACEMENT_NOTE=Place C4510 close to MCP79
PLACEMENT_NOTE=Place C4511 next to C4510
PLACEMENT_NOTE=Place C4515 next to C4516
PLACEMENT_NOTE=Place C4516 close to J4501
USB 2.0 Connector

Connect to 5V 55 or 23 per layout

USB/SMC MUX

Dual switch has ganged output
Both switches will trip together at 1.5A-2.2A

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB/SMC MUX

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%

USB EXTERNAL CONNECTORS

PLACE C4675 NEAR U4675

R4675 1/20W 100U MF 5%
NOTE: Ground pins have "SMB_X_CG" names. Ground pins designed as outputs can be left floating. VSS pins designed as inputs require pull-ups.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.

If SMS interrupt is not used, pull up to SMC rail.
**SMC Reset Button / Brownout Detect**

- **Silk:** "SMC_RST"
- Place R5001 on bottom side, near board edge.

**Debug Power Button**

- Place R5010 on bottom side, near board edge.
- Place both near board edge.

**SMC Crystal Circuit**

- SMC_XTAL
- SMC_EXTAL

**SMC AVREF Supply**

- SMC_PROCHOT
- CPU_PROCHOT

**SMC 1.05V to 3.3V Level Shifting**

- CPU_PROCHOT_BUF
- CPU_PROCHOT_L_R

**SMC Support**

- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
- AGREES TO THE FOLLOWING
  - I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
  - THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
- III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
- AGREES TO THE FOLLOWING
  - I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
  - THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY
ACIN VOLTAGE SENSE

- MAX 16.5V + 10% ACIN = 3.0V SMC_ACIN_VSENSE
- R5300 and R5301 values chosen for RC filter @ 4.53kΩ THÉVENIN resistance

MCP VOLTAGE SENSE

- Place RC close to SMC TO PBUS CURRENT SENSOR
- Enables PBUS VSense divider when high.

PBUS VOLTAGE SENSE

- Place C5300 NEAR SMC
- R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53kΩ THEVENIN RESISTANCE
- MAX 16.5V + 10% ACIN = 3.0V SMC_ACIN_VSENSE
CPU/MCP T-Diode Thermal Sensor

LOCAL TEMP NEAR FRONT EDGE

LOCAL TEMP NEAR AIR VENT

LOCAL TEMP NEAR POWER SUPPLIES

(Write: 0x92 Read: 0x93)

(Write: 0x90 Read: 0x91)

(Write: 0x92 Read: 0x93)
The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. Not to reproduce or copy it
II. Not to reveal or publish in whole or part
III. To maintain the document in confidence

NOTICE OF PROPRIETARY PROPERTY

DRAFT NUMBER
SHEET OF SIZE

5%

3.3K
1/20W

R6100

PLACEMENT NOTE = Place close to U6100

5%
1/20W
MF

201

R6150

68 41

M25P32

CRITICAL
OMIT
VFQFPN
3
4
8
9
1
2
7
6
U6100

PLACEMENT NOTE = Place close to U6100

5%
1/20W
MF

201

R6152

68 41

402
1/16W
MF-LF

5%

0
21

R6105

0.1UF
10%
6.3V
X5R201

C6100

5%
3.3K
1/20W
MF2012

1
R6101

SPI ROM

SPI_CLK
SPI_CLK_MUX
SPI_MOSI_MUX
SPI_MOSI
SPI_MLB_CS_L

SPI_HOLD_L
SPI_MISO_R
SPI_WP_L
SPI_MISO_MUX

68
68
41
7

= PP3V3_S5_ROM

SYNC DATE = 02/15/2008
SYNC MASTER = CHANGZHANG

SPI ROM

APPLE INC.
D 051-8064

D PIHERI-COMIC

www.laptop-schematics.com

D PIHERI-COMIC

www.laptop-schematics.com
3.425V "G3Hot" Supply

Supply used to generate 3.425V delivered to the board processor.

Q6990 will pull down
P469200_A11_1 in the event
generated when left shift, option, and control
and the power button is depressed.
1V05 S5 POWER SUPPLY

supply for MCP1V05 AUX, FSB (CPU & MCP) VTT, 1V05 S0
1.5V/0.75V POWER SUPPLY

Vout = 0.75V * (1 + Ra / Rb)

Routing Note:

C7500 1UF
put 6 vias under the thermal pad

C7508
6.3V
20K

Connect CS_GND to using Kelvin connection.

MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm

PLACE XW7502 NEAR L7520

CRITICAL

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm

PLACE C7543 NEAR NB

CRITICAL
NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

Some signals require 27.4-ohm single-ended impedance.

Design Guide recommends each strobe/signal group is routed on the same layer.

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

**MCP FSB COMP Signal Constraints**

- DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.
- FSB 2X signals/groups shown in signal table on right.
- Intel Design Guide recommends FSB signals be routed only on internal layers.

**CPU / FSB Net Properties**

**SPACING RULE SET**

**CPU SIGNAL**

- DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.
- FSB 2X signals/groups shown in signal table on right.
- Intel Design Guide recommends FSB signals be routed only on internal layers.

**CPU / FSB Constraint**

Not to reproduce or copy in whole or part.

NOTICE OF PROPRIETARY PROPERTY

Drawn to specifications as of:

Dec. 31, 1999

As a courtesy, the VCCSense pair is specified at 7 mils. This is not a measurement of intent but a typical implementation size.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

No DQS to clock matching requirement.
### Analog Video Signal Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Interface</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP79</td>
<td>Interface DG (DG-03328-001_v0D), Section 2.7.1.</td>
<td>R/G/B signals should be matched as close as possible and &lt; 10 inches. - 75-ohm from output of three-pole filter to connector (if possible).</td>
</tr>
</tbody>
</table>

### Digital Video Signal Constraints

- LVDS intra-pair matching should be 5 mils. - Pairs should be within 100 mils of clock length.

### SATA Interface Constraints

- SATA Interface Constraints (SATA_100D_HDD)
- CRT_2SWITCHER
- MCP_PEX_COMP

- SATA Interface Constraints (SATA)
- LVDS

- LVDS intra-pair matching should be 5 mils. - Pairs should be within 100 mils of clock length.

### MCP Constraints 1

- 37-ohm from MCP to first termination resistor.
- 68-ohm from first to second termination resistor.
- CRT-2 SWITCHER should be within 100 mils of clock length.

### NOTICE OF PROPRIETARY PROPERTY

This document contains unpublished proprietary information of Apple Computer, Inc. The possession, use, or disclosure of this document, in whole or in part, is subject to the following terms and conditions:

- It is not to be reproduced or used in any manner not expressly authorized in writing by Apple Computer, Inc.
- It may not be used or included in any product or other work except as specifically authorized in writing by Apple Computer, Inc.
- It may not be disclosed to any third party except as specifically authorized in writing by Apple Computer, Inc.

- Apple Inc. (800) 548-2000
- 1234567890

- NOTICE OF PROPRIETARY PROPERTY

This document contains unpublished proprietary information of Apple Computer, Inc. The possession, use, or disclosure of this document, in whole or in part, is subject to the following terms and conditions:

- It is not to be reproduced or used in any manner not expressly authorized in writing by Apple Computer, Inc.
- It may not be used or included in any product or other work except as specifically authorized in writing by Apple Computer, Inc.
- It may not be disclosed to any third party except as specifically authorized in writing by Apple Computer, Inc.

- Apple Inc. (800) 548-2000
- 1234567890
- NOTICE OF PROPRIETARY PROPERTY

This document contains unpublished proprietary information of Apple Computer, Inc. The possession, use, or disclosure of this document, in whole or in part, is subject to the following terms and conditions:

- It is not to be reproduced or used in any manner not expressly authorized in writing by Apple Computer, Inc.
- It may not be used or included in any product or other work except as specifically authorized in writing by Apple Computer, Inc.
- It may not be disclosed to any third party except as specifically authorized in writing by Apple Computer, Inc.

- Apple Inc. (800) 548-2000
- 1234567890
- NOTICE OF PROPRIETARY PROPERTY

This document contains unpublished proprietary information of Apple Computer, Inc. The possession, use, or disclosure of this document, in whole or in part, is subject to the following terms and conditions:

- It is not to be reproduced or used in any manner not expressly authorized in writing by Apple Computer, Inc.
- It may not be used or included in any product or other work except as specifically authorized in writing by Apple Computer, Inc.
- It may not be disclosed to any third party except as specifically authorized in writing by Apple Computer, Inc.

- Apple Inc. (800) 548-2000
- 1234567890
**PCI Bus Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
<th>Count</th>
<th>Pitch</th>
<th>Notes</th>
</tr>
</thead>
</table>

**LPC Bus Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
<th>Count</th>
<th>Pitch</th>
<th>Notes</th>
</tr>
</thead>
</table>

**USB 2.0 Interface Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
<th>Count</th>
<th>Pitch</th>
<th>Notes</th>
</tr>
</thead>
</table>

**SMBus Interface Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
<th>Count</th>
<th>Pitch</th>
<th>Notes</th>
</tr>
</thead>
</table>

**HD Audio Interface Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
<th>Count</th>
<th>Pitch</th>
<th>Notes</th>
</tr>
</thead>
</table>

**SIO Signal Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
<th>Count</th>
<th>Pitch</th>
<th>Notes</th>
</tr>
</thead>
</table>

**SPI Interface Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Length</th>
<th>Count</th>
<th>Pitch</th>
<th>Notes</th>
</tr>
</thead>
</table>

**NOTICE OF PROPRIETARY PROPERTY**

This publication or any portion thereof may not be reproduced or copied in any form without the express written permission of the proprietor.

This publication is intended for use by Apple Inc. employees only and may not be disclosed or distributed to any third party.

*Apple Inc.*

**MCP Constraints 2**

*Scale декабря 2001 г.*

**APPLE INC.**

**051-8064**
### SMC SMBus Net Properties

<table>
<thead>
<tr>
<th>Value</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SDA</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SDA</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

### SMC SMBus Charger Net Properties

<table>
<thead>
<tr>
<th>Value</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSI_P</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>CHGR_CSO_P</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>CHGR_CSO_N</td>
<td>0.1</td>
<td>0.1</td>
</tr>
</tbody>
</table>

### SMC Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sync Master</td>
<td>M97</td>
</tr>
<tr>
<td>Sync Date</td>
<td>02/04/2008</td>
</tr>
<tr>
<td>Sheet</td>
<td>Title</td>
</tr>
<tr>
<td>-------</td>
<td>-------</td>
</tr>
<tr>
<td>A</td>
<td>M96 BOARD-SPECIFIC SPACING &amp; PHYSICAL CONSTRAINTS</td>
</tr>
<tr>
<td>B</td>
<td>M96 RULE DEFINITIONS</td>
</tr>
<tr>
<td>C</td>
<td>M96 RULE DEFINITIONS</td>
</tr>
<tr>
<td>D</td>
<td>M96 RULE DEFINITIONS</td>
</tr>
</tbody>
</table>