1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEMATIC, Pleox-II

MacBookAir

03/19/2009

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
A		691254	PRODUCTION RELEASED	04/09/09	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

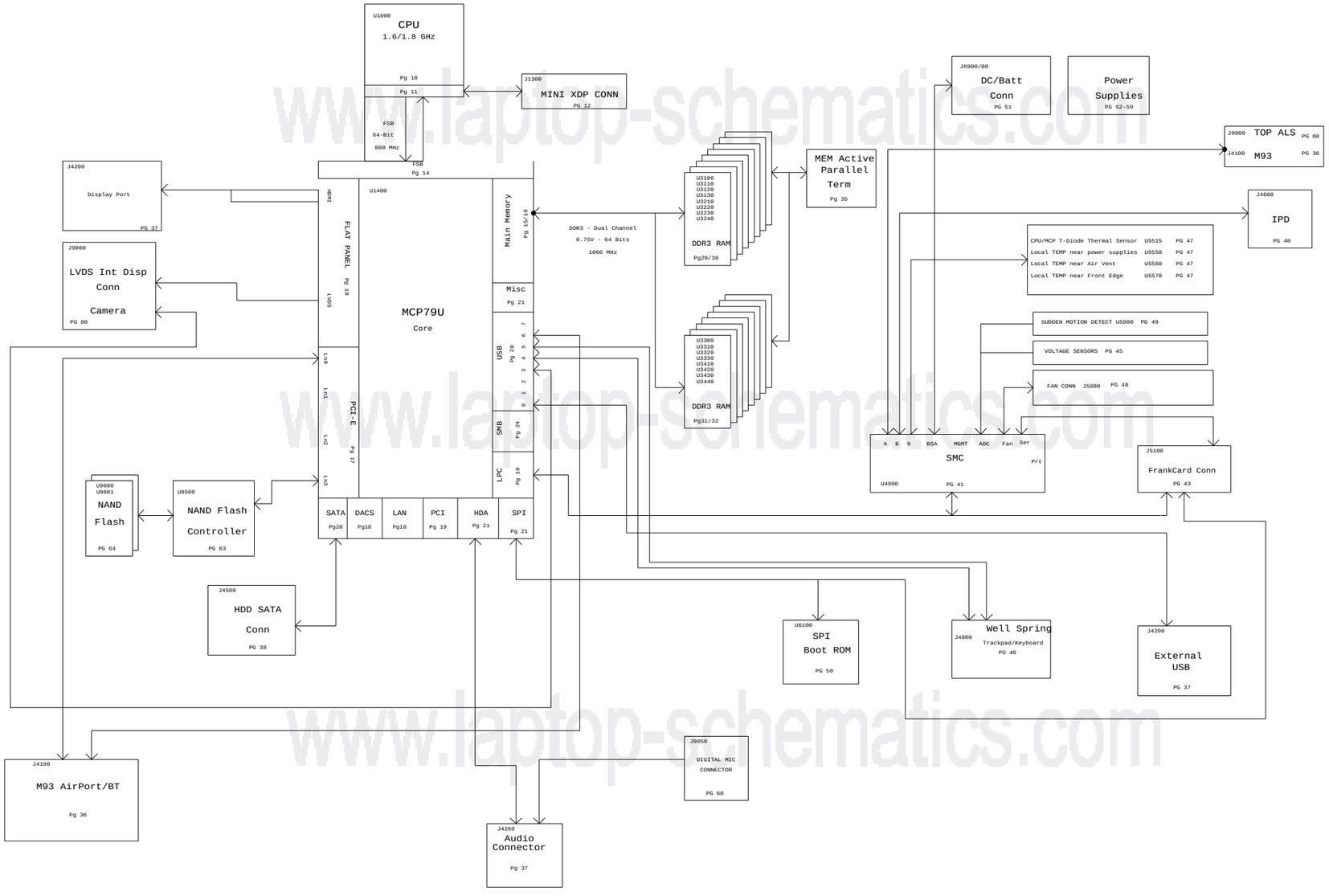
SIZE D

APPLE INC.

TITLE
SCHEM,Pleox-II

DRAWING NUMBER 051-8064
REV. A

SHT 1 OF 109



System Block Diagram

SYNC_MASTER=WFERRY-WF SYNC_DATE=05/11/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	2	109

Pleox-II POWER SYSTEM ARCHITECTURE

DC-JACK J6980 — PP18V5_DCIN — 6A FUSE F6900 — PP18V5_G3H_CHGR

PPDCIN_G3H_R, PPVBATT_G3H_R, PPBUSB_G3H, PPVIN_G3H_DCIN — D6901

PPDCIN_G3H → 3.425V G3HOT LTC3470A U6900 (PAGE 51) → PP3V42_G3H_REG (200 mA MAX CURRENT)

PP3V42_G3H_SMC → SMC PWRGD RN5VD30A-F U5000 (PAGE 42) → SMC_RESET_L

SMBUS_SMC_BSA_SCL, SMBUS_SMC_BSA_SDA

PBUS Supply/ BATTERY CHARGER ISL6258 U7900 (PAGE 59)

BATTERY 2S2P

PPVBAT_G3H_CHGR_REG — 7A FUSE — PPBUSB_G3H — R7980 (0.002) — PBUSA_G3H

A R7930 — Q7950 — CHGR_BGATE — BATT_POS_F

V Q5315

Q7853 — PP1V05_S0_FET — P1V05S0_EN

1.05V ISL6236 U7200 (PAGE 53): P1V05_S5_EN (S5) → PP1V05_S5_REG (7 A MAX CURRENT); MCPCORES0_EN (S0) → PPMCPCORE_S0_REG (25 A MAX CURRENT); PG1 → P1V05_S5_PGOOD; PG2 → MCPCORES0_PGOOD

MCP79U U1400: LPC_RESET* → DEBUG_RESET_L, SMC_LRESET_L; PCIE_RESET* → FC_RESET_L, PCA9557D_RESET_L, AIRPORT_RST_L, BKLT_PLT_RST_L; PS_PWRGD ← MCP_PS_PWRGD; PWRBTN*, RSMRST*, CPU_RESET*, CPU_PWRGD

CPUVCORE: VIN ← PPBUSA_G3H; VOUT → PPVCORE_S0_CPU_REG → PPVCORE_S0_CPU (30 A MAX CURRENT)

IMVP_VR_ON → ISL6261CRZ U7100 (PAGE 52) VR_ON; PGOOD → VR_PWRGOOD_DELAY → U2850

CPU U1000 (PAGE 10): PWRGOOD, RESET* ← FSB_CPURST_L

MCP79U: SLP_S5*, SLP_S4*, SLP_S3*, PCI_RESET0*

SMC_ADAPTER_PRESENT, WOW_EN, PM_SLP_S3_L, PM_WLAN_EN_L

DELAY R-1K C-0.47uF → P3V3S3_EN; DELAY R-5.1K C-0.47uF → DDRREG_EN; DELAY R-100K C-NoStuff → P5V3S3_EN_L

PP3V3_S5_PWRCTL → Q7710

P3V3S0_EN, P5VS0_EN, PBUSVSENS_EN

DELAY R-0 C-0.47uF → P1V05S0_EN (S0); DELAY R-5.1k C-0.47uF → P1V8S0_EN (S0); DELAY R-0 C-0.47uF → MCPDDR_EN (S0); DELAY R-33k C-0.47uF → CPUVTTS0_EN (S0); DELAY R-22k C-0,47uF → MCPCORES0_EN (S0)

=PPBUSB_G3H

SMC U4900 (PAGE 41): IMVP_VR_ON, SMC_PM_G2_EN (P68)

PP3V42_G3H_PWRCTL → Q7700 → PM_G2_P3V3S5_EN_L → PP3V3S5_EN_L (S5)

SMC_PM_G2_EN → DELAY R-5.1K C-0.47uF → P1V05_S5_EN

U7770 LTC2909 (PAGE 57): ADJ1 ← PP1V5_S0_VMON; ADJ2 ← PP1V05_S0_VMON; RST* → S0PGOOD_PWROK

MCPCORES0_PGOOD, P5V3V3_PGOOD → ALL_SYS_PWRGD

Q7840 — PP5V_S0_FET — P5VS0_EN_L

Q7621: P5VS3_EN_L (S3), PP3V3S5_EN_L (S5)

5V / 3.3V TPS51120 U7600 (PAGE 60): VO1 → PP5V_S3_REG (? A MAX CURRENT) → PP5V_S3; VO2 → PP3V3_S5_REG (? A MAX CURRENT) → PP3V3_S5; PGOOD1,2 → P5V3V3_PGOOD

Q7810 — PP3V3_S3 — P3V3S3_EN_L

1.8V S0 TPS19918 U7360 (PAGE 54): P1V8_S0_EN, PPVIN_S0_P1V8S0 → PP1V8_S0_REG (200 mA MAX)

Q7830 — PP3V3_S0_FET — P3V3S0_EN_L

U7740 TPS19918 (PAGE 57): P3V3_S5_PWRCTL, PP1V5_S5_PGOOD → RSMRST_PWRGD

SMC U4900 (PAGE 41): RSMRST_OUT(P15) → PM_RSMRST_L; PWRGD(P12) ← ALL_SYS_PWRGD, 100ms DLY; IMVP_VR_ON(P16) → IMVP_VR_ON; RSMRST_IN(P13) ← RSMRST_PWRGD; PWR_BUTTON(P90) ← SMC_ONOFF_L; P17(BTN_OUT) → PM_PWRBTN_L; PLT_RST* → SMC_LRESET_L; RST* → SMC_RESET_L; SLP_S5_L(P95) ← PM_SLP_S5_L; SLP_S4_L(P94) ← PM_SLP_S4_L; SLP_S3_L(P93) ← PM_SLP_S3_L

BATTERY ONLY: 05

Q7801 — PP1V5_S3_P1V5S0FET → =PP1V5_S0_FET — MCPDDR_EN

PP0V75_S3_VTTREF

1.5V / 0.75V TPS51116 U7500 (PAGE 55): DDRREG_EN → S5; DDRVTT_EN ← MEM_VTT_EN_R via R2870; VOUT1 → PP1V5_S3_REG (11 A MAX CURRENT); VOUT2 → PP0V75_S0_REG; DDRREG_PGOOD

Power Block Diagram

SYNC_MASTER=POWER SYNC_DATE=06/30/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	3	109

BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0160	PCBA,MLB,1.86GHZ,HY 2GB,SS CAP,M96A	EEE_9CW,M96A_COMMON,M96A_HYNIX,M96A_SS_CAP,CPU_1_86GHZ
639-0161	PCBA,MLB,1.86GHZ,HY 2GB,MU CAP,M96A	EEE_9CX,M96A_COMMON,M96A_HYNIX,M96A_MU_CAP,CPU_1_86GHZ
639-0159	PCBA,MLB,1.86GHZ,HY 2GB,TY CAP,M96A	EEE_9CV,M96A_COMMON,M96A_HYNIX,M96A_TY_CAP,CPU_1_86GHZ
639-0166	PCBA,MLB,2.13GHZ,HY 2GB,SS CAP,M96A	EEE_9D5,M96A_COMMON,M96A_HYNIX,M96A_SS_CAP,CPU_2_13GHZ
639-0164	PCBA,MLB,2.13GHZ,HY 2GB,MU CAP,M96A	EEE_9D1,M96A_COMMON,M96A_HYNIX,M96A_MU_CAP,CPU_2_13GHZ
639-0165	PCBA,MLB,2.13GHZ,HY 2GB,TY CAP,M96A	EEE_9D4,M96A_COMMON,M96A_HYNIX,M96A_TY_CAP,CPU_2_13GHZ
639-0157	PCBA,MLB,1.86GHZ,MI 2GB,SS CAP,M96A	EEE_9CK,M96A_COMMON,M96A_MICRON,M96A_SS_CAP,CPU_1_86GHZ
639-0158	PCBA,MLB,1.86GHZ,MI 2GB,MU CAP,M96A	EEE_9CU,M96A_COMMON,M96A_MICRON,M96A_MU_CAP,CPU_1_83GHZ
639-0162	PCBA,MLB,1.86GHZ,MI 2GB,TY CAP,M96A	EEE_9CZ,M96A_COMMON,M96A_MICRON,M96A_TY_CAP,CPU_1_86GHZ
639-0163	PCBA,MLB,2.13GHZ,MI 2GB,SS CAP,M96A	EEE_9D0,M96A_COMMON,M96A_MICRON,M96A_SS_CAP,CPU_2_13GHZ
639-0167	PCBA,MLB,2.13GHZ,MI 2GB,MU CAP,M96A	EEE_9D6,M96A_COMMON,M96A_MICRON,M96A_MU_CAP,CPU_2_13GHZ
639-0168	PCBA,MLB,2.13GHZ,MI 2GB,TY CAP,M96A	EEE_9D7,M96A_COMMON,M96A_MICRON,M96A_TY_CAP,CPU_2_13GHZ

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9CW]	CRITICAL	EEE_9CW
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9CX]	CRITICAL	EEE_9CX
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9CV]	CRITICAL	EEE_9CV
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9D5]	CRITICAL	EEE_9D5
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9D1]	CRITICAL	EEE_9D1
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9D4]	CRITICAL	EEE_9D4
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9CK]	CRITICAL	EEE_9CK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9CU]	CRITICAL	EEE_9CU
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9CZ]	CRITICAL	EEE_9CZ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9D0]	CRITICAL	EEE_9D0
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9D6]	CRITICAL	EEE_9D6
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:9D7]	CRITICAL	EEE_9D7

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M96_COMMON	ALTERNATE,COMMON,M96_COMMON1,M96_COMMON2,M96_COMMON3
M96_COMMON1	MCP_B02,BOOTROM_FINAL,SMC_PRGRM,BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP,NO_VREFMRGN
M96_COMMON2	LPCPLUS,LPCPLUS_CONN,XDP
M96_COMMON3	MCP_CS1_NO
M96_HYNIX	DRAM_HYNIX
M96_MICRON	DRAM_MICRON,DRAM_SPD_2
M96_SS_CAP	SS_CAP_2_2UF,SS_CAP_10UF,SS_CAP_1UF
M96_MU_CAP	MU_CAP_2_2UF,MU_CAP_10UF,MU_CAP_1UF
M96_TY_CAP	TY_CAP_2_2UF,TY_CAP_10UF,TY_CAP_1UF

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3751	1	IC,PDC,SLGA8,PRQ,1.86GHZ,17W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_1_86GHZ
337S3758	1	IC,PDC,SLGEQ,PRQ,2.13GHZ,17W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_2_13GHZ
338S0604	1	IC,GMCP,MCP79U-A01Q,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_A01Q
338S0601	1	IC,GMCP,MCP79U-B01,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_B01
338S0637	1	IC,GMCP,MCP79U-B02,27MMX27MM,BGA1588	U1400	CRITICAL	MCP_B02
335S0615	1	IC, 32MBIT 8-PIN SERIAL FLASH, WSON8	U6100	CRITICAL	BOOTROM_BLANK_4MB
341S2382	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M96	U6100	CRITICAL	BOOTROM_DEVEL
341S2326	1	IC,EFI,BOOTROM FINAL (LOCKED),M96	U6100	CRITICAL	BOOTROM_FINAL
338S0563	1	IC,SMC,HS8/2117	U4900	CRITICAL	SMC_BLANK
341S2327	1	IC,PRGRM,SMC (NEW),M96	U4900	CRITICAL	SMC_PRGRM
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_HYNIX
333S0476	4	HYNIX,DDR3,128M16,9x11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_HYNIX
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3100,U3110,U3120,U3130	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3200,U3210,U3220,U3230	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3300,U3310,U3320,U3330	CRITICAL	DRAM_MICRON
333S0475	4	MICRON,DDR3,128M16,9x11.5	U3400,U3410,U3420,U3430	CRITICAL	DRAM_MICRON
353S1938	1	IC,ISL6258,REV2,BAT CHGR, 28P QFN	U7900	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	REFERENCE DESIGNATOR(S)	DESCRIPTION	BOM OPTION
128S0093	128S0092	ALL	33UF 20% 16V DCASE	
376S0466	376S0410	ALL	Si4413 for Si4405	
740S0067	740S0028	ALL	0.5A OC FUSE	
104S0023	104S0018	ALL	1206 1/4W .002 OHM	
152S0684	152S0421	ALL	1.0UH,22A,10MOHM	
376S0627	376S0723	ALL	POWER NFET, 30V, 18A	
152S0905	152S0861	ALL	IND,IHLP4040CZ,0.68uH,18A	
128S0262	128S0220	ALL	100UF 20% 6.3V BCASE	
353S1381	353S1912	ALL	SMC AVREF	

CONFIGURATION OPTIONS

SYNC_MASTER=(N/A) SYNC_DATE=(N/A)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 4 OF 109	

1UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0629	4	CAP, 1UF, 6.3V, 10%, 0402	C7947,C7360,C2504,C2505	CRITICAL	SS_CAP_1UF
138S0629	7	CAP, 1UF, 6.3V, 10%, 0402	C2506,C2507,C2516,C2517,C7100,C7101,C7103	CRITICAL	SS_CAP_1UF
138S0629	9	CAP, 1UF, 6.3V, 10%, 0402	C2860,C7296,C7297,C7492,C7500,C7940,C7941,C9760,C7603	CRITICAL	SS_CAP_1UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0628	4	CAP, 1UF, 6.3V, 10%, 0402	C7947,C7360,C2504,C2505	CRITICAL	MU_CAP_1UF
138S0628	7	CAP, 1UF, 6.3V, 10%, 0402	C2506,C2507,C2516,C2517,C7100,C7101,C7103	CRITICAL	MU_CAP_1UF
138S0628	9	CAP, 1UF, 6.3V, 10%, 0402	C2860,C7296,C7297,C7492,C7500,C7940,C7941,C9760,C7603	CRITICAL	MU_CAP_1UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0630	4	CAP, 1UF, 6.3V, 10%, 0402	C7947,C7360,C2504,C2505	CRITICAL	TY_CAP_1UF
138S0630	7	CAP, 1UF, 6.3V, 10%, 0402	C2506,C2507,C2516,C2517,C7100,C7101,C7103	CRITICAL	TY_CAP_1UF
138S0630	9	CAP, 1UF, 6.3V, 10%, 0402	C2860,C7296,C7297,C7492,C7500,C7940,C7941,C9760,C7603	CRITICAL	TY_CAP_1UF

2.2UF 0402 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	SS_CAP_2_2UF
138S0632	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1283,C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	SS_CAP_2_2UF
138S0632	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3640,C3641	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655	CRITICAL	SS_CAP_2_2UF
138S0632	7	CAP, 2.2UF, 6.3V, 20%, 0402	C2530,C2531,C2532,C2533,C2534,C2535,C2536	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2550,C2551,C2552,C2553,C2555,C2560,C2562,C2564	CRITICAL	SS_CAP_2_2UF
138S0632	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2570,C2571,C2572,C2573,C2574,C2575,C2576,C2610	CRITICAL	SS_CAP_2_2UF
138S0632	3	CAP, 2.2UF, 6.3V, 20%, 0402	C4800,C7362,C7511	CRITICAL	SS_CAP_2_2UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	MU_CAP_2_2UF
138S0633	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1283,C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	MU_CAP_2_2UF
138S0633	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3640,C3641	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655	CRITICAL	MU_CAP_2_2UF
138S0633	7	CAP, 2.2UF, 6.3V, 20%, 0402	C2530,C2531,C2532,C2533,C2534,C2535,C2536	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2550,C2551,C2552,C2553,C2555,C2560,C2562,C2564	CRITICAL	MU_CAP_2_2UF
138S0633	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2570,C2571,C2572,C2573,C2574,C2575,C2576,C2610	CRITICAL	MU_CAP_2_2UF
138S0633	3	CAP, 2.2UF, 6.3V, 20%, 0402	C4800,C7362,C7511	CRITICAL	MU_CAP_2_2UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1240,C1241,C1242,C1243,C1244,C1245,C1246,C1247,C1248,C1249	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C1250,C1251,C1252,C1253,C1254,C1255,C1256,C1257,C1258,C1259	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C1260,C1261,C1262,C1263,C1264,C1265,C1266,C1267	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9900,C9901,C9902,C9903,C9904,C9905,C9906,C9907,C9908,C9909	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9910,C9911,C9912,C9913,C9914,C9915,C9916,C9917,C9918,C9919	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9920,C9921,C9922,C9923,C9924,C9925,C9926,C9927,C9928,C9929	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C9930,C9931,C9932,C9933,C9934,C9935,C9936,C9937,C9938,C9939	CRITICAL	TY_CAP_2_2UF
138S0634	12	CAP, 2.2UF, 6.3V, 20%, 0402	C1283,C1284,C1285,C1286,C1287,C1288,C1291,C1292,C1293,C1294,C1295,C1296	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3500,C3501,C3504,C3505,C3510,C3511,C3512,C3514,C3515,C3516	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3520,C3521,C3524,C3525,C3530,C3531,C3534,C3535,C3540,C3541	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3542,C3544,C3545,C3546,C3550,C3551,C3554,C3555	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3600,C3601,C3604,C3605,C3610,C3611,C3612,C3614,C3615,C3616	CRITICAL	TY_CAP_2_2UF
138S0634	10	CAP, 2.2UF, 6.3V, 20%, 0402	C3620,C3621,C3624,C3625,C3630,C3631,C3634,C3635,C3640,C3641	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C3642,C3644,C3645,C3646,C3650,C3651,C3654,C3655	CRITICAL	TY_CAP_2_2UF
138S0634	7	CAP, 2.2UF, 6.3V, 20%, 0402	C2530,C2531,C2532,C2533,C2534,C2535,C2536	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2550,C2551,C2552,C2553,C2555,C2560,C2562,C2564	CRITICAL	TY_CAP_2_2UF
138S0634	8	CAP, 2.2UF, 6.3V, 20%, 0402	C2570,C2571,C2572,C2573,C2574,C2575,C2576,C2610	CRITICAL	TY_CAP_2_2UF
138S0634	3	CAP, 2.2UF, 6.3V, 20%, 0402	C4800,C7362,C7511	CRITICAL	TY_CAP_2_2UF

10UF 0603 CAPACITOR VENDOR TABLES FOR ACOUSTICS

SAMSUNG

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	SS_CAP_10UF
138S0626	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	SS_CAP_10UF
138S0626	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1280	CRITICAL	SS_CAP_10UF
138S0626	8	CAP, 10UF, 6.3V, 20%, 0603	C4109,C4613,C5066,C7502,C7541,C7650,C7690,C9012	CRITICAL	SS_CAP_10UF
138S0626	5	CAP, 10UF, 6.3V, 20%, 0603	C7266,C7267,C7269,C7401,C7605	CRITICAL	SS_CAP_10UF

MURATA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	MU_CAP_10UF
138S0625	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	MU_CAP_10UF
138S0625	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1280	CRITICAL	MU_CAP_10UF
138S0625	8	CAP, 10UF, 6.3V, 20%, 0603	C4109,C4613,C5066,C7502,C7541,C7650,C7690,C9012	CRITICAL	MU_CAP_10UF
138S0625	5	CAP, 10UF, 6.3V, 20%, 0603	C7266,C7267,C7269,C7401,C7605	CRITICAL	MU_CAP_10UF

TAIYO YUDEN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1200,C1201,C1202,C1203,C1204,C1205,C1206,C1207,C1208,C1209	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1210,C1211,C1212,C1213,C1214,C1215,C1216,C1217,C1218,C1219	CRITICAL	TY_CAP_10UF
138S0627	10	CAP, 10UF, 6.3V, 20%, 0603	C1220,C1221,C1222,C1223,C1224,C1225,C1226,C1227,C1228,C1229	CRITICAL	TY_CAP_10UF
138S0627	3	CAP, 10UF, 6.3V, 20%, 0603	C1230,C1231,C1280	CRITICAL	TY_CAP_10UF
138S0627	8	CAP, 10UF, 6.3V, 20%, 0603	C4109,C4613,C5066,C7502,C7541,C7650,C7690,C9012	CRITICAL	TY_CAP_10UF
138S0627	5	CAP, 10UF, 6.3V, 20%, 0603	C7266,C7267,C7269,C7401,C7605	CRITICAL	TY_CAP_10UF

Acoustic Cap BOM Config Tables

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE NONE	SHT 5	OF 109

Functional Test Points

NB NO_TESTS

These are normally testpoints but become NC

NO_TEST

Power Supply NO_TESTs

NO_TEST

CLOCK NO_TESTS

NO_TEST

LVDS NO_TESTS

NO_TEST

REQUIRED NETS

FUNC TEST - BATTERY CONNECTOR

x2	I647	TRUE	BATT_POS	49
x2	I649	TRUE	GND	
	I638	TRUE	SMC_BS_ALRT_L	39 40 49
	I644	TRUE	SMBUS_SMC_BSA_SCL	42 69
	I639	TRUE	SMBUS_SMC_BSA_SDA	42 69

FUNC TEST - DC-IN CONNECTOR

x6	I648	TRUE	PP18V5_DCIN	49 70
	I650	TRUE	ADAPTER_SENSE	49
x6	I708	TRUE	GND	

FUNC TEST - FAN CONNECTOR

	I666	TRUE	=PP5V_S0_FAN	7 46
	I667	TRUE	FAN_RT_PWM	46
	I669	TRUE	FAN_RT_TACH	46
	I714	TRUE	GND	

FUNC TEST - AIRPORT

	I741	TRUE	CK505_SRC_CLKREQ6_L	6
	I742	TRUE	PCIE_WAKE_L	6 16 34
	I743	TRUE	AIRPORT_RST_L	6 24 34
	I744	TRUE	=SMB_AIRPORT_CLK	6 34 42
	I745	TRUE	=SMB_AIRPORT_DATA	6 34 42
	I746	TRUE	GND	

FUNC TEST - MIC

	I747	TRUE	PP3V3_S0_MIC_F	59 70
	I748	TRUE	AUD_MIC_DATA_F	59
	I749	TRUE	AUD_MIC_CLK_F	59
	I750	TRUE	GND_MIC_F	59

FUNC TEST - AUDIO CONNECTOR

	I645	TRUE	HDA_SYNC	20 35 68
	I646	TRUE	HDA_BIT_CLK	20 35 68
	I731	TRUE	AUD_MIC_DATA	35 59
	I730	TRUE	HDA_SDOUT	20 35 68
	I733	TRUE	=PPVIN_S0_AUDIO	7 35
	I735	TRUE	HDA_SDIN0	20 35 68
	I749	TRUE	AUD_MIC_CLK	35 59
	I734	TRUE	PM_SLP_S3_L	20 34 35 39 56

FUNC TEST - IPD CONNECTOR

	I507	TRUE	SMC_LID	38 39 40
	I508	TRUE	PP3V42_G3H_IPD_F	38 70
	I509	TRUE	SMC_SYS_KBDLED	38 39
	I506	TRUE	SMC_SYS_LED	38 39
	I510	TRUE	=USB2_TPAD_N	8 38
	I512	TRUE	=USB2_TPAD_P	8 38
	I511	TRUE	SMC_ONOFF_L	6 38 39 40
	I513	TRUE	=USB2_IR_N	6 8 38
	I514	TRUE	=USB2_IR_P	6 8 38
	I515	TRUE	PP5V_S0_KBDLED_F	6 38 70
	I516	TRUE	PP5V_S3_TOPCASE_F	38 70
	I517	TRUE	=I2C_TPAD_SCL	38 42
	I518	TRUE	=I2C_TPAD_SDA	38 42
	I524	TRUE	SMC_ONOFF_L	6 38 39 40
	I519	TRUE	=USB2_IR_N	6 8 38
	I527	TRUE	=USB2_IR_P	6 8 38
	I674	TRUE	PP5V_S0_KBDLED_F	6 38 70
	I735	TRUE	LSOC_PRESS_H_R	38

FUNC TEST - M93 WIRELESS CONNECTOR

	I478	TRUE	AIRPORT_RST_L	6 24 34
	I475	TRUE	PCIE_WAKE_L	6 16 34
	I479	TRUE	CK505_SRC_CLKREQ6_L	6
	I478	TRUE	PCIE_CLK100M_MINI_N_F	34
	I476	TRUE	PCIE_CLK100M_MINI_P_F	34
	I477	TRUE	PCIE_E_D2R_N_F	34
	I480	TRUE	PCIE_E_D2R_P_F	34
	I483	TRUE	PCIE_E_R2D_C_N_F	6 34
	I484	TRUE	PCIE_E_R2D_C_P_F	6 34
	I482	TRUE	AIRPORT_RST_L	6 24 34
	I499	TRUE	=SMB_AIRPORT_DATA	6 34 42
	I500	TRUE	=SMB_AIRPORT_CLK	6 34 42
	I501	TRUE	PCIE_E_R2D_C_N_F	6 34
	I502	TRUE	PCIE_E_R2D_C_P_F	6 34
	I503	TRUE	PP3V3_S3_AP_AUX	34 70

NICE2HAVE NETS

FUNC TEST - Power Supplies

	I92	TRUE	PPVCORE_S0_CPU	7 70
	I454	TRUE	PP0V75_S0	7 70
	I455	TRUE	PP1V05_S0	7 70
	I457	TRUE	PP1V5_S0	7 70
	I460	TRUE	PP1V5_S3	7 70
	I459	TRUE	PP1V05_S5	7 70
	I458	TRUE	PPMCPCORE_S0	7 70
	I461	TRUE	PP5V_S0	7 70
	I466	TRUE	PP3V3_S0	7 70
	I465	TRUE	PP3V3_S3	7 70
	I462	TRUE	PP5V_S3	7 70
	I467	TRUE	PP3V3_S5	7 70
	I468	TRUE	PP3V42_G3H	7 70
	I474	TRUE	PP18V5_G3H	7 70
	I472	TRUE	PPDCIN_G3H	7 70
	I472	TRUE	PPBUS_G3H	7 70
	I474	TRUE	PPBUS_R_G3H	7 70
	I467	TRUE	PP1V8_S0	7 70

FUNC TEST - SATA HDD

	I751	TRUE	PP3V3_S0_HDD_F	36 70
	I752	TRUE	SATA_HDD_R2D_N	36 67
	I753	TRUE	SATA_HDD_R2D_P	36 67
	I754	TRUE	SATA_HDD_D2R_C_N	36 67
	I755	TRUE	SATA_HDD_D2R_C_P	36 67
	I756	TRUE	GND	

FUNC TEST - RIO HATCH CONNECTOR

	I716	TRUE	DP_ML_C_N<3..0>	61 67
	I717	TRUE	DP_ML_C_P<3..0>	61 67
	I718	TRUE	DP_AUX_CH_C_N	35 60 61 67
	I719	TRUE	DP_AUX_CH_C_P	35 60 61 67
	I720	TRUE	DP_CA_DET_Q	35 61
	I721	TRUE	HDMI_CEC	35 61
	I722	TRUE	DP_HPD_Q	35 61
	I723	TRUE	PP3V3_S0_DPPWR	35 61 70
	I725	TRUE	USB2_EXTA_F_P	35 37
	I726	TRUE	USB2_EXTA_F_N	35 37
	I727	TRUE	PP5V_S3_USB2_EXTA_F	35 37 70
	I728	TRUE	GND	

FUNC TEST - XDP/ITP CONNECTOR

	I693	TRUE	XDP_BPM_L<0..5>	8 12 65
	I696	TRUE	TP_XDP_OBSFN_B0	12
	I688	TRUE	TP_XDP_OBSFN_B1	12
	I681	TRUE	TP_XDP_OBSDATA_B0	12
	I683	TRUE	TP_XDP_OBSDATA_B1	12
	I682	TRUE	TP_XDP_OBSDATA_B2	12
	I684	TRUE	TP_XDP_OBSDATA_B3	12
	I685	TRUE	XDP_PWRGD	12
	I687	TRUE	XDP_OBS20	12
	I686	TRUE	SMBUS_MCP_0_DATA	12 20 42 68
	I680	TRUE	SMBUS_MCP_0_CLK	12 20 42 68
	I697	TRUE	XDP_TCK	8 12 65
	I691	TRUE	JTAG_MCP_TDO_CONN	12
	I690	TRUE	JTAG_MCP_TRST_L	12 20
	I692	TRUE	MCP_DEBUG<7..0>	12 18 68
	I694	TRUE	JTAG_MCP_TDI	12 20
	I695	TRUE	JTAG_MCP_TMS	12 20
	I698	TRUE	FSB_CLK_ITP_P	12 13 65
	I697	TRUE	FSB_CLK_ITP_N	12 13 65
	I698	TRUE	XDP_CPURST_L	12 65
	I699	TRUE	XDP_DBRESET_L	8 12 24
	I701	TRUE	XDP_TDO_CONN	12
	I700	TRUE	XDP_TRST_L	8 12 65
	I702	TRUE	XDP_TDI	8 12 65
	I703	TRUE	XDP_TMS	8 12 65
	I704	TRUE	=PP3V3_S0_XDP	7 12
	I705	TRUE	=PP1V05_S0_CPU	7 8 10 11 12

FUNC TEST - CAMERA USB, LVDS, ALS

x2	I654	TRUE	PP5V_S3_CAMERA_F	59 70
	I655	TRUE	USB2_CAMERA_F_P	59
	I656	TRUE	USB2_CAMERA_F_N	59
	I657	TRUE	LCDBKLT_RTN<1..6>	59 62
	I658	TRUE	LVDS_IG_A_DATA_N<0..2>	17 59 67
	I659	TRUE	LVDS_IG_A_DATA_P<0..2>	17 59 67
	I660	TRUE	PPVOUT_S0_LCDBKLT	59 62 70
	I661	TRUE	LVDS_IG_A_CLK_F_N	59 67
	I662	TRUE	LVDS_IG_A_CLK_F_P	59 67
	I663	TRUE	LVDS_IG_DDC_CLK	17 59
	I664	TRUE	LVDS_IG_DDC_DATA	17 59
	I665	TRUE	PP3V3_S0_LCD_F	59 70
x2	I666	TRUE	PP3V3_LCDVDD_SW_F	59 70
	I711	TRUE	=I2C_ALS_SDA	42 59
	I712	TRUE	=I2C_ALS_SCL	42 59
x10	I713	TRUE	GND	

x13 I822 TRUE GND

Functional Test and No-Tests

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 7 OF 109	

"S0" RAILS

50 =PPVCORE_S0_CPU_REG
27 A
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVCORE_S0_CPU 10 11 64

51 =PPMCPCORE_S0_REG
11.551 A
PPMCPCORE_S0
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
=PPVCORE_S0_MCP 21 22
=PPVCORE_S0_MCP_VSENSE 43

54 =PP0V75_S0_REG
1.075 A
PP0V75_S0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPVTT_S0_VTTCLAMP 57
=PP0V75_S0_MEM_VTT_A 33
=PP0V75_S0_MEM_VTT_B 33

57 =PP1V05_S0_FET
7.047 A
PP1V05_S0
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S0_CPU 6 9 10 11 12
=PP1V05_S0_MCP_AVDD_UF 22
=PP1V05_S0_MCP_FSB 8 13 21 22
=PP1V05_S0_MCP_HDMI_VDD 17 23
=PP1V05_S0_MCP_PEX_DVDD 7 22
=PP1V05_S0_MCP_PLL_UF 22
=PP1V05_S0_MCP_SATA_DVDD 19 22
=PP1V05_S0_SMC_LS 40
=PP1V05_S0_VMON 56

57 =PP1V5_S0_FET
5.027 A
PP1V5_S0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V5_S0_CPU 10 11
=PP1V5_S0_VMON 56
=PP1V8R1V5_S0_MCP_MEM 15 22 66

52 =PP1V8_S0_REG
19 mA
PP1V8_S0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP3V3R1V8_S0_MCP_IFP_VDD 17 23

57 =PP3V3_S0_FET
2.046 A
PP3V3_S0
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S0_DPCONN 61
=PP3V3_S0_FAN 46
=PP3V3_S0_IMVP 50
=PP3V3_S0_LCD 59
=PP3V3_S0_LCDBKLT 62
=PP3V3_S0_MCP 20 21 22
=PP3V3_S0_MCP_GPIO 17 18 20
=PP3V3_S0_MCP_PLL_UF 22
=PP3V3_S0_MCP_VPLL_UF 23
=PP3V3_S0_PWRCTL 24 56
=PP3V3_S0_SMBUS_SMC_0_S0 42
=PP3V3_S0_THRM_SNR 45
=PP3V3_S0_VMON 56
=PP3V3_S0_XDP 6 12
=PPVIN_S0_P1V8S0 52
=PP3V3_S0_LPCPLUS 41
=PP3V3_S0_HDD 36
=PP3V3_S0_SMBUS_SMC_B_S0 42
=PP3V3_S0_SMBUS_MCP_0 42
=PP3V3R1V5_S0_MCP_HDA 20 22
=PP3V3_S0_SMC_LS 40
=PP3V3_S0_MIC 59

57 =PP5V_S0_FET
562 mA
PP5V_S0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_CPU_IMVP 50
=PP5V_S0_DP_AUX_MUX 60
=PP5V_S0_FAN 6 46
=PP5V_S0_KBDLED 38
=PP5V_S0_LPCPLUS 41

"S3" RAILS

54 =PP0V75_S3_VTTREF
1.075 A
PP0V75_S3
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
=PPVTT_S3_DDR_BUF 25

54 =PP1V5_S3_REG
12.984 A
PP1V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V5_S3_MEM_A 27 28 31 33
=PP1V5_S3_MEM_B 29 30 32 33
=PP1V5_S3_P1V5S0FET 57
=PP1V5_S3_MEMRESET 26

57 =PP3V3_S3_FET
315 mA
PP3V3_S3
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S3_BT 34
=PP3V3_S3_SMBUS_SMC_A_S3 42
=PP3V3_S3_SMC 40
=PP3V3_S3_SMS 47
=PP3V3_S3_VREFMRGN 25
=PP3V3_S3_SMBUS_SMC_MGMT 42
=PP3V3_S3_DDRREG 54
=PP3V3_S3_MCPREG 51
=PP3V3_S3_MCP_GPIO 20

55 =PP5V_S3_REG
3.134 A
PP5V_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S3_CAMERA 59
=PP5V_S3_MCPDDRFET 57
=PP5V_S3_P1V05S0FET 57
=PP5V_S3_TOPCASE 38
=PP5V_S3_VTTCLAMP 57
=PP5V_S3_1V5S30V75S0 54
=PP5V_S3_EXTUSB 37
=PP5V_S3_P5VS0FET 57
=PP5V_S3_MCPREG 51

"RMGT" RAILS

57 =PP3V3_RMGT_FET
PP3V3_RMGT
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_ENET_MCP_RMGT 17 22

57 =PP1V05_RMGT_FET
PP1V05_RMGT
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_ENET_MCP_RMGT 17 22
=PP1V05_ENET_MCP_PLL_MAC 22

"S5" RAILS

53 =PP1V05_S5_REG
7.368 A
PP1V05_S5
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V05_S5_MCP_VDD_AUXC 21 22
=PP1V05_S5_P1V05S0FET 57
=PP1V05_RMGT_P1V05RMGTFET 57

55 =PP3V3_S5_REG
4.011 A
PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S5_AIRPORT_AUX 34
=PP3V3_S5_LCD 59
=PP3V3_S5_MCP 21 22
=PP3V3_S5_MCPPWRGD 24
=PP3V3_S5_MCP_GPIO 17 19 20
=PP3V3_S5_P1V05FET 57
=PP3V3_S5_P3V3S0FET 57
=PP3V3_S5_P3V3S3FET 57
=PP3V3_S5_PWRCTL 56
=PP3V3_S5_ROM 41 48
=PP3V3_S5_SMBUS_MCP_1 42
=PP3V3_S5_MEMRESET 26
=PP3V3_S5_P3V3RMGTFET 57
=PP3V3_S5_P1V05RMGTFET 57

"G3H" RAILS

49 24 =PP3V42_G3H_REG
165 mA
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
=PP3V42_G3H_SMC 39 40
=PP3V42_G3H_SMCVREF 40
=PP3V42_G3H_SMBUS_SMC_BSA 42
=PP3V42_G3H_IPD 38
=PP3V42_G3H_SMCUSBMUX 37
=PP3V42_G3H_CHGR 58
=PP3V42_G3H_LPCPLUS 41

58 49 =PP18V5_G3H_CHGR
PP18V5_G3H
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE

49 =PPDCIN_G3H
PPDCIN_G3H
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
=PPVIN_G3H_P3V42G3H 49

58 44 =PPBUSA_G3H
13 A
PPBUS_R_G3H
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S5_CPU_IMVP 50
=PPVIN_S5_1V5S30V75S0 54
=PPVIN_S0_MCPCORES0 51
=PPVIN_S5_1V05 53

58 44 =PPBUSB_G3H
6.207 A
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVIN_S3_5VS3 55
=PPVIN_S5_3V3S5 55
=PPVIN_S0_AUDIO 6 35
=PPVIN_G3H_DCIN 49
=PPBUS_S0_LCDBKLT 63
=PPBUS_G3HRS5 43

PEX & SATA AVDD/DVDD aliases

70 22 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
206 mA (A01)
=PP1V05_S0_MCP_PEX_AVDD0 16
=PP1V05_S0_MCP_PEX_AVDD1 16
206 mA (A01)

22 7 =PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)
=PP1V05_S0_MCP_PEX_DVDD0 16
=PP1V05_S0_MCP_PEX_DVDD1 16
57 mA (A01)

Power Aliases

SYNC_MASTER=WFERRY SYNC_DATE=06/15/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 8 OF 109	

EMI SPRING CLIPS

PLACE CLIPS PER MCO ON TOPSIDE NEAR BATTERY CONNECTOR J6900

CRITICAL
SC0900
EMI_SPRING
PS-25N

BOSSES

Z0900 4.5OD2.0H-M1.6X0.35
Z0901 4.5OD2.0H-M1.6X0.35
Z0902 4.5OD2.0H-M1.6X0.35
Z0903 4.5OD2.0H-M1.6X0.35
Z0904 4.5OD2.0H-M1.6X0.35

STANDOFFS

Z0910 STDOFF-4.0OD2.4H-0.5-THNP
Z0911 STDOFF-4.0OD2.4H-0.5-THNP
Z0912 STDOFF-4.0OD2.4H-0.5-THNP

SMC ALIASES

NO-CONNECT UNUSED SMC INTERFACE PORTS

		NO_TEST
SMC_PA0	NC_SMC_PA0	TRUE
SMC_PA1	NC_SMC_PA1	TRUE
SMC_ESTARLDO_EN	NC_SMC_ESTARLDO_EN	TRUE
SMC_P26	NC_SMC_P26	TRUE
SMC_P41	NC_SMC_P41	TRUE
SMC_BIL_BUTTON_L	NC_SMC_P67	TRUE
SMC_GFX_OVERTEMP_L	NC_SMC_GFX_OVERTEMP_L	TRUE
SMC_EXCARD_OC_L	NC_EXCARD_OC_L	TRUE
SMC_P24	NC_SMC_P24	TRUE
SMC_EXCARD_CP	NC_SMC_EXCARD_CP	TRUE
ALS_RIGHT	NC_ALS_RIGHT	TRUE
ALS_GAIN	NC_ALS_GAIN	TRUE
SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	TRUE
SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	TRUE
SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	TRUE
SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	TRUE
SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	TRUE
SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	TRUE
SMC_EXCARD_PWR_EN	NC_SMC_RSTGATE_L	TRUE
ISENSE_CAL_EN	NC_ISENSE_CAL_EN	TRUE
SMC_FWE	NC_SMC_FWE	TRUE
SMC_ANALOG_ID	NC_SMC_ANALOG_ID	TRUE
ALS_LEFT	NC_ALS_LEFT	TRUE
SMC_NB_DDR_ISENSE	NC_SMC_NB_DDR_ISENSE	TRUE
SMC_P10	NC_SMC_P10	TRUE
SMC_PA5	NC_SMC_PA5	TRUE
SMC_GPU_ISENSE	NC_SMC_GPU_ISENSE	TRUE

MAKE_BASE=TRUE

SMC_IG_THROTTLE_L — SMC_GFX_THROTTLE_L
SMC_SMS_INT_L — =SMC_SMS_INT
SMC_ADAPTER_EN — SMC_ADAPTER_PRESENT

PCI-E ALIASES

UNUSED GPU LANES

=PEG_D2R_N<15:0>	NC_PEG_D2R_N<15:0>
=PEG_D2R_P<15:0>	NC_PEG_D2R_P<15:0>
=PEG_R2D_C_N<15:0>	NC_PEG_R2D_C_N<15:0>
=PEG_R2D_C_P<15:0>	NC_PEG_R2D_C_P<15:0>
PEG_PRSNT_L	TP_PEG_PRSNT_L
PEG_CLKREQ_L	TP_PEG_CLKREQ_L
PEG_CLK100M_P	TP_PEG_CLK100M_P
PEG_CLK100M_N	TP_PEG_CLK100M_N
EXTGPU_PWR_EN	TP_EXTGPU_PWR_EN
EXTGPU_RESET_L	TP_EXTGPU_RESET_L

NO_TEST=TRUE MAKE_BASE=TRUE

AIRPORT CARD AND TURBOMEM PRESENT SIGNAL

PCIE_MINI_PRSNT_L
PCIE_FC_PRSNT_L
MAKE_BASE=TRUE

HDA PULL-DOWN

UNUSED IPHS SIGNAL(FOR IPHONE JACK)

AUD_IPHS_SWITCH_EN

AUD_I2C_INT_L IS PU ON MCP PAGE

R0920 100K 5% 1/20W MF 201

DP HOTPLUG PULL-DOWN

HPLUG_DET2 — =DVI_HPD_GMUX_INT
MAKE_BASE=TRUE

R0940 20K 5% 1/20W MF 201

LAN ALIASES

UNUSED ETHERNET RG/MII INTERFACE

ENET_RXD<0>
ENET_RXD<1>
ENET_RXD<2>
ENET_RXD<3>
ENET_MDIO
ENET_RX_CTRL
ENET_CLK125M_TXCLK
MCP_MII_VREF
ENET_CLK125M_RXCLK
ENET_INTR_L

RP0930 10K 5% 1/32W 4X0201-HF (8 7 6 5 / 1 2 3 4)
RP0931 10K 5% 1/32W 4X0201-HF (8 7 6 5 / 1 2 3 4)
RP0932 10K 5% 1/32W 4X0201-HF (8 7 6 5 / 1 2 3 4)

ENET_RESET_L	NC_ENET_RESET_L
MCP_CLK25M_BUF0_R	NC_MCP_CLK25M_BUF0_R
ENET_PWRDWN_L	NC_ENET_PWRDWN_L
ENET_MDC	NC_ENET_MDC
ENET_TX_CTRL	NC_ENEX_TX_CTRL
ENET_TXD<3..0>	NC_ENET_TXD<3..0>

MAKE_BASE=TRUE

GND
VOLTAGE=0V
MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.30 MM

DACS ALIASES

UNUSED CRT & TV-OUT INTERFACE

MCP_TV_DAC_RSET	NC_MCP_TV_DAC_RSET
MCP_TV_DAC_VREF	NC_MCP_TV_DAC_VREF
MCP_CLK27M_XTALIN	NC_MCP_CLK27M_XTALIN
MCP_CLK27M_XTALOUT	NC_MCP_CLK27M_XTALOUT
CRT_IG_R_C_PR	NC_CRT_IG_R_C_PR
CRT_IG_G_Y_Y	NC_CRT_IG_G_Y_Y
CRT_IG_B_COMP_PB	NC_CRT_IG_B_COMP_PB
CRT_IG_HSYNC	NC_CRT_IG_HSYNC
CRT_IG_VSYNC	NC_CRT_IG_VSYNC

NO_TEST=TRUE MAKE_BASE=TRUE

LVDS ALIASES

UNUSED LVDS SIGNALS

LVDS_IG_A_DATA_P<3>	NC_LVDS_IG_A_DATA_P3
LVDS_IG_A_DATA_N<3>	NC_LVDS_IG_A_DATA_N3
LVDS_IG_B_CLK_P	NC_LVDS_IG_B_CLK_P
LVDS_IG_B_CLK_N	NC_LVDS_IG_B_CLK_N
LVDS_IG_B_DATA_P<3:0>	NC_LVDS_IG_B_DATA_P<3:0>
LVDS_IG_B_DATA_N<3:0>	NC_LVDS_IG_B_DATA_N<3:0>

NO_TEST=TRUE MAKE_BASE=TRUE

MISC NC MCP79 ALIASES

CPU_PECI_MCP	TP_CPU_PECI_MCP
FW_PME_L	TP_FW_PME_L
ODD_PWR_EN_L	TP_ODD_PWR_EN_L

MAKE_BASE=TRUE

SATA ALIASES

UNUSED SATA ODD SIGNALS

SATA_ODD_R2D_C_P	TP_SATA_ODD_R2D_C_P
SATA_ODD_R2D_C_N	TP_SATA_ODD_R2D_C_N
SATA_ODD_D2R_P	TP_SATA_ODD_D2R_P
SATA_ODD_D2R_N	TP_SATA_ODD_D2R_N

MAKE_BASE=TRUE

USB ALIASES

UNUSED USB PORTS

USB_EXTB_P	TP_USB_EXTB_P
USB_EXTB_N	TP_USB_EXTB_N
USB_EXTC_P	TP_USB_EXTC_P
USB_EXTC_N	TP_USB_EXTC_N
USB_EXTD_P	TP_USB_EXTD_P
USB_EXTD_N	TP_USB_EXTD_N
USB_EXCARD_P	TP_USB_EXCARD_P
USB_EXCARD_N	TP_USB_EXCARD_N
USB_MINI_P	TP_USB_MINI_P
USB_MINI_N	TP_USB_MINI_N

MAKE_BASE=TRUE

EXTERNAL PORT A

=USB2_EXTA_P	USB_EXTA_P	19 68
=USB2_EXTA_N	USB_EXTA_N	19 68
=EXTAUSB_OC_L	USB_EXTA_OC_L	19

CAMERA

=USB2_CAMERA_P	USB_CAMERA_P	19 68
=USB2_CAMERA_N	USB_CAMERA_N	19 68

TRACKPAD(WELLSPRING)

=USB2_TPAD_P	USB_TPAD_P	19 68
=USB2_TPAD_N	USB_TPAD_N	19 68

IR

=USB2_IR_P	USB_IR_P	19 68
=USB2_IR_N	USB_IR_N	19 68

BT (M93)

=USB2_BT_P	USB_BT_P	19 68
=USB2_BT_N	USB_BT_N	19 68

MAKE_BASE=TRUE

CPU FSB FREQUENCY STRAPS

CPU_BSEL<0:2> — =MCP_BSEL<0:2>
MAKE_BASE=TRUE

BSEL<2..0>	FSB MHZ
0 0 0	266
0 0 1	133
0 1 0	200
0 1 1	(166)
1 0 0	333
1 0 1	100
1 1 0	(400)
1 1 1	(RSVD)

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa

=PP1V05_S0_MCP_FSB

R0995 220 1/20W MF 201 — NO STUFF
R0997 200 5% 1/20W MF 201 — NO STUFF
R0999 150 5% 1/20W MF 201 — NO STUFF
R0996 62 5% 1/20W MF 201 — NO STUFF
R0998 150 5% 1/20W MF 201 — NO STUFF

CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI

MEM ALIASES

		NO_TEST
TP_MEM_A_CLK4P	NC_MEM_A_CLK4P	TRUE
TP_MEM_A_CLK4N	NC_MEM_A_CLK4N	TRUE
TP_MEM_A_CLK3P	NC_MEM_A_CLK3P	TRUE
TP_MEM_A_CLK3N	NC_MEM_A_CLK3N	TRUE
TP_MEM_A_CS_L<2>	NC_MEM_A_CS_L<2>	TRUE
TP_MEM_A_CS_L<3>	NC_MEM_A_CS_L<3>	TRUE
TP_MEM_A_CKE<2>	NC_MEM_A_CKE<2>	TRUE
TP_MEM_A_CKE<3>	NC_MEM_A_CKE<3>	TRUE
TP_MEM_B_CLK4P	NC_MEM_B_CLK4P	TRUE
TP_MEM_B_CLK4N	NC_MEM_B_CLK4N	TRUE
TP_MEM_B_CLK3P	NC_MEM_B_CLK3P	TRUE
TP_MEM_B_CLK3N	NC_MEM_B_CLK3N	TRUE
TP_MEM_B_CS_L<2>	NC_MEM_B_CS_L<2>	TRUE
TP_MEM_B_CS_L<3>	NC_MEM_B_CS_L<3>	TRUE
TP_MEM_B_ODT<2>	NC_MEM_B_ODT<2>	TRUE
TP_MEM_B_ODT<3>	NC_MEM_B_ODT<3>	TRUE
TP_MEM_B_CKE<2>	NC_MEM_B_CKE<2>	TRUE
TP_MEM_B_CKE<3>	NC_MEM_B_CKE<3>	TRUE

MAKE_BASE=TRUE

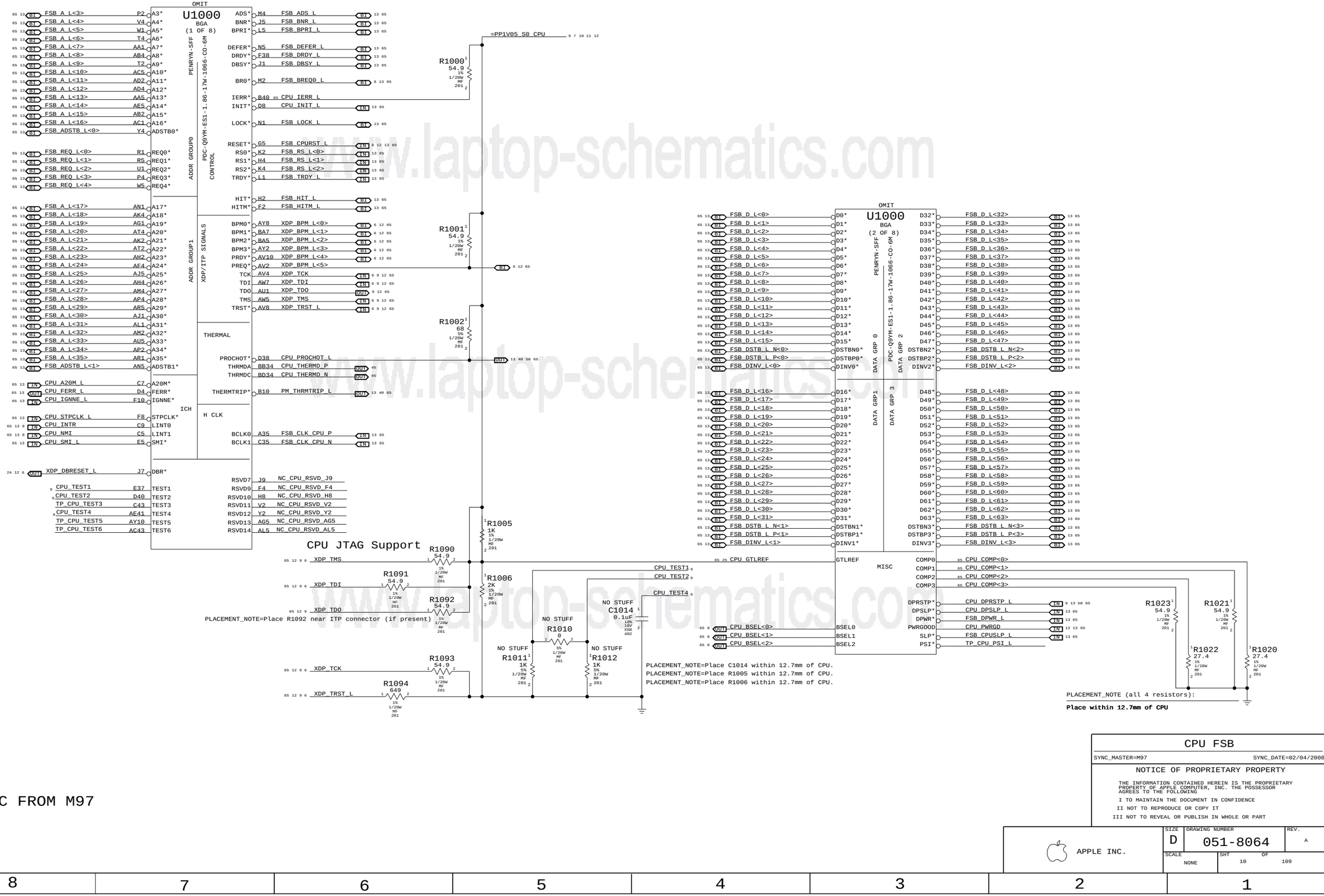
SIGNAL ALIAS /RESET

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE: NONE SHT 9 OF 109



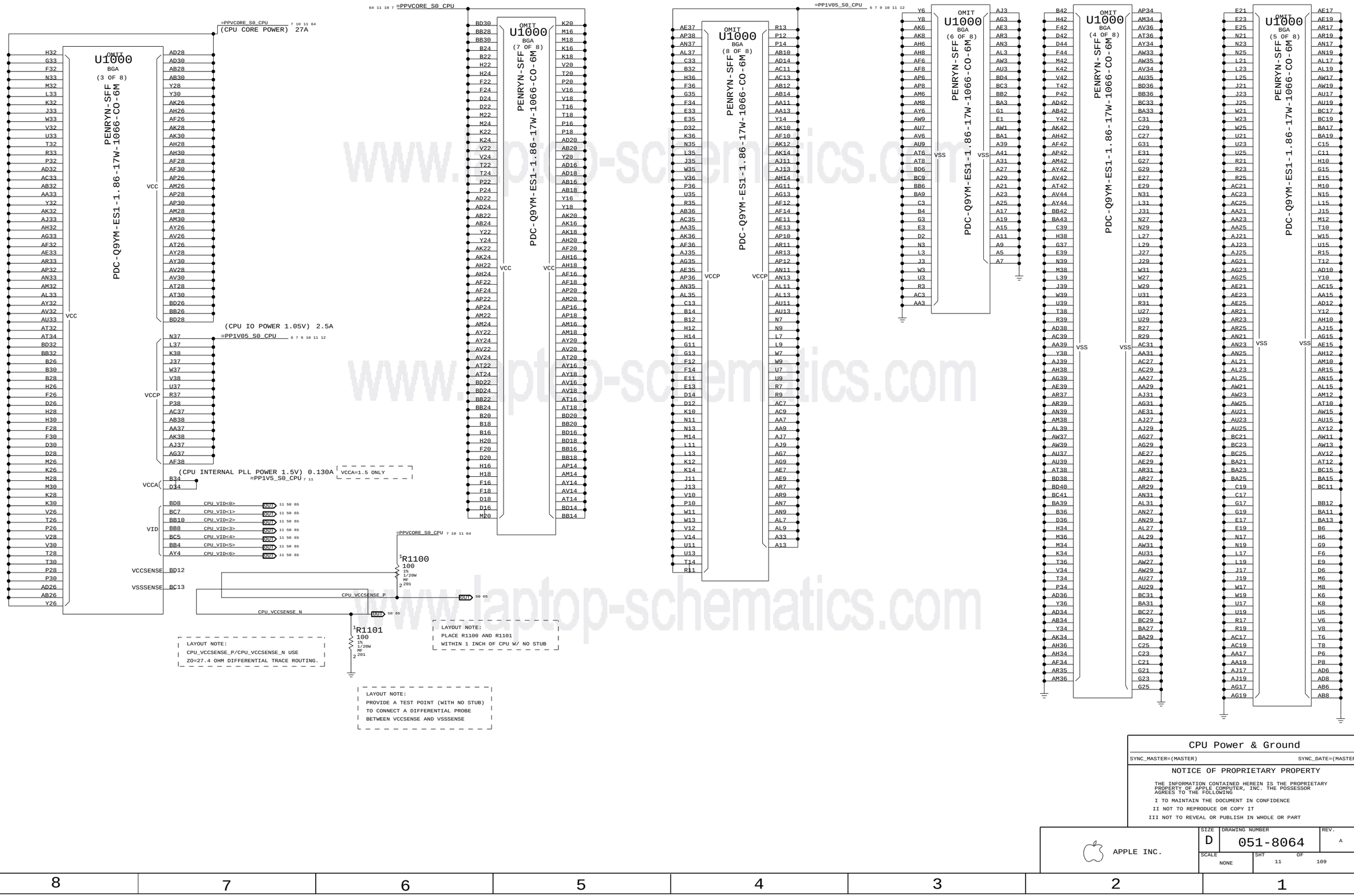
SYNC FROM M97

CPU FSB

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 10 OF 109	



CPU VCORE HF AND BULK DECOUPLING

3x 330uF. 32x 10uF 0603, 28x 2.2uF 0402 + 40x 2.2uF 0402

64 10 7 =PPVCORE_S0_CPU

10UF 0603 = APN:138S0568 = MURATA,TAIYO,TDK,SAMSUNG

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1200 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1201 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1202 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1203 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1204 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1205 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1206 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1207 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1208 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1209 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1210 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1211 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1212 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1213 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1214 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1215 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1216 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1217 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1218 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1219 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1220 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1221 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1222 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1223 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1224 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1225 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1226 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1227 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1228 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1229 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1230 10UF 20% 6.3V OMIT X5R 603
CRITICAL C1231 10UF 20% 6.3V OMIT X5R 603

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1240 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1241 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1242 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1243 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1244 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1245 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1246 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1247 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1248 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1249 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1250 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1251 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1252 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1253 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1254 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1255 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1256 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1257 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1258 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1259 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C1260 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1261 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1262 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1263 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1264 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1265 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1266 2.2UF 20% 6.3V CERM OMIT 402-LF
CRITICAL C1267 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CRITICAL C1270 330UF 20% 2.0V POLY-TANT D2T-SM1
CRITICAL C1271 330UF 20% 2.0V POLY-TANT D2T-SM1

Intel recommends 3x220UF @ 9mOHM

CRITICAL C1272 330UF 20% 2.0V POLY-TANT D2T-SM1

LAYOUT NOTE:
PLACE ON SAME SIDE AS CPU

CPU VCORE VID CONNECTIONS

65 50 10 CPU_VID<0..6> — IMVP6_VID<0..6> 65
MAKE_BASE=TRUE

VCCA (CPU AVdd) DECOUPLING

10 7 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

C1280 10uF OMIT 20% 6.3V X5R 603
C1281 0.01UF 10% 10V X5R 201

LAYOUT NOTE:
PLACE C1281 NEAR PIN B34 OF U1000

VCCP (CPU I/O) DECOUPLING

12 10 9 7 6 =PP1V05_S0_CPU

1X 330UF, 12X 2.2UF

C1283 2.2UF 20% 6.3V CERM OMIT 402-LF
C1284 2.2UF 20% 6.3V CERM OMIT 402-LF
C1285 2.2UF 20% 6.3V CERM OMIT 402-LF
C1286 2.2UF 20% 6.3V CERM OMIT 402-LF
C1287 2.2UF 20% 6.3V CERM OMIT 402-LF
C1288 2.2UF 20% 6.3V CERM OMIT 402-LF

CRITICAL C1290 330UF 20% 2.5V POLY-TANT CASE-C2-SM

C1291 2.2UF 20% 6.3V CERM OMIT 402-LF
C1292 2.2UF 20% 6.3V CERM OMIT 402-LF
C1293 2.2UF 20% 6.3V CERM OMIT 402-LF
C1294 2.2UF 20% 6.3V CERM OMIT 402-LF
C1295 2.2UF 20% 6.3V CERM OMIT 402-LF
C1296 2.2UF 20% 6.3V CERM OMIT 402-LF

LAYOUT NOTE:
PLACE C1290 CLOSE TO CPU
PLACE C1283-C1288 CLOSE TO FSB ADDRESS PINS
PLACE C1291-C1296 CLOSE TO FSB DATA PINS

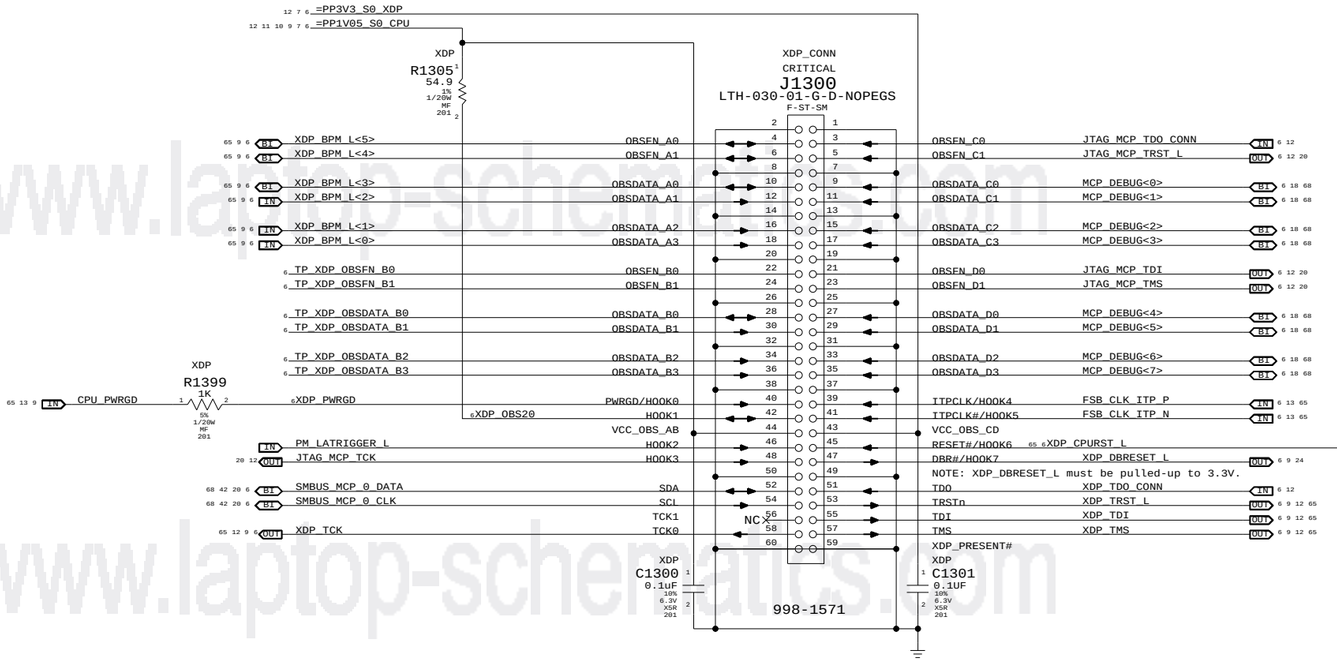
CPU Decoupling & VID

SYNC_MASTER=MSARWAR SYNC_DATE=04/26/2006

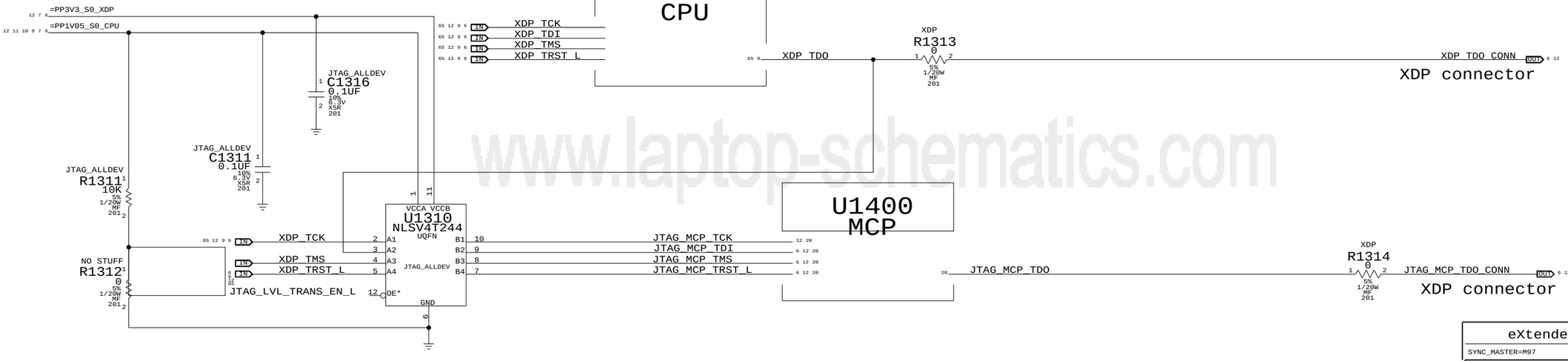
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 12 OF 109	

MCP79-specific pinout



From XDP connector



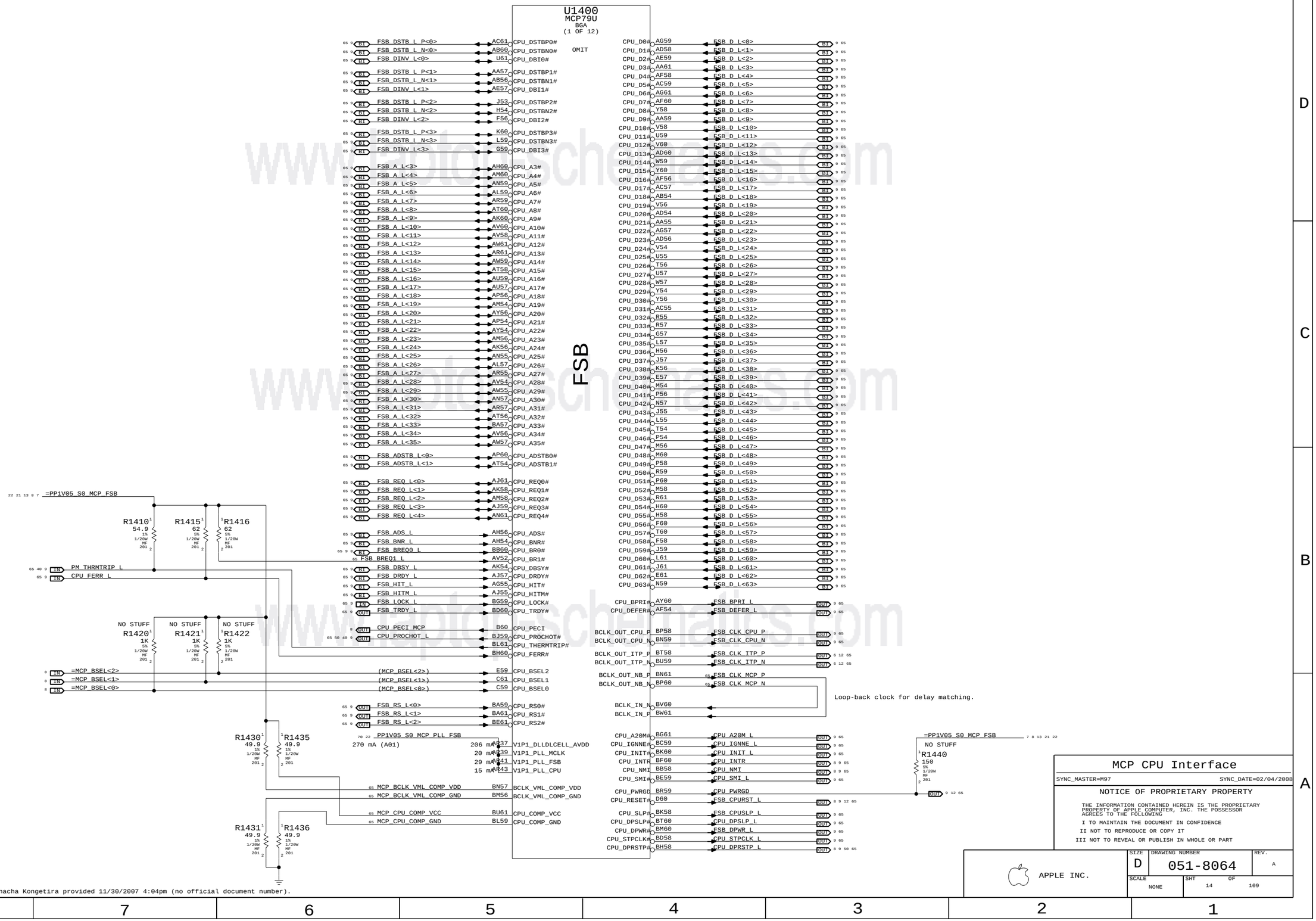
eXtended Debug Port (XDP)

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

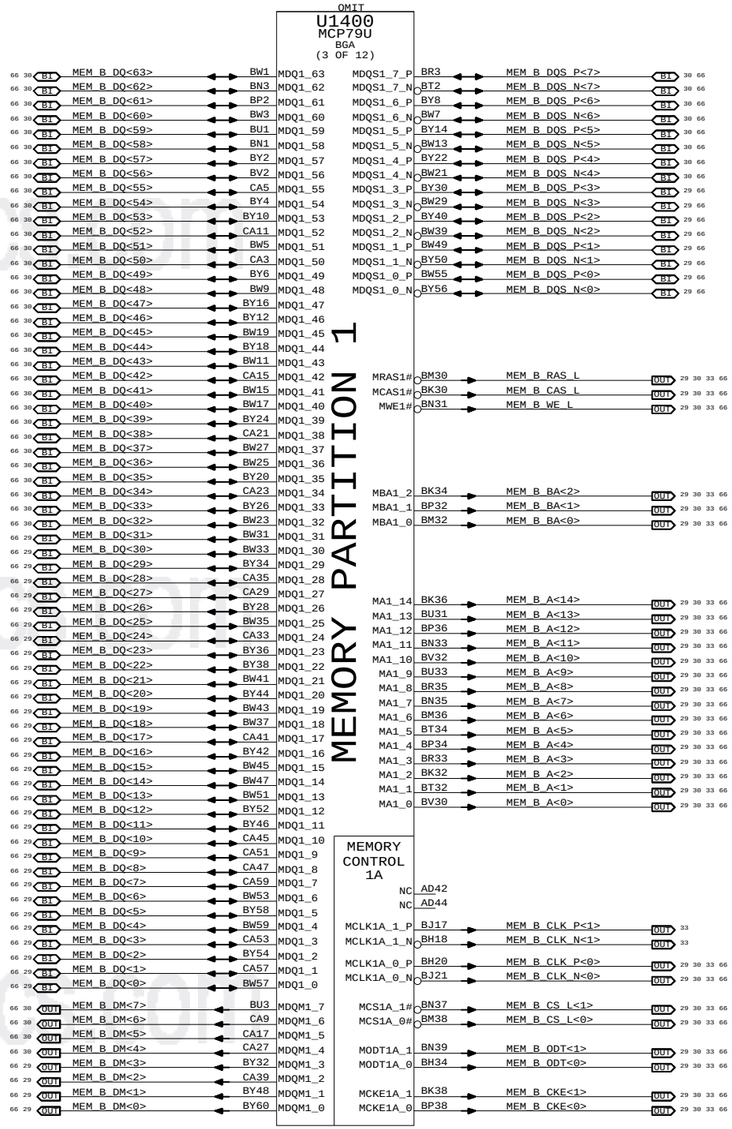
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	13	109



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



MCP Memory Interface

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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SIZE	DRAWING NUMBER	REV.
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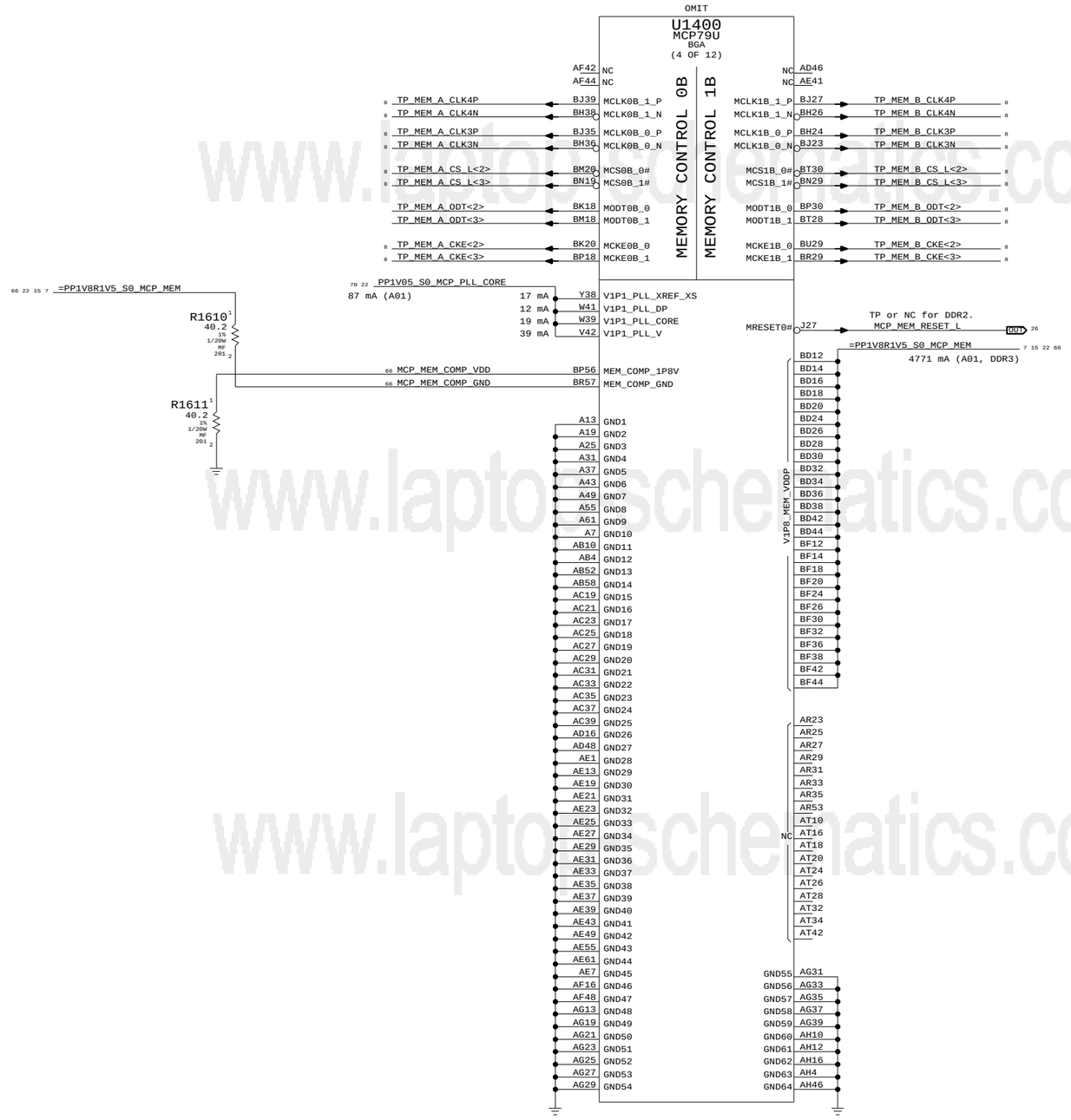
SCALE: NONE	SHT 15 OF 109	



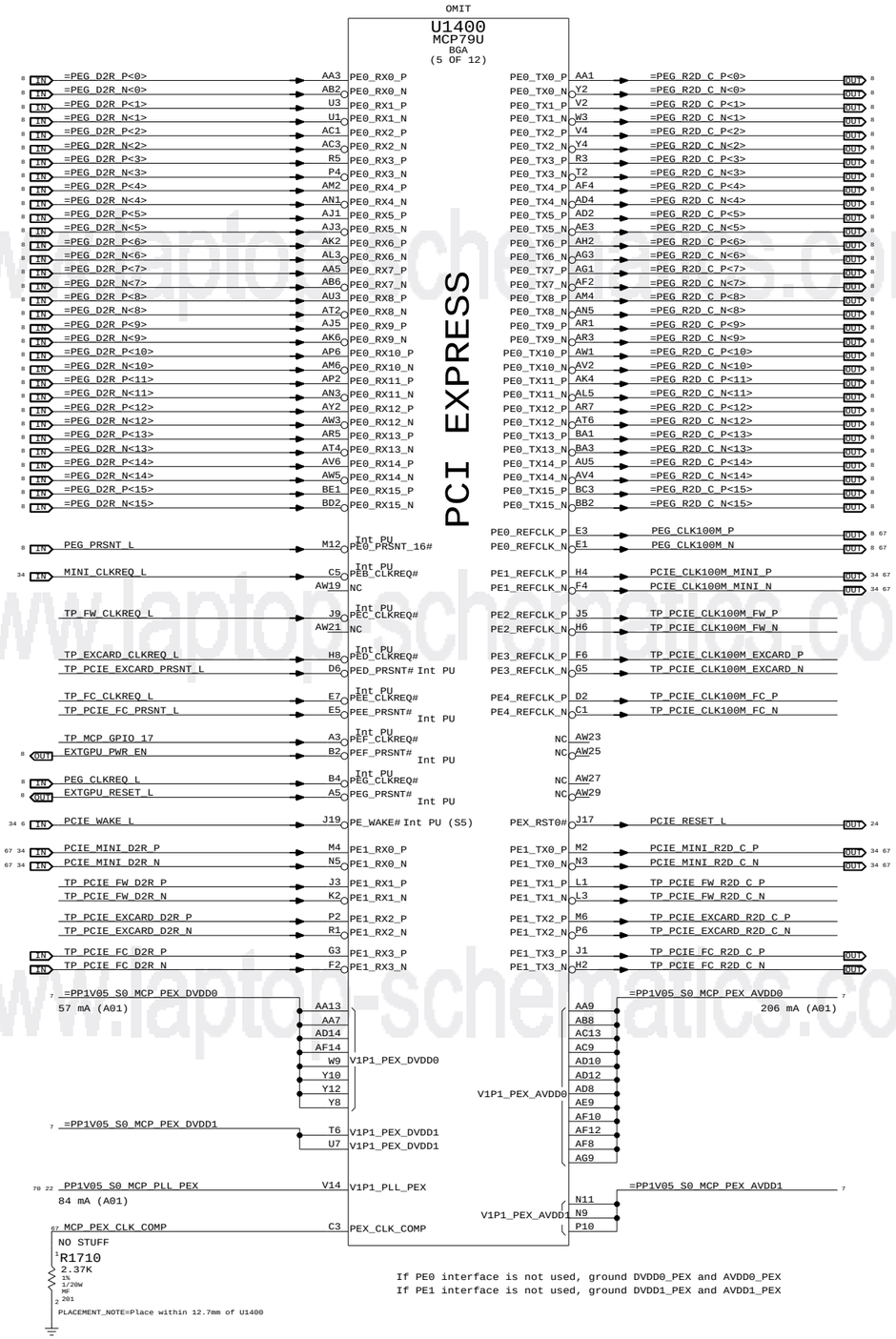
MCP Memory Misc

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 16 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



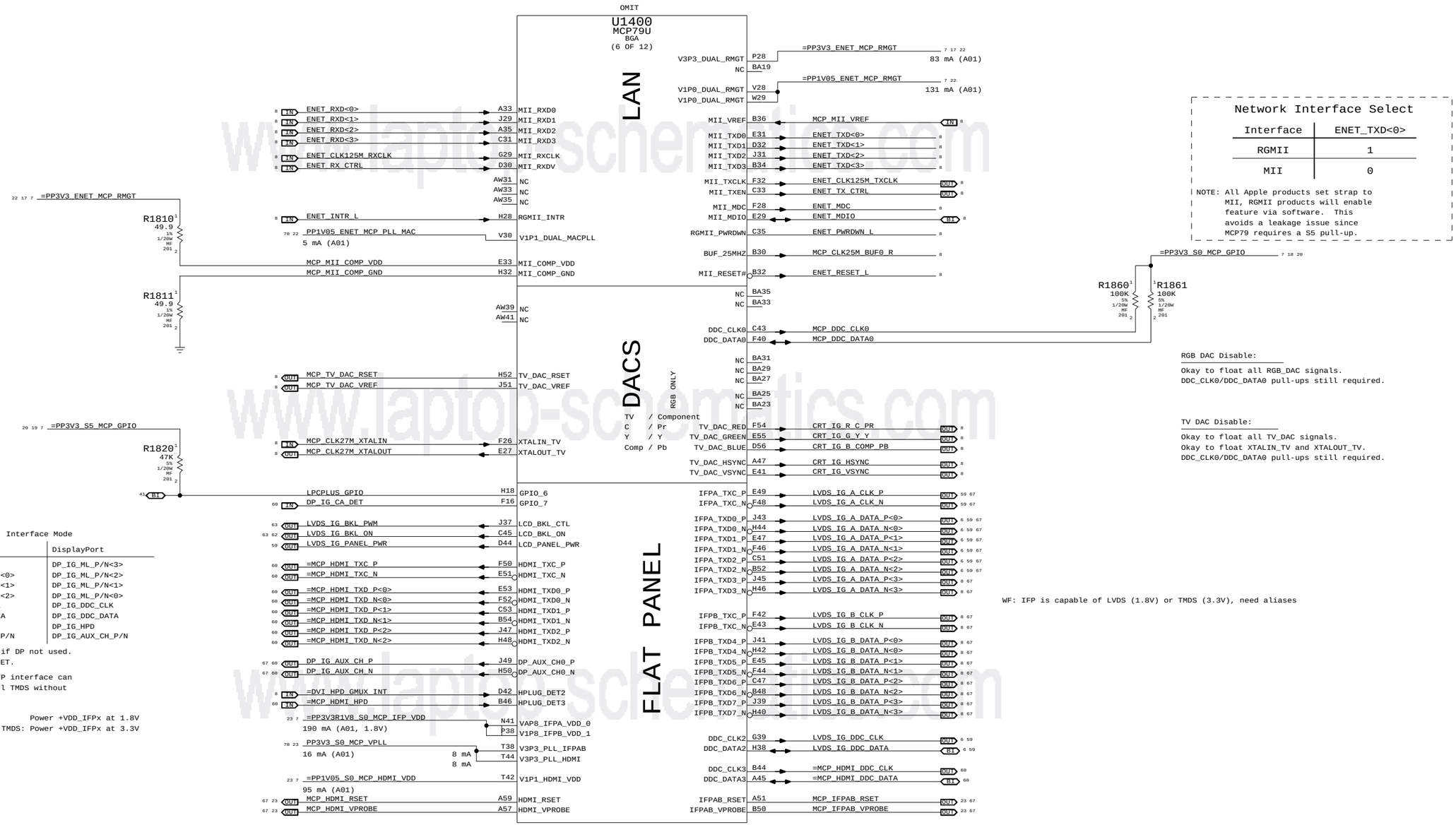
MCP PCIe Interfaces

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 17 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HOTPLUG_DET.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

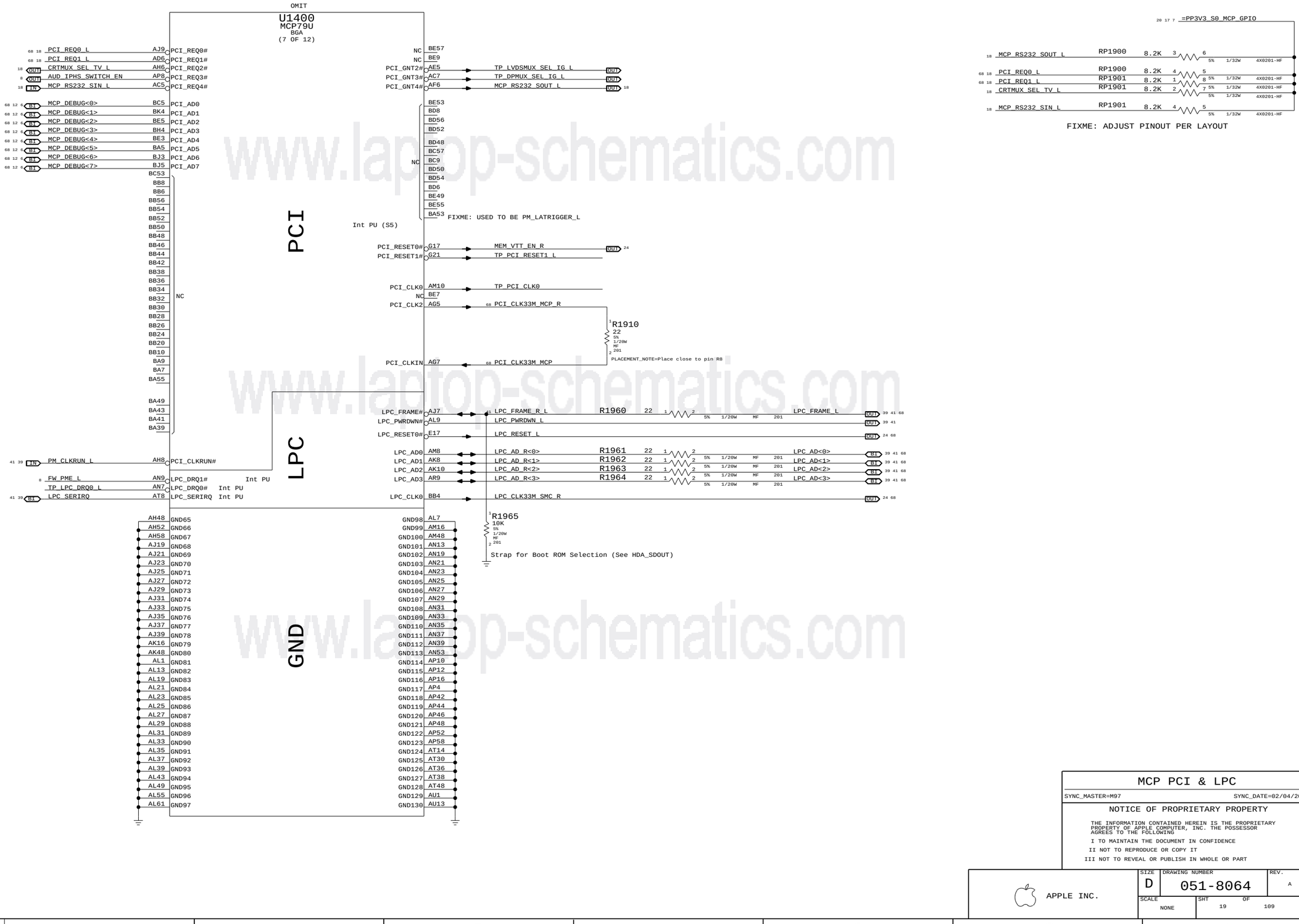
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Ethernet & Graphics

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 18 OF 109	



MCP PCI & LPC

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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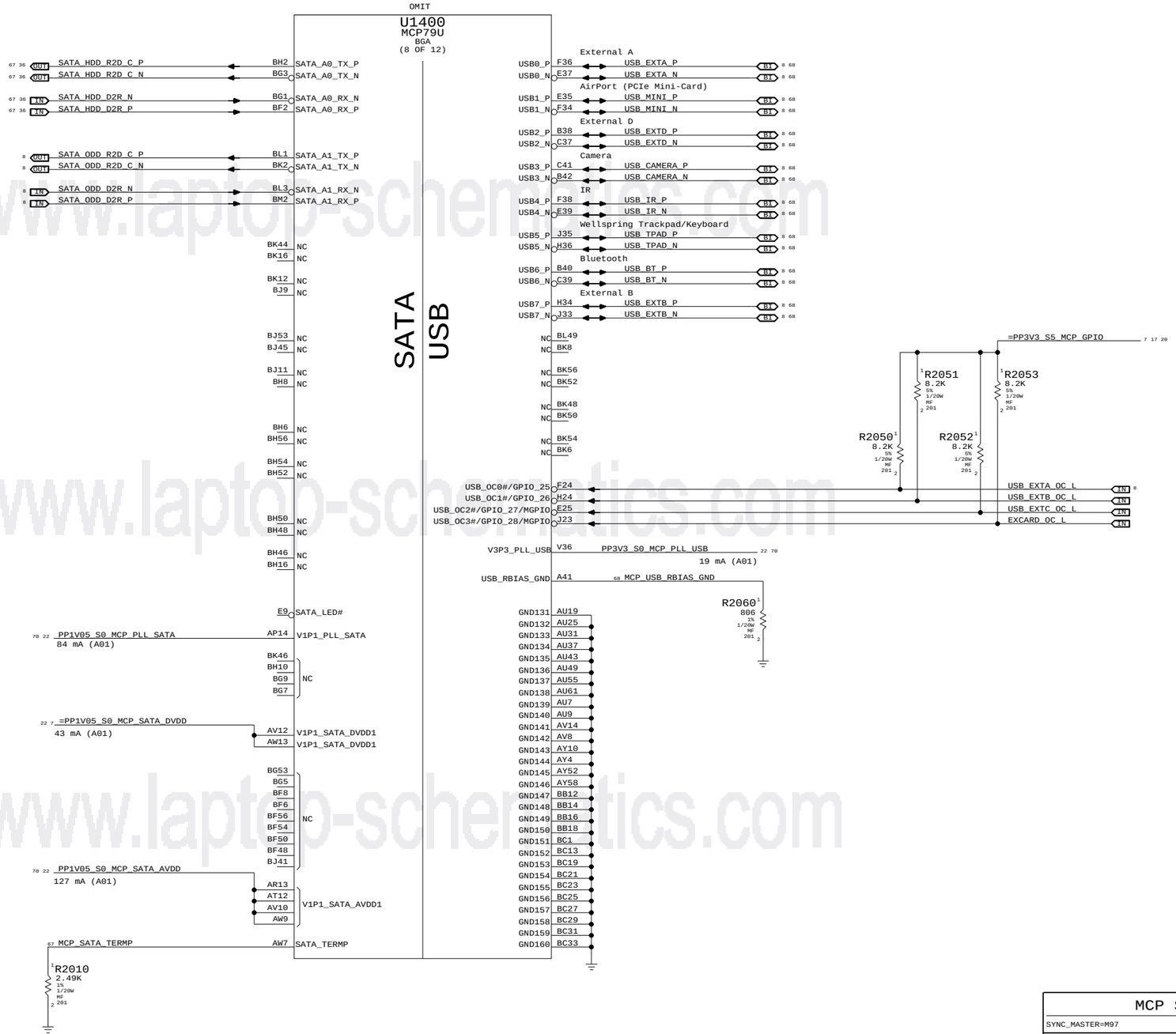
SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	19	109



MCP SATA & USB

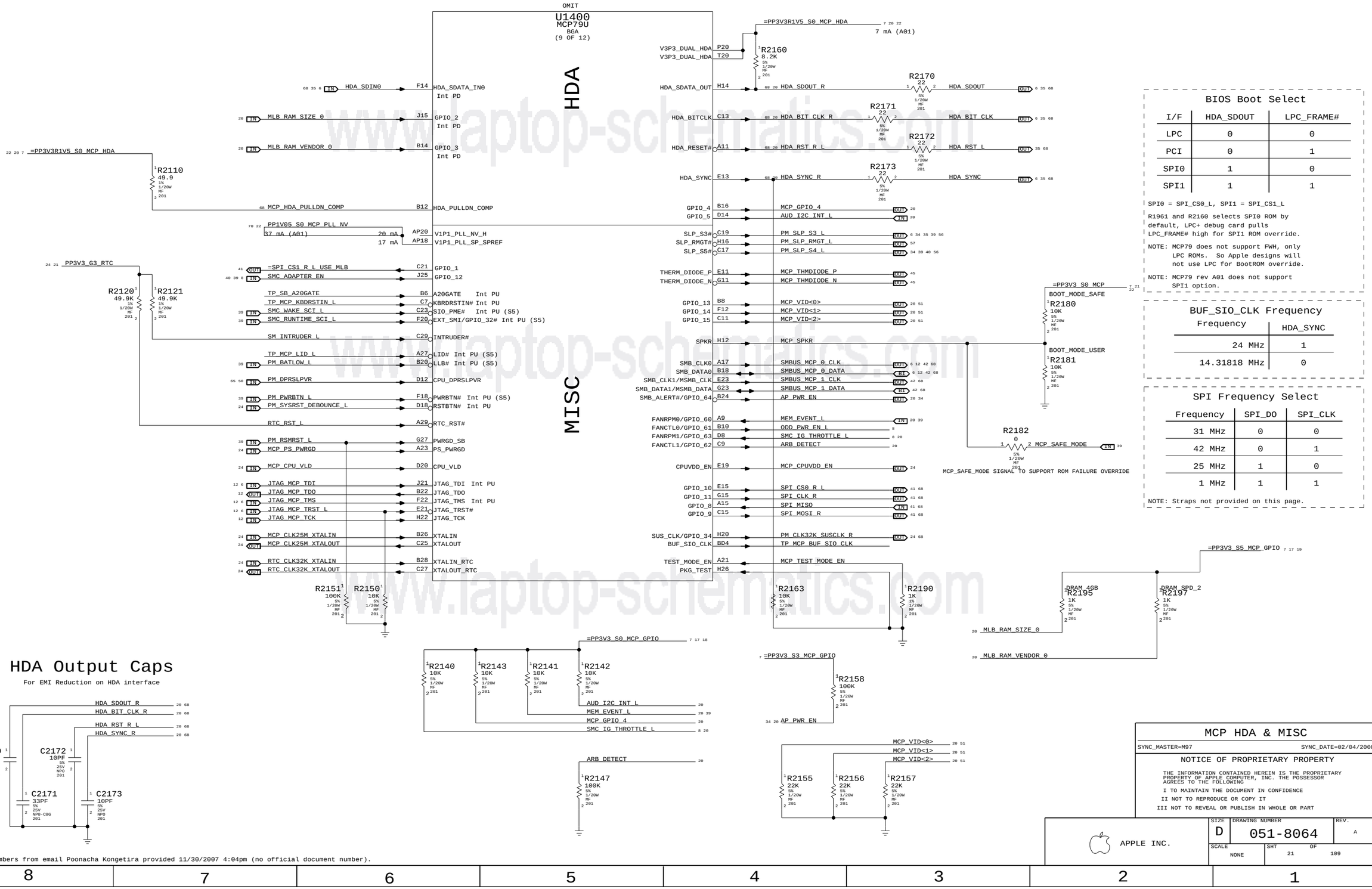
SYNC_MASTER=M97 SYNC_DATE=02/04/2008

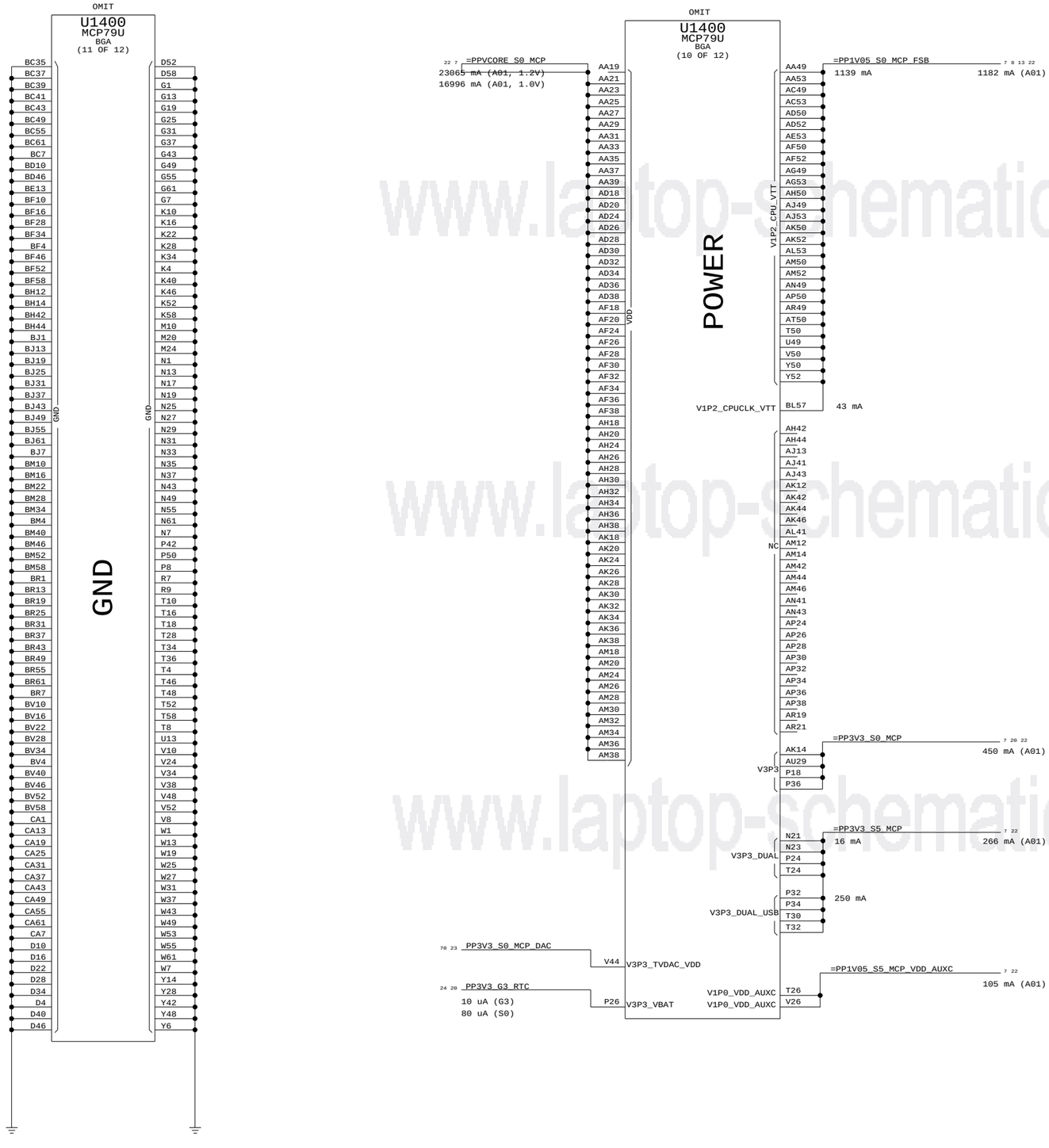
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	20	109

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).





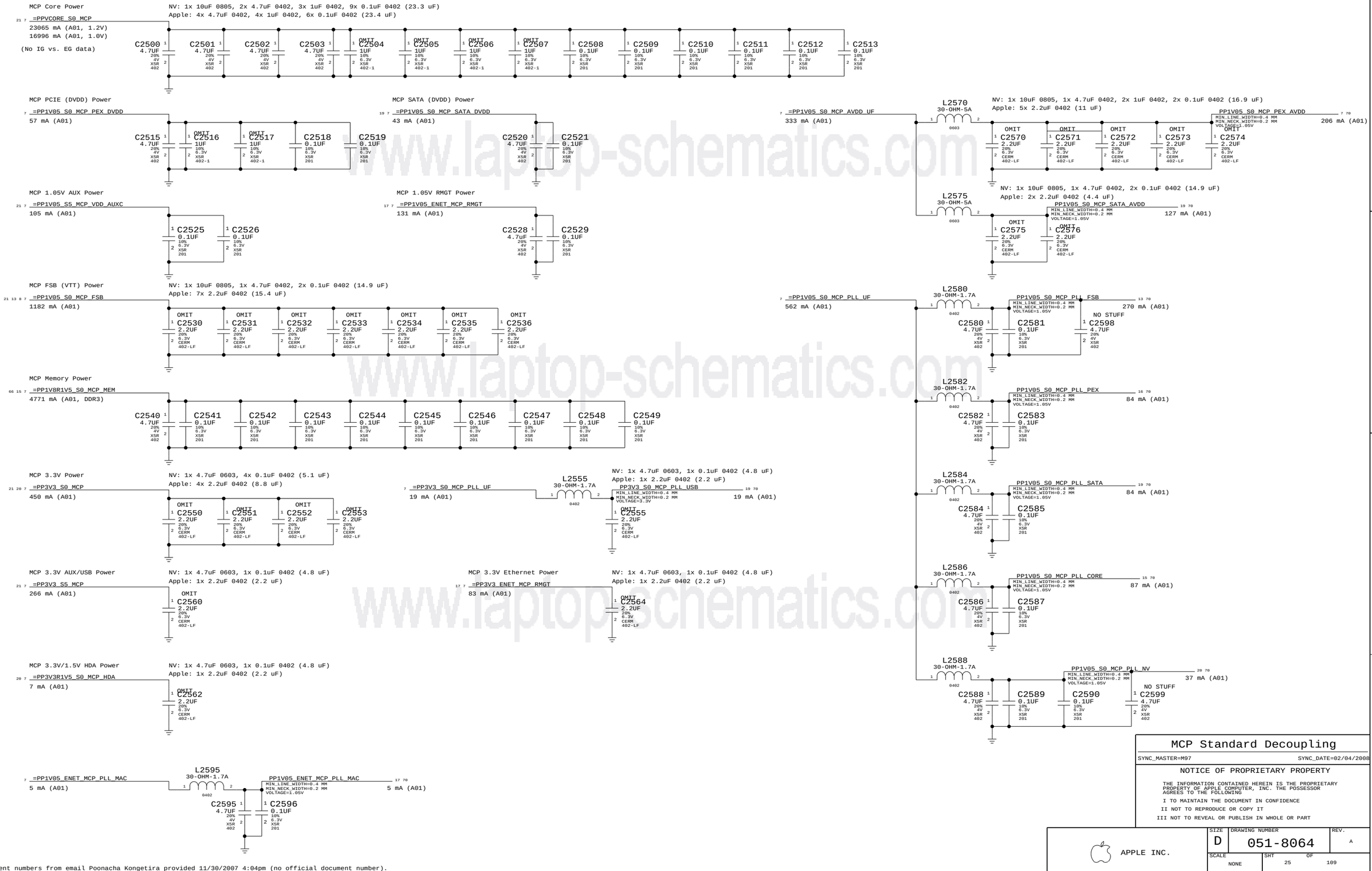
MCP Power & Ground

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 22 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

17 7 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

OMIT
C2610
2.2UF
20%
6.3V
CERM
402-LF

PP3V3_S0_MCP_DAC 21 70

R2650
0
5%
1/16W
MF-LF
402

17 7 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615
4.7UF
20%
4V
X5R
402

C2616
0.1UF
10%
6.3V
X5R
201

67 17 MCP_HDMI_RSET
67 17 MCP_HDMI_VPROBE

NO STUFF
C2620
0.1UF
10%
6.3V
X5R
201

R2620
1K
1%
1/20W
MF
201

67 17 MCP_IFPAB_RSET
67 17 MCP_IFPAB_VPROBE

NO STUFF
C2630
0.1UF
10%
6.3V
X5R
201

NO STUFF
R2630
1K
1%
1/20W
MF
201

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

7 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640
30-OHM-1.7A
0402

PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

17 70
16 mA (A01)

C2640
4.7UF
20%
6.3V
CERM
603

C2641
0.1uF
10%
6.3V
X5R
201

SYNC FROM M97

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Graphics Support

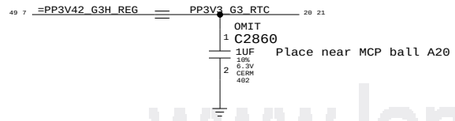
SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

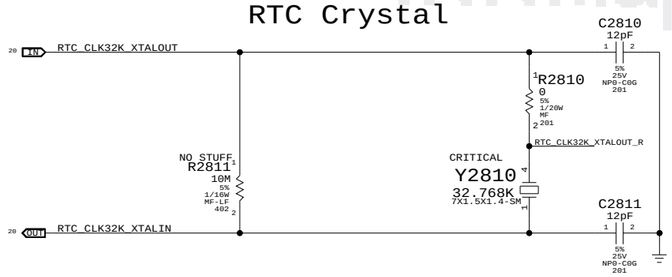
SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	26	109

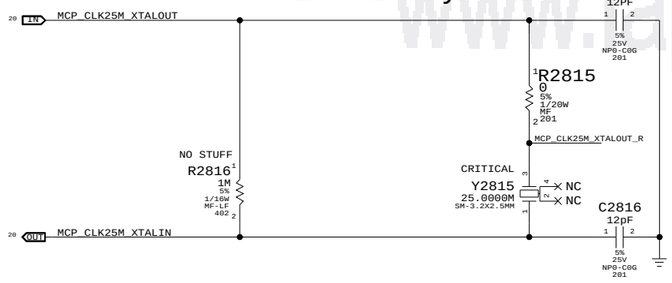
RTC Power Sources



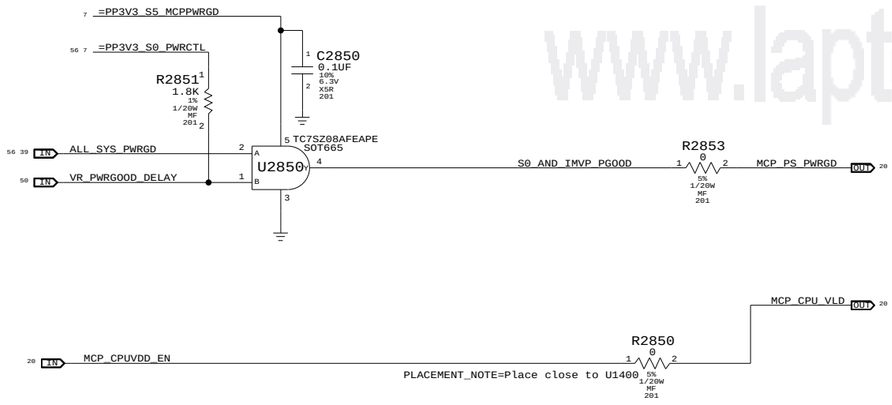
RTC Crystal



MCP 25MHz Crystal



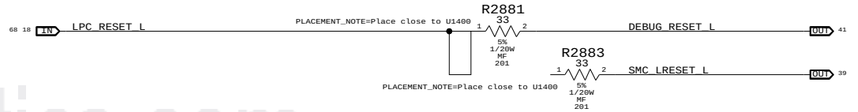
MCP S0 PWRGD & CPU_VLD



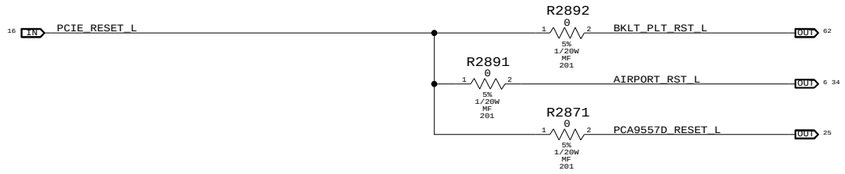
SYNC FROM M97
CHANGED RTC POWER SOURCE TO DIRECT CONNECTION
ADDED MCPSEQ_SMC LOGIC

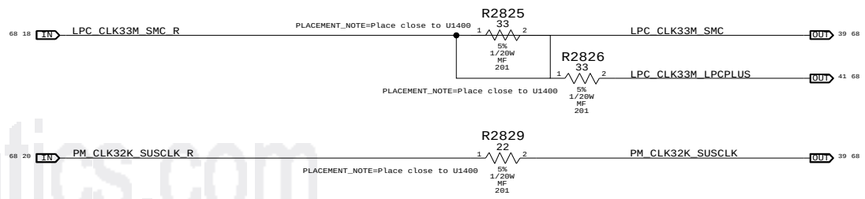
Platform Reset Connections

LPC Reset (Unbuffered)

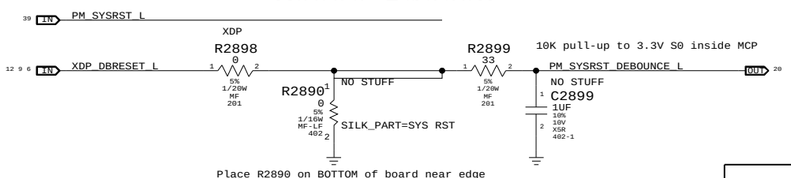


PCIE Reset (Unbuffered)





Reset Button



SB Misc		
SYNC_MASTER=M97	SYNC_DATE=02/04/2008	

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8064	A
	SCALE: NONE	SHT 28 OF 109	

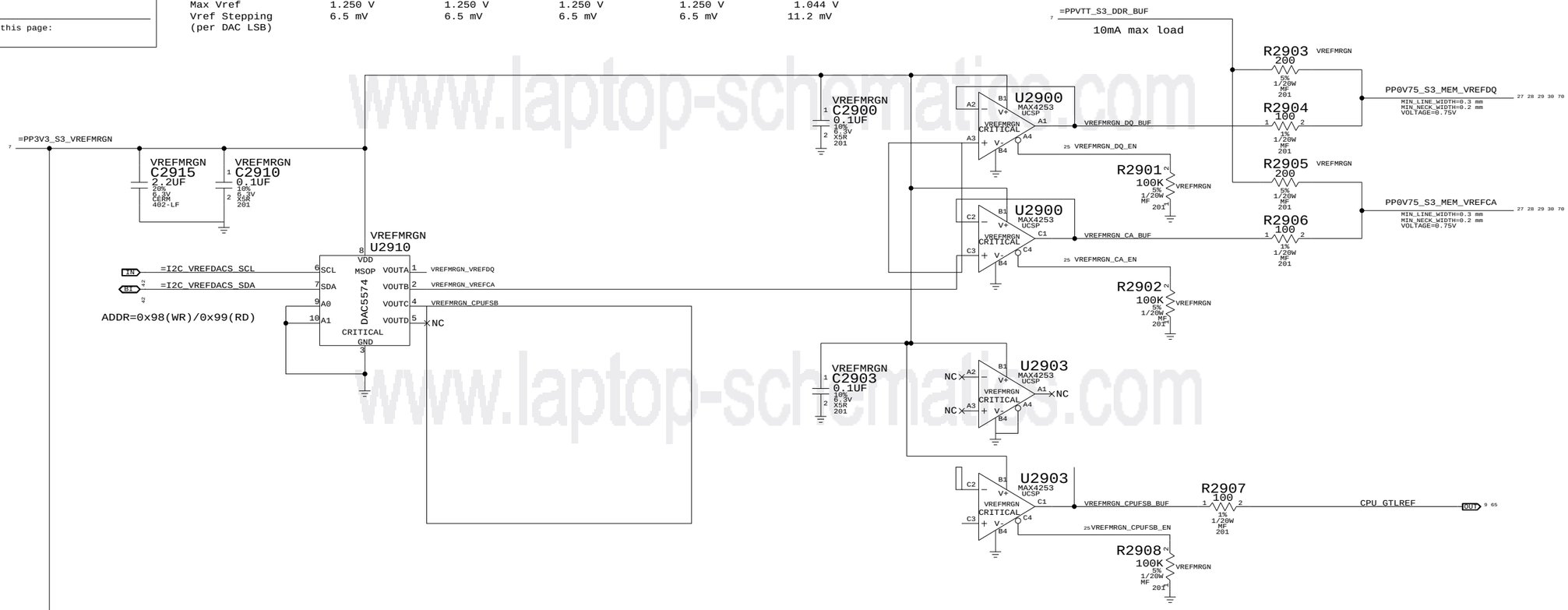
Page Notes

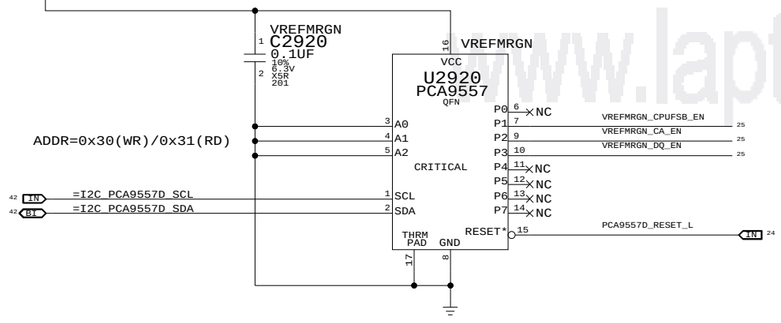
Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV





Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	1	RES,MTL FILM,0,5%,0201,SM,LF	R2903	CRITICAL	NO_VREFMRGN
117S0002	1	RES,MTL FILM,0,5%,0201,SM,LF	R2905	CRITICAL	NO_VREFMRGN

FSB/DDR3 Vref Margining

SYNC_MASTER=BEN SYNC_DATE=01/15/2008

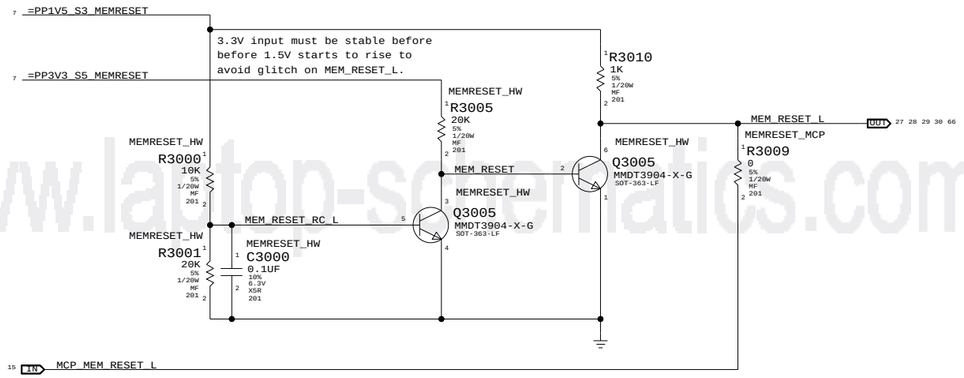
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE NONE SHT 29 OF 109

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=01/30/2008

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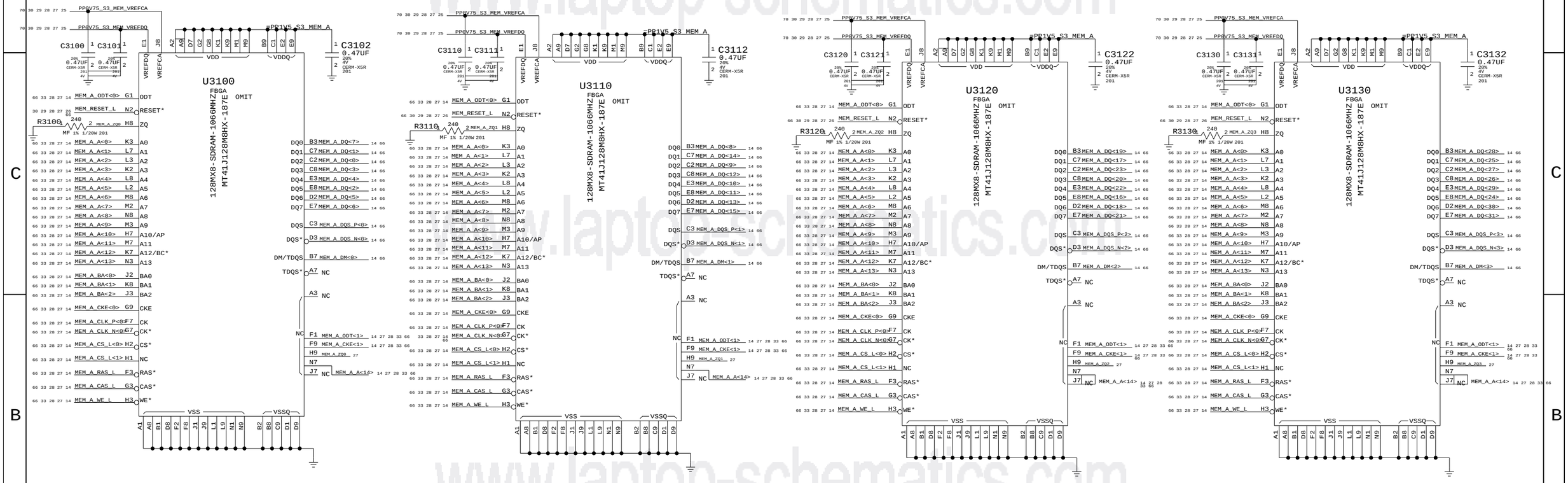
SCALE	SHT	OF
NONE	30	109



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel A (0-31)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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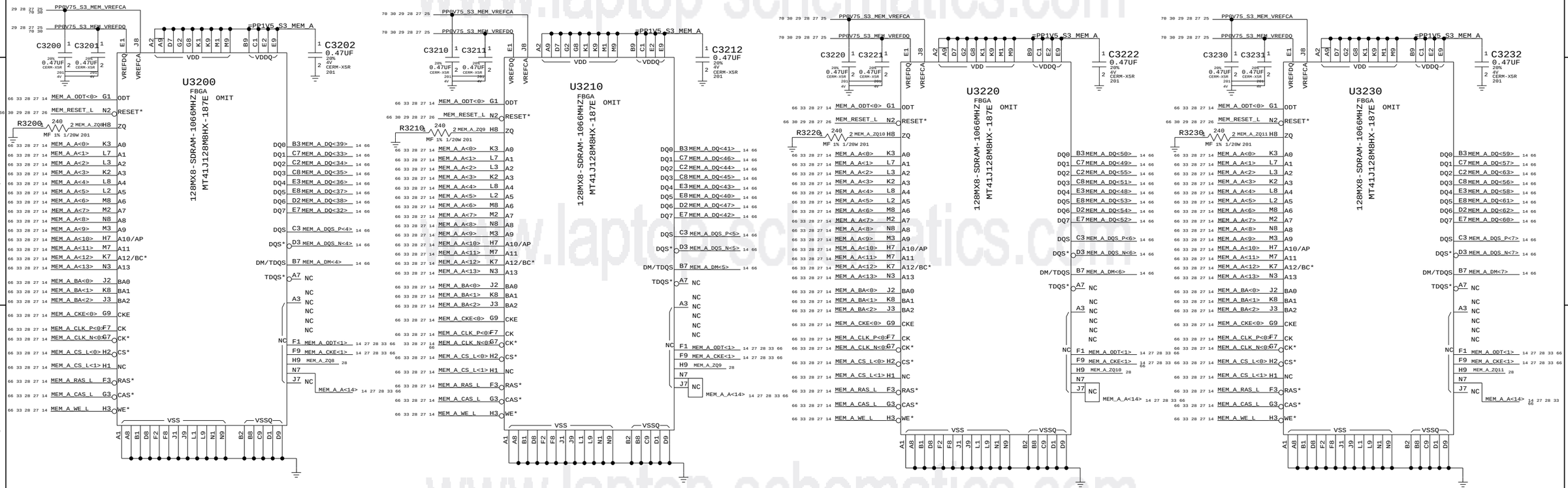
SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 31 OF 109	

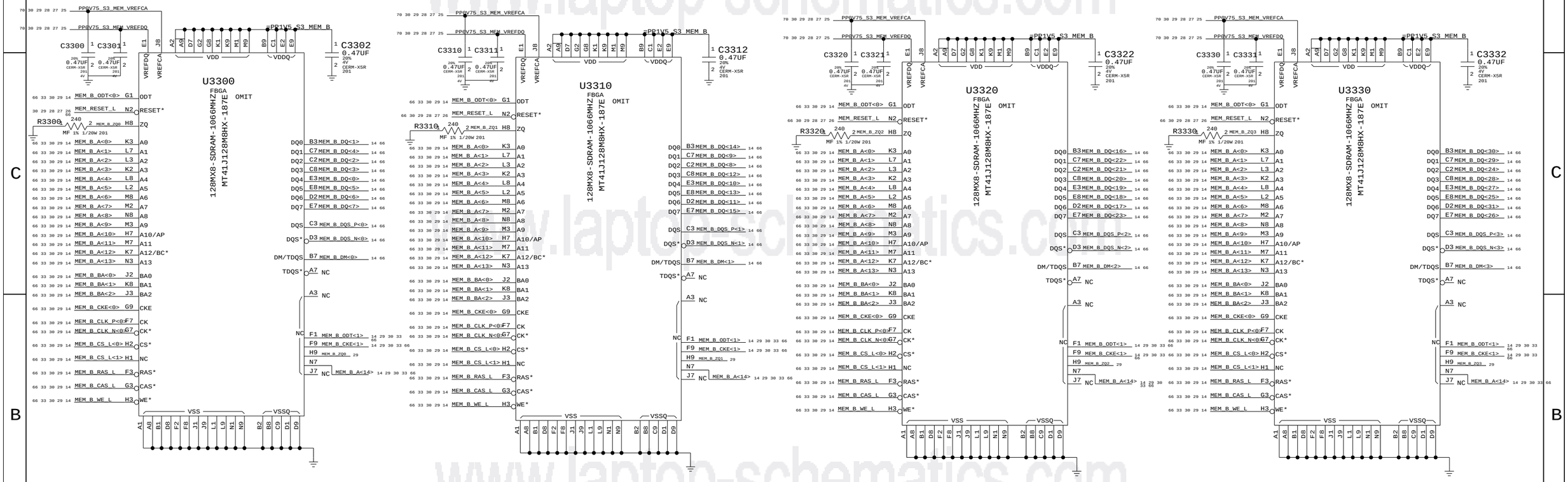


A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel A (32-63)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 32 OF 109	



DDR3 DRAM Channel B (0-31)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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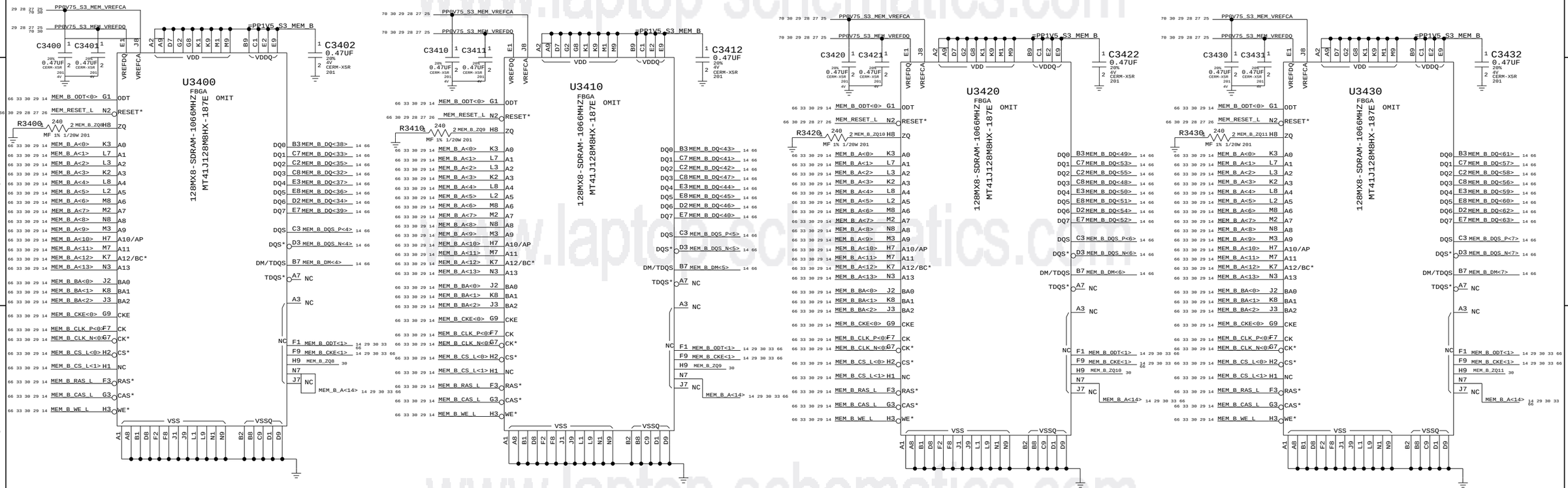
SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	33	109



A14/A15 FOR 2G/4G MONO ONLY
CS1 IS FOR 2G DDP RANK CONTROL

DDR3 DRAM Channel B (32-63)

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SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	34	109

33 31 28 27 7 =PP1V5_S3_MEM_A

OMIT C3500 2.2UF 20% 6.3V CERM 402-LF
OMIT C3501 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

OMIT C3510 2.2UF 20% 6.3V CERM 402-LF
OMIT C3511 2.2UF 20% 6.3V CERM 402-LF
OMIT C3512 2.2UF 20% 6.3V CERM 402-LF

OMIT C3520 2.2UF 20% 6.3V CERM 402-LF
OMIT C3521 2.2UF 20% 6.3V CERM 402-LF

OMIT C3504 2.2UF 20% 6.3V CERM 402-LF
OMIT C3505 2.2UF 20% 6.3V CERM 402-LF

OMIT C3514 2.2UF 20% 6.3V CERM 402-LF
OMIT C3515 2.2UF 20% 6.3V CERM 402-LF
OMIT C3516 2.2UF 20% 6.3V CERM 402-LF

OMIT C3524 2.2UF 20% 6.3V CERM 402-LF
OMIT C3525 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

33 31 28 27 7 =PP1V5_S3_MEM_A

OMIT C3530 2.2UF 20% 6.3V CERM 402-LF
OMIT C3531 2.2UF 20% 6.3V CERM 402-LF

OMIT C3540 2.2UF 20% 6.3V CERM 402-LF
OMIT C3541 2.2UF 20% 6.3V CERM 402-LF
OMIT C3542 2.2UF 20% 6.3V CERM 402-LF

OMIT C3550 2.2UF 20% 6.3V CERM 402-LF
OMIT C3551 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

OMIT C3534 2.2UF 20% 6.3V CERM 402-LF
OMIT C3535 2.2UF 20% 6.3V CERM 402-LF

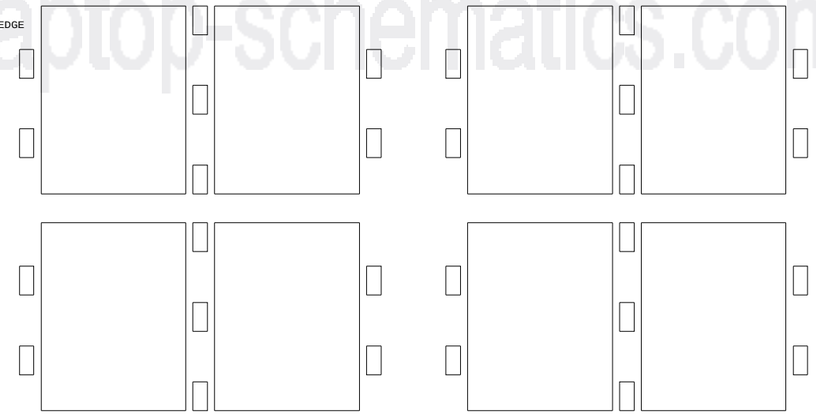
OMIT C3544 2.2UF 20% 6.3V CERM 402-LF
OMIT C3545 2.2UF 20% 6.3V CERM 402-LF
OMIT C3546 2.2UF 20% 6.3V CERM 402-LF

OMIT C3554 2.2UF 20% 6.3V CERM 402-LF
OMIT C3555 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

APPROXIMATE CAP ARRANGEMENT

TWO 0402 CAPS ALONG PACKAGE EDGE



COLUMN OF THREE 0402 CAPS BETWEEN PACKAGES

DDR BYPASSING 1

SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 35 OF 109	

33 32 30 29 7 =PP1V5_S3_MEM_B

OMIT C3600 2.2UF 20% 6.3V CERM 402-LF
OMIT C3601 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

OMIT C3610 2.2UF 20% 6.3V CERM 402-LF
OMIT C3611 2.2UF 20% 6.3V CERM 402-LF
OMIT C3612 2.2UF 20% 6.3V CERM 402-LF

OMIT C3620 2.2UF 20% 6.3V CERM 402-LF
OMIT C3621 2.2UF 20% 6.3V CERM 402-LF

OMIT C3604 2.2UF 20% 6.3V CERM 402-LF
OMIT C3605 2.2UF 20% 6.3V CERM 402-LF

OMIT C3614 2.2UF 20% 6.3V CERM 402-LF
OMIT C3615 2.2UF 20% 6.3V CERM 402-LF
OMIT C3616 2.2UF 20% 6.3V CERM 402-LF

OMIT C3624 2.2UF 20% 6.3V CERM 402-LF
OMIT C3625 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

33 32 30 29 7 =PP1V5_S3_MEM_B

OMIT C3630 2.2UF 20% 6.3V CERM 402-LF
OMIT C3631 2.2UF 20% 6.3V CERM 402-LF

OMIT C3640 2.2UF 20% 6.3V CERM 402-LF
OMIT C3641 2.2UF 20% 6.3V CERM 402-LF
OMIT C3642 2.2UF 20% 6.3V CERM 402-LF

OMIT C3650 2.2UF 20% 6.3V CERM 402-LF
OMIT C3651 2.2UF 20% 6.3V CERM 402-LF

2 CAPS ALONG PACKAGE EDGE

OMIT C3634 2.2UF 20% 6.3V CERM 402-LF
OMIT C3635 2.2UF 20% 6.3V CERM 402-LF

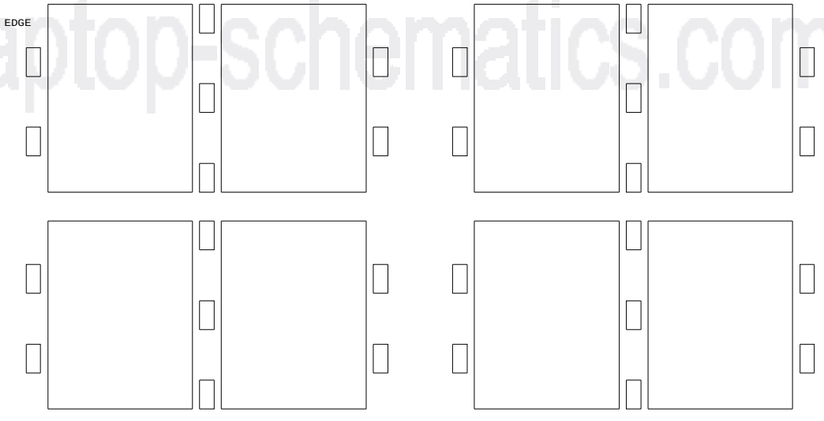
OMIT C3644 2.2UF 20% 6.3V CERM 402-LF
OMIT C3645 2.2UF 20% 6.3V CERM 402-LF
OMIT C3646 2.2UF 20% 6.3V CERM 402-LF

OMIT C3654 2.2UF 20% 6.3V CERM 402-LF
OMIT C3655 2.2UF 20% 6.3V CERM 402-LF

COLUMN OF THREE CAPS BETWEEN PACKAGES

APPROXIMATE CAP ARRANGEMENT

TWO 0402 CAPS ALONG PACKAGE EDGE



COLUMN OF THREE 0402 CAPS BETWEEN PACKAGES

DDR BYPASSING 2

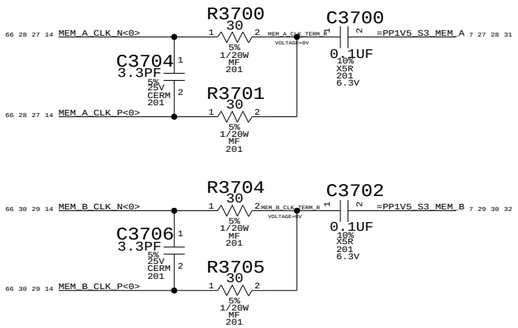
SYNC_MASTER=MEMORY SYNC_DATE=06/20/2005

APPLE INC.

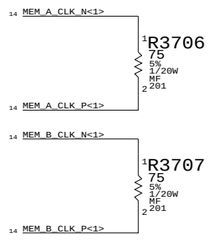
SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 36 OF 109	

MEM CLOCK TERMINATION

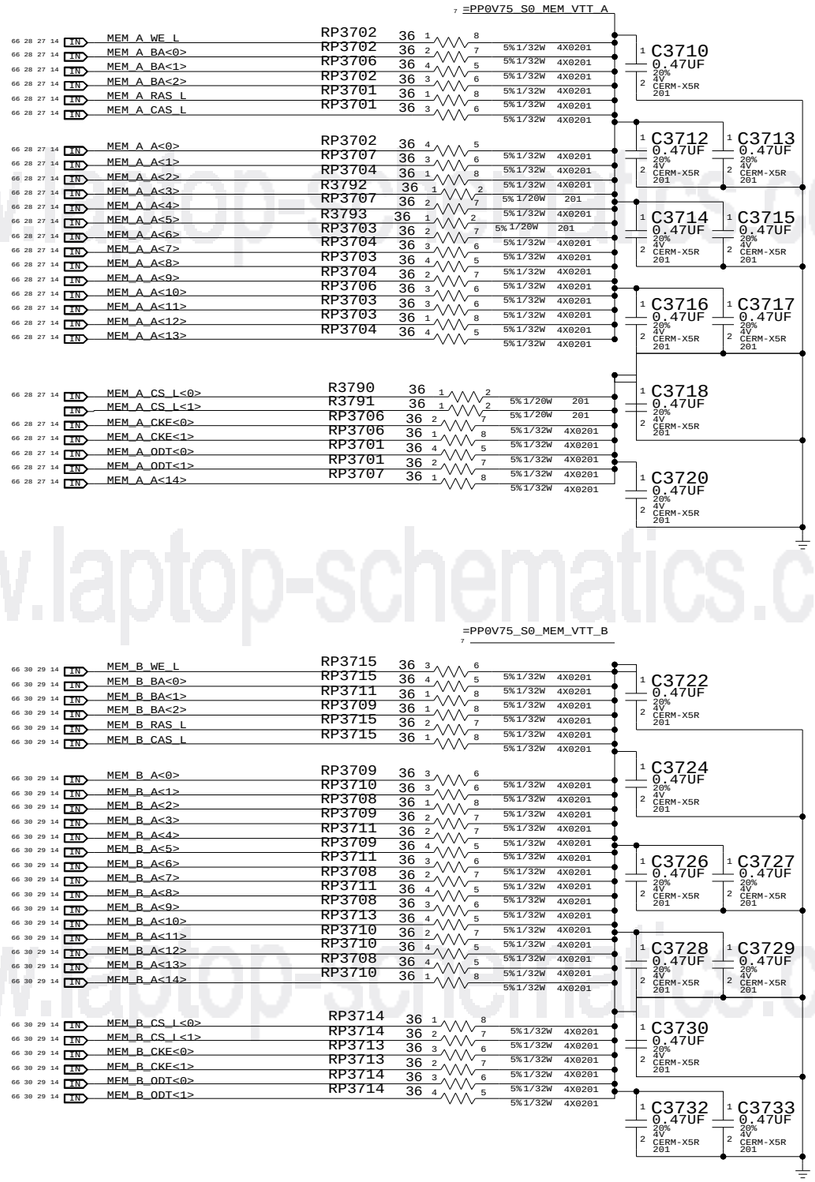
Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



Unused Clock Termination



JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

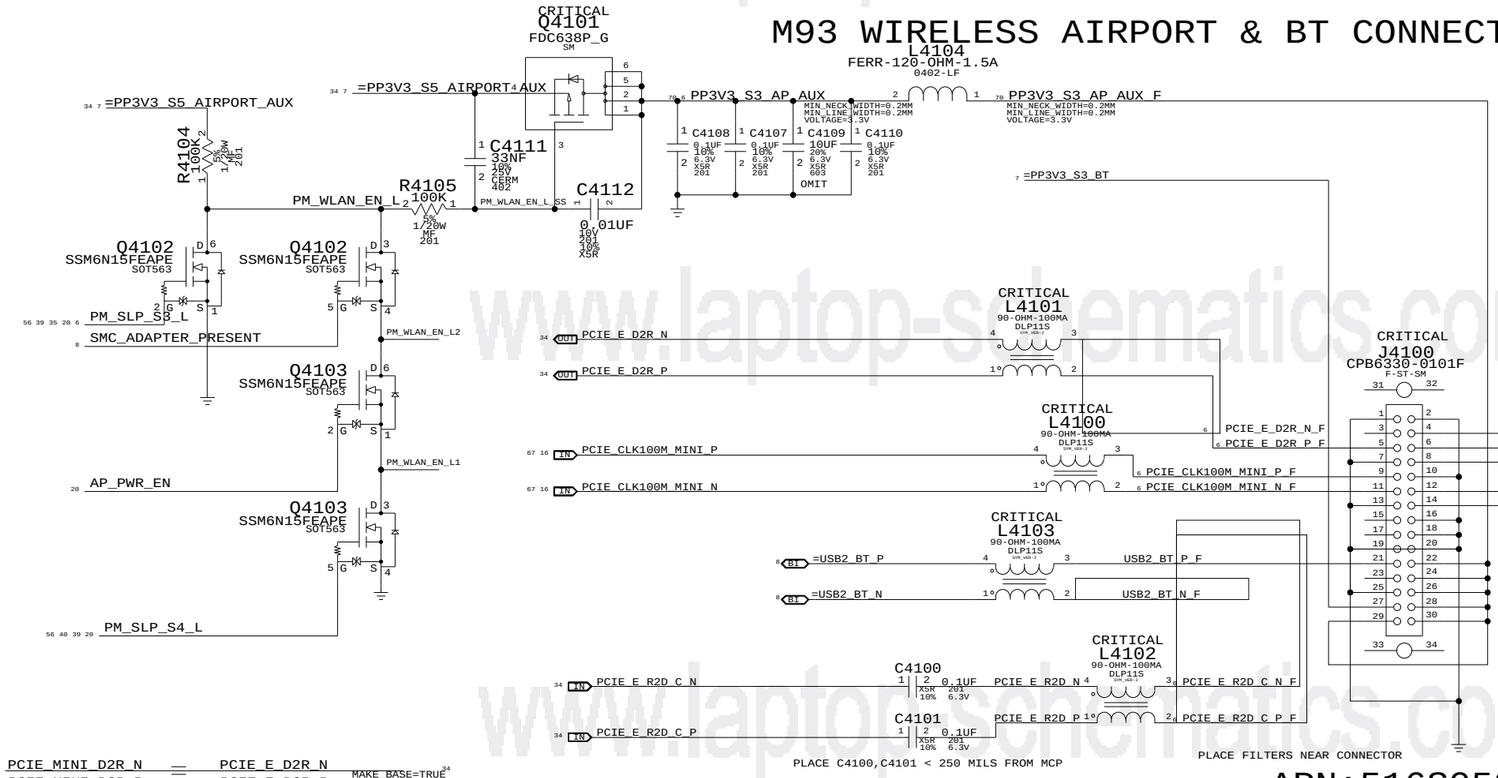


Memory Active Termination

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 37 OF 109	

M93 WIRELESS AIRPORT & BT CONNECTOR



PCIE_MINI_D2R_N — PCIE_E_D2R_N MAKE_BASE=TRUE
PCIE_MINI_D2R_P — PCIE_E_D2R_P MAKE_BASE=TRUE
PCIE_MINI_R2D_C_N — PCIE_E_R2D_C_N MAKE_BASE=TRUE
PCIE_MINI_R2D_C_P — PCIE_E_R2D_C_P MAKE_BASE=TRUE

PLACE C4100,C4101 < 250 MILS FROM MCP

PLACE FILTERS NEAR CONNECTOR

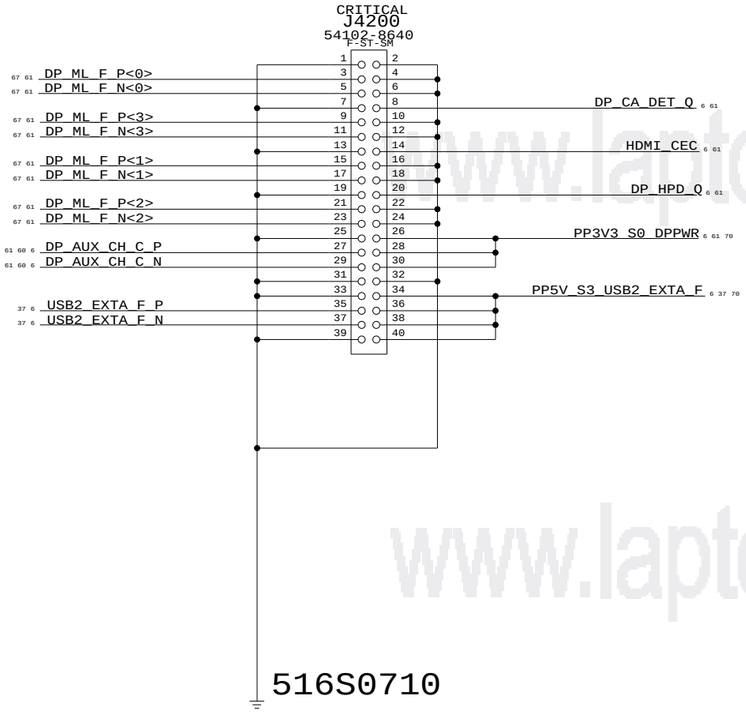
APN:516S0580

Wireless M93 Connector

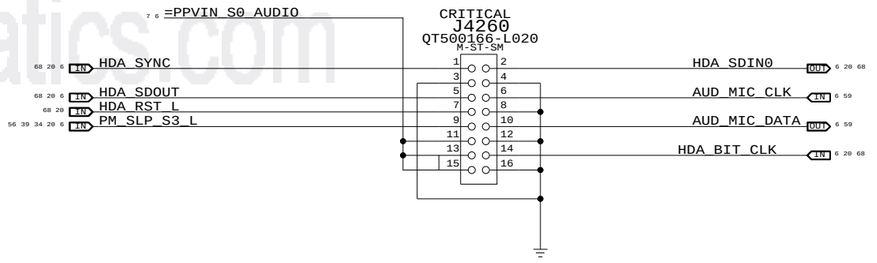
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 41 OF 109	

Micro-DisplayPort / USB to RIO Hatch Assembly



Audio Connector



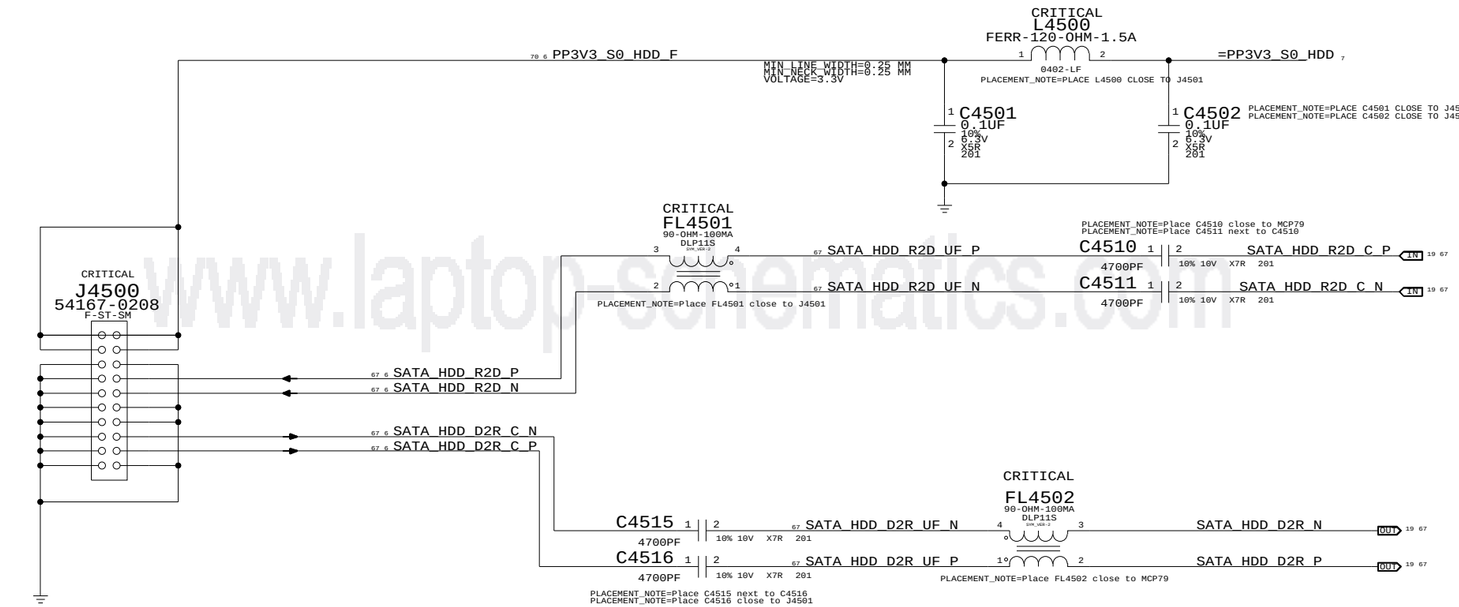
Hatch and Audio Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 42 OF 109	

SATA HDD PORT



516S0678

SATA Connectors

SYNC_MASTER=CHANGZHANG SYNC_DATE=02/05/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 45 OF 109	

USB 2.0 CONNECTOR

CONNECT TO 5V S5 or S3 PER LAYOUT

CRITICAL
C4610 100UF 20% 6.3V POLY-TANT CASE-B2-SM

CRITICAL
L4602 FERR-120-OHM-3A 0603
PP5V_S3_USB2_EXTA_F
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

ROUTE USB DATA LINES AS DIFFERENTIAL PAIRS

CRITICAL
L4600 90-OHM-100MA DLP11S

PP5V_S3_USB2_EXTA_F
USB2_EXTA_F_N
USB2_EXTA_F_P
CONNECT TO RIO CONNECTOR J4200

68 37 USB_EXTA_MUXED_N
68 37 USB_EXTA_MUXED_P

C4602 0.01UF 10% 10V X5R 201

CRITICAL
D4600 SC-75 RCLAMP0502B

LAYOUT NOTE:C4602 IS AN EMC BY-PASS CAP FOR J4200

7 =PP5V_S3_EXTUSB
OMIT
C4613 10uF 20% 6.3V X5R 603
C4612 0.1UF 10% 6.3V X5R 201

CRITICAL
U4600 TPS2052B MSOP
IN OUT1 OUT2 OC1* EN1 OC2* EN2 GND TPAD

70 PP5V_S3_USB2_EXTA
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

56 =USBPWR_EN

DUAL SWITCH HAS GANGED OUTPUT
BOTH SWITCHES WILL TRIP TOGETHER AT 1.5A-2.2A

EXTAUSB_OC_F_L
R4650 1K 5% 1/16W MF-LF 402
=EXTAUSB_OC_L 8
C4650 0.47UF 10% 6.3V CERM-X5R 402

USB/SMC MUX

7 =PP3V42_G3H_SMCUSBMUX

R4675 100 5% 1/20W MF 201
70 PP3V42_G3H_SMCUSBMUX_R
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V

C4675 0.1UF 10% 6.3V X5R 201
PLACE C4675 NEAR U4675

R4677 10K 5% 1/20W MF 201

USB_EXTA_MUXED_P 37 68
USB_EXTA_MUXED_N 37 68

VCC
41 40 39 SMC_RX_L
41 40 39 SMC_TX_L
8 =USB2_EXTA_P
8 =USB2_EXTA_N

CRITICAL
U4675 PI3USB102ZLE TQFN
M+ M- D+ D- OE* Y+ Y- SEL GND

39 USB_DEBUGPRT_EN_L
SEL=0 CHOOSE SMC
SEL=1 CHOOSE USB

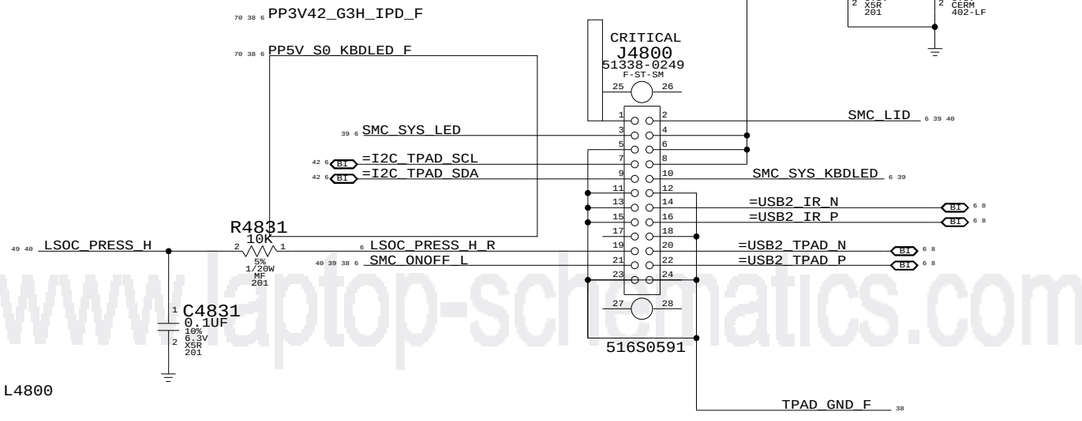
NOSTUFF
R4678 0 5% 1/20W MF 201
PLACE NEAR U4675

NOSTUFF
R4679 0 5% 1/20W MF 201

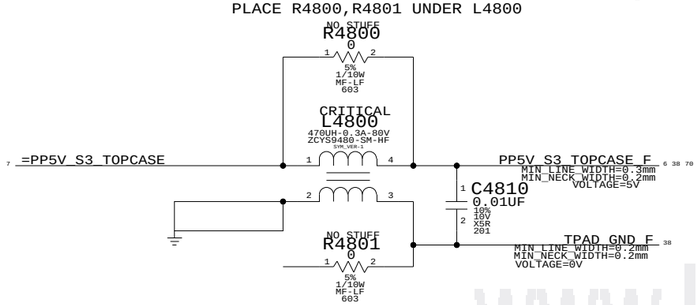
USB EXTERNAL CONNECTORS	
SYNC_MASTER=M70	SYNC_DATE=01/09/2007

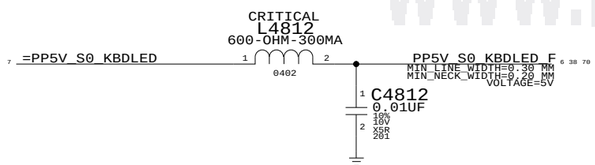
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8064	A
	SCALE NONE	SHT 46 OF 109	

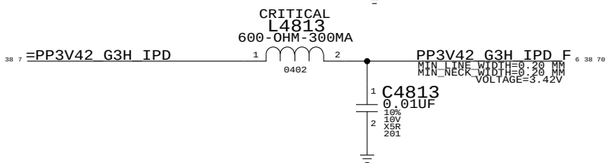
IPD Connector



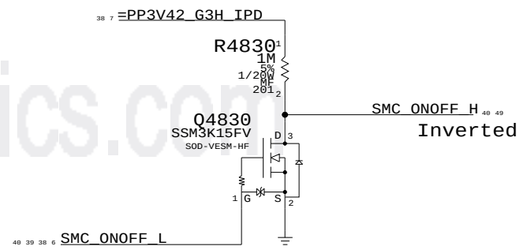
PLACE R4800,R4801 UNDER L4800







Power Button Inverter



Inverted to drive SMC_RESET logic

IPD Connector

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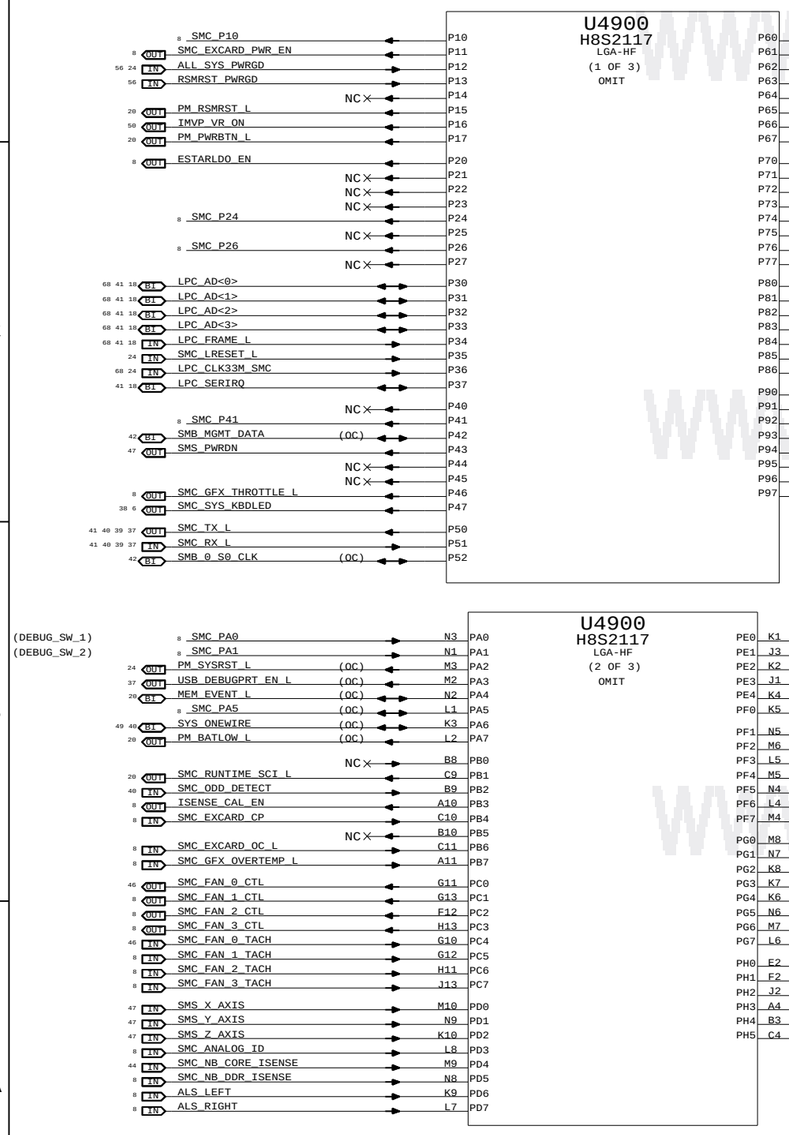
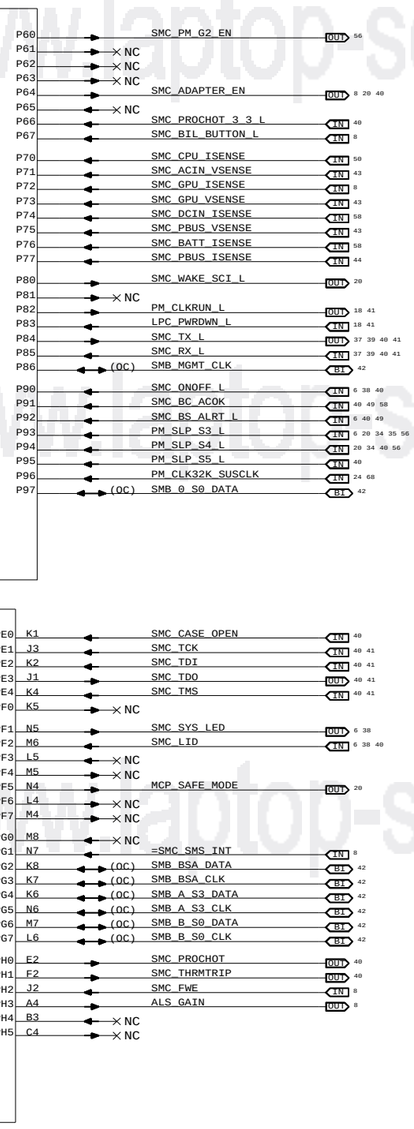
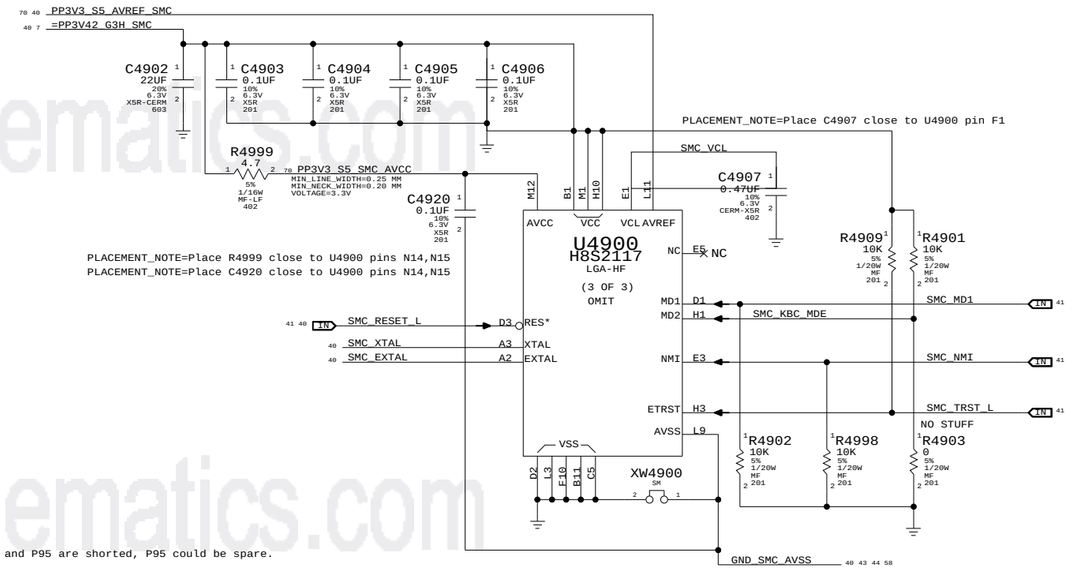
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 48 OF 109	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.







NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SMC

SYNC_MASTER=M97 SYNC_DATE=02/21/2008

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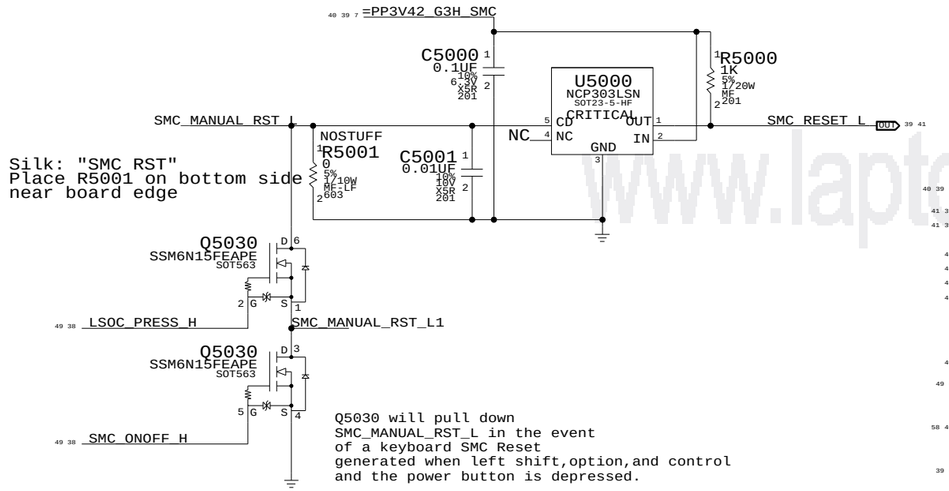
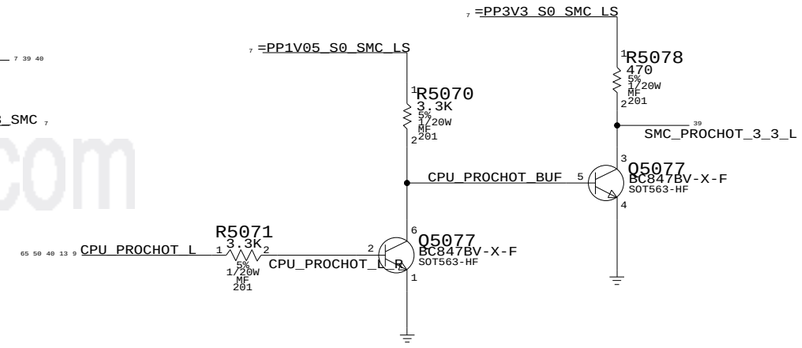
APPLE INC.

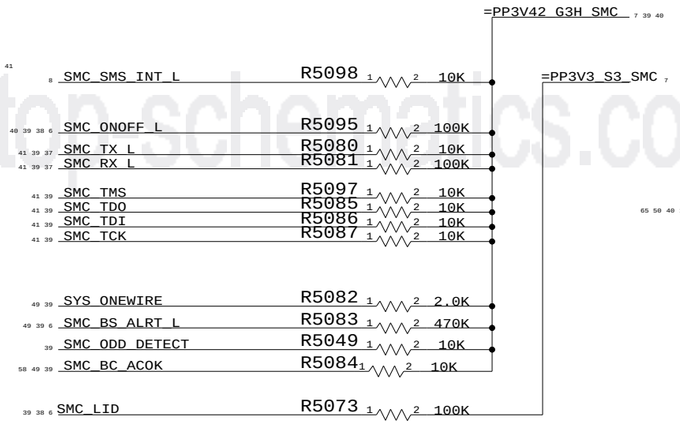
SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 49 OF 109	

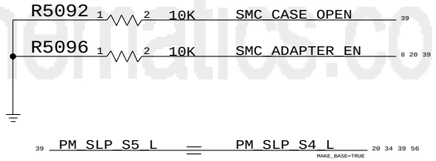
SMC Reset Button / Brownout Detect



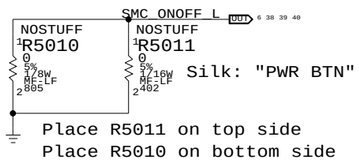
SMC 1.05V to 3.3V Level Shifting



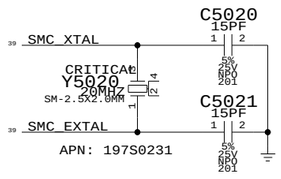




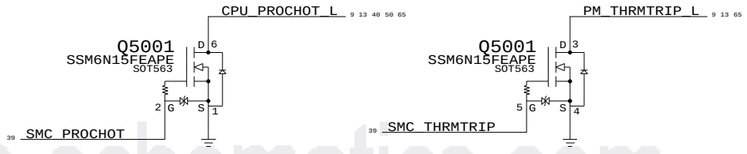
Debug Power Button



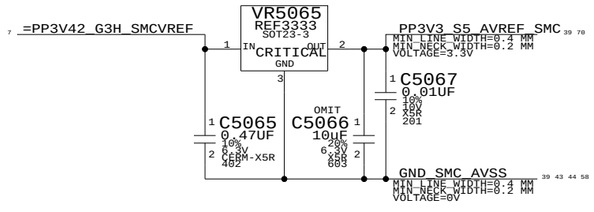
SMC Crystal Circuit



SMC 3.3V to 1.05V Level Shifting



SMC AVREF Supply



SMC SUPPORT

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

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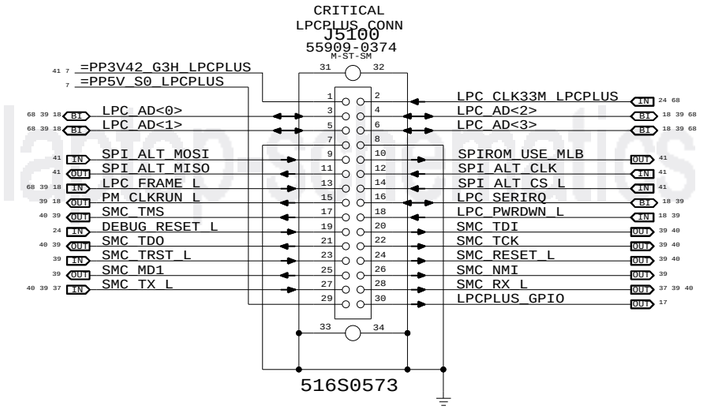
APPLE INC.

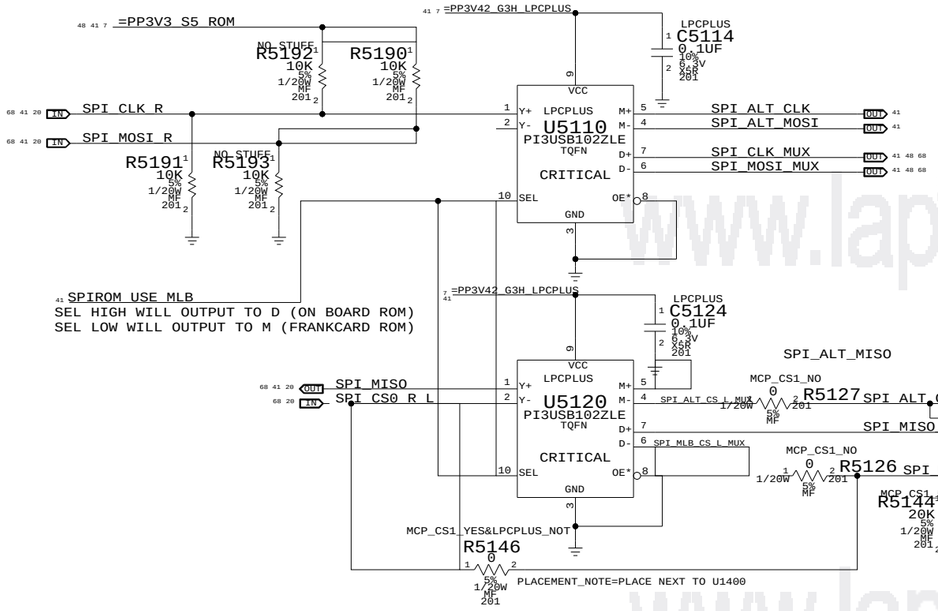
SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 50 OF 109	

LPC+SPI Connector

MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

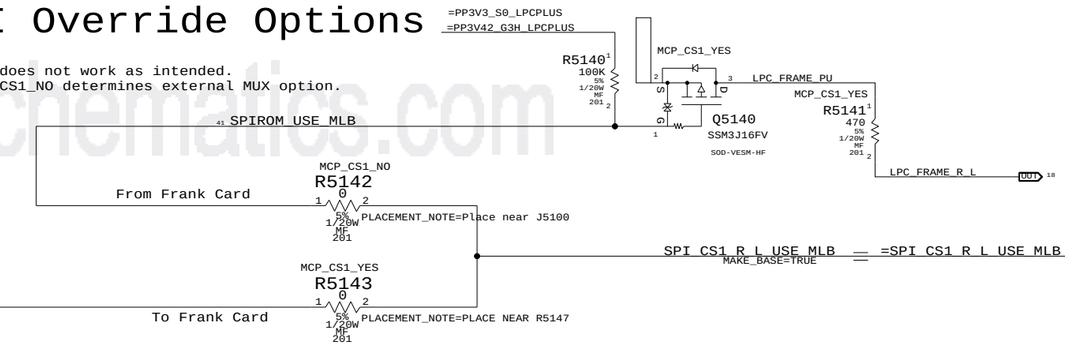
25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected w/ R5190,R5191,R5192,R5193





MCP SPI Override Options

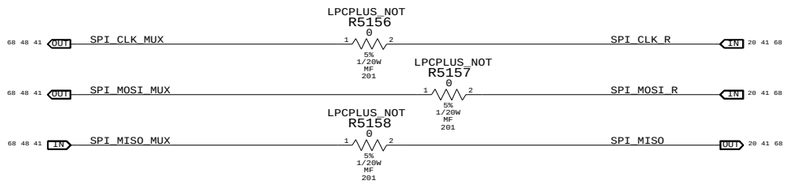
Internal MUX in rev B01 does not work as intended.
Now MCP_CS1_YES and MCP_CS1_NO determines external MUX option.



MCP79 Internal SPI MUX Support

Not supported in Rev A01 MCP79 silicon

SPI MUX BYPASS



LPC+SPI Debug Connector

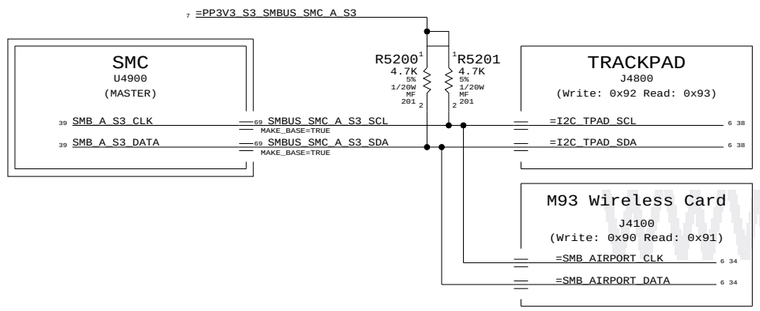
SYNC_MASTER=CHANGZHANG SYNC_DATE=01/24/2008

APPLE INC.

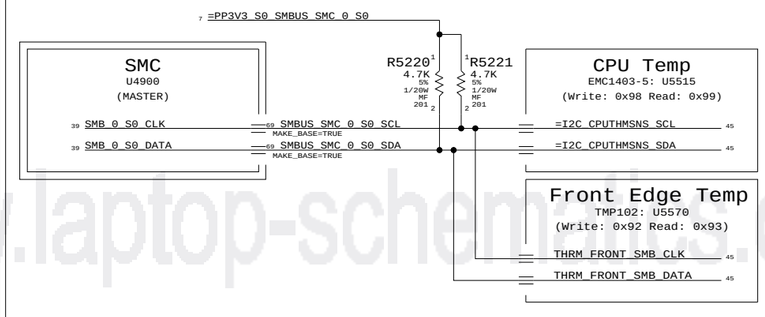
SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 51 OF 109	

SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

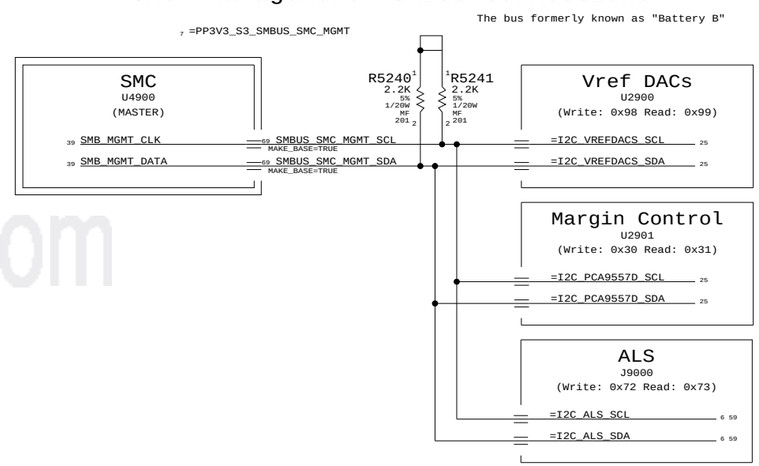


SMC "0" SMBus Connections

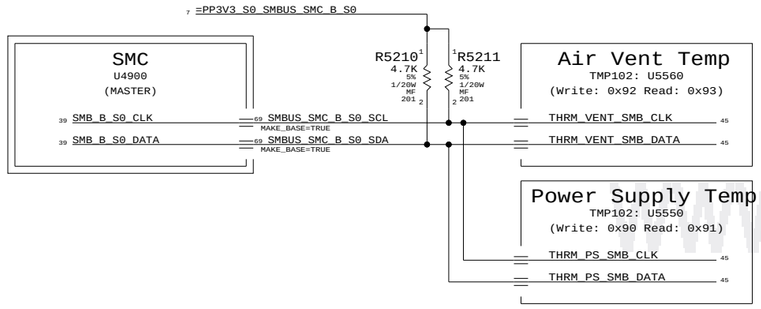


SMC "Management" SMBus Connections

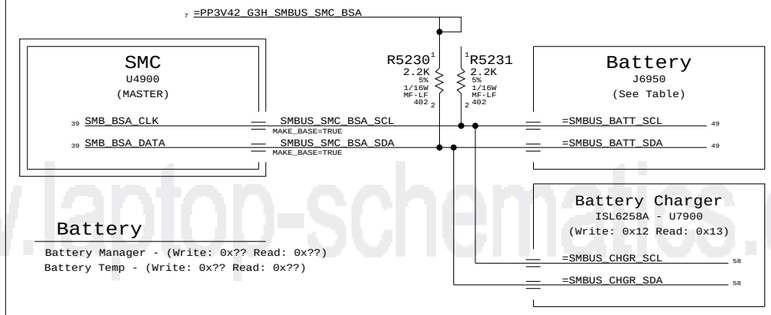
The bus formerly known as "Battery B"



SMC "B" SMBus Connections



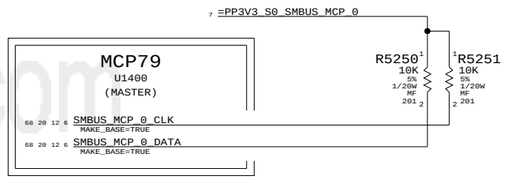
SMC "Battery A" SMBus Connections



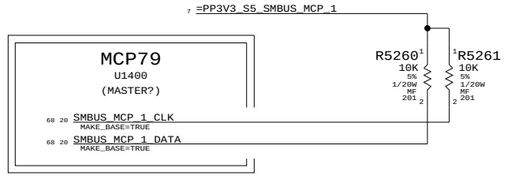
Battery

Battery Manager - (Write: 0x?? Read: 0x??)
Battery Temp - (Write: 0x?? Read: 0x??)

MCP79 SMBUS "0" CONNECTIONS



MCP79 SMBUS "1" CONNECTIONS



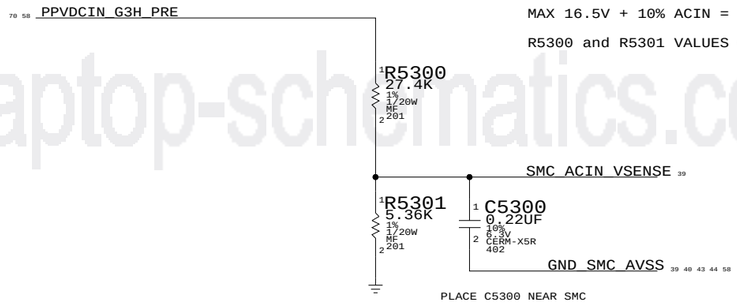
M97 SMBUS CONNECTIONS

SYNC_MASTER=BEN SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 52 OF 109	

ACIN VOLTAGE SENSE



MAX 16.5V + 10% ACIN = 3.0V SMC_ACIN_VSENSE

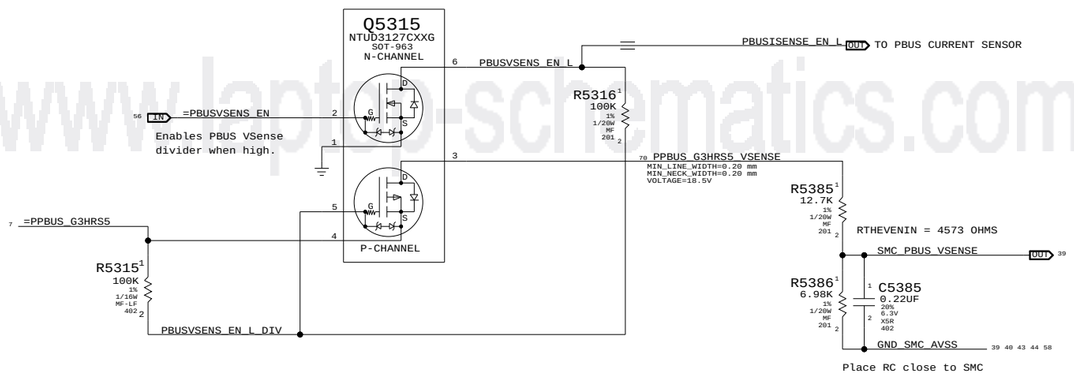
R5300 and R5301 VALUES CHOSEN FOR RC FILTER @ 4.53KOHM THEVENIN RESISTANCE

PLACE C5300 NEAR SMC

MCP VOLTAGE SENSE

PLACE R5310.C5310 NEAR SMC

PBUS VOLTAGE SENSE



Place RC close to SMC

Voltage Sensors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

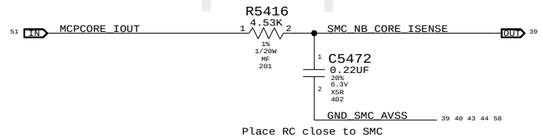
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	53	109

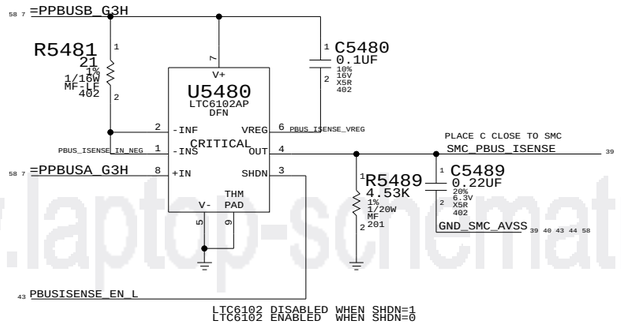
MCP VCore Current Sense

MCP VCore Current Sense Filter



Place RC close to SMC

PBUS Current Sense



LTC6102 DISABLED WHEN SHDN=1
LTC6102 ENABLED WHEN SHDN=0

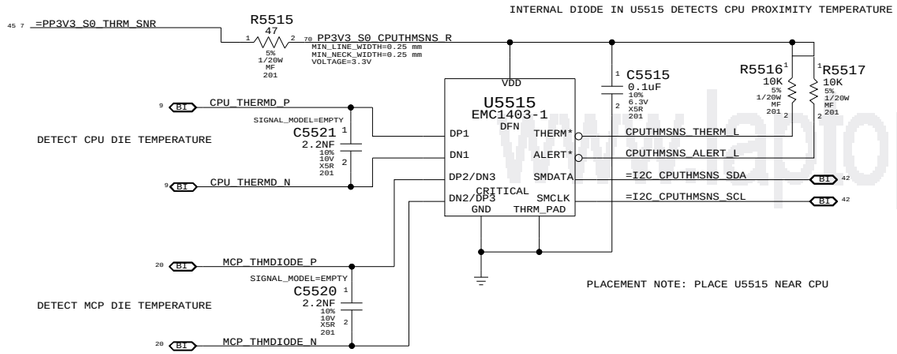
Current Sensing

SYNC_MASTER=YUNWU SYNC_DATE=02/04/2008

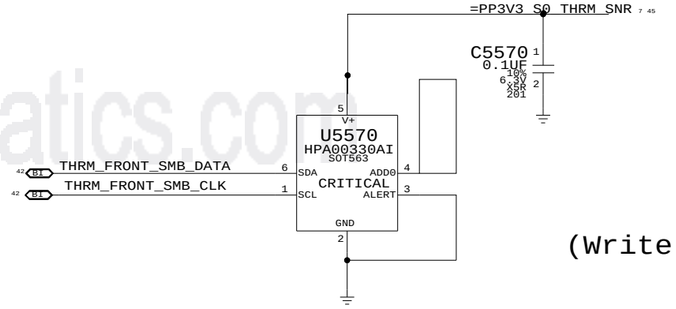
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 54 OF 109	

CPU/MCP T-Diode Thermal Sensor

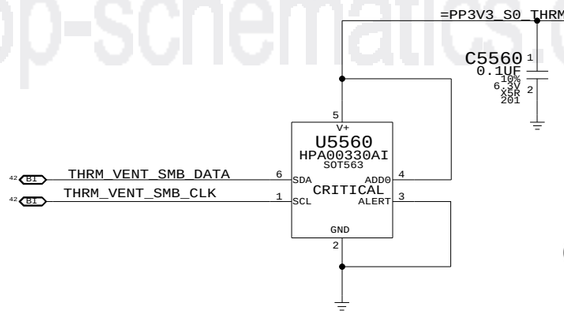


LOCAL TEMP NEAR FRONT EDGE



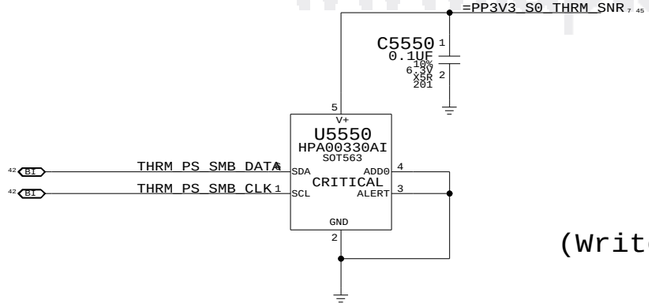
(Write: 0x92 Read: 0x93)

LOCAL TEMP NEAR AIR VENT



(Write: 0x92 Read: 0x93)

LOCAL TEMP NEAR POWER SUPPLIES



(Write: 0x90 Read: 0x91)

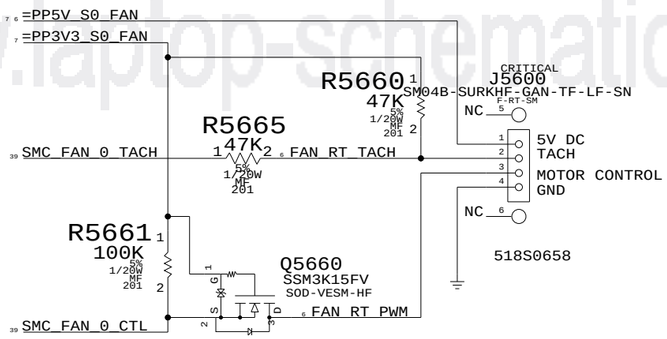
TEMPERATURE SENSORS

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 55 OF 109	

FAN CONNECTOR



Fan

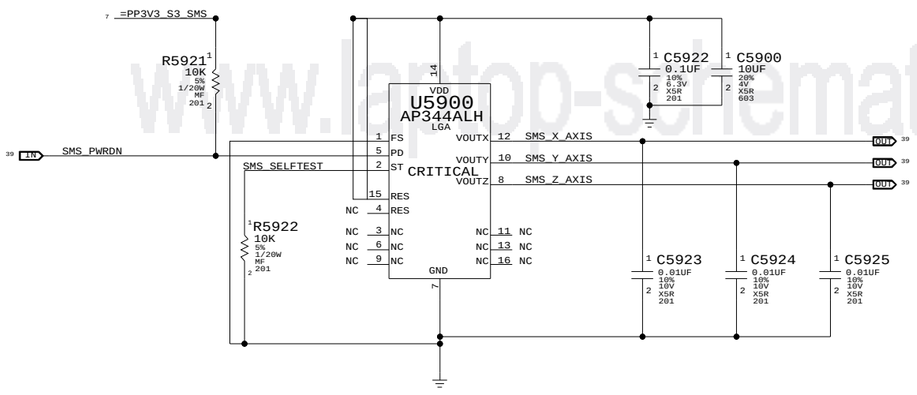
SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

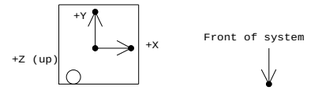
SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	56	109

SUDDEN MOTION SENSOR



Desired orientation when placed on board top-side:



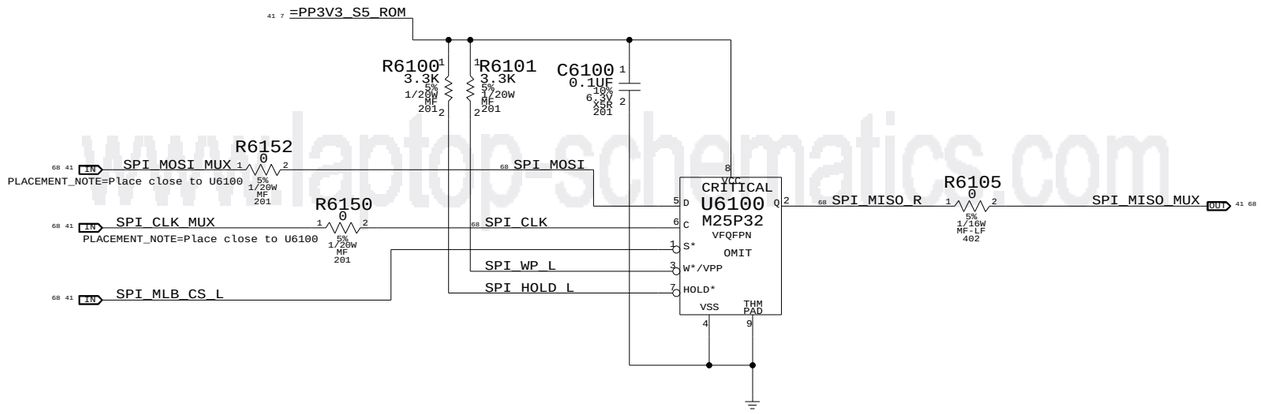
Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

SYNC_MASTER=M76_MLB SYNC_DATE=01/12/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 59 OF 109	



SPI ROM

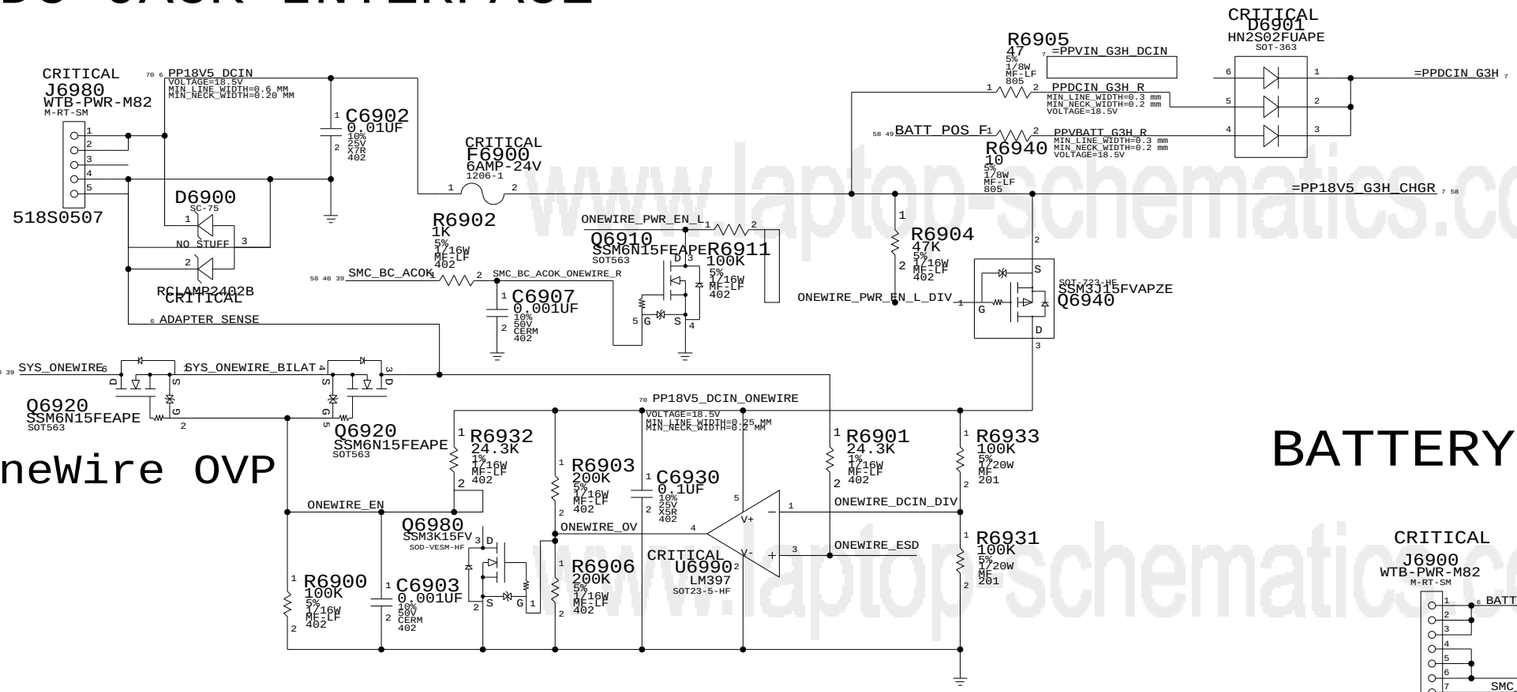
SYNC_MASTER=CHANGZHANG SYNC_DATE=02/15/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

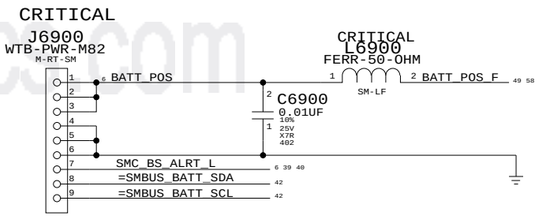
SCALE	SHT	OF
NONE	61	109

DC-JACK INTERFACE



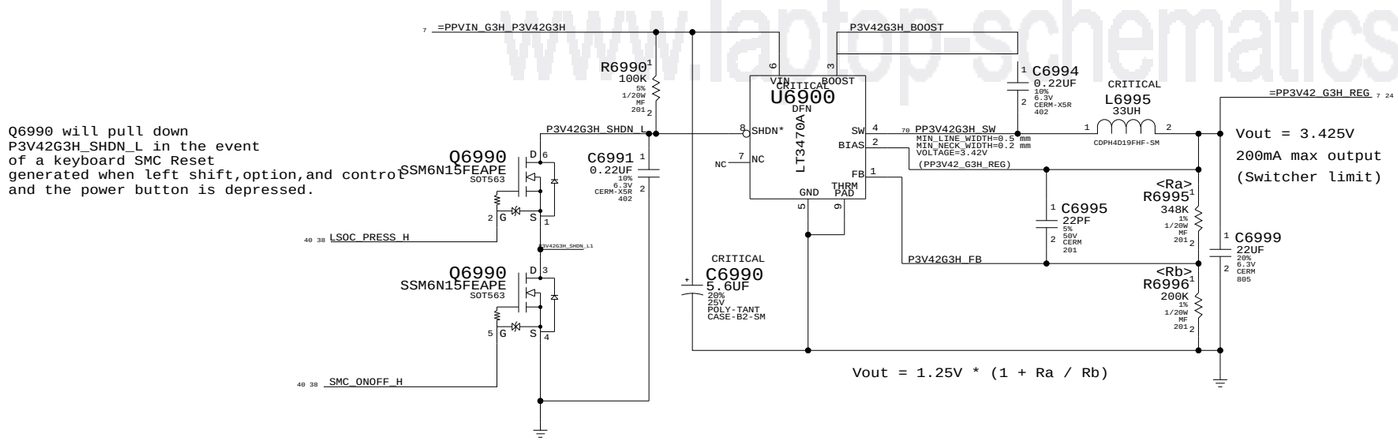
OneWire OVP

BATTERY INTERFACE



3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



Q6990 will pull down P3V42G3H_SHDN_L in the event of a keyboard SMC Reset generated when left shift,option,and control and the power button is depressed.

Vout = 3.425V
200mA max output
(Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

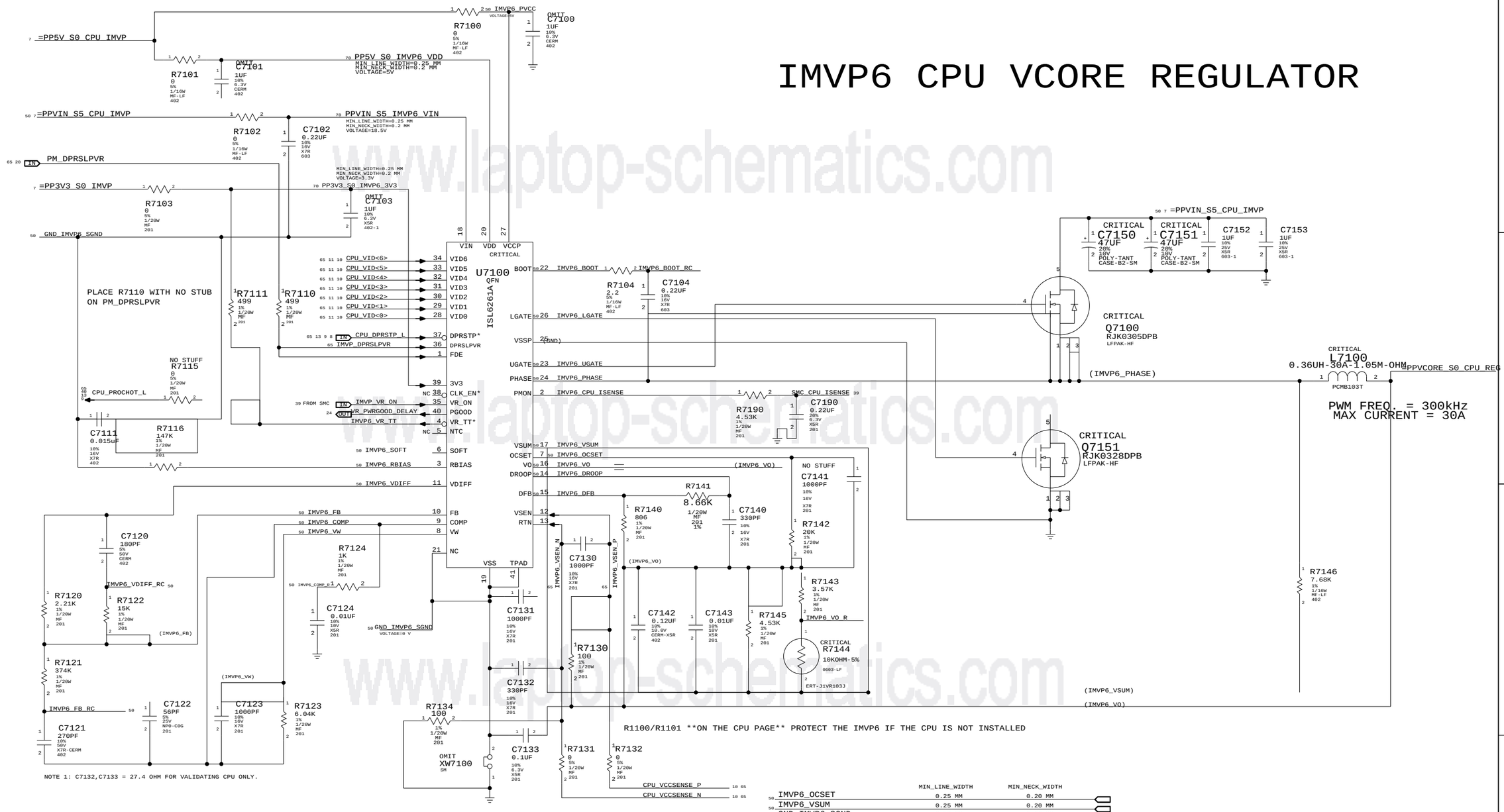
DC-In & Battery Connectors

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 69 OF 109	

IMVP6 CPU VCORE REGULATOR



NOTE 1: C7132,C7133 = 27.4 OHM FOR VALIDATING CPU ONLY.

R1100/R1101 **ON THE CPU PAGE** PROTECT THE IMVP6 IF THE CPU IS NOT INSTALLED

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_PHASE	1.5 MM	0.20 MM
IMVP6_BOOT	0.25 MM	0.20 MM
IMVP6_UGATE	1.5 MM	0.20 MM
IMVP6_LGATE	1.5 MM	0.20 MM

	MIN_LINE_WIDTH	MIN_NECK_WIDTH
IMVP6_OCSET	0.25 MM	0.20 MM
IMVP6_VSUM	0.25 MM	0.20 MM
GND_IMVP6_SGND	0.50 MM	0.20 MM
IMVP6_VO	0.25 MM	0.20 MM
IMVP6_DROOP	0.25 MM	0.20 MM
IMVP6_DFB	0.25 MM	0.20 MM
IMVP6_SOFT	0.25 MM	0.20 MM
IMVP6_RBIAS	0.25 MM	0.20 MM
IMVP6_VDIFF	0.25 MM	0.20 MM
IMVP6_FB	0.25 MM	0.20 MM
IMVP6_COMP	0.25 MM	0.20 MM
IMVP6_VW	0.25 MM	0.20 MM
IMVP6_PVCC	0.25 MM	0.20 MM
IMVP6_COMP_R	0.25 MM	0.20 MM
IMVP6_FB_RC	0.25 MM	0.20 MM
IMVP6_VDIFF_RC	0.25 MM	0.20 MM

IMVP6 CPU VCore Regulator

SYNC_MASTER=POWER SYNC_DATE=07/13/2005

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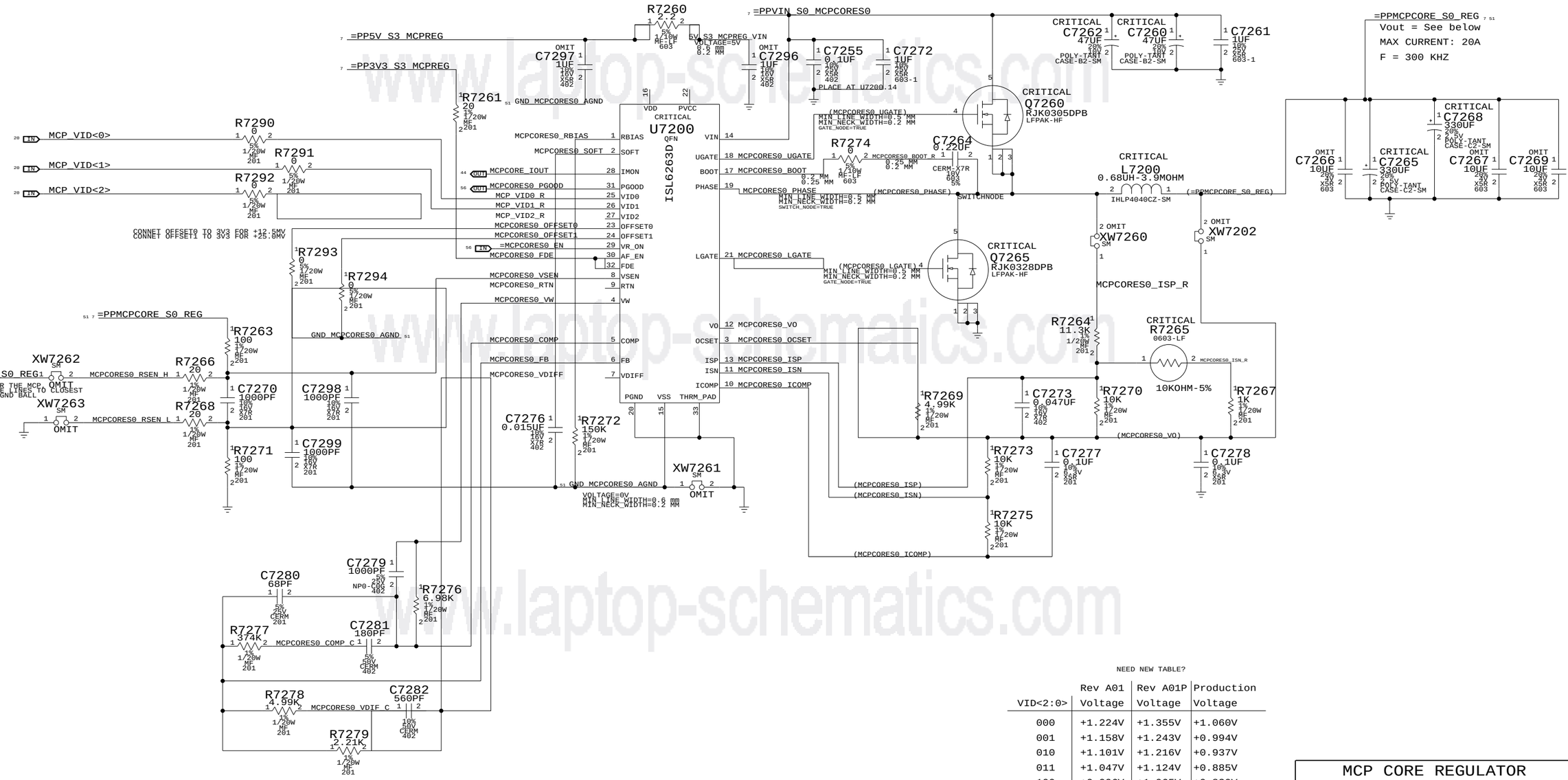
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 71 OF 109	

MCP CORE POWER SUPPLY



NEED NEW TABLE?

VID<2:0>	Rev A01 Voltage	Rev A01P Voltage	Production Voltage
000	+1.224V	+1.355V	+1.060V
001	+1.158V	+1.243V	+0.994V
010	+1.101V	+1.216V	+0.937V
011	+1.047V	+1.124V	+0.885V
100	+0.996V	+1.065V	+0.830V
101	+0.952V	+0.994V	+0.789V
110	+0.913V	+0.977V	+0.752V
111	+0.876V	+0.917V	+0.719V

(Also A01Q)

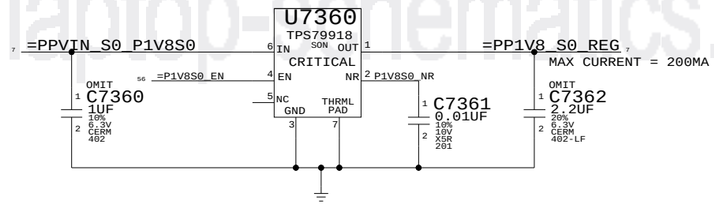
MCP CORE REGULATOR

SYNC_MASTER=MINGJING SYNC_DATE=06/24/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 72 OF 109	

1.8V S0 LDO



1.8V LDO Supply

SYNC_MASTER= SYNC_DATE=

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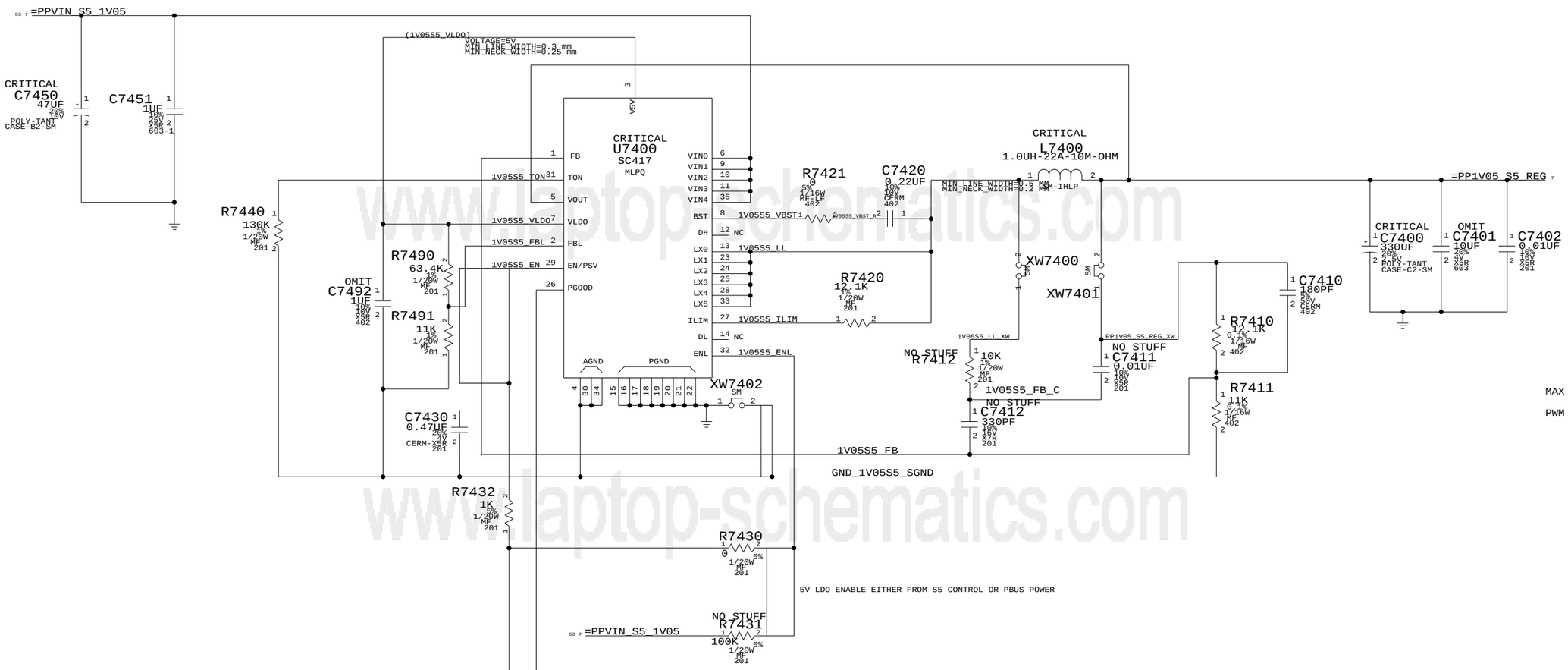
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 73 OF 109	

1V05 S5 POWER SUPPLY

supply for MCP1V05 AUX, FSB (CPU & MCP) VTT, 1V05 S0



1V05 S5 Power Supply			
SYNC_MASTER=RXU_K20	SYNC_DATE=05/21/2008		
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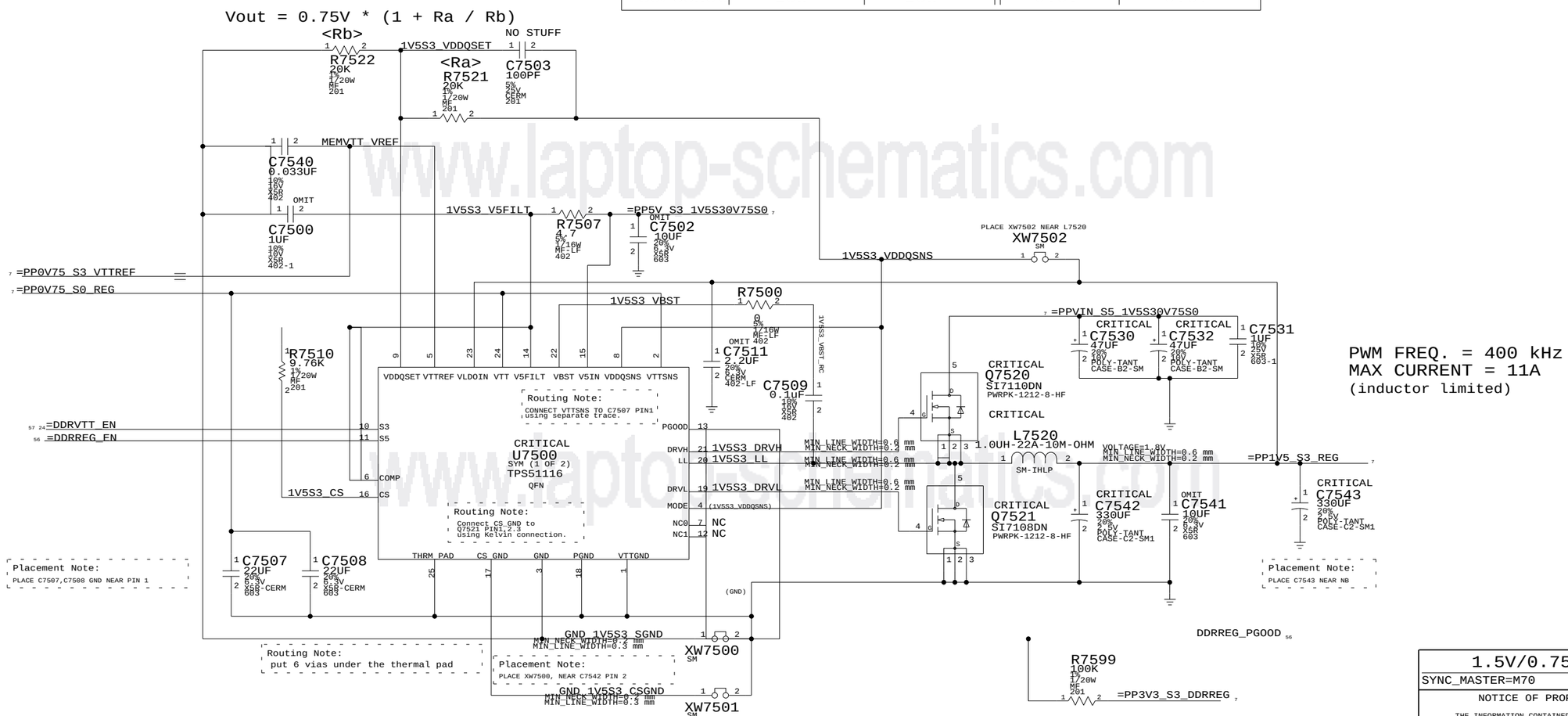
APPLE INC.	SIZE D	DRAWING NUMBER 051-8064	REV. A
	SCALE NONE	SHT 74 OF 109	

1.5V/0.75V POWER SUPPLY

State	PM_S4_STATE_L	PM_SLP_S3_L	PP1V5_S3	PP0V75_S0
S0	HIGH	HIGH	1.5V	0.75V
S3	HIGH	LOW	1.5V	0.0V
S5/G3Hot	LOW	LOW	0.0V	0.0V



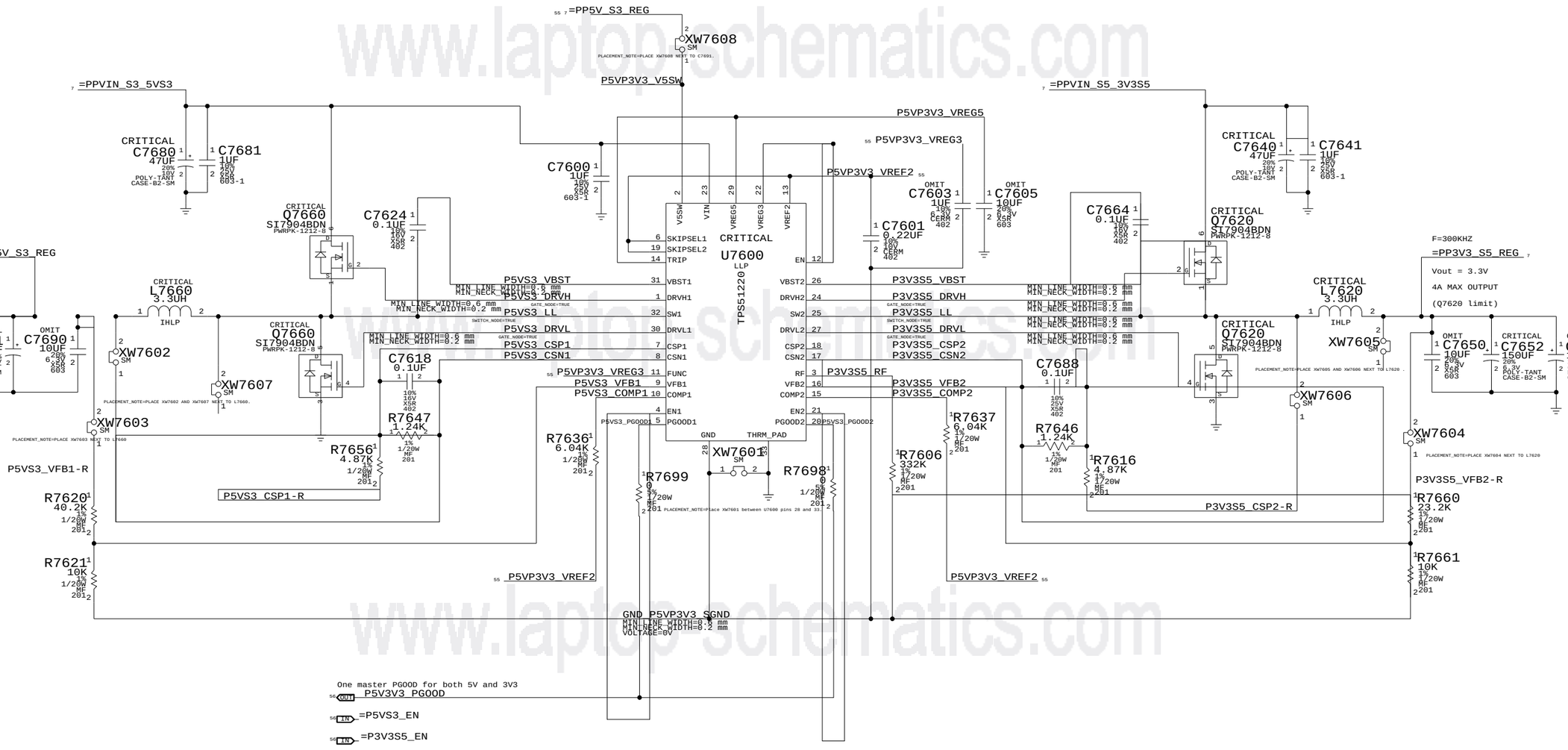
1.5V/0.75V Supplies

SYNC_MASTER=M70 SYNC_DATE=01/09/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 75 OF 109	

5V_S3 / 3V3_S5 POWER SUPPLY



5V / 3.3V Power Supply

SYNC_MASTER=RXU_K20 SYNC_DATE=05/21/2008

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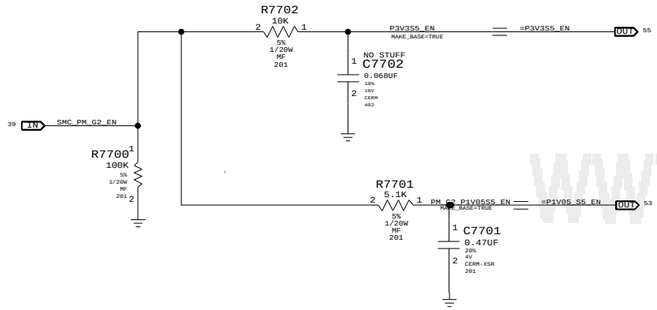
APPLE INC.

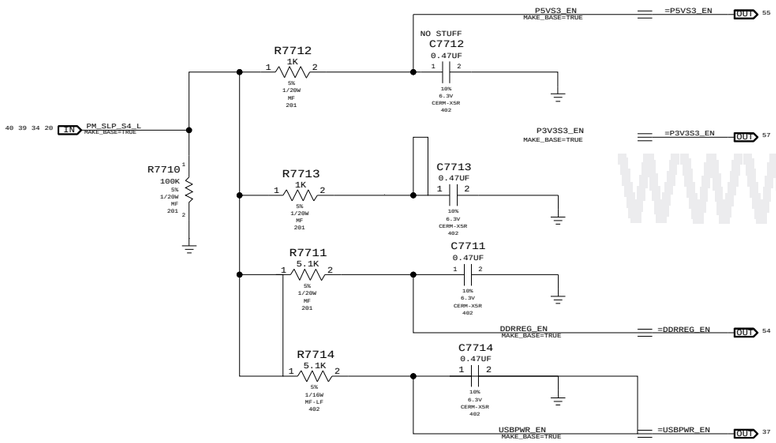
SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 76 OF 109	

Power Control Signals

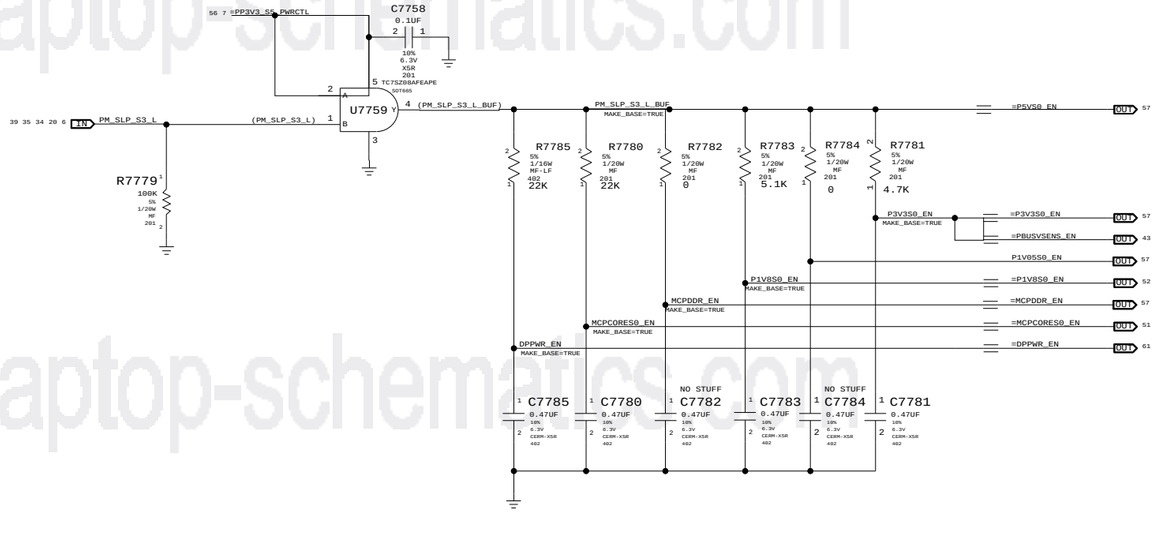
S5 ENABLE



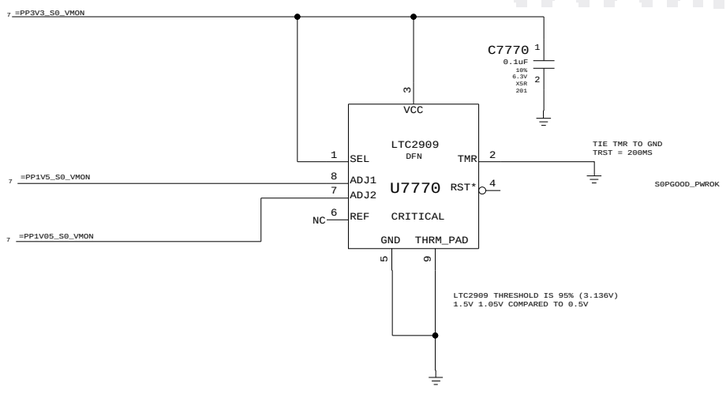
S3 ENABLE



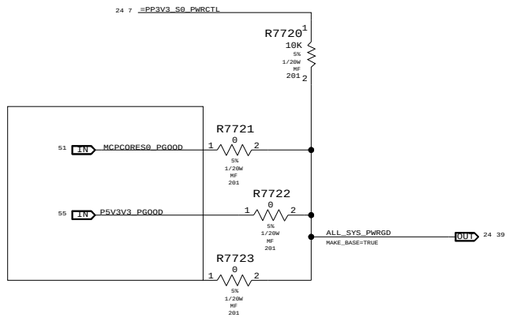
S0 ENABLE



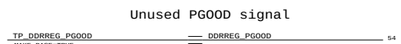
3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

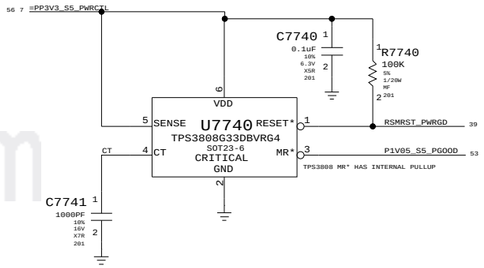


OTHER S0 RAILS PGOOD



Unused PGOOD signal





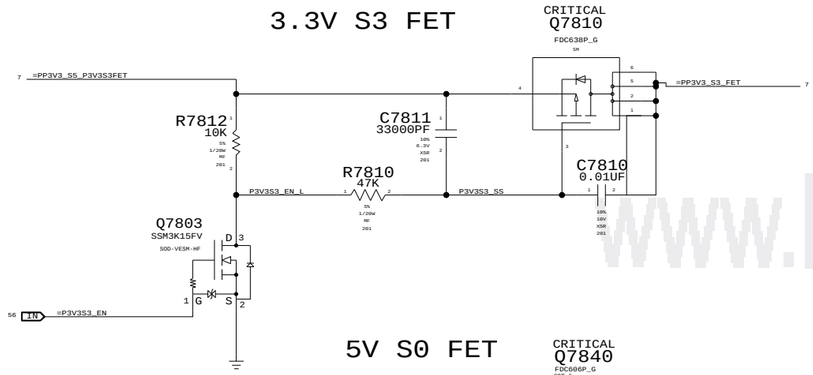
POWER SEQUENCING

SYNC_MASTER=YUAN.MA SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 77 OF 109	

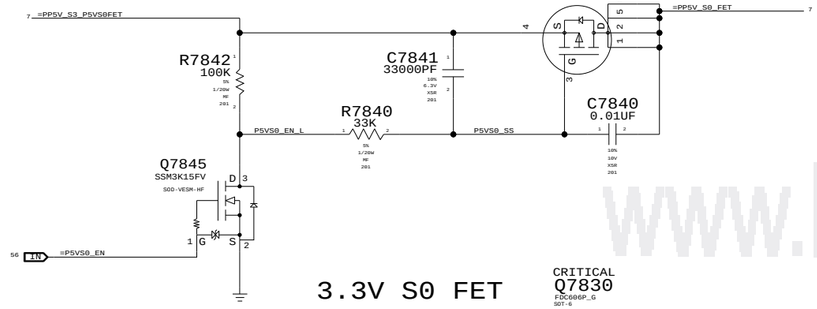
3.3V S3 FET



3.3V S3 FET

MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.315 A (EDP)

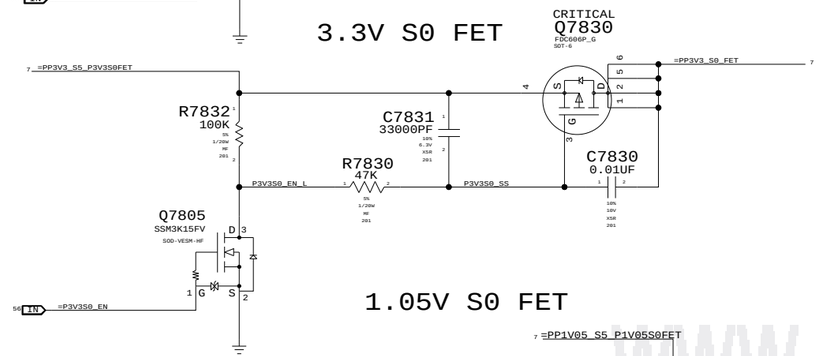
5V S0 FET



5V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	0.562 A (EDP)

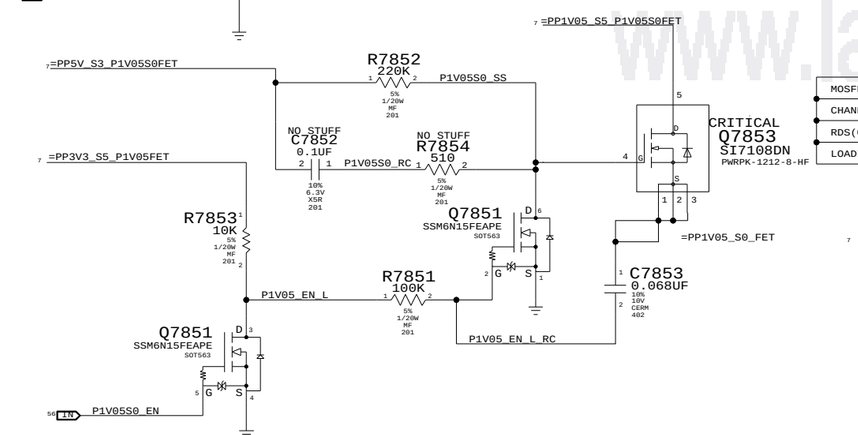
3.3V S0 FET



3.3V S0 FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	2.046 A (EDP)

1.05V S0 FET

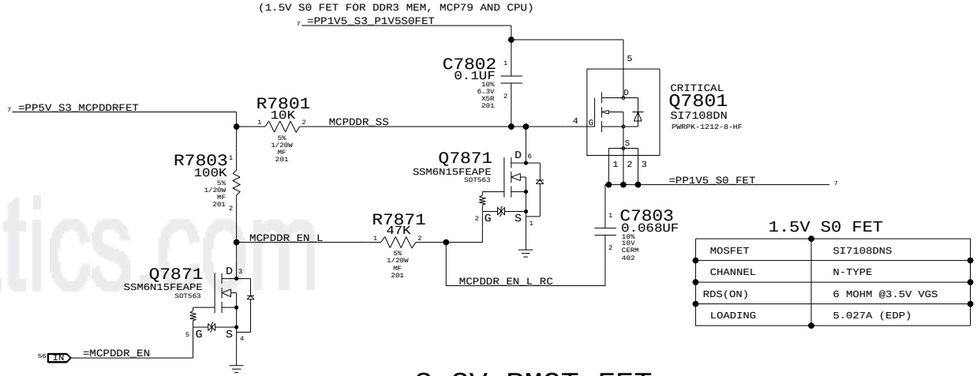


1.05V S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6.1 MOHM @4.5V VGS
LOADING	8.25A (EDP)

1.5V S0 FET

(1.5V S0 FET FOR DDR3 MEM, MCP79 AND CPU)

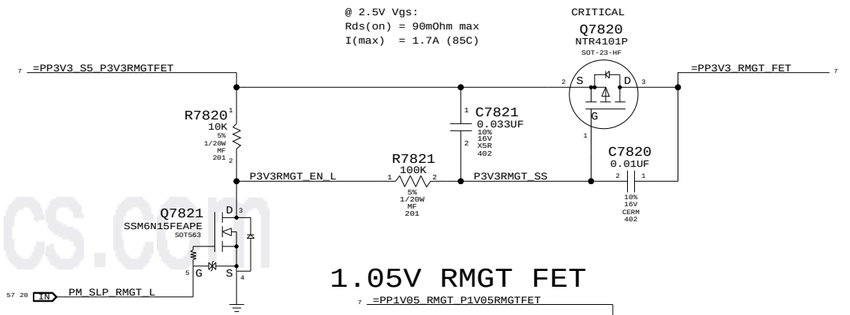


1.5V S0 FET

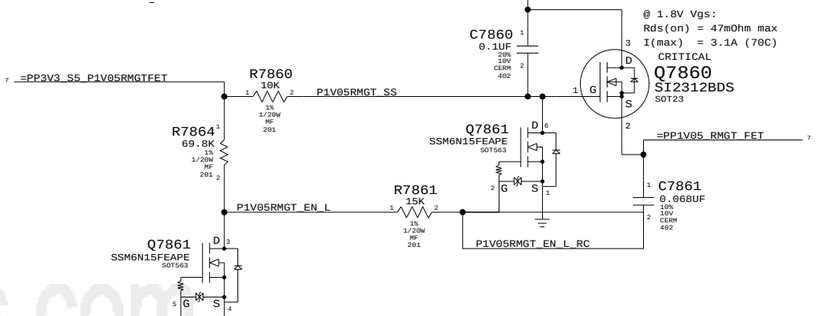
MOSFET	SI7108DNS
CHANNEL	N-TYPE
RDS(ON)	6 MOHM @3.5V VGS
LOADING	5.027A (EDP)

3.3V RMGT FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

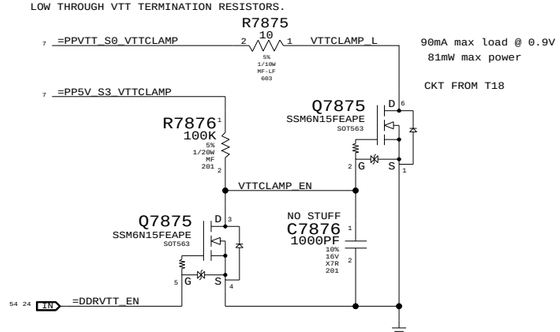


1.05V RMGT FET



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT
NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE
MUST GUARANTEE MEM_CKE SIGNALS ARE LOW
BEFORE RAIL IS TURNED OFF, AND REMAINS LOW
UNTIL AFTER RAIL TURNS BACK ON OR DIMMS
WILL EXIT SELF-REFRESH PREMATURELY.
MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP
ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS
LOW THROUGH VTT TERMINATION RESISTORS.



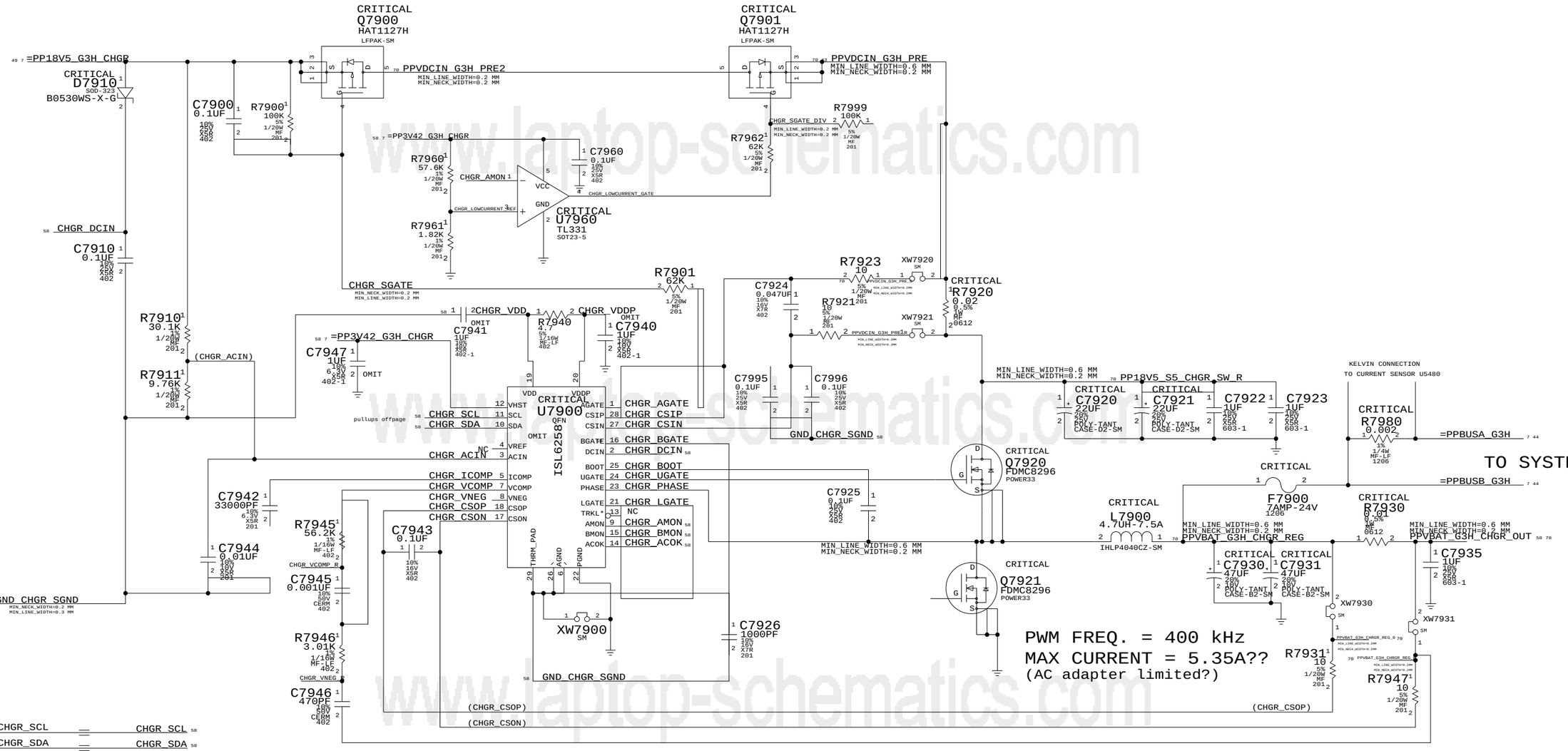
POWER FETS

SYNC_MASTER=YUAN.MA SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 78 OF 109	

PBUS SUPPLY / BATTERY CHARGER



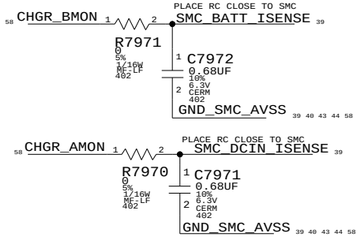
=SMBUS_CHGR_SCL — CHGR_SCL

=SMBUS_CHGR_SDA — CHGR_SDA

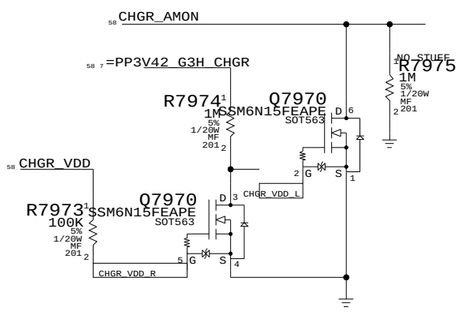
ACOK pullup/down on SMC page

=SMBUS_BC_ACOK — CHGR_ACOK

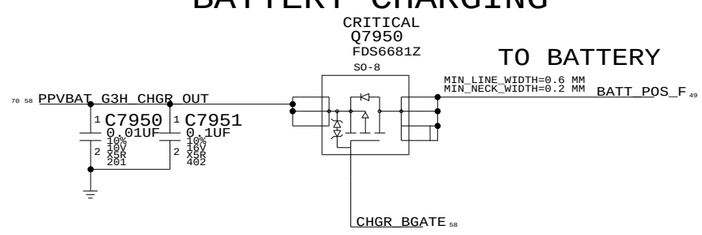
MAKE_BASE=TRUE



AMON PULLDOWN LOGIC



BATTERY CHARGING



PBUS Supply/Battery Charger		
SYNC_MASTER=M70	SYNC_DATE=01/09/2007	

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-8064	A
	SCALE: NONE	SHT 79 OF 109	

LCD + CAMERA CONNECTOR

=PP3V3_S5_LCD
R9002 100K 5% 1/20W MF 201
C9040 0.1UF 10% 6.3V X5R 201
Q9004 SSM3K15FV SOD-VESM-HF
R9014 100K 5% 1/20W MF 201
LVDS_IG_PANEL_PWR
LCDVDD_PWREN_L
R9023 10K 5% 1/20W MF 201
CRITICAL Q9003 FDC638P_G SM
LCDVDD_PWREN_L_R
C9013 3300PF 10% 10V X7R 201
C9011 0.1UF 10% 10V X5R 201
C9012 10UF 20% 6.3V X5R 603 OMIT
PP3V3_LCDVDD_SW
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM

=USB2_CAMERA_N
=USB2_CAMERA_P
CRITICAL L9007 90-OHM-100MA DLP11S
CRITICAL L9005 FERR-120-OHM-1.5A 0402-LF
=PP5V_S3_CAMERA
C9016 1000PF 10% 16V X7R 201
CRITICAL L9004 FERR-120-OHM-1.5A 0402-LF
C9015 1000PF 10% 16V X7R 201

PLACE FILTERS AND CAPS NEAR PINS ON CONNECTOR

L9008 120-OHM-0.3A-EMI 0402-LF
=PP3V3_S0_LCD
(LVDS_DDC_POWER)
C9010 1000PF 10% 16V X7R 201
R9008 10K 5% 1/20W MF 201
R9009 10K 5% 1/20W MF 201
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA

L9052 240-OHM-0.2A-0.8-OHM 0201
=I2C_ALS_SDA
I2C_ALS_SDA_F
L9051 240-OHM-0.2A-0.8-OHM 0201
=I2C_ALS_SCL
I2C_ALS_SCL_F
C9052 10PF 5% 25V NPO 201
C9051 10PF 5% 25V NPO 201

CRITICAL J9000 20347-130E-11 F-RT-SM

VOLTAGE=5V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
PP5V_S3_CAMERA_F
USB2_CAMERA_F_P
USB2_CAMERA_F_N
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
PP3V3_LCDVDD_SW_F
VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM
PP3V3_S0_LCD_F

CAMERA I/F
LCD I/F

LVDS_IG_A_DATA_F_N<0>
LVDS_IG_A_DATA_F_P<0>
LVDS_IG_A_DATA_F_N<1>
LVDS_IG_A_DATA_F_P<1>
LVDS_IG_A_DATA_F_N<2>
LVDS_IG_A_DATA_F_P<2>
LVDS_IG_A_CLK_F_N
LVDS_IG_A_CLK_F_P

LCDBKLT_RTN<1>
LCDBKLT_RTN<2>
LCDBKLT_RTN<3>
LCDBKLT_RTN<4>
LCDBKLT_RTN<5>
LCDBKLT_RTN<6>
PPVOUT_S0_LCDBKLT

LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_P<0>
CRITICAL L9010 90-OHM-100MA DLP11S

LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_P<1>
CRITICAL L9011 90-OHM-100MA DLP11S

LVDS_IG_A_DATA_N<2>
LVDS_IG_A_DATA_P<2>
CRITICAL L9012 90-OHM-100MA DLP11S

LVDS_IG_A_CLK_N
LVDS_IG_A_CLK_P
CRITICAL L9006 90-OHM-100MA DLP11S

518S0433

MIC CONNECTOR

CRITICAL J9050 GS03067-11131-7F F-RT-SM
PP3V3_S0_MIC_F
NC
NC
GND_MIC_F

CRITICAL L9050 600-OHM-300MA 0402
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.20MM VOLTAGE=3.3V
=PP3V3_S0_MIC

CRITICAL L9030 600-OHM-300MA
AUD_MIC_DATA_F
AUD_MIC_DATA

CRITICAL L9031 600-OHM-300MA 0402
AUD_MIC_CLK_F
AUD_MIC_CLK

CRITICAL L9053 600-OHM-300MA 0402
MIN_LINE_WIDTH=0.20MM MIN_NECK_WIDTH=0.20MM
C9050 0.01UF 10% 16V CERM 402
C9053 0.01UF 10% 16V CERM 402
C9030 10PF 5% 25V NPO 201 NO STUFF
C9031 10PF 5% 25V NPO 201 NO STUFF

APN:518S0536

LVDS,Camera Conn. and ALS Conn.

SYNC_MASTER=GPU SYNC_DATE=06/23/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 90 OF 109	

17 =MCP_HDMI_TXC_P — DP_ML_P<3> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_TXC_N — DP_ML_N<3> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_P<0> — DP_ML_P<2> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_N<0> — DP_ML_N<2> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_P<1> — DP_ML_P<1> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_N<1> — DP_ML_N<1> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_P<2> — DP_ML_P<0> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_TXD_N<2> — DP_ML_N<0> — 61 67 MAKE_BASE=TRUE
17 =MCP_HDMI_HPD — DP_HPD — 61 MAKE_BASE=TRUE
17 =MCP_HDMI_DDC_CLK — DP_IG_DDC_CLK — 60 MAKE_BASE=TRUE
17 =MCP_HDMI_DDC_DATA — DP_IG_DDC_DATA — 60 MAKE_BASE=TRUE

DP_AUX_CH_C_N — BI — 6 35 61 67

DP_AUX_CH_C_P — BI — 6 35 61 67

60 BI DP_IG_DDC_DATA — R9300 33 5% 1/20W MF 201 — C9300 0.1UF 10% 6.3V X5R 201 — 67 DP_AUX_CH_SW_N

60 BI DP_IG_DDC_CLK — R9301 33 5% 1/20W MF 201 — C9301 0.1UF 10% 6.3V X5R 201 — 67 DP_AUX_CH_SW_P

Q9300 SSM6N15FEAPE SOT563 (pins 3 D, 4 S, G 5)

Q9300 SSM6N15FEAPE SOT563 (pins D 6, 2 G, S 1)

67 17 BI DP_IG_AUX_CH_P

67 17 BI DP_IG_AUX_CH_N

1R9306 1K 5% 1/20W MF 201

=PP5V_S0_DP_AUX_MUX (7)

1R9302 100K 5% 1/20W MF 201

DDC_CA_DET_LS5V_L

Q9301 SSM3K15FV SOD-VESM-HF (pins 3 D, 2 S, G 1)

61 ANA DP_CA_DET

DP_IG_CA_DET — OUT — 17

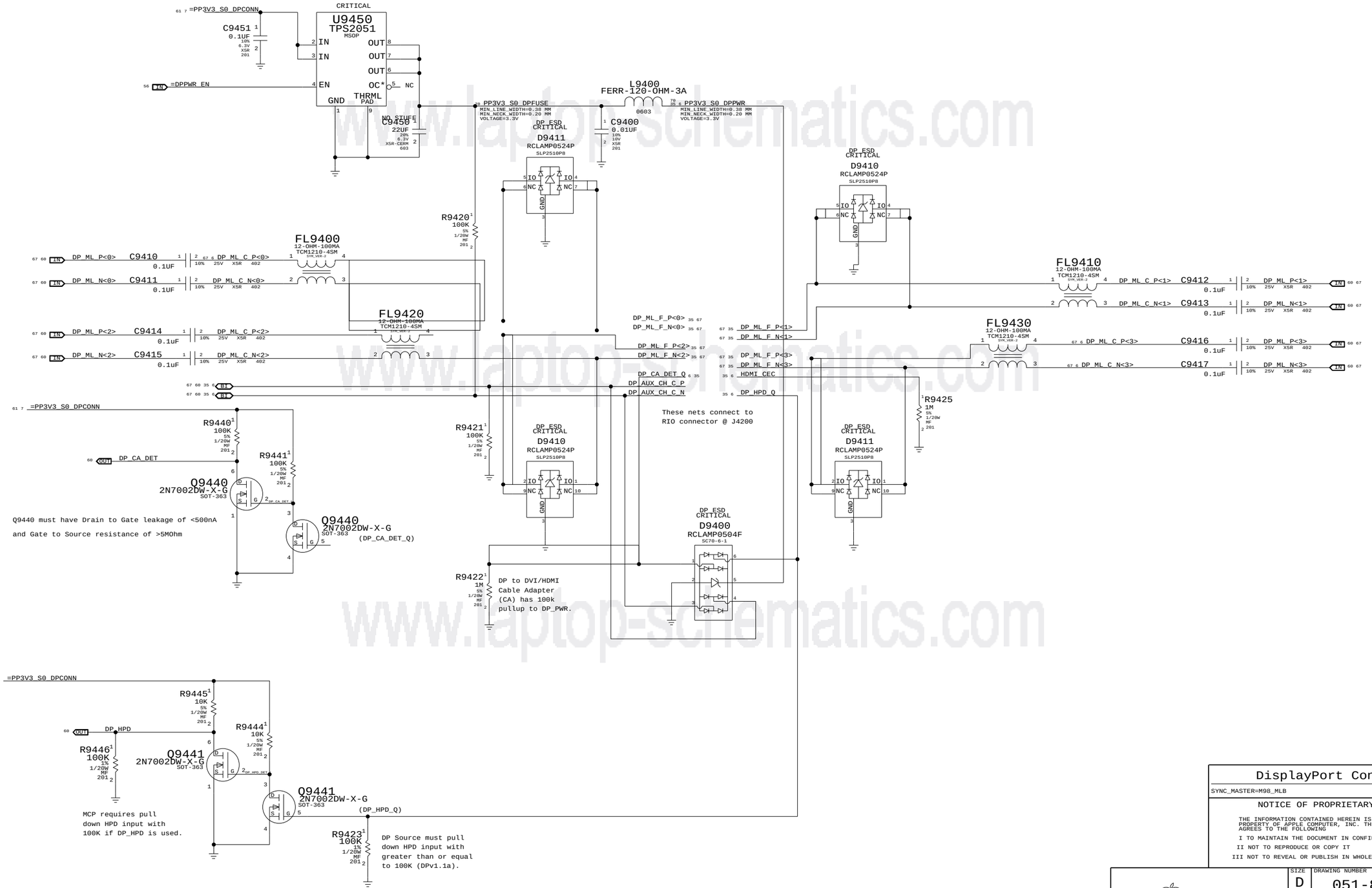
DISPLAYPORT SUPPORT

SYNC_MASTER=NMARTIN SYNC_DATE=12/18/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE NONE — SHT 93 OF 109



DisplayPort Connector

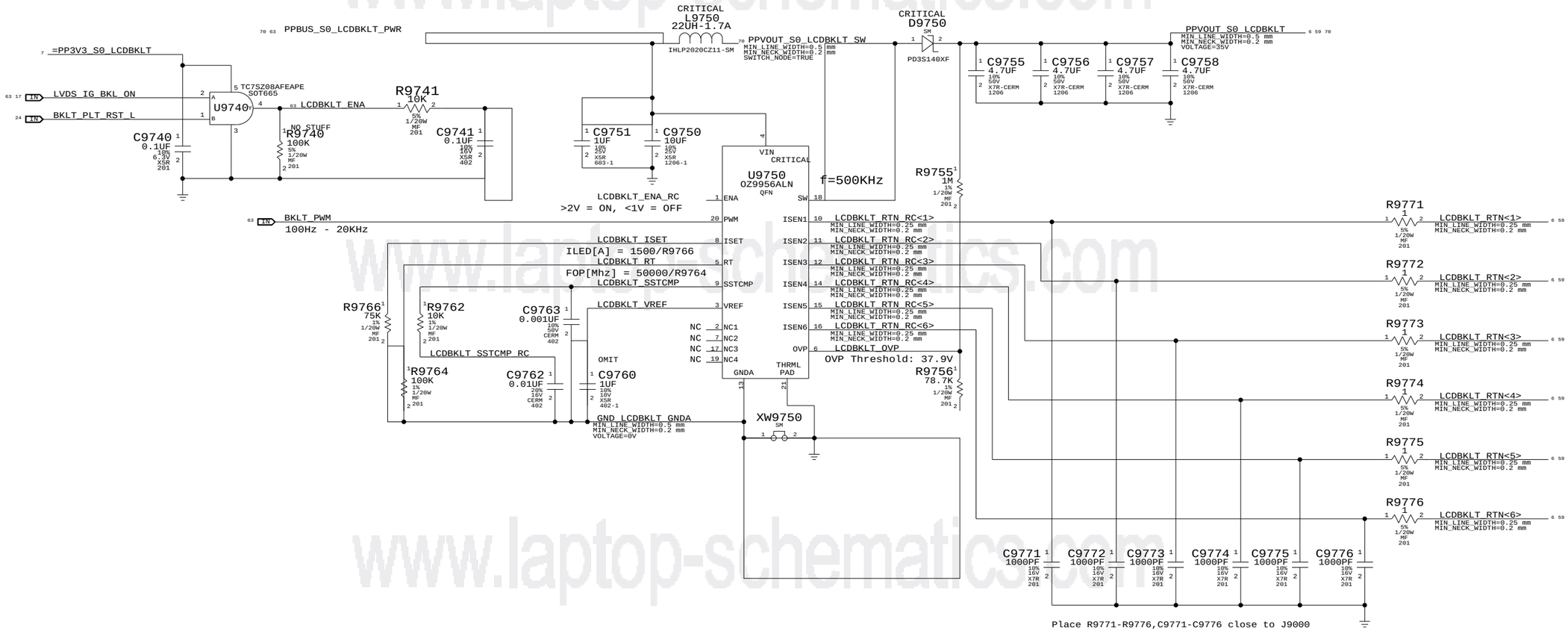
SYNC_MASTER=M98_MLB SYNC_DATE=01/17/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	94	109

LED Backlight Driver

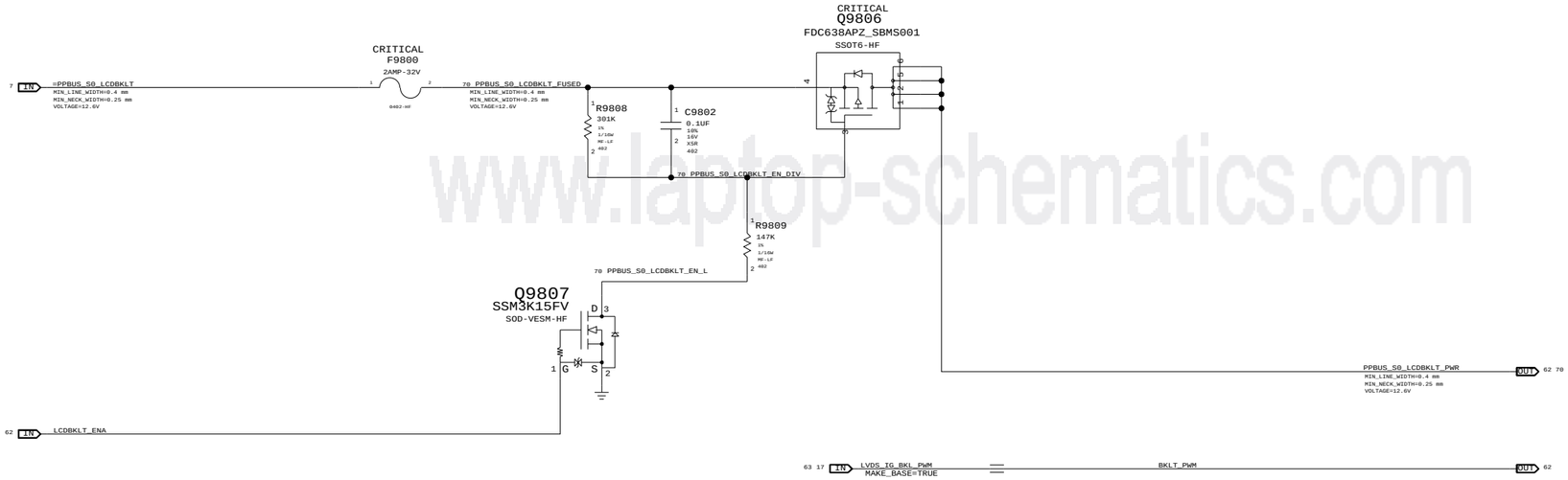


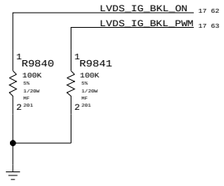
LED Backlight Driver

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 97 OF 109	





LCD Backlight Support

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT 98 OF 109	

ADDITIONAL CPU VCORE HF DECOUPLING

40x 2.2uF 0402

11 10 7 =PPVCORE_S0_CPU

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C9900 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9901 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9902 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9903 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9904 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9905 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9906 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9907 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9908 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9909 2.2UF 20% 6.3V CERM 402-LF OMIT

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C9910 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9911 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9912 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9913 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9914 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9915 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9916 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9917 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9918 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9919 2.2UF 20% 6.3V CERM 402-LF OMIT

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C9920 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9921 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9922 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9923 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9924 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9925 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9926 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9927 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9928 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9929 2.2UF 20% 6.3V CERM 402-LF OMIT

LAYOUT NOTE:
PLACE ON OPPOSITE SIDE OF CPU

CRITICAL C9930 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9931 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9932 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9933 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9934 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9935 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9936 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9937 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9938 2.2UF 20% 6.3V CERM 402-LF OMIT	CRITICAL C9939 2.2UF 20% 6.3V CERM 402-LF OMIT

Additional CPU/GPU Decoupling

SYNC_MASTER= SYNC_DATE=

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE	SHT	OF
NONE	99	109

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	9 13
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	9 13
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	9 13
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	9 13
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	9 13
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	9 13
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	9 13
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	9 13
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	9 13
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	9 13
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	9 13
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	9 13
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	9 13
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	9 13
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	9 13
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	8 9 13
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	13
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	9 13
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	8 9 12 13
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	9 13
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	9 13
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	8 9
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	9 13
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	8 9 13
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	8 9 13
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	9 13 40 50
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	9 12 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	9 13
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	9 13
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	9 13 40
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	9 13
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	9 13
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	8 9 13 50
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	9 13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	13
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	9 13
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	9 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	6 12 13
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	6 12 13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	13
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	13
	CPU_IERR_L	CPU_50S		CPU_IERR_L	9
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	20 50
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	50
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	9 25
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	9
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	9
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	9
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 9 12
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	9 12
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 9 12
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 9 12
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 9 12
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	6 9 12
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	6 9 12
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	6 12
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	10 11 50
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	11
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	10 50
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	10 50
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	50
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	50

CPU/FSB Constraints

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A
SCALE: NONE	SHT: 100 OF 109	

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_50S	*	=50_OHM_SE	=50_OHM_SE	0.110 MM	=50_OHM_SE	=STANDARD	=STANDARD
MEM_50S_VDD	*	=50_OHM_SE	=50_OHM_SE	0.110 MM	=50_OHM_SE	=STANDARD	=STANDARD
MEM_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
MEM_90D_VDD	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=2.28:1_SPACING	?
MEM_CTRL2CTRL	*	=1.1:1_SPACING	?
MEM_CTRL2MEM	*	=2.28:1_SPACING	?
MEM_CMD2CMD	*	=1.1:1_SPACING	?
MEM_CMD2MEM	*	=2.28:1_SPACING	?
MEM_DATA2DATA	*	=1.1:1_SPACING	?
MEM_DATA2MEM	*	=2.28:1_SPACING	?
MEM_DQS2MEM	*	=2.28:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PP1V5_MEM	*	PWR_P2MM
MEM_CTRL	PP1V5_MEM	*	PWR_P2MM
MEM_DATA	PP1V5_MEM	*	PWR_P2MM
MEM_DQS	PP1V5_MEM	*	PWR_P2MM
MEM_CMD	PP1V5_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	PWR	*	BUS2PWR_GND
MEM_CLK	GND	*	BUS2PWR_GND
MEM_CTRL	PWR	*	BUS2PWR_GND
MEM_CTRL	GND	*	BUS2PWR_GND
MEM_CMD	PWR	*	BUS2PWR_GND
MEM_CMD	GND	*	BUS2PWR_GND
MEM_DATA	PWR	*	BUS2PWR_GND
MEM_DATA	GND	*	BUS2PWR_GND
MEM_DQS	PWR	*	BUS2PWR_GND
MEM_DQS	GND	*	BUS2PWR_GND

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_90D	MEM_CLK	MEM_A_CLK_P<0>	14 27 28 33
MEM_A_CLK	MEM_90D	MEM_CLK	MEM_A_CLK_N<0>	14 27 28 33
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CKE<1..0>	14 27 28 33
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_CS_L<1..0>	14 27 28 33
MEM_A_CNTL	MEM_50S	MEM_CTRL	MEM_A_ODT<1..0>	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_A<14..0>	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_BA<2..0>	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_RAS_L	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_CAS_L	14 27 28 33
MEM_A_CMD	MEM_50S	MEM_CMD	MEM_A_WE_L	14 27 28 33
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	14 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	14 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	14 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	14 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	14 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	14 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	14 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	14 28
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DM<0>	14 27
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DM<1>	14 27
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DM<2>	14 27
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DM<3>	14 27
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DM<4>	14 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DM<5>	14 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DM<6>	14 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DM<7>	14 28
MEM_A_DQS0	MEM_90D	MEM_DQS	MEM_A_DQS_P<0>	14 27
MEM_A_DQS0	MEM_90D	MEM_DQS	MEM_A_DQS_N<0>	14 27
MEM_A_DQS1	MEM_90D	MEM_DQS	MEM_A_DQS_P<1>	14 27
MEM_A_DQS1	MEM_90D	MEM_DQS	MEM_A_DQS_N<1>	14 27
MEM_A_DQS2	MEM_90D	MEM_DQS	MEM_A_DQS_P<2>	14 27
MEM_A_DQS2	MEM_90D	MEM_DQS	MEM_A_DQS_N<2>	14 27
MEM_A_DQS3	MEM_90D	MEM_DQS	MEM_A_DQS_P<3>	14 27
MEM_A_DQS3	MEM_90D	MEM_DQS	MEM_A_DQS_N<3>	14 27
MEM_A_DQS4	MEM_90D	MEM_DQS	MEM_A_DQS_P<4>	14 28
MEM_A_DQS4	MEM_90D	MEM_DQS	MEM_A_DQS_N<4>	14 28
MEM_A_DQS5	MEM_90D	MEM_DQS	MEM_A_DQS_P<5>	14 28
MEM_A_DQS5	MEM_90D	MEM_DQS	MEM_A_DQS_N<5>	14 28
MEM_A_DQS6	MEM_90D	MEM_DQS	MEM_A_DQS_P<6>	14 28
MEM_A_DQS6	MEM_90D	MEM_DQS	MEM_A_DQS_N<6>	14 28
MEM_A_DQS7	MEM_90D	MEM_DQS	MEM_A_DQS_P<7>	14 28
MEM_A_DQS7	MEM_90D	MEM_DQS	MEM_A_DQS_N<7>	14 28
MEM_B_CLK	MEM_90D	MEM_CLK	MEM_B_CLK_P<0>	14 29 30 33
MEM_B_CLK	MEM_90D	MEM_CLK	MEM_B_CLK_N<0>	14 29 30 33
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CKE<1..0>	14 29 30 33
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_CS_L<1..0>	14 29 30 33
MEM_B_CNTL	MEM_50S	MEM_CTRL	MEM_B_ODT<1..0>	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_A<14..0>	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_BA<2..0>	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_RAS_L	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_CAS_L	14 29 30 33
MEM_B_CMD	MEM_50S	MEM_CMD	MEM_B_WE_L	14 29 30 33
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	14 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	14 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	14 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	14 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	14 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	14 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	14 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	14 30
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DM<0>	14 29
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DM<1>	14 29
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DM<2>	14 29
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DM<3>	14 29
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DM<4>	14 30
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DM<5>	14 30
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DM<6>	14 30
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DM<7>	14 30
MEM_B_DQS0	MEM_90D	MEM_DQS	MEM_B_DQS_P<0>	14 29
MEM_B_DQS0	MEM_90D	MEM_DQS	MEM_B_DQS_N<0>	14 29
MEM_B_DQS1	MEM_90D	MEM_DQS	MEM_B_DQS_P<1>	14 29
MEM_B_DQS1	MEM_90D	MEM_DQS	MEM_B_DQS_N<1>	14 29
MEM_B_DQS2	MEM_90D	MEM_DQS	MEM_B_DQS_P<2>	14 29
MEM_B_DQS2	MEM_90D	MEM_DQS	MEM_B_DQS_N<2>	14 29
MEM_B_DQS3	MEM_90D	MEM_DQS	MEM_B_DQS_P<3>	14 29
MEM_B_DQS3	MEM_90D	MEM_DQS	MEM_B_DQS_N<3>	14 29
MEM_B_DQS4	MEM_90D	MEM_DQS	MEM_B_DQS_P<4>	14 30
MEM_B_DQS4	MEM_90D	MEM_DQS	MEM_B_DQS_N<4>	14 30
MEM_B_DQS5	MEM_90D	MEM_DQS	MEM_B_DQS_P<5>	14 30
MEM_B_DQS5	MEM_90D	MEM_DQS	MEM_B_DQS_N<5>	14 30
MEM_B_DQS6	MEM_90D	MEM_DQS	MEM_B_DQS_P<6>	14 30
MEM_B_DQS6	MEM_90D	MEM_DQS	MEM_B_DQS_N<6>	14 30
MEM_B_DQS7	MEM_90D	MEM_DQS	MEM_B_DQS_P<7>	14 30
MEM_B_DQS7	MEM_90D	MEM_DQS	MEM_B_DQS_N<7>	14 30
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD VOLTAGE=0V	15
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND VOLTAGE=1.5V	15
		MEM_CLK	MEM_RESET_L	30 26 27 28 29

=PP1V8R1V5_S0_MCP_MEM NET_SPACING_TYPE=PP1V5_MEM 22 15

GND NET_SPACING_TYPE=GND

Memory Constraints

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE: NONE SHT 101 OF 109

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SATA_100D_HDD	*	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD	=100_OHM_DIFF_HDD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	16 34
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	16 34
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	16 34
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	16 34
	PCIE_90D	PCIE	PCIE_FW_R2D_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_N	
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_N	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	
	PCIE_90D	PCIE	PCIE_FC_R2D_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_N	
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P	
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N	
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P	
	PCIE_90D	PCIE	PCIE_FC_D2R_N	
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	8 16
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	16 34
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	16 34
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N	
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	16
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	6 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	6 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_F_P<3..0>	35 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_F_N<3..0>	35 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	60 61
DP_ML	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	60 61
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	17 60
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	17 60
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	6 35 60 61
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	6 35 60 61
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_P	60
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_SW_N	60
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	17 23
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	17 23
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_P	6 59
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_F_N	6 59
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	17 59
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	17 59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_F_P<2..0>	59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_F_N<2..0>	59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	6 17 59
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	6 17 59
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	8 17
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	8 17
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	8 17
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	8 17
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	8 17
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	8 17
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	8 17
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	8 17
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	17 23
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	17 23
SATA_HDD_R2D	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_P	19 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_C_N	19 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_P	6 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_N	6 36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_P	36
	SATA_100D_HDD	SATA	SATA_HDD_R2D_UF_N	36
SATA_HDD_D2R	SATA_100D_HDD	SATA	SATA_HDD_D2R_P	19 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_N	19 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_P	6 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_C_N	6 36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_P	36
	SATA_100D_HDD	SATA	SATA_HDD_D2R_UF_N	36
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	19

MCP Constraints 1

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0> 6 12 18
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>
PCI_AD24	PCI_55S	PCI	PCI_AD<24>
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>
PCI_AD	PCI_55S	PCI	PCI_PAR
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>
PCI_CNTL	PCI_55S	PCI	PCI_IRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_DEVSEL_L
PCI_CNTL	PCI_55S	PCI	PCI_PERR_L
PCI_CNTL	PCI_55S	PCI	PCI_SERR_L
PCI_CNTL	PCI_55S	PCI	PCI_STOP_L
PCI_CNTL	PCI_55S	PCI	PCI_TRDY_L
PCI_CNTL	PCI_55S	PCI	PCI_FRAME_L
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L 18
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L 18
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R 18
	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP 18
LPC_AD	LPC_55S	LPC	LPC_AD<3..0> 18 39 41
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L 18 39 41
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L 18 24
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R 18 24
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC 24 39
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS 24 41
USB_EXTA	USB_90D	USB	USB_EXTA_P 8 19
	USB_90D	USB	USB_EXTA_N 8 19
	USB_90D	USB	USB_EXTA_MUXED_P 37
	USB_90D	USB	USB_EXTA_MUXED_N 37
	USB_90D	USB	CONN_USB_EXTA_P
	USB_90D	USB	CONN_USB_EXTA_N
USB_MINI	USB_90D	USB	USB_MINI_P 8 19
	USB_90D	USB	USB_MINI_N 8 19
USB_EXTD	USB_90D	USB	USB_EXTD_P 8 19
	USB_90D	USB	USB_EXTD_N 8 19
USB_CAMERA	USB_90D	USB	USB_CAMERA_P 8 19
	USB_90D	USB	USB_CAMERA_N 8 19
	USB_90D	USB	USB_CAMERA_CONN_P
	USB_90D	USB	USB_CAMERA_CONN_N
USB_BT	USB_90D	USB	USB_BT_P 8 19
	USB_90D	USB	USB_BT_N 8 19
	USB_90D	USB	CONN_USB2_BT_P
	USB_90D	USB	CONN_USB2_BT_N
USB_TPAD	USB_90D	USB	USB_TPAD_P 8 19
	USB_90D	USB	USB_TPAD_N 8 19
	USB_90D	USB	CONN_TPAD_USB_P
	USB_90D	USB	CONN_TPAD_USB_N
USB_IR	USB_90D	USB	USB_IR_P 8 19
	USB_90D	USB	USB_IR_N 8 19
USB_EXTB	USB_90D	USB	USB_EXTB_P 8 19
	USB_90D	USB	USB_EXTB_N 8 19
	USB_90D	USB	CONN_USB_EXTB_P
	USB_90D	USB	CONN_USB_EXTB_N
USB_EXCARD	USB_90D	USB	USB_EXCARD_P 8
	USB_90D	USB	USB_EXCARD_N 8
USB_EXTC	USB_90D	USB	USB_EXTC_P 8
	USB_90D	USB	USB_EXTC_N 8
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND 19
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK 6 12 20 42
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA 6 12 20 42
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK 20 42
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA 20 42
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK 6 20 35
	HDA_55S	HDA	HDA_BIT_CLK_R 20
HDA_SYNC	HDA_55S	HDA	HDA_SYNC 6 20 35
	HDA_55S	HDA	HDA_SYNC_R 20
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L 20
	HDA_55S	HDA	HDA_RST_L 20 35
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0 6 20 35
	HDA_55S	HDA	HDA_SDIN_CODEC
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT 6 20 35
	HDA_55S	HDA	HDA_SDOUT_R 20
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP 20
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R 20 24
	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK 24 39
SPI_CLK	SPI_55S	SPI	SPI_CLK_R 20 41
	SPI_55S	SPI	SPI_CLK 48
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R 20 41
	SPI_55S	SPI	SPI_MOSI 48
SPI_MISO	SPI_55S	SPI	SPI_MISO 20 41
	SPI_55S	SPI	SPI_MISO_R 48
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L 20 41
	SPI_55S	SPI	SPI_CS0_L
SPI_CLK	SPI_55S	SPI	SPI_CLK_MUX 41 48
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_MUX 41 48
SPI_MISO	SPI_55S	SPI	SPI_MISO_MUX 41 48
SPI_CS0	SPI_55S	SPI	SPI_MLB_CS_L 41 48

MCP Constraints 2

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8064	A

SCALE: NONE SHT 103 OF 109

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL 42
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA 42
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL 42
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA 42
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL 42
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA 42
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL 6 42
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA 6 42
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL 42
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P
	1TO1_DIFFPAIR		CHGR_CSI_N
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P
	1TO1_DIFFPAIR		CHGR_CSO_N

SMC Constraints

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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1	PP0V75_S0	NET_SPACING_TYPE=PWR 6 7
2	PP0V75_S3	NET_SPACING_TYPE=PWR 7
3	PP0V75_S3_MEM_VREFCA	NET_SPACING_TYPE=PWR 25 27 28 29 30
4	PP0V75_S3_MEM_VREFDQ	NET_SPACING_TYPE=PWR 25 27 28 29 30
5	PP18V5_DCIN	NET_SPACING_TYPE=PWR 6 49
6	PP18V5_DCIN_ONEWIRE	NET_SPACING_TYPE=PWR 49
7	PP18V5_G3H	NET_SPACING_TYPE=PWR 6 7
8	PP18V5_S5_CHGR_SW_R	NET_SPACING_TYPE=PWR 58
10	PP1V05_ENET_MCP_PLL_MAC	NET_SPACING_TYPE=PWR 17 22
9	PP1V05_RMGT	NET_SPACING_TYPE=PWR 7
12	PP1V05_S0	NET_SPACING_TYPE=PWR 6 7
11	PP1V05_S0_MCP_PEX_AVDD	NET_SPACING_TYPE=PWR 7 22
13	PP1V05_S0_MCP_PEX_AVDD_R	NET_SPACING_TYPE=PWR
14	PP1V05_S0_MCP_PEX_DVDD_R	NET_SPACING_TYPE=PWR
16	PP1V05_S0_MCP_PLL_CORE	NET_SPACING_TYPE=PWR 15 22
15	PP1V05_S0_MCP_PLL_FSB	NET_SPACING_TYPE=PWR 13 22
18	PP1V05_S0_MCP_PLL_NV	NET_SPACING_TYPE=PWR 20 22
17	PP1V05_S0_MCP_PLL_PEX	NET_SPACING_TYPE=PWR 16 22
19	PP1V05_S0_MCP_PLL_SATA	NET_SPACING_TYPE=PWR 19 22
21	PP1V05_S0_MCP_SATA_AVDD	NET_SPACING_TYPE=PWR 19 22
20	PP1V05_S5	NET_SPACING_TYPE=PWR 6 7
23	PP1V2_S0_FC_VDD	NET_SPACING_TYPE=PWR
160	PP1V5_S0	NET_SPACING_TYPE=PP1V5_MEM 6 7
161	PP1V5_S0_FC_AVDDL_F	NET_SPACING_TYPE=PWR
22	PP1V5_S0_FC_AVDDT_F	NET_SPACING_TYPE=PWR
24	PP1V5_S3	NET_SPACING_TYPE=PP1V5_MEM 6 7
25	PP1V8_S0	NET_SPACING_TYPE=PWR 6 7
26	PP2V_S0_MCPREG_REF	NET_SPACING_TYPE=PWR
28	PP3V3_LCDVDD_SW	NET_SPACING_TYPE=PWR 59
27	PP3V3_LCDVDD_SW_F	NET_SPACING_TYPE=PWR 6 59
30	PP3V3_RMGT	NET_SPACING_TYPE=PWR 7
29	PP3V3_S0	NET_SPACING_TYPE=PWR 6 7
31	PP3V3_S0_CPUTHMSNS_R	NET_SPACING_TYPE=PWR 45
33	PP3V3_S0_DPFUSE	NET_SPACING_TYPE=PWR 61
32	PP3V3_S0_DPPWR	NET_SPACING_TYPE=PWR 6 35 61
35	PP3V3_S0_FC_AVDD_F	NET_SPACING_TYPE=PWR
34	PP3V3_S0_HDD_F	NET_SPACING_TYPE=PWR 6 36
36	PP3V3_S0_IMVP6_3V3	NET_SPACING_TYPE=PWR 50
38	PP3V3_S0_LCD_F	NET_SPACING_TYPE=PWR 6 59
37	PP3V3_S0_MCPREG_VREF3	NET_SPACING_TYPE=PWR
39	PP3V3_S0_MCP_DAC	NET_SPACING_TYPE=GND 21 23
41	PP3V3_S0_MCP_PLL_USB	NET_SPACING_TYPE=PWR 19 22
40	PP3V3_S0_MCP_VPLL	NET_SPACING_TYPE=PWR 17 23
43	PP3V3_S3	NET_SPACING_TYPE=PWR 6 7
42	PP3V3_S3_AP_AUX	NET_SPACING_TYPE=PWR 6 34
44	PP3V3_S3_AP_AUX_F	NET_SPACING_TYPE=PWR 34
46	PP3V3_S0_MIC_F	NET_SPACING_TYPE=PWR 6 59
45	PP3V3_S5	NET_SPACING_TYPE=PWR 6 7
48	PP3V3_S5_AVREF_SMC	NET_SPACING_TYPE=PWR 39 40
47	PP3V3_S5_MCP	NET_SPACING_TYPE=PWR
49	PP3V3_S5_SMC_AVCC	NET_SPACING_TYPE=PWR 39
50	PP3V42G3H_SW	NET_SPACING_TYPE=PWR 49
52	PP3V42_G3H	NET_SPACING_TYPE=PWR 6 7
51	PP3V42_G3H_IPD_F	NET_SPACING_TYPE=PWR 6 38
54	PP3V42_G3H_SMCUSBMUX_R	NET_SPACING_TYPE=PWR 37
53	PP5V_S0	NET_SPACING_TYPE=PWR 6 7
55	PP5V_S0_IMVP6_VDD	NET_SPACING_TYPE=PWR 50
57	PP5V_S0_KBDLED_F	NET_SPACING_TYPE=PWR 6 38
56	PP5V_S0_MCPREG_VCC	NET_SPACING_TYPE=PWR
59	PP5V_S3	NET_SPACING_TYPE=PWR 6 7
58	PP5V_S3_CAMERA_F	NET_SPACING_TYPE=PWR 6 59
72	PP5V_S3_MCPREG_LDO	NET_SPACING_TYPE=PWR
71	PP5V_S3_TOPCASE_F	NET_SPACING_TYPE=PWR 6 38
73	PP5V_S3_USB2_EXTA	NET_SPACING_TYPE=PWR 37
74	PP5V_S3_USB2_EXTA_F	NET_SPACING_TYPE=PWR 6 35 37
76	PPBUS_G3H	NET_SPACING_TYPE=PWR 6 7
75	PPBUS_G3HRS5_VSENSE	NET_SPACING_TYPE=PWR 43
78	PPBUS_R_G3H	NET_SPACING_TYPE=PWR 6 7
77	PPBUS_S0_LCDBKLT_EN_DIV	NET_SPACING_TYPE=PWR 63
79	PPBUS_S0_LCDBKLT_EN_L	NET_SPACING_TYPE=PWR 63
81	PPBUS_S0_LCDBKLT_FUSED	NET_SPACING_TYPE=PWR 63
80	PPBUS_S0_LCDBKLT_PWR	NET_SPACING_TYPE=PWR 62 63
83	PPDCIN_G3H	NET_SPACING_TYPE=PWR 6 7
82	PPDCIN_G3H_R	NET_SPACING_TYPE=PWR 49
84	PPMCPCORE_S0	NET_SPACING_TYPE=PWR 6 7
86	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR 49 70
85	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR 58 70
102	PPVBATT_G3H_R	NET_SPACING_TYPE=PWR 49 70
103	PPVBAT_G3H_CHGR_OUT	NET_SPACING_TYPE=PWR 58 70
104	PPVBAT_G3H_CHGR_REG	NET_SPACING_TYPE=PWR 58
105	PPVBAT_G3H_CHRGR_REG_0	NET_SPACING_TYPE=PWR 58
106	PPVBAT_G3H_CHRGR_REG_R	NET_SPACING_TYPE=PWR 58
108	PPVCORE_S0_CPU	NET_SPACING_TYPE=PWR 6 7
109	PPVDCIN_G3H_PRE	NET_SPACING_TYPE=PWR 43 58
107	PPVDCIN_G3H_PRE2	NET_SPACING_TYPE=PWR 58
110	PPVDCIN_G3H_PRE_0	NET_SPACING_TYPE=PWR 58
112	PPVDCIN_G3H_PRE_R	NET_SPACING_TYPE=PWR 58
113	PPVIN_S5_IMVP6_VIN	NET_SPACING_TYPE=PWR 50
111	PPVOUT_S0_LCDBKLT	NET_SPACING_TYPE=PWR 6 59 62
114	PPVOUT_S0_LCDBKLT_SW	NET_SPACING_TYPE=PWR 62

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR	*	=STANDARD	?
BUS2PWR_GND	*	0.228 MM	?

M96 Power and Ground Nets

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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M96 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,ISL12,ISL13,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	0.200 MM	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.210 MM	0.200 MM			
55_OHM_SE	ISL2,ISL13	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.250 MM	0.200 MM			
50_OHM_SE	ISL2,ISL13	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.350 MM	0.200 MM			
40_OHM_SE	ISL2,ISL13	Y	0.122 MM	0.122 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	Y	0.110 MM	0.110 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.215 MM	0.200 MM			
27P4_OHM_SE	*	Y	0.215 MM	0.215 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.132 MM	0.132 MM		0.200 MM	0.200 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.180 MM	0.180 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.205 MM	0.200 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.179 MM	0.179 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF_HDD	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF_HDD	ISL2,ISL4,ISL5,ISL10,ISL11,ISL13	Y	0.065 MM	0.065 MM		0.280 MM	0.280 MM
100_OHM_DIFF_HDD	TOP,BOTTOM	Y	0.179 MM	0.179 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE_MEM	TOP,BOTTOM	Y	0.170 MM	0.110 MM	10 MM		
40_OHM_SE_MEM	ISL2,ISL13	Y	0.122 MM	0.066 MM	170 MM	=STANDARD	=STANDARD
40_OHM_SE_MEM	*	Y	0.110 MM	0.066 MM	170 MM	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
4:1_SPACING	*	0.4 MM	?
2.28:1_SPACING	*	0.228 MM	?
1.1:1_SPACING	*	0.110 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.230 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.345 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.460 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.575 MM	?
2X_DIELECTRIC	ISL2,ISL13	0.110 MM	?
3X_DIELECTRIC	ISL2,ISL13	0.165 MM	?
4X_DIELECTRIC	ISL2,ISL13	0.220 MM	?
5X_DIELECTRIC	ISL2,ISL13	0.275 MM	?
2X_DIELECTRIC	*	0.120 MM	?
3X_DIELECTRIC	*	0.180 MM	?
4X_DIELECTRIC	*	0.240 MM	?
5X_DIELECTRIC	*	0.300 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V5_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_STATIC		=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_LPC	*	BGA_P1MM	BGA_P2MM
CLK_PCI	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_SLOW	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_50S	BGA_P1MM	STANDARD

M96 RULE DEFINITIONS

SYNC_MASTER=M97 SYNC_DATE=02/04/2008

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SCALE	SHT	OF
NONE	109	109