### NC On Unused Aliases

<table>
<thead>
<tr>
<th>Net Description</th>
<th>Alias</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP_PCIE_CLK100M_PE4P</td>
<td>NC_PCIE_CLK100M_PE4P</td>
</tr>
<tr>
<td>TP_PCIE_CLK100M_PE4N</td>
<td>NC_PCIE_CLK100M_PE4N</td>
</tr>
<tr>
<td>PCIE_EXCARD_PRSNT_L</td>
<td>NC_PCIE_EXCARD_PRSNT_L</td>
</tr>
<tr>
<td>NC_PCIE_CLK100M_PE5P</td>
<td>NC_PCIE_CLK100M_PE5P</td>
</tr>
<tr>
<td>NC_PCIE_CLK100M_PE4N</td>
<td>NC_PCIE_CLK100M_PE4N</td>
</tr>
<tr>
<td>NC_PCIE_CLK100M_EXCARD_P</td>
<td>NC_PCIE_EXCARD_P</td>
</tr>
<tr>
<td>NC_PCIE_EXCARD枘</td>
<td>NC_PCIE_EXCARD枘</td>
</tr>
<tr>
<td>TP_PCI_CLK1</td>
<td>NC_PCI_CLK1</td>
</tr>
<tr>
<td>TP_PCI_C_BE_L&lt;3&gt;</td>
<td>NC_PCI_C_BE_L&lt;3&gt;</td>
</tr>
<tr>
<td>PC_FE4_CLKREQ_L</td>
<td>NC_FE4_CLKREQ_L</td>
</tr>
<tr>
<td>TP_USB_11P</td>
<td>NC_USB_11P</td>
</tr>
<tr>
<td>TP_USB_11N</td>
<td>NC_USB_11N</td>
</tr>
<tr>
<td>TP_USB_10P</td>
<td>NC_USB_10P</td>
</tr>
<tr>
<td>TP_USB_10N</td>
<td>NC_USB_10N</td>
</tr>
<tr>
<td>TP_PCIE_CLK100M_EXCARD_P</td>
<td>NC_PCIE_EXCARD_P</td>
</tr>
<tr>
<td>TP_PCIE_CLK100M_EXCARD_P</td>
<td>NC_PCIE_EXCARD_P</td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td>NO_TEST=TRUE</td>
</tr>
</tbody>
</table>

### Unused Internal USB Ports

<table>
<thead>
<tr>
<th>Net Description</th>
<th>Alias</th>
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<tbody>
<tr>
<td>TP_PCI_AD&lt;8&gt;</td>
<td>NC_PCI_AD&lt;8&gt;</td>
</tr>
<tr>
<td>TP_USB_EXCARD_P</td>
<td>NC_USB_EXCARD_P</td>
</tr>
<tr>
<td>TP_USB_EXCARD_N</td>
<td>NC_USB_EXCARD_N</td>
</tr>
<tr>
<td>TP_PCIE_CLK100M_EXCARD_P</td>
<td>NC_PCIE_EXCARD_P</td>
</tr>
<tr>
<td>MAKE_BASE=TRUE</td>
<td>MAKE_BASE=TRUE</td>
</tr>
<tr>
<td>NO_TEST=TRUE</td>
<td>NO_TEST=TRUE</td>
</tr>
</tbody>
</table>

### Unused Memory Signals

<table>
<thead>
<tr>
<th>Net Description</th>
<th>Alias</th>
</tr>
</thead>
<tbody>
<tr>
<td>TP_PCIE_EXCARD_R2D_C_P</td>
<td>NC_PCIE_EXCARD_R2D_C_P</td>
</tr>
<tr>
<td>TP_VR_PWRGD_CLKEN_L</td>
<td>NC_VR_PWRGD_CLKEN_L</td>
</tr>
<tr>
<td>GALIGN_JTAG_TCK_L</td>
<td>NC_GALIGN_JTAG_TCK_L</td>
</tr>
<tr>
<td>GALIGN_JTAG_TDI</td>
<td>NC_GALIGN_JTAG_TDI</td>
</tr>
<tr>
<td>MEM_B_A&lt;15&gt;</td>
<td>NC_MEM_B_A&lt;15&gt;</td>
</tr>
<tr>
<td>MEM_A_A&lt;15&gt;</td>
<td>NC_MEM_A_A&lt;15&gt;</td>
</tr>
<tr>
<td>USB_TPAD_N</td>
<td>NC_USB_TPAD_N</td>
</tr>
</tbody>
</table>

### Testpoint Alias for Unused Nets

<table>
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<tr>
<td>TP_PCIE_EXCARD_R2D_C_P</td>
<td>NC_PCIE_EXCARD_R2D_C_P</td>
</tr>
<tr>
<td>TP_VR_PWRGD_CLKEN_L</td>
<td>NC_VR_PWRGD_CLKEN_L</td>
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<tr>
<td>GALIGN_JTAG_TCK_L</td>
<td>NC_GALIGN_JTAG_TCK_L</td>
</tr>
<tr>
<td>GALIGN_JTAG_TDI</td>
<td>NC_GALIGN_JTAG_TDI</td>
</tr>
<tr>
<td>MEM_B_A&lt;15&gt;</td>
<td>NC_MEM_B_A&lt;15&gt;</td>
</tr>
<tr>
<td>MEM_A_A&lt;15&gt;</td>
<td>NC_MEM_A_A&lt;15&gt;</td>
</tr>
<tr>
<td>USB_TPAD_N</td>
<td>NC_USB_TPAD_N</td>
</tr>
</tbody>
</table>

### Testpoint for Optional GMUX JTAG from MCP

<table>
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<tbody>
<tr>
<td>GMUX_JTAG_TCK_L</td>
<td>NC_GMUX_JTAG_TCK_L</td>
</tr>
<tr>
<td>GMUX_JTAG_TDI</td>
<td>NC_GMUX_JTAG_TDI</td>
</tr>
<tr>
<td>GMUX_JTAG_TDO</td>
<td>NC_GMUX_JTAG_TDO</td>
</tr>
<tr>
<td>GMUX_JTAG_TMS</td>
<td>NC_GMUX_JTAG_TMS</td>
</tr>
</tbody>
</table>

### Unused Signal Alias/Stand Off

<table>
<thead>
<tr>
<th>Net Description</th>
<th>Alias</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOST_IN</td>
<td>NC_MOST_IN</td>
</tr>
<tr>
<td>SDF0800</td>
<td>NC_SDF0800</td>
</tr>
<tr>
<td>SDF0800</td>
<td>NC_SDF0800</td>
</tr>
<tr>
<td>SDF0800</td>
<td>NC_SDF0800</td>
</tr>
</tbody>
</table>

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**APPEL INC.**

**D**

**911-7175  A**

**051-7973**

**OF 1098**
MCP79-specific pinout

eXtended Debug Port (XDP)

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SYNC_DATE=01/07/2009

DRAWING NUMBER
SHT 13
REV.

eXtended Debug Port (XDP)
In MCP79 these pins have undocumented internal pull-downs (1K or stronger) must be used by default. Pull-down (20k) required in all cases.

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**D**

**MCP Ethernet & Graphics**
Minimum 1.025V for Gen2 support

OUT

IN

45C5

45D5

45C5

45C5

25B2

28C2

28B3

45C3

45C3

45C3

45C3

1/16W

46B3

46B3

46B3

46B3

806

402

1%

47B4

47B4

46D5

8B6

8B6

7B8

8C4

7B8

103C3

103C3

103C3

103C3

103C3

103C3

103C3

103D3

103C3

103C3

103C3

103C3

103C3

103C3

103D3

103C3

103C3

103C3

103C3

103C3

103C3

103C3

103C3

8.2K

5%

8.2K

5%

8.2K

5%

R2050

8.2K

1/16W

5%

R2052

8.2K

1/16W

5%

MF-LF

402

USB_EXTC_OC_L

USB_EXTB_OC_L

USB_EXTA_OC_L

EXCARD_OC_L

=PP3V3_S5_MCP_GPIO

SYNC_DATE=01/07/2009

DRAWING NUMBER

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APPLE INC.
HDA Output Caps

For EMI Reduction on HDA interface

10PF CERM 402 5%

21D3 25A8

For EMI Reduction on HDA interface

8 7 6 5 4 3 2 1

=PP3V3_S0_MCP_HDA

C2171

402

1/16W

R2120

49.9K 1%

1/16W

MF-LF 1/16W

21D4 103B3 7A4 7A4 7A4

100A3 13B6 13C3

49C5 50D3 70A2

98C6 51B1 9A2 9A4

OUT

IN

IN

IN

IN

IN

IN

IN

HDA_RST_R_L

C2173

CERM 402

R2150

2

1

17 mA

MF-LF 1/16W

1/16W

AE17 B19 J18 F19 E20 C20 C16 M22 M24 B20 C18 C19 L13 L26 J14 G15

10K 402 5%

XTALIN

HDA_SDATA_IN0

JTAG_TDI

PWRGD_SB

LLB#

LID#

EXT_SMI/GPIO_32#

RSTBTN#

PWRBTN#

A20GATE

Int PD

Int PD

Int PD

Int PU (S5)

Int PU (S5)

Int PU

Int PU

Int PU (S5)

10K 402 5%

1/16W

10K

5%

MF-LF

1/16W

XTALIN

HDA_SDATA_IN0

JTAG_TDI

PWRGD_SB

LLB#

LID#

EXT_SMI/GPIO_32#

RSTBTN#

PWRBTN#

A20GATE

Int PD

Int PD

Int PD

Int PU (S5)

Int PU (S5)

Int PU

Int PU

Int PU (S5)

10K 402 5%

1/16W

10K

5%

MF-LF

1/16W

XTALIN

HDA_SDATA_IN0

JTAG_TDI

PWRGD_SB

LLB#

LID#

EXT_SMI/GPIO_32#

RSTBTN#

PWRBTN#

A20GATE

Int PD

Int PD

Int PD

Int PU (S5)

Int PU (S5)

Int PU

Int PU

Int PU (S5)
CPU FSB Frequency Straps

NOTE: () values not supported by MCP79.

Merom/Penryn do not officially support PECI, but it's not clear whether PECI interface is present or not. Till used pin F6.

Extra FSB Pull-ups
Exist in SSH but not Intel designs. Here for CYA.

CPU FSB Frequency Straps

Debug: CPU
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e., not simultaneously) due to current limitation of TP51116 regulator.
Caps to couple MCP 1V5_S0_MEM and DIMMS 1V5_S3

Caps to couple MCP 1V5_S0_MEM on DIMM A (further from MCP)

Caps to couple MCP 1V5_S0_MEM on DIMM B (closer to MCP)

Extra decoupling caps for MCP MEM rail

Memory coupling caps
**DDR3 RESET Support**

MCP79 cannot control this signal directly since it must be high in sleep and MEM rails are not powered in sleep.

- **R3310**: 5% 1/16W MF-LF 1K
- **C3300**: CERM 20% 0.1UF MEM_RESET_HW
- **R3300**: 10K 5% 1/16W MF-LF
- **R3309**: 5% 1/16W MF-LF
- **R3305**: 20K 5% 1/16W MF-LF
- **R3301**: 20K 5% 1/16W MF-LF
- **Q3305**: MMDT3904-X-G MEMRESET_HW SOT-363-LF

**Notes:**
- 3.3V input must be stable before 1.5V starts to rise to avoid glitch on MEM_RESET_L.
- DDR3 RESET Support
- SYNC_DATE=01/07/2009
- SYNC_MASTER=K50
- DDR3 Support
- 6D3 = PP1V5_S3_MEMRESET
- 6D1 = PP3V3_S5_MEMRESET
- MC13232 32C2
NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

NOTE: NOT USING THE BUILT-IN 1.05V REGULATOR OF THE PHY.

ENET ALIASES
MCP_CLK25M_BUF0_R = RBL8211_CLK25M_CKXTAL1
PP1V05_RMGT = PP1V05_ENET_MCP_PLL_MAC
PP3V3_RMGT = PP3V3_ENET_MCP_RMGT
PP3V3_ENET_PHY_VDDREG = RTL8211_REGOUT
PP1V05_ENET_PHY = PP1V05_ENET_PHY
PP3V3_ENET_PHY = PP3V3_ENET_PHY
MCP79_ENET_ALIASES

3.3V ENET FET
I(MAX)  = 1.7A (85C)
@ 2.5V VGS:
RDS(ON) = 47MOHM MAX
I(MAX)  = 4.1A
@ 1.8V VGS:

1.05V ENET FET

RTL8211 25MHz Clock

SOURCE SELECT
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NOTE: Q4200 COLLECTOR CONNECT TO CAPS WITH 0.4 SQ-IN HEAT SINK

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED. NO STUFF MEANS THAT IT IS IN BILINGUAL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643

NOTE: MULTIPLE VIAS TO DGND
MCP79 Rev A01 requires external MUX, Rev B01 should support internal MUX.
**1.5V S0 CURRENT SENSE**

- **US400**
- **C5400**

**MCP CORE CURRENT SENSE**

- **R5400**
- **C5401**
- **C5402**
- **C5403**

**MCP CORE VOLTAGE SENSE**

- **R5401**
- **R5402**
- **R5403**
- **R5404**

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Revision: A

Drawing Number: SHT 051-7973 A

Size: 10/4

Table 5:

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Apple Inc.
NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.

SST25VF016B max speed for READ command is 25MHz.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>42 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>25 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE: 87654321D is used for SPI command in 2MBs.

R6100, R6101: 402, 3.3K, MF-LF, 5%, 1/16W
R6105, R6152: PLACEMENT_NOTE=PLACE CLOSE TO U6100
R6150, R6190, R6191: PLACEMENT_NOTE=PLACE CLOSE TO U6100
C6100, C6102: 0.1UF, 10V

MCP79 SPI Frequency Select

PLACEMENT_NOTE=PLACE CLOSE TO U6100

SYNCHRONIZATION

SYNC_MASTER=K50
SYNC_DATE=01/07/2009
=PP3V3_S5_ROM

APPLE INC.

REV. A

A051-7973 651-7975 A
**S0 POWER RAIL SEQUENCING**

- CPU_VCORE
- VTT_S0_DDR_LDO

**S3 POWER RAIL SEQUENCING**

- MCP_VCORE
- SB: PM_SLP_S3_L
- SB: PM_SLP_S4_L

**RMGT POWER RAIL SEQUENCING**

- 3V3_RMGT
- 1V05_RMGT

**SHUT DOWN (SHUTDOWN OR SLEEP) TIMING**

- CPU_PWRGD DISABLED
- SUSPEND SOON
- SB SAYS PWROK DISABLE
- SB SAYS CLK GEN DISABLED

**POWER SEQUENCING BLOCK DIAGRAM**

- SMC_PM_G2_ENABLE
- SMC_STARTS
- SMC: IMVP_VR_ON
- SB: PM_SLP_M_L
- SB: PM_SUS_STAT#
- SB: PM_SLP_S3_L
- SB: PM_SLP_S4_L

**NOTE:**

- NO SEQUENCING REQUIREMENTS FOR THESE 3 RAILS
- 3V3_S0 FET GATED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG; RC SOFT TURN-ON CIRCUIT; SLOWER THAN 5V_S0
- 1V8_S0 LDO SOURCED FROM 5V_S0, ENABLED BY 5V_S0 WITH RC DELAY
- 12V_S0 SUPPLIED BY AC/DC, GATED BY PM_SLP_S3_L
- MCP_VCORE REGULATOR INTERNAL LOGIC POWERED FROM 5V_S3, SOURCED FROM 12V_S5,
  ENABLED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG WITH RC DELAY
- 1V05_S0 REGULATOR SHARES INTERNAL LOGIC POWER WITH 3V3_S5 REG, SOURCED FROM 12V_S0
- 5V_S0 FET GATED BY PM_SLP_S3_L*12VS0_PG*1V5_S3_PG; RC SOFT TURN-ON CIRCUIT
- 1V05_S5 SWITCHER SOURCED FROM 3V3_S5 AND ENABLED FROM 3V3_S5_PGOOD
- 12V_S5 SUPPLIED BY AC/DC MAX RAMP TIME < 50MS MAX RAMP RATE 10V/MS
- SOURCED BY 12V_S5; MUST RAMP IN < 2MS
- 5V_S3 SWITCHER LOGIC POWERED BY INTERNAL LDO (EN BY SLP_S4_L)
- OUTPUT SOURCED FROM 12V_S5 AND ENABLED BY PM_SLP_S4_L + LDO OUTPUT GOOD
- 1V5_S3 SWITCHER POWERED BY 5V_S3 SO ENABLED BY PGOOD_5V_S3
- 3V3_S3 FET GATED BY PM_SLP_S4_L

**SHUTDOWN (BOOT OR WAKE) TIMING**

- SLEEP OR SHUTDOWN
- SHUTDOWN CPU IN RESPONSE TO SMC SAYS SHUTDOWN CPU
- POWER RAILS ON DURING THIS TIME

**STARTUP (BOOT OR WAKE) TIMING**

- CPU_PWRGD DISABLED
- SLEEP OR SHUTDOWN
- CPU_VCORE OFF
EN_LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN (1.05_S0), IS TIED TO VCC, FED INTERNALLY TO FET 3965-10A-13.6MOHM AS SOON AS LDO OUTPUT IS 3.3V.
EN1 (1.05_S0) CONTROLLED SEPARATELY

INPUT POWER OF 12V_S5

INPUT POWER OF 12V_S0

EN LDO ASAP

INPUT POWER OF 12V_S5
MCP 1.05V_S5 AUXC SUPPLY

\[ V_{OUT} = 0.6V \times \left(1 + \frac{R_a}{R_b}\right) \]
MCP ONLY 1.8V_S0 POWER SUPPLY

VOUT = 0.5 * (1 + RA/RB)

MAX CURRENT = 300MA
VOUT = 1.8V

SYNC_MASTER=K50
SYNC_DATE=01/07/2009

SYNC_DATE=01/07/2009

1V8 POWER SUPPLY

MIN_NECK_WIDTH=0.1MM
SWITCHNODEMIN_LINE_WIDTH=0.3MM
Unused DP Interfaces

Unused DP Interfaces

Unused DP Interfaces
PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR
**Memory Bus Constraints**

- All memory signals maximum length is 1.005 ps.
- CLK minimum length is 594 ps (lengths include substrate).

**MCP MEM COMP Signal Constraints**

- DDR3:
- DDR2:

**Memory Bus Spacing Group Assignments**

- Source: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3

**Memory Net Properties**

- Table of Memory Net Properties
- Table of Memory Net Properties
- Table of Memory Net Properties

**MCP MEM COMP Signal Constraints**

- Table of MCP MEM COMP Signal Constraints
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# SMBus Interface Constraints

<table>
<thead>
<tr>
<th>SMC SMBus Net Properties</th>
<th>Min Width</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
<td>550 mm</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
<td>550 mm</td>
</tr>
<tr>
<td>SMBUS_MCP_0_CLK</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
<td>550 mm</td>
</tr>
<tr>
<td>SMBUS_MCP_0_DATA</td>
<td>0.1 mm</td>
<td>0.1 mm</td>
<td>550 mm</td>
</tr>
</tbody>
</table>

### SMBus Interface Constraints

- SMBUS_SMC_B_S0_SCL: 0.1 mm minimum width, 0.1 mm minimum neck width, 550 mm maximum neck length.
- SMBUS_SMC_B_S0_SDA: 0.1 mm minimum width, 0.1 mm minimum neck width, 550 mm maximum neck length.
- SMBUS_MCP_0_CLK: 0.1 mm minimum width, 0.1 mm minimum neck width, 550 mm maximum neck length.
- SMBUS_MCP_0_DATA: 0.1 mm minimum width, 0.1 mm minimum neck width, 550 mm maximum neck length.
Digital Video Signal Constraints

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
### SPACING RULE SET

#### NET_SPACING_TYPE1
- NET_PHYSICAL_TYPE
- MCP_USB_RBIAS
- MCP_MEM_COMP
- PPDDR_MEM
- MCP_DV_COMP
- CLK_PCIE
- MEM_CTRL

### AREA_TYPE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE

### TABLE_PHYSICAL_ASSIGNMENT_HEAD
- MINIMUM LINE WIDTH
- SPACING_RULE_SET
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM

### TABLE_SPACING_ASSIGNMENT_ITEM
- GND_P2MM
- GND_P2MM
- PWR_P2MM
- GND_P2MM
- MEM_DATA

### TABLE_SPACING_RULE_ASSIGNMENT_ITEM
- CPU_VCCSENSE
- CPU_GTLREF
- CPU_COMP

### PP1V5_S3_MEM_B
- 5VS3_SW
- IMVP6_PHASE3
- IMVP6_PHASE1
- =PP1V5_S3_MEM_B

### 1V05S5_SW
- 6D3
- 74C5
- 79C5
- 80C5
- 72C6 72A7
- 76C3
- 76C6
- 75B6
- 75C6
- 75B7
- 75D7
- 75C7
- 54D6
- 53B3 53C4
- 55B3
- 55A8 55B6 55B8
- 10C6 55D4
- 55B6
- 55C6
- 55D6
- 54D6
- 53B3 53B4
- 21C3 55C4
- 55A8 55B6 55B8

### THERMAL
- THERM_DIFF

### TABLE_PHYSICAL_RULE_ITEM
- SIZE
- NONE

### SYNC_MASTER=K50
- K50/K51 SPECIFIC CONSTRAINTS

### SYNC_DATE=01/07/2009
- NOTICE OF PROPRIETARY PROPERTY
- APPLE INC.

### Table 1

<table>
<thead>
<tr>
<th>NET</th>
<th>LOWER NODE</th>
<th>UPPER NODE</th>
<th>LOWER WIDTH</th>
<th>UPPER WIDTH</th>
<th>LOWER HT</th>
<th>UPPER HT</th>
<th>LOWER HT_MIN</th>
<th>UPPER HT_MIN</th>
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</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

### K50/K51 SPECIFIC NET PROPERTIES

- CPU_THERMD_P
- SNS_T_DN4_DP5
- SNS_T_DP4_DN5
- SNS_CPU_H_N
- SNS_CPU_H_P

### Footnotes:
- To view the full document, please visit the official Apple Inc. website.
## K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

### PHYSICAL CONSTRAINTS

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Top, Bottom</th>
<th>Layer</th>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>NECK WIDTH</td>
<td>Top, Bottom</td>
<td>Layer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NECK LENGTH</td>
<td>Top, Bottom</td>
<td>Layer</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PRIMARY GAP</td>
<td></td>
<td>Layer</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### CONSTRAINTS FOR BGA AREA

<table>
<thead>
<tr>
<th>Constraint</th>
<th>BGA Type</th>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1MM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P2MM</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P3MM</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SPACING RULE SET

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Width</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINIMUM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MAXIMUM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**Constraints are based on M579 design guide D0-03226-001_V04.**

PC1, LPC, USB, RCA, SPI, SMI, SMDI, SMDO are routed as 55 GNM SE signals.