

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

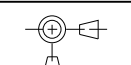
REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
A		676436	PRODUCTION RELEASED	DATE	DATE
				02/26/09	?

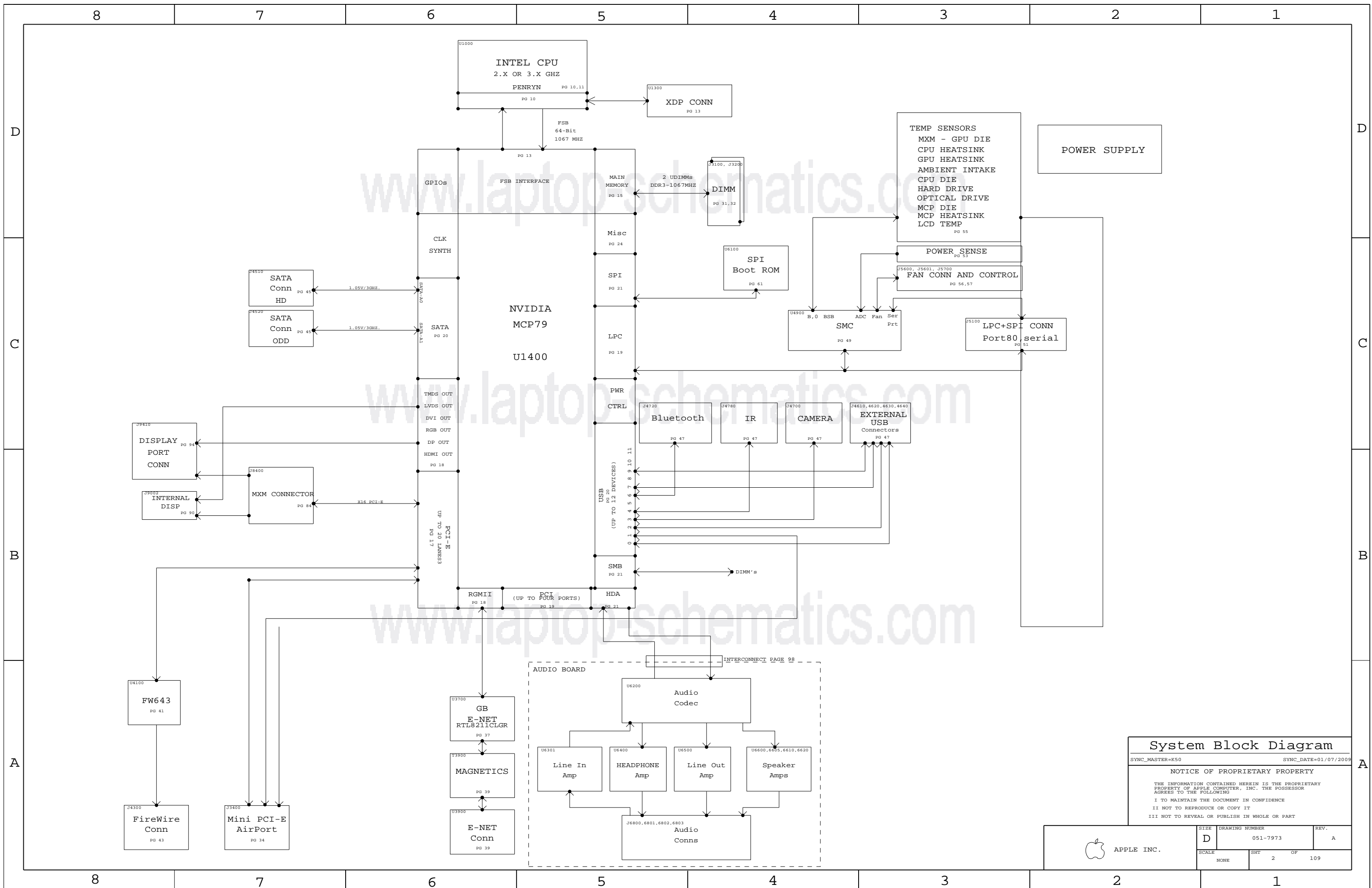
SCHEMATIC, GINSU (K51A)

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DRAWING
TITLE=K51
ABBREV=DRAWING
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DIMENSIONS ARE IN MILLIMETERS		METRIC		APPLE INC.	
XX :	_____	DRAPTR	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX :	_____	ENG APPD	MFG APPD		
X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
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				SHEET 1 OF 109	



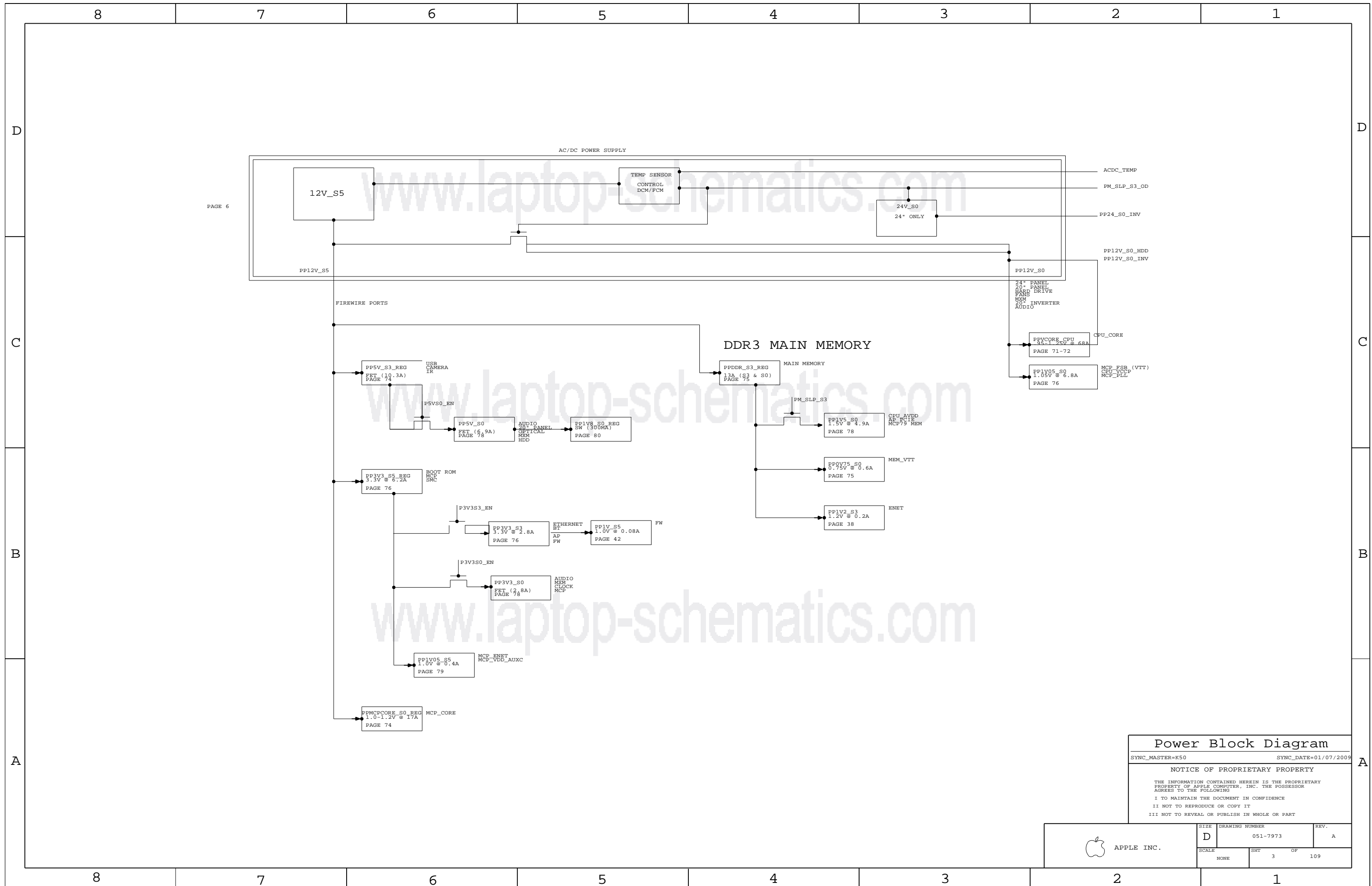
System Block Diagram

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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	SCALE NONE	SHEET 2	OF 109



Power Block Diagram

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	3		

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0018	PCBA,MLB,K51A,BETTER,RENESAS FET	24_INCH_LCD,2P66GHZ_CPU,BASIC,IG,RENESAS_FET
639-0019	PCBA,MLB,K51A,BEST,RENESAS FET	24_INCH_LCD,2P93GHZ_CPU,BASIC,MXM,MXM_PWR_SENSE,12V_PWR_SENSE,24_INCH_MXM,RENESAS_FET
639-0020	PCBA,MLB,K51A,CTO_ULT,RENESAS FET	24_INCH_LCD,3P06GHZ_CPU,BASIC,MXM,MXM_PWR_SENSE,12V_PWR_SENSE,24_INCH_MXM,RENESAS_FET
607-4702	K51A MLB DEVELOPMENT	DEVELOPMENT_XDP_CONN,LPCPLUS,VREFMRGN,MCP_PWR_SENSE

BOM NUMBER	BOM NAME	BOM OPTIONS
639-0015	PCBA,MLB,K51A,BETTER,TOSHIBA FET	24_INCH_LCD,2P66GHZ_CPU,BASIC,IG,TOSHIBA_FET
639-0016	PCBA,MLB,K51A,BEST,TOSHIBA FET	24_INCH_LCD,2P93GHZ_CPU,BASIC,MXM,MXM_PWR_SENSE,12V_PWR_SENSE,24_INCH_MXM,TOSHIBA_FET
639-0017	PCBA,MLB,K51A,CTO_ULT,TOSHIBA FET	24_INCH_LCD,3P06GHZ_CPU,BASIC,MXM,MXM_PWR_SENSE,12V_PWR_SENSE,24_INCH_MXM,TOSHIBA_FET

COMMON (DELETED HDCP ROM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0636	1	IC,ONCP,MCP79-B02,35X35MM, BGA1437, DT	U1400	CRITICAL	MCP_B02
338S0654	1	IC,FW643-06,1394B, REV-E	U4100	CRITICAL	
820-2404	1	PCB,FAB,IO ALIGNMENT,K50/K51	IO1	CRITICAL	
825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
341T0174	1	EFI ROM,K50A/K51A/K50E	U6100	CRITICAL	
511S0038	1	CONN,INTEL SKT-P, BGA,26X26-479	U1000	CRITICAL	
338S0570	1	IC,RTL8211CL,GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	

K51A PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7973	1	PCB,SCHEM,MLB,K51A	SCH1		24_INCH_LCD
820-2491	1	PCB,FAB,MLB,K51,HF	MLB1		24_INCH_LCD
341T0177	1	IC,SMC,K51A	U4900	CRITICAL	24_INCH_LCD
114S0308	1	RES,8.45K,0402,1%,1/16W,LF	R7117		24_INCH_LCD
132S0010	1	CAP,CER,390PF,10%,50V,0402	C7113		24_INCH_LCD
132S0178	1	CAP,CER,0.47UF,10%,6.3V,0402	C7128		24_INCH_LCD
132S0082	1	CAP,CER,0.068UF,10%,10V,0402	C7134		24_INCH_LCD

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,MCP_TDIODE,MCP79,CPUV_PHASE3,XDP,CPU_TDIODE,MCP_B02,PRODUCTION
MCP79	BOOT_MODE_USER,MEMRESET_HW,MEMRESET_MCP

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3705	1	IC,PRO,FDC,SLGRD,2.66,55W,1066,80,6M,PGA	CPU	CRITICAL	2P66GHZ_CPU
337S3706	1	IC,PRO,FDC,SLGRB,2.93,55W,1066,80,6M,PGA	CPU	CRITICAL	2P93GHZ_CPU
337S3707	1	IC,PRO,FDC,SLGEA,3.06,55W,1066,80,6M,PGA	CPU	CRITICAL	3P06GHZ_CPU

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

ALTERNATES

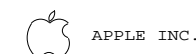
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152-0104	152-0099		L7100,L7101,L7200	MSQ-1211-R36L-F
152-0105	152-0101		L7530	MSQ-1211-1R5L-F
338S0694	338S0570		U3700	RTL8211CL/RTL8251CA
104S0018	101S0414		R5400	USE 20MOHM AS OR

BOM Configuration

SYNC_MASTER=K50A SYNC_DATE=01/13/2009

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SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	4	109

"S0" RAILS

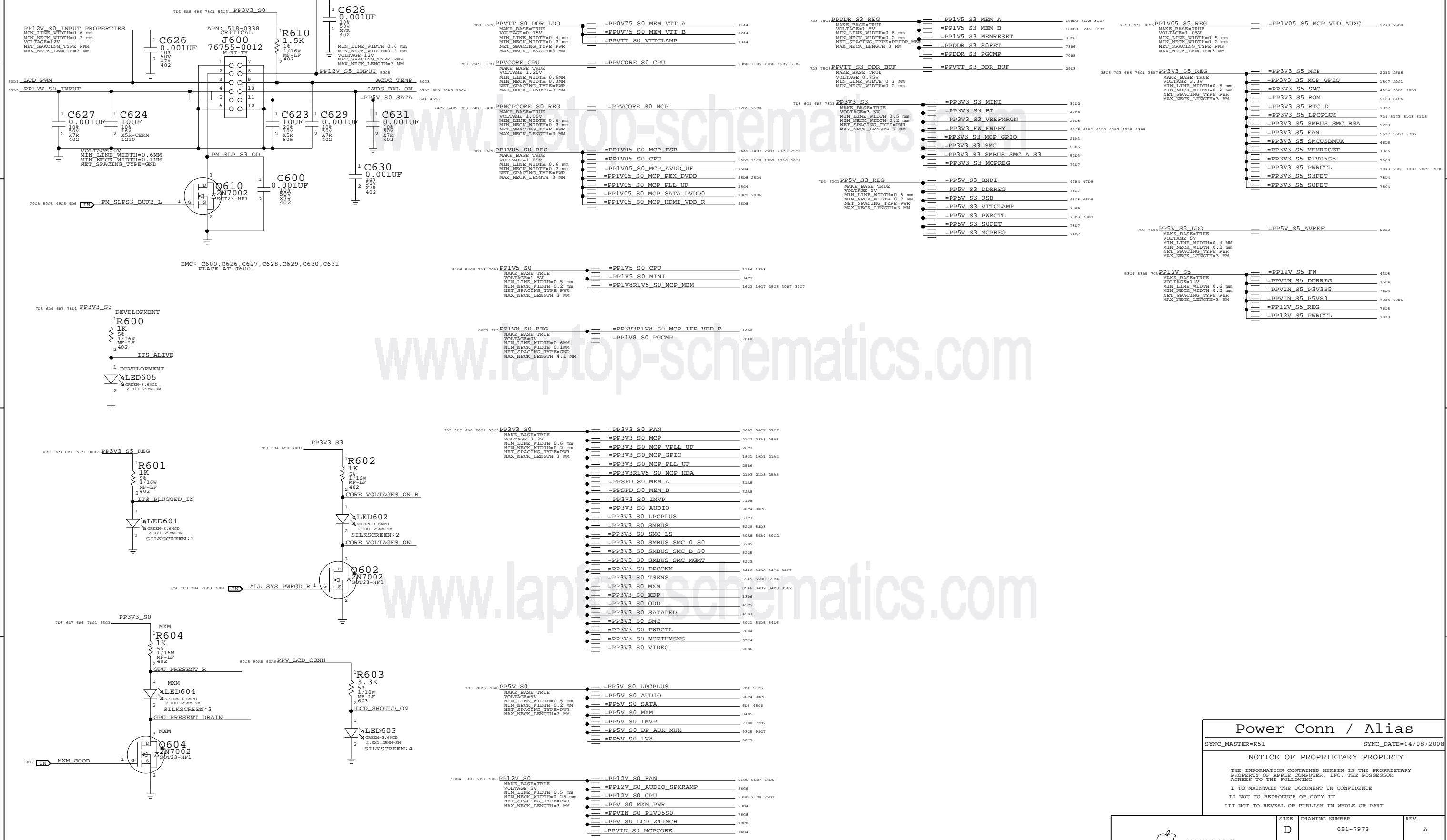
ONLY ON IN RUN

"S3" RAILS

ON IN RUN AND SLEEP

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



EMC: C600,C626,C627,C628,C629,C630,C631 PLACE AT J600.

Power Conn / Alias

SYNC_MASTER=K51 SYNC_DATE=04/08/2008

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

LAYOUT NOTE: PLACE NEAR J1000

LAYOUT NOTE: PLACE NEAR U1400

LAYOUT NOTE: PLACE NEAR U3700

LPC CONNECTOR

S0 RAILS

MISC GROUND VIAS

Table of test points for J1000 including FSB A L<6>, FSB ADSTB L<0>, FSB A L<27>, FSB ADSTB L<1>, FSB D L<0>, FSB DSTB L P<0>, FSB DINV L<0>, FSB D L<16>, FSB DSTB L P<1>, FSB D L<41>, FSB DSTB L N<2>, FSB DINV L<2>, FSB D L<59>, FSB DSTB L N<3>, FSB DINV L<3>, CPU INIT L, CPU AZOM L, CPU IGNNR L, CPU STCLK L, CPU INTR, CPU NMI, CPU SMI L, FSB REQ L<0>, FSB REQ L<1>, FSB REQ L<2>, FSB REQ L<3>, FSB REQ L<4>, FSB CLK CPU P, FSB CLK CPU N.

Table of test points for U1400 including FSB A L<6>, FSB ADSTB L<0>, FSB A L<27>, FSB ADSTB L<1>, FSB D L<0>, FSB DSTB L P<0>, FSB DINV L<0>, FSB D L<16>, FSB DSTB L P<1>, FSB D L<41>, FSB DSTB L N<2>, FSB DINV L<2>, FSB D L<59>, FSB DSTB L N<3>, FSB DINV L<3>, FSB LOCK L, FSB HIT L, FSB HITM L, FSB BNR L, FSB BREO L, FSB DBSY L, FSB DPWR L, FSB REQ L<0>, FSB REQ L<1>, FSB REQ L<2>, FSB REQ L<3>, FSB REQ L<4>, VR PWGOOD DELAY.

Table of test points for U3700 including ENET RESET L.

LAYOUT NOTE: PLACE NEAR U4100

Table of test points for U4100 including PCIE CLK100M FW P, PCIE CLK100M FW N, PCIE FW R2D P, PCIE FW R2D N, FW RESET L.

LAYOUT NOTE: PLACE NEAR U4900

Table of test points for U4900 including SMC LRESET L, SMC RESET L, SMC AD<1>, SMC LOCK L, SMC HIT L, SMC HITM L, SMC BNR L, SMC BREO L, SMC DBSY L, SMC DPWR L, SMC REQ L<0>, SMC REQ L<1>, SMC REQ L<2>, SMC REQ L<3>, SMC REQ L<4>, VR PWGOOD DELAY.

Table of test points for LPC CONNECTOR including PP3V3 S5 LPCPLUS, PP5V S0 LPCPLUS, LPC CLK33M LPCPLUS, LPC AD<0>, LPC AD<1>, LPC AD<2>, LPC AD<3>, LPC FRAME L, PM CLKRUN L, SMC TMS, DEBUG RESET L, SMC TRST L, SMC TDO, SMC MD1, SMC TX L, SMC SERIO, SMC TDI, SMC TCK, SMC RESET L, SMC NMI, SMC RX L, LPC PWRDWN L, LPCPLUS GPIO, SPI ALT CLK, SPI ALT CS L, SPI ALT MOSI, SPI ALT MISO, SPROM USE MLB, GND 16 TP'S.

Table of test points for *S0* RAILS including PPVTT S0 DDR LDO, PPVCORE CPU, PPMCCORE S0 REG, PPIV05 S0 REG, PPIV8 S0, PPIV8 S0 REG.

S3 RAILS

Table of test points for *S3* RAILS including PPDDR S3 REG, PPVTT S3 DDR BUF, PP3V3 S3, PP5V S3 REG.

S5 RAILS

Table of test points for *S5* RAILS including PPIV05 S5 REG, PP3V3 S5 REG, PP5V S5 LDO, PPI2V S5.

Table of test points for PM SYSRST L, SMC MANUAL RST L, ALL SYS PWGRD R.

PWR0K SEQUENCING

Table of test points for ALL SYS PWGRD R.

STARTUP (BOOT/WAKE) TIMING

Table of test points for IMVP VR_ON, VR PWGOOD DELAY.

SHUTDOWN/SLEEP TIMING

Table of test points for PM SLP S3 L, PM SLP S4 L, ALL SYS PWGRD R, CPU PWGRD.

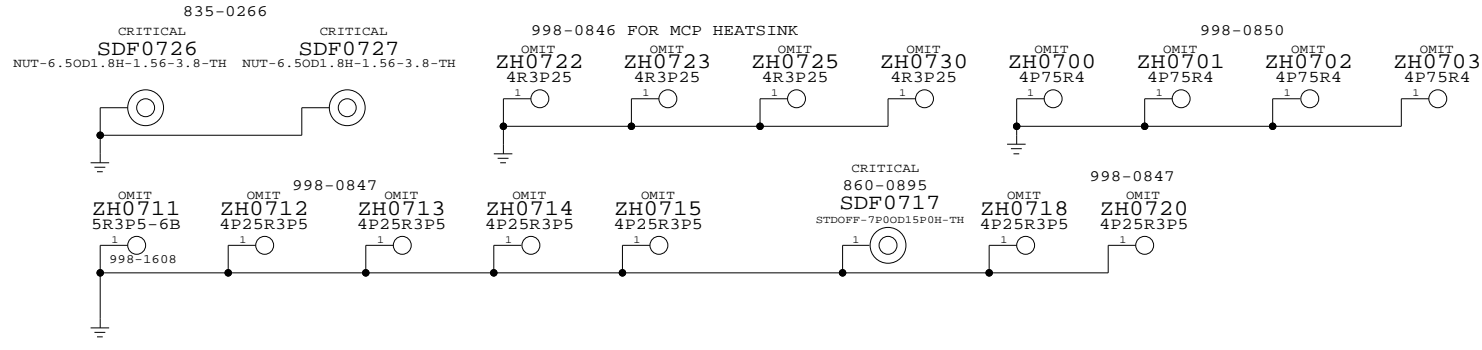
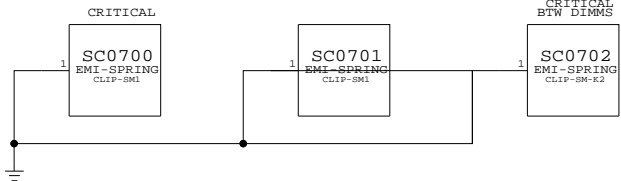
XDP CONNECTOR

Table of test points for XDP BPM L<5..0>, TP XDP OBSFN B0, TP XDP OBSFN B1, TP XDP OBSDATA B0, TP XDP OBSDATA B1, TP XDP OBSDATA B2, TP XDP OBSDATA B3, XDP PWGRD, PM LATRIGGER L, SMBUS MCP 0 DATA, SMBUS MCP 0 CLK, MCP DEBUG<0..7>, FSB CLK ITP P, FSB CLK ITP N, XDP CPURST L, XDP DBRESET L, XDP TRST L, XDP TDI, XDP TMS, XDP TDO, XDP TCK, JTAG MCP TDI, JTAG MCP TMS, JTAG MCP TCK, JTAG MCP TDO, JTAG MCP TRST L.

LAYOUT NOTE: PLACE NEAR U1400

Table of test points for U1400 including PCIE MINI D2R P, PCIE MINI D2R N, PCIE FW D2R P, PCIE FW D2R N, PM SYSRST L, PM CLKRUN L, SATA ODD D2R P, SATA ODD D2R N, SATA HDD D2R P, SATA HDD D2R N, LPC AD<1>, USB CAMERA P, USB CAMERA N, USB BT P, USB BT N, SPI CLK R, SPI MISO.

Table of test points for U1400 including MEM A DQ<7>, MEM A DQ<14>, MEM A DQ<16>, MEM A DQ<25>, MEM A DQ<47>, MEM A DQ<59>, MEM A DQS P<1>, MEM A DQS P<2>, MEM A DQS P<3>, MEM A DQS P<4>, MEM A DQS P<5>, MEM A DQS N<6>, MEM B DQ<6>, MEM B DQ<8>, MEM B DQ<23>, MEM B DQ<25>, MEM B DQ<38>, MEM B DQ<62>, MEM B DQS P<2>, MEM B DQS N<3>, MEM B DQS N<4>, MEM B DQS P<5>, MEM B DQS N<5>, MEM B DQS P<6>, MEM B DQS N<7>, PEG D2R P<7>, PEG D2R N<7>.



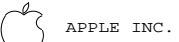
Functional / ICT Test

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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Table with columns: SIZE (D), DRAWING NUMBER (051-7973), REV. (A), SCALE (NONE), SHEET (7 OF 109).



NC ON UNUSED ALIASES

TESTPOINT ALIAS FOR UNUSED NETS

1806	MCP_TV_DAC_RSET	==	NC_MCP_TV_DAC_RSET	NO_TEST=TRUE
1806	MCP_TV_DAC_VREF	==	NC_MCP_TV_DAC_VREF	NO_TEST=TRUE
1806	MCP_CLK27M_XTALIN	==	NC_MCP_CLK27M_XTALIN	NO_TEST=TRUE
1806	MCP_CLK27M_XTALOUT	==	NC_MCP_CLK27M_XTALOUT	NO_TEST=TRUE
1803	CRT_IG_R_C_PR	==	NC_CRT_IG_R_C_PR	NO_TEST=TRUE
1803	CRT_IG_G_Y_Y	==	NC_CRT_IG_G_Y_Y	NO_TEST=TRUE
1803	CRT_IG_B_COMP_PB	==	NC_CRT_IG_B_COMP_PB	NO_TEST=TRUE
1803	CRT_IG_HSYNC	==	NC_CRT_IG_HSYNC	NO_TEST=TRUE
1803	CRT_IG_VSYNC	==	NC_CRT_IG_VSYNC	NO_TEST=TRUE
1803	TP_MCP_RGB_HSYNC	==	NC_MCP_RGB_HSYNC	NO_TEST=TRUE
1803	TP_MCP_RGB_VSYNC	==	NC_MCP_RGB_VSYNC	NO_TEST=TRUE
1907	TP_PCI_AD<31..15>	==	NC_PCI_AD<31..15>	NO_TEST=TRUE
1904	TP_PCI_IRDY_L	==	NC_PCI_IRDY_L	NO_TEST=TRUE
1904	TP_PCI_C_BE_L<1..0>	==	NC_PCI_C_BE_L<1..0>	NO_TEST=TRUE
1904	TP_PCI_SERR_L	==	NC_PCI_SERR_L	NO_TEST=TRUE
1904	TP_PCI_DEVSEL_L	==	NC_PCI_DEVSEL_L	NO_TEST=TRUE
1904	TP_PCI_PERR_L	==	NC_PCI_PERR_L	NO_TEST=TRUE
1904	TP_LPC_DRO0_L	==	NC_LPC_DRO0_L	NO_TEST=TRUE
2103	TP_MCP_BUF_SIO_CLK	==	NC_MCP_BUF_SIO_CLK	NO_TEST=TRUE
1606	TP_MEM_A_ODT<3..2>	==	NC_MEM_A_ODT<3..2>	NO_TEST=TRUE
1606	TP_MEM_A_CKE<3..2>	==	NC_MEM_A_CKE<3..2>	NO_TEST=TRUE
1606	TP_MEM_A_CS_L<3..2>	==	NC_MEM_A_CS_L<3..2>	NO_TEST=TRUE
1585	TP_MEM_A_CLK2P	==	NC_MEM_A_CLK2P	NO_TEST=TRUE
1585	TP_MEM_A_CLK2N	==	NC_MEM_A_CLK2N	NO_TEST=TRUE
1606	TP_MEM_A_CLK3P	==	NC_MEM_A_CLK3P	NO_TEST=TRUE
1606	TP_MEM_A_CLK3N	==	NC_MEM_A_CLK3N	NO_TEST=TRUE
1606	TP_MEM_A_CLK4P	==	NC_MEM_A_CLK4P	NO_TEST=TRUE
1606	TP_MEM_A_CLK4N	==	NC_MEM_A_CLK4N	NO_TEST=TRUE
1606	TP_MEM_A_CLK5P	==	NC_MEM_A_CLK5P	NO_TEST=TRUE
1606	TP_MEM_A_CLK5N	==	NC_MEM_A_CLK5N	NO_TEST=TRUE
1603	TP_MEM_B_CS_L<3..2>	==	NC_MEM_B_CS_L<3..2>	NO_TEST=TRUE
1603	TP_MEM_B_ODT<3..2>	==	NC_MEM_B_ODT<3..2>	NO_TEST=TRUE
1603	TP_MEM_B_CKE<3..2>	==	NC_MEM_B_CKE<3..2>	NO_TEST=TRUE
1581	TP_MEM_B_CLK2P	==	NC_MEM_B_CLK2P	NO_TEST=TRUE
1581	TP_MEM_B_CLK2N	==	NC_MEM_B_CLK2N	NO_TEST=TRUE
1603	TP_MEM_B_CLK3P	==	NC_MEM_B_CLK3P	NO_TEST=TRUE
1603	TP_MEM_B_CLK3N	==	NC_MEM_B_CLK3N	NO_TEST=TRUE
1603	TP_MEM_B_CLK4P	==	NC_MEM_B_CLK4P	NO_TEST=TRUE
1603	TP_MEM_B_CLK4N	==	NC_MEM_B_CLK4N	NO_TEST=TRUE
1603	TP_MEM_B_CLK5P	==	NC_MEM_B_CLK5P	NO_TEST=TRUE
1603	TP_MEM_B_CLK5N	==	NC_MEM_B_CLK5N	NO_TEST=TRUE

1806	TP_ENET_INTR_L	==	NC_ENET_INTR_L	NO_TEST=TRUE
1803	TP_ENET_PWDWN_L	==	NC_ENET_PWDWN_L	NO_TEST=TRUE
2107	TP_MCP_KBDRSTIN_L	==	NC_MCP_KBDRSTIN_L	NO_TEST=TRUE
1786	TP_MCP_GPIO_18	==	NC_MCP_GPIO_18	NO_TEST=TRUE
2107	TP_MLB_RAM_SIZE	==	NC_MLB_RAM_SIZE	NO_TEST=TRUE
1904	TP_PCI_C_BE_L<3>	==	NC_PCI_C_BE_L<3>	NO_TEST=TRUE
1904	TP_PCI_CLK0	==	NC_PCI_CLK0	NO_TEST=TRUE
1904	TP_PCI_CLK1	==	NC_PCI_CLK1	NO_TEST=TRUE
1904	TP_PCI_FRAME_L	==	NC_PCI_FRAME_L	NO_TEST=TRUE
1904	TP_PCI_GNT0_L	==	NC_MCP_PCI_GNT0_L	NO_TEST=TRUE
1904	TP_PCI_GNT1_L	==	NC_PCI_GNT1_L	NO_TEST=TRUE
1907	TP_PCI_INTW_L	==	NC_PCI_INTW_L	NO_TEST=TRUE
1907	TP_PCI_INTX_L	==	NC_PCI_INTX_L	NO_TEST=TRUE
1907	TP_PCI_INTY_L	==	NC_PCI_INTY_L	NO_TEST=TRUE
1907	TP_PCI_INTZ_L	==	NC_PCI_INTZ_L	NO_TEST=TRUE
1904	TP_PCI_PAR	==	NC_PCI_PAR	NO_TEST=TRUE
1904	TP_PCI_RESET1_L	==	NC_PCI_RESET1_L	NO_TEST=TRUE
1904	TP_PCI_STOP_L	==	NC_PCI_STOP_L	NO_TEST=TRUE
1907	TP_PCI_TRDY_L	==	NC_PCI_TRDY_L	NO_TEST=TRUE
1703	TP_PCIE_CLK100M_PE4N	==	NC_PCIE_CLK100M_PE4N	NO_TEST=TRUE
1703	TP_PCIE_CLK100M_PE4P	==	NC_PCIE_CLK100M_PE4P	NO_TEST=TRUE
1781	TP_PCIE_CLK100M_PE5N	==	NC_PCIE_CLK100M_PE5N	NO_TEST=TRUE
1781	TP_PCIE_CLK100M_PE5P	==	NC_PCIE_CLK100M_PE5P	NO_TEST=TRUE
1781	TP_PCIE_CLK100M_PE6P	==	NC_PCIE_CLK100M_PE6P	NO_TEST=TRUE
1704	PCIE_EXCARD_PRSENT_L	==	NC_PCIE_EXCARD_PRSENT_L	NO_TEST=TRUE
1706	TP_PE4_CLKREQ_L	==	NC_PE4_CLKREQ_L	NO_TEST=TRUE
1706	TP_PE4_PRSENT_L	==	NC_PE4_PRSENT_L	NO_TEST=TRUE
2107	TP_SB_A20GATE	==	NC_SB_A20GATE	NO_TEST=TRUE
2003	TP_USB_10N	==	NC_USB_10N	NO_TEST=TRUE
2003	TP_USB_10P	==	NC_USB_10P	NO_TEST=TRUE
2003	TP_USB_11N	==	NC_USB_11N	NO_TEST=TRUE
2003	TP_USB_11P	==	NC_USB_11P	NO_TEST=TRUE
2003	USB_EXCARD_N	==	NC_USB_EXCARD_N	NO_TEST=TRUE
2003	USB_EXCARD_P	==	NC_USB_EXCARD_P	NO_TEST=TRUE
2103	ODD_PWR_EN_L	==	NC_ODD_PWR_EN_L	NO_TEST=TRUE
1703	PCIE_CLK100M_EXCARD_P	==	NC_PCIE_CLK100M_EXCARD_P	NO_TEST=TRUE
1703	PCIE_CLK100M_EXCARD_N	==	NC_PCIE_CLK100M_EXCARD_N	NO_TEST=TRUE
1706	EXCARD_CLKREQ_L	==	NC_EXCARD_CLKREQ_L	NO_TEST=TRUE
1907	TP_PCI_AD<12..10>	==	NC_PCI_AD<12..10>	NO_TEST=TRUE
1907	TP_PCI_AD<8>	==	NC_PCI_AD<8>	NO_TEST=TRUE

1786	PCIE_EXCARD_D2R_P	==	TP_PCIE_EXCARD_D2R_P	NO_TEST=TRUE
1786	PCIE_EXCARD_D2R_N	==	TP_PCIE_EXCARD_D2R_N	NO_TEST=TRUE
1783	PCIE_EXCARD_R2D_C_P	==	TP_PCIE_EXCARD_R2D_C_P	NO_TEST=TRUE
1783	PCIE_EXCARD_R2D_C_N	==	TP_PCIE_EXCARD_R2D_C_N	NO_TEST=TRUE
7107	VR_PWRGD_CLKEN_L	==	TP_VR_PWRGD_CLKEN_L	NO_TEST=TRUE
9004_90A3_006_87D5	LVDS_BKL_ON	==	TP_LVDS_BKL_ON	NO_TEST=TRUE

UNUSED INTERNAL USB PORTS

2003	USB_TPAD_N	==	TP_USB_TPAD_N	NO_TEST=TRUE
2003	USB_TPAD_P	==	TP_USB_TPAD_P	NO_TEST=TRUE

MCP HAS INTERNAL 15K PULL-DOWNS

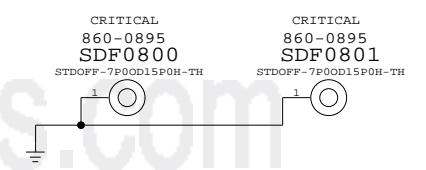
UNUSED MEMORY SIGNALS

3105	MEM_A_A<15>	==	TP_MEM_A_A<15>	NO_TEST=TRUE
3205	MEM_B_A<15>	==	TP_MEM_B_A<15>	NO_TEST=TRUE

TESTPOINT FOR OPTIONAL GMUX JTAG FROM MCP

1786	GMUX_JTAG_TCK_L	==	NC_GMUX_JTAG_TCK_L	NO_TEST=TRUE
1786	GMUX_JTAG_TDO	==	NC_GMUX_JTAG_TDO	NO_TEST=TRUE
1804	GMUX_JTAG_TDI	==	NC_GMUX_JTAG_TDI	NO_TEST=TRUE
1804	GMUX_JTAG_TMS	==	NC_GMUX_JTAG_TMS	NO_TEST=TRUE

K51 ONLY STANDOFFS



UNUSED SIGNAL ALIAS/STAND OFF

SYNC_MASTER=K51 SYNC_DATE=04/07/2008

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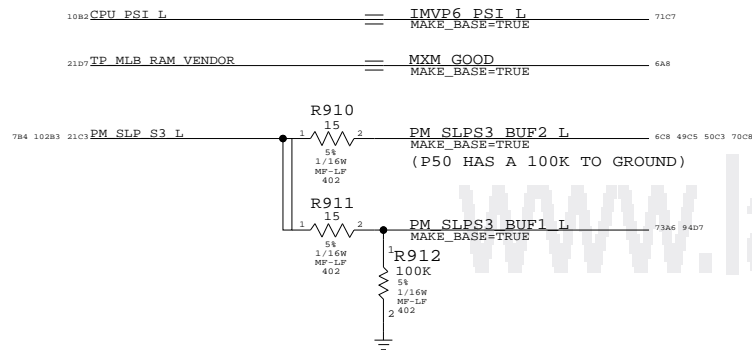
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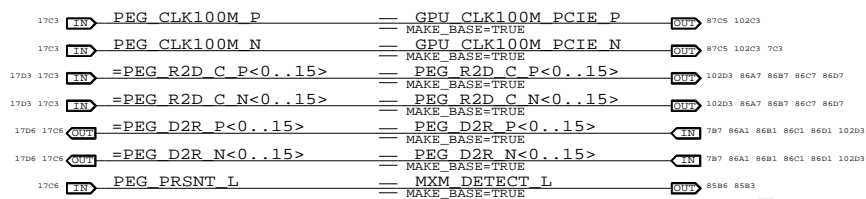
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE D	DRAWING NUMBER 051-7973	REV. A
	SCALE NONE	SHT 8 OF 109	

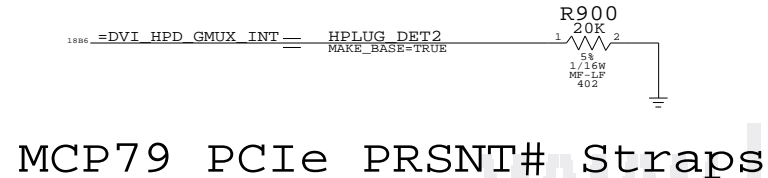
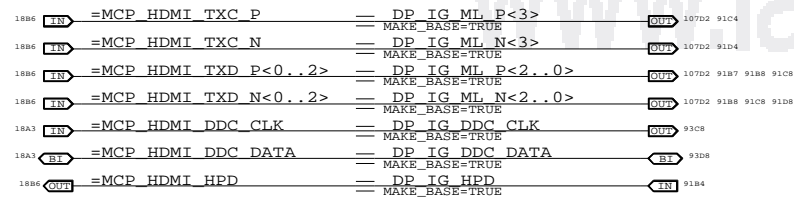
SIGNAL ALIAS



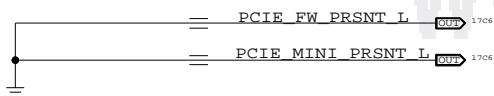
PEG Slot Support



DisplayPort / TMDS Support



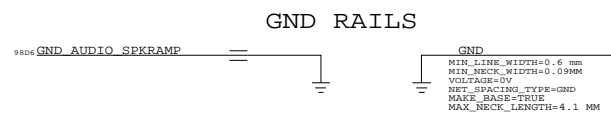
MCP79 PCIe PRSNT# Straps



USB ALIAS

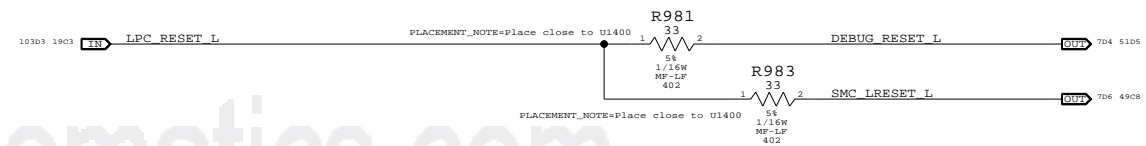


GROUND ALIAS

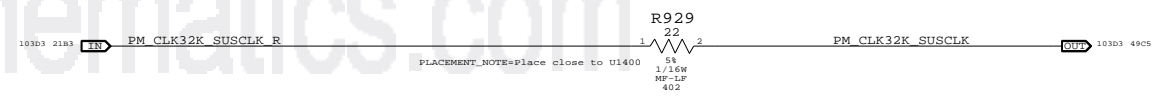
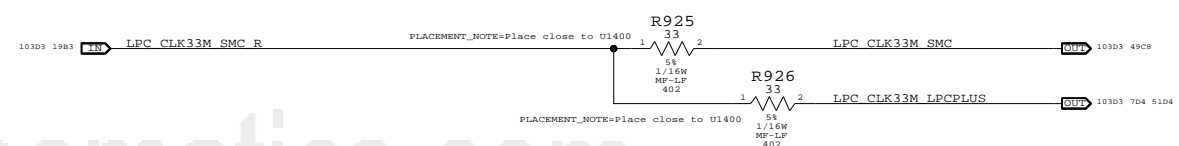
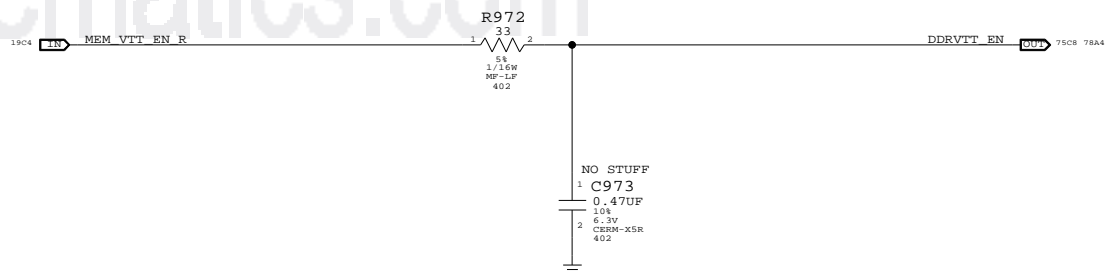
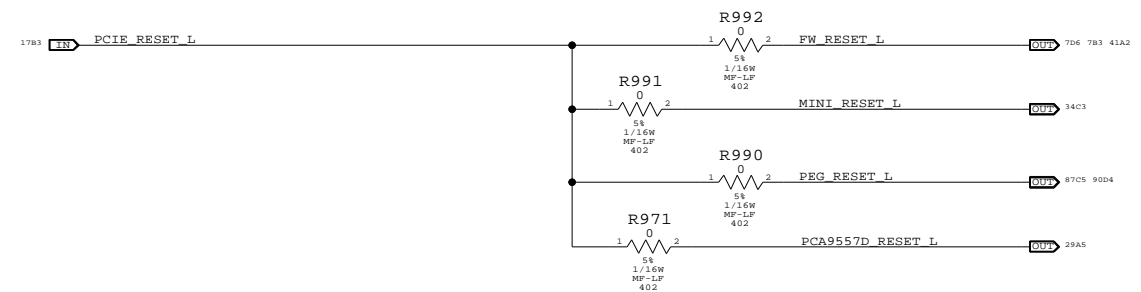


Platform Reset Connections

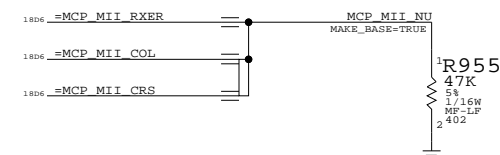
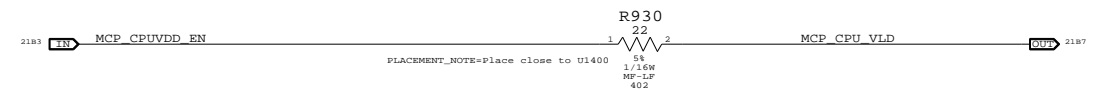
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



MCP_CPUVDD_EN WILL ASSERT AFTER MCP_PS_PWRGD IS UP

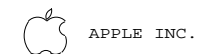


SIGNAL & GND ALIASES

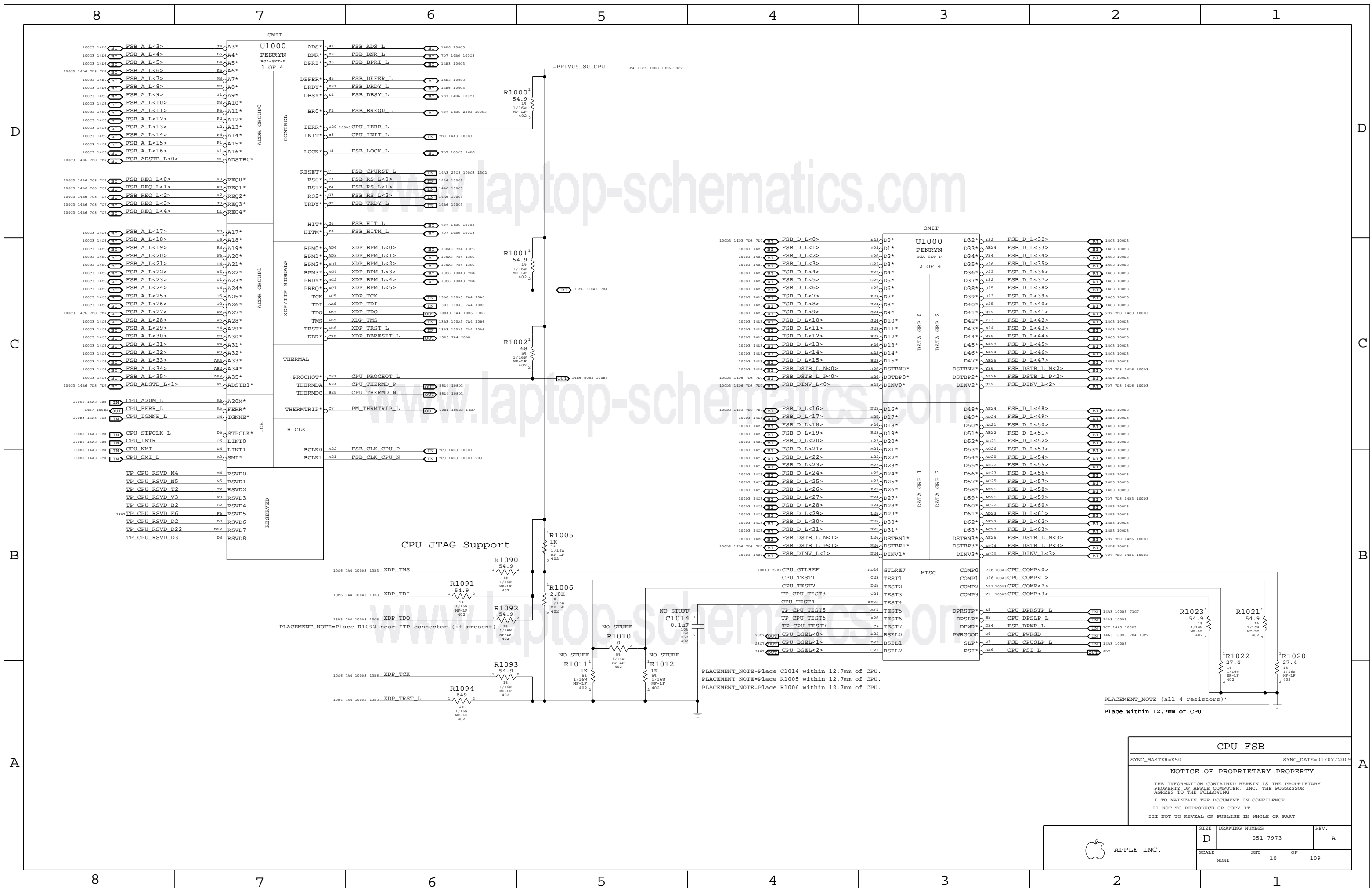
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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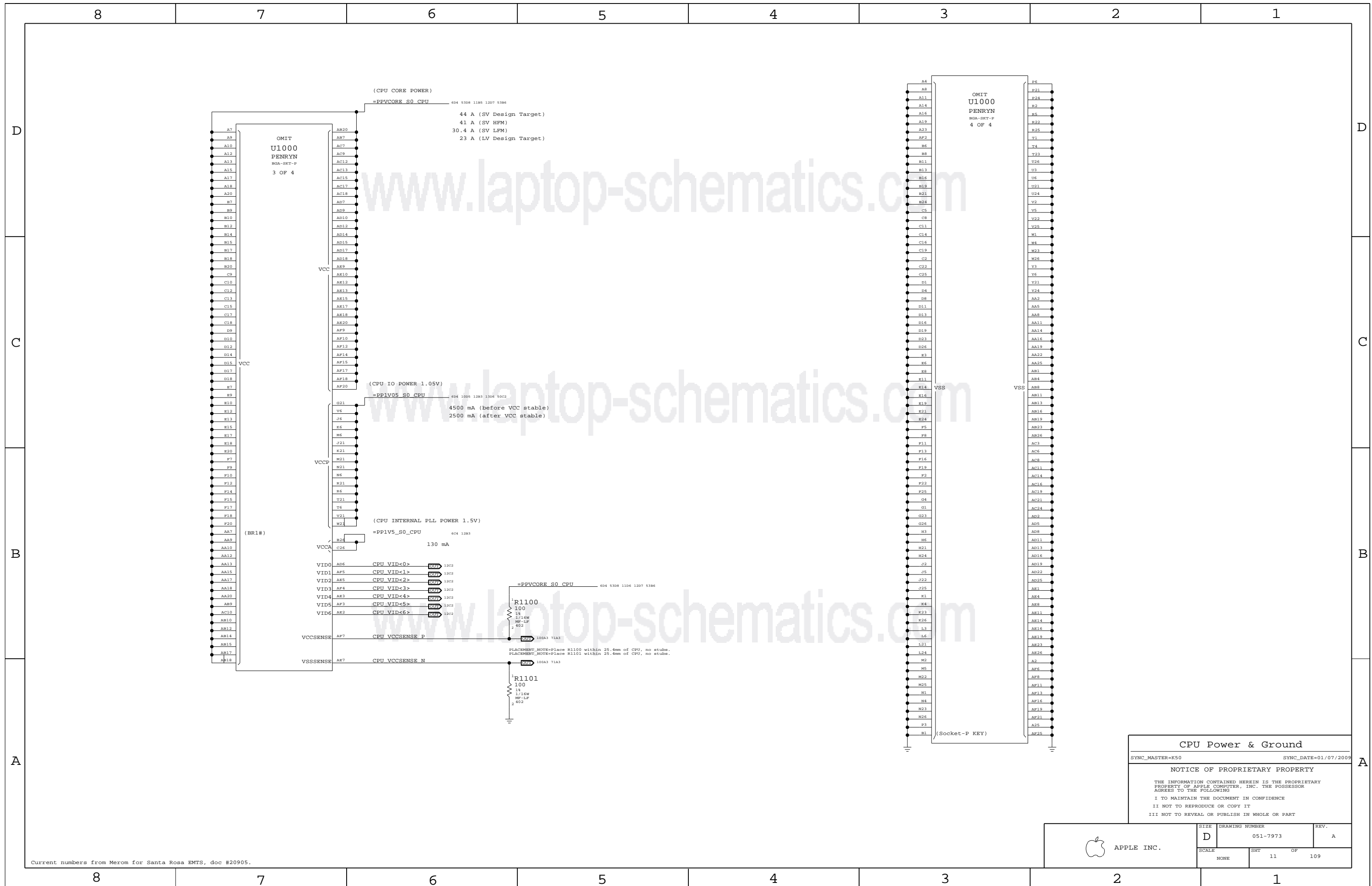
B

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A

CPU FSB		
SYNC_MASTER=K50	SYNC_DATE=01/07/2009	
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CPU Power & Ground

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NONE	11		

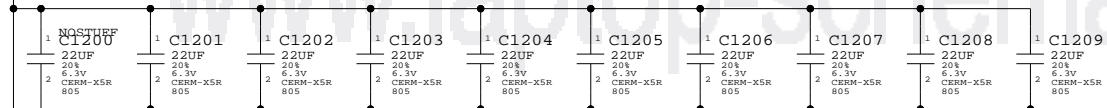
Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CPU VCORE HF AND BULK DECOUPLING
6X 220UF, 32X 22UF 0805

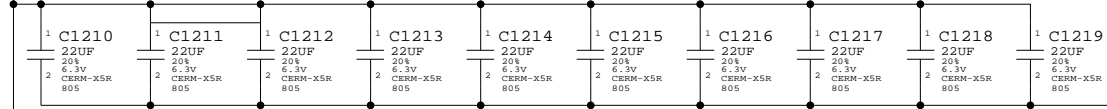
5386 1106 1185 5308 604=PPVCORE_S0_CPU

NOTE: CHANGED TO X5R CAPS TO MATCH PREVIOUS IMACS AND FOR C4

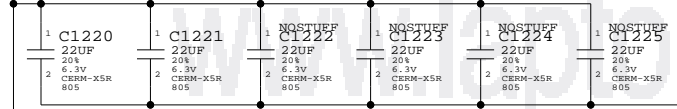
LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)



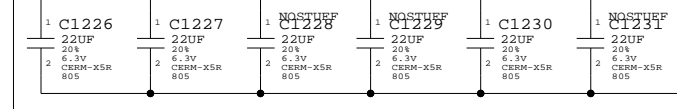
LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)



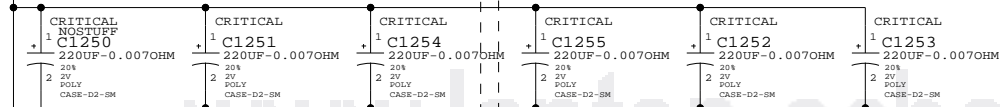
LAYOUT NOTE:
PLACE NEAR SOCKET NORTH SIDE (ON TOPSIDE)



LAYOUT NOTE:
PLACE NEAR SOCKET SOUTH SIDE (ON TOPSIDE)

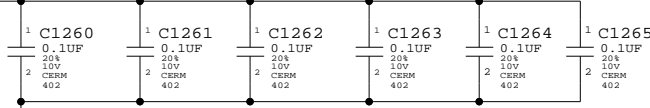


LAYOUT NOTE:
PLACE ON BOTTOMSIDE

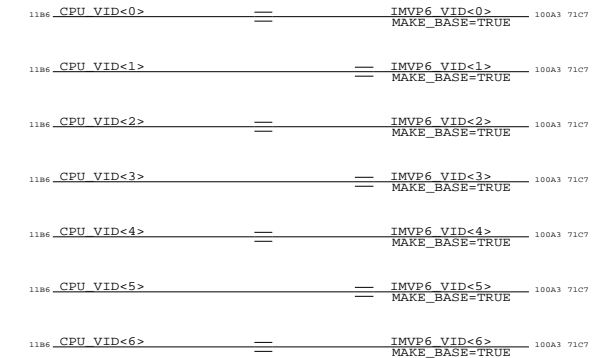


LAYOUT NOTE:
PLACE ON BOTTOMSIDE

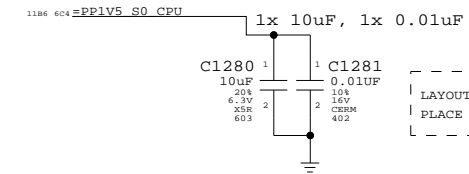
LAYOUT NOTE:
PLACE NEAR MCP



CPU VCORE VID CONNECTIONS



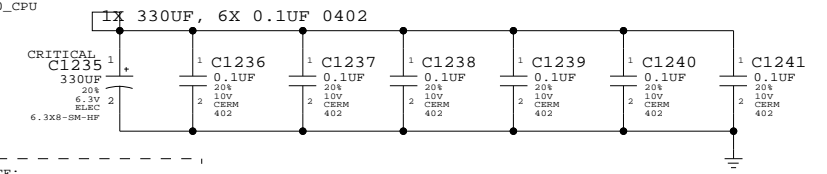
VCCA (CPU AVdd) DECOUPLING



LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

5002 1106 1106 1005 604=PP1V05_S0_CPU



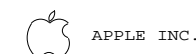
LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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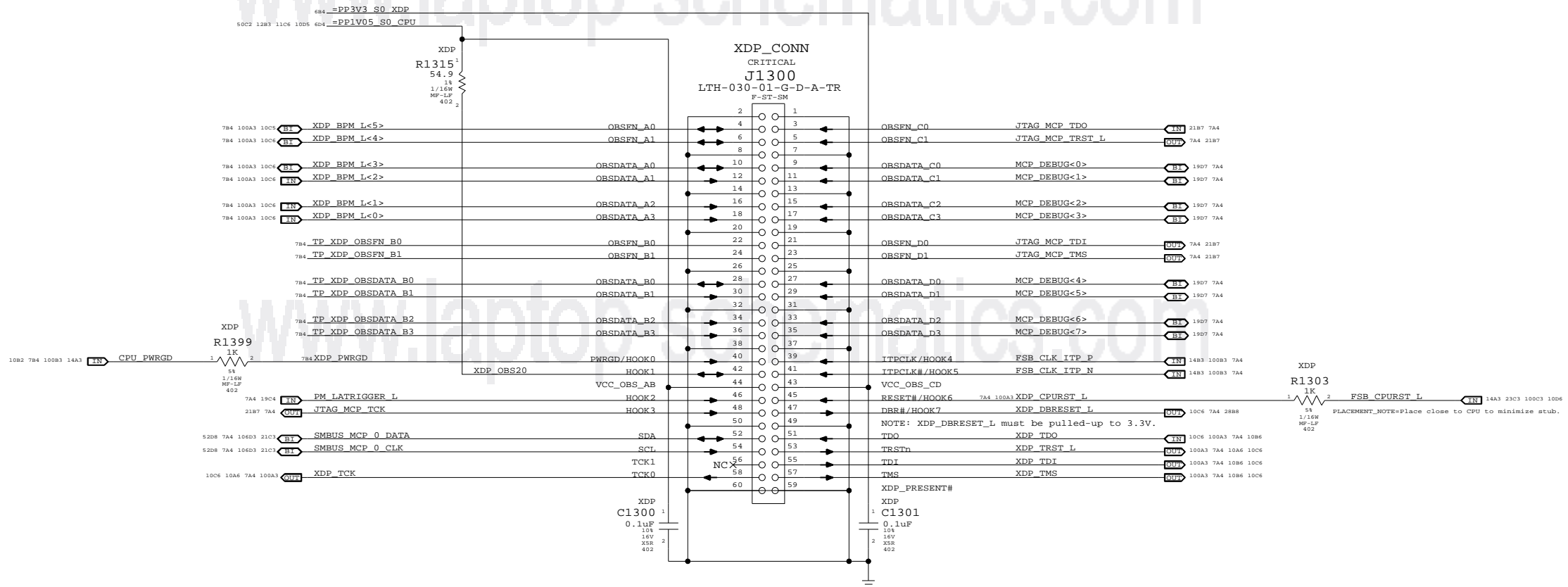
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NONE	12	109

MCP79-specific pinout

www.laptop-schematics.com



www.laptop-schematics.com

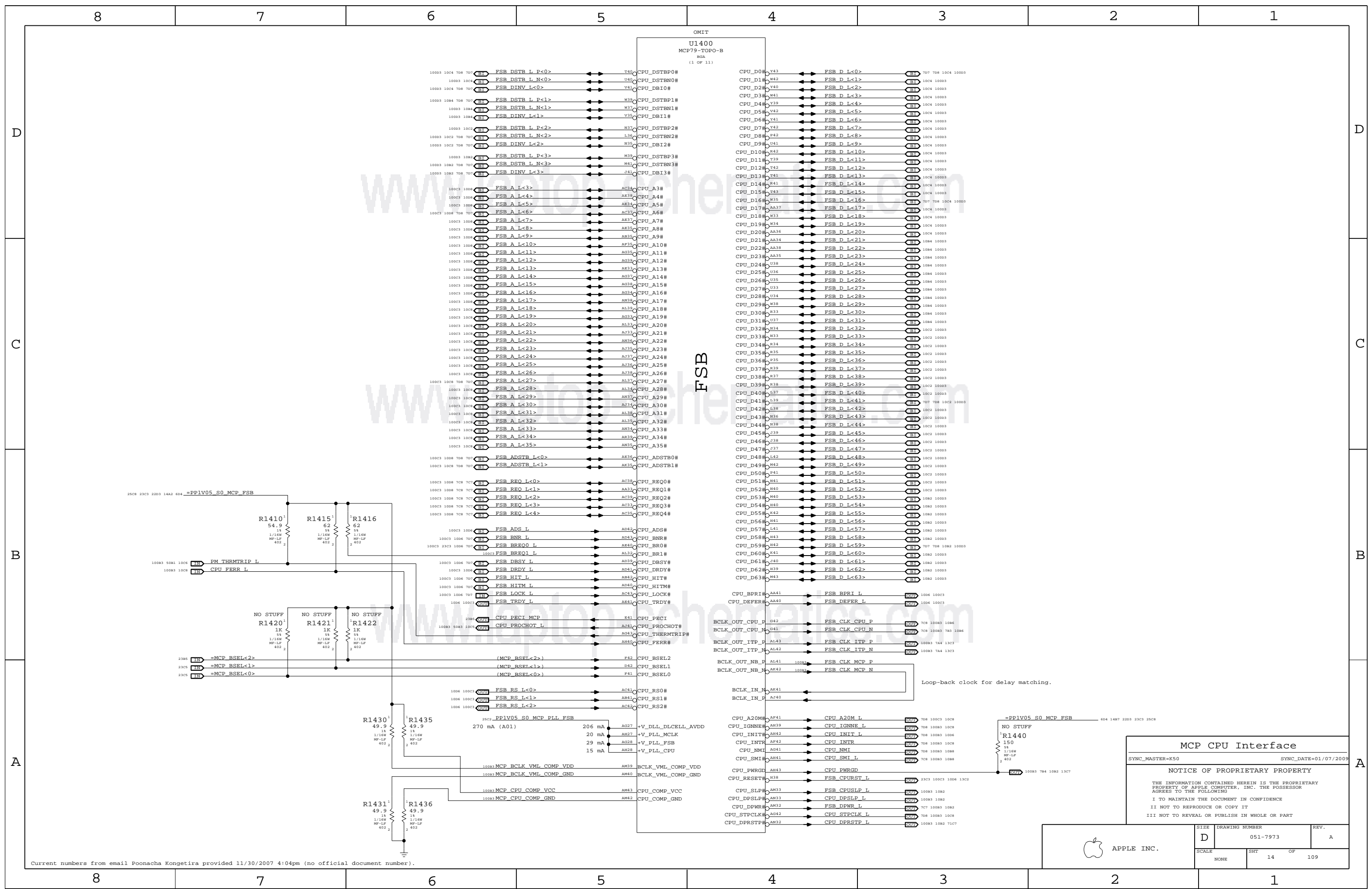
eXtended Debug Port (XDP)

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NONE	13		

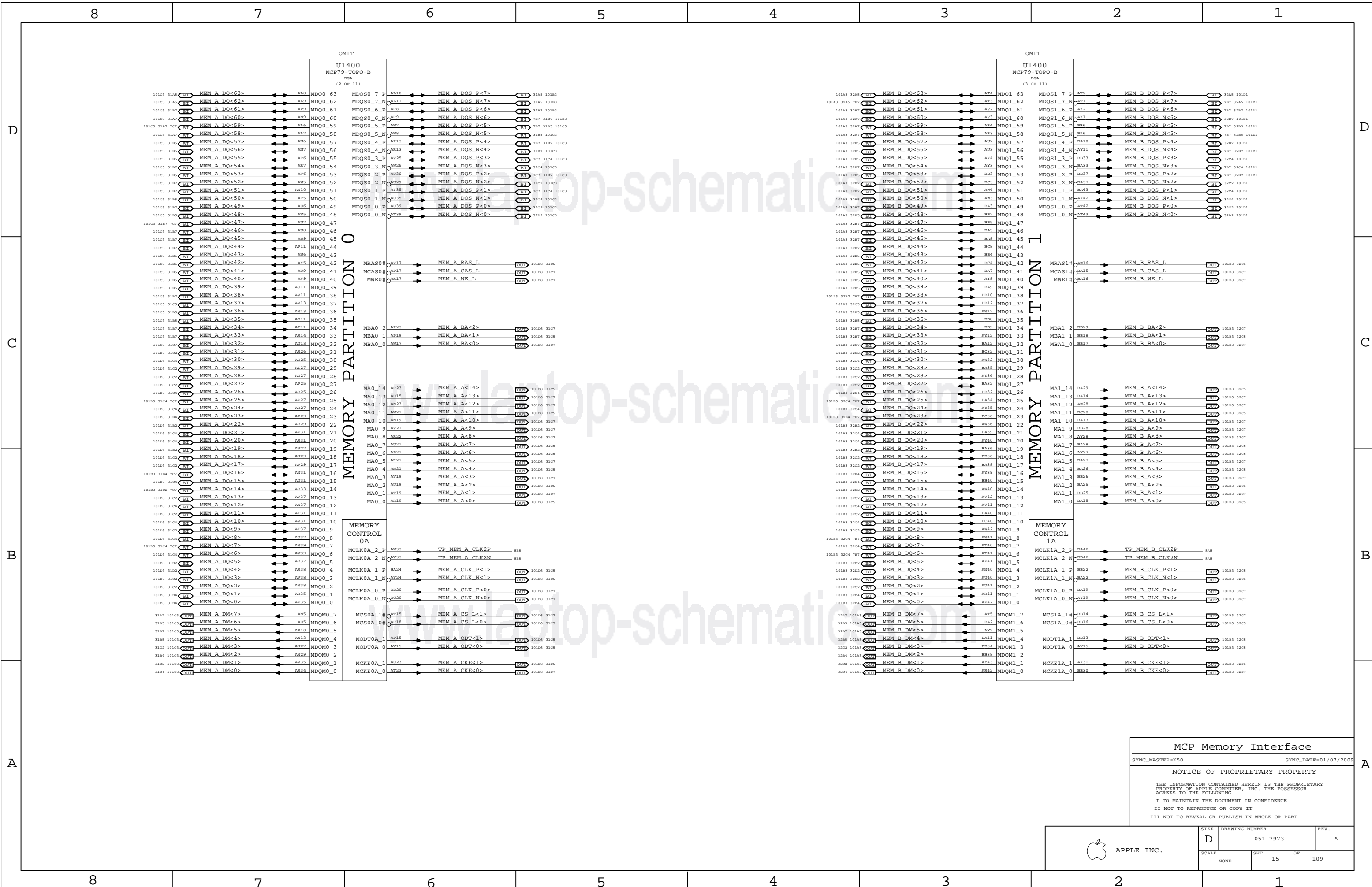


www.topshere.com

MCP CPU Interface
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NONE	14	109	

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MCP Memory Interface

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

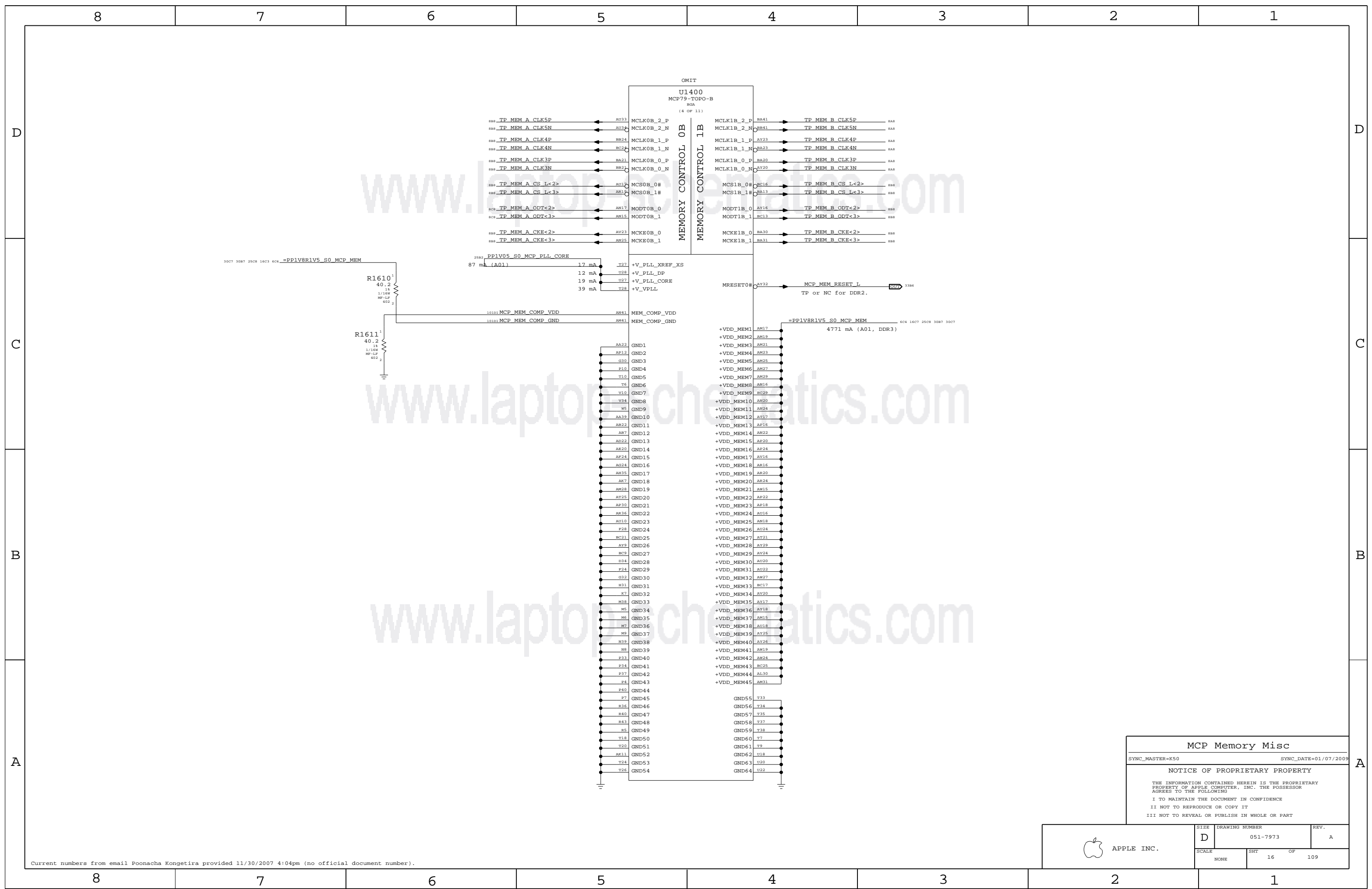
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MCP Memory Misc

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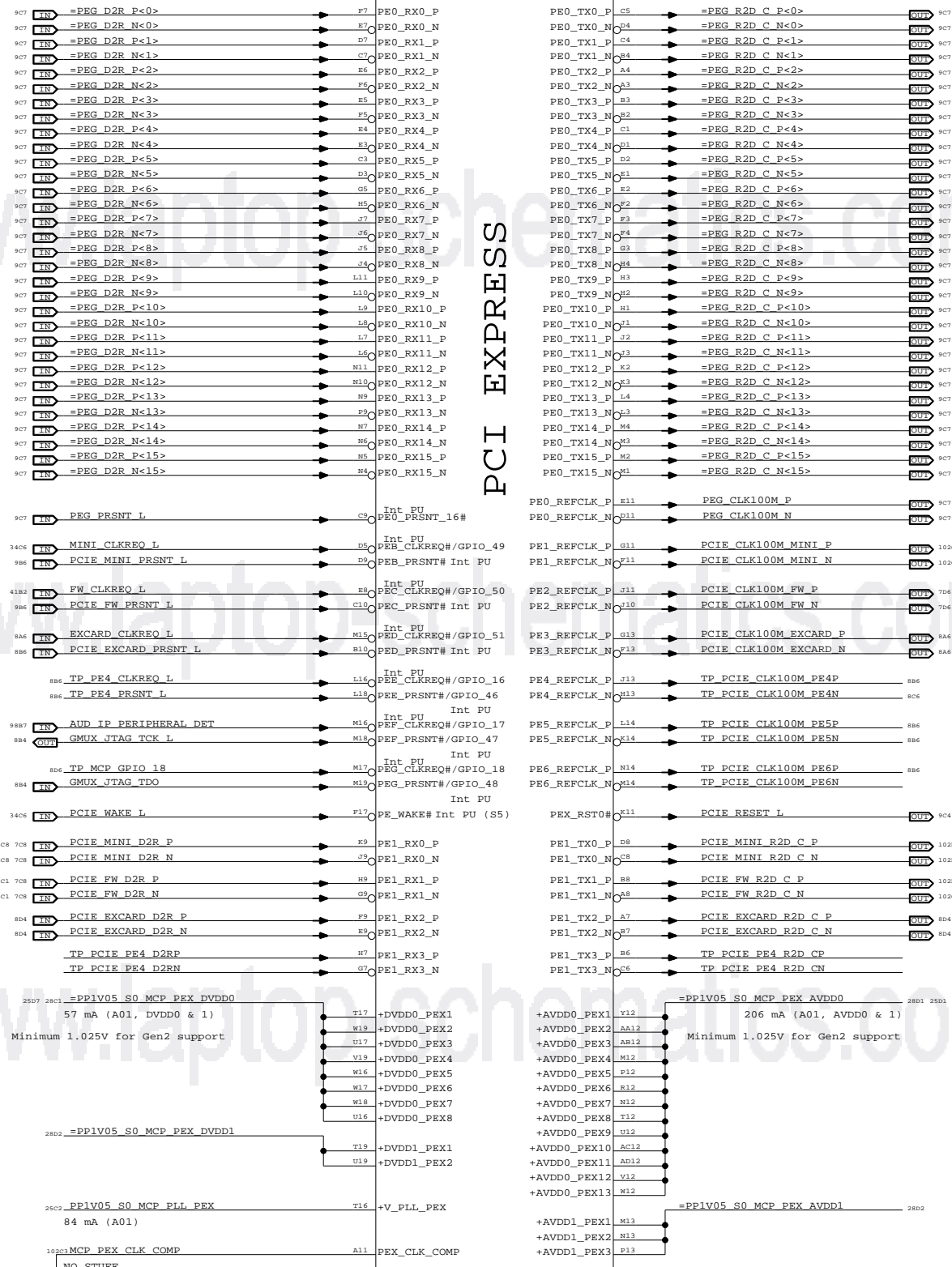
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OMIT

U1400
MCP79-TOPO-B
BGA
(5 OF 11)

PCI EXPRESS



If PEG interface is not used, ground DVDD0_PEX and AVDD0_PEX.
If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

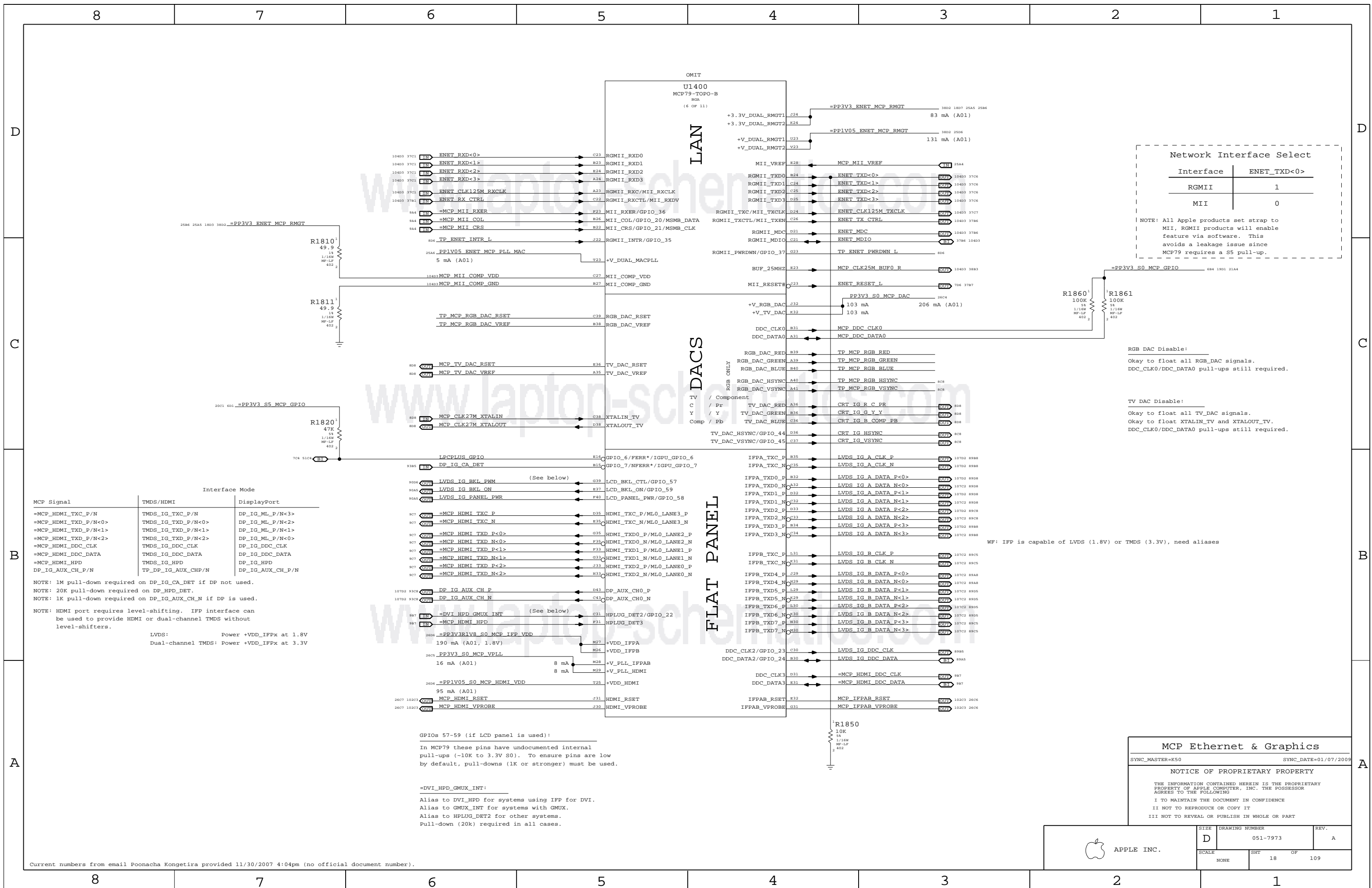
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NONE	17	109



Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable: _____
 Okay to float all RGB_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable: _____
 Okay to float all TV_DAC signals.
 DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
 NOTE: 20K pull-down required on DP_HPD_DET.
 NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
 NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS: Power +VDD_IPFx at 1.8V
 Dual-channel TMDS: Power +VDD_IPFx at 3.3V

GPIOs 57-59 (if LCD panel is used):
 In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:
 Alias to DVI_HPD for systems using IFP for DVI.
 Alias to GMUX_INT for systems with GMUX.
 Alias to HPLUG_DET2 for other systems.
 Pull-down (20k) required in all cases.

MCP Ethernet & Graphics

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

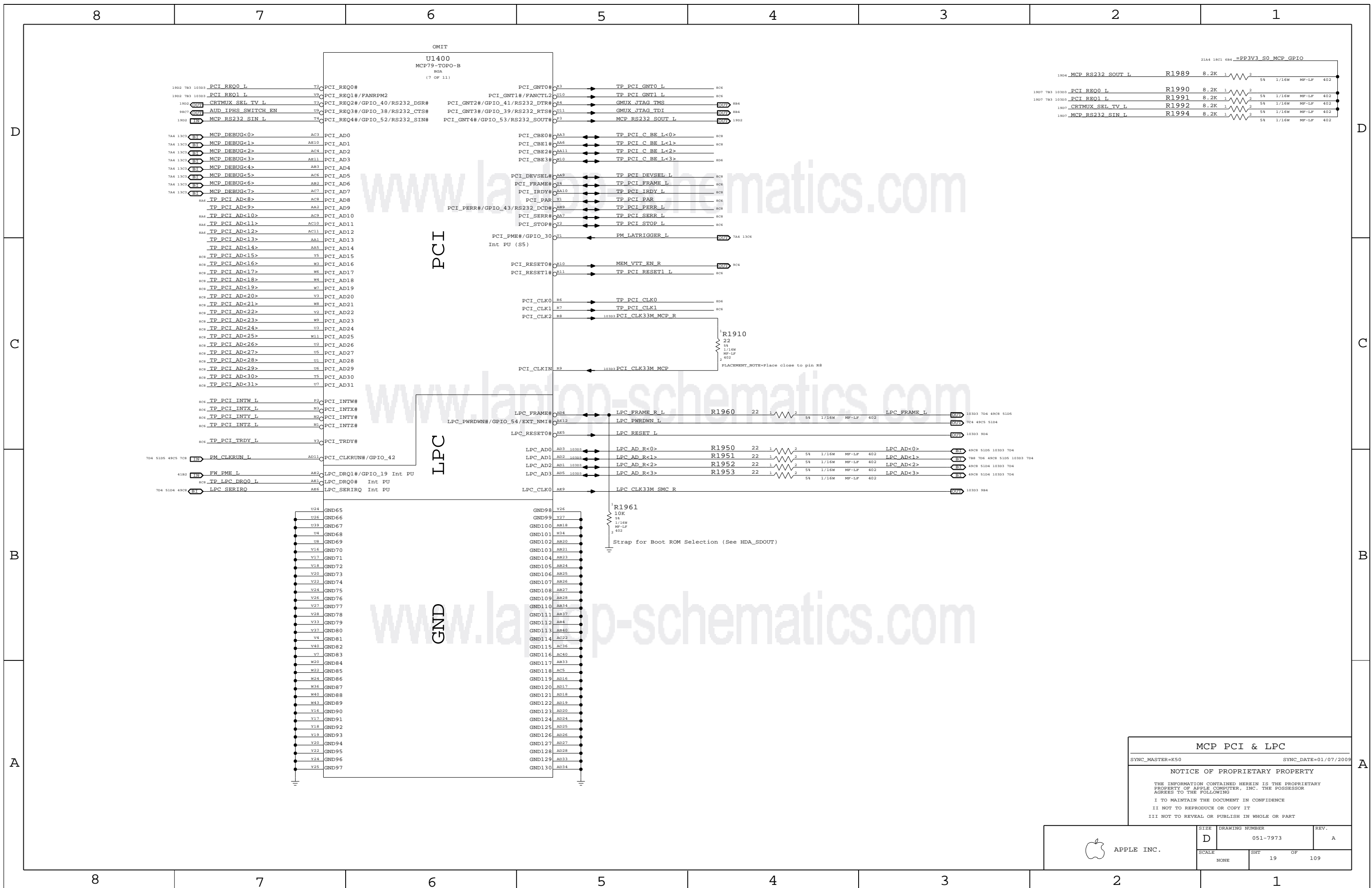
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NONE	18	109



MCP PCI & LPC

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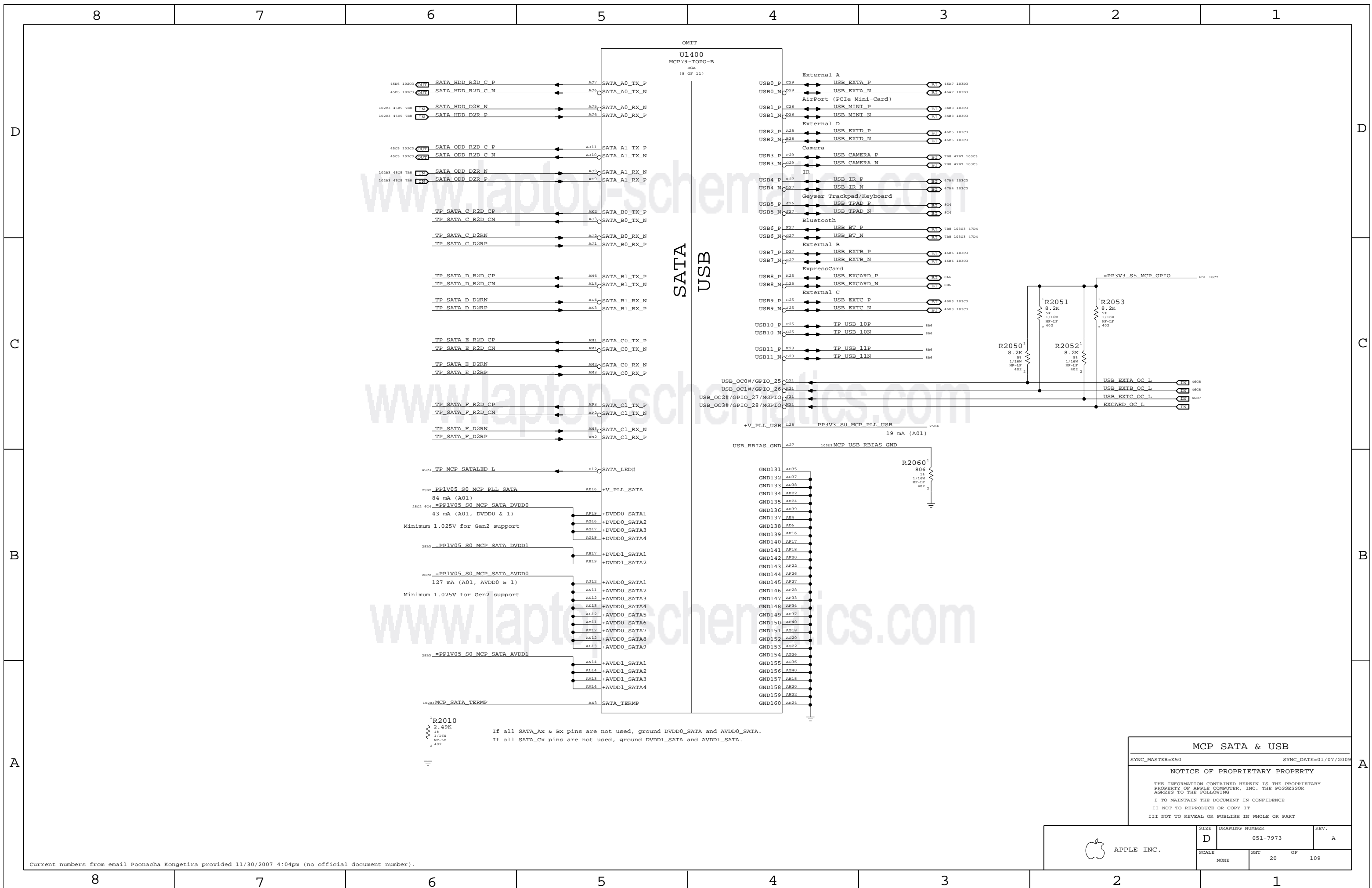
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	19		



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MCP SATA & USB

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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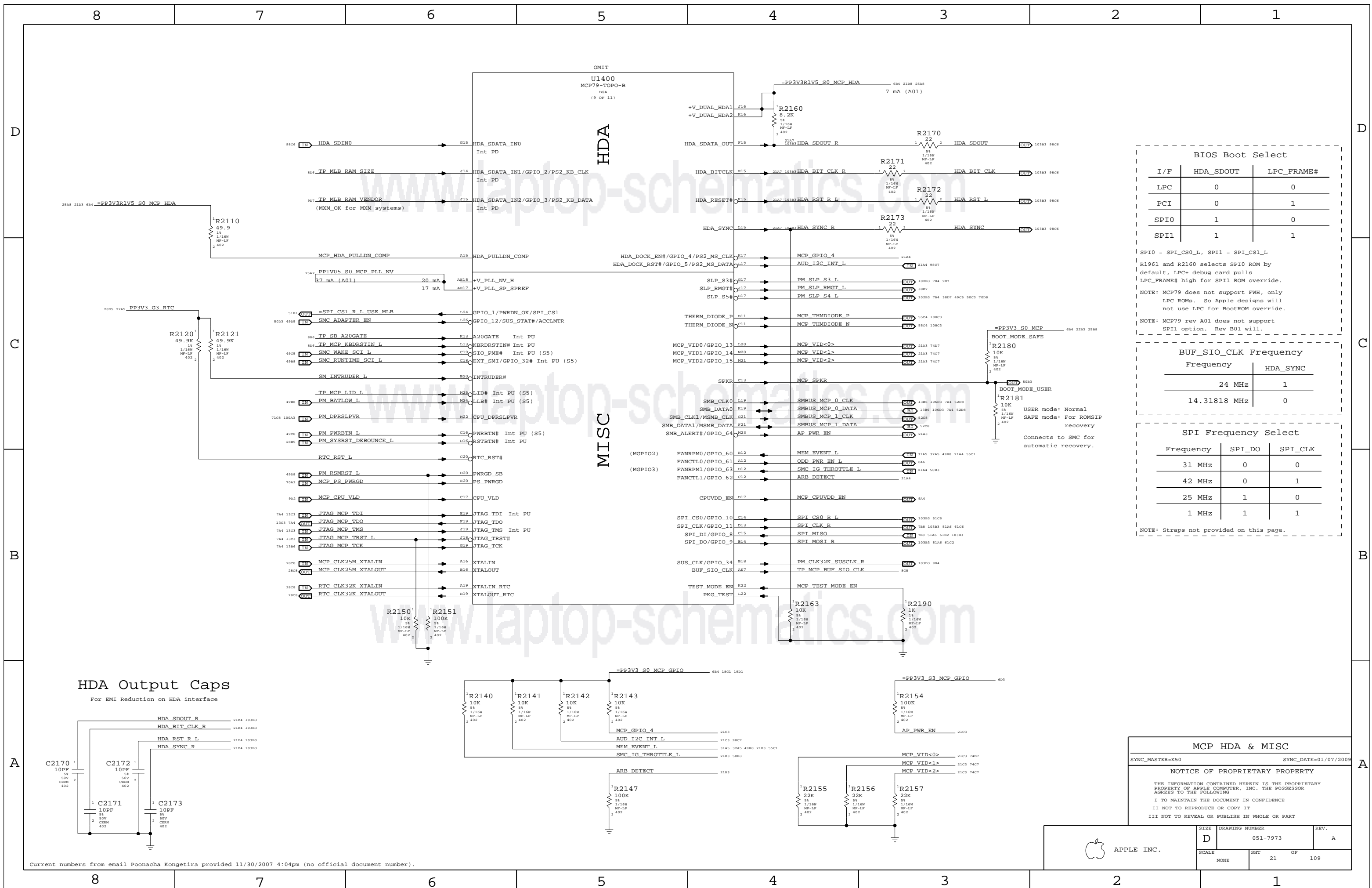
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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	20	109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
 NOTE: MCP79 does not support FWB, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
 NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

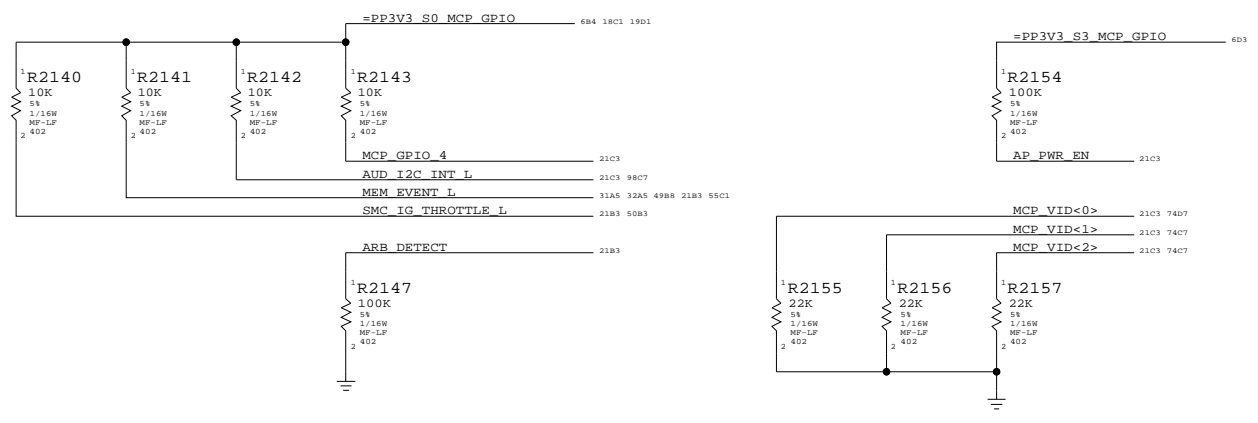
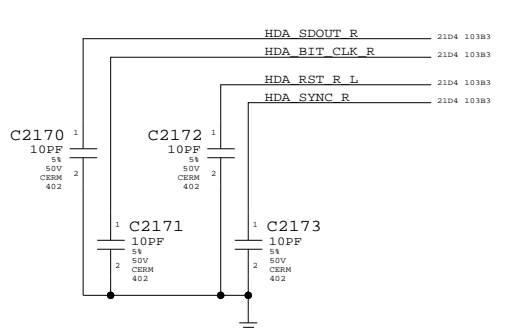
Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps
For EMI Reduction on HDA interface



MCP HDA & MISC

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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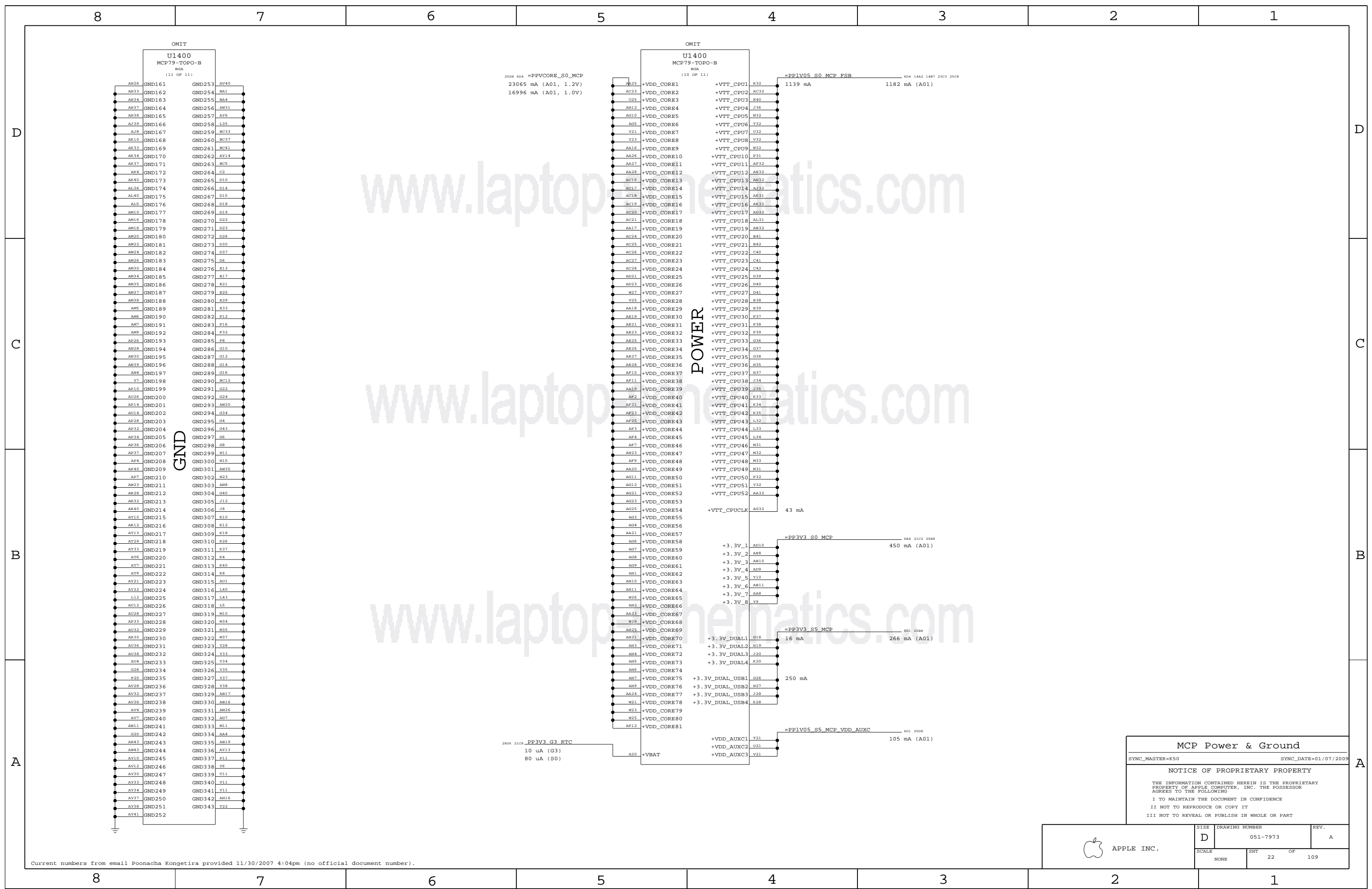
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	21		

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MCP Power & Ground

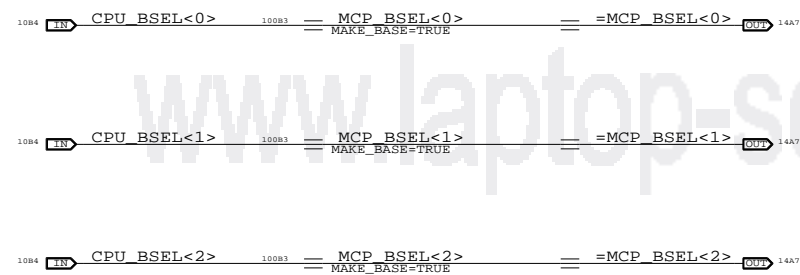
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	22	109	

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CPU FSB Frequency Straps

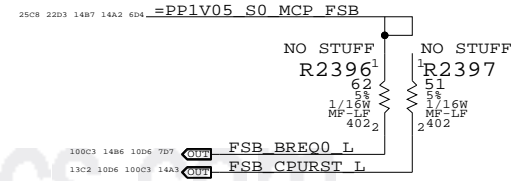


BSEL<2..0>	FSB MHz
000	266
001	133
010	200
011	(166)
100	333
101	100
110	(400)
111	(RSVD)

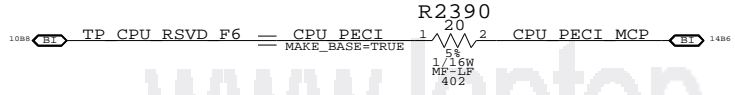
NOTE: () values not supported by MCP79.

Extra FSB Pull-ups

Exist in MRB but not Intel designs. Here for CYA. If found to be necessary, will move to pagel4.csa



Merom/Penryn do not officially support PECI, but it's not clear whether PECI interface is present or not. T12 used pin F6.



Debug: CPU

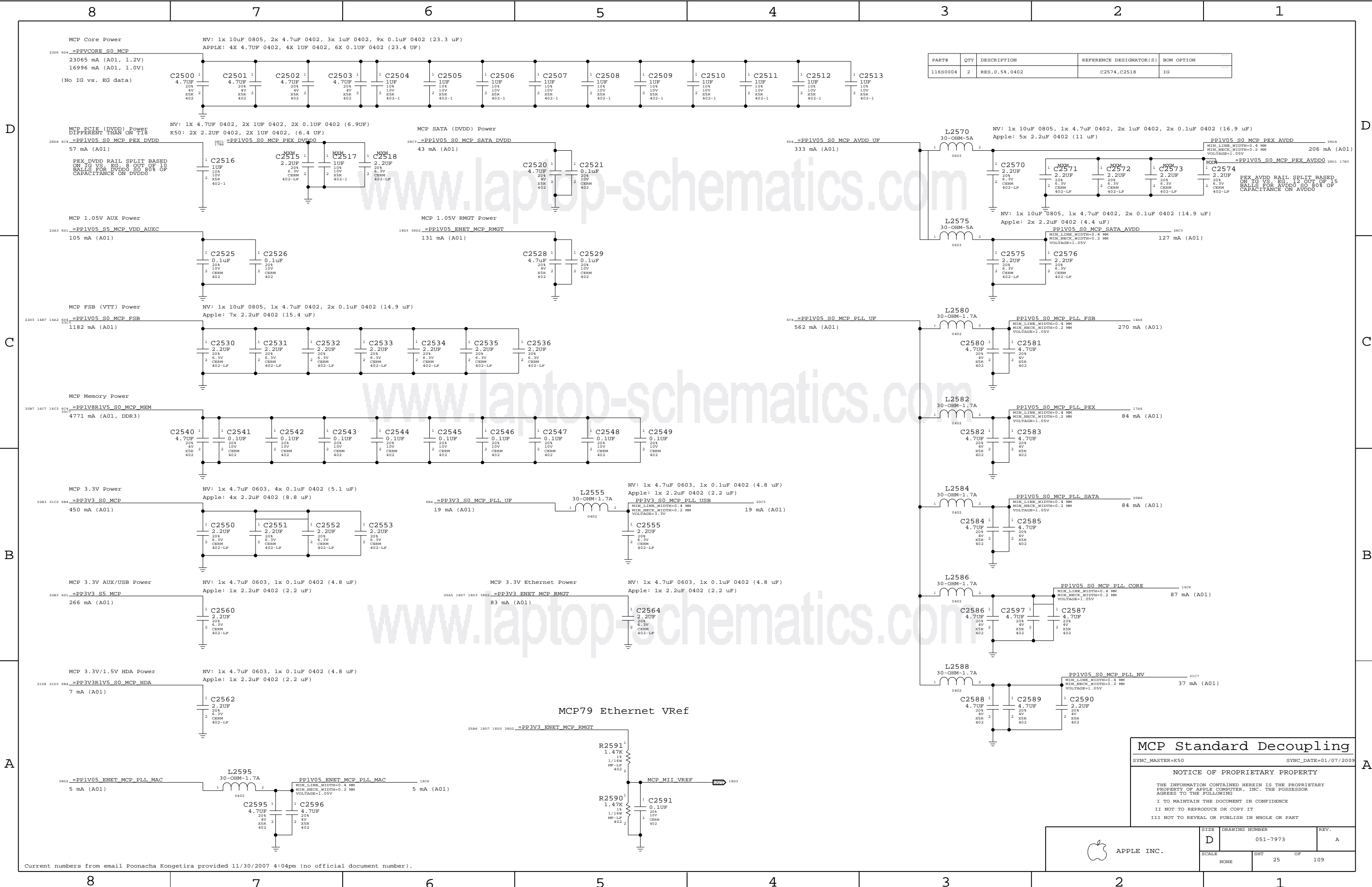
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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	D	051-7973	A
SCALE	SHT	OF	109
NONE	23		



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	2	RES,0.5%,0402	C2574,C2518	IG

MCP Standard Decoupling

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT 25 OF 109	

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

8

7

6

5

4

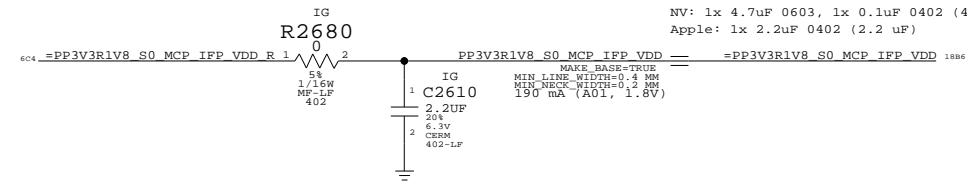
3

2

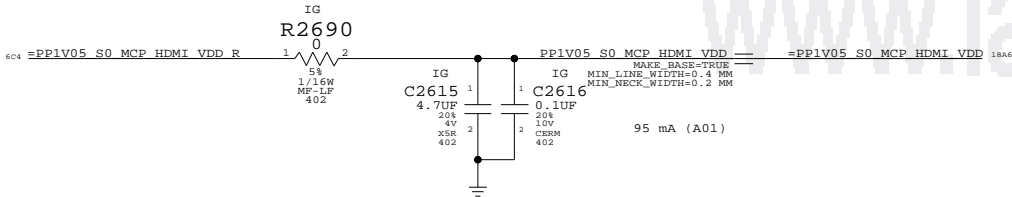
1

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

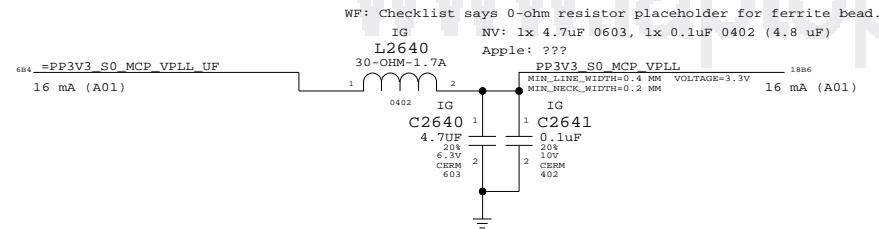
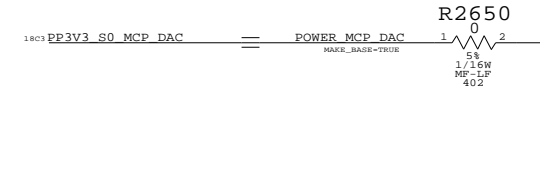
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0.5%,402	C2610		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0.5%,402	C2616		MXM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0004	1	RES,0.5%,402	C2641		MXM

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MCP Graphics Support

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	26	109

8

7

6

5

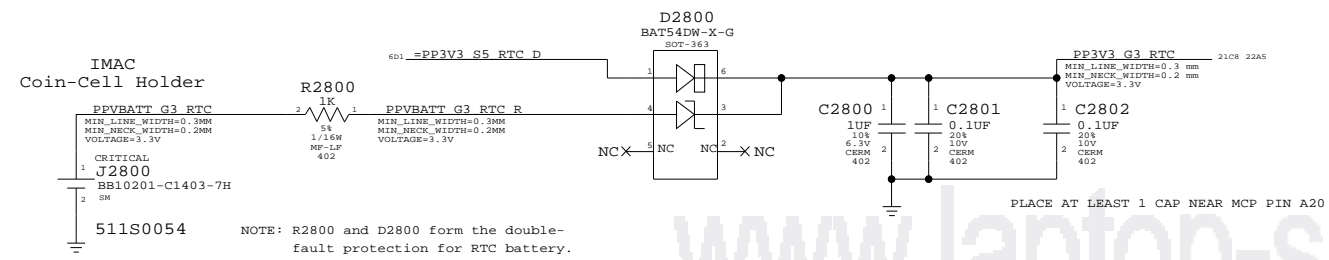
4

3

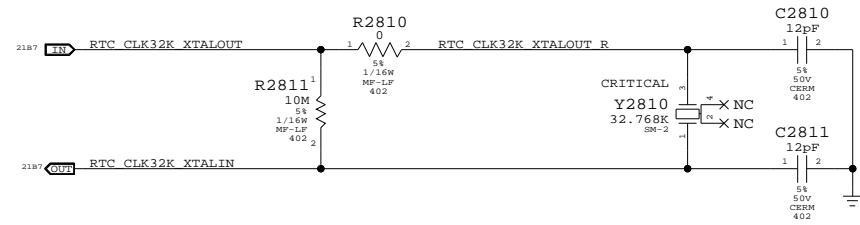
2

1

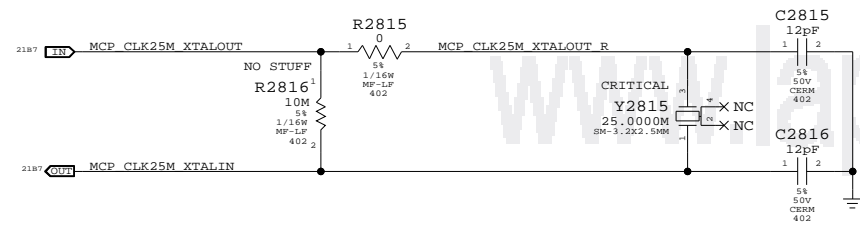
RTC Power Sources



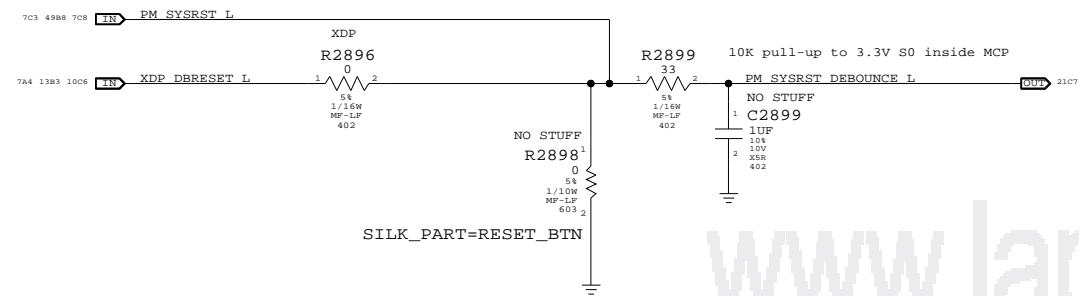
RTC Crystal



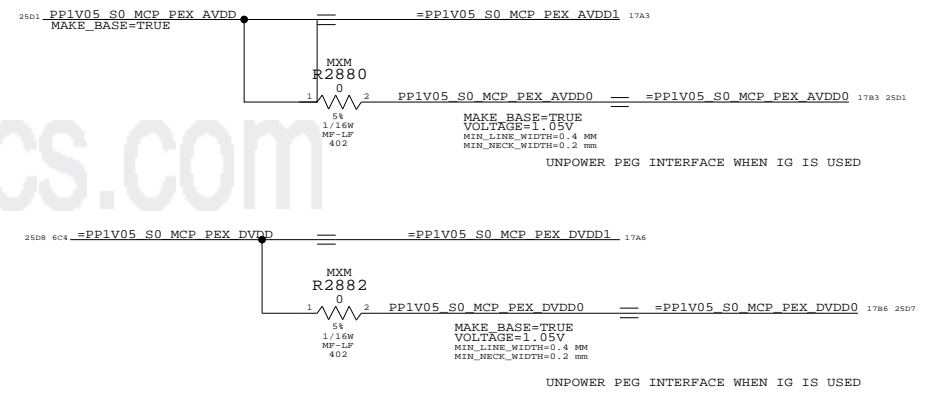
MCP 25MHz Crystal



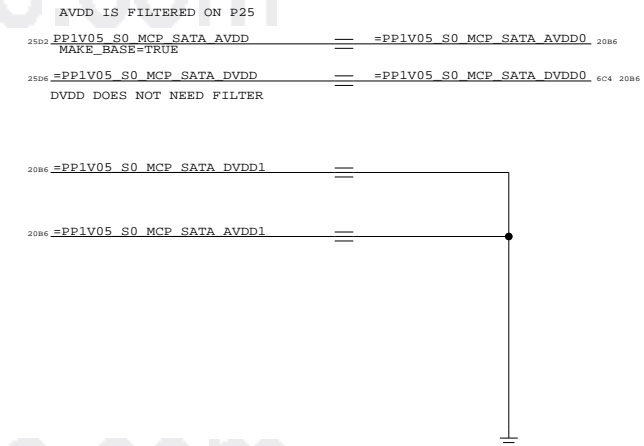
Reset Button



PEG POWER ALIAS/OPTION TO GND UNUSED POWER PIN



SATA ALIAS/GROUNDING UNUSED DVDD1 AND AVDD1

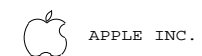


SB Misc

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D	051-7973	A
SCALE	SHT	OF
NONE	28	109

Page Notes

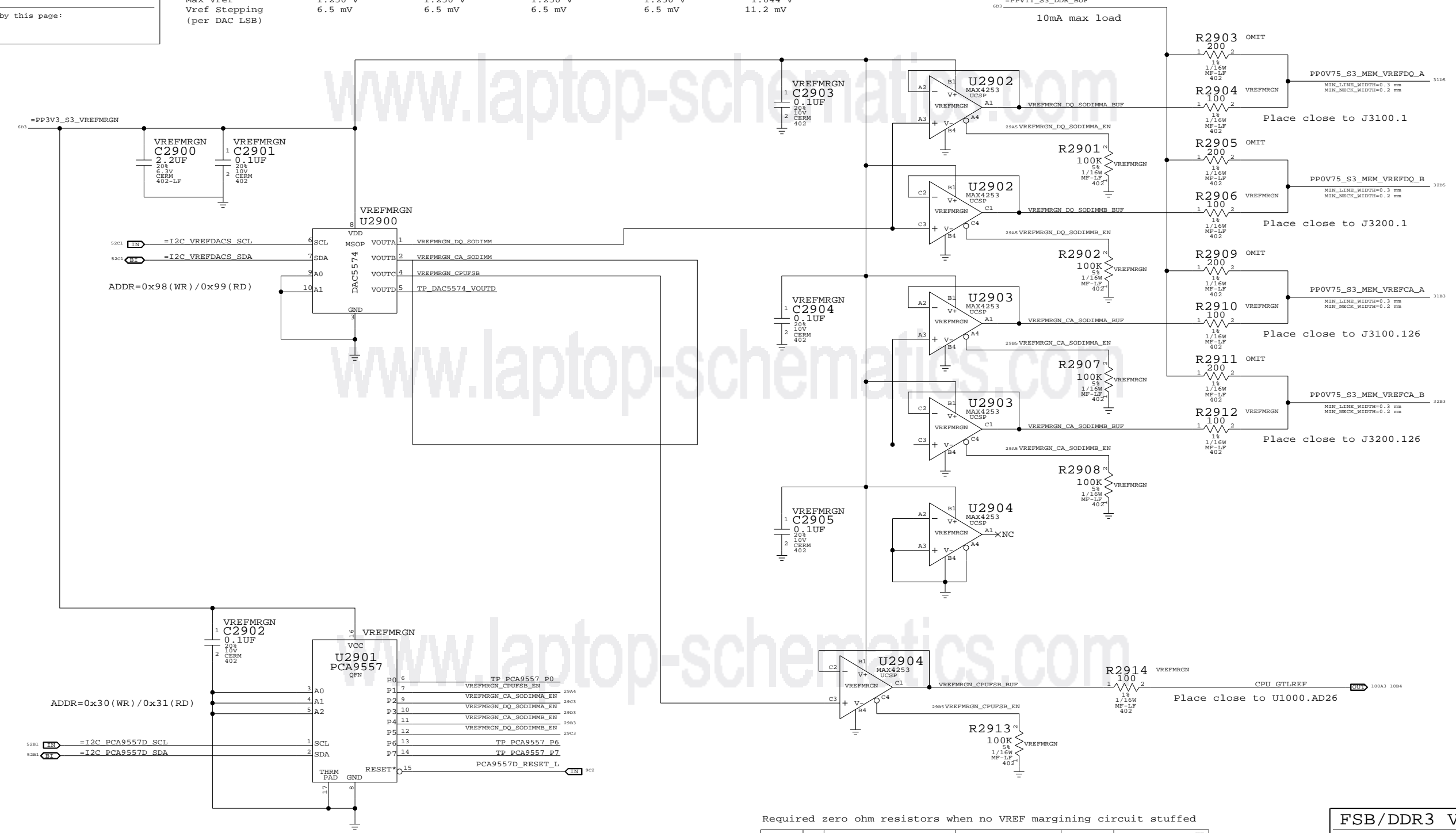
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF
DAC channel	A	B	A	B	C
Min DAC code	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480149	1	RES, 402, 1/16W, 200 OHM, 1%	R2903		VREFMRGN
11680004	1	RES, 402, 1/16W, 0 OHM, 5%	R2903		PRODUCTION
11480149	1	RES, 402, 1/16W, 200 OHM, 1%	R2905		VREFMRGN
11680004	1	RES, 402, 1/16W, 0 OHM, 5%	R2905		PRODUCTION
11480149	1	RES, 402, 1/16W, 200 OHM, 1%	R2909		VREFMRGN
11680004	1	RES, 402, 1/16W, 0 OHM, 5%	R2909		PRODUCTION
11480149	1	RES, 402, 1/16W, 200 OHM, 1%	R2911		VREFMRGN
11680004	1	RES, 402, 1/16W, 0 OHM, 5%	R2911		PRODUCTION

FSB/DDR3 Vref Margining

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	29		

D

D

C

C

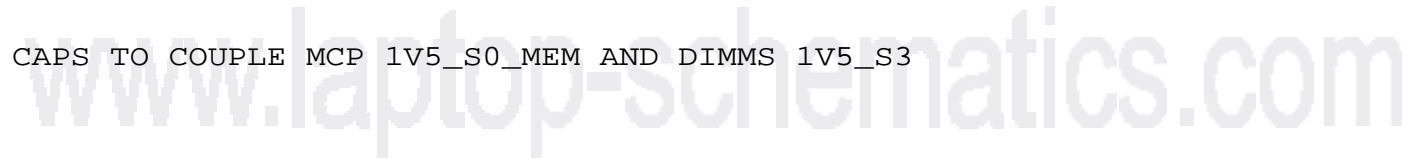
B

B

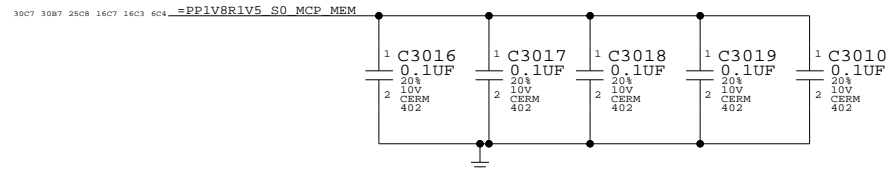
A

A

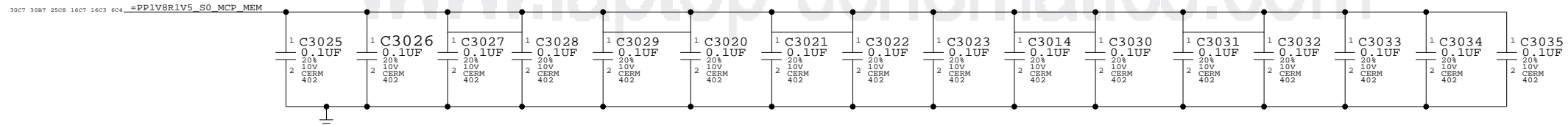
CAPS TO COUPLE MCP 1V5_S0_MEM AND DIMMS 1V5_S3



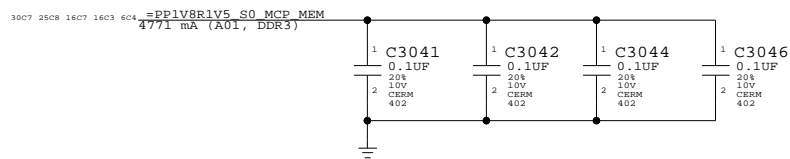
CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM A (FURTHER FROM MCP)



CAPS TO COUPLE MCP 1V5_S0_MEM ON DIMM B (CLOSER TO MCP)



EXTRA DECOUPLING CAPS FOR MCP MEM RAIL



MEMORY COUPLING CAPS

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	D	051-7973	A
SCALE	SHT	OF	
NONE	30	109	

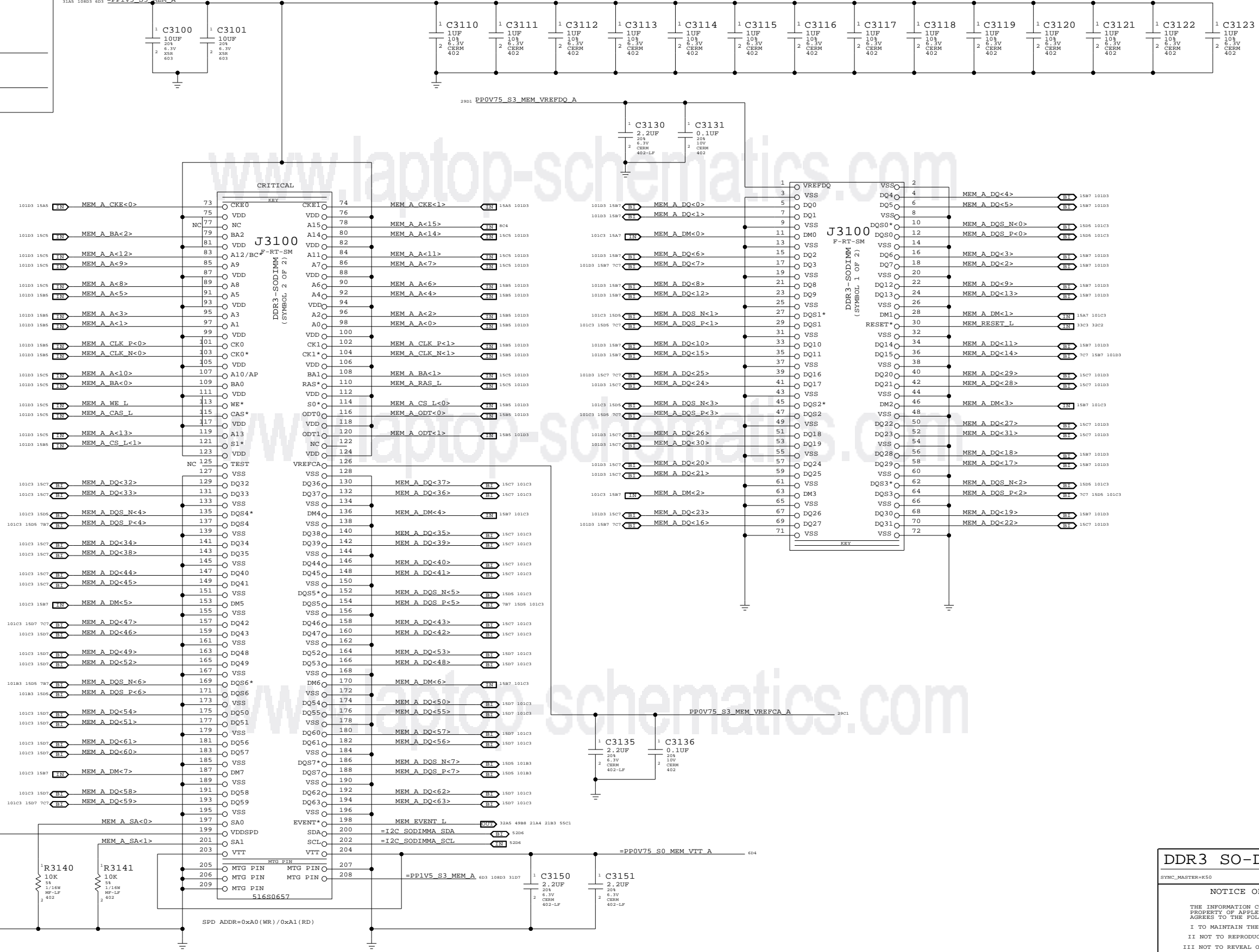
Page Notes

Power aliases required by this page:
 - =PP1V5_S0_MEM_A
 - =PP1V5_S3_MEM_A
 - =PP0V75_S0_MEM_VTT_A
 - =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

BOM options provided by this page:
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 SO-DIMM Connector A

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	D	051-7973	A
SCALE	SHT	OF	
NONE	31	109	

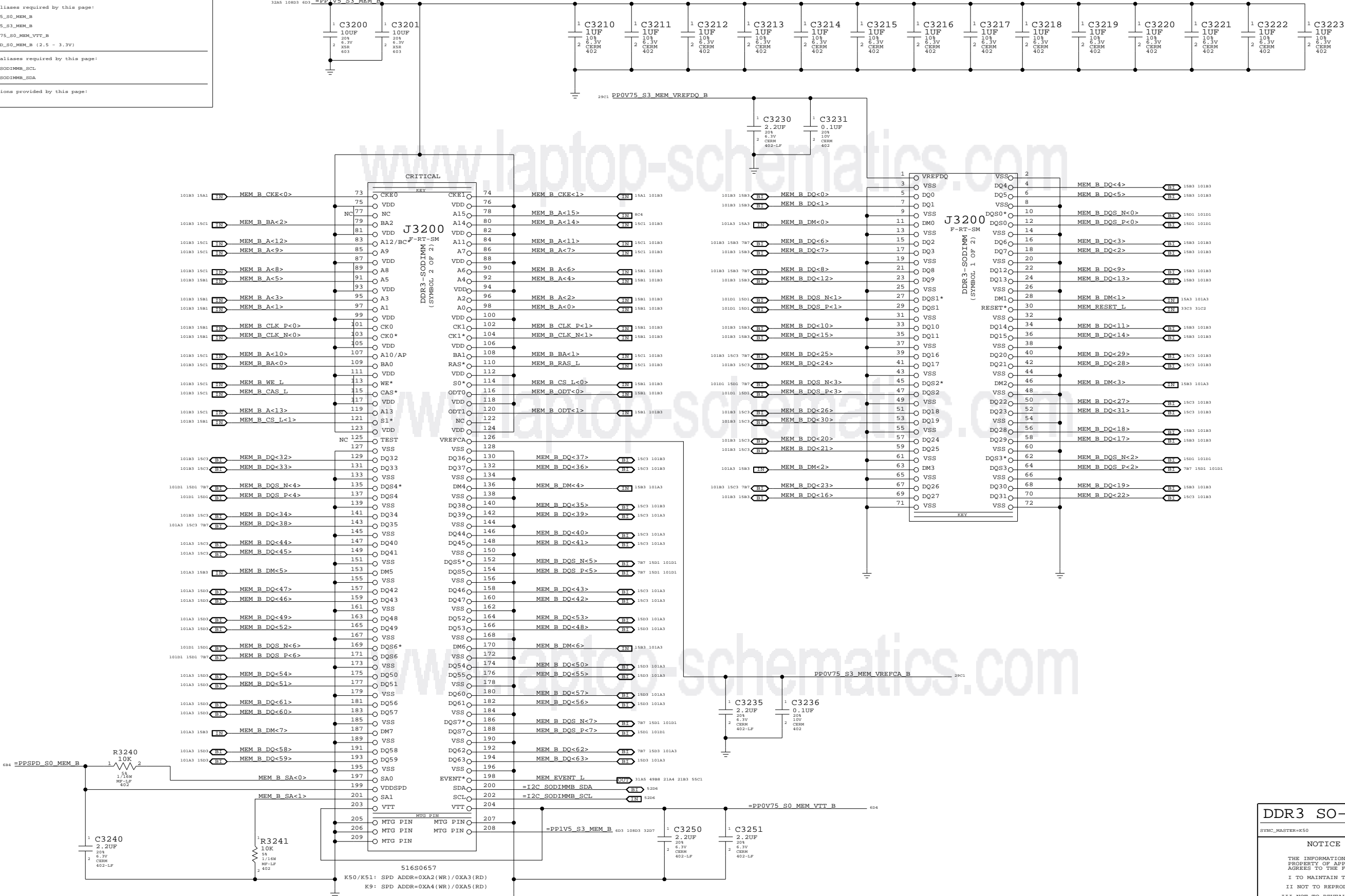
Page Notes

Power aliases required by this page:
 - =PP1V5_S0_MEM_B
 - =PP1V5_S3_MEM_B
 - =PP0V75_S0_MEM_VTT_B
 - =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

BOM options provided by this page:
 (NONE)

DDR3 DECOUPLING AND GROUND RETURN CAPS (CONNECTOR SIDE)



DDR3 SO-DIMM CONNECTOR B

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

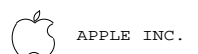
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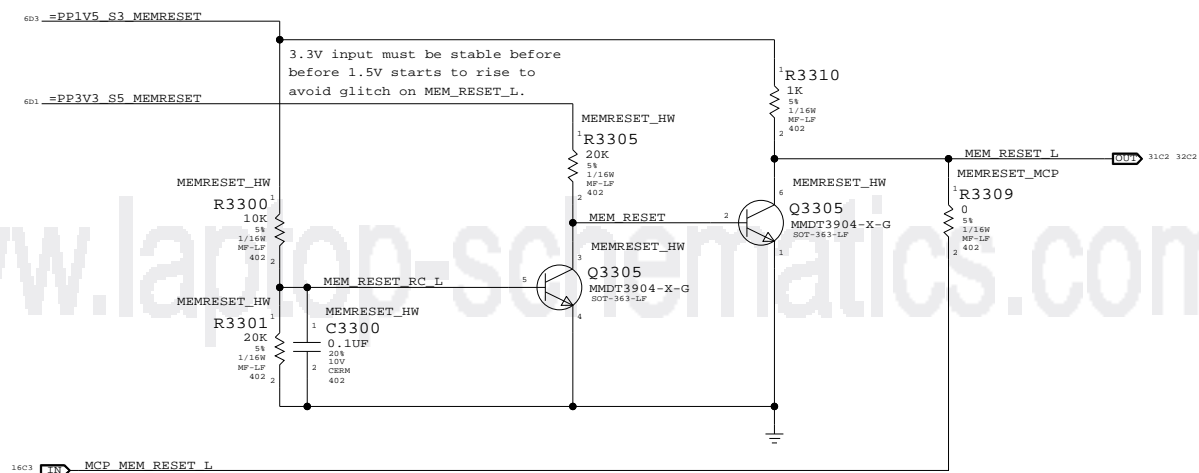
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	32	109

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DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



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DDR3 Support
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SCALE	SHT	OF	
NONE	33	109	

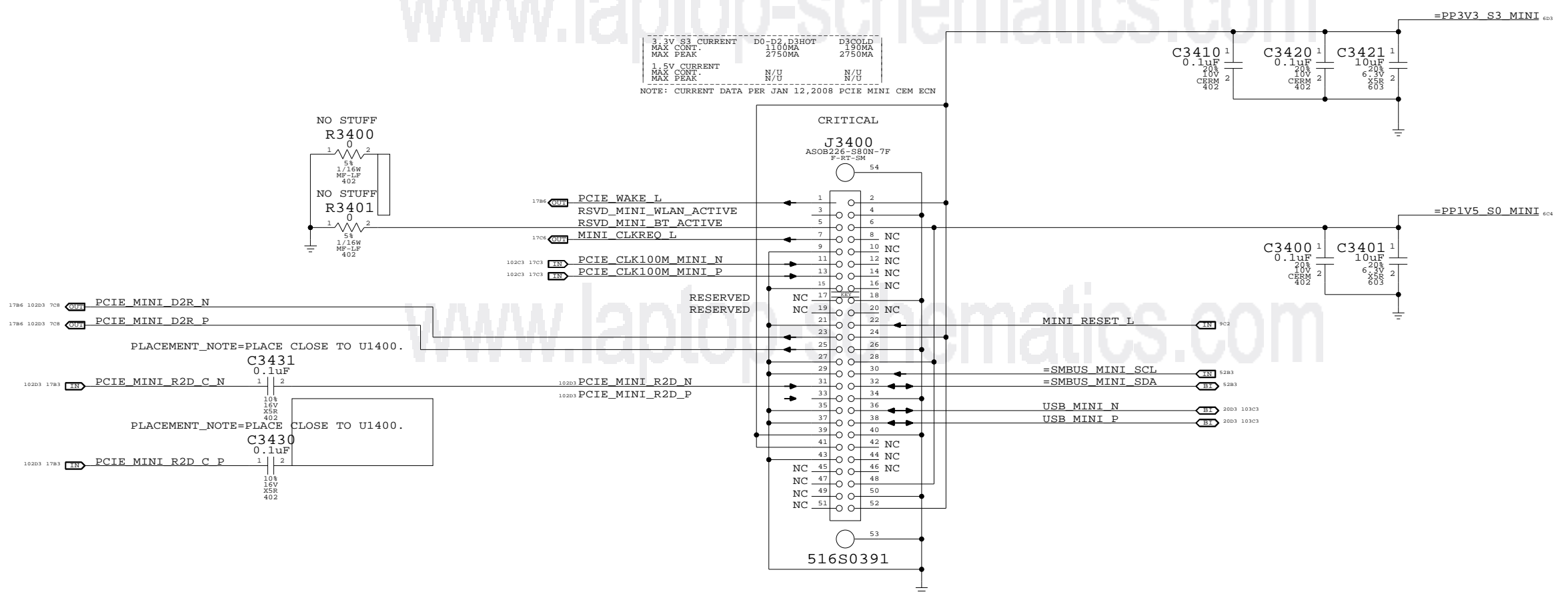
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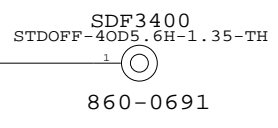
www.laptop-schematics.com

3.3V S3 CURRENT	D0-D2, D3HOT	D3COLD
MAX CONT.	1100MA	190MA
MAX PEAK	2750MA	2750MA
1.5V CURRENT	N/U	N/U
MAX CONT.	N/U	N/U
MAX PEAK	N/U	N/U

NOTE: CURRENT DATA PER JAN 12, 2008 PCIE MINI CEM ECN



STANDOFF FOR J3400
CRITICAL



PCI-E MiniCard Connector
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	34	109	

D

D

C

C

B

B

A

A

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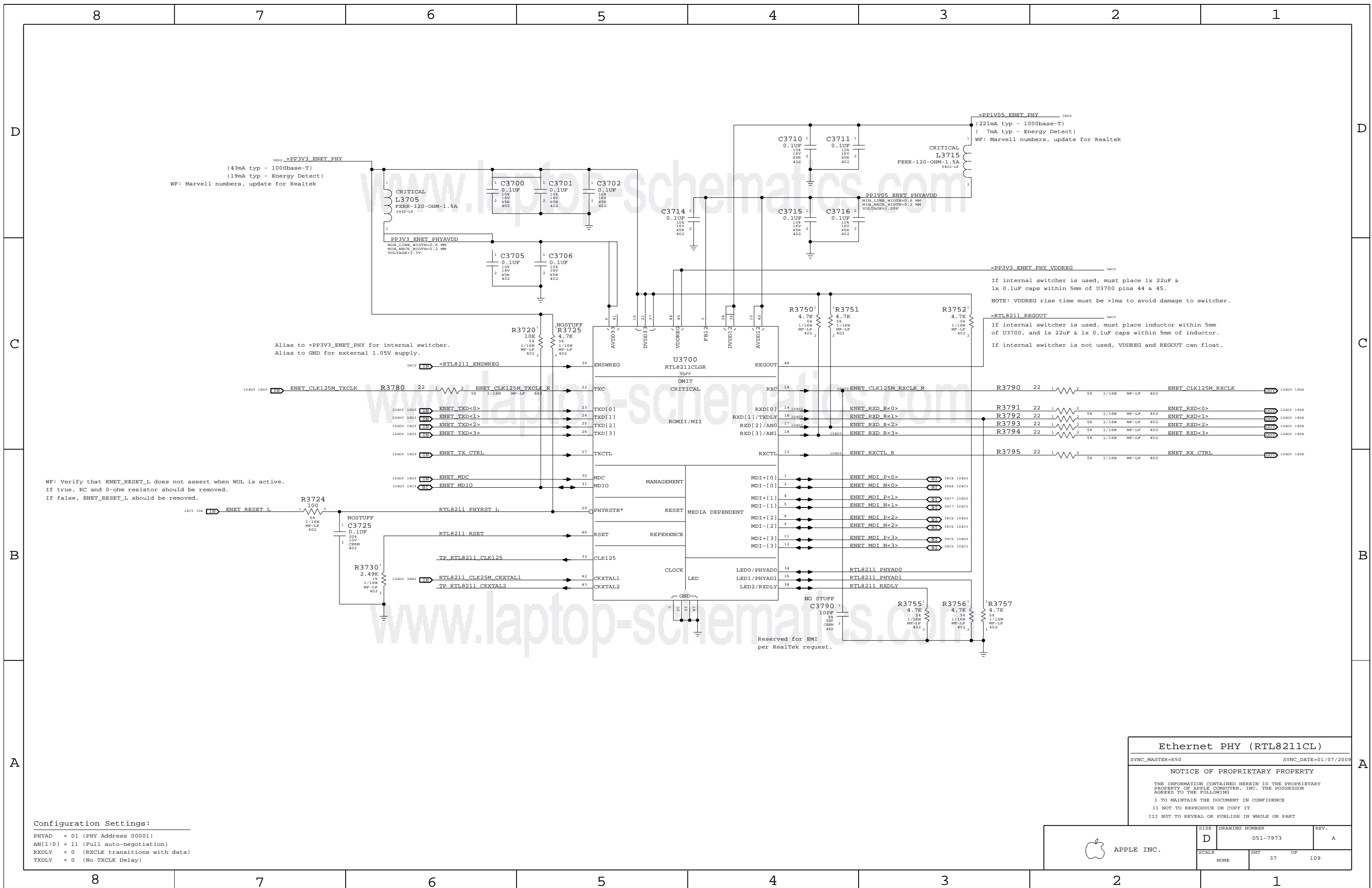
5

4

3

2

1



18D02 =PP3V3_ENET_PHY
 (43mA typ - 1000base-T)
 (19mA typ - Energy Detect)
 WF: Marvell numbers, update for Realtek

Alias to =PP3V3_ENET_PHY for internal switcher.
 Alias to GND for external 1.05V supply.

=PP3V3_ENET_PHY_VDDREG
 If internal switcher is used, must place 1x 22uF &
 1x 0.1uF caps within 5mm of U3700 pins 44 & 45.
 NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

=RTL8211_REGOUT
 If internal switcher is used, must place inductor within 5mm
 of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.
 If internal switcher is not used, VDDREG and REGOUT can float.

WF: Verify that ENET_RESET_L does not assert when WOL is active.
 If true, RC and 0-ohm resistor should be removed.
 If false, ENET_RESET_L should be removed.

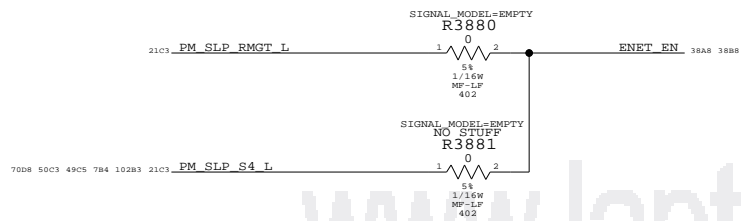
Reserved for EMI
 per Realtek request.

Configuration Settings:
 PHYAD = 01 (PHY Address 00001)
 AN[1:0] = 11 (Full auto-negotiation)
 RXDLY = 0 (RXCLK transitions with data)
 TXDLY = 0 (No TXCLK Delay)

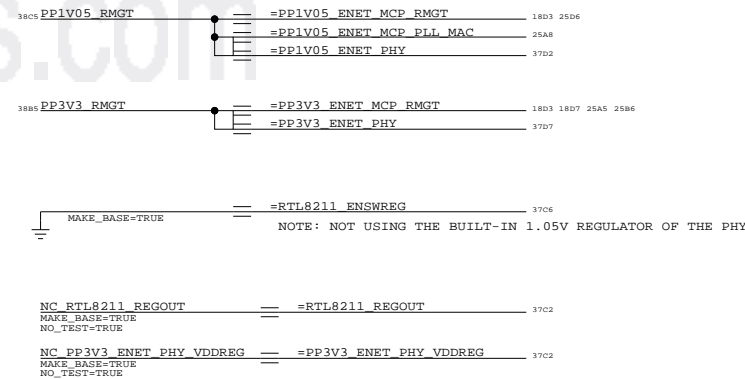
Ethernet PHY (RTL8211CL)
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	37		

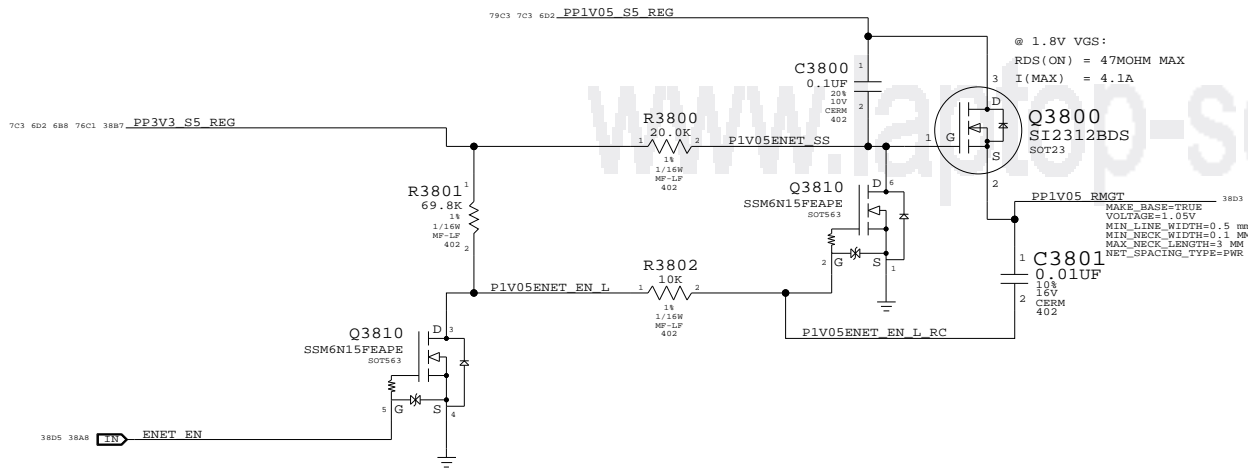
SOURCE SELECT



ENET ALIASES

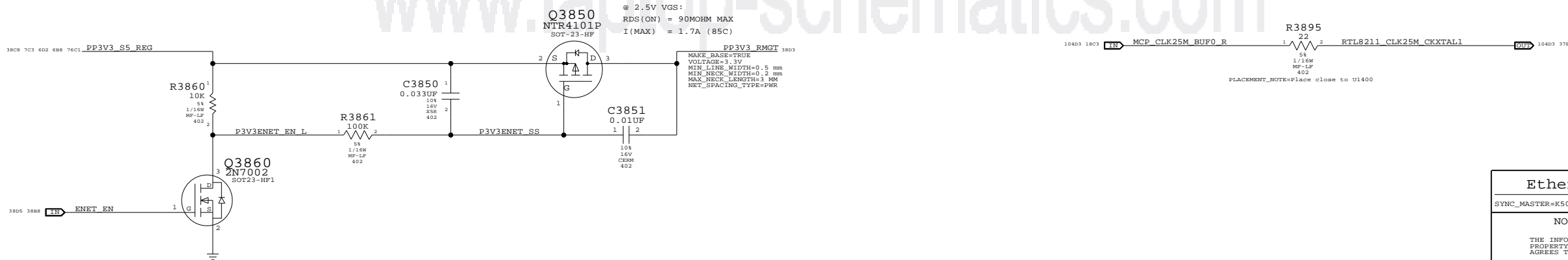


1.05V ENET FET



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



Ethernet & AirPort Support
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	38		

D

D

C

C

B

B

A

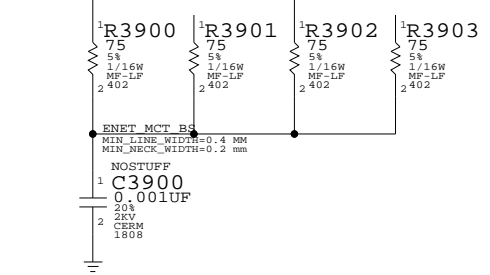
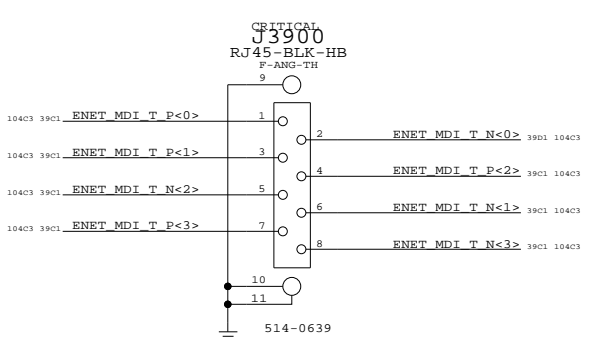
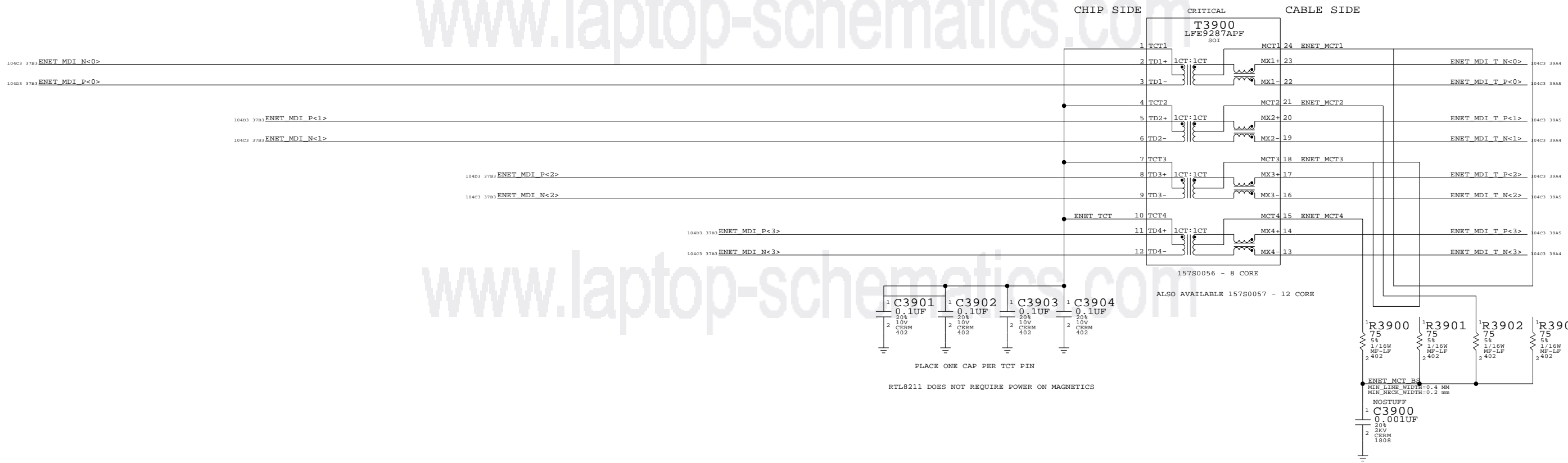
A

NOTE: DELTA RECOMMENDS CENTER-TAP BE FLOATING WHEN USING REALTEK PHY.

www.laptop-schematics.com

www.laptop-schematics.com

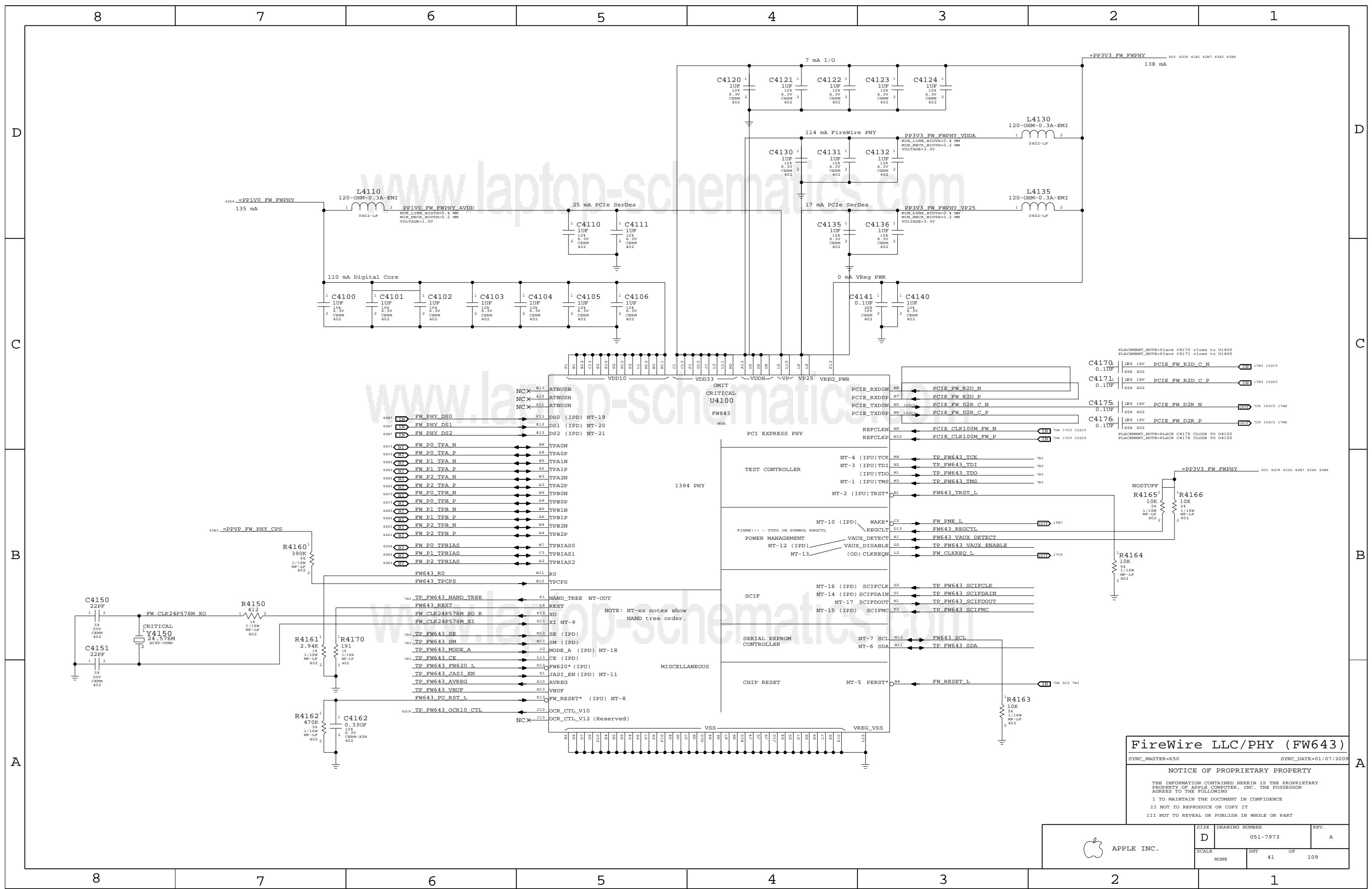
www.laptop-schematics.com



NOTE: BOB SMITH TERMINATION FOR EMC INVESTIGATION.

ETHERNET CONNECTOR
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT		OF
NONE	39		109



FireWire LLC/PHY (FW643)

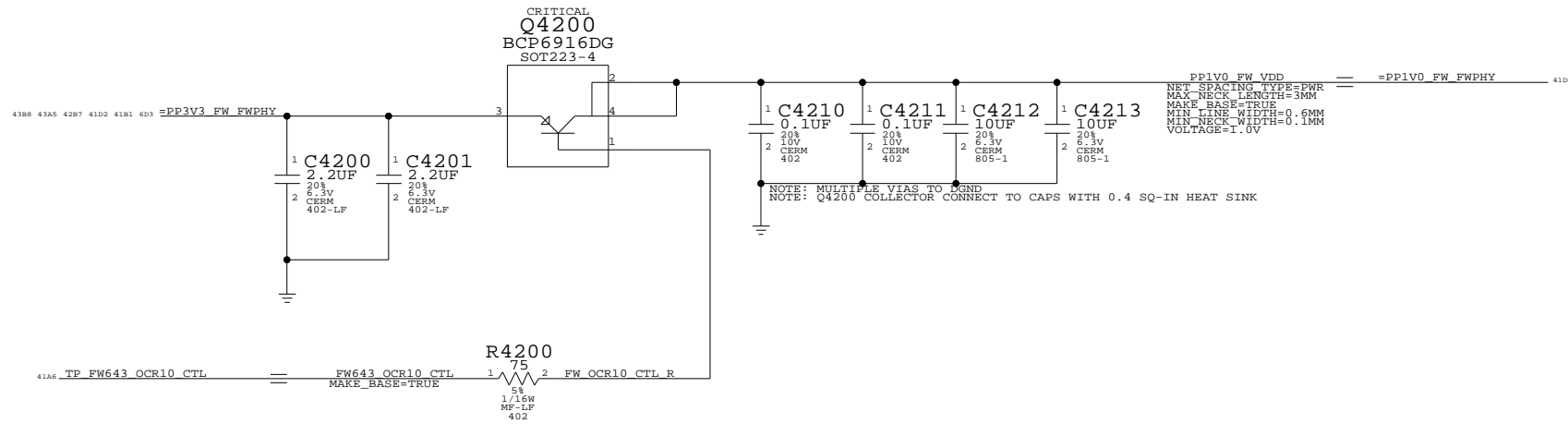
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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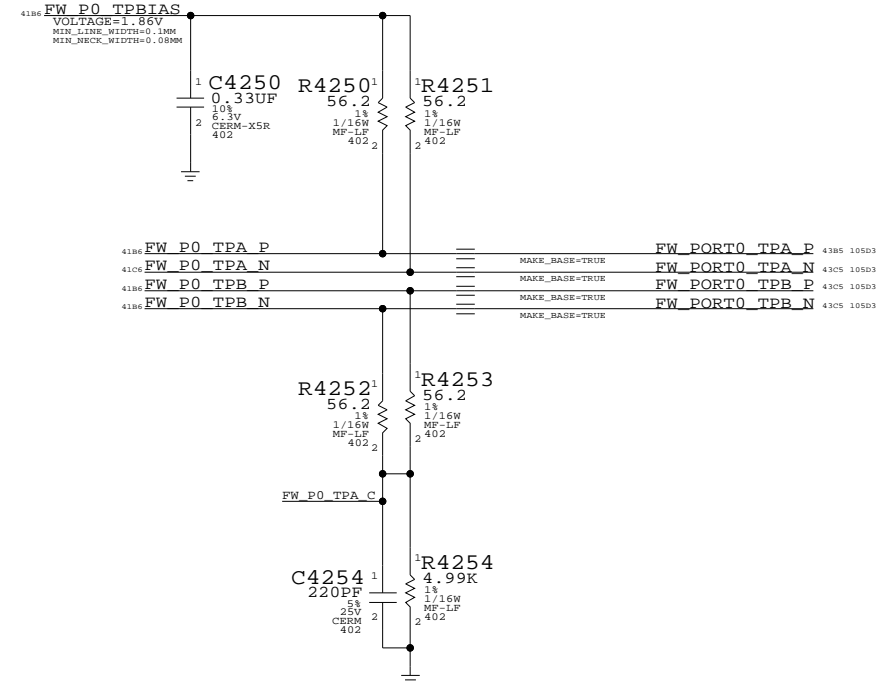
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SCALE	SHT	OF	
NONE	41	109	

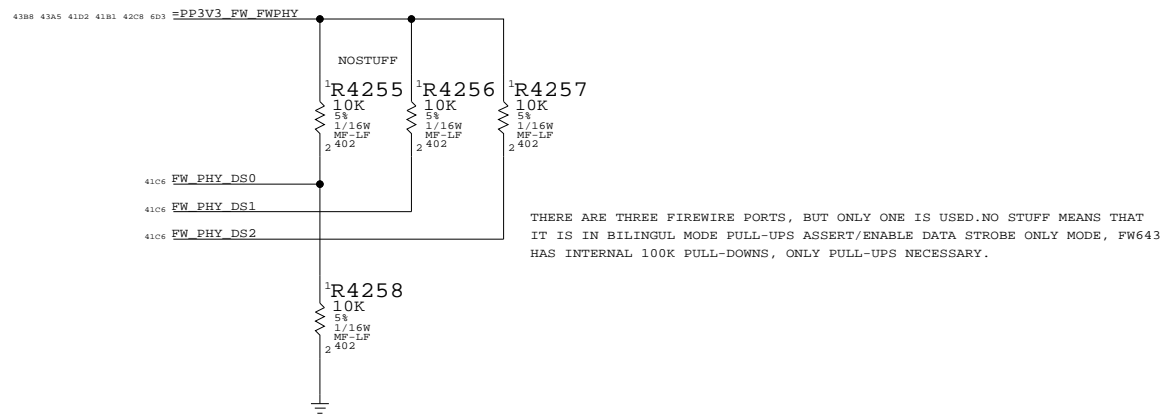
FW643 1.0V GENERATION



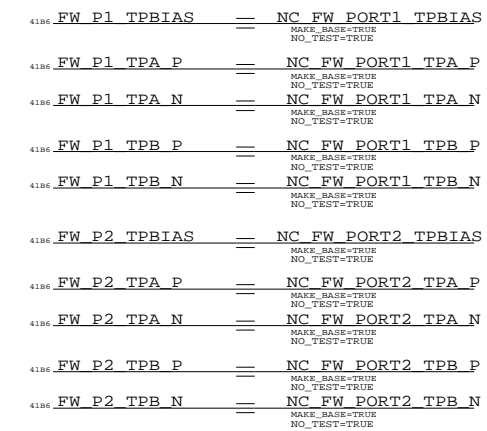
Termination
Place close to FireWire PHY



1394 PHY DATA/STROBE OPTIONS



2ND & 3RD TPA/TPB PAIR UNUSED



NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

FW: 1394B MISC

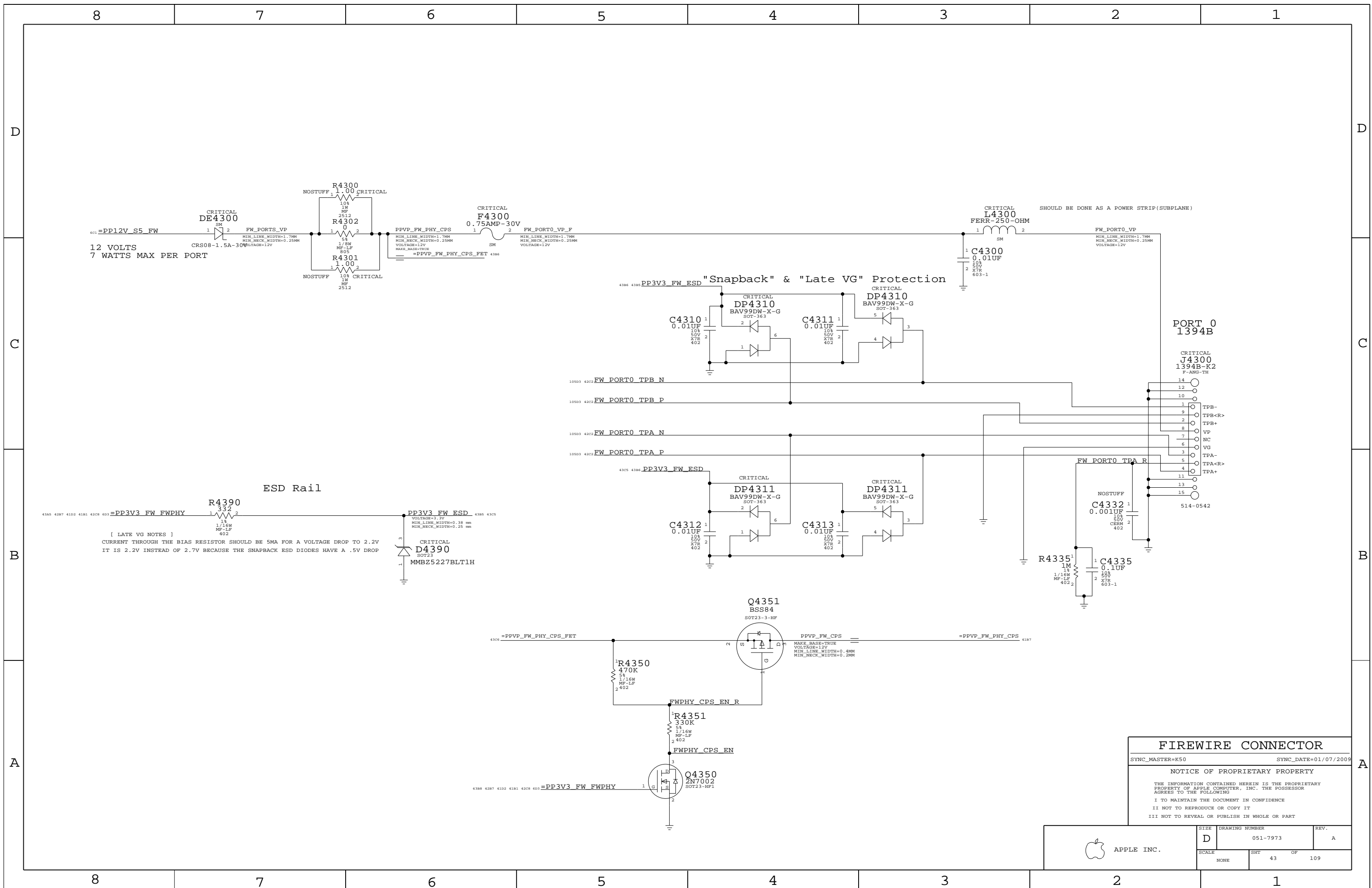
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SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	42	109



8 7 6 5 4 3 2 1

D

D

C

C

B

B

A

A

12 VOLTS
7 WATTS MAX PER PORT

SHOULD BE DONE AS A POWER STRIP (SUBPLANE)

ESD Rail

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

"Snapback" & "Late VG" Protection

PORT 0
1394B

CRITICAL
J4300
1394B-K2
P-ANG-TH

14
12
10
9
8
7
6
5
4
3
2
1
TPB-
TPB-<R>
TPB+
VP
NC
VG
TPA-
TPA-<R>
TPA+
514-0542

FIREWIRE CONNECTOR

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

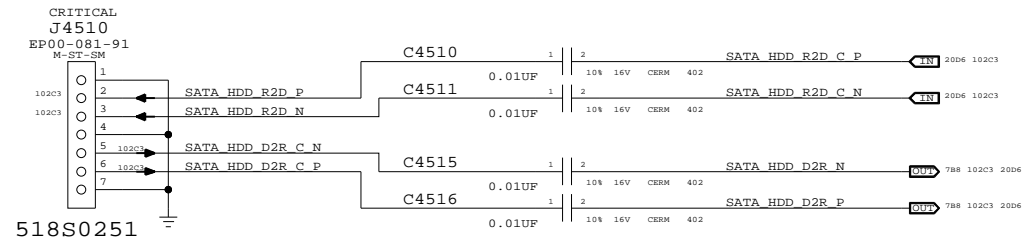
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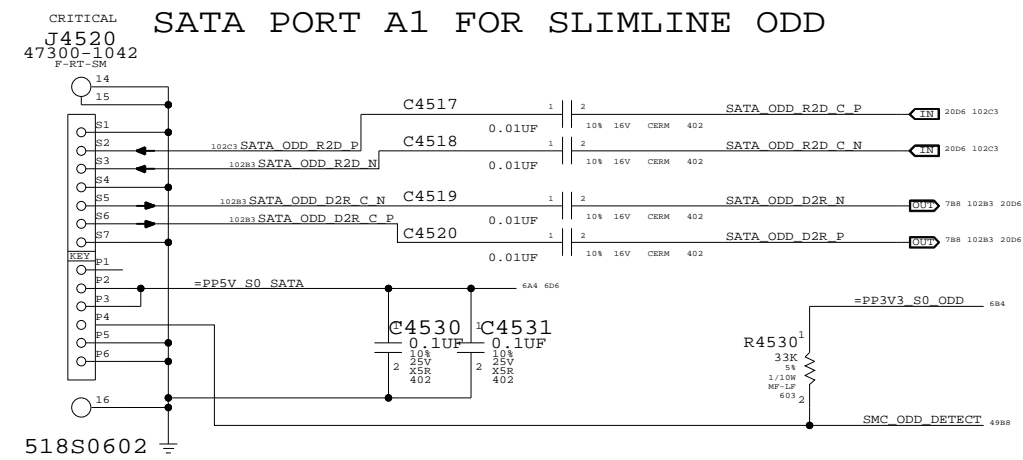
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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	43	109	

8 7 6 5 4 3 2 1

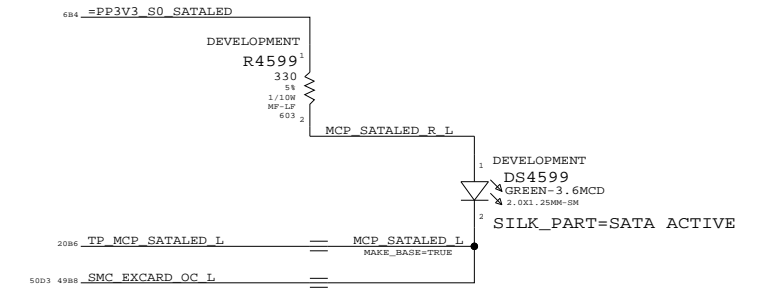
SATA PORT A0 FOR HDD



SATA PORT A1 FOR SLIMLINE ODD



SATA Activity LED



SATA Connectors

SYNC_MASTER=k50 SYNC_DATE=01/07/2009

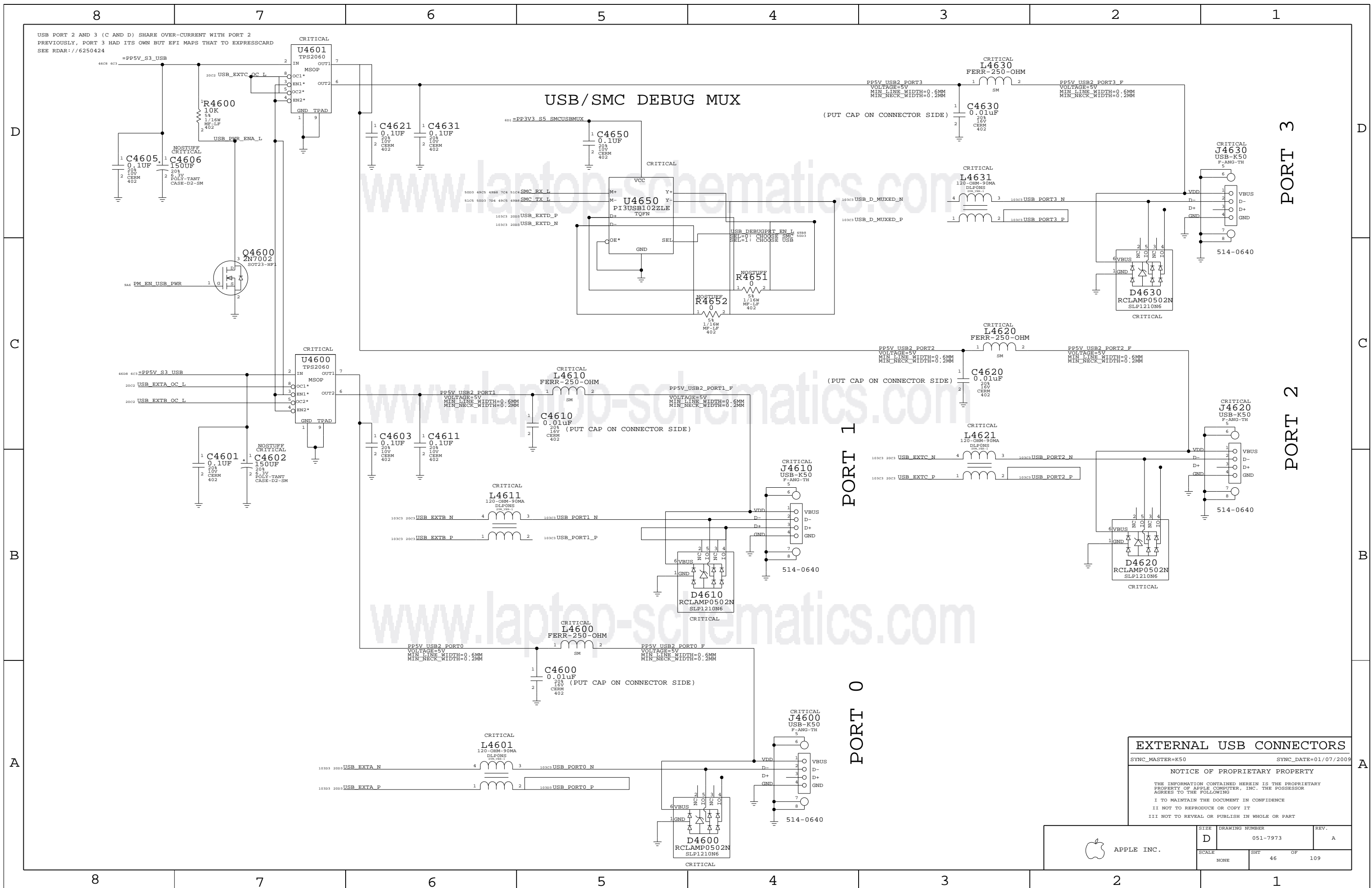
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT 45 OF 109	
NONE		



USB PORT 2 AND 3 (C AND D) SHARE OVER-CURRENT WITH PORT 2
PREVIOUSLY, PORT 3 HAD ITS OWN BUT EFI MAPS THAT TO EXPRESSCARD
SEE RDAR://6250424

USB/SMC DEBUG MUX

EXTERNAL USB CONNECTORS

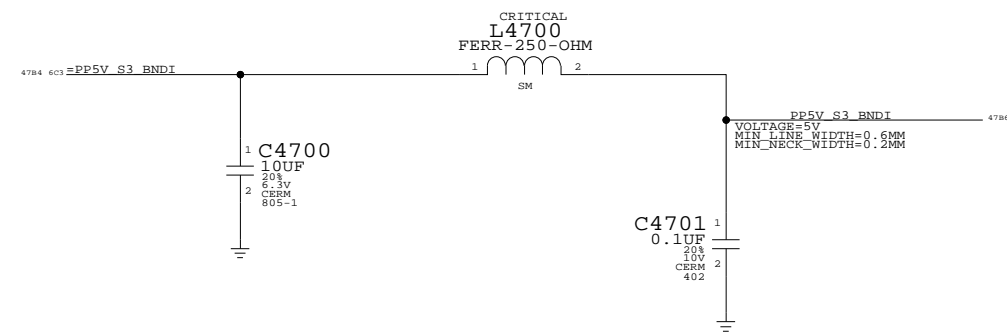
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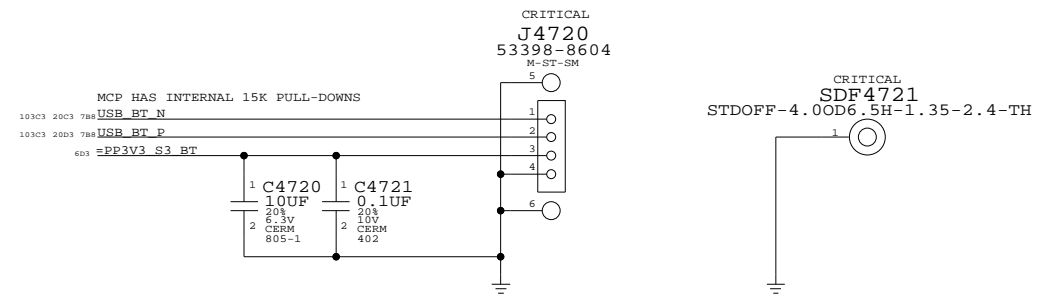
 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	46		

CAMERA POWER FILTERING

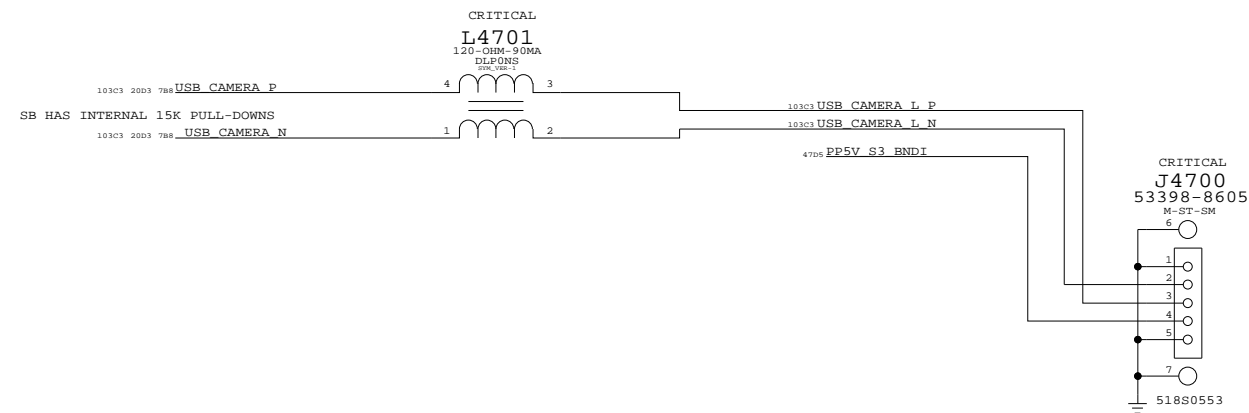


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

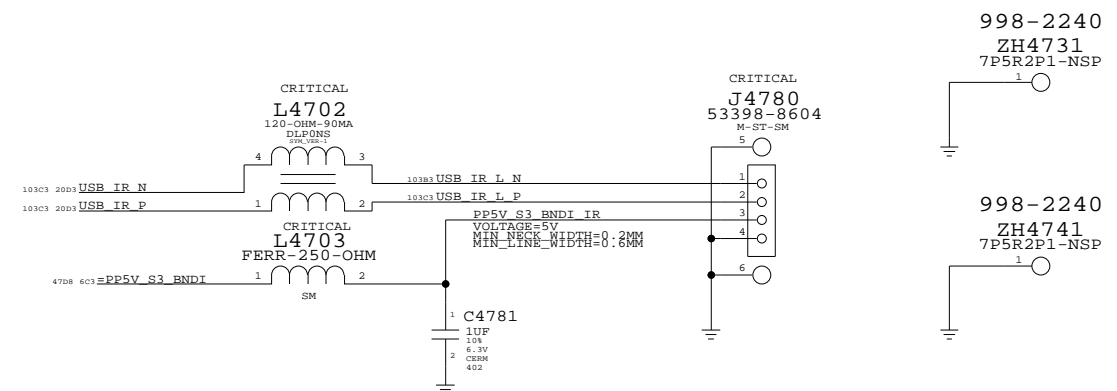
K37L (BLUETOOTH) CONNECTOR



CAMERA CONNECTOR



IR RECEIVER



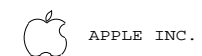
Internal USB Connections

SYNC_MASTER=k51 SYNC_DATE=07/09/2008

NOTICE OF PROPRIETARY PROPERTY

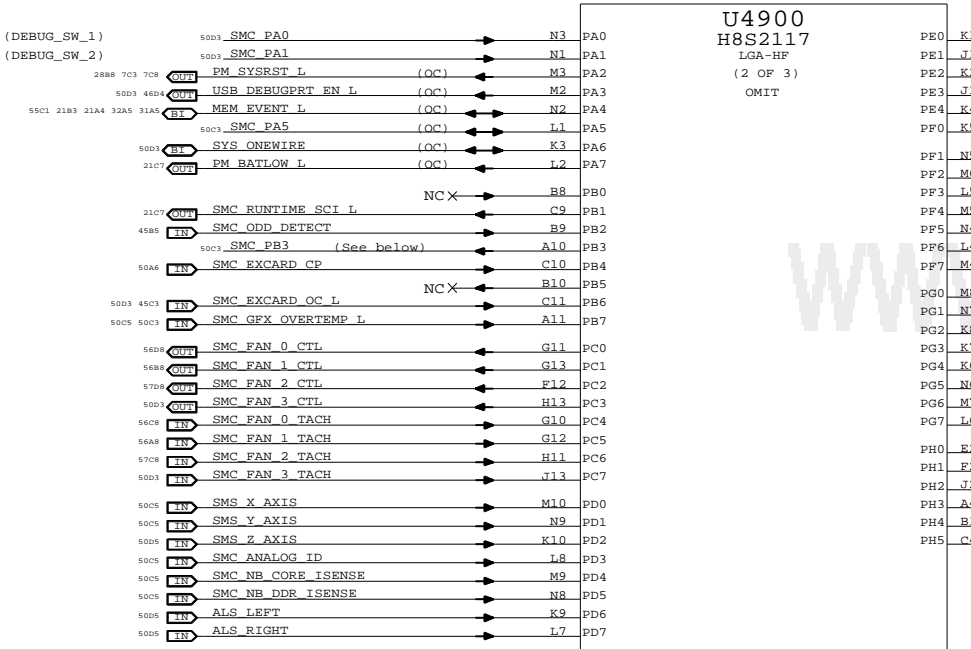
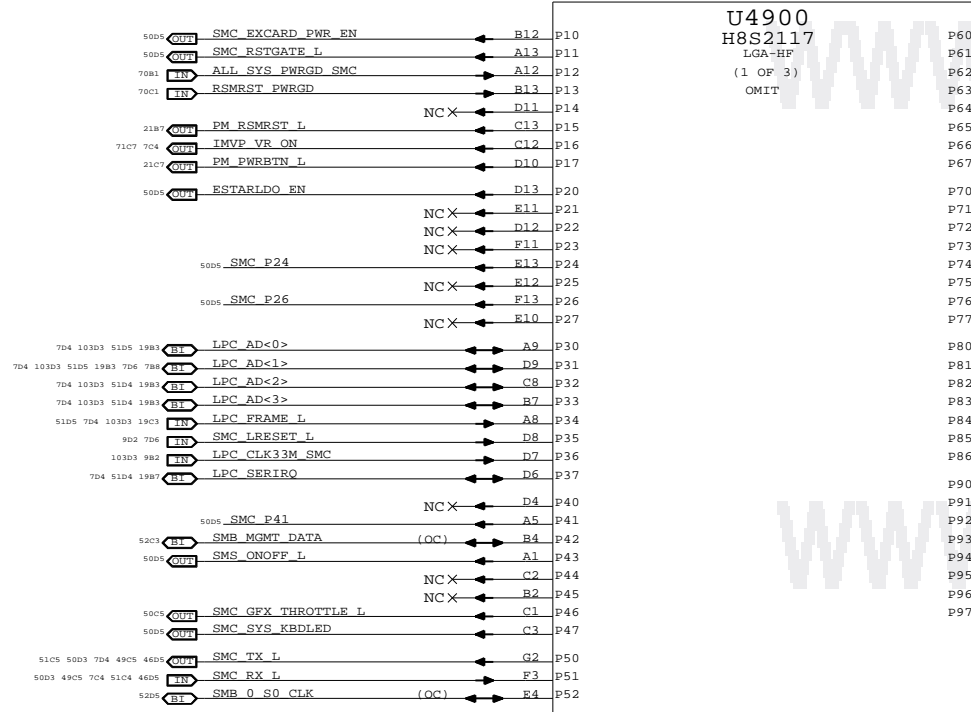
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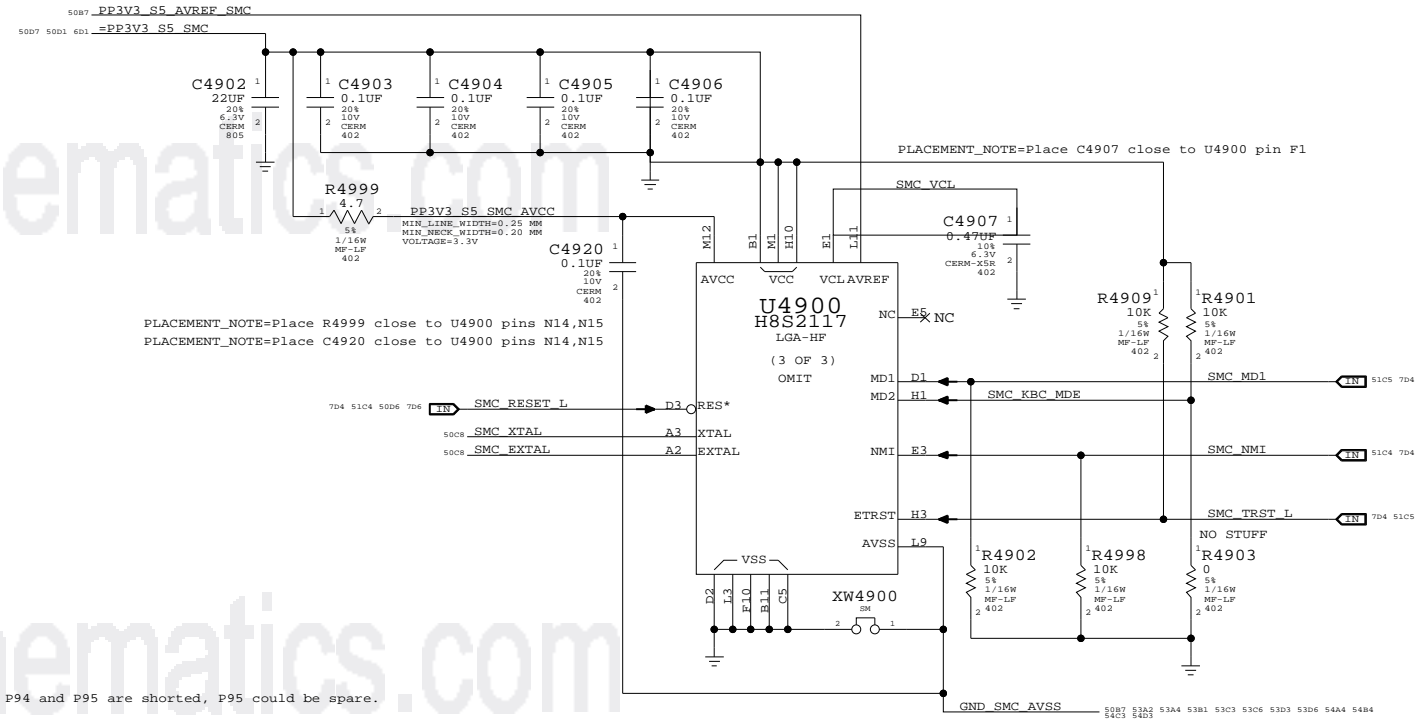


SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	47	109

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

BROKE SYNC FROM T18 ON 7/1/08; K50 NOW MASTER

SMC

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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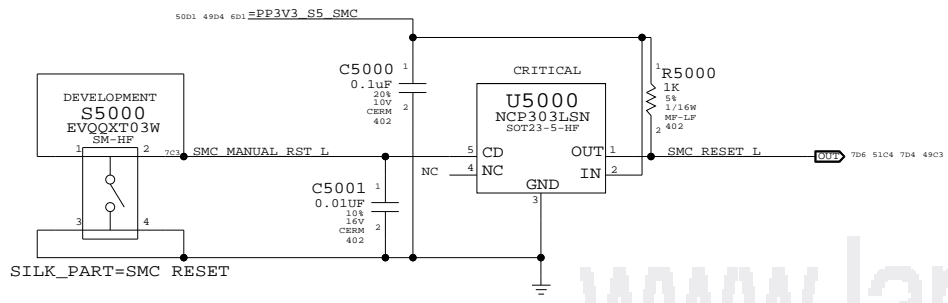
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

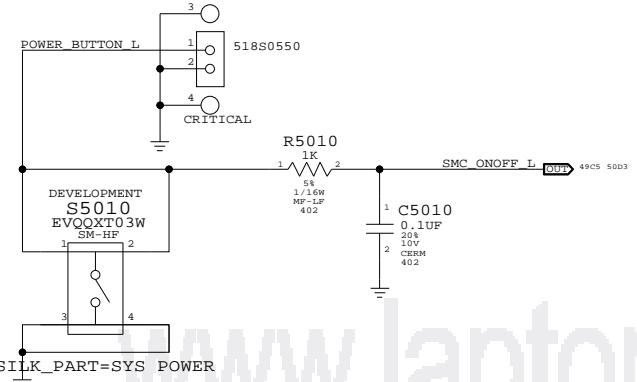
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	49		

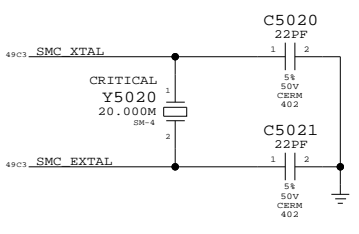
SMC Reset Button / Brownout Detect



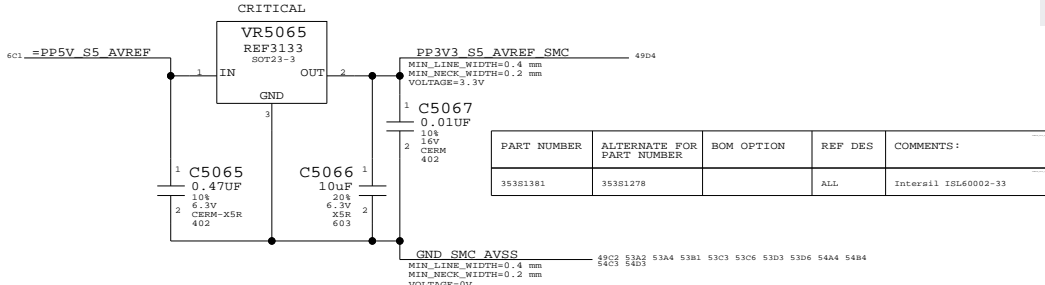
POWER BUTTON
SILK_PART=PWR BTN



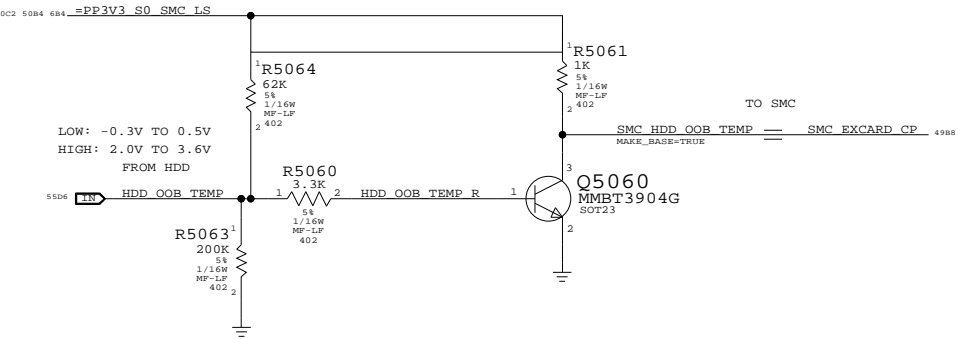
SMC Crystal Circuit



SMC AVREF Supply



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



UNUSED TP/NC ALIASES - PORT D - INTERNAL PULLUPS

- 49A8 SMS_Z_AXIS == NC_SMS_Z_AXIS
- 49A8 ALS_LEFT == TP_ALS_LEFT
- 49A8 ALS_RIGHT == TP_ALS_RIGHT

UNUSED TP/NC ALIASES

- 49A5 ALS_GAIN == NC_ALS_GAIN
- 49D5 SMC_PM_G2_EN == TP_SMC_PM_G2_EN
- 49C8 SMC_SYS_KBDLED == TP_SMC_SYS_KBDLED
- 49D8 SMC_EXCARD_PWR_EN == TP_SMC_EXCARD_PWR_EN
- 49C8 SMS_ONOFF_L == TP_SMS_ONOFF_L
- 49D8 SMC_RSTGATE_L == TP_SMC_RSTGATE_L
- 49C8 SMC_P24 == TP_SMC_P24
- 49C8 SMC_P26 == TP_SMC_P26
- 49C8 SMC_P41 == TP_SMC_P41
- 49C8 ESTARLDO_EN == TP_ESTARLDO_EN

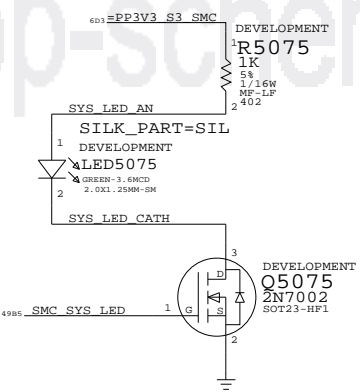
ANALOG SENSORS

- 49C5 SMC_DCIN_ISENSE == SMC_12V_S0_ISENSE
- 49C5 SMC_PBUS_VSENSE == SMC_12V_S0_VSENSE
- 49C5 SMC_BATT_ISENSE == SMC_12V_S5_ISENSE
- 49C5 SMC_NB_MISC_ISENSE == SMC_12V_S5_VSENSE
- 49A8 SMS_X_AXIS == SMC_1V5_S0_VSENSE
- 49A8 SMS_Y_AXIS == SMC_MCP_CORE_VSENSE
- 49A8 SMC_NB_DDR_ISENSE == SMC_1V5_S0_ISENSE
- 49A8 SMC_NB_CORE_ISENSE == SMC_MCP_CORE_ISENSE

MISC. SIGNAL ALIASES

- 49A8 SMC_ANALOG_ID == ACDC_TEMP
- 50C3 49B8 SMC GFX_OVERTEMP_L == MXM_ALERT_L
- 49C8 SMC GFX_THROTTLE_L == MXM_PWR_LEVEL
- 49B5 SMC_MCP_SAFE_MODE == MCP_SPKR

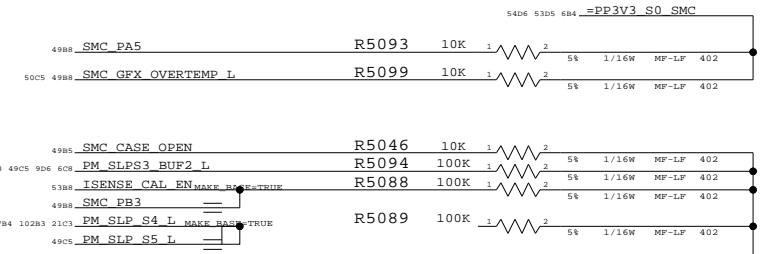
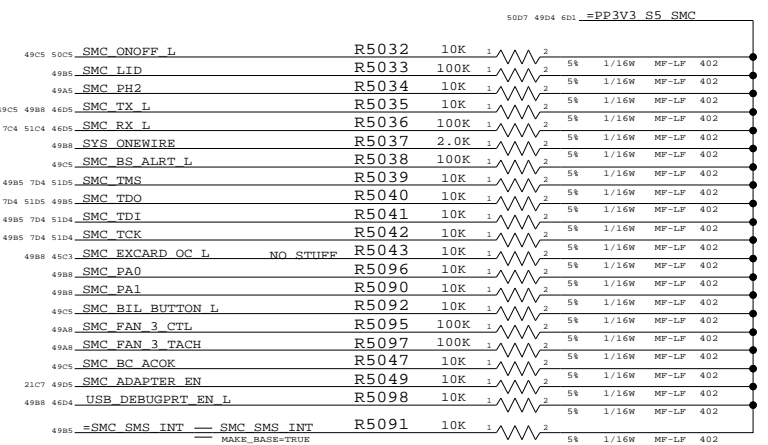
SIL: FOR DEVELOPMENT USE ONLY



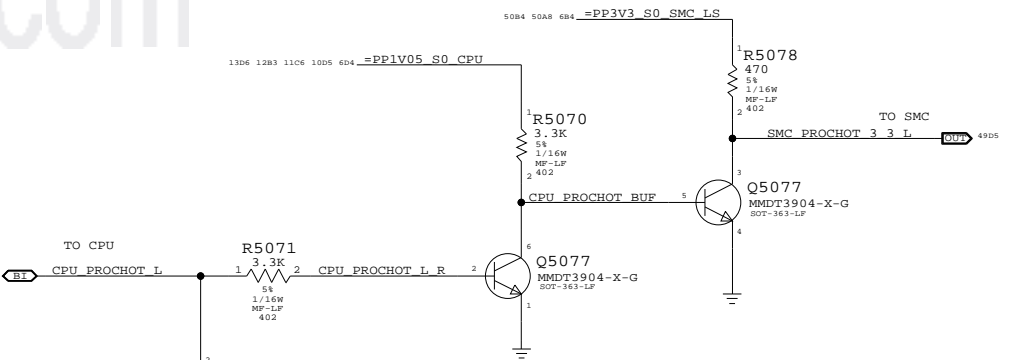
SMC SYS LED



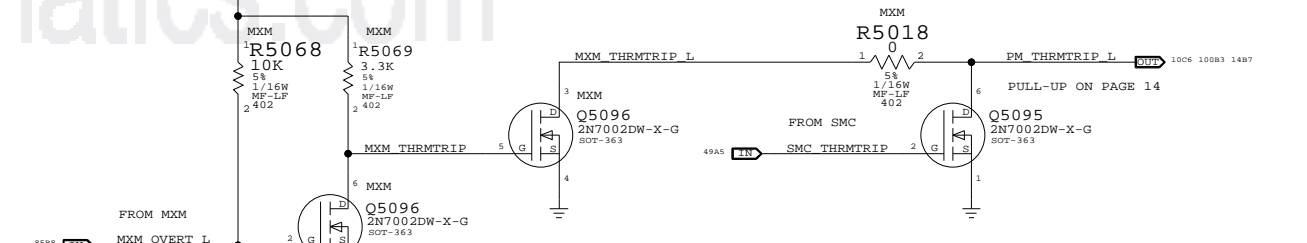
SMC SYS LED



SMC PROCHOT 3.3V LEVEL SHIFTING

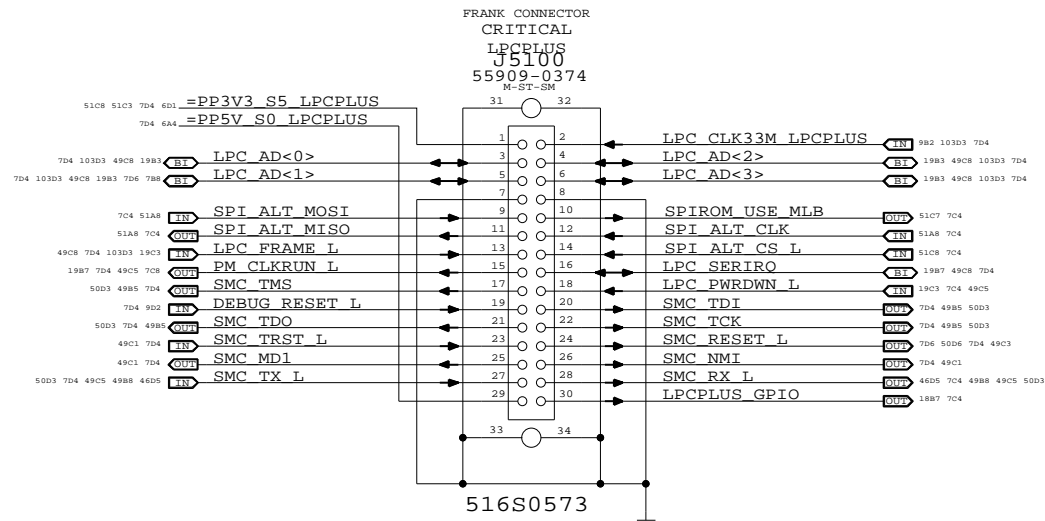


SMC & MXM THERMTRIP LEVEL SHIFTING

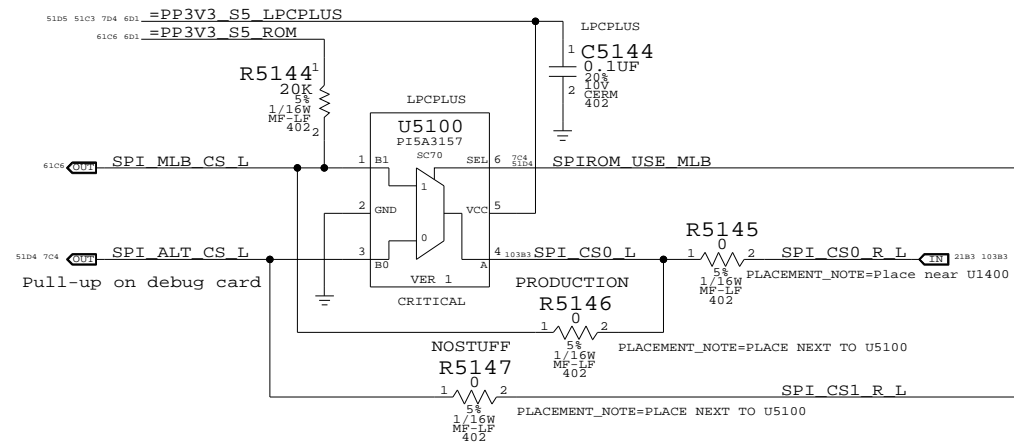


SMC Support
 SYNC_MASTER=k50 SYNC_DATE=01/07/2009
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LPC+SPI Connector

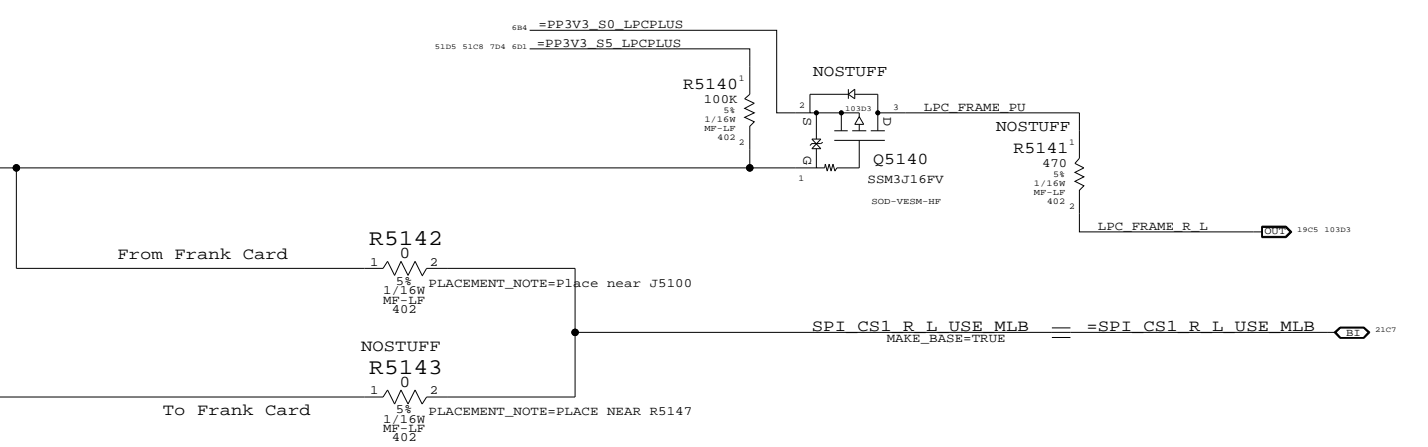


Alternate SPI ROM Support



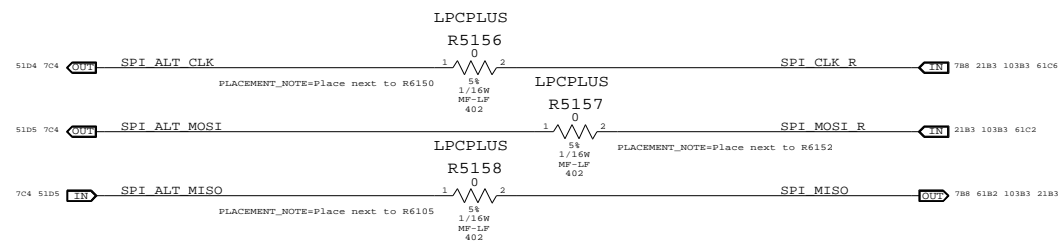
MCP79 Internal SPI MUX Support

Not supported in Rev A01 MCP79 silicon



MCP79 Rev A01 requires external MUX, Rev B01 should support internal MUX

SPI Bus Series Resistance Option

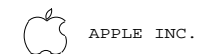


LPC+SPI Debug Connector

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

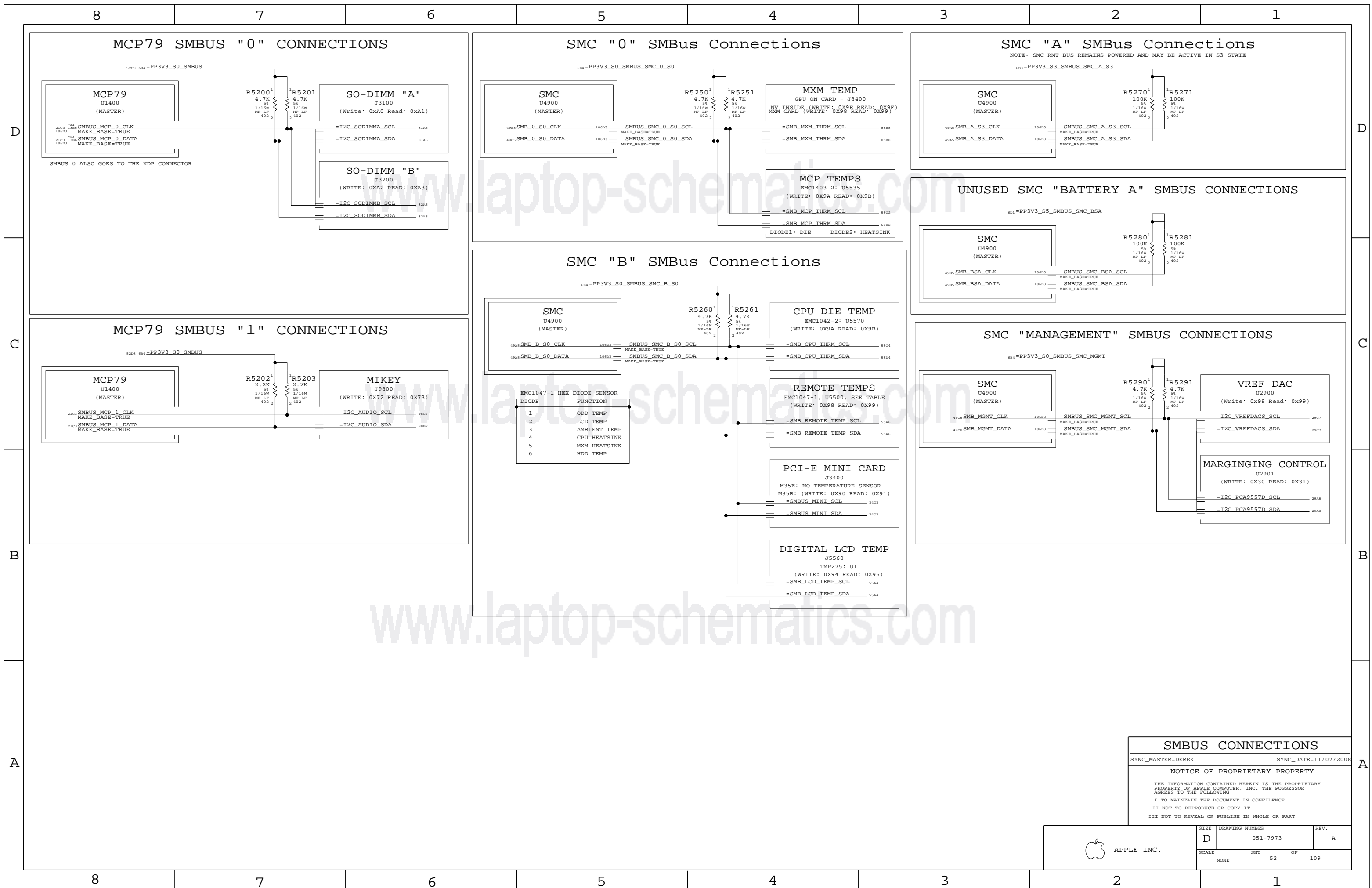
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APPLE INC.

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D	051-7973	A
SCALE	SHT	OF
NONE	51	109



MCP79 SMBUS "0" CONNECTIONS

SMC "0" SMBus Connections

SMC "A" SMBus Connections

MCP79 SMBUS "1" CONNECTIONS

SMC "B" SMBus Connections

UNUSED SMC "BATTERY A" SMBUS CONNECTIONS

SMC "MANAGEMENT" SMBUS CONNECTIONS

SMBUS CONNECTIONS

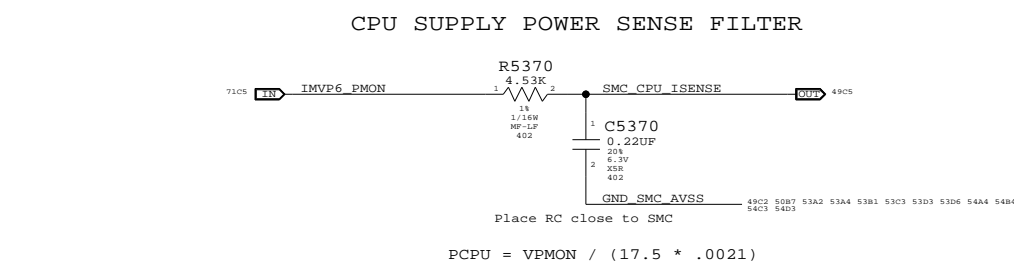
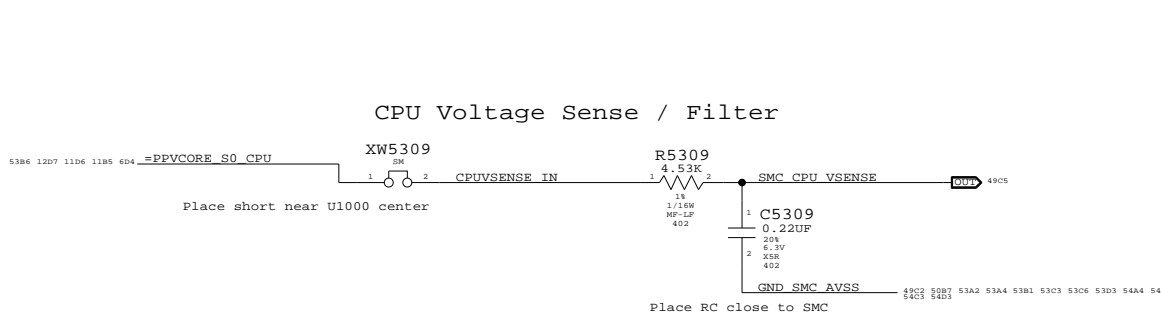
SYNC_MASTER=DEREK SYNC_DATE=11/07/2008

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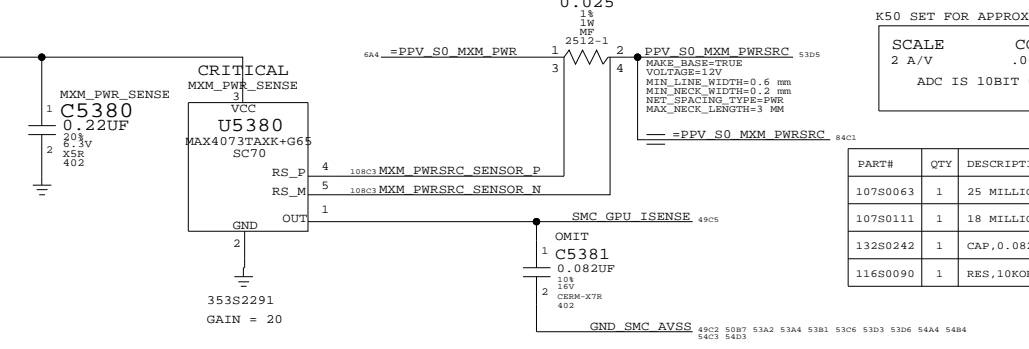
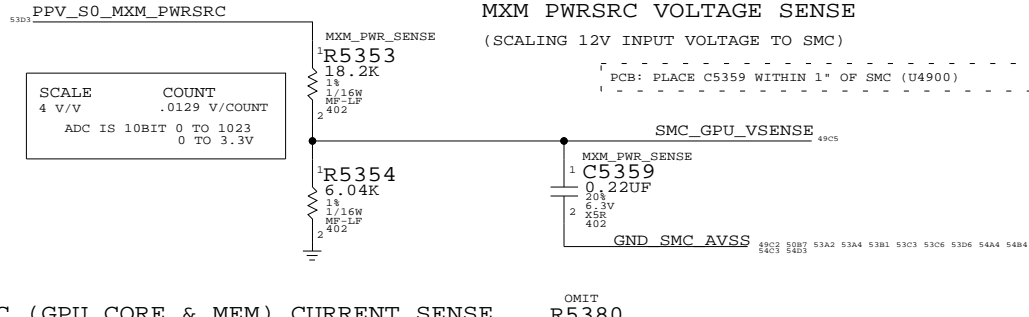
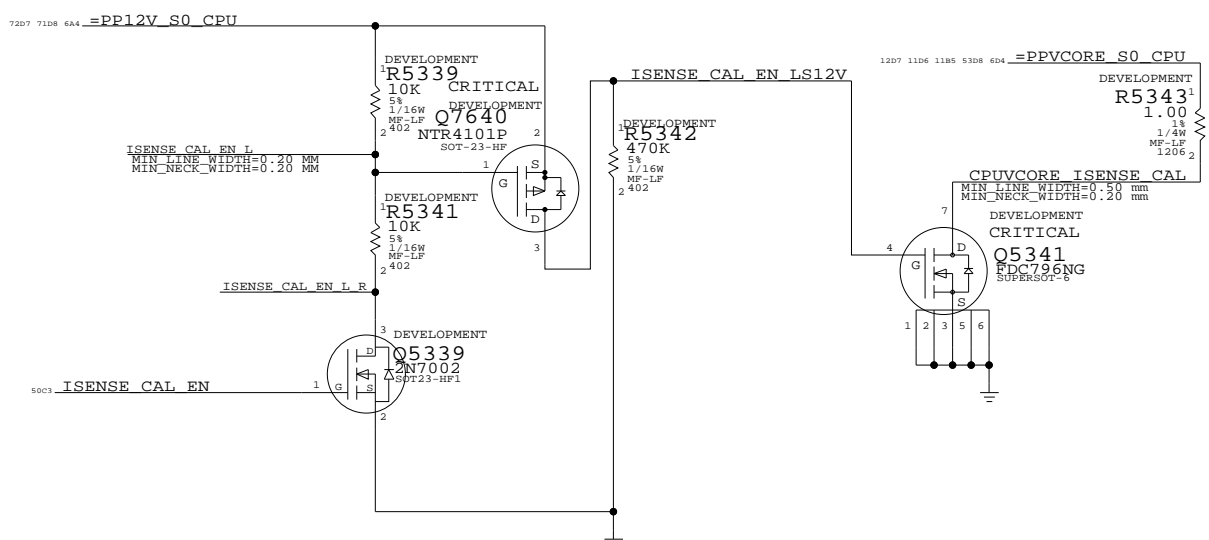


SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	52	109

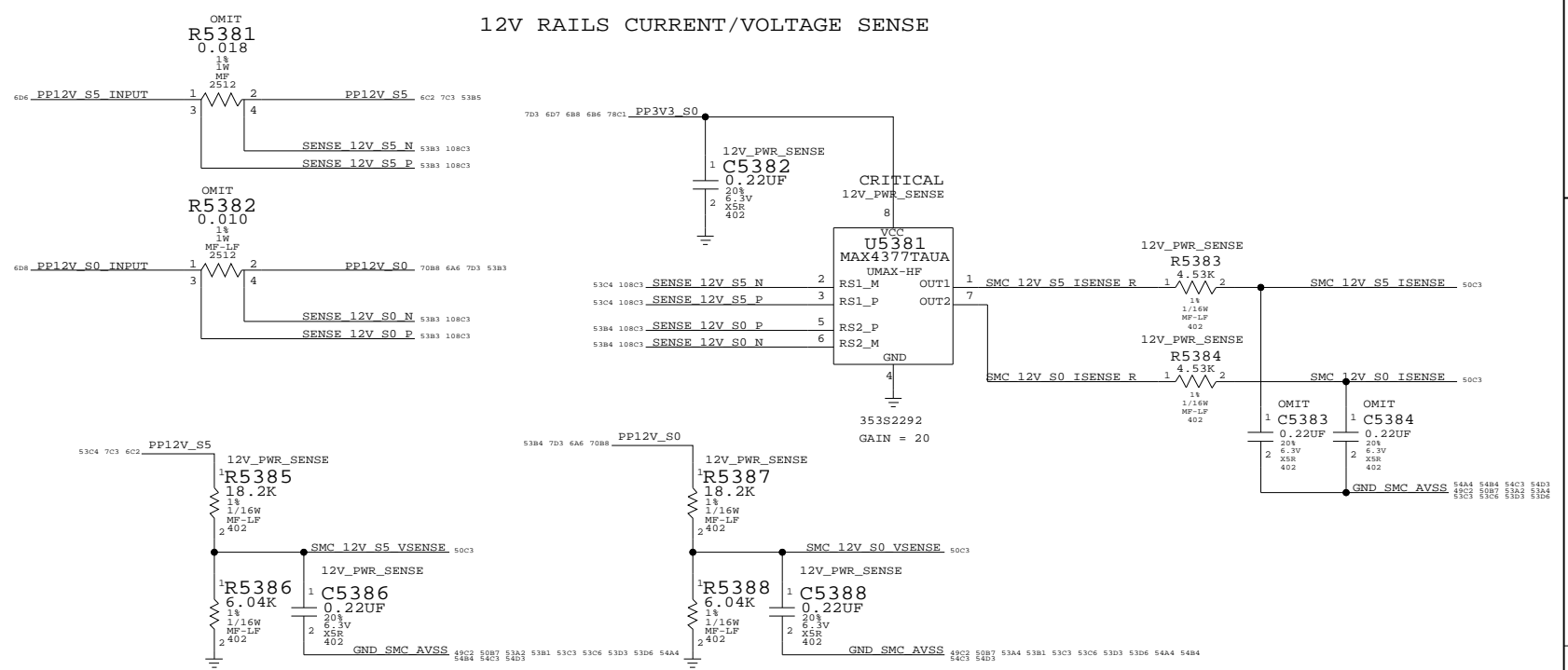


CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	K50_BETTER
107S0111	1	18 MILLIOHM	R5380	CRITICAL	24_INCH_MXM
132S0242	1	CAP,0.082UF,402	C5381	CRITICAL	MXM_PWR_SENSE
116S0090	1	RES,10KOHM,5%,402	C5381	CRITICAL	IG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	RANGE
107S0069	1	10 MILLIOHM	R5382	CRITICAL	K50_BETTER	10A
107S0112	1	8 MILLIOHM	R5382	CRITICAL	24_INCH_MXM	12.5A
107S0070	2	RES,0 OHM,2512	R5381,R5382	CRITICAL	IG	
107S0111	1	18 MILLIOHM	R5381	CRITICAL	12V_PWR_SENSE	5.5A
116S0090	2	RES,10KOHM,5%,402	C5383,C5384		IG	
132S0080	2	CAP,0.22UF,20%,6.3V,X5R,402	C5383,C5384		12V_PWR_SENSE	

12V_PWR_SENSE SHOULD BE STUFFED FOR MXM CONFIGS
 IG CONFIGS WILL NOT HAVE THE SENSORS, SO CAPS FROM THE RC FILTER BECOME RESISTORS TO GROUND (SO SMC READS 0)
 IG CONFIGS DO NOT NEED 12V POWER SENSE BECAUSE THE CONFIGURATION DOES NOT DRAW CURRENT WHICH APPROACHES THE ADC SPEC

Current & Voltage Sensing
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	53		

8

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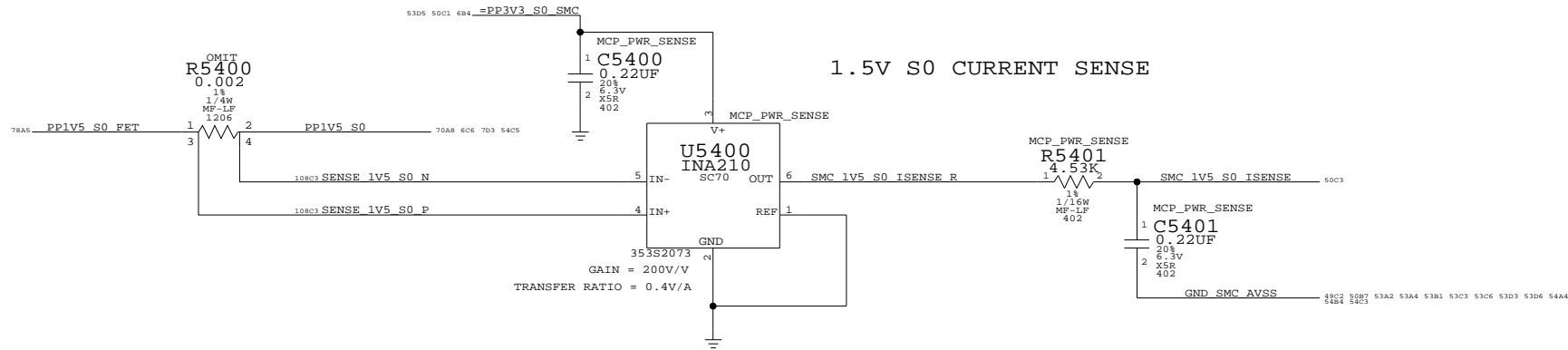
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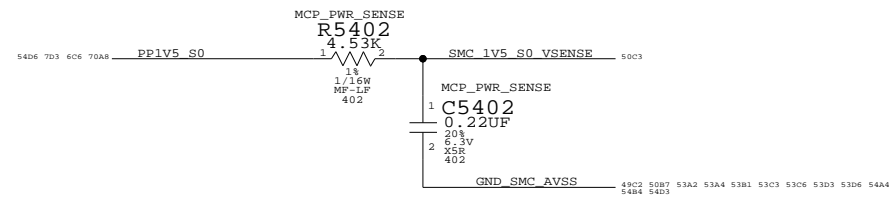
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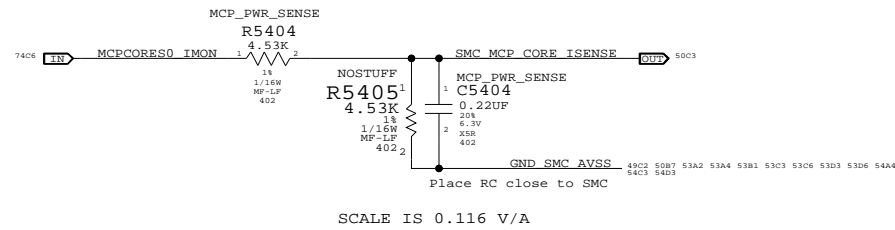
1.5V S0 CURRENT SENSE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
10480018	1	RES,2 MILLIOHM,1206	R5400	CRITICAL	MCP_PWR_SENSE
10180414	1	RES,0 OHM,1206,20MILLIOHM MAX	R5400	CRITICAL	PRODUCTION

1.5V S0 VOLTAGE SENSE

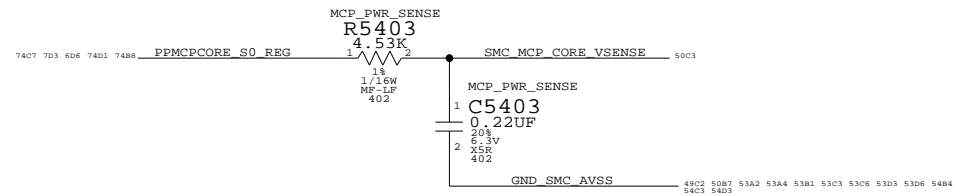


MCP CORE CURRENT SENSE



SCALE IS 0.116 V/A

MCP CORE VOLTAGE SENSE



MCP CURRENT AND VOLTAGE SENSE

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	54	109

8

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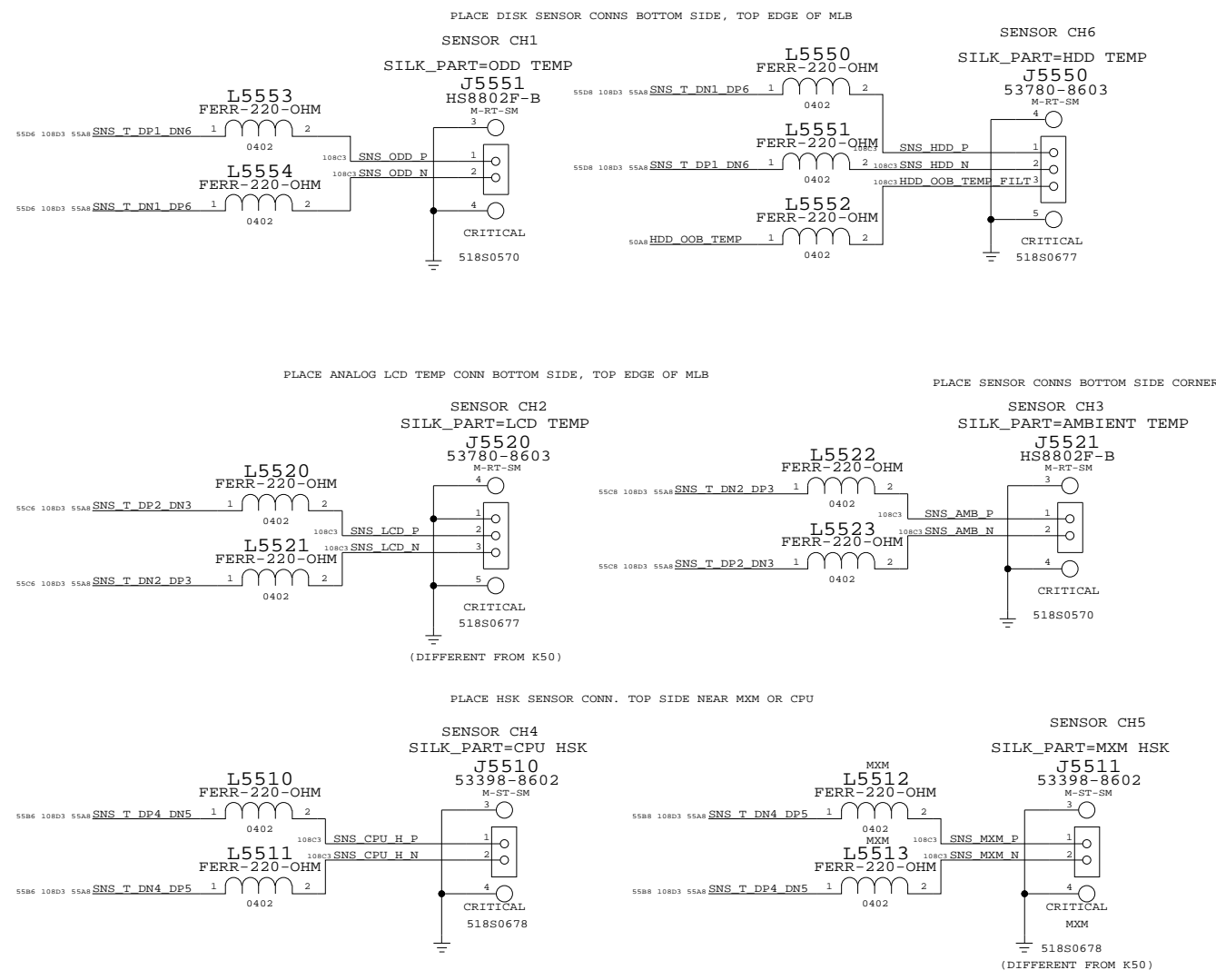
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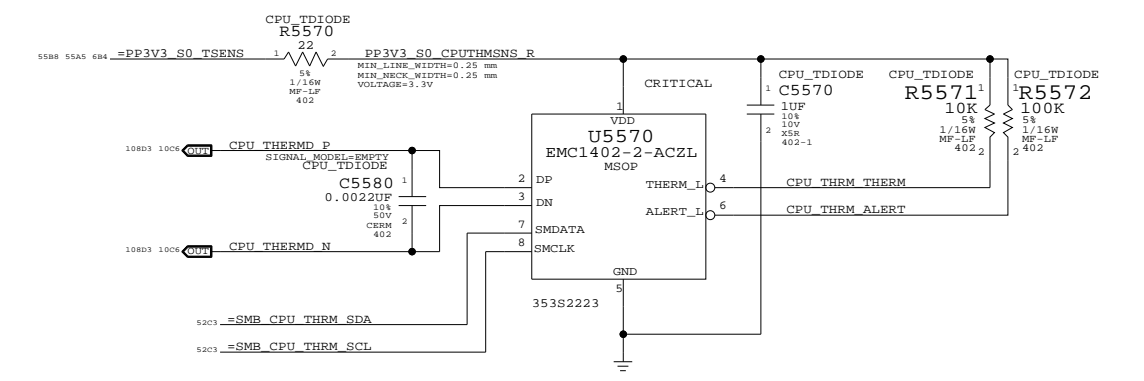
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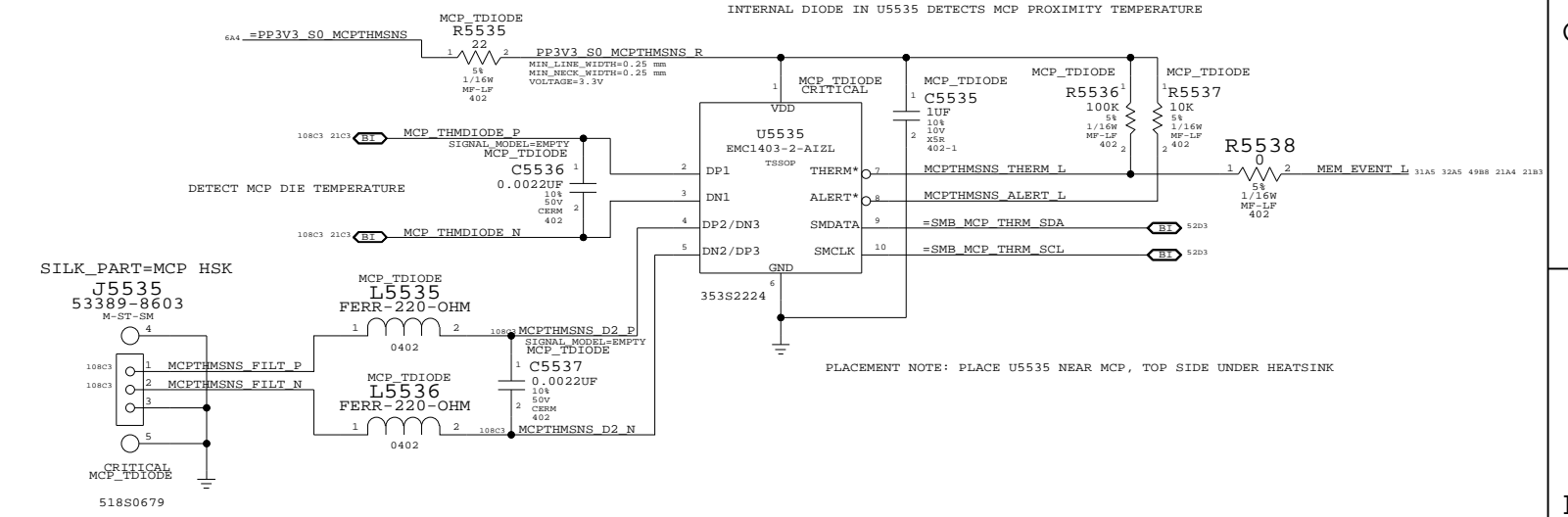
REMOTE THERMAL SENSORS HEATSINKS, AMBIENT, PANEL AND DISKS



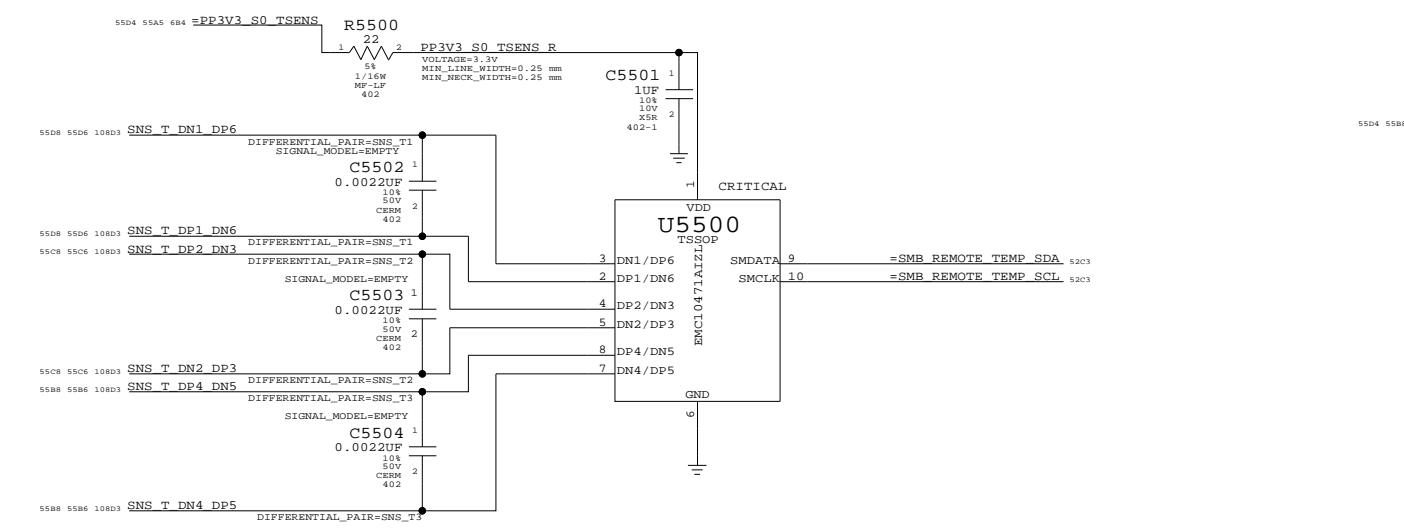
CPU T-Diode Thermal Sensor



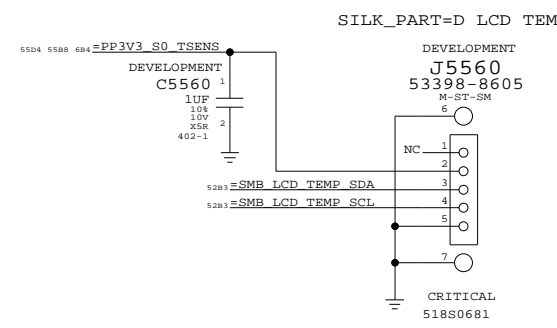
MCP T-Diode Thermal Sensor



REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)



DIGITAL LCD TEMP SENSOR



BROKE SYNC FROM K50 ON 7/9

Thermal Sensors

SYNC_MASTER=DEREK SYNC_DATE=11/07/2008

NOTICE OF PROPRIETARY PROPERTY

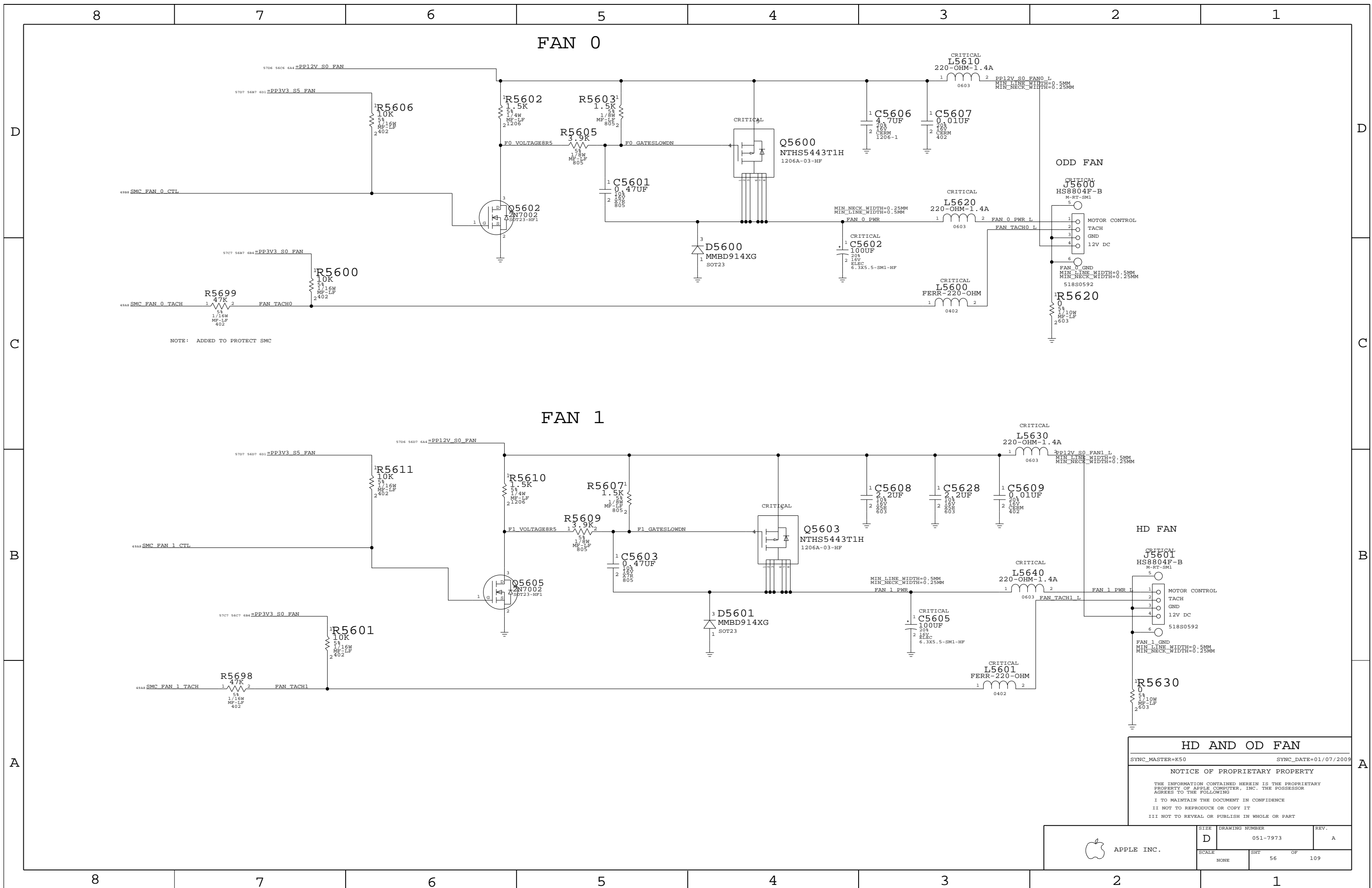
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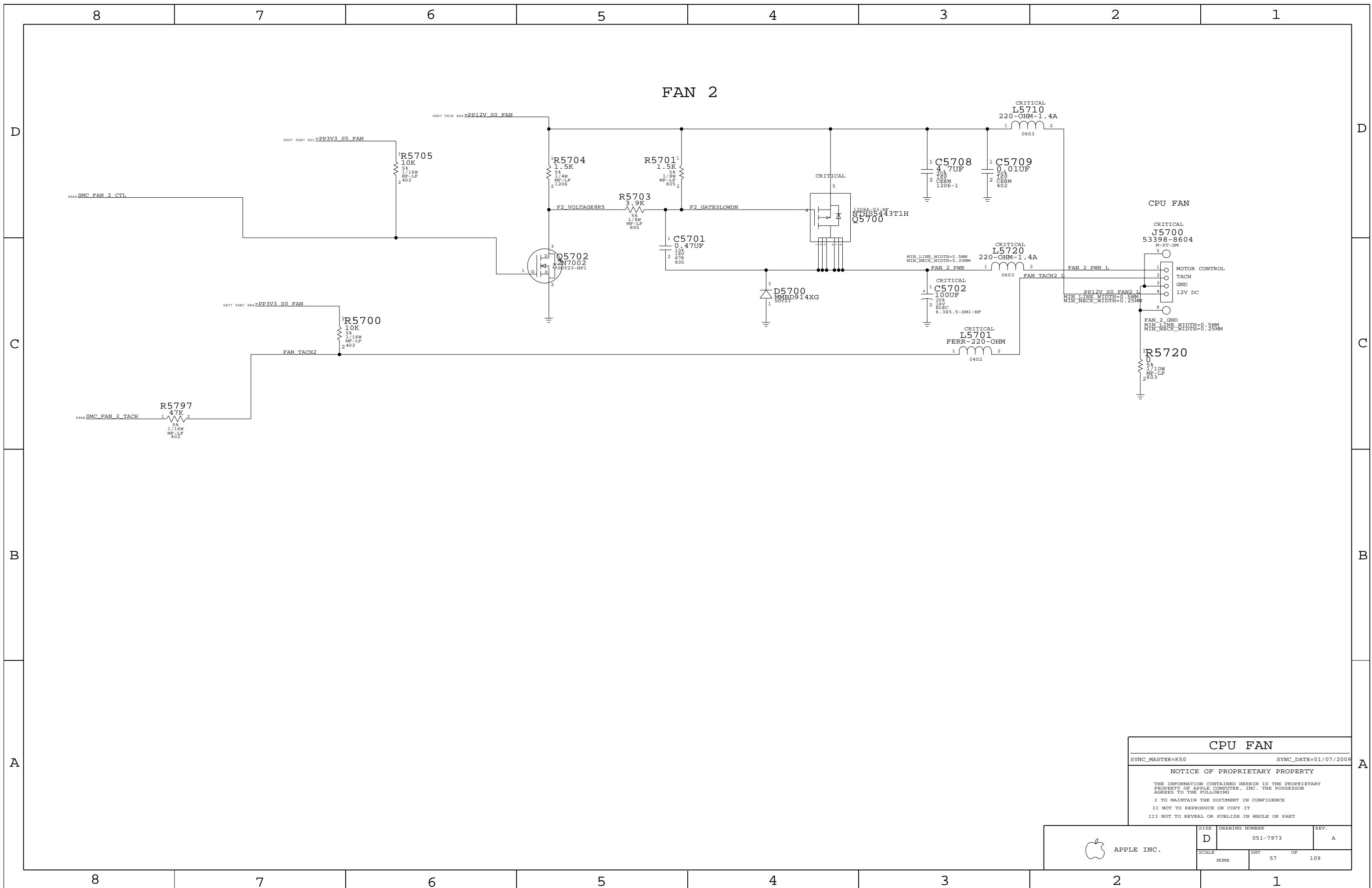
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	55		





CPU FAN

SYNC_MASTER=k50 SYNC_DATE=01/07/2009

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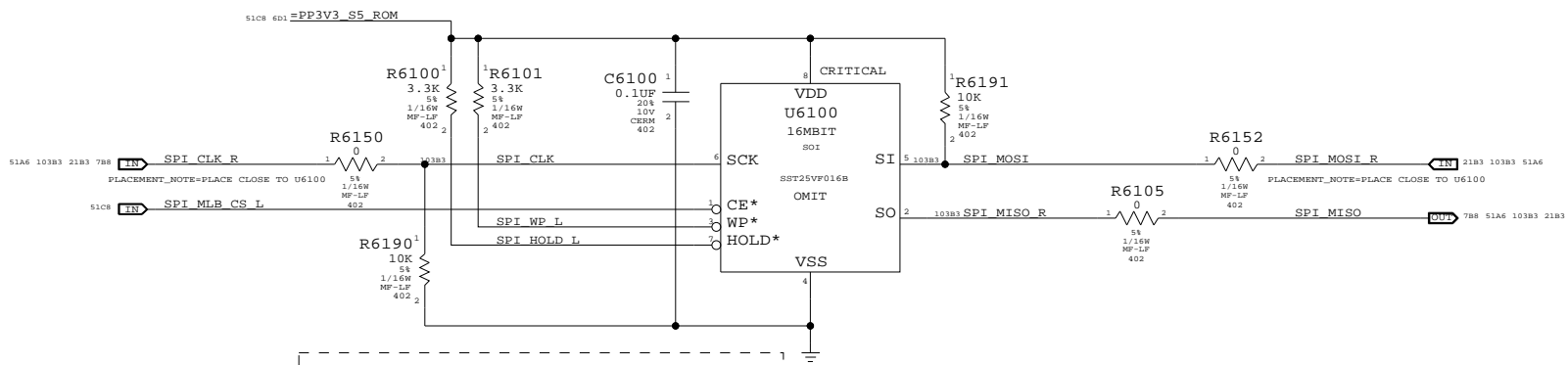
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	57	109	



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: MCP79 only issues 'READ' (0x03) commands not 'READ_FAST' (0x0B). Limits SPI bus frequency and part selection.
SST25VF016B max speed for READ command is 25MHz.

SPI ROM

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT OF		
NONE	61 OF		109

8

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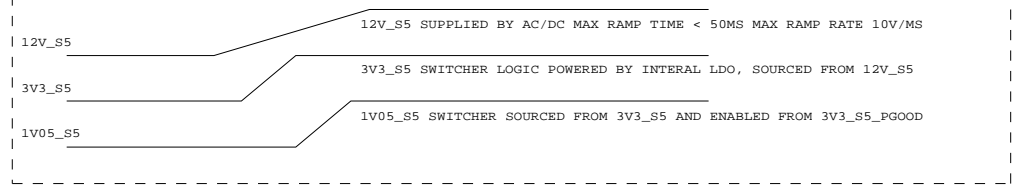
B

B

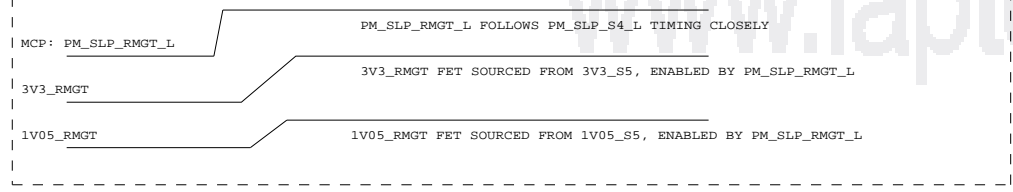
A

A

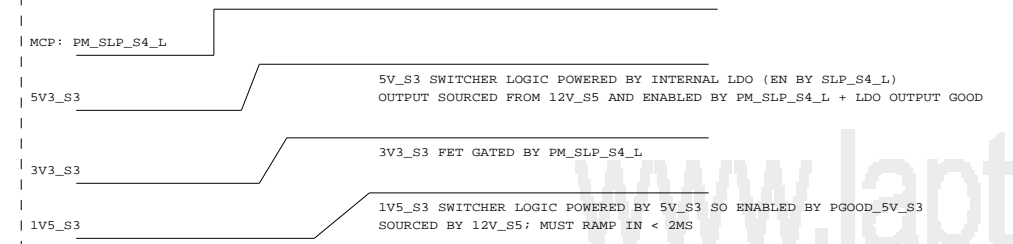
S5 POWER RAIL SEQUENCING



RMGT POWER RAIL SEQUENCING

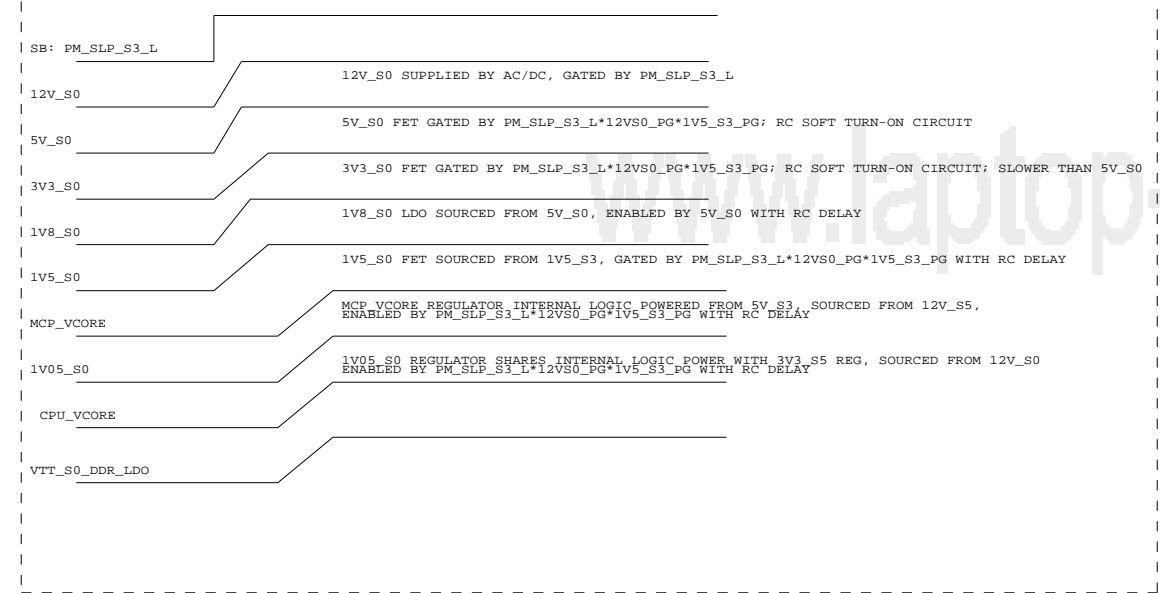


S3 POWER RAIL SEQUENCING

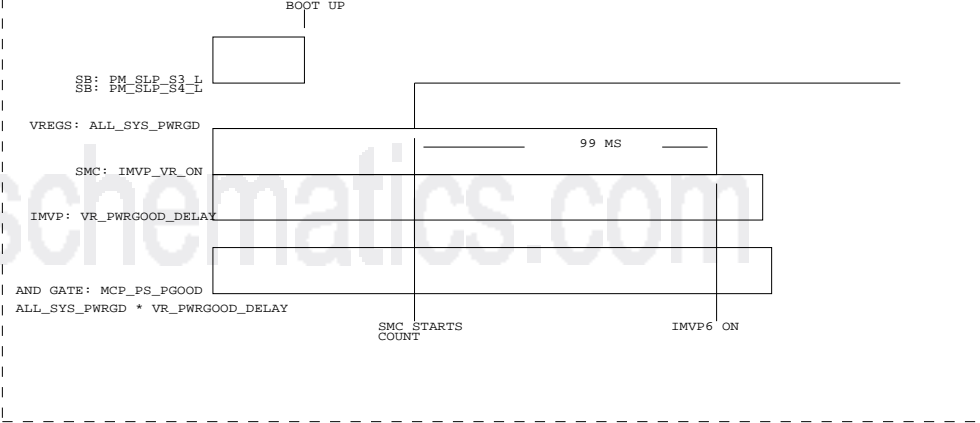


NOTE: NO SEQUENCING REQUIREMENTS FOR THESE 3 RAILS

S0 POWER RAIL SEQUENCING

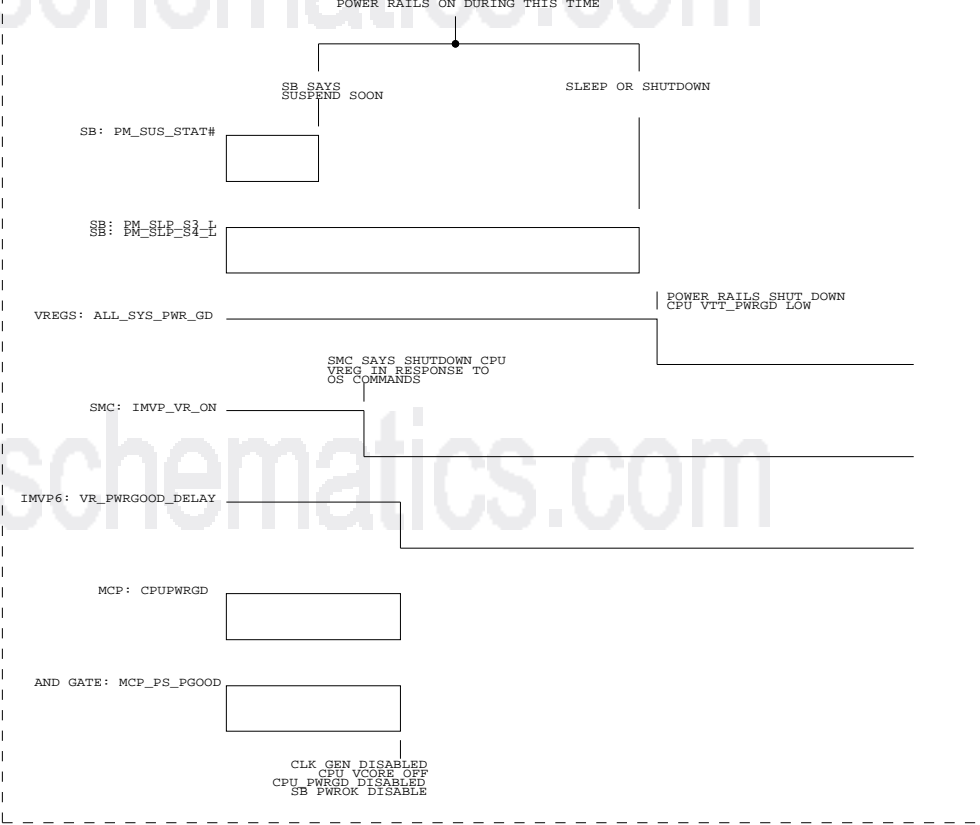


STARTUP (BOOT OR WAKE) TIMING



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



POWER SEQUENCING BLOCK DIAGRAM

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	69	109

8

7

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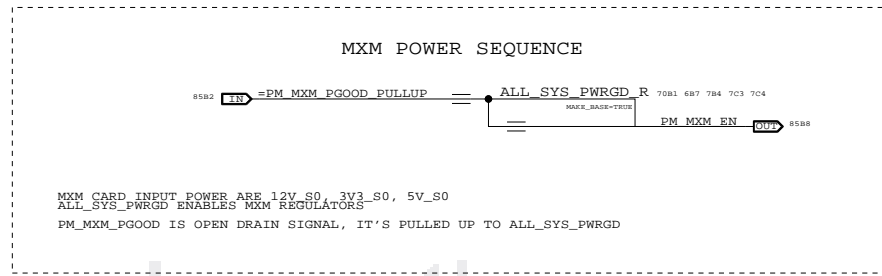
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3

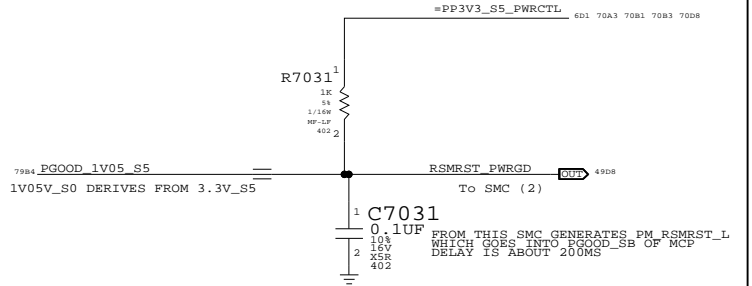
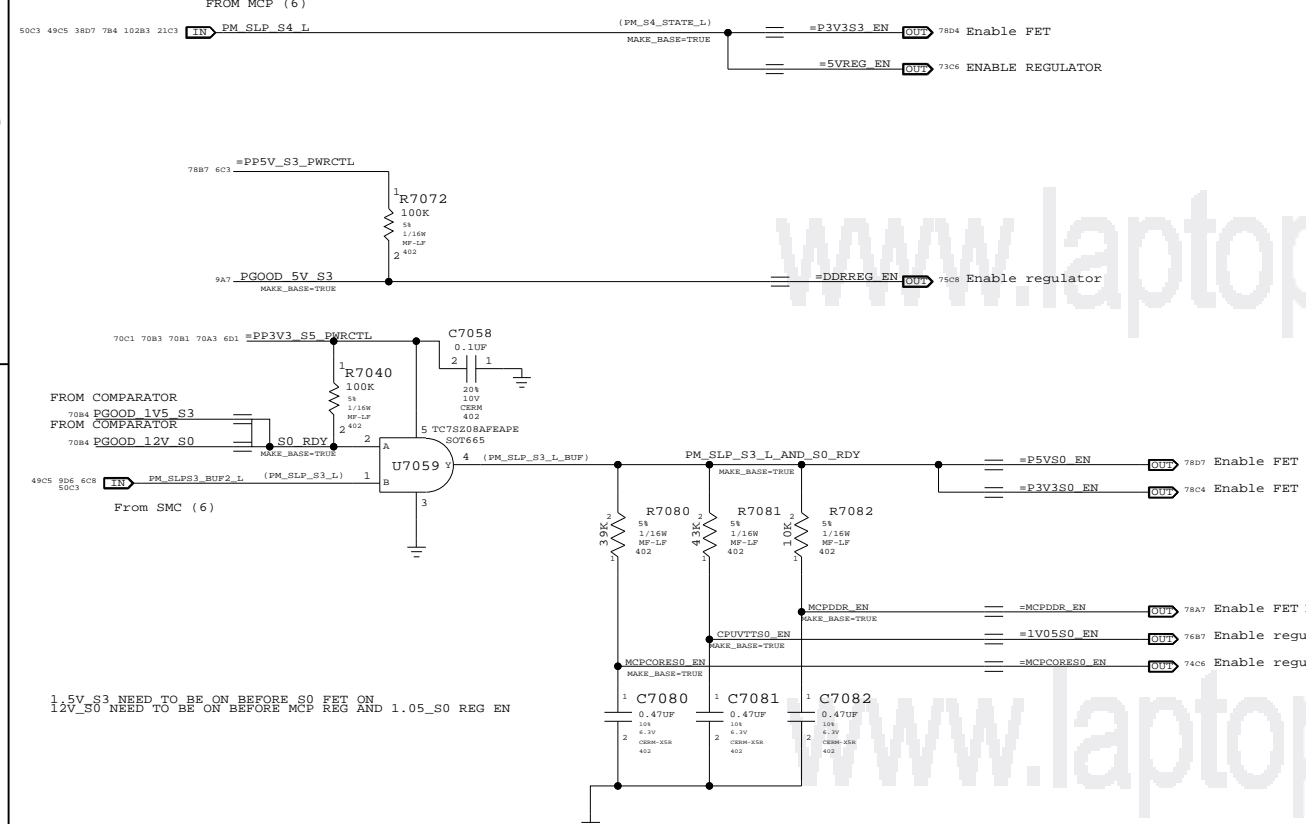
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1

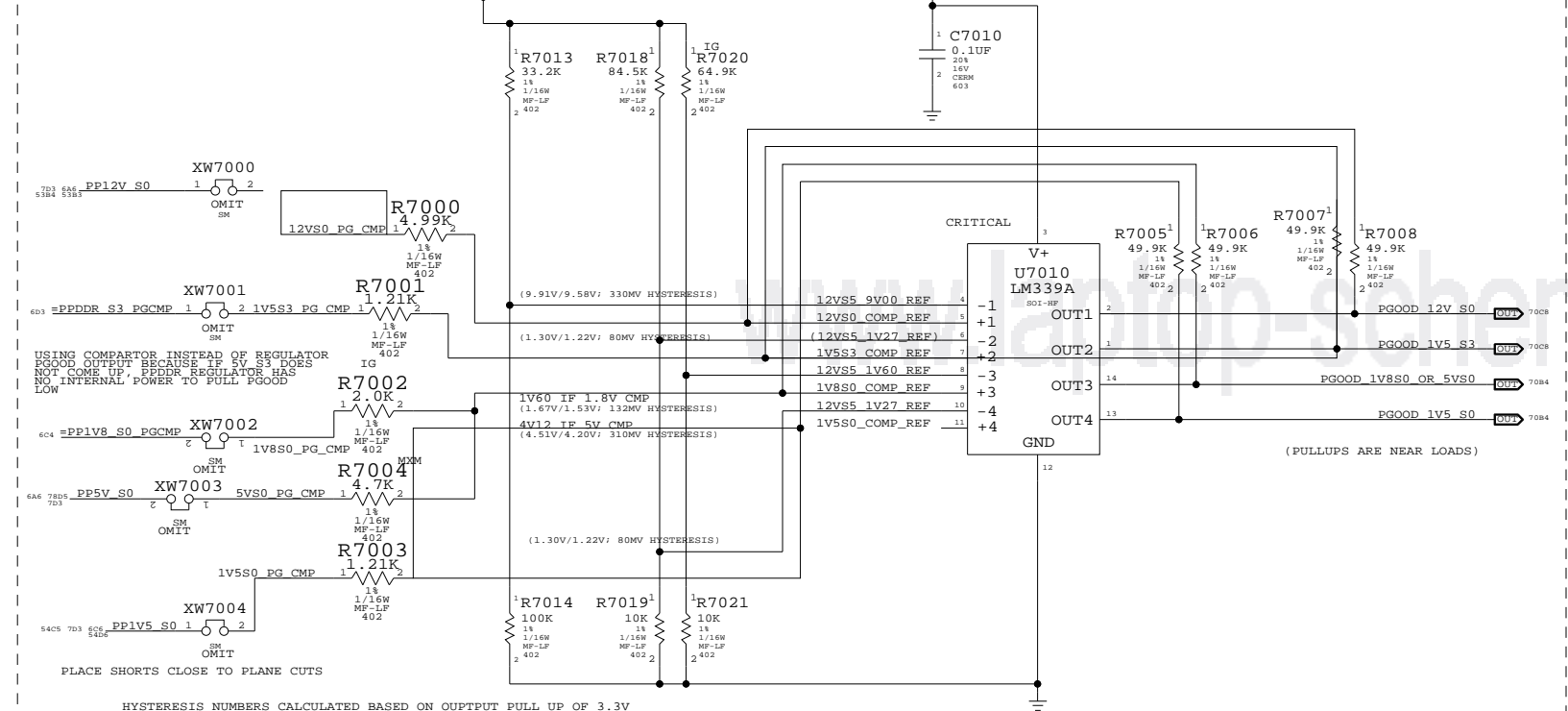
State	SMC_PM_G2_ENABLE (PORTABLES)	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0



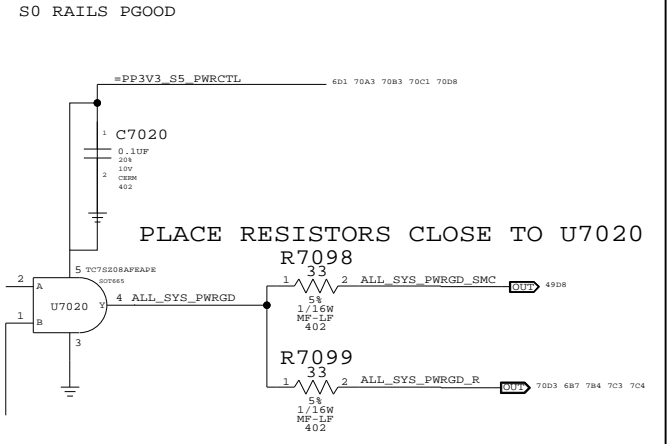
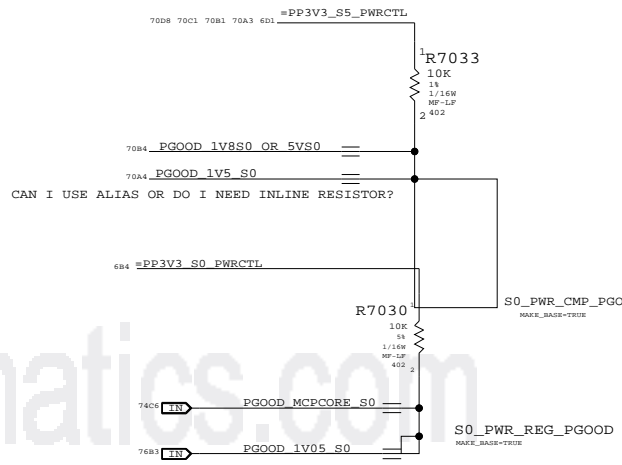
Power Control Signals
3.3V, 5V S3 enable



PGOOD Comparators



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11480341	1	RES, 19.1K, 1%, 402	R7020		MXM



I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM 8V
IRF7413	9.6A	18mOHM 20V
FDS4435	8.8A	35mOHM 25V
IRF7406	5.8A	70mOHM 20V
IRF6402	3.7A	65mOHM 12V
SI2302	1.6A	115mOHM 8V

PGOOD and Power Sequencing

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

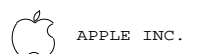
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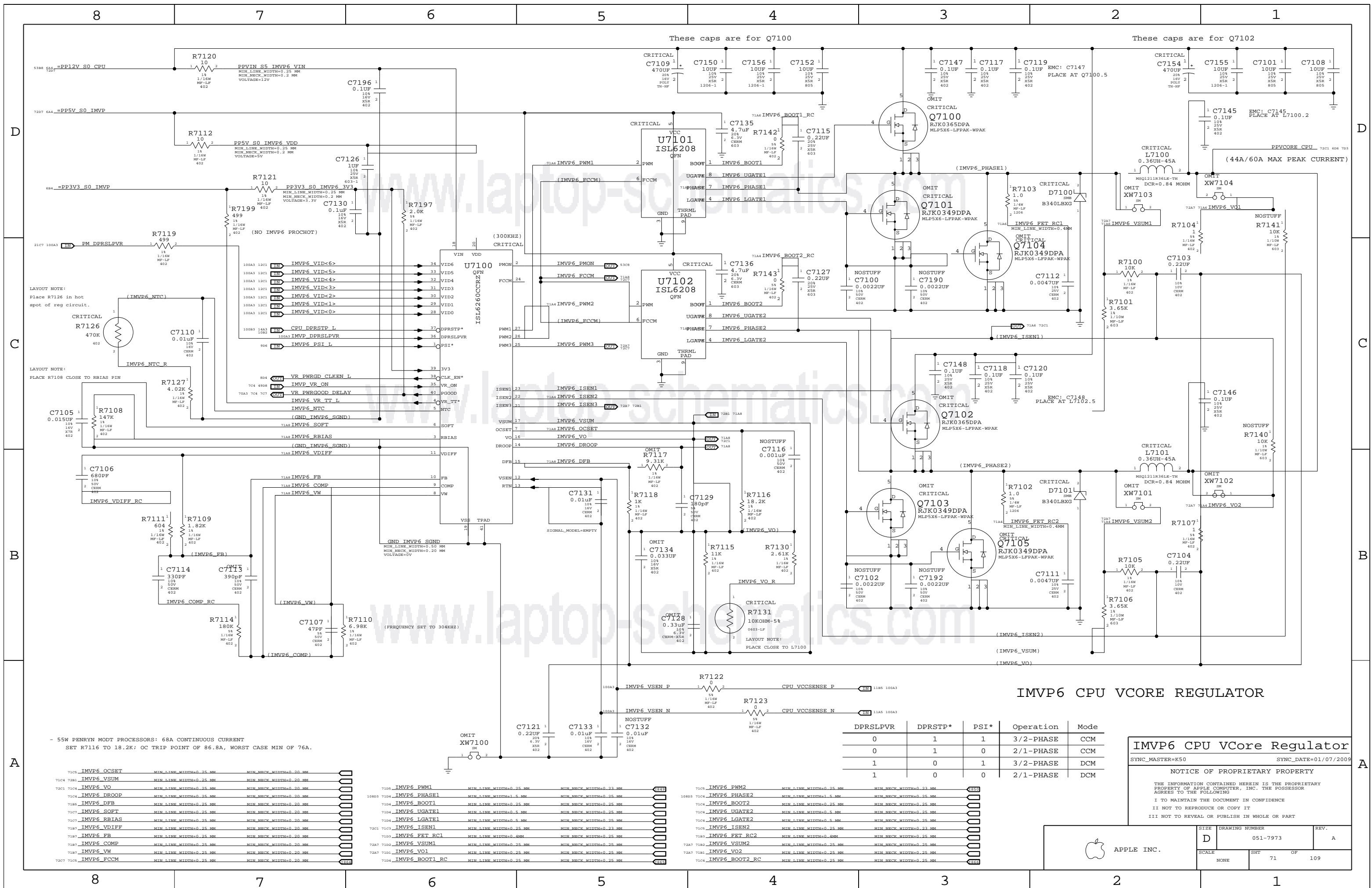
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SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	70	109



IMVP6 CPU VCore Regulator

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

IMVP6 CPU VCore Regulator

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	
NONE	71	109	

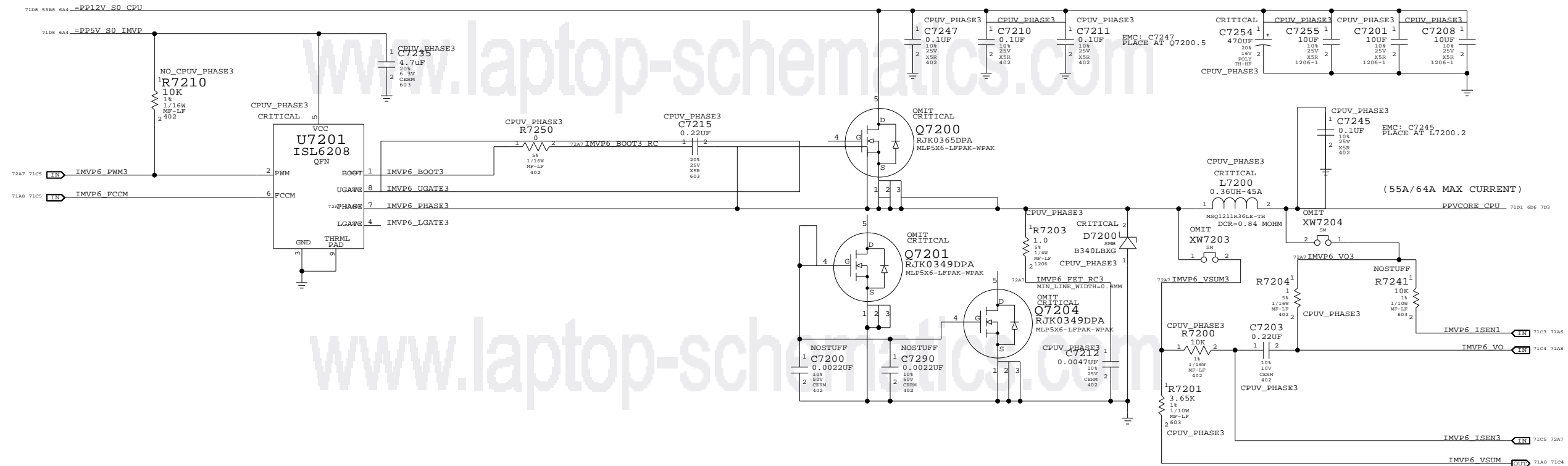
- 55W PENRYN MODT PROCESSORS: 68A CONTINUOUS CURRENT
 SET R7116 TO 18.2K; OC TRIP POINT OF 86.8A, WORST CASE MIN OF 76A.

7105	IMVP6_OCSET	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7104	IMVP6_VSUM	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7201	IMVP6_VO	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7104	IMVP6_DROOP	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7185	IMVP6_DFB	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7107	IMVP6_SOFT	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7107	IMVP6_RBIAS	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7187	IMVP6_VDIFF	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7187	IMVP6_FB	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7187	IMVP6_COMP	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7187	IMVP6_VW	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7207	IMVP6_FCCM	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM

7105	IMVP6_PWM1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.23 MM
10803	IMVP6_PHASE1	MIN LINE WIDTH=1.5 MM	MIN NECK WIDTH=0.25 MM
7104	IMVP6_BOOT1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7104	IMVP6_UGATE1	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.25 MM
7104	IMVP6_LGATE1	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.25 MM
7201	IMVP6_ISEN1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.23 MM
7105	IMVP6_FET_RC1	MIN LINE WIDTH=0.4 MM	MIN NECK WIDTH=0.25 MM
72A7	IMVP6_VSUM1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
72A7	IMVP6_VO1	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7104	IMVP6_BOOT1_RC	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM

7105	IMVP6_PWM2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.23 MM
10803	IMVP6_PHASE2	MIN LINE WIDTH=1.5 MM	MIN NECK WIDTH=0.25 MM
7104	IMVP6_BOOT2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7104	IMVP6_UGATE2	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.25 MM
7104	IMVP6_LGATE2	MIN LINE WIDTH=0.5 MM	MIN NECK WIDTH=0.25 MM
7105	IMVP6_ISEN2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.23 MM
7185	IMVP6_FET_RC2	MIN LINE WIDTH=0.4 MM	MIN NECK WIDTH=0.25 MM
72A7	IMVP6_VSUM2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
72A7	IMVP6_VO2	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM
7104	IMVP6_BOOT2_RC	MIN LINE WIDTH=0.25 MM	MIN NECK WIDTH=0.20 MM

IMVP6 CPU VCORE REGULATOR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	6	RENESAS BOT FET	Q7101,Q7103,Q7104,Q7105,Q7201,Q7204	RENESAS_FET
376S0733	6	TOSHIBA BOT FET	Q7101,Q7103,Q7104,Q7105,Q7201,Q7204	TOSHIBA_FET
376S0694	3	RENASAS TOP FET	Q7100,Q7102,Q7200	RENESAS_FET
376S0732	3	TOSHIBA TOP FET	Q7100,Q7102,Q7200	TOSHIBA_FET

NO TEST FOR CPU VREG, ADDED K2/K3

71A6 71D1	IMVP6_VO1	NO_TEST=TRUE
71A4 71A2	IMVP6_VO2	NO_TEST=TRUE
72A7 72C7	IMVP6_VO3	NO_TEST=TRUE
71A6 71D1	IMVP6_VSUM1	NO_TEST=TRUE
71A4 71A2	IMVP6_VSUM2	NO_TEST=TRUE
72A7 72C7	IMVP6_VSUM3	NO_TEST=TRUE

72C7 71C5	IMVP6_PWM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	454
108D3 72C4	IMVP6_PHASE3	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.25 MM	458
72C4	IMVP6_BOOT3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	459
72C4	IMVP6_UGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	459
72C4	IMVP6_LGATE3	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.25 MM	459
72B1 71C5	IMVP6_ISEN3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	460
72C7	IMVP6_FET_RC3	MIN_LINE_WIDTH=0.4MM	MIN_NECK_WIDTH=0.25 MM	460
72A7 72C7	IMVP6_VSUM3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	460
72A7 72C7	IMVP6_VO3	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	460
72C7	IMVP6_BOOT3_RC	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	461

IMVP6 3RD PHASE

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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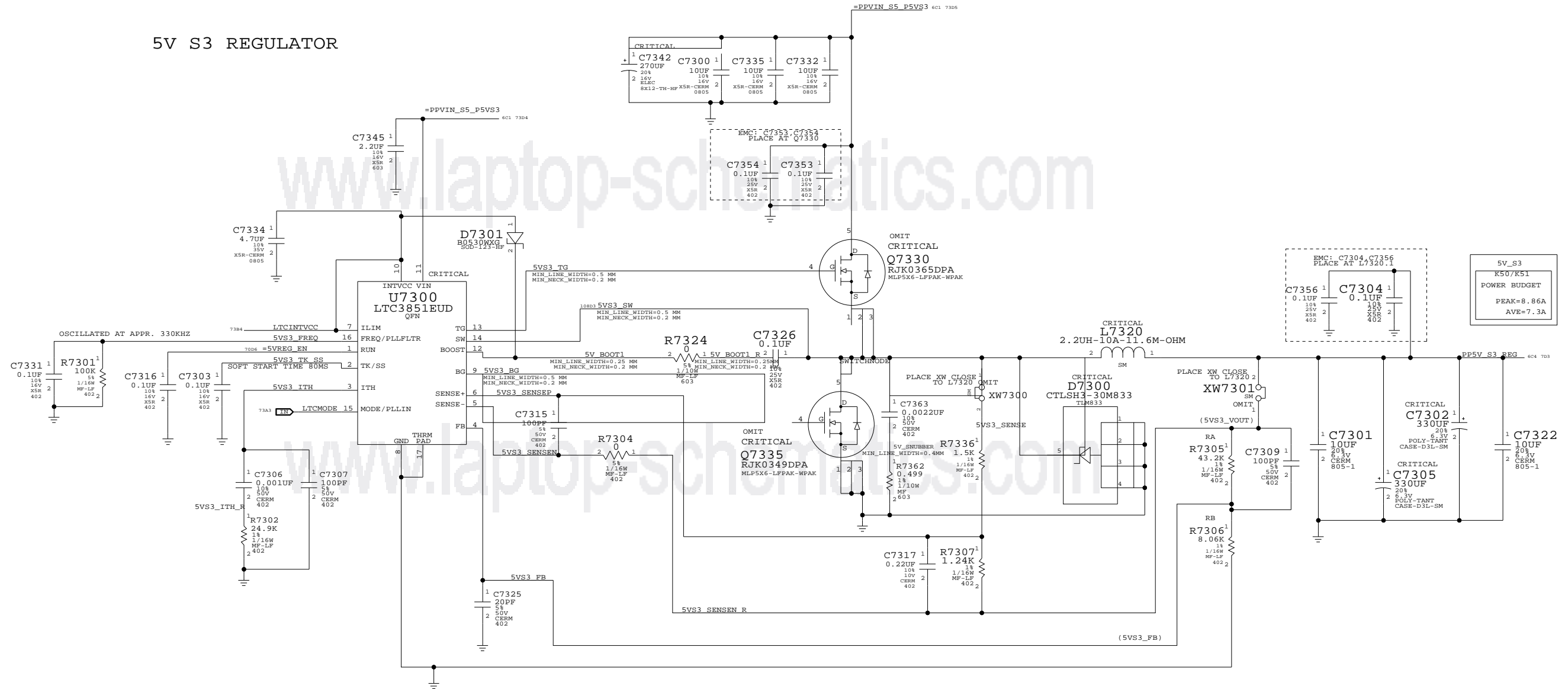
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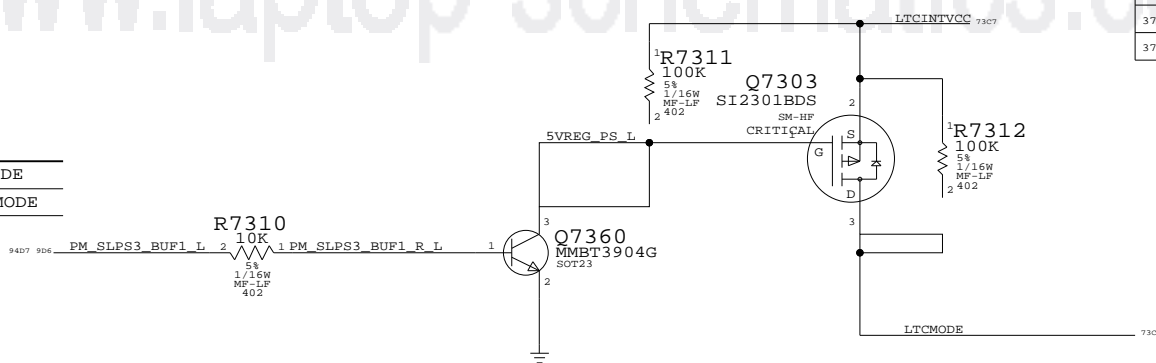
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	72		

5V S3 REGULATOR



STATE	PM_SLP3_BUF1_L	5VREG_PS_L	LTCMODE	Mode
S0	1	0	1	CONT MODE
S3	0	1	0	BURST MODE



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	1	RENESAS BOT FET	Q7335	RENESAS_FET
376S0733	1	TOSHIBA BOT FET	Q7335	TOSHIBA_FET
376S0694	1	RENESAS TOP FET	Q7330	RENESAS_FET
376S0732	1	TOSHIBA TOP FET	Q7330	TOSHIBA_FET

5V_S3 REGULATOR

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	73		

MCP CORE

8 7 6 5 4 3 2 1

D

D

C

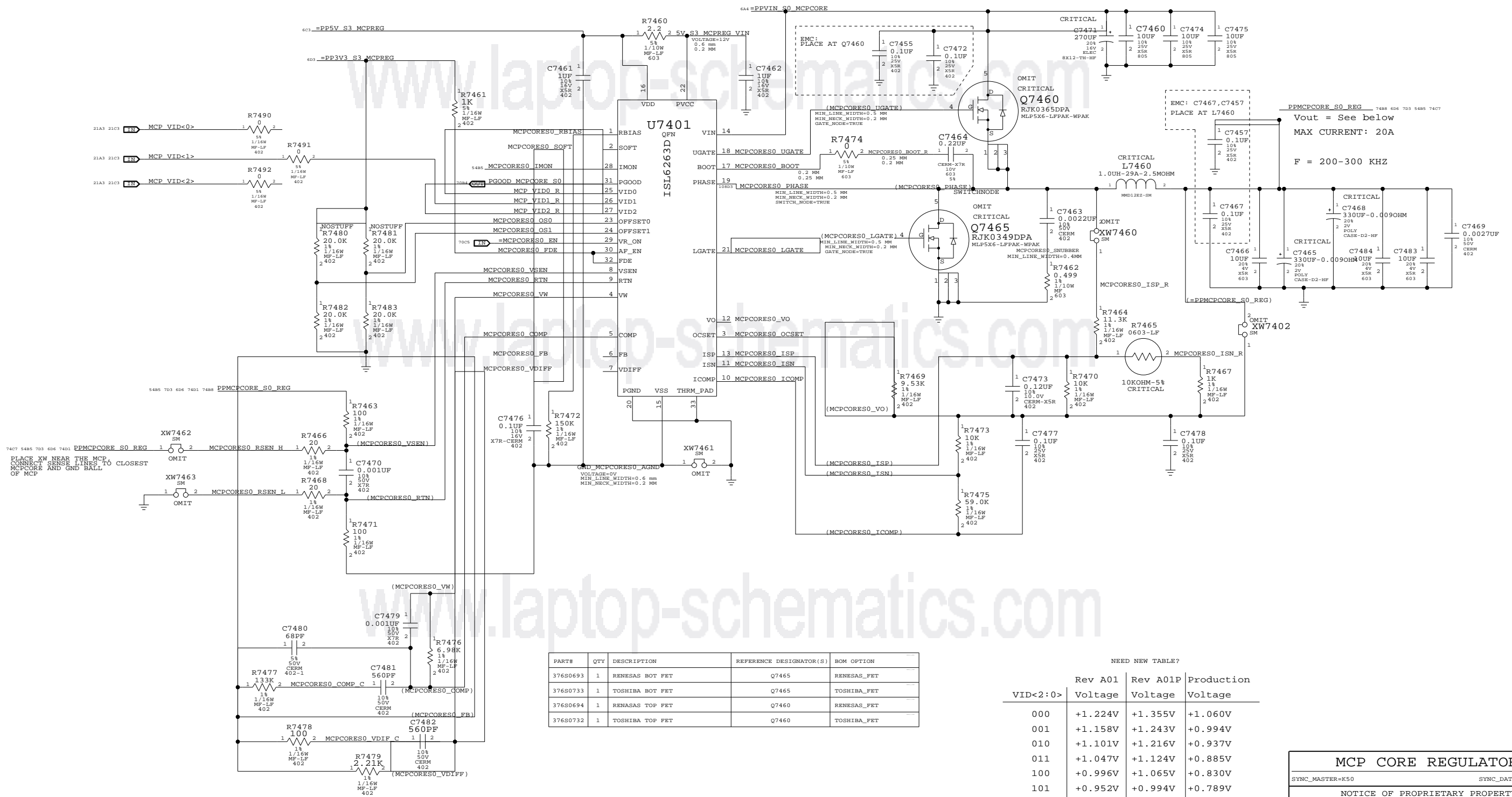
C

B

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A

A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	1	RENESAS BOT FET	Q7465	RENESAS_FET
376S0733	1	TOSHIBA BOT FET	Q7465	TOSHIBA_FET
376S0694	1	RENESAS TOP FET	Q7460	RENESAS_FET
376S0732	1	TOSHIBA TOP FET	Q7460	TOSHIBA_FET

NEED NEW TABLE?

VID<2>0>	Rev A01 Voltage	Rev A01P Voltage	Production Voltage
000	+1.224V	+1.355V	+1.060V
001	+1.158V	+1.243V	+0.994V
010	+1.101V	+1.216V	+0.937V
011	+1.047V	+1.124V	+0.885V
100	+0.996V	+1.065V	+0.830V
101	+0.952V	+0.994V	+0.789V
110	+0.913V	+0.977V	+0.752V
111	+0.876V	+0.917V	+0.719V

(Also A01Q)

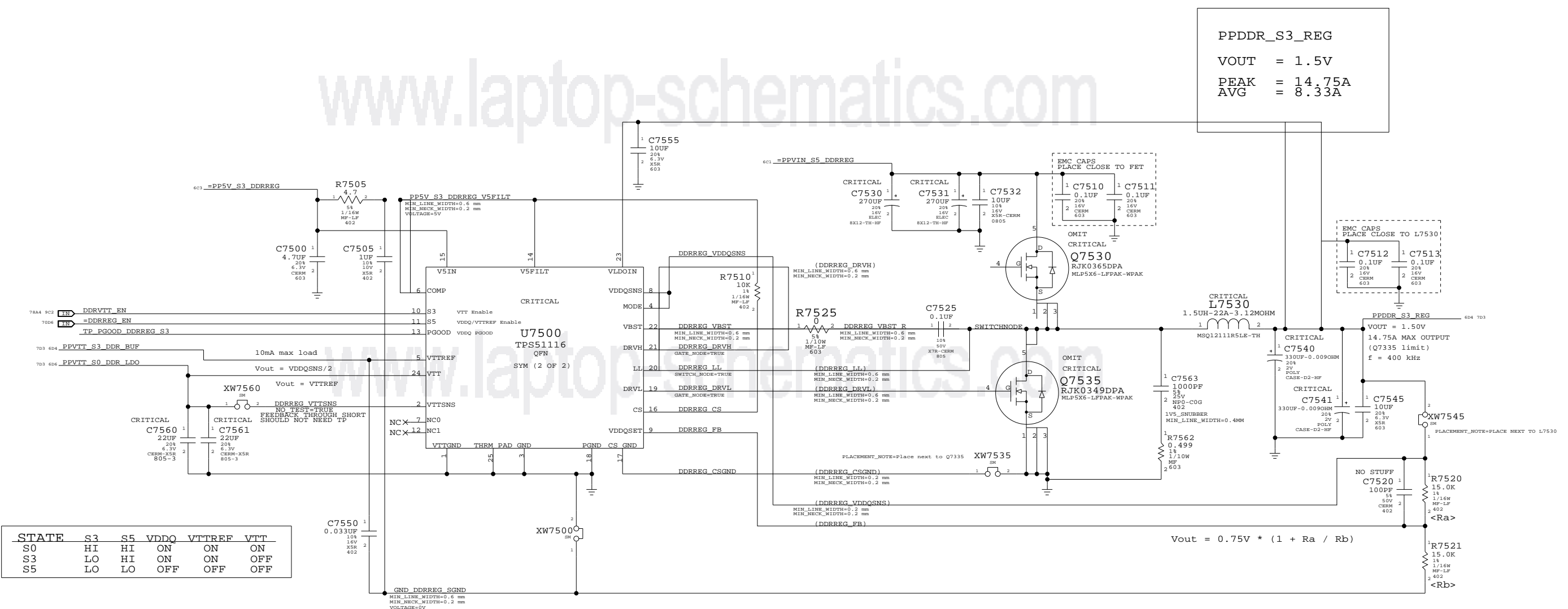
MCP CORE REGULATOR
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	74	109	

8 7 6 5 4 3 2 1

1.5 V DDR SUPPLY

www.laptop-schematics.com



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0693	1	RENESAS BOT FET	Q7535	RENESAS_FET
376S0733	1	TOSHIBA BOT FET	Q7535	TOSHIBA_FET
376S0694	1	RENESAS TOP FET	Q7530	RENESAS_FET
376S0732	1	TOSHIBA TOP FET	Q7530	TOSHIBA_FET

PPDDR_S3_REG
 VOUT = 1.5V
 PEAK = 14.75A
 AVG = 8.33A

$$V_{out} = 0.75V * (1 + R_a / R_b)$$

1.5V DDR SUPPLY
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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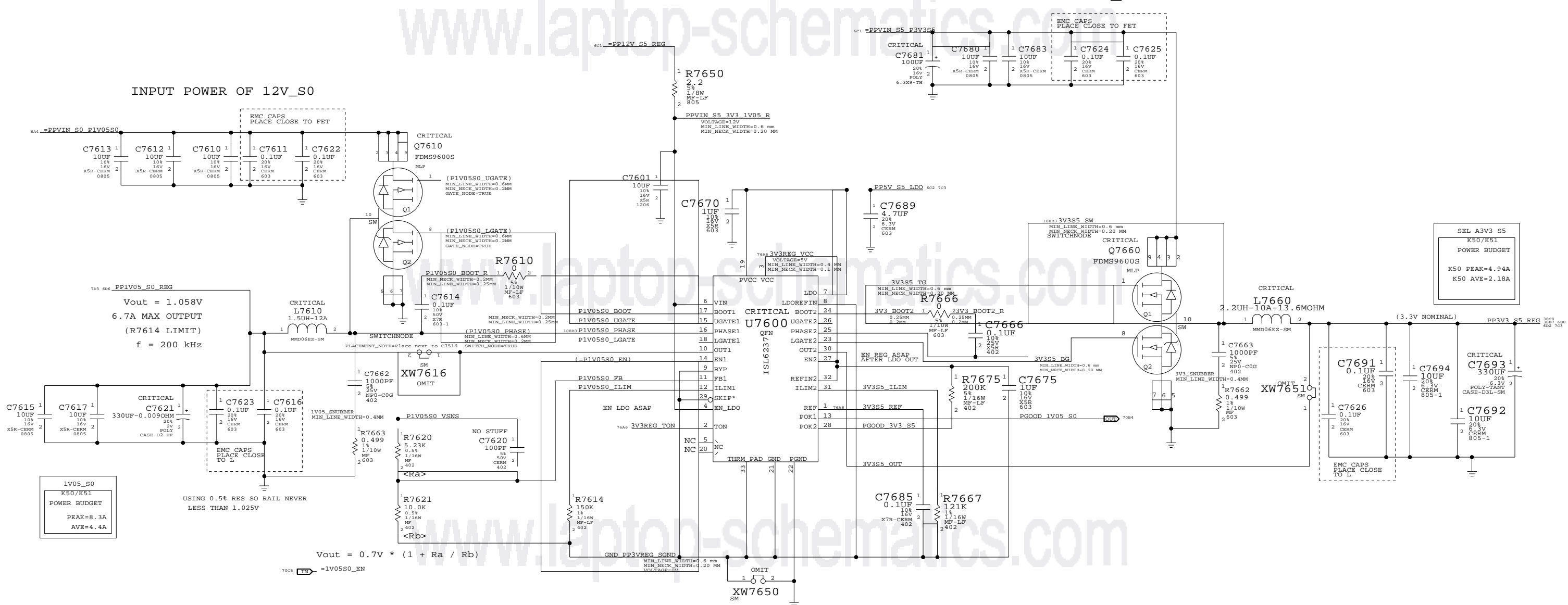
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT 75 OF 109		
NONE			

3.3V S5 AND 1.05 S0 RAILS

www.laptop-schematics.com

INPUT POWER OF 12V_S5

INPUT POWER OF 12V_S0



Vout = 1.058V
6.7A MAX OUTPUT
(R7614 LIMIT)
f = 200 kHz

USING 0.5% RES SO RAIL NEVER
LESS THAN 1.025V

$$V_{out} = 0.7V * (1 + R_a / R_b)$$

EN LDO TIED TO 12V_S5 TO EN LDO FIRST & REGULATOR INTERNAL LOGIC GETS POWER
EN2 (3V3_S5) IS TIED TO VCC, TIED INTERNALLY TO PVCC
TIED EXTERNALLY TO LDO OUT, SO REGULATOR IS ENABLED
AS SOON AS LDO OUTPUT IS GOOD

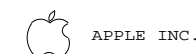
EN1 (1.05_S0) CONTROLLED SEPARATELY

1.05VS0/3.3V S5 SUPPLIES

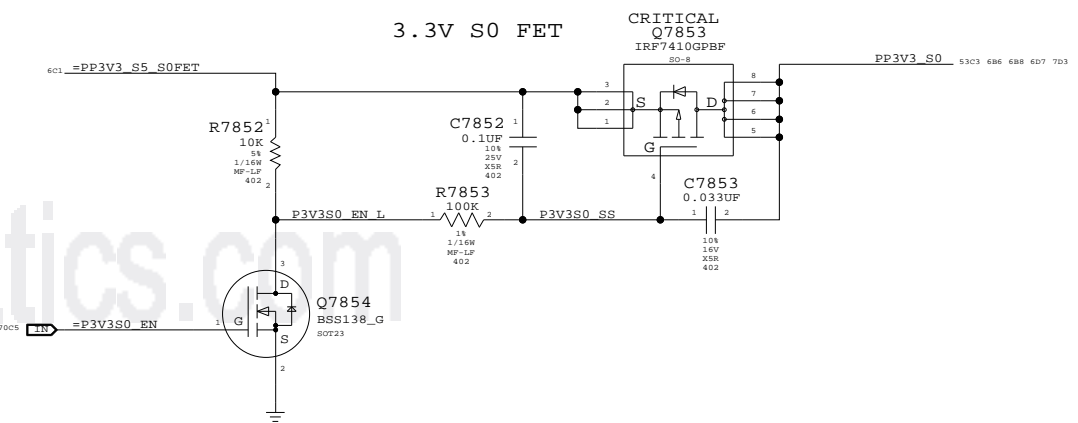
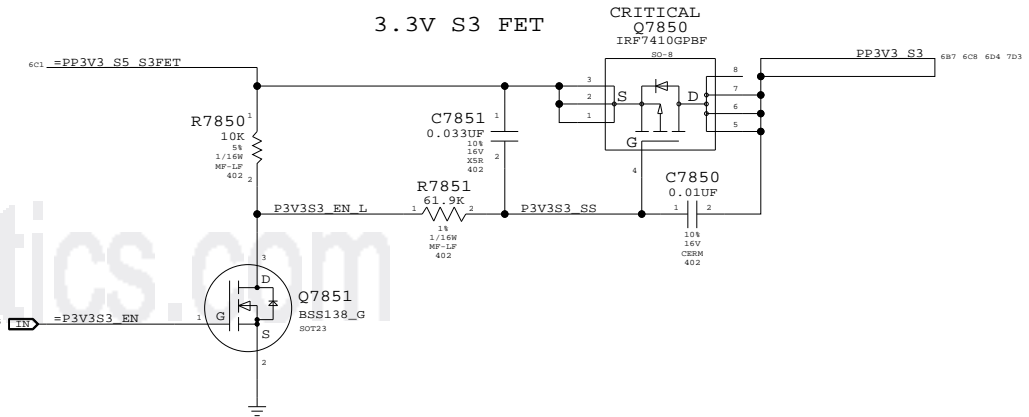
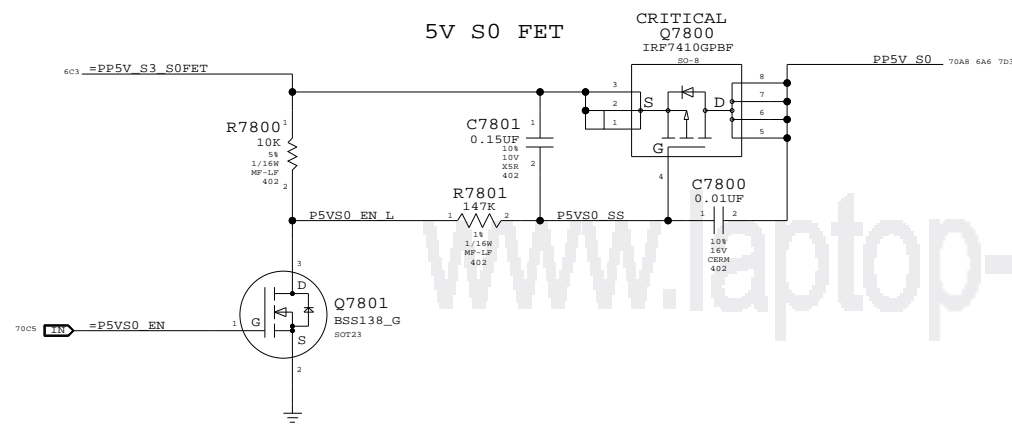
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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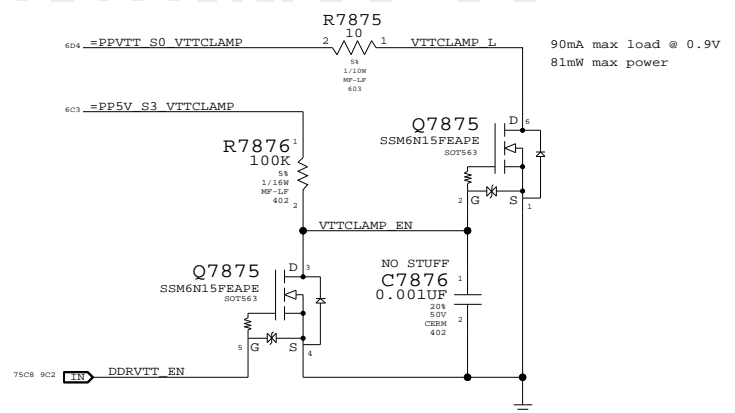
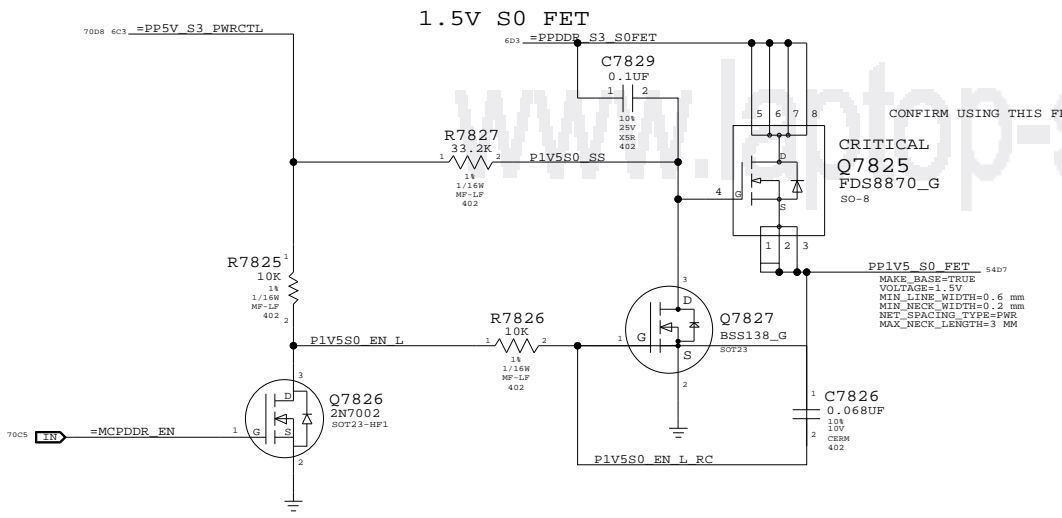


SIZE	DRAWING NUMBER	REV.
D	051-7973	A
SCALE	SHT	OF
NONE	76	109



MCP79 DDRVTT FET

MCP79 DDR PAD LEAKAGE IS HIGH ENOUGH THAT NVIDIA RECOMMENDS UNPOWERING DURING SLEEP. IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW BEFORE RAIL IS TURNED OFF, AND REMAINS LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS WILL EXIT SELF-REFRESH PREMATURELY. MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS LOW THROUGH VTT TERMINATION RESISTORS.



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

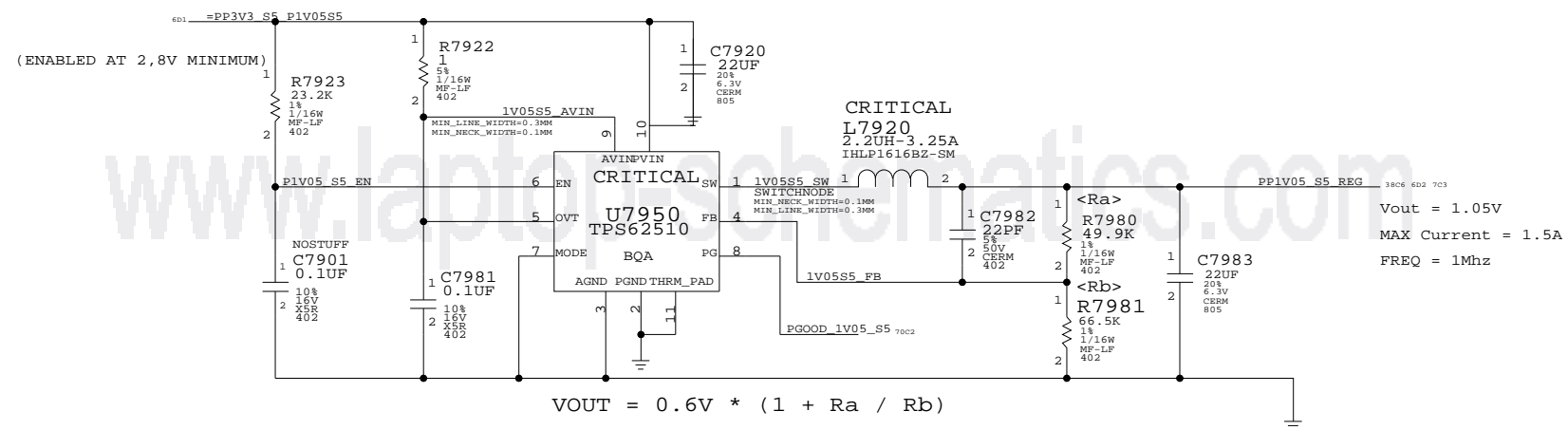
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	D	051-7973	A
SCALE	SHT	OF	
NONE	78	109	

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MCP 1.05V_S5 AUXC SUPPLY



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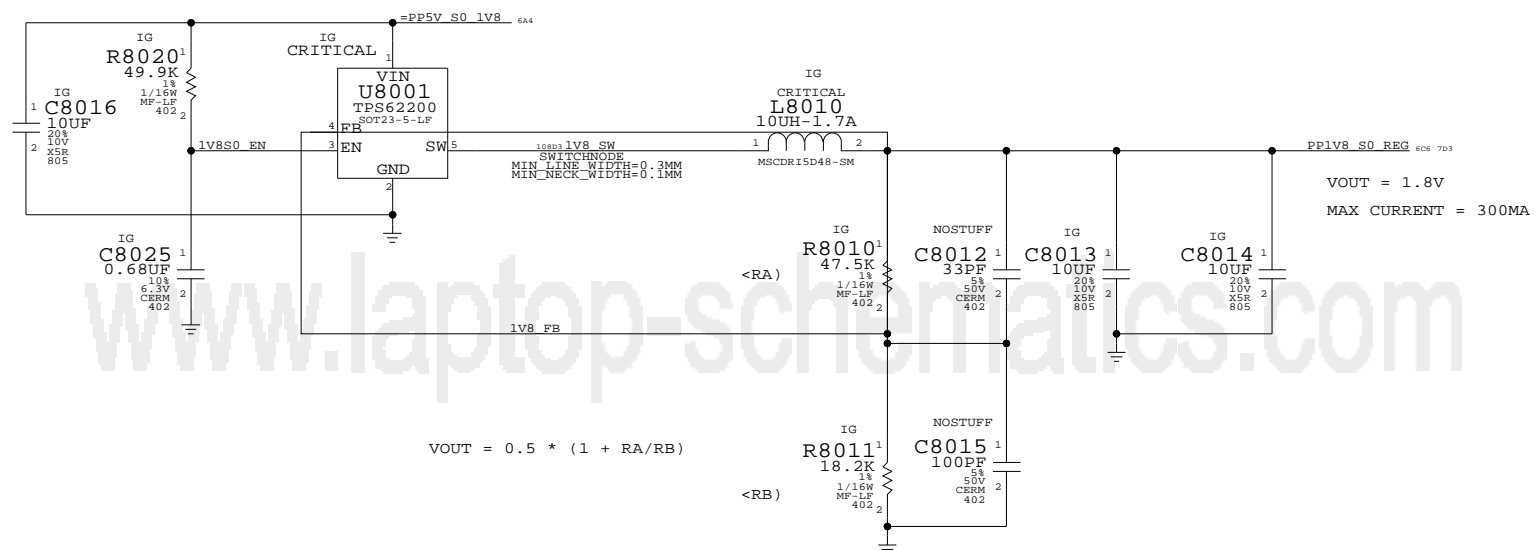
1V05 S5 POWER SUPPLY
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	79	109	

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MCP ONLY 1.8V_S0 POWER SUPPLY



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1V8 POWER SUPPLY
SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT 80 OF 109		
NONE			

8

7

6

5

4

3

2

1

D

D

C

C

B

B

A

A

8

7

6

5

4

3

2

1

Page Notes

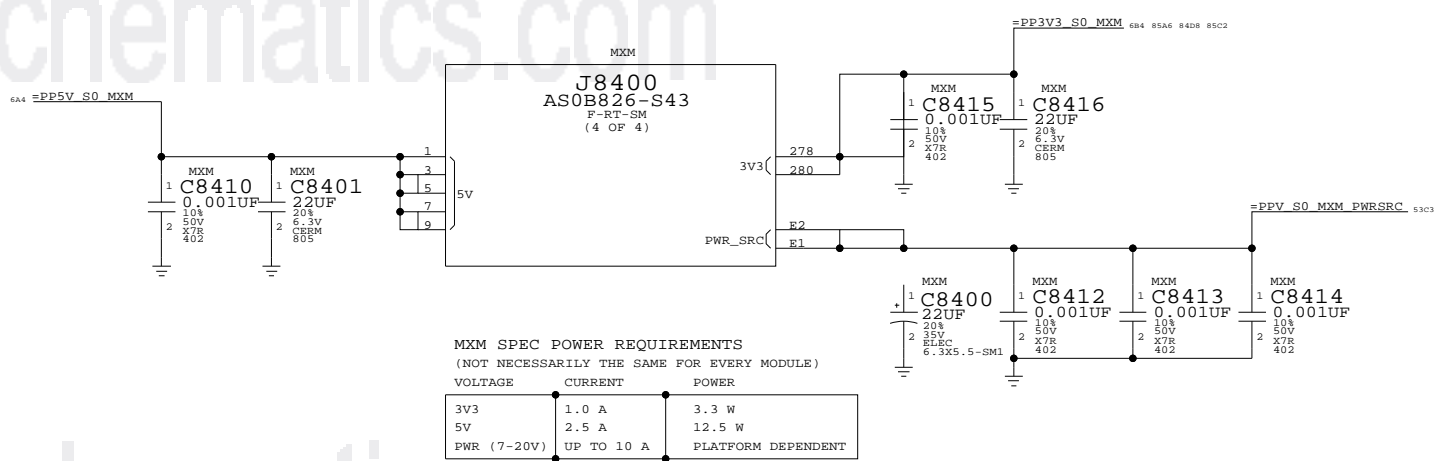
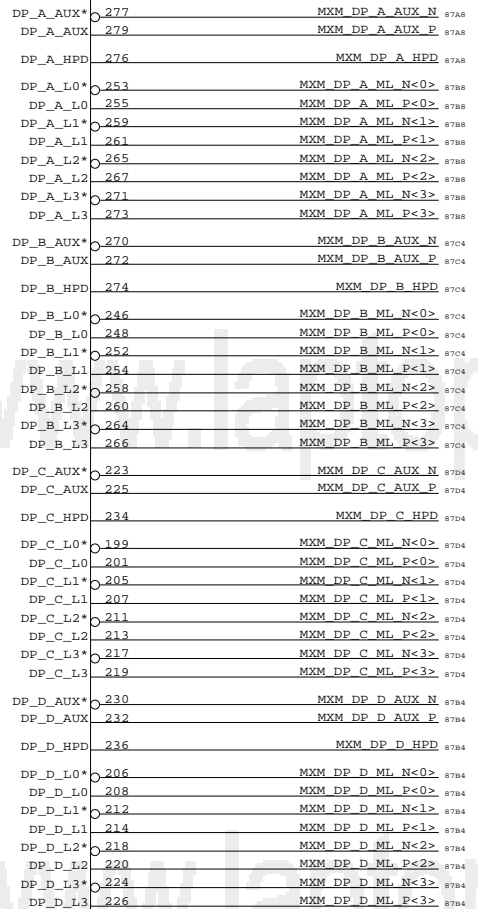
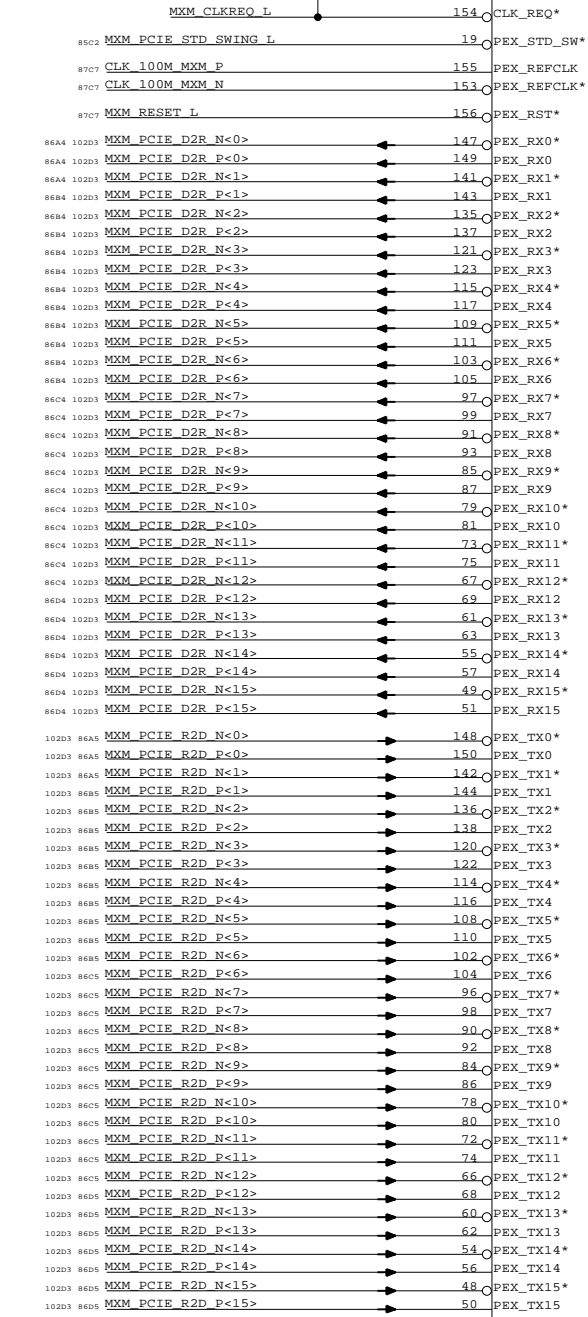
Power aliases required by this page:
 - =PP3V3_S0_MXM
 - =PP5V_S0_MXM
 - =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - MXM

85C2 84D2 85A6 684 =PP3V3_S0_MXM

MXM
J8400
AS0B826-S43
 F-RT-SM
 (2 OF 4)
 APPLE P/N: 516S0676



MXM SPEC POWER REQUIREMENTS
 (NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

MXM PCIe, DP & Power
 SYNC_MASTER=k50 SYNC_DATE=01/07/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	84		

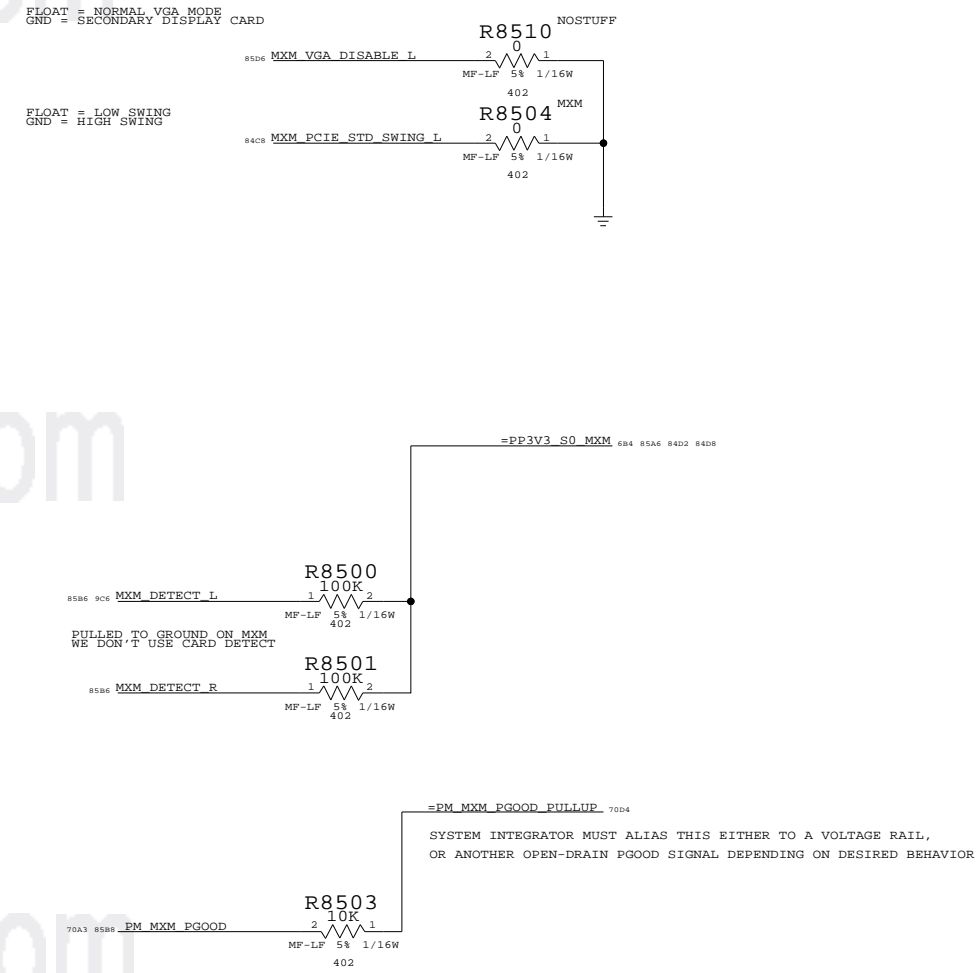
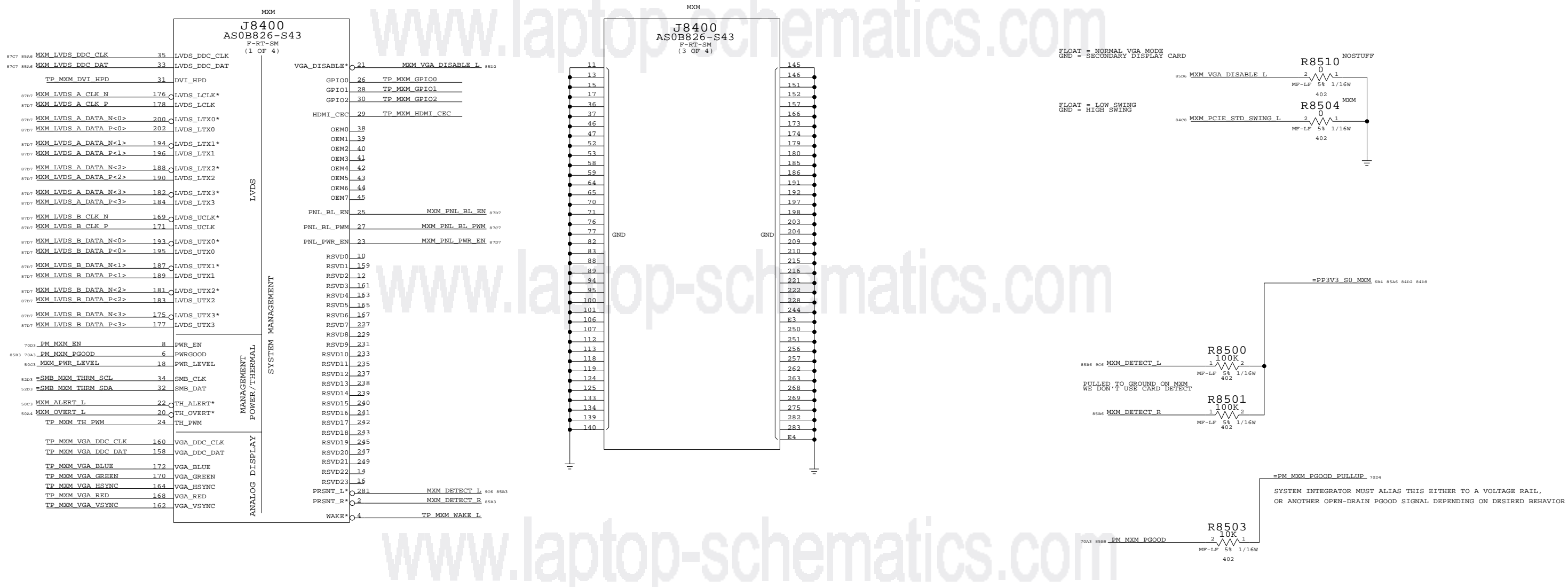
Page Notes

Power aliases required by this page:
 - =PP3V3_S0_MXM

Signal aliases required by this page:
 - =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
 - =SMB_MXM_THRM_CLK

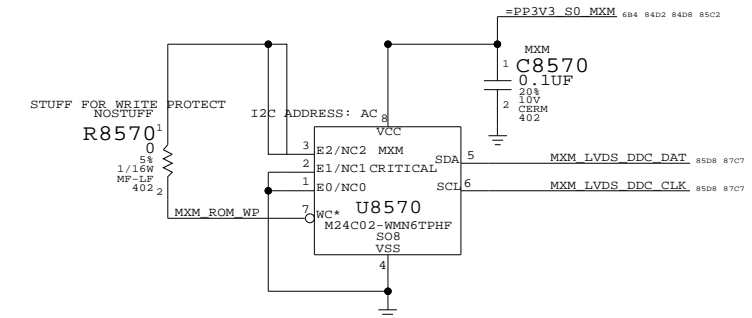
BOM options provided by this page:

PULLUPS & PULLDOWNS AT MXM CONNECTOR



MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



MXM I/O

SYNC_MASTER=k50 SYNC_DATE=01/07/2009

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	85		

Page Notes

Power aliases required by this page:
 - =PP5V_DP_AUX

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

UNUSED DP INTERFACES

85C9	MXM LVDS A DATA P<3..0>	==	LVDS EG A DATA P<3..0>	107C2 8986 89C6 89D6 90A6 90A8
			MAKE_BASE=TRUE	
85C9	MXM LVDS A DATA N<3..0>	==	LVDS EG A DATA N<3..0>	107C2 8986 89C6 89D6 90A6 90A8
			MAKE_BASE=TRUE	
85C9	MXM LVDS B DATA P<3..0>	==	LVDS EG B DATA P<3..0>	107C2 89A6 89C3 89D3 90A8 90B6
			MAKE_BASE=TRUE	
85C9	MXM LVDS B DATA N<3..0>	==	LVDS EG B DATA N<3..0>	107C2 89A6 89C3 89D3 90A6 90B8
			MAKE_BASE=TRUE	
85C9	MXM LVDS A CLK N	==	LVDS EG A CLK N	8986 107C2
			MAKE_BASE=TRUE	
85C9	MXM LVDS A CLK P	==	LVDS EG A CLK P	8986 107C2
			MAKE_BASE=TRUE	
85C9	MXM LVDS B CLK N	==	LVDS EG B CLK N	89C3 107C2
			MAKE_BASE=TRUE	
85C9	MXM LVDS B CLK P	==	LVDS EG B CLK P	89C3 107C2
			MAKE_BASE=TRUE	
85C6	MXM PNL BL EN	==	LVDS_BKL_ON	6D6 8D3 90A3 90C4
			MAKE_BASE=TRUE	
85C6	MXM PNL PWR EN	==	LVDS EG PANEL PWR	90A3 90B8
			MAKE_BASE=TRUE	
85C6	MXM PNL BL PWM	==	LVDS EG BKL PWM	90D6
			MAKE_BASE=TRUE	
85D8 85A6	MXM LVDS DDC DAT	==	LVDS EG DDC DATA	89A3 90A6
			MAKE_BASE=TRUE	
85D8 85A6	MXM LVDS DDC CLK	==	LVDS EG DDC CLK	89B3 90A8
			MAKE_BASE=TRUE	
84C9	CLK 100M MXM P	==	GPU_CLK100M_PCIE_P	906 102C3
			MAKE_BASE=TRUE	
84C9	CLK 100M MXM N	==	GPU_CLK100M_PCIE_N	906 102C3 7C3
			MAKE_BASE=TRUE	
84C9	MXM RESET L	==	PEG RESET L	902 90D4
			MAKE_BASE=TRUE	

84B5	MXM DP C ML N<0..3>	==	TP MXM DP C ML N<0..3>	MAKE_BASE=TRUE
84B5	MXM DP C ML P<0..3>	==	TP MXM DP C ML P<0..3>	MAKE_BASE=TRUE
84C5	MXM DP C AUX N	==	TP MXM DP C AUX N	MAKE_BASE=TRUE
84C5	MXM DP C AUX P	==	TP MXM DP C AUX P	MAKE_BASE=TRUE
84B5	MXM DP C HPD	==	TP MXM DP C HPD	MAKE_BASE=TRUE
84C5	MXM DP B ML N<0..3>	==	TP MXM DP B ML N<0..3>	MAKE_BASE=TRUE
84C5	MXM DP B ML P<0..3>	==	TP MXM DP B ML P<0..3>	MAKE_BASE=TRUE
84C5	MXM DP B AUX N	==	TP MXM DP B AUX N	MAKE_BASE=TRUE
84C5	MXM DP B AUX P	==	TP MXM DP B AUX P	MAKE_BASE=TRUE
84C5	MXM DP B HPD	==	TP MXM DP B HPD	MAKE_BASE=TRUE

MXM

EXTERNAL DP CONN

THESE ALIASES ARE TO CONFORM WITH K50/K52 SHARED CONNECTOR PAGE

84C5	MXM DP A ML N<0>	==	DP EG ML N<0>	107D2 91D8
			MAKE_BASE=TRUE	
84C5	MXM DP A ML P<0>	==	DP EG ML P<0>	107D2 91C8
			MAKE_BASE=TRUE	
84C5	MXM DP A ML N<1>	==	DP EG ML N<1>	107D2 91C8
			MAKE_BASE=TRUE	
84C5	MXM DP A ML P<1>	==	DP EG ML P<1>	107D2 91C8
			MAKE_BASE=TRUE	
84C5	MXM DP A ML N<2>	==	DP EG ML N<2>	107D2 91B8
			MAKE_BASE=TRUE	
84C5	MXM DP A ML P<2>	==	DP EG ML P<2>	107D2 91B7
			MAKE_BASE=TRUE	
84C5	MXM DP A ML N<3>	==	DP EG ML N<3>	107D2 91C4
			MAKE_BASE=TRUE	
84C5	MXM DP A ML P<3>	==	DP EG ML P<3>	107D2 91C4
			MAKE_BASE=TRUE	
84C5	MXM DP A HPD	==	DP EG HPD	91B4
			MAKE_BASE=TRUE	
84C9	MXM DP A AUX N	==	DP EG AUXCH N	9304 107D2
			MAKE_BASE=TRUE	
84C9	MXM DP A AUX P	==	DP EG AUXCH P	93B4 107D2
			MAKE_BASE=TRUE	

MXM ALIASES

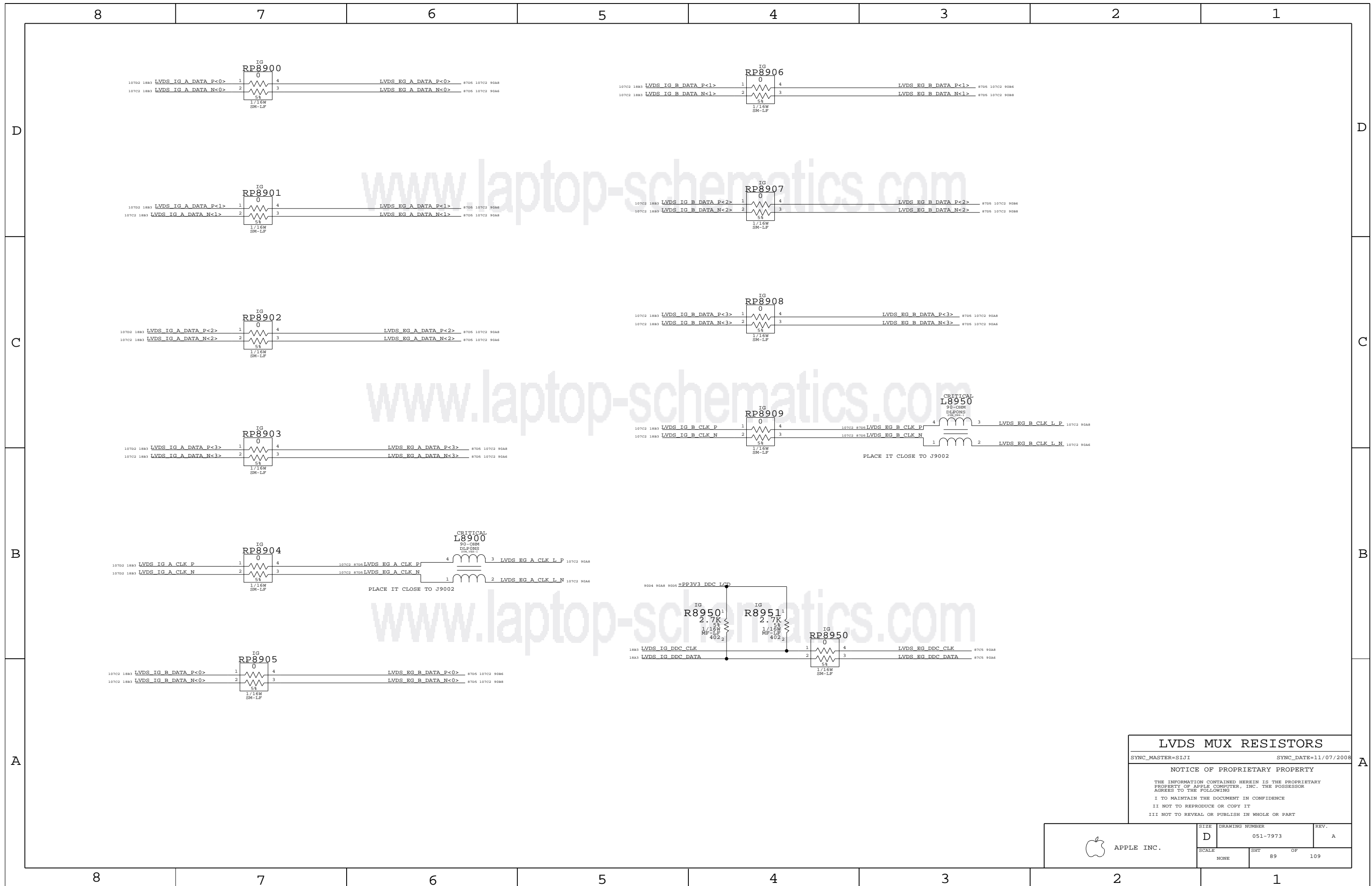
SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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SCALE	SHT	OF
NONE	87	109



LVDS MUX RESISTORS

SYNC_MASTER=SIJI SYNC_DATE=11/07/2008

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	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	89	109	

INVERTER INTERFACE

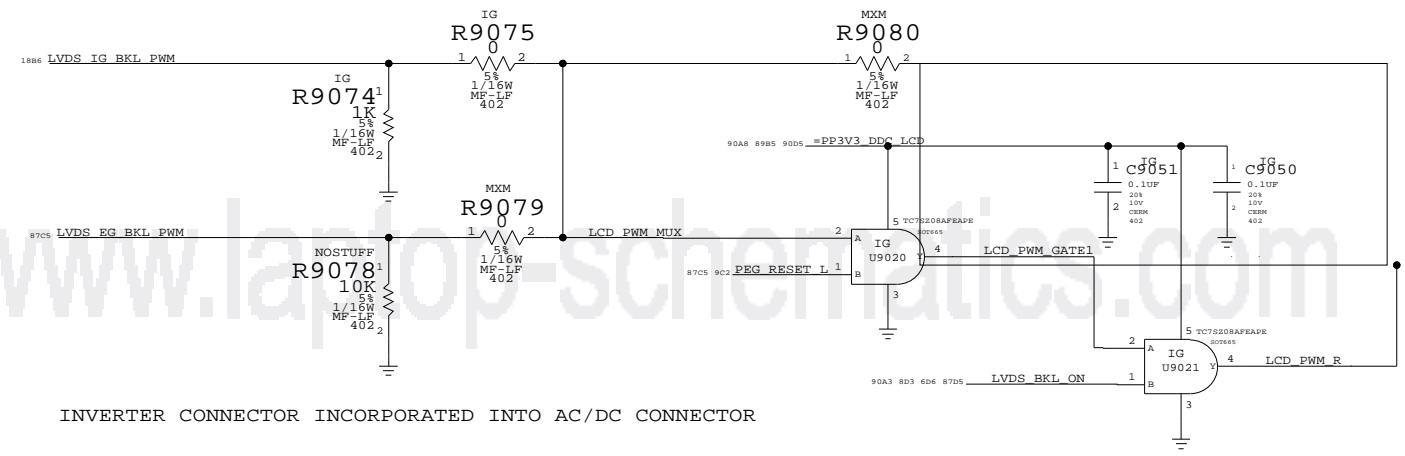
6A4=PP3V3_S0_VIDEO ==PP3V3_DDC_LCD 8985 90A8 90D4

Page Notes

Power aliases required by this page:
 - =PPV_S0_LCD_20INCH
 - =PP3V3_S0_VIDEO

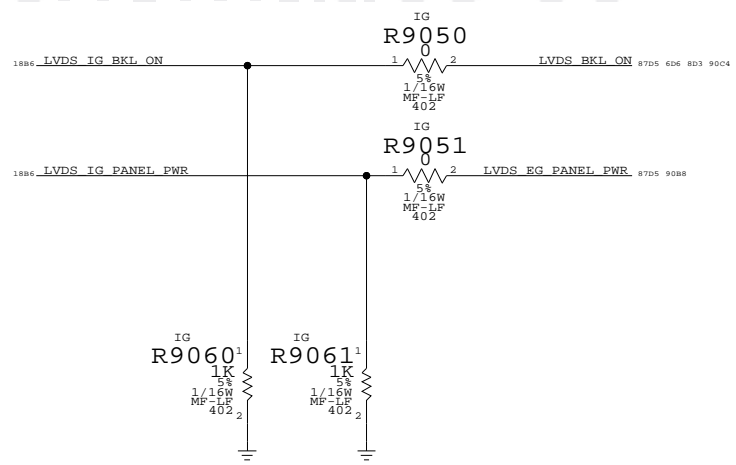
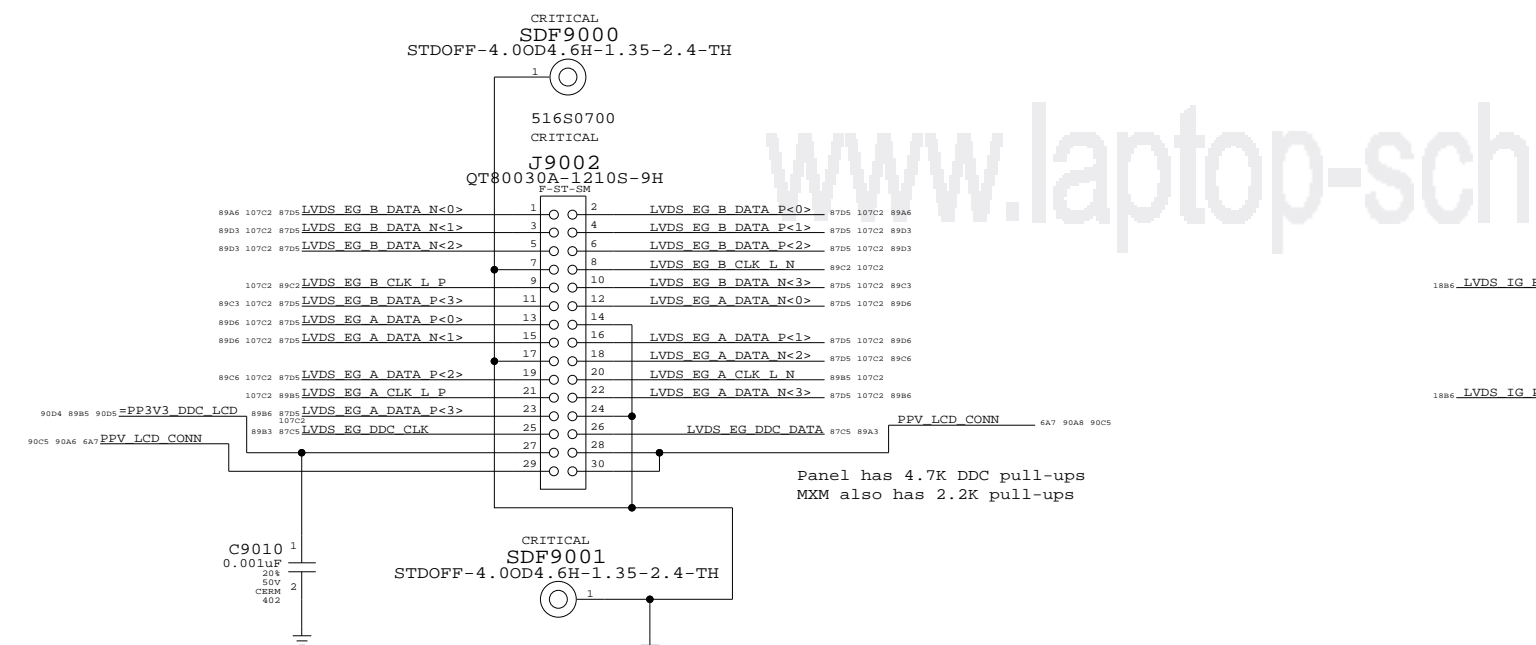
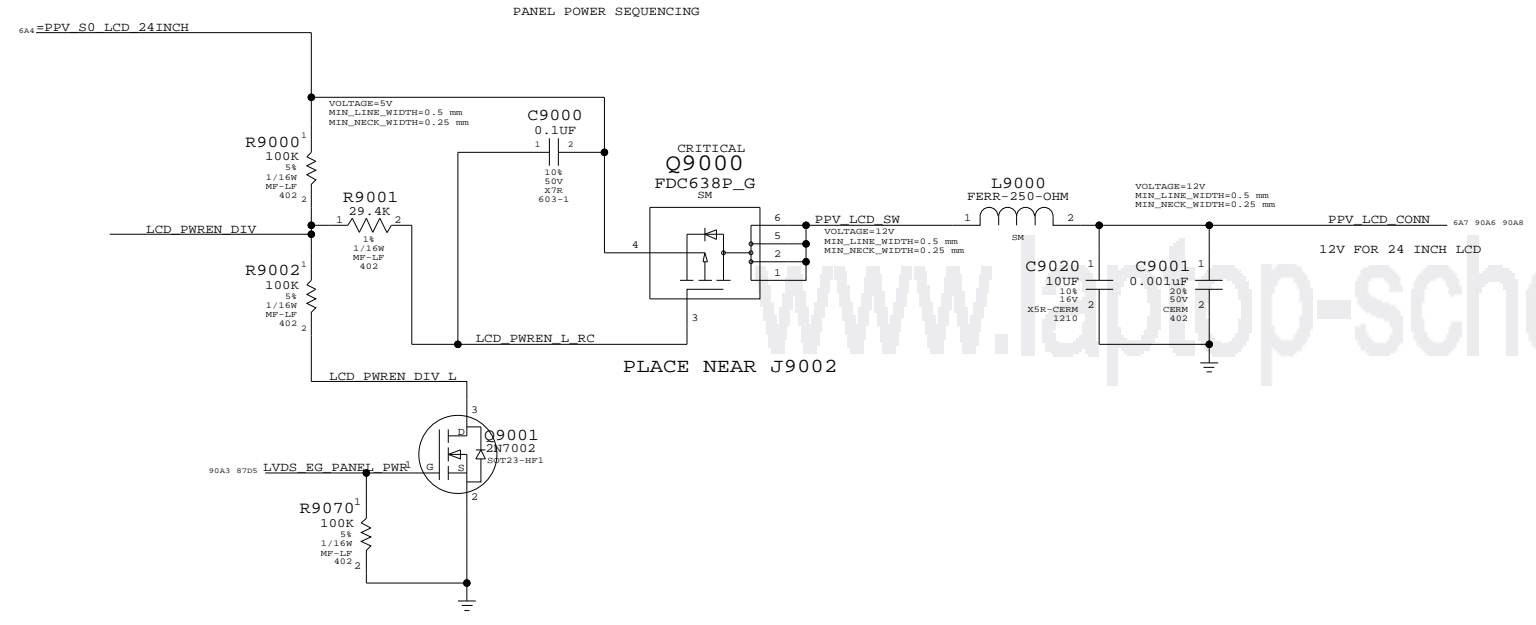
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 IG, MXM



LCD (LVDS) INTERFACE

INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR



INTERNAL DISPLAY CONNS

SYNC_MASTER=SIJI SYNC_DATE=11/07/2008

NOTICE OF PROPRIETARY PROPERTY

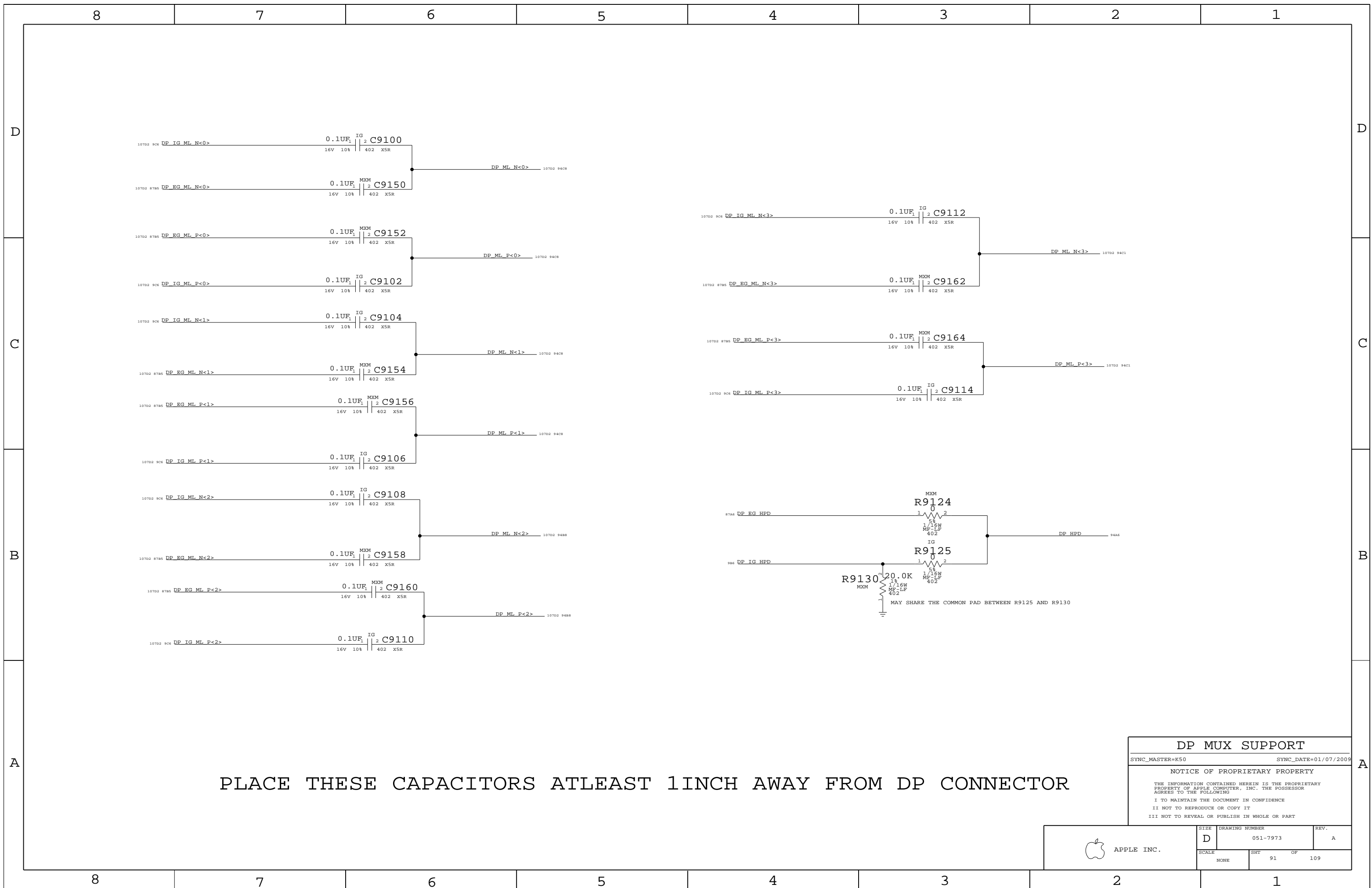
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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	90	109	



PLACE THESE CAPACITORS ATLEAST 1INCH AWAY FROM DP CONNECTOR

DP MUX SUPPORT

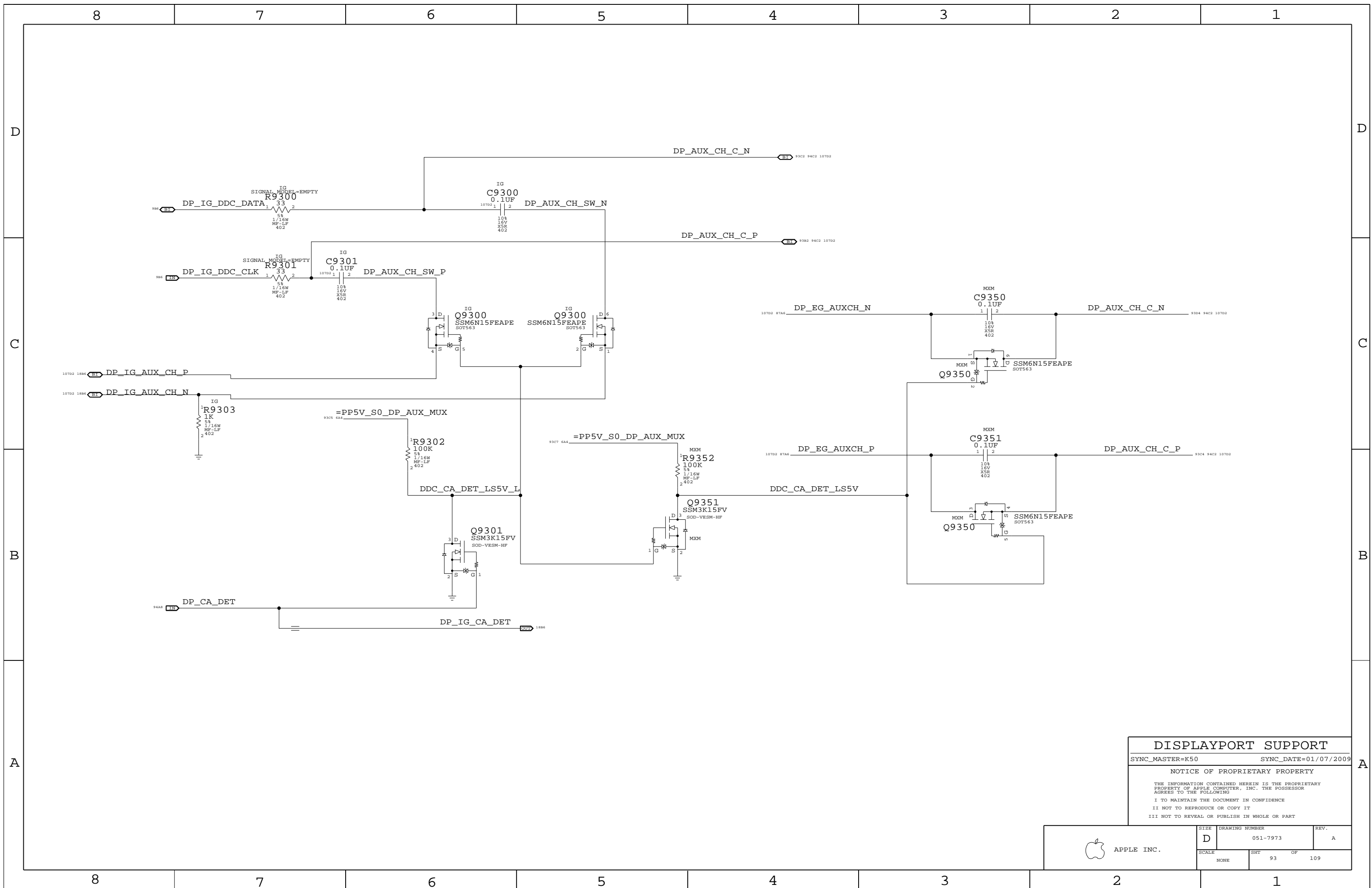
SYNC_MASTER=k50 SYNC_DATE=01/07/2009

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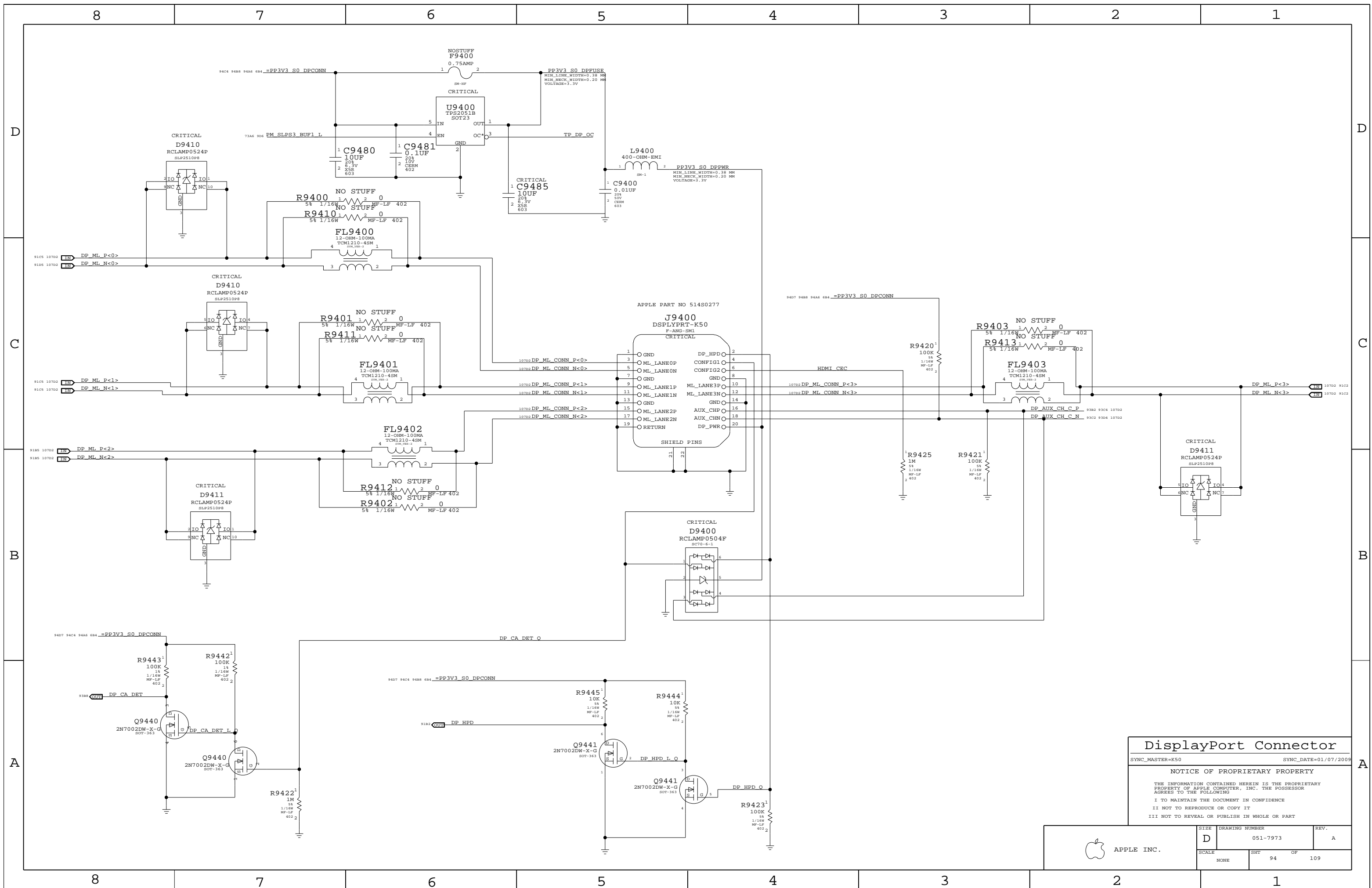
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	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	91	109	



DISPLAYPORT SUPPORT
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7973	REV. A
	SCALE NONE	SHIT 93	OF 109



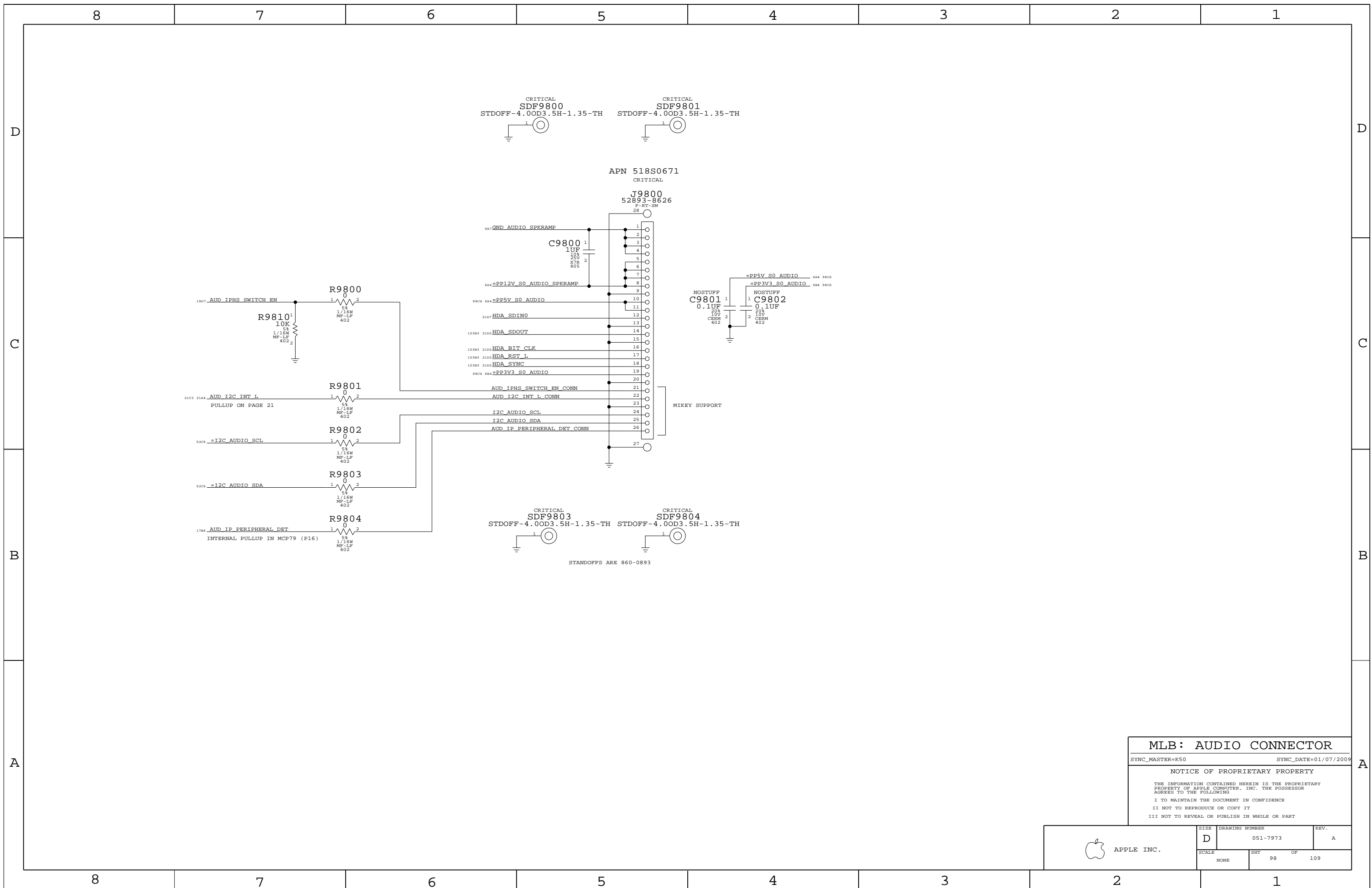
DisplayPort Connector

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	94	109	



MLB: AUDIO CONNECTOR

SYNC_MASTER=k50 SYNC_DATE=01/07/2009

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	SIZE	DRAWING NUMBER	REV.
	D	051-7973	A
SCALE	SHT	OF	109
NONE	98		

FSB (Front-Side Bus) Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include FSB_50S and FSB_DSTB_50S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include FSB_DATA, FSB_DSTB, FSB_ADDR, FSB_ADSTB, FSB_1X.

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADTSB#.

FSB 1X signals shown in signal table on right.

Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include CPU_50S and CPU_27P4S.

NOTE: 7 mil gap is for VCCsense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include CPU_AGTL, CPU_SMIL, CPU_COMP, CPU_GTLREF, CPU_ITP, CPU_VCCSENSE.

SR DG recommends at least 25 mils, >50 mils preferred

MOST CPU SIGNALS WITH IMPEDANCE REQUIREMENTS ARE 50-OHM SINGLE-ENDED.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes MCP_50S.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes MCP_FSB_COMP.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes CLK_FSB_100D.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes CLK_FSB.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

Large table listing electrical constraint sets, physical properties (layer, spacing), and signal names with IDs. Includes categories like FSB 4X Signal Groups, FSB 2X Signals, and FSB 1X Signals.

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CPU/FSB Constraints

SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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D 051-7973 A
SCALE NONE SHIT 100 OF 109

Memory Bus Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Rows include MEM_40S, MEM_40S_VDD, MEM_70D, MEM_70D_VDD.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Rows include MEM_CLK2MEM, MEM_CTRL2CTRL, MEM_CTRL2MEM, MEM_CMD2CMD, MEM_CMD2MEM, MEM_DATA2DATA, MEM_DATA2MEM, MEM_DQS2MEM, MEM_2OTHER.

Memory Bus Spacing Group Assignments

Table with 8 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_CLK, MEM_CTRL, MEM_CMD, MEM_DATA, MEM_DQS.

Table with 8 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_CTRL, MEM_DATA, MEM_CMD, MEM_DQS.

Table with 8 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Rows include MEM_DQS, MEM_CTRL, MEM_CMD, MEM_DATA, MEM_2OTHER.

Need to support MEM*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair. DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement. All DQS pairs should be matched within 100 ps of clocks. CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps. A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement. All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate). DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair. DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps No DQS to clock matching requirement. CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps. A/BA/cmd signals should be matched within 5 ps of CLK pairs. All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate). DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

Table with 8 columns: PHYSICAL_RULE_SET, LAYER, ALLOW ROUTE ON LAYER?, MINIMUM LINE WIDTH, MINIMUM NECK WIDTH, MAXIMUM NECK LENGTH, DIFFPAIR PRIMARY GAP, DIFFPAIR NECK GAP. Row includes MCP_MEM_COMP.

Table with 4 columns: SPACING_RULE_SET, LAYER, LINE-TO-LINE SPACING, WEIGHT. Row includes MCP_MEM_COMP.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

Table with 3 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING. Lists various net types like MEM_A_CLK, MEM_A_CMD, MEM_A_CKE, MEM_A_CS, MEM_A_ODT, MEM_A_A, MEM_A_BA, MEM_A_RAS, MEM_A_CAS, MEM_A_WE, MEM_A_DQ, MEM_A_DM, MEM_B_CLK, MEM_B_CMD, MEM_B_CKE, MEM_B_CS, MEM_B_ODT, MEM_B_A, MEM_B_BA, MEM_B_RAS, MEM_B_CAS, MEM_B_WE, MEM_B_DQ, MEM_B_DM.

Memory Net Properties

Table with 3 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, SPACING. Lists various net types like MEM_B_DQS0, MEM_B_DQS1, MEM_B_DQS2, MEM_B_DQS3, MEM_B_DQS4, MEM_B_DQS5, MEM_B_DQS6, MEM_B_DQS7, MCP_MEM_COMP, MCP_MEM_COMP_VDD, MCP_MEM_COMP_GND.

Memory Constraints

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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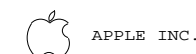


Table with 3 columns: DRAWING NUMBER (051-7973), REV. (A), SCALE (NONE), SHEET (101 OF 109).

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_E_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCI_E_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_E	*	=3X_DIELECTRIC	?	PCI_E	TOP,BOTTOM	=4X_DIELECTRIC	?
CLK_PCI_E	*	0.5 MM	?				
MCP_PEX_COMP	*	0.2 MM	?				

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?	SATA	TOP,BOTTOM	=3X_DIELECTRIC	?
SATA_TERM	*	0.2 MM	?				

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE	
	PCI_E_90D	PCI_E	PEG_R2D_C_P<15..0>	906 86A7 86B7 86C7 86D7
	PCI_E_90D	PCI_E	PEG_R2D_C_N<15..0>	906 86A7 86B7 86C7 86D7
	PCI_E_90D	PCI_E	PEG_D2R_P<15..0>	787 86A1 86B1 86C1 86D1 906
	PCI_E_90D	PCI_E	PEG_D2R_N<15..0>	787 86A1 86B1 86C1 86D1 906
	PCI_E_90D	PCI_E	MMX_PCI_E_R2D_P<15..0>	86A5 86B5 86C5 86D5 8A4B 8A8B
	PCI_E_90D	PCI_E	MMX_PCI_E_R2D_N<15..0>	86A5 86B5 86C5 86D5 8A4B 8A8B
	PCI_E_90D	PCI_E	MMX_PCI_E_D2R_P<7..0>	8408 86A4 86B4 86C4
	PCI_E_90D	PCI_E	MMX_PCI_E_D2R_P<8>	8408 86C4
	PCI_E_90D	PCI_E	MMX_PCI_E_D2R_P<15..9>	8488 8408 86A4 86D4
	PCI_E_90D	PCI_E	MMX_PCI_E_D2R_N<15..0>	8488 8408 86A4 86B4 86C4 86D4
	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_P	3406
	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_N	3406
	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_C_P	1783 3408
	PCI_E_90D	PCI_E	PCI_E_MINI_R2D_C_N	1783 3408
	PCI_E_90D	PCI_E	PCI_E_MINI_D2R_P	708 3408 1786
	PCI_E_90D	PCI_E	PCI_E_MINI_D2R_N	708 3408 1786
	PCI_E_90D	PCI_E	PCI_E_FW_R2D_P	706 4103
	PCI_E_90D	PCI_E	PCI_E_FW_R2D_N	706 4103
	PCI_E_90D	PCI_E	PCI_E_FW_R2D_C_P	1783 4101
	PCI_E_90D	PCI_E	PCI_E_FW_R2D_C_N	1783 4101
	PCI_E_90D	PCI_E	PCI_E_FW_D2R_P	708 4101 1786
	PCI_E_90D	PCI_E	PCI_E_FW_D2R_N	708 4101 1786
	PCI_E_90D	PCI_E	PCI_E_FW_D2R_C_P	4103
	PCI_E_90D	PCI_E	PCI_E_FW_D2R_C_N	4103
	CLK_PCI_E_100D	CLK_PCI_E	GPU_CLK100M_PCI_E_P	906 8705
	CLK_PCI_E_100D	CLK_PCI_E	GPU_CLK100M_PCI_E_N	906 8705 703
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_MINI_P	1703 3406
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_MINI_N	1703 3406
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_FW_P	706 1703 4102
	CLK_PCI_E_100D	CLK_PCI_E	PCI_E_CLK100M_FW_N	706 1703 4102
	MCP_HDMI_RSET	MCP_DV_COMP	MCP_HDMI_RSET	18A6 26C7
	MCP_HDMI_VPROBE	MCP_DV_COMP	MCP_HDMI_VPROBE	18A6 26C7
	MCP_PEX_CLK_COMP	MCP_50S	MCP_PEX_CLK_COMP	17A6
	MCP_IPFAB_RSET	MCP_DV_COMP	MCP_IPFAB_RSET	18A3 2606
	MCP_IPFAB_VPROBE	MCP_PEX_COMP	MCP_IPFAB_VPROBE	18A3 2606
	SATA_HDD_R2D	SATA_100D	SATA_HDD_R2D_C_P	2006 4505
	SATA_HDD_R2D	SATA_100D	SATA_HDD_R2D_C_N	2006 4505
	SATA_HDD_R2D	SATA_100D	SATA_HDD_R2D_P	4507
	SATA_HDD_R2D	SATA_100D	SATA_HDD_R2D_N	4507
	SATA_HDD_D2R_PP	SATA_100D	SATA_HDD_D2R_P	788 4505 2006
	SATA_HDD_D2R_PP	SATA_100D	SATA_HDD_D2R_N	788 4505 2006
	SATA_HDD_D2R_PP	SATA_100D	SATA_HDD_D2R_C_P	4507
	SATA_HDD_D2R_PP	SATA_100D	SATA_HDD_D2R_C_N	4507
	SATA_ODD_R2D	SATA_100D	SATA_ODD_R2D_C_P	2006 4505
	SATA_ODD_R2D	SATA_100D	SATA_ODD_R2D_C_N	2006 4505
	SATA_ODD_R2D	SATA_100D	SATA_ODD_R2D_P	4507
	SATA_ODD_R2D	SATA_100D	SATA_ODD_R2D_N	4507
	SATA_ODD_D2R_PP	SATA_100D	SATA_ODD_D2R_P	788 4505 2006
	SATA_ODD_D2R_PP	SATA_100D	SATA_ODD_D2R_N	788 4505 2006
	SATA_ODD_D2R_PP	SATA_100D	SATA_ODD_D2R_C_P	4507
	SATA_ODD_D2R_PP	SATA_100D	SATA_ODD_D2R_C_N	4507
	MCP_SATA_TERM	MCP_50S	MCP_SATA_TERM	20A6
	PM_SLP_S3_L		PM_SLP_S3_L	2103 784 907
	PM_SLP_S4_L		PM_SLP_S4_L	2103 784 3807 4905 5003 7008

MCP Constraints 1
 SYNC_MASTER=K50 SYNC_DATE=01/07/2009
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	D	051-7973	A
SCALE	SHT	OF	REV.
NONE	102	109	

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2X_DIELECTRIC	?
MCP_HDA_COMP	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

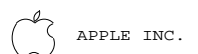
ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	783 1902 1907
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	783 1902 1907
PCI_CLK33M_MCP	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP_R	1905
PCI_CLK33M_MCP	CLK_PCI_55S	CLK_PCI	PCI_CLK33M_MCP	1905
LPC_AD	LPC_55S	LPC	LPC_AD<0>	1983 4908 5104 704
LPC_AD_2DP	LPC_55S	LPC	LPC_AD<1>	788 704 1983 4908 5104 704
LPC_AD	LPC_55S	LPC	LPC_AD<3..2>	1983 4908 5104 704
LPC_AD	LPC_55S	LPC	LPC_AD_E<3..0>	1985
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	1903 704 4908 5104
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_PU	5102
LPC_FRAME_R_L	LPC_55S	LPC	LPC_FRAME_R_L	1905 5101
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	1903 904
LPC_CLK33M	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	1983 984
LPC_CLK33M	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	982 4908
MCP_USB_CLK	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	982 704 5104
MCP_USB_CLK	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK_R	2183 984
MCP_USB_CLK	CLK_LPC_55S	CLK_LPC	PM_CLK32K_SUSCLK	982 4905
MCP_USB_RBIAS	MCP_USB_RBIAS	USB	MCP_USB_RBIAS_GND	2004
USB_EXT	USB_90D	USB	USB_EXT_A_P	2003 46A7
USB_EXT	USB_90D	USB	USB_EXT_A_N	2003 46A7
USB_EXT	USB_90D	USB	USB_PORT0_P	46A5
USB_EXT	USB_90D	USB	USB_PORT0_N	46A5
USB_EXT	USB_90D	USB	USB_EXTB_P	2003 46B6
USB_EXT	USB_90D	USB	USB_EXTB_N	2003 46B6
USB_EXT	USB_90D	USB	USB_PORT1_P	46B5
USB_EXT	USB_90D	USB	USB_PORT1_N	46B5
USB_EXT	USB_90D	USB	USB_EXTC_P	2003 46B3
USB_EXT	USB_90D	USB	USB_EXTC_N	2003 46B3
USB_EXT	USB_90D	USB	USB_PORT2_P	46B2
USB_EXT	USB_90D	USB	USB_PORT2_N	46B2
USB_EXT_MUXEN	USB_90D	USB	USB_EXTD_P	2003 46D5
USB_EXT_MUXEN	USB_90D	USB	USB_EXTD_N	2003 46D5
USB_D_MUXED	USB_90D	USB	USB_D_MUXED_P	46D4
USB_D_MUXED	USB_90D	USB	USB_D_MUXED_N	46D4
USB_MINI	USB_90D	USB	USB_PORT3_P	46D3
USB_MINI	USB_90D	USB	USB_PORT3_N	46D3
USB_MINI	USB_90D	USB	USB_MINI_P	2003 34B3
USB_MINI	USB_90D	USB	USB_MINI_N	2003 34B3
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	788 2003 47B7
USB_CAMERA	USB_90D	USB	USB_CAMERA_N	788 2003 47B7
USB_CAMERA	USB_90D	USB	USB_CAMERA_L_P	47B6
USB_CAMERA	USB_90D	USB	USB_CAMERA_L_N	47B6
USB_BT_PP	USB_90D	USB	USB_BT_P	788 2003 47D4
USB_BT_PP	USB_90D	USB	USB_BT_N	788 2003 47D4
USB_IR	USB_90D	USB	USB_IR_P	2003 47B4
USB_IR	USB_90D	USB	USB_IR_N	2003 47B4
USB_IR	USB_90D	USB	USB_IR_L_P	47B3
USB_IR	USB_90D	USB	USB_IR_L_N	47B3
SPI_CLK	MCP_50S	SPI	SPI_CLK_R	788 2183 51A6 6106
SPI_CLK	MCP_50S	SPI	SPI_CLK	6105
SPI_MOSI	MCP_50S	SPI	SPI_MOSI_R	2183 51A6 6102
SPI_MOSI	MCP_50S	SPI	SPI_MOSI	6104
SPI_MISO	MCP_50S	SPI	SPI_MISO_R	788 51A6 61B2 2183
SPI_MISO	MCP_50S	SPI	SPI_MISO	61B4
SPI_CS0	MCP_50S	SPI	SPI_CS0_R_L	2183 5106
SPI_CS0	MCP_50S	SPI	SPI_CS0_L	5107
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	2102 9806
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK_R	2104 21A7
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	2102 9806
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	2104 21A7
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	2102 9806
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT_R	2104 21A7
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	2102 9806
HDA_SYNC	HDA_55S	HDA	HDA_SYNC_R	2104 21A7

MCP Constraints 2

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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SCALE	SHT	OF
NONE	103	109

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MCP RGMI (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	0.2 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

RTL8211CLGR (ETHERNET PHY) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		NET_NAME	REF
	PHYSICAL	SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	1806
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	1806
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	1803 3883
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	3882 3786
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	1803 3786
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	1803 3786
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	3701 1806
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	3704
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	3701 1806
	ENET_MII_55S	ENET_MII	ENET_RXD_R<0>	3704
ENET_RXD_STEAD	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	3701 1806
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..1>	3704
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	3781 1806
	ENET_MII_55S	ENET_MII	ENET_RXCTL_R	3784
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	1803 3707
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<0>	1803 3706
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	1803 3706
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	1803 3786
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	3783 3905 3906 3907 3908
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	3783 3905 3906 3907 3908
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_P<3..0>	3901 3944 3945
	ENET_MDI_100D	ENET_MDI	ENET_MDI_T_N<3..0>	3901 3901 3944 3945

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Ethernet Constraints

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SCALE	SHT	OF
NONE	104	109

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE		
		PHYSICAL	SPACING	
FW_0_TPA	FW_110D	FW_TP		FW PORT0 TPA P 4202 438S
	FW_110D	FW_TP		FW PORT0 TPA N 4202 43CS
FW_0_TPB	FW_110D	FW_TP		FW PORT0 TPB P 4202 43CS
	FW_110D	FW_TP		FW PORT0 TPB N 4202 43CS
PORT 1 & 2 NOT USED				

D

D

C

C

B

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A

FireWire Constraints

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D	051-7973	A
SCALE	SHT	OF
NONE	105	109

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMB_55S	SMB	55OHM	SMBUS_SMC_A_S3_SCL	5202
SMB_55S	SMB	55OHM	SMBUS_SMC_A_S3_SDA	5202
SMB_55S	SMB	55OHM	SMBUS_SMC_B_S0_SCL	5205
SMB_55S	SMB	55OHM	SMBUS_SMC_B_S0_SDA	5205
SMB_55S	SMB	55OHM	SMBUS_SMC_O_S0_SCL	5205
SMB_55S	SMB	55OHM	SMBUS_SMC_O_S0_SDA	5205
SMB_55S	SMB	55OHM	SMBUS_SMC_BSA_SCL	5202
SMB_55S	SMB	55OHM	SMBUS_SMC_BSA_SDA	5202
SMB_55S	SMB	55OHM	SMBUS_SMC_MGMT_SCL	10403 5202
SMB_55S	SMB	55OHM	SMBUS_SMC_MGMT_SDA	10403 5202
SMB_55S	SMB	55OHM	SMBUS_SMC_MGMT_SCL	10403 5202
SMB_55S	SMB	55OHM	SMBUS_SMC_MGMT_SDA	10403 5202
SMB_55S	SMB	55OHM	SMBUS_MCP_O_CLK	1386 21C3 7A4 5208
SMB_55S	SMB	55OHM	SMBUS_MCP_O_DATA	1386 21C3 7A4 5208

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SMC Constraints

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NONE	106	109

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	0.5 MM	0.5 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
 DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
 DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
 Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP EG ML P<3..0>	8785 9187 9104 9108
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP IG ML P<3..0>	906 9187 9188 9104 9108
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP EG ML N<3..0>	8785 9188 9104 9108 9108
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP IG ML N<3..0>	906 9188 9108 9104 9108
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP ML P<3..0>	9185 9102 9105 9488 9401 9408
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP ML N<3..0>	9185 9102 9105 9105 9488 9401 9408
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP ML CONN P<3..0>	9404 9405
DP_ML_MXM3	DP_100D	DISPLAYPORT	DP ML CONN N<3..0>	9404 9405
DP_IG_AUX_CH	DP_100D	DISPLAYPORT	DP IG AUX CH P	1886 9308
DP_IG_AUX_CH	DP_100D	DISPLAYPORT	DP IG AUX CH N	1886 9308
DP_AUX_CH	DP_100D	DISPLAYPORT	DP AUX CH SW P	9306
DP_AUX_CH	DP_100D	DISPLAYPORT	DP AUX CH SW N	9306
DP_AUX_CH	DP_100D	DISPLAYPORT	DP AUX CH C P	9302 9304 9402
DP_AUX_CH	DP_100D	DISPLAYPORT	DP AUX CH C N	9302 9304 9402
DP_AUX_CH	DP_100D	DISPLAYPORT	DP EG AUXCH P	8746 9304
DP_AUX_CH	DP_100D	DISPLAYPORT	DP EG AUXCH N	8746 9304
LVDS_A_CLK_MXM3	LVDS_100D	LVDS	LVDS IG A CLK P	1883 8988
LVDS_A_CLK_MXM3	LVDS_100D	LVDS	LVDS IG A CLK N	1883 8988
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS IG A DATA P<3..0>	1883 8988 8908 8908
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS IG A DATA N<3..0>	1883 8988 8908 8908
LVDS_B_CLK_MXM3	LVDS_100D	LVDS	LVDS IG B CLK P	1883 8905
LVDS_B_CLK_MXM3	LVDS_100D	LVDS	LVDS IG B CLK N	1883 8905
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS IG B DATA P<3..0>	1883 8908 8905 8905
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS IG B DATA N<3..0>	1883 8908 8905 8905
LVDS_A_CLK_MXM3	LVDS_100D	LVDS	LVDS EG A CLK P	8705 8986
LVDS_A_CLK_MXM3	LVDS_100D	LVDS	LVDS EG A CLK N	8705 8986
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS EG A DATA P<3..0>	8705 8986 8906 8906 90A6 90A8
LVDS_A_DATA_MXM3	LVDS_100D	LVDS	LVDS EG A DATA N<3..0>	8705 8986 8906 8906 90A6 90A8
LVDS_B_CLK_MXM3	LVDS_100D	LVDS	LVDS EG B CLK P	8705 8903
LVDS_B_CLK_MXM3	LVDS_100D	LVDS	LVDS EG B CLK N	8705 8903
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS EG B DATA P<3..0>	8705 89A6 8903 8903 90A6 90A8
LVDS_B_DATA_MXM3	LVDS_100D	LVDS	LVDS EG B DATA N<3..0>	8705 89A6 8903 8903 90A6 90A8
	LVDS_100D	LVDS	LVDS EG A CLK L P	8985 90A8
	LVDS_100D	LVDS	LVDS EG A CLK L N	8985 90A8
	LVDS_100D	LVDS	LVDS EG B CLK L P	8902 90A8
	LVDS_100D	LVDS	LVDS EG B CLK L N	8902 90A8

GRAPHICS CONSTRAINTS

SYNC_MASTER=K50 SYNC_DATE=09/03/2008

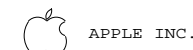
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SCALE	SHT	OF	109
NONE	107		

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PPDDR_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PPDDR_MEM	*	PWR_P2MM
MEM_CMD	PPDDR_MEM	*	PWR_P2MM
MEM_CTRL	PPDDR_MEM	*	PWR_P2MM
MEM_DATA	PPDDR_MEM	*	PWR_P2MM
MEM_DQS	PPDDR_MEM	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	600 MIL	VERRIDE	VERRIDE
MEM_40S_VDD_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	600 MIL	VERRIDE	VERRIDE
MEM_70D_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	600 MIL	VERRIDE	VERRIDE
PCIE_90D_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	500 MIL	VERRIDE	VERRIDE
USB_90D_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	500 MIL	VERRIDE	VERRIDE
MCP_IV_COMP_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	500 MIL	VERRIDE	VERRIDE
MCP_MEM_COMP_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	500 MIL	VERRIDE	VERRIDE
MCP_MII_COMP_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	500 MIL	VERRIDE	VERRIDE
MCP_USB_RBIA_OVERRIDE	TOP	VERRIDE	VERRIDE	0.1 MM	500 MIL	VERRIDE	VERRIDE
MCP_IV_COMP_OVERRIDE	*	VERRIDE	VERRIDE	0.25 MM	250 MIL	VERRIDE	VERRIDE
CPU_27F4S_OVERRIDE	BOTTOM	VERRIDE	VERRIDE	0.23 MM	100 MIL	VERRIDE	VERRIDE

K50/K51 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING		
		PPDDR_MEM	=PP1V5_S3 MEM A	603	31A8 31D7
		PPDDR_MEM	=PP1V5_S3 MEM B	603	32A5 32D7
		SWITCHNODE	IMVP6 PHASE1	71D4	71A6
		SWITCHNODE	IMVP6 PHASE2	71C4	71A4
		SWITCHNODE	IMVP6 PHASE3	72C6	72A7
		SWITCHNODE	1V8 SW	80C5	
		SWITCHNODE	1V05S5 SW	79C5	
		SWITCHNODE	F1V05S0 PHASE	76C6	
		SWITCHNODE	3V3S5 SW	76C3	
		SWITCHNODE	5V3S3 SW	73C5	
		SWITCHNODE	MCPCORES0 PHASE	74C5	
	THERM_DIFF	THERM_DIFF	THERMAL	SNS T DP1 DN6	55A8 55D6 55D8
	THERM_DIFF	THERM_DIFF	THERMAL	SNS T DN1 DP6	55A8 55D6 55D8
	THERM_DIFF	THERM_DIFF	THERMAL	SNS T DP2 DN3	55A8 55C6 55C8
	THERM_DIFF	THERM_DIFF	THERMAL	SNS T DN2 DP3	55A8 55C6 55C8
	THERM_DIFF	THERM_DIFF	THERMAL	CPU THERMD P	10C6 55D4
	THERM_DIFF	THERM_DIFF	THERMAL	CPU THERMD N	10C6 55D4
	THERM_DIFF	THERM_DIFF	THERMAL	SNS T DP4 DN5	55A8 5586 5588
	THERM_DIFF	THERM_DIFF	THERMAL	SNS T DN4 DP5	55A8 5586 5588
	THERM_DIFF	THERM_DIFF	THERMAL	MCP THMDIODE P	21C3 55C4
	THERM_DIFF	THERM_DIFF	THERMAL	MCP THMDIODE N	21C3 55C4
	THERM_DIFF	THERM_DIFF	THERMAL	MCP THMSNS D2 P	5583
	THERM_DIFF	THERM_DIFF	THERMAL	MCP THMSNS D2 N	5583
	THERM_DIFF	THERM_DIFF	THERMAL	MXM PWRSRC SENSOR P	53C4
	THERM_DIFF	THERM_DIFF	THERMAL	MXM PWRSRC SENSOR N	53C4
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE 12V S0 P	5383 5384
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE 12V S0 N	5383 5384
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE 12V S5 P	5383 53C4
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE 12V S5 N	5383 53C4
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE 1V5 S0 P	54D6
	THERM_DIFF	THERM_DIFF	THERMAL	SENSE 1V5 S0 N	54D6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS LCD P	55C7
	THERM_DIFF	THERM_DIFF	THERMAL	SNS LCD N	55C7
	THERM_DIFF	THERM_DIFF	THERMAL	SNS ODD P	55D7
	THERM_DIFF	THERM_DIFF	THERMAL	SNS ODD N	55D7
	THERM_DIFF	THERM_DIFF	THERMAL	SNS CPU H P	5587
	THERM_DIFF	THERM_DIFF	THERMAL	SNS CPU H N	5587
	THERM_DIFF	THERM_DIFF	THERMAL	SNS HDD P	55D6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS HDD N	55D6
	THERM_DIFF	THERM_DIFF	THERMAL	HDD OOB TEMP FILT	55D6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS AMB P	55C6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS AMB N	55C6
	THERM_DIFF	THERM_DIFF	THERMAL	SNS MXM P	5586
	THERM_DIFF	THERM_DIFF	THERMAL	SNS MXM N	5586
	THERM_DIFF	THERM_DIFF	THERMAL	MCP THMSNS FILT P	5584
	THERM_DIFF	THERM_DIFF	THERMAL	MCP THMSNS FILT N	5584

K50/K51 SPECIFIC CONSTRAINTS

SYNC_MASTER=K50 SYNC_DATE=01/07/2009

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	D	051-7973	A
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NONE	108	109	

K50/K51 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM	NO_TYPE, BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27F4_OHM_SE	TOP, BOTTOM	Y	0.345 MM	0.085 MM	=STANDARD		
27F4_OHM_SE	*	Y	0.275 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.19 MM	0.085 MM	=STANDARD		
40_OHM_SE	*	Y	0.15 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.125 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.1 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.125 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.121 MM	0.085 MM	=STANDARD	0.18 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.085 MM	=STANDARD	0.180 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP, BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	0.3 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
1:1_DIFFPAIR	TOP, BOTTOM	Y	=STANDARD	=STANDARD	=STANDARD	0.125 MM	0.085 MM

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.6 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP, BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP, BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP, BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP, BOTTOM	0.400 MM	?

CONSTRAINTS ARE BASED ON MCP79 DESIGN GUIDE DG-03328-001_V06
PCI, LPC, SMB, HDA, SPI, RGMII, SMBUS ARE ROUTED AS 55 OHM SE SIGNALS

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?
BGA_P3MM	*	0.3 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MCP_FSB_COMP	*	BGA_P1MM	BGA_P2MM
MCP_MEM_COMP	*	BGA_P1MM	BGA_P2MM
MCP_PEX_COMP	*	BGA_P1MM	BGA_P2MM
MCP_HDA_COMP	*	BGA_P1MM	BGA_P2MM

K50/K51 RULE DEFINITIONS

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