**K36B MLB SCHEMATIC**

1. All capacitance values are in microfarads; 0.1 watt ± 5%.
2. All resistance values are in ohms, 0.1 watt ± 5%.

---

**Schematic / PCB #’s**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE LOG</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Table of Contents**

- System Block Diagram
- Power Block Diagram
- Configuration Options
- Revision History
- JTAG JTAG Chain
- Pin Test
- Power Aliases
- Signal Alias
- CPU Power & Ground
- MCP CPU Interface
- MCP Memory Interface
- MCP PCH Interface
- MCP Controller & Translator
- MCP PCH & ACP
- MCP SATA & GUI
- MCP DMA & PED
- MCP Power & Ground
- MCP’s 65W Power Support
- MCP Standard Enclosure
- MCP Graphic Support
- JU Tests
- FLEXBASE UEP MACHINING
- DQ12 3G-SMB Connector A
- DQ12 3G-SMB Connector B
- Memory Active Termination
- Sleep & Sata Support
- Ethernet PHY (10/100)
- Ethernet PHY (10/100)
- Ethernet PHY (10/100)
- Ethernet PHY (10/100)
- Ethernet PHY (10/100)

---

**Release**

12/23/2008 © APPLE INC.

NOTICE OF PROPRIETARY PROPERTY

The information contained herein is the proprietary property of Apple Inc. and may not be copied, transmitted, or disclosed to others in whole or in part. This document is the property of Apple Inc. and is not to be used, copied, or reproduced for any other purpose.

---

**BOM Option**

- 051-7852

---

**Metric**

**Notice of Proprietary Property**

The information contained herein is the proprietary property of Apple Inc. and may not be copied, transmitted, or disclosed to others in whole or in part. This document is the property of Apple Inc. and is not to be used, copied, or reproduced for any other purpose.
### Board Stack-up and Construction

<table>
<thead>
<tr>
<th>Top</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>GROUND</td>
</tr>
<tr>
<td>3</td>
<td>SIGNAL (High Speed)</td>
</tr>
<tr>
<td>4</td>
<td>SIGNAL (High Speed)</td>
</tr>
<tr>
<td>5</td>
<td>GROUND</td>
</tr>
<tr>
<td>6</td>
<td>POWER</td>
</tr>
<tr>
<td>7</td>
<td>POWER</td>
</tr>
<tr>
<td>8</td>
<td>GROUND</td>
</tr>
<tr>
<td>9</td>
<td>SIGNAL (High Speed)</td>
</tr>
<tr>
<td>10</td>
<td>SIGNAL (High Speed)</td>
</tr>
<tr>
<td>11</td>
<td>GROUND</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bottom</th>
<th>SIGNAL</th>
</tr>
</thead>
</table>

### BOM Option

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
<th>BOOTROM_PROG</th>
<th>SMC_PROG</th>
</tr>
</thead>
<tbody>
<tr>
<td>338S0694</td>
<td>IC, GMCP, MCP79, 35X35MM, BGA1437, B03</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>338S0702</td>
<td>IC, RTL8251CA-VB-GR, GIGE TRANSCEIVER, 48P</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>338S0654</td>
<td>IC, FW643E, 1394B PHY/OHCI LINK/PCI-E, 127</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>337S3693</td>
<td>IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>514-0669</td>
<td>LBL, P/N LABEL, PCB, 28MMX6MM</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>514-0668</td>
<td>PDC, SLGE3, PRQ, 2.0GHz, 25W, 1066, R0, 3M, BGA</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>514-0667</td>
<td>IC, CYPRESS, CY7C63833</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>514-0666</td>
<td>IC, GMCP, MCP79, 35X35MM, BGA1437, B03</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Alternate Options

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
<th>BOOTROM_PROG</th>
<th>SMC_PROG</th>
</tr>
</thead>
<tbody>
<tr>
<td>152S0778</td>
<td>IC, RTL8251CA-VB-GR, GIGE TRANSCEIVER, 48P</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0693</td>
<td>IC, FW643E, 1394B PHY/OHCI LINK/PCI-E, 127</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0796</td>
<td>IC, FLASH, SPI, 32MBIT, 3.3V, 86MHZ, 8-SOP</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0685</td>
<td>LBL, P/N LABEL, PCB, 28MMX6MM</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0874</td>
<td>PDC, SLGE3, PRQ, 2.0GHz, 25W, 1066, R0, 3M, BGA</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0516</td>
<td>IC, CYPRESS, CY7C63833</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>152S0847</td>
<td>IC, GMCP, MCP79, 35X35MM, BGA1437, B03</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Configuration Options

**SYNC_MASTER=K36B_MLB**

**SYNC_DATE=08/17/2008**

Notice of Proprietary Property:

The Information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

1. Not to disclose or publish it in whole or part.
2. Not to reproduce or copy it.
3. To maintain the document in confidence.

For the information regarding the use of this documentation, please refer to the accompanied documentation. It may not be to reproduce or copy it.

For any inquiries or further assistance, please contact the appropriate department.
- R0602 BOM OPTION FROM JTAG_1DEV CHANGE TO NO STUFF.
- R7859 CHANGE TO 100 OHM.
- CHANGE R9460, R9461 TO 0 OHM.
- C7601 FROM 138S0578 CHANGE TO 138S0614.
- Q7500 FROM 376S0512 CHANGE TO 376S0652.
- C7343 FROM 128S0073 CHANGE TO 128S0233.

- RTC FOLLOW M97 DESIGN AND USE SUPERCAP SOLUTION.

- C7291, C7292, C7252, C7251 FROM 128S0115 (POLY, CASE-B2) CHANGE TO
  C7281, C7241, C7272 FROM 138S0555 (603) CHANGE TO 138S0615 (603-1)

- ADD =PP3V3_S5_P3V3ENETFET LINK TO PP3V3_S5.
- SMC_NB_DDR_ISENSE CHANGE TO SMC_MCP_DDR_ISENSE.
- CHANGE XDP_TDO_CONN TO XDP_TDO.
- ADD =RTL8211_REGOUT LINK TO NC_RTL8211_REGOUT.

- R2400~R2413 FOR MCP A01 VERSION.
- R5280/R5281 = 1K (FOLLOW M97D)
- MCP S0 PWRGD FOLLOW M97 DESIGN
- R5417 ADD BOM OPTION FOR NO STUFF
- XDP FOLLOW M97 DESIGN. CONNECTOR FROM 998-1571 CHANGE TO 516S0625.
- XDP FOLLOW M98 DESIGN. CONNECTOR FROM 516S0625 CHANGE TO 998-1571.
- ADD SMC_EXCARD_PWR_EN TEST_POINT

- REMOVE R9010, R9011

- REMOVE R3400, R3401

- L3401 FROM NO STUFF CHANGE TO STUFF.

- C9003 CHANGE TO 116S0004 (0 ohm, 5%, 0402)
- J6950 516S0735 CHANGE TO 516S0620
- J3400 516S0729 CHANGE TO 516S0635
- C4803 CHANGE TO 138S0614
- I2C_ALS_SDA CHANGE TO I2C_MINI_PCIE_SDA
- C6605 CHANGE TO HF APN 128S0221, HF APN 128S0148, and REMOVE BOM OPTION OMIT
- R5416 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5417 CHANGE TO 4.53K AND DELETE BOM OPTION.
- R5418 CHANGE TO 4.53K AND DELETE BOM OPTION.

- REMOVE USB_PWR_EN_S3
- R1860 AND R1861 CHANGE TO PAGE 68.

- REMOVE J9001 PIN 20 AND PIN21 NET.

- ADD SMC_SYS_KBDLED TO NC_SMC_SYS_KBDLED

- ADD R5055 10KOHM LINK SMC_NB_MISC_ISENSE PULL DOWN TO GND.
- ADD SMC_ANALOG_ID TO NC_SMC_ANALOG_ID
- ADD SMC_RSTGATE_L TO TP_SMC_RSTGATE_L

- NET DPMUX_SEL_IG_L SYNC M97 NETNAME

- NET ENETINTR_L CHANGE TO TP_ENETINTR_L.

- R5164 and R5144 changed to 10K 5% 0402 (116S0090)
- BOM change U1400 CHANGE FROM 338S0678 TO 338S0702
- U3700 CHANGE FROM 338S0570 TO 338S0694
- U4100 CHANGE FROM 338S0523 TO 338S0654
- U1000 CHANGE FROM 373S3646 TO 373S3702

- REMOVE ALT TABLE

- REMOVE ALT TABLE

- REMOVE K36 BOM OPTION TABLE AND ALT TABLE

- ADD R3731 (116S0026 22 ohm 5% 0402) FOR EMI 125MHZ NOISE

- REMOVE BOMOPTION TABLE OF R2903/R2905/R2909/R2911
1.05V TO 3.3V LEVEL TRANSLATOR (K36B: ON ICT FIXTURE)

From XDP connector

CPU

U1000

To XDP connector

and/or level translator

From XDP connector

MCP

U1400

or via level translator

XDP connector
## Functional Test Points

### A. #J5600 Fan Connectors
- TRUE

### B. #J6050 Battery/Lid Connector
- TRUE

### C. #J6500 MagSafe DC Power Jack
- TRUE

### D. #J8000 INVERTER Connector
- TRUE

### B. #J9000 LCD + CAMERA CONNECTOR
- TRUE

### A. #J6700 MIC CONNECTOR
- TRUE

### B. #J6702 Left SPEAKER CONNECTOR
- TRUE

### B. #J6703 Right SPEAKER CONNECTOR
- TRUE

### A. #J5800 HEATSINK AND CPU/RM REMOTE TEMP SENSORS
- TRUE

### A. #J5520 CPU/RM Thermal Sensor
- TRUE

### A. #J4810 BLUETOOTH
- TRUE

### A. #J4500 SATA ODD
- TRUE

### # J4501 SATA HD System LED and IR
- TRUE

### #J1300 XDP
- TRUE

### # J5100 LPC+SPI Connector
- TRUE

---

**NOTICE OF PROPRIETARY PROPERTY**

The information contained herein is the proprietary property of Apple Inc. It is not to be disclosed or reproduced in whole or part, in any manner, without the prior written consent of Apple Inc.

---

APPLE INC.
Current numbers from Merom for Santa Rosa EMTS, doc #20905.

CHANGE CPU FROM SOCKET TO BGA SYMBOL

SYNC FROM T18
CHANGE CPU FROM SOCKET TO BGA SYMBOL
CPU VCore HF and Bulk Decoupling

VCCA (CPU AVdd) DECOUPLING

VCCP (CPU I/O) DECOUPLING

Sync from T18

Place inside sockets, torque to mounting stud(s).

Place on secondary side.

Place inside socket cavity on secondary side.
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

See with XDP-XDP adapter board to support CPU XDP debugging.

MCP79-specific pinout

Direction of XDP module

PLACEMENT NOTE=Place close to CPU to minimize stub.

SYNC_DATE=01/08/2008

SYNC_MASTER=M99_MLB

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR TO MAINTAIN THE DOCUMENT IN CONFIDENCE

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY NOTICE OF PROPRIETARY PROPERTY
NOTE: All Apple products are not designed to include dual-channel TMDS without pull-downs. A pull-down resistor of at least 0.33A should be used on all TMDS signals. If left open, the TMDS signals will be left floating.

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.

NOTE: All Apple products require pull-up resistors on all unused signals via software. This is required to maintain the document in confidence.

NOTE: All Apple products set strap to 1 to activate this feature.

NOTE: All Apple products set strap to 1 to activate this feature.

NOTE: All Apple products set strap to 1 to activate this feature.

NOTE: All Apple products set strap to 1 to activate this feature.

NOTE: All Apple products set strap to 1 to activate this feature.

NOTE: All Apple products set strap to 1 to activate this feature.
SYNC FROM T18
REMOVE MCP 27MHZ CRYSTAL CIRCUIT SINCE NOT SUPPORTING TV-OUT
REMOVE DAC TERMINATIONS R2665, C2665 AND R2670 TO R2672
Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE

Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE

Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE

Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE

Voltage divider resistor values at op-amp outputs not yet finalized.

BOM OPTION TO SELECT VREF SOURCE

Voltage divider resistor values at op-amp outputs not yet finalized.
Page Notes

- DDR2-800
- DDR2-667

BOM options provided by this page:

- NONE
- =I2C_MEM_SCL

Work allowed required by this page.

- 4V0V_4V0V (2.5V - 3.3V)

Optional items provided by this page:

- 30V_30V

The 4.7uF and 1.0uF caps can be changed to 2x 2.2uF caps, when they get cheaper.
PLACE ONE CAP EACH NEAR PINS 3 AND 4 OF T3901 AND T3902.
FireWire Port Power Switch

- FW_PORT_FAULT_PU

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PPVP_FW_SUMNODE (power passthru summation node)
- =PP3V3_FW_LATEVG_ACTIVE

Signal aliases required by this page:
- =PP3V3_FW_LATEVG
- =PP2V4_FW_LATEVG

BOM options provided by this page:

- FW_PORT_P3.3V_PU

Page Notes

- CRITICAL

Late-VG Event Detection

- FWLATEGV_3V_REF
- P2V4_FWLATEVG_RC

Enables port power when machine is running or on AC.

FW_PORTPWR_EN enable port power when machine is running or on AC.

FW_PORTPWR_EN_FET enables port power when machine is running or on AC.

CRITICAL

VOLTAGE=12.6V

MIN_LINE_WIDTH=0.5 mm

MIN_NECK_WIDTH=0.25 mm

PPBUS_FW_FWPWRSW_F

PPBUS_FW_FWPWRSW_D

APPLE INC.
FireWire PHY Config Straps

Configures PHY for:
- 1-port Portable Power Class (0)

Late-VG Protection Power

PP2V4_FW_LATEVG needs to be biased to at least 2.4V for Port 1 and should be biased to 2.0V for ports 2 and 3.

FireWire Ports

- FIREWIRE_PORT1
  - 37
  - 37
  - 37

Cable Power

Critical

PORT 1

12500 12500 12500 12500

Page Notes

- Power aliases required by this page:
  - GND_CHASSIS_FW_EMI_R
  - GND_CHASSIS_FW_PORT1

- BOM options provided by this page:
  - GND_CHASSIS_FW_EMI_R
  - GND_CHASSIS_FW_PORT1

- FireWire TPA/TPB pairs are NOT assumed that FireWire PHY page will provide the appropriate constraints to apply to native TRAPo/TPB pairs. 

A
- Page Notes

B
- A

C
- D

D
- C

Note: This page is expected to contain the necessary aliases to map the FireWire TRAPo/TPB pairs to their appropriate connections and/or to properly terminate unused signals.

Note: FireWire TPA/TPB pairs are NOT constrained on this page. It will provide the appropriate constraints to apply to native TRAPo/TPB pairs.

Note: Implementation based on Apple Firewire Design Guide (FWDG 0.6, 5/14/03)
some extracted text
Alternate SPI ROM Support

SPI Bus Series Resistance Option
DETECT FIN-STACK TEMPERATURE

DETECT HEAT-PIPE TEMPERATURE

DETECT CPU DIE TEMPERATURE

DETECT MCP DIE TEMPERATURE

CPU T-Diode Thermal Sensor

MCP T-Diode Thermal Sensor

INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE

INTERNAL DIODE IN U5515 DETECTS CPU PROXIMITY TEMPERATURE

PLACEMENT NOTE: PLACE U5535 NEAR MCP

PLACEMENT NOTE: PLACE U5515 NEAR CPU

C5515 0.1uF CERM 402

C5535 0.1uF CERM 402

R5516 10K

R5536 10K

R5517 10K

R5537 10K

CERM

CERM

SIGNAL_MODOL=EMPTY

SIGNAL_MODOL=EMPTY

SIGNAL_MODOL=EMPTY

SIGNAL_MODOL=EMPTY

VOLTAGE=3.3V

VOLTAGE=3.3V

VOLTAGE=3.3V

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.25 mm

MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=0.25 mm

MIN_LINE_WIDTH=0.25 mm

MCP T-Diode Thermal Sensor

CPU T-Diode Thermal Sensor

INTERNAL DIODE IN U5535 DETECTS MCP PROXIMITY TEMPERATURE

INTERNAL DIODE IN U5515 DETECTS CPU PROXIMITY TEMPERATURE

PLACEMENT NOTE: PLACE U5535 NEAR MCP

PLACEMENT NOTE: PLACE U5515 NEAR CPU

C5515 0.1uF CERM 402

C5535 0.1uF CERM 402

R5516 10K

R5536 10K

R5517 10K

R5537 10K

CERM

CERM

SIGNAL_MODOL=EMPTY

SIGNAL_MODOL=EMPTY

SIGNAL_MODOL=EMPTY

SIGNAL_MODOL=EMPTY

VOLTAGE=3.3V

VOLTAGE=3.3V

VOLTAGE=3.3V

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.25 mm

MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=0.25 mm

MIN_LINE_WIDTH=0.25 mm

Internal to Outside Highlighting
25 MHz is selected with R5164 and R5144
Any of the 4 frequencies can be selected
with R6190, R6191, R5164, and R5144
1.8V/0.9V (DDR2) POWER SUPPLY

VOUT = 0.75V * (1 + RA / RB)

MAX CURRENT = 12A

PWM FREQ. = 400 KHZ

PUT ONE BULK CAP NEXT TO THE LOAD

1.8V/0.9V DDR2 SUPPLY

<table>
<thead>
<tr>
<th>STATE</th>
<th>PM_SLP_S4_L</th>
<th>PM_SLP_S3_L</th>
<th>PP1V8_S3</th>
<th>PP0V9_S0</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>HIGH</td>
<td>HIGH</td>
<td>1.8V</td>
<td>0.9V</td>
</tr>
<tr>
<td>S3</td>
<td>HIGH</td>
<td>LOW</td>
<td>1.8V</td>
<td>0.9V</td>
</tr>
<tr>
<td>S1/G3HOT</td>
<td>LOW</td>
<td>LOW</td>
<td>0.0V</td>
<td>0.0V</td>
</tr>
</tbody>
</table>
CPUVT TT POWER SUPPLY
FireWire 1.0V (Core) Supply

MCP 1.05V_S5 AUXC Supply

1.5V S0 Switch

MISC POWER SUPPLIES

NOTICE OF PROPRIETARY PROPERTY

NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

NOT TO REPRODUCE OR COPY IT

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

SHT 1/1
REV. D
051-7852
109

DIMENSIONS
SCALE

NONE

APPLE INC.
### FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>MINIMUM DISTANCE</th>
<th>MAXIMUM DISTANCE</th>
<th>notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_MCP_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_MCP_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_ITP_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_ITP_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_DSTB_N_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_DSTB_N_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
</tbody>
</table>

### CPU Signal Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>MINIMUM DISTANCE</th>
<th>MAXIMUM DISTANCE</th>
<th>notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_BSEL_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>CPU_BSEL_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>CPU_PWRGD_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>CPU_PWRGD_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>CPU_FERR_L</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>CPU_ASYNC</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
</tbody>
</table>

### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Net Name</th>
<th>MINIMUM DISTANCE</th>
<th>MAXIMUM DISTANCE</th>
<th>notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_DSTB_L_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_DSTB_L_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_ADS_L</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_BPRI_L</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_BREQ0_L</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_BREQ1_L</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_LOCK_L</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_DINV_L</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
</tbody>
</table>

### FSB Clock Constraints

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>MINIMUM DISTANCE</th>
<th>MAXIMUM DISTANCE</th>
<th>notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_MCP_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_MCP_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_ITP_P</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_ITP_N</td>
<td>3x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
<td></td>
</tr>
</tbody>
</table>

---

**SOURCE:** MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

Signals within each group should be matched within 5 ps of strobe.

Signals within each group should be matched within 25 mils, >50 mils preferred.

**SOURCE:** Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

**SOURCE:** MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB 1X signals shown in signal table on right.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

Most CPU signals with impedance requirements are 55-ohm single-ended.

FSB 1X = STANDARD

**SOURCE:** Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

Some signals require 27.4-ohm single-ended impedance.

Design Guide recommends each strobe/signal group is routed on the same layer.

---

**TABLE**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Min to Min</th>
<th>Min to Adj</th>
<th>Adj to Adj</th>
<th>Adj to Min</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
<tr>
<td>2</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
<tr>
<td>3</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
<tr>
<td>4</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
</tbody>
</table>

---

**TABLE**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Min to Min</th>
<th>Min to Adj</th>
<th>Adj to Adj</th>
<th>Adj to Min</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
<tr>
<td>2</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
<tr>
<td>3</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
<tr>
<td>4</td>
<td>25 MIL</td>
<td>50 MIL</td>
<td>25 MIL</td>
<td>50 MIL</td>
</tr>
</tbody>
</table>
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

DDR3:

DQS signals should be matched within 20 ps of associated DQS pair.

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.
- 75-ohm from output of three-pole filter to connector (if possible).

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.
- 37.5-ohm from MCP to first termination resistor.
# FCU Bus Constraints

<table>
<thead>
<tr>
<th>NET</th>
<th>TYPE</th>
<th>LAYER</th>
<th>MINIMUM WIDTH</th>
<th>MAXIMUM WIDTH</th>
<th>MINIMUM SPACING</th>
<th>MAXIMUM SPACING</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDA_SDIN0</td>
<td>USB</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>HDA_RST_L</td>
<td>SMB</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>MCP_HDA_COMP</td>
<td>SPI</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
</tbody>
</table>

# LPC Bus Constraints

<table>
<thead>
<tr>
<th>NET</th>
<th>TYPE</th>
<th>LAYER</th>
<th>MINIMUM WIDTH</th>
<th>MAXIMUM WIDTH</th>
<th>MINIMUM SPACING</th>
<th>MAXIMUM SPACING</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB_MINI</td>
<td>USB</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>SPI_MISO</td>
<td>SPI</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>SPI_MOSI_MUX</td>
<td>SPI</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
</tbody>
</table>

# USB 2.0 Interface Constraints

<table>
<thead>
<tr>
<th>NET</th>
<th>TYPE</th>
<th>LAYER</th>
<th>MINIMUM WIDTH</th>
<th>MAXIMUM WIDTH</th>
<th>MINIMUM SPACING</th>
<th>MAXIMUM SPACING</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB_BT_N</td>
<td>USB</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>USB_BT_P</td>
<td>USB</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>USB_BT_F_CONN</td>
<td>USB</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
</tbody>
</table>

# SPI Interface Constraints

<table>
<thead>
<tr>
<th>NET</th>
<th>TYPE</th>
<th>LAYER</th>
<th>MINIMUM WIDTH</th>
<th>MAXIMUM WIDTH</th>
<th>MINIMUM SPACING</th>
<th>MAXIMUM SPACING</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI_CS0_L</td>
<td>SPI</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>SPI_CLK</td>
<td>SPI</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
</tbody>
</table>

# SIO Signal Constraints

<table>
<thead>
<tr>
<th>NET</th>
<th>TYPE</th>
<th>LAYER</th>
<th>MINIMUM WIDTH</th>
<th>MAXIMUM WIDTH</th>
<th>MINIMUM SPACING</th>
<th>MAXIMUM SPACING</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPI_MISO_R</td>
<td>SPI</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
<tr>
<td>SPI_MOSI_MUX</td>
<td>SPI</td>
<td>8</td>
<td>6 mil</td>
<td>20 mil</td>
<td>6 mil</td>
<td>20 mil</td>
</tr>
</tbody>
</table>
### MCP RGMII (Ethernet) Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Allow Route</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>=55_OHM_SE</td>
<td>MINIMUM LINE WIDTH</td>
</tr>
<tr>
<td>7</td>
<td>=100_OHM_DIFF</td>
<td>MAXIMUM NECK LENGTH</td>
</tr>
<tr>
<td>6</td>
<td>=STANDARD</td>
<td>MINIMUM NECK WIDTH</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>DIFFPAIR PRIMARY GAP</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>DIFFPAIR NECK GAP</td>
</tr>
</tbody>
</table>

### ON LAYER?

<table>
<thead>
<tr>
<th>Layer</th>
<th>SPACING RULE SET</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>PHYSICAL RULE SET</td>
</tr>
<tr>
<td>7</td>
<td>ELECTRICAL RULE SET</td>
</tr>
<tr>
<td>6</td>
<td>SPACING RULE SET</td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

### Table of Spacing Rule Items

<table>
<thead>
<tr>
<th>Rule Item</th>
<th>Rule Item</th>
<th>Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td>LINE-TO-LINE SPACING</td>
<td>ON LAYER?</td>
<td>ALLOW ROUTE</td>
</tr>
</tbody>
</table>

### Table of Physical Rule Items

<table>
<thead>
<tr>
<th>Rule Item</th>
<th>Rule Item</th>
<th>Rule Item</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINIMUM LINE WIDTH</td>
<td>MAXIMUM NECK LENGTH</td>
<td>DIFFPAIR PRIMARY GAP</td>
</tr>
</tbody>
</table>

### Table of Electrical Rule Items

<table>
<thead>
<tr>
<th>Physical Rule Set</th>
<th>Electrical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP_BUF0_CLK</td>
<td>ENET_PWRDWN_L</td>
</tr>
<tr>
<td>ENET_MDC</td>
<td>ENET_RST_L</td>
</tr>
<tr>
<td>ENET_TXseries</td>
<td>ENET_CLK125M_TXCLK</td>
</tr>
<tr>
<td>ENET_CLK125M_RXCLK</td>
<td></td>
</tr>
<tr>
<td>ENET_CLK125M_TXCLK_R</td>
<td></td>
</tr>
<tr>
<td>ENET_CLK125M_RXCLK_R</td>
<td></td>
</tr>
</tbody>
</table>

### ENET_MDC (Ethernet PHY) Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>LAYER 8</td>
<td>55_OHM_SE</td>
</tr>
<tr>
<td>LAYER 7</td>
<td>100_OHM_DIFF</td>
</tr>
<tr>
<td>LAYER 6</td>
<td>STANDARD</td>
</tr>
<tr>
<td>LAYER 5</td>
<td></td>
</tr>
<tr>
<td>LAYER 4</td>
<td></td>
</tr>
<tr>
<td>LAYER 3</td>
<td></td>
</tr>
<tr>
<td>LAYER 2</td>
<td></td>
</tr>
<tr>
<td>LAYER 1</td>
<td></td>
</tr>
</tbody>
</table>
### SMCSMBus Net Properties

<table>
<thead>
<tr>
<th>Net_Type</th>
<th>Min_Spacing</th>
<th>Phys_Spacing</th>
<th>Min_Neck</th>
<th>Max_Neck</th>
<th>Min_Gap</th>
<th>Max_Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBus_SMC_B_S0_SCL</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBus_SMC_B_SA_SDA</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
</tbody>
</table>

### SMBus Charger Net Properties

<table>
<thead>
<tr>
<th>Net_Type</th>
<th>Min_Spacing</th>
<th>Phys_Spacing</th>
<th>Min_Neck</th>
<th>Max_Neck</th>
<th>Min_Gap</th>
<th>Max_Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSO</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSO_N</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
</tbody>
</table>

### SMC Constraints

**NOTICE OF PROPRIETARY PROPERTY**

The information contained herein is the proprietary property of Apple Inc. The possessor agrees to the following:

I. Not to reproduce or copy it

II. Not to reveal or publish in whole or part

III. To maintain the document in confidence

**SYNC_DATE=08/17/2008**

**SYNC_MASTER=K36B_MLB**

**APPLE INC.**

**DRAWING NUMBER**

**REV.**

**TABLE_PHYSICAL_RULE_HEAD**

**ELECTRICAL_CONSTRAINT_SET**

**PHYSICAL**

**SPACING**

**NET_TYPE**

**SCALE**
## K36B Board-Specific Spacing & Physical Constraints

### Board Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>ISL3</th>
<th>ISL4</th>
<th>ISL9</th>
<th>ISL10</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>N</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
</tr>
</tbody>
</table>

### Minimum Line Width

- **Default**: 0.115 mm, 0.115 mm
- **Standard**: 0.076 mm, 0.090 mm
- **Minimum Neck Width**: 0.077 mm, 0.077 mm
- **Maximum Neck Length**
- **Line-to-Line Spacing**
- **Area Type**
- **Net Physical Type**

### Space_Pair Primary Gap

- **Standard**: 0.230 mm
- **Default**: 0.200 mm

### Space_Pair Neck Gap

- **Standard**: 0.200 mm
- **Default**: 0.175 mm

### Physical Rule Set

- **5X Dielectric**
- **4X Dielectric**
- **3X Dielectric**
- **2X Dielectric**
- **1.5:1 Spacing**
- **4:1 Spacing**

### Table Physical Rule Item

<table>
<thead>
<tr>
<th>Item</th>
<th>TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, BOTTOM</th>
</tr>
</thead>
<tbody>
<tr>
<td>LAYER</td>
<td></td>
</tr>
<tr>
<td>Y</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td></td>
</tr>
</tbody>
</table>

### Table Physical Rule Head

- **Table Physical Rule Item**
- **Table Physical Rule Assignment**
- **Table Physical Rule Definitions**

### Table Spacing Rule Item

- **Table Spacing Rule Assignment**
- **Table Spacing Rule Definitions**

### Table Area Type

- **BGA_P1MM**
- **BGA_P2MM**
- **BGA_P3MM**
- **BSB_DSTB**

### Table Net Physical Type

- **CLK_PCI**
- **CLK_FSB**

---

*This content is for informational purposes only and is not to be reproduced or copied without the express written consent of Apple, Inc.*