### Table of Contents

<table>
<thead>
<tr>
<th>Page</th>
<th>Contents</th>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Table of Contents</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>System Block Diagram</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Power Block Diagram</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>ROM Configuration</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Power Con / Alias</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>MILS</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>USB SIGNAL ALIAS</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Signal Alias</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>DDR FAN</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>USB Test &amp; Misc</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>CPU Power &amp; Decaps</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Extended USB Power [MSP]</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>NP GPO Interface</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>NP Memory Interface</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>NP POWER (Inst &amp; Misc)</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>NP Bias Interface</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>NP Ethernet &amp; Graphics</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>NP Eth &amp; PCIe</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>NP DATA &amp; Misc</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>NP GPO &amp; Misc</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>NP Power &amp; Ground</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>NP Standard Designing</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>NP Graphic Support</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>NP Bias</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>FET/ ORK Vref Marginig</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>Memory Care</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>USB 400-PIN CONNECTOR A</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>USB 400-PIN CONNECTOR B</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>IDEAL SUPPORT &amp; BIMAPS</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>PUT-W Wireless Controller</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Ethernet PHY (88271/88118)</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Ethernet Support</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Ethernet Connector</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Firewire Controller [x02/03/04]</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>Firewire Connector</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>DATA Connectors</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>External USB Connectors</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>Internal USB Connectors</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>USB Support</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>IDE Support</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>Reset B busy Connector</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>IDEAL SUPPORT</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>IDEAL Connectors</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>CPU/DRAM CURRENT AND VOLTAGE SENSE</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>NP CURRENT AND VOLTAGE SENSE</td>
<td></td>
</tr>
</tbody>
</table>

---

1. All resistance values are in ohms; 0.1 watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystal & oscillator values are in hertz.
BOARD STACK-UP

<table>
<thead>
<tr>
<th>TOP</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>GROUND</td>
</tr>
<tr>
<td>3</td>
<td>SIGNAL</td>
</tr>
<tr>
<td>4</td>
<td>POWER</td>
</tr>
<tr>
<td>5</td>
<td>POWER</td>
</tr>
<tr>
<td>6</td>
<td>SIGNAL</td>
</tr>
<tr>
<td>7</td>
<td>GROUND</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BOTTOM</th>
<th>SIGNAL</th>
</tr>
</thead>
</table>
MCP79-specific pinout

- **CPU_XDP_BPMB<2>**
- **CPU_XDP_BPMB<0>**
- **XDP_OBS20**
- **SMBUS_MCP_0_DATA**
- **CPU_XDP_TCK**
- **CPU_XDP_TRST_LSMBUS_MCP_0_CLK**
- **PM_LATRIGGER_L**
- **JTAG_MCP_TCK**
- **XDP_PWRGD**
- **XDP_DBRESET_L**
- **MCP_DEBUG<7>**
- **MCP_DEBUG<6>**
- **MCP_DEBUG<5>**
- **MCP_DEBUG<4>**
- **MCP_DEBUG<3>**
- **MCP_DEBUG<2>**
- **MCP_DEBUG<1>**
- **MCP_DEBUG<0>**
- **CPU_XDP_TDI**
- **CPU_XDP_TMS**
- **JTAG_MCP_TDI**
- **JTAG_MCP_TMS**
- **FSB_CLK_ITP_P**
- **FSB_CLK_ITP_N**
- **XDP_CPURST_L**
- **CPU_XDP_BPM_L<3>**
- **CPU_XDP_BPM_L<5>**
- **CPU_XDP_BPM_L<4>**
- **CPU_XDP_BPM_L<2>**
- **CPU_XDP_BPM_L<1>**
- **CPU_XDP_BPM_L<0>**
- **CPU_PWRGD**
- **CPU_XDP_TDO**
- **JTAG_MCP_TDO**
- **JTAG_MCP_TRST_L**
- **MCP_DEBUG<3>**
- **MCP_DEBUG<2>**
- **MCP_DEBUG<1>**
- **MCP_DEBUG<0>**
- **MCP_DEBUG<5>**
- **MCP_DEBUG<4>**
- **MCP_DEBUG<7>**
- **CPU_XDP_BPM_L<6>**
- **CPU_XDP_BPM_L<7>**
- **CPU_XDP_BPM_L<8>**
- **CPU_XDP_BPM_L<9>**
- **CPU_XDP_BPM_L<10>**
- **CPU_XDP_BPM_L<11>**
- **CPU_XDP_BPM_L<12>**
- **CPU_XDP_BPMB<3>**
- **CPU_XDP_BPM_L<13>**
- **CPU_XDP_BPM_L<14>**
- **CPU_XDP_BPM_L<15>**
- **CPU_XDP_BPM_L<16>**
- **CPU_XDP_BPM_L<17>**
- **CPU_XDP_BPM_L<18>**
- **CPU_XDP_BPM_L<19>**
- **CPU_XDP_BPM_L<20>**
- **CPU_XDP_BPM_L<21>**
- **CPU_XDP_BPM_L<22>**
- **CPU_XDP_BPM_L<23>**
- **CPU_XDP_BPM_L<24>**
- **CPU_XDP_BPM_L<25>**
- **CPU_XDP_BPM_L<26>**
- **CPU_XDP_BPM_L<27>**
- **CPU_XDP_BPM_L<28>**
- **CPU_XDP_BPM_L<29>**
- **CPU_XDP_BPM_L<30>**
- **CPU_XDP_BPM_L<31>**
- **CPU_XDP_BPM_L<32>**
- **CPU_XDP_BPM_L<33>**
- **CPU_XDP_BPM_L<34>**
- **CPU_XDP_BPM_L<35>**
- **CPU_XDP_BPM_L<36>**
- **CPU_XDP_BPM_L<37>**
- **CPU_XDP_BPM_L<38>**
- **CPU_XDP_BPM_L<39>**
- **CPU_XDP_BPM_L<40>**
- **CPU_XDP_BPM_L<41>**
- **CPU_XDP_BPM_L<42>**
- **CPU_XDP_BPM_L<43>**
- **CPU_XDP_BPM_L<44>**
- **CPU_XDP_BPM_L<45>**
- **CPU_XDP_BPM_L<46>**
- **CPU_XDP_BPM_L<47>**
- **CPU_XDP_BPM_L<48>**
- **CPU_XDP_BPM_L<49>**
- **CPU_XDP_BPM_L<50>**
- **CPU_XDP_BPM_L<51>**
- **CPU_XDP_BPM_L<52>**
- **CPU_XDP_BPM_L<53>**
- **CPU_XDP_BPM_L<54>**
- **CPU_XDP_BPM_L<55>**
- **CPU_XDP_BPM_L<56>**
- **CPU_XDP_BPM_L<57>**
- **CPU_XDP_BPM_L<58>**
- **CPU_XDP_BPM_L<59>**
- **CPU_XDP_BPM_L<60>**
- **CPU_XDP_BPM_L<61>**
- **CPU_XDP_BPM_L<62>**
- **CPU_XDP_BPM_L<63>**

**Note:** XDP_DBRESET_L must be pulled-up to 3.3V.
Minimum 1.025V for Gen2 support

OUT

IN

127 mA (A01, AVDD0 & 1)
43 mA (A01, DVDD0 & 1)

R2010 2.49K
402 MF-LF 1/16W

TP_MCP_SATALED_L

TP_SATA_F_R2D_CP
TP_SATA_E_R2D_CP
TP_SATA_D_R2D_CN
TP_SATA_C_R2D_CN
SATA_ODD_R2D_C_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P

MCP_SATA_TERMP

=PP1V05_S0_MCP_SATA_AVDD1
=PP1V05_S0_MCP_SATA_AVDD0
PP1V05_S0_MCP_PLL_SATA

TP_SATA_F_D2RP
TP_SATA_F_D2RN
TP_SATA_E_D2RP
TP_SATA_E_D2RN
TP_SATA_D_D2RP
TP_SATA_D_D2RN
TP_SATA_C_D2RP
TP_SATA_C_D2RN

SATA_ODD_D2R_P
SATA_ODD_D2R_N
SATA_HDD_D2R_N

If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.
If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
HDA Output Caps
For SPI references or DAC outputs

MCP HDA & MISC
Apple Inc.

Sheet 1 of 110

www.laptop-schematics.com
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

Apple: ???

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)

16 mA (A01)

95 mA (A01, 1.8V)

190 mA (A01, 1.8V)

Apple: 1x 2.2uF 0402 (2.2 uF)

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)

16 mA (A01)
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.

**RTL8211 25MHz Clock**

**NOTE: NOT USING THE BUILT-IN 1.05V REGULATOR OF THE PHY**
1394 PHY 1.95V SUPPLY

FireWire Aliases For Connectivity

1394 PHY STRAPPING OPTIONS

Termination
Place close to FireWire PHY

2ND & 3RD TPA/TPB PAIR UNUSED
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V.
CAMERA CONNECTOR & FILTER

K37L (BLUETOOTH) CONNECTOR

IR RECEIVER CONNECTOR

SD Card Reader Board Connector

Internal USB Connections

www.laptop-schematics.com
LPC+SPI Connector

SPI Bus Series Resistance Option

Alternate SPI ROM Support
1.5V S3 NEED TO BE ON BEFORE S0 FET ON FROM COMPARATOR

LOW

NO INTERNAL POWER TO PULL PGOOD NOT COME UP, PPDDR REGULATOR HAS USING COMPARTOR INSTEAD OF REGULATOR

1.21K

1/16W

1%

0.1UF

CERM-X5R

1/16W

5%

10K

MF-LF

1/16W

2

5

0.47UF

R7082

43K

1/16W

10%

1/16W

55

2

3

0.1uF

CERM

603

16V

20%

402

R7040

R7002

1/16W

1%

49.9K

1%

5%

10K

1/16W

1%

2

1

1/16W

1/16W

1/16W

PLACEMENT NOTE = Place close to U1400

ENABLE REGULATOR

DELAY OF ~18MS FROM PM_SLP_S3_L

MAKE_BASE = TRUE

OUT

ENABLE FET

OUT

EN

PGOOD_1V8_S0

PGOOD_MCPCORE_S0

PM_PGOOD_PVCORE_CPU

PM_MXM_PGOOD_PULLUP

PGOOD_1V5S3_COMP_REF1V5S3_PG_CMP

12VS5_9V00_REF

1V05V_S0 DERIVES FROM 3.3V_S5

Battery Off (G3Hot)

10V

20%

PLACE RESISTORS CLOSE TO U7020

USB Port Switch

SI2302

115mOHM

35mOHM
IN ORDER TO SUPPORT UNPOWERING RAIL, HARDWARE MUST GUARANTEE MEM_CKE SIGNALS ARE LOW UNTIL AFTER RAIL TURNS BACK ON OR DIMMS.

NVIDIA RECOMMENDS UNPOWERING DURING SLEEP.

MEM_VTT_EN OUTPUT FROM MCP79 USED TO ENABLE CLAMP ON VTT RAIL, WHICH PULLS ALL CKE SIGNALS BEFORE RAIL IS TURNED OFF, AND REMAINS LOW THROUGH VTT TERMINATION RESISTORS.

MCP79 DDRVTI FET

MAKE_BASE=TRUE
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
MCP Connections

Unused LVDS Interfaces

Unused MXM DP Interfaces

Unused MXM Interfaces

Unused MCP Interfaces

Display: Aliases
Display: BiDiVi Support

Apple Inc.

PAGE

BRANCH

DRAWING NUMBER

SIZE

95 OF 110

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THE INFORMATION CONTAINED HEREIN IS THE
POSSESSEE AGREES TO THE FOLLOWING:

DisplayPort

AUDIO MUX

BiDiVi MUX Enable

Panel/Backlight Control MUX

Hot Plug Detect Support

External AUX Channel and HPD Buffers & filters

SMD Signals for BiDiVi

*Some inputs driven high & outputs driven low under the SMD display
Failure & should prevent any issues in the input

inputs are driven low by default.
**Memory Bus Constraints**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Mem Ctrl</th>
<th>Dqs</th>
<th>Mem Data</th>
<th>Mem Cmd</th>
<th>Mem Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
</tbody>
</table>

**Memory Net Properties**

<table>
<thead>
<tr>
<th>Source Net</th>
<th>Destination Net</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Min Width</th>
<th>Max Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mem Ctrl</td>
<td>Mem Ctrl</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Dqs</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Mem Data</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>14</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Mem Cmd</td>
<td>15</td>
<td>16</td>
<td>17</td>
<td>18</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Mem Clock</td>
<td>19</td>
<td>20</td>
<td>21</td>
<td>22</td>
</tr>
</tbody>
</table>

**Memory Bus Spacing Group Assignments**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Mem Ctrl</th>
<th>Dqs</th>
<th>Mem Data</th>
<th>Mem Cmd</th>
<th>Mem Clock</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
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<td>6</td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
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<th>Min Length</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Mem Ctrl</td>
<td>Mem Ctrl</td>
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<td>4</td>
<td>5</td>
<td>6</td>
</tr>
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<td>9</td>
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<td>13</td>
<td>14</td>
</tr>
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<td>17</td>
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</tr>
<tr>
<td>Mem Ctrl</td>
<td>Mem Clock</td>
<td>19</td>
<td>20</td>
<td>21</td>
<td>22</td>
</tr>
</tbody>
</table>

**MCP MEM COMP Signal Constraints**

- Mem Ctrl should be matched within 10 ps of associated high-pair.
- Mem Ctrl should be matched within 0 ps of associated low-pair.
- Mem Ctrl should be matched within 10 ps of associated high-pair.
- Mem Ctrl should be matched within 0 ps of associated low-pair.
- Mem Ctrl should be matched within 10 ps of associated high-pair.
- Mem Ctrl should be matched within 0 ps of associated low-pair.

**Memory Constraints**

- Mem Ctrl should be matched within 10 ps of associated high-pair.
- Mem Ctrl should be matched within 0 ps of associated low-pair.
- Mem Ctrl should be matched within 10 ps of associated high-pair.
- Mem Ctrl should be matched within 0 ps of associated low-pair.
- Mem Ctrl should be matched within 10 ps of associated high-pair.
- Mem Ctrl should be matched within 0 ps of associated low-pair.

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<table>
<thead>
<tr>
<th>Source Net</th>
<th>Destination Net</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Min Width</th>
<th>Max Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mem Ctrl</td>
<td>Mem Ctrl</td>
<td>3</td>
<td>4</td>
<td>5</td>
<td>6</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Dqs</td>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Mem Data</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>14</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Mem Cmd</td>
<td>15</td>
<td>16</td>
<td>17</td>
<td>18</td>
</tr>
<tr>
<td>Mem Ctrl</td>
<td>Mem Clock</td>
<td>19</td>
<td>20</td>
<td>21</td>
<td>22</td>
</tr>
</tbody>
</table>
**MCP RMII (Ethernet) Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
<th>Value 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SourceA</td>
<td>MCP MII Comp</td>
<td>MCP MII Comp GND</td>
<td>ENET MDC</td>
<td>MCP MII Comp VDD</td>
</tr>
<tr>
<td>SourceB</td>
<td>ENET MII TXD&lt;3..1&gt;</td>
<td>ENET MII TXD&lt;0&gt;</td>
<td>ENET MII RXD&lt;3..1&gt;</td>
<td>ENET MII RXD&lt;0&gt;</td>
</tr>
<tr>
<td>SourceC</td>
<td>ENET MII TX_CLK125M_RXCLK</td>
<td>ENET MII RX_CLK125M_TXCLK</td>
<td>ENET MII MDIO</td>
<td>ENET MII MDI</td>
</tr>
</tbody>
</table>

---

**RTL8211CLGR (Ethernet PHY) Constraints**

<table>
<thead>
<tr>
<th>Source</th>
<th>Value 1</th>
<th>Value 2</th>
<th>Value 3</th>
<th>Value 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>SourceA</td>
<td>MCP MII Comp</td>
<td>MCP MII Comp</td>
<td>ENET MDC</td>
<td>MCP MII Comp VDD</td>
</tr>
<tr>
<td>SourceB</td>
<td>ENET MII TXD&lt;3..1&gt;</td>
<td>ENET MII TXD&lt;0&gt;</td>
<td>ENET MII RXD&lt;3..1&gt;</td>
<td>ENET MII RXD&lt;0&gt;</td>
</tr>
<tr>
<td>SourceC</td>
<td>ENET MII TX_CLK125M_RXCLK</td>
<td>ENET MII RX_CLK125M_TXCLK</td>
<td>ENET MII MDIO</td>
<td>ENET MII MDI</td>
</tr>
</tbody>
</table>

---

**Ethernet Constraints**

- **Source:** MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4
- **Source:** MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4
FireWire Interface Constraints

<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>PHYSICAL</th>
<th>PORT 1 &amp; 2 NOT USED</th>
</tr>
</thead>
<tbody>
<tr>
<td>FW_PORT0_TPA_N</td>
<td>FW_110D FW_TP</td>
<td>FW_110D FW_P0_TPB_L_P</td>
</tr>
<tr>
<td>FW_TPFW_110D</td>
<td>FW_PORT0_TPB_P</td>
<td>FW_TP</td>
</tr>
</tbody>
</table>

FireWire Net Properties

<table>
<thead>
<tr>
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<th>PHYSICAL</th>
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</tr>
</thead>
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<td>FW_110D FW_TP</td>
<td>FW_110D FW_P0_TPB_L_P</td>
</tr>
<tr>
<td>FW_TPFW_110D</td>
<td>FW_PORT0_TPB_P</td>
<td>FW_TP</td>
</tr>
</tbody>
</table>

FireWire Interface Constraints

<table>
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<tbody>
<tr>
<td>FW_PORT0_TPA_N</td>
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<td>FW_110D FW_P0_TPB_L_P</td>
</tr>
<tr>
<td>FW_TPFW_110D</td>
<td>FW_PORT0_TPB_P</td>
<td>FW_TP</td>
</tr>
</tbody>
</table>

### FireWire Net Properties

- FireWire Net Properties
- PORT 1 & 2 NOT USED

### FireWire Interface Constraints

- FireWire Interface Constraints
- PORT 1 & 2 NOT USED

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- 105 of 110
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.
### Physical Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Min. Neck Width</th>
<th>Allow Route</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>0.081 MM</td>
<td></td>
</tr>
<tr>
<td>BOTTOM</td>
<td>0.085 MM</td>
<td></td>
</tr>
</tbody>
</table>

### Spacing Rule Set

<table>
<thead>
<tr>
<th>Rule Set</th>
<th>Net Type</th>
<th>Min. Spacing</th>
<th>Max. Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.15 MM</td>
<td>0.15 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.2 MM</td>
<td>0.2 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.3 MM</td>
<td>0.3 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.4 MM</td>
<td>0.4 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.5 MM</td>
<td>0.5 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.6 MM</td>
<td>0.6 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.8 MM</td>
<td>0.8 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.0 MM</td>
<td>1.0 MM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.5 MM</td>
<td>1.5 MM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Constraints for BGA Area

<table>
<thead>
<tr>
<th>Area Type</th>
<th>Min. Neck Length</th>
<th>Allow Route</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0 MM</td>
<td>1.0 MM</td>
<td></td>
</tr>
<tr>
<td>1.5 MM</td>
<td>1.5 MM</td>
<td></td>
</tr>
<tr>
<td>2.0 MM</td>
<td>2.0 MM</td>
<td></td>
</tr>
<tr>
<td>2.5 MM</td>
<td>2.5 MM</td>
<td></td>
</tr>
</tbody>
</table>

### Rule Definitions

- **0.1 MM**: Minimum width for signal lines.
- **0.15 MM**: Minimum width for power lines.
- **0.2 MM**: Minimum width for differential pairs.
- **0.3 MM**: Minimum width for 70 Ohm differential pairs.
- **0.4 MM**: Minimum width for 100 Ohm differential pairs.
- **0.5 MM**: Minimum width for 3.0 MM differential pairs.
- **0.6 MM**: Minimum width for 1000 Ohm differential pairs.
- **0.8 MM**: Minimum width for 27P4 Ohm differential pairs.
- **1.0 MM**: Minimum width for 0 MM differential pairs.
- **1.5 MM**: Minimum width for 50 Ohm differential pairs.
- **2.0 MM**: Minimum width for 40 Ohm differential pairs.
- **2.5 MM**: Minimum width for 110 Ohm differential pairs.