1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0000821428	PRODUCTION RELEASED	2009-11-20

SCHEM,MBP 15MLB,K19

RAMP

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7892	1	SCHEM,CORNHOLE,K19	SCH	CRITICAL	
820-2523	1	PCBF,CORNHOLE,K19	PCB	CRITICAL	

DRAWING TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Thu May 28 19:04:18 2009

DRAWING TITLE: SCHEM,MBP 15MLB

Apple Inc.

DRAWING NUMBER: 051-7892 | SIZE: D
REVISION: C.0.0
BRANCH:
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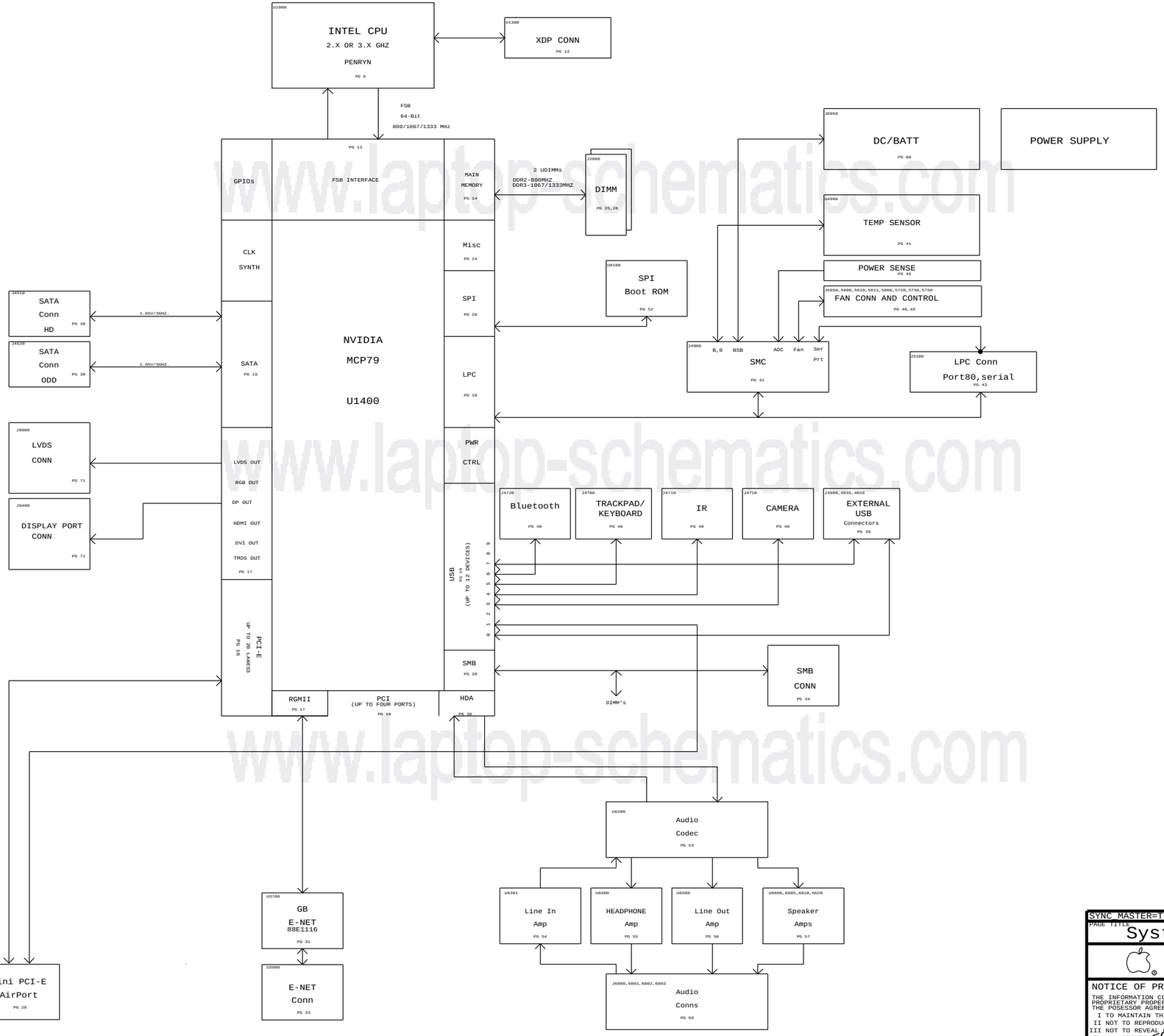
SHEET: 1 OF 97



SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

PAGE TITLE: System Block Diagram

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

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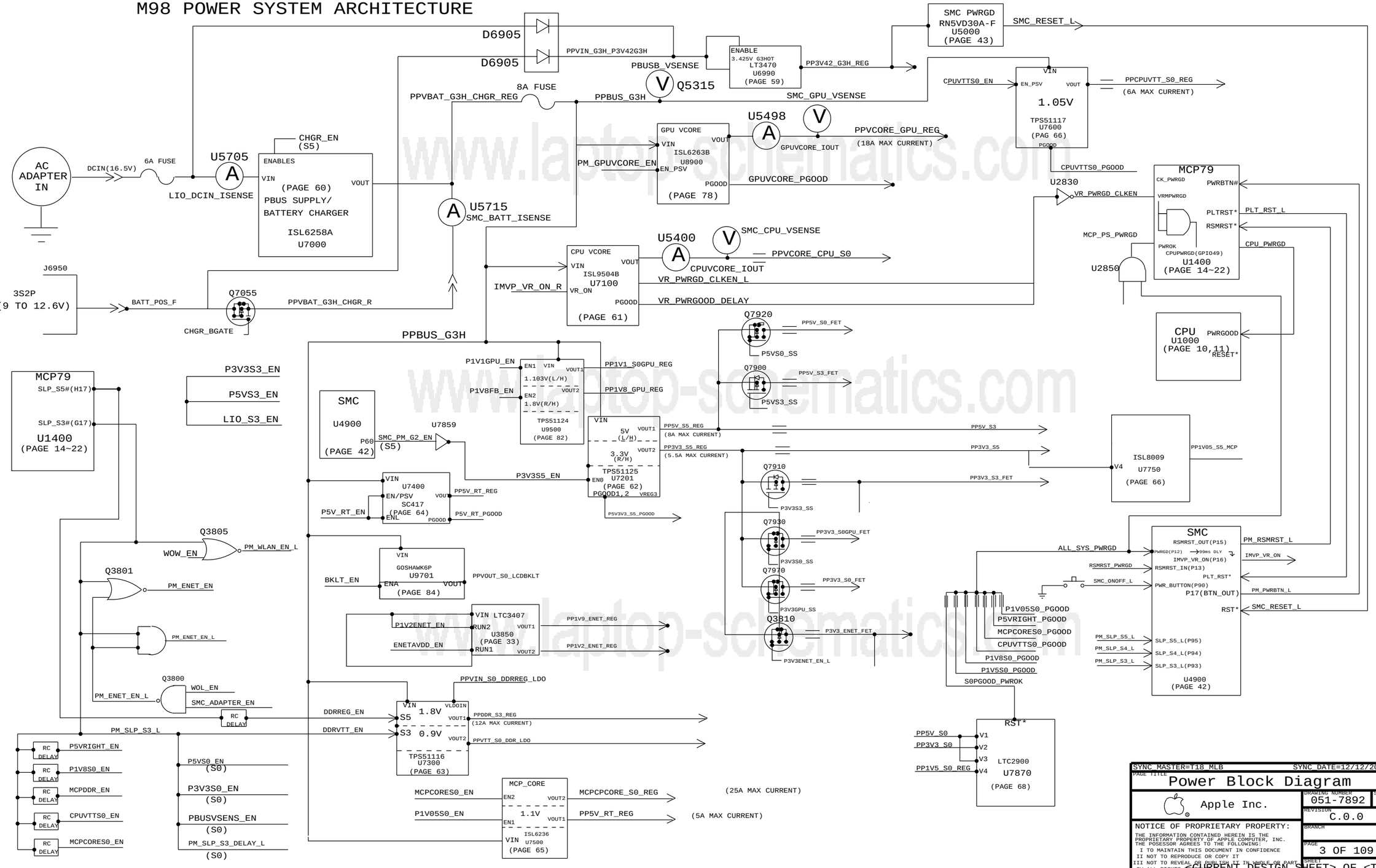
M98 POWER SYSTEM ARCHITECTURE



SYNC MASTER=T18_MLB SYNC DATE=12/12/2007

PAGE TITLE

Power Block Diagram

Apple Inc.

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SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE

Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9965	PCBA,2.66GHZ,256SAM_VRAM,HB_AUDIO,K19	K19_COMMON,K19_PROD,EEE_6XN,CPU_2_66GHZ,FB_256_SAMSUNG
630-9966	PCBA,2.66GHZ,256HYN_VRAM,HB_AUDIO,K19	K19_COMMON,K19_PROD,EEE_6XP,CPU_2_66GHZ,FB_256_HYNIX
630-9967	PCBA,2.80GHZ,512SAM_VRAM,HB_AUDIO,K19	K19_COMMON,K19_PROD,EEE_6XQ,CPU_2_80GHZ,FB_512_SAMSUNG
630-9968	PCBA,2.80GHZ,512HYN_VRAM,HB_AUDIO,K19	K19_COMMON,K19_PROD,EEE_6XR,CPU_2_80GHZ,FB_512_HYNIX
630-9969	PCBA,3.06GHZ,512SAM_VRAM,HB_AUDIO,K19	K19_COMMON,K19_PROD,EEE_6XS,CPU_3_06GHZ,FB_512_SAMSUNG
630-9970	PCBA,3.06GHZ,512HYN_VRAM,HB_AUDIO,K19	K19_COMMON,K19_PROD,EEE_6XT,CPU_3_06GHZ,FB_512_HYNIX
085-0736	K19 MLB DEVELOPMENT	K19_DEVEL_PVT

K19 BOM Groups

BOM GROUP	BOM OPTIONS
K19_COMMON	ALTERNATE,COMMON,K19,K19_COMMON1,K19_COMMON2,K19_PROGPARTS
K19_COMMON1	BOOT_MODE_USER,DPMUX_EN_S0,DP_CA_DET_EG_PLD,DP_ESD,EG_PWRSEQ_HW,EXTRACT_BUFF
K19_COMMON2	GMUX_1V8,GPUVID_1P00V,GPU_SS_INT,ISL6258A,MCP_B03,MCPSEQ_SMC,MIKEY,MUXGFX,SMC_DEBUG_YES,XDP
K19_DEVEL_ENG	BMON_ENG,DEBUG_ADC,GMUX_JTAG,LPCPLUS,VREFMRGN,XDP_CONN
K19_DEVEL_PVT	BMON_PROD,LPCPLUS,NO_VREFMRGN,XDP_CONN
K19_PROD	BMON_PROD,LPCPLUS_NOT,NO_VREFMRGN
K19_PROGPARTS	GMUX_PROG,BOOTROM_PROG,SMC_PROG,TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4,VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4,VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM4,VRAM_512_SAMSUNG
FB_512_HYNIX	VRAM4,VRAM_512_HYNIX

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XN]	CRITICAL	EEE_6XN
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XP]	CRITICAL	EEE_6XP
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XQ]	CRITICAL	EEE_6XQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XR]	CRITICAL	EEE_6XR
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XS]	CRITICAL	EEE_6XS
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:6XT]	CRITICAL	EEE_6XT

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3761	1	IC,PDC,SLGLA,PRQ,2.66G,25W,1066,RD,3M,BGA	U1000	CRITICAL	CPU_2_66GHZ
337S3682	1	IC,PDC,SLGEM,PRQ,2.80G,35W,1066,ED,6M,BGA	U1000	CRITICAL	CPU_2_80GHZ
337S3744	1	IC,PDC,SLGKH,Q5,3.06G,35W,1066,E0,6M,BGA	U1000	CRITICAL	CPU_3_06GHZ
338S0710	1	IC,MCP79MXT-B3,35X35MM,BGA1437	U1400	CRITICAL	MCP_B03
338S0694	1	IC,RTL8251CA-VB-GR,GIGE TRANSCEIVER,48P LQFP	U3700	CRITICAL	
338S0654	1	IC,FW643-E,1394B PHY/DHCI LINK/PCI-E,12	U4100	CRITICAL	
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
338S0563	1	IC,SMC,HS8/2117,9MMX9MM,TLP	U4900	CRITICAL	SMC_BLANK
341S2462	1	IC,SMC,DEVELOPMENT,K19	U4900	CRITICAL	SMC_PROG
341S2503	1	IC,PSOC +W/USB,56PIN,MLF,K19	U5701	CRITICAL	TPAD_PROG
335S0384	1	IC,32MBIT 8-PIN SPI SERIAL FLASH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S2457	1	IC,EFI ROM,LOCKED,K19	U6100	CRITICAL	BOOTROM_PROG
338S0554	1	IC,GPU,55nm,NV G96-GS,BGA969,LF	U8000	CRITICAL	
333S0507	4	IC,SGRAM,GDDR3,16Mx32,1000MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC,SGRAM,GDDR3,16Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_256_HYNIX
333S0511	4	IC,SGRAM,GDDR3,32Mx32,800MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_SAMSUNG
333S0506	4	IC,SGRAM,GDDR3,32Mx32,900MHZ,136 FBGA	U8400,U8450,U8500,U8550	CRITICAL	VRAM_512_HYNIX

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-0736	1	K19 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
13850603	13850602		ALL	Murata alt to Samsung
35351681	35351294		ALL	LM4051,SP4DMP, OEM
15250276	15250683		ALL	Maglayers alt to Dale/Vishay
34152367	34152366		ALL	Macronix alt to SST
15251034	15250867		ALL	Yuko alt to Delta
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
15250915	15250796		ALL	Maglayers alt to Cyntec 3mm
12850220	12850262		ALL	KEMET ALT TO SANYO
127S0062	127S0108		ALL	ROHM ALT TO KEMET
15250968	15250966		ALL	Maglayer alt to Delta
311S0447	311S0406		ALL	NXP alt to TI
33850714	33850554		ALL	Low Leakage G96 GPU
107S0138	107S0074		ALL	CYNTEC alt to YDS
107S0139	107S0075		ALL	CYNTEC alt to YDS
516-0213	516-0201		ALL	Molex alt to Foxconn
516S0790	516S0706		ALL	Molex alt to Foxconn

SYNC MASTER=DDR SYNC DATE=12/18/2008

PAGE TITLE

BOM Configuration

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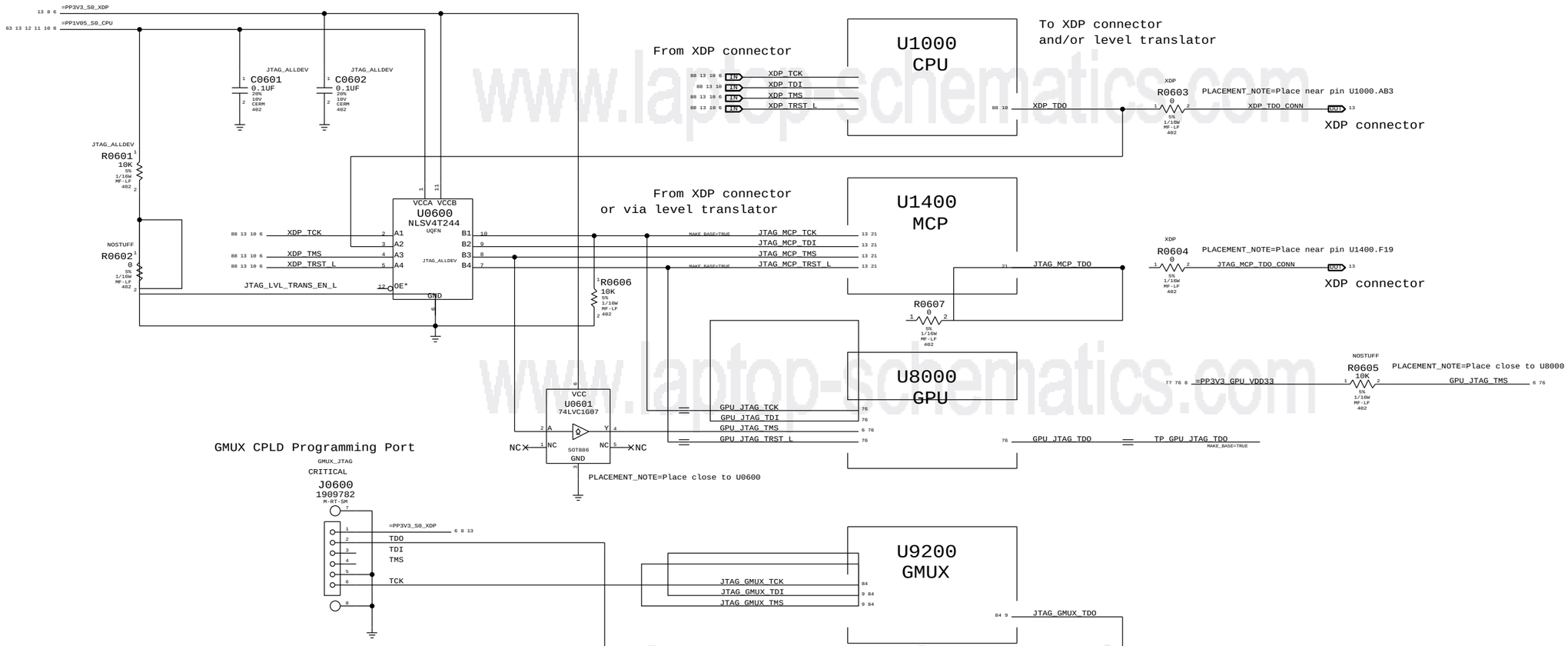
1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



SYNC_MASTER=DDR	SYNC_DATE=07/22/2008
PAGE TITLE	JTAG Scan Chain
Apple Inc.	DRAWING NUMBER 051-7892 · SIZE D
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	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Functional Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_RT	8 49	3 TPs
TRUE	FAN_LT_PWM	49	
TRUE	FAN_LT_TACH	49	
TRUE	FAN_RT_PWM	49	
TRUE	FAN_RT_TACH	49	
TRUE	GND		5 TPs

LVDS Connector

FUNC_TEST

TRUE	=PP3V3_S0_DDC_LCD	8 77 80	
TRUE	PP3V3_SW_LCD	80	
TRUE	PPVOUT_S0_LCDBKLT	7 53 80 85	
TRUE	LVDS_DDC_CLK	80 81	
TRUE	LVDS_DDC_DATA	80 81	
TRUE	LVDS_CONN_A_DATA_N<0>	80 81 95	
TRUE	LVDS_CONN_A_DATA_P<0>	80 81 95	
TRUE	LVDS_CONN_A_DATA_N<1>	80 81 95	
TRUE	LVDS_CONN_A_DATA_P<1>	80 81 95	
TRUE	LVDS_CONN_A_DATA_N<2>	80 81 95	
TRUE	LVDS_CONN_A_DATA_P<2>	80 81 95	
TRUE	LVDS_CONN_A_CLK_F_N	80 95	
TRUE	LVDS_CONN_A_CLK_F_P	80 95	
TRUE	LVDS_CONN_B_DATA_N<0>	80 81 95	
TRUE	LVDS_CONN_B_DATA_P<0>	80 81 95	
TRUE	LVDS_CONN_B_DATA_N<1>	80 81 95	
TRUE	LVDS_CONN_B_DATA_P<1>	80 81 95	
TRUE	LVDS_CONN_B_DATA_N<2>	80 81 95	
TRUE	LVDS_CONN_B_DATA_P<2>	80 81 95	
TRUE	LVDS_CONN_B_CLK_F_N	80 95	
TRUE	LVDS_CONN_B_CLK_F_P	80 95	
TRUE	LED_RETURN_1	80 85	
TRUE	LED_RETURN_2	80 85	
TRUE	LED_RETURN_3	80 85	
TRUE	LED_RETURN_4	80 85	
TRUE	LED_RETURN_5	80 85	
TRUE	LED_RETURN_6	80 85	
TRUE	BKL_ISEN1	85	
TRUE	BKL_ISEN2	85	
TRUE	BKL_ISEN3	85	
TRUE	BKL_ISEN4	85	
TRUE	BKL_ISEN5	85	
TRUE	BKL_ISEN6	85	
TRUE	GND		5 TPs

IPD Flex Connector

FUNC_TEST

TRUE	PP3V3_S3_LDO	7 51	
TRUE	PP18V5_S3	7 51	
TRUE	Z2_CS_L	50 51	
TRUE	Z2_DEBUG3	50 51	
TRUE	Z2_MOSI	50 51	
TRUE	Z2_MISO	50 51	
TRUE	Z2_SCLK	50 51	
TRUE	Z2_BOOST_EN	51	
TRUE	Z2_HOST_INTN	50 51	
TRUE	Z2_CLKIN	50 51	
TRUE	Z2_KEY_ACT_L	50 51	
TRUE	Z2_RESET	50 51	
TRUE	PSOC_MISO	50 51	
TRUE	PSOC_MOSI	50 51	
TRUE	PSOC_SCLK	50 51	
TRUE	SMBUS_SMC_A_S3_SDA	45 94	
TRUE	SMBUS_SMC_A_S3_SCL	45 94	
TRUE	PSOC_F_CS_L	50 51	
TRUE	PICKB_L	50 51	
TRUE	GND		2 TPs

SD Card Connector

FUNC_TEST

TRUE	SD_D<7..0>	32 93	
TRUE	SD_CMD	32 93	
TRUE	SD_CLK	32 93	
TRUE	SD_CD_L	32	
TRUE	SD_WP	32	
TRUE	GND		2 TPs

Speaker Connectors

FUNC_TEST

TRUE	BI_MIC_LO	59 60	
TRUE	BI_MIC_SHIELD	59 60	
TRUE	BI_MIC_HI	59 60	
TRUE	SPKRCONN_L_OUT_P	58 59 96	
TRUE	SPKRCONN_L_OUT_N	58 59 96	
TRUE	SPKRCONN_R_OUT_P	58 59 96	
TRUE	SPKRCONN_R_OUT_N	58 59 96	
TRUE	SPKRCONN_S_OUT_P	58 59 96	
TRUE	SPKRCONN_S_OUT_N	58 59 96	
TRUE	GND		6 TPs

SATA ODD Connectors

FUNC_TEST

TRUE	PP5V_SW_ODD	7 39 53	4 TPs
TRUE	SMC_ODD_DETECT	39 42	
TRUE	SATA_ODD_R2D_P	39 90	
TRUE	SATA_ODD_R2D_N	39 90	
TRUE	SATA_ODD_D2R_C_N	39 90	
TRUE	SATA_ODD_D2R_C_P	39 90	
TRUE	GND		3 TPs

Keyboard Connector

FUNC_TEST

TRUE	PP3V3_S3	7 8	
TRUE	PP3V42_G3H	7 8	
TRUE	WS_KBD1	50	
TRUE	WS_KBD2	50	
TRUE	WS_KBD3	50	
TRUE	WS_KBD4	50	
TRUE	WS_KBD5	50	
TRUE	WS_KBD6	50	
TRUE	WS_KBD7	50	
TRUE	WS_KBD8	50	
TRUE	WS_KBD9	50	
TRUE	WS_KBD10	50	
TRUE	WS_KBD11	50	
TRUE	WS_KBD12	50	
TRUE	WS_KBD13	50	
TRUE	WS_KBD14	50	
TRUE	WS_KBD15_CAP	50	
TRUE	WS_KBD16_NUM	50	
TRUE	WS_KBD17	50	
TRUE	WS_KBD18	50	
TRUE	WS_KBD19	50	
TRUE	WS_KBD20	50	
TRUE	WS_KBD21	50	
TRUE	WS_KBD22	50	
TRUE	WS_KBD23	50	
TRUE	WS_KBD_ONOFF_L	50	
TRUE	WS_LEFT_SHIFT_KBD	50	
TRUE	WS_LEFT_OPTION_KBD	50	
TRUE	WS_CONTROL_KBD	50	
TRUE	KBDLED_ANODE	7 51	
TRUE	GND		2 TPs

Airport/BT/Camera Conn.

FUNC_TEST

TRUE	PCIE_MINI_D2R_P	17 31 90	
TRUE	PCIE_MINI_D2R_N	17 31 90	
TRUE	PCIE_MINI_R2D_P	31 90 96	
TRUE	PCIE_MINI_R2D_N	31 90 96	
TRUE	PCIE_CLK100M_MINI_CONN_P	31 96	
TRUE	PCIE_CLK100M_MINI_CONN_N	31 96	
TRUE	MINI_CLKREQ_Q_L	31	
TRUE	PCIE_WAKE_L	17 31	
TRUE	MINI_RESET_CONN_L	31	
TRUE	PP5V_WLAN	31	
TRUE	PP3V3_S3_BT_F	31	
TRUE	PP5V_S3_BTCAMERA_F	31	
TRUE	I2C_ALS_SDA	31 45	
TRUE	I2C_ALS_SCL	31 45	
TRUE	USB_CAMERA_CONN_P	31 96	
TRUE	USB_CAMERA_CONN_N	31 96	
TRUE	CONN_USB2_BT_P	31 96	
TRUE	CONN_USB2_BT_N	31 96	
TRUE	GND		10 TPs

SATA HDD Connector

FUNC_TEST

TRUE	PP5V_S0_HDD_FLT	7 39	4 TPs
TRUE	PP5V_S3_IR_R	39	
TRUE	SATA_HDD_R2D_P	39 90	
TRUE	SATA_HDD_R2D_N	39 90	
TRUE	SATA_HDD_D2R_C_P	39 90	
TRUE	SATA_HDD_D2R_C_N	39 90	
TRUE	IR_RX_OUT	39 41	
TRUE	SYS_LED_ANODE_R	39	
TRUE	GND		6 TPs

KBD Backlight Conn.

FUNC_TEST

TRUE	KBDLED_ANODE	7 51	2 TPs
TRUE	SMC_KDBLED_PRESENT_L	51	
TRUE	GND		

DC Power Connector

FUNC_TEST

TRUE	PP18V5_DCIN_FUSE	61	3 TPs
TRUE	ADAPTER_SENSE	61	
TRUE	GND		3 TPs

Battery Connector

FUNC_TEST

TRUE	PPVBAT_G3H_CONN	61 62	3 TPs
TRUE	=SMBUS_BATT_SCL	7 45 61	
TRUE	=SMBUS_BATT_SDA	7 45 61	
TRUE	SYS_DETECT_L	61	
TRUE	GND_BATT_CHGND	9 61	6 TPs

Batt Signal Connector

FUNC_TEST

TRUE	PP3V42_G3H	7 8	3 TPs
TRUE	=SMBUS_BATT_SCL	7 45 61	
TRUE	=SMBUS_BATT_SDA	7 45 61	
TRUE	SMC_BIL_BUTTON_L	42 43 61	
TRUE	SMC_LID_R	61	
TRUE	GND		3 TPs

Power Nets

FUNC_TEST

TRUE	PPVCORE_S0_CPU	8	
TRUE	PPVCORE_S0_MCP_REG	8	
TRUE	PP0V9R0V75_S0_DDRVTT	8	
TRUE	PPCPUVTT_S0	8	
TRUE	PP1V8R1V5_S0_FET	8	
TRUE	PP1V8_S0	8	
TRUE	PP3V3_S0	8 96	
TRUE	PP1V8R1V5_S3	8	
TRUE	PP3V3_S3	7 8	
TRUE	PP1V2R1V05_S5	8	
TRUE	PP3V3_S5	8 96	
TRUE	PP3V42_G3H	7 8	
TRUE	PPBUS_G3H	8 46	
TRUE	PP3V3_ENET_PHY	8	
TRUE	PP1V2R1V05_ENET	8	
TRUE	PP5V_S3	8	
TRUE	PP3V3_S5_AVREF_SMC	42 43	
TRUE	PP18V5_S3	7 51	
TRUE	PP3V3_S3_LDO	7 51	
TRUE	PPVOUT_S0_LCDBKLT	7 53 80 85	
TRUE	PP4V5_AUDIO_ANALOG	55	
TRUE	SMC_PM_G2_EN	42 64 69	
TRUE	PM_SLP_S4_L	21 40 42 43 69	
TRUE	PM_SLP_S3_L	21 34 37 42 69 82 84	
TRUE	PP1V05_S0_MCP_PLL_UF	8	
TRUE	PP5V_SW_ODD	7 39 53	
TRUE	PP5V_S0_HDD_FLT	7 39	
TRUE	BKL_VLDO	85	
TRUE	GND		6 TPs

ICT Test Points

				NO_TEST
55	TP_AUD_LO1_N_L	NC_AUD_LO1_N_L		
55	TP_AUD_LO1_P_L	NC_AUD_LO1_P_L	MAKE_BASE=TRUE	TRUE
26	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE	TRUE
26	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE	TRUE
18	TP_ENET_INTR_L	NC_ENET_INTR_L	MAKE_BASE=TRUE	TRUE
18	TP_ENET_PWRDWN_L	NC_ENET_PWRDWN_L	MAKE_BASE=TRUE	TRUE
			MAKE_BASE=TRUE	TRUE
19	TP_LPC_DRQ0_L	NC_LPC_DRQ0_L		
			MAKE_BASE=TRUE	TRUE
16	TP_MEM_A_CKE<3..2>	NC_MEM_A_CKE<3..2>		
15	TP_MEM_A_CLK2N	NC_MEM_A_CLK2N	MAKE_BASE=TRUE	TRUE
16	TP_MEM_A_CLK3N	NC_MEM_A_CLK3N	MAKE_BASE=TRUE	TRUE
16	TP_MEM_A_CLK3P	NC_MEM_A_CLK3P	MAKE_BASE=TRUE	TRUE
16	TP_MEM_A_CLK4P	NC_MEM_A_CLK4P	MAKE_BASE=TRUE	TRUE
16	TP_MEM_A_CS_L<3>	NC_MEM_A_CS_L<3>	MAKE_BASE=TRUE	TRUE
16	TP_MEM_A_ODT<3..2>	NC_MEM_A_ODT<3..2>	MAKE_BASE=TRUE	TRUE
			MAKE_BASE=TRUE	TRUE
16	TP_MEM_B_CKE<2>	NC_MEM_B_CKE<2>		
16	TP_MEM_B_CLK3P	NC_MEM_B_CLK3P	MAKE_BASE=TRUE	TRUE
16	TP_MEM_B_CLK4N	NC_MEM_B_CLK4N	MAKE_BASE=TRUE	TRUE
16	TP_MEM_B_CLK4P	NC_MEM_B_CLK4P	MAKE_BASE=TRUE	TRUE
16	TP_MEM_B_CLK5N	NC_MEM_B_CLK5N	MAKE_BASE=TRUE	TRUE
16	TP_MEM_B_ODT<2>	NC_MEM_B_ODT<2>	MAKE_BASE=TRUE	TRUE
21	TP_MLB_RAM_SIZE	NC_MLB_RAM_SIZE	MAKE_BASE=TRUE	TRUE
50	TP_P7_7	NC_P7_7	MAKE_BASE=TRUE	TRUE
19	TP_PCI_AD<31..8>	NC_PCI_AD<31..8>	MAKE_BASE=TRUE	TRUE
			MAKE_BASE=TRUE	TRUE
19	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>		
			MAKE_BASE=TRUE	TRUE
19	TP_PCI_CLK0	NC_PCI_CLK0		
19	TP_PCI_CLK1	NC_PCI_CLK1	MAKE_BASE=TRUE	TRUE
19	TP_PCI_DEVSEL_L	NC_PCI_DEVSEL_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_FRAME_L	NC_PCI_FRAME_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_GNT0_L	NC_PCI_GNT0_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_GNT1_L	NC_PCI_GNT1_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_INTW_L	NC_PCI_INTW_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_INTX_L	NC_PCI_INTX_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_INTZ_L	NC_PCI_INTZ_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_IRDY_L	NC_PCI_IRDY_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_PERR_L	NC_PCI_PERR_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_RESET1_L	NC_PCI_RESET1_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_SERR_L	NC_PCI_SERR_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_STOP_L	NC_PCI_STOP_L	MAKE_BASE=TRUE	TRUE
19	TP_PCI_TRDY_L	NC_PCI_TRDY_L	MAKE_BASE=TRUE	TRUE
17	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	TRUE
17	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	TRUE
17	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	TRUE
17	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	TRUE
17	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	TRUE
17	TP_PCIE_PE4_D2RN	NC_PCIE_PE4_D2RN	MAKE_BASE=TRUE	TRUE
17	TP_PCIE_PE4_R2D_CN	NC_PCIE_PE4_R2D_CN	MAKE_BASE=TRUE	TRUE
17	TP_PE4_PRSNT_L	NC_PE4_PRSNT_L	MAKE_BASE=TRUE	TRUE
50	TP_PSOC_P1_3	NC_PSOC_P1_3	MAKE_BASE=TRUE	TRUE
50	TP_PSOC_SDA	NC_PSOC_SDA	MAKE_BASE=TRUE	TRUE
20	TP_SATA_C_D2RP	NC_SATA_C_D2RP	MAKE_BASE=TRUE	TRUE
20	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CN	MAKE_BASE=TRUE	TRUE
20	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CP	MAKE_BASE=TRUE	TRUE
20	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE	TRUE
20	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE	TRUE
21	TP_SB_A20GATE	NC_SB_A20GATE	MAKE_BASE=TRUE	TRUE
			MAKE_BASE=TRUE	TRUE

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 88
TRUE	FSB_ADS_L	10 14 88
TRUE	FSB_ADSTB_L<1..0>	10 14 88
TRUE	FSB_D_L<63..0>	10 14 88
TRUE	FSB_DINV_L<3..0>	10 14 88
TRUE	FSB_DSTB_L_N<3..0>	10 14 88
TRUE	FSB_DSTB_L_P<3..0>	10 14 88
TRUE	FSB_HIT_L	10 14 88
TRUE	FSB_HITM_L	10 14 88
TRUE	FSB_LOCK_L	10 14 88
TRUE	USB_BT_N	20 31 91
TRUE	USB_BT_P	20 31 91
TRUE	USB_CAMERA_N	20 31 91
TRUE	USB_CAMERA_P	
TRUE	SATA_ODD_D2R_UF_N	39 96
TRUE	SATA_ODD_D2R_UF_P	39 96
TRUE	DP_ML_C_P<3..0>	82 95

Note.
NO_TEST properties are also on page9,26,43,50

SYNC_MASTER=N/A SYNC_DATE=N/A

PAGE TITLE: Functional / ICT Test

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 7 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

"G3Hot" (Always-Present) Rails

62 =PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12V
MAKE_BASE=TRUE
7 46
=PPVIN_S5_P5VP3V3 64
=PPVIN_S0_CPUVTTS0 67
=PPBUS_S0_LCDBKLT 86
=PPBUS_S5_FWPWRSW 37
=PPVIN_GPU_GPUVCORE 79
=PPVIN_S5_CPU_IMVP_ISNS_R 46
=PPVIN_S0_MCPCORE 66
=PPVIN_S3_DDRREG 65
=PPVIN_S0GPU_P1V8P1V1 83
=PPVBAT_G3H_P3V42G3H 61
=PPVIN_S0_5VRT

46 =PPVIN_S5_CPU_IMVP_ISNS
PPBUS_CPU_IMVP_ISNS
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12V
MAKE_BASE=TRUE
=PPVIN_S5_CPU_IMVP 63

61 =PP18V5_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18V
MAKE_BASE=TRUE
=PPDCIN_S5_CHGR 62

61 =PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.42V
MAKE_BASE=TRUE
7
=PP3V42_G3H_SMCUSBMUX 40
=PP3V42_G3H_SMBUS_SMC_BSA 45
=PP3V3_S5_SMC 42 43
=PP3V3_S5_LPCPLUS 44
=PPVIN_S5_SMCVREF 43
=PP3V42_G3H_PWRCTL 64 69
=PP3V42_G3H_CHGR 62
=PP3V3_S5_RTC_D 26
=PP3V42_G3H_BATT 61
=PP3V42_G3H_TPAD 50
=PP3V42_G3H_BMON_ISNS 46
=PP3V42_G3H_CPUCOREFISNS 46
=PP3V42_G3H_ONEWIREPROT 61

5V Rails

64 =PP5V_S3_REG
PP5V_S3
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.17MM
VOLTAGE=5.0V
MAKE_BASE=TRUE
7
=PP5V_S3_SYSLED 43
=PP5V_S3_BTCAMERA 31
=PP5V_S3_WLAN 31
=PP5V_S3_IR 39 41
=PP5V_S3_P1V8GPU 70
=PP5V_S3_DDRREG 65
=PP5V_S3_GPUVCORE 79
=PP5V_S3_RTUSB 40
=PP5V_S3_TPAD 51
=PP5V_S3_MCPDDRFET 70
=PP5V_S3_VTTCLAMP 70
=PP5V_S3_AUDIO 9 55
=PP5V_S3_DEBUG_ADC_AVDD 53
=PP5V_S3_DEBUG_ADC_DVDD 53
=PP5V_S3_DEBUG_ISNS 53
=PP5V_S3_P5VS0FET 70

70 =PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
=PP5V_S0_FAN_LT 49
=PP5V_S0_FAN_RT 7 49
=PP5V_S0_CPU_IMVP 63
=PP5V_S0_CPUVTTS0 67
=PP5V_S0_KBDLED 51
=PP5V_S0GPU_P1V1P1V8_GPU 83
=PP5V_S0_LPCPLUS 44
=PP5V_S0_ODD 39
=PP5V_S0_HDD 39
=PP5V_S0_MCPREG 66
=PP5V_S0_BKL 85

Chipset "VCore" Rails

63 =PPVCORE_S0_CPU_REG
PPVCORE_S0_CPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.25V
MAKE_BASE=TRUE
7
=PPVCORE_S0_CPU 11 12 46

66 =PPMCPCORE_S0_REG
PPVCORE_S0_MCP_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
=PPVCORE_S0_MCP 22 24 46

3.3V-2.5V Rails

64 =PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
7 96
=PP3V3_S5_ROM 44 54
=PP3V3_S5_MEMRESET 30
=PP3V3_S3_P3V3S3FET 70
=PP3V3_S5_P1V2P1V8 87
=PP3V3_S0_P3V3S0FET 70
=PP3V3_GPU_P3V3GPUFET 70
=PP3V3_S5_PWRCTL 69
=PP3V3_S5_P1V05S5 68
=PP3V3_S5_MCP 22 24
=PP3V3_S5_MCP_GPIO 18 20
=PP3V3_FW_LATEVG_ACTIVE 37
=PP3V3_S5_P1V05FWFET 37
=PP3V3_S5_MCPPWRGD 26
=PP3V3_FW_LATEVG 38
=PP3V3_S5_P1V05ENETFET 34
=PP3V3_S5_P3V3ENETFET 34
=PP3V3_S5_DP_PORT_PWR 82

70 =PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.48MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
7
=PP3V3_S3_BT 31
=PP3V3_S3_SMBUS_SMC_A_S3 45
=PP3V3_S3_SMS 52
=PP3V3_S3_TPAD 50
=PP3V3_S3_CARDREADER 32
=PP3V3_S3_WLAN 31
=PP3V3_S3_MCP_GPIO 21
=PP3V3_S3_VREFMRGN 27
=PP3V3_S3_SMBUS_SMC_MGMT 45

70 =PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
7 96
=PP3V3_S0_SMC 43
=PP3V3_S0_SMBUS_SMC_B_S0 45
=PP3V3_S0_MCPDDRISNS 47
=PP3V3_S0_GPU1V8ISNS 47
=PP3V3_S0_CPUTHMSNS 48
=PP3V3_S0_GPUTHMSNS 48
=PP3V3_S0_FAN_LT 49
=PP3V3_S0_FAN_RT 49
=PP3V3_S0_IMVP 63
=PP3V3_S0_PWRCTL 69
=PP3V3_S0_DDC_LCD 7 77 80
=PP3V3_S0_XDP 6 13
=PP3V3_S0_REMTHMSNS 48
=PPSPD_S0_MEM_A 28
=PPSPD_S0_MEM_B 29
=PP3V3_S0_LCD 80
=PP3V3_S0_SMBUS_MCP_0 45
=PP3V3_S0_GMUX 84
=PP3V3_S0_DPMUX 81
=PP3V3_S0_DPCONN 82
=PP3V3_S0_MCP_GPIO 18 19 21
=PP3V3R1V5_S0_MCP_HDA 21 24
=PP3V3_S0_MCP_PLL_UF 24
=PP3V3_S0_MCP_VPLL_UF 25
=PP3V3_S0_MCP 21 22 24
=PP3V3_S0_AUDIO 55 59 60
=PP3V3_S0_ODD 39
=PP3V3_S0_VMON 69
=PP3V3_S0_SMBUS_MCP_1 45
=PP3V3_S0_P3V3FWFET 37
=PP3V3_S0_MCP_PLL_VLDO 68
=PP3V3_S0_LVDSDDCMUX 81
=PP3V3_S0_BATTCHARGERTMPSNSR
=PP3V3_GPU_SMBUS_SMC_0_S0 45
=PP3V3_S0_TPAD 51
=PP3V3_S0_BKL_VDDIO 85
=PP3V3_S0_FWPWRCTL 37

87 =PP1V2_S0_REG
PP1V2_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
=PP1V2_S0_GMUX 84

1.8V/DDR 1.5V Rails

87 70 =PP1V8_S0_REG
PP1V8_S0
MIN_LINE_WIDTH=0.10MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
7
500 mA max supply
190 mA =PP3V3R1V8_S0_MCP_IFP_VDD 18 25
=PP1V8_S0_AUDIO 55
=PP1V8_S0_VMON 69
=PP2V5_S0_GMUX 84

65 =PPDDR_S3_REG
PP1V8R1V5_S3
MIN_LINE_WIDTH=0.8 mm
MIN_NECK_WIDTH=0.1 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
7
=PP1V8R1V5_S0_MCP_FET 70
=PPVIN_S0_DDRREG_LDO 65
=PP1V5_S3_MEM_A 28
=PP1V5_S3_MEM_B 29
=PP1V5_S3_MEMRESET 30

70 =PP1V8R1V5_S0_FET
PP1V8R1V5_S0_FET
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.17mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
7
130 mA =PP1V5_S0_CPU 11 12
500 mA
=PP1V5_S0_VMON 69
4771 mA =PP1V8R1V5_S0_MCP_MEM 16 24
=PP1V5_S0_MEM_A 28
=PP1V5_S0_MEM_B 29
=PP1V5_S0_HDD 39
=PP1V5_S0_MCP_PLL_VLDO 68

24 8 =PP1V05_S0_MCP_PEX_DVDD
=PP1V05_S0_MCP_PEX_DVDD0
=PP1V05_S0_MCP_PEX_DVDD1 17
24 PP1V05_S0_MCP_PEX_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_PEX_AVDD0 17
=PP1V05_S0_MCP_PEX_AVDD1 17
24 8 =PP1V05_S0_MCP_SATA_DVDD
=PP1V05_S0_MCP_SATA_DVDD0 20
24 PP1V05_S0_MCP_SATA_AVDD
MAKE_BASE=TRUE
=PP1V05_S0_MCP_SATA_AVDD0 20

67 =PPCPUVTT_S0_REG
PPCPUVTT_S0
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
4500 mA =PP1V05_S0_CPU 6 10 11 12 13 63
1182 mA =PP1V05_S0_MCP_FSB 9 14 22 24
6600 MA
=PP1V05_S0_MCP_AVDD_UF 24
=PP1V05_S0_MCP_PEX_DVDD 8 24
1034 mA =PP1V05_S0_MCP_SATA_DVDD 8 24
241 mA max load
=PP1V05_S0_MCP_HDMI_VDD 18 25

68 =PP1V05_S5_MCP
PP1V2R1V05_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
105 mA/241 mA =PP1V05_S5_MCP_VDD_AUXC 22 24
139 mA/ 0 mA =PP1V05_ENET_P1V05ENETFET 34

65 27 =PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE

65 =PPVTT_S0_DDR_LDO
PP0V9R0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
7
=PP0V75_S0_MEM_VTT_A 28
=PP0V75_S0_MEM_VTT_B 29
=PPVTT_S0_VTTCLAMP 70
OR 0.75V

ENET Rails

34 =PP1V05_ENET_FET
PP1V2R1V05_ENET
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
7
=PP1V05_ENET_MCP_PLL_MAC 24
=PP1V05_ENET_MCP_RMGT 18 24
=PP1V05_ENET_PHY 33
=PP1V05_FW_P1V05FWFET 37
=PP1V05_FWPWRCTL 37

34 =PP3V3_ENET_FET
PP3V3_ENET_PHY
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
7
=PP3V3_ENET_MCP_RMGT 18 24
=PP3V3_ENET_PHY 33

"FW" (FireWire) Rails

37 =PPBUS_S5_FW_FET
PPVP_FW
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
=PPVP_FW_PORT1 38
=PPVP_FW_PHY_CPS_FET 38

37 36 =PP1V0_FW_FWPHY
PP1V0_FW
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PP1V0_FW_FET 37

38 37 36 =PP3V3_FW_FWPHY
PP3V3_FW_FWPHY
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_FW_FET 37
=PP3V3_S0_P1V05FWFET 37

68 24 =PP1V05_S0_MCP_PLL_UF
PP1V05_S0_MCP_PLL_UF
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
7

"GPU" Rails

70 =PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.38MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_VDD33 6 76 77
=PP3V3_GPU_MIO 76 77
=PP3V3_GPU_LVDS_DDC 81
=PP3V3_GPU_PWRCTL 69
=PP3V3_GPU_VCORELOGIC 79

83 =PP1V1_S0GPU_REG
PP1V1_S0GPU_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
MAKE_BASE=TRUE
=PP1V1_GPU_PEX_IOVDDQ 71
=PP1V1_GPU_PEX_IOVDD 71
=PP1V1_GPU_PEX_PLLXVDD 71
=PP1V1_GPU_PLLVDD 76
=PP1V1_GPU_H_PLLVDD 76
=PP1V1_GPU_VID_PLLVDD 76
=PP1V1_GPU_FBPLLAVDD 73
=PP1V1_GPU_IFPCD_IOVDD 78

70 =PP1V8_GPUIFPX_REG
PP1V8_GPUIFPX
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.15 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_IFPX 78

47 =PP1V8_S0GPU_ISNS
PP1V8_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_GPU_FB_VDD 74 75
=PP1V8_GPU_FB_VDDQ 9 74 75
=PP1V8_GPU_FBVDDQ 72
=PP1V8_GPU_FBIO 73

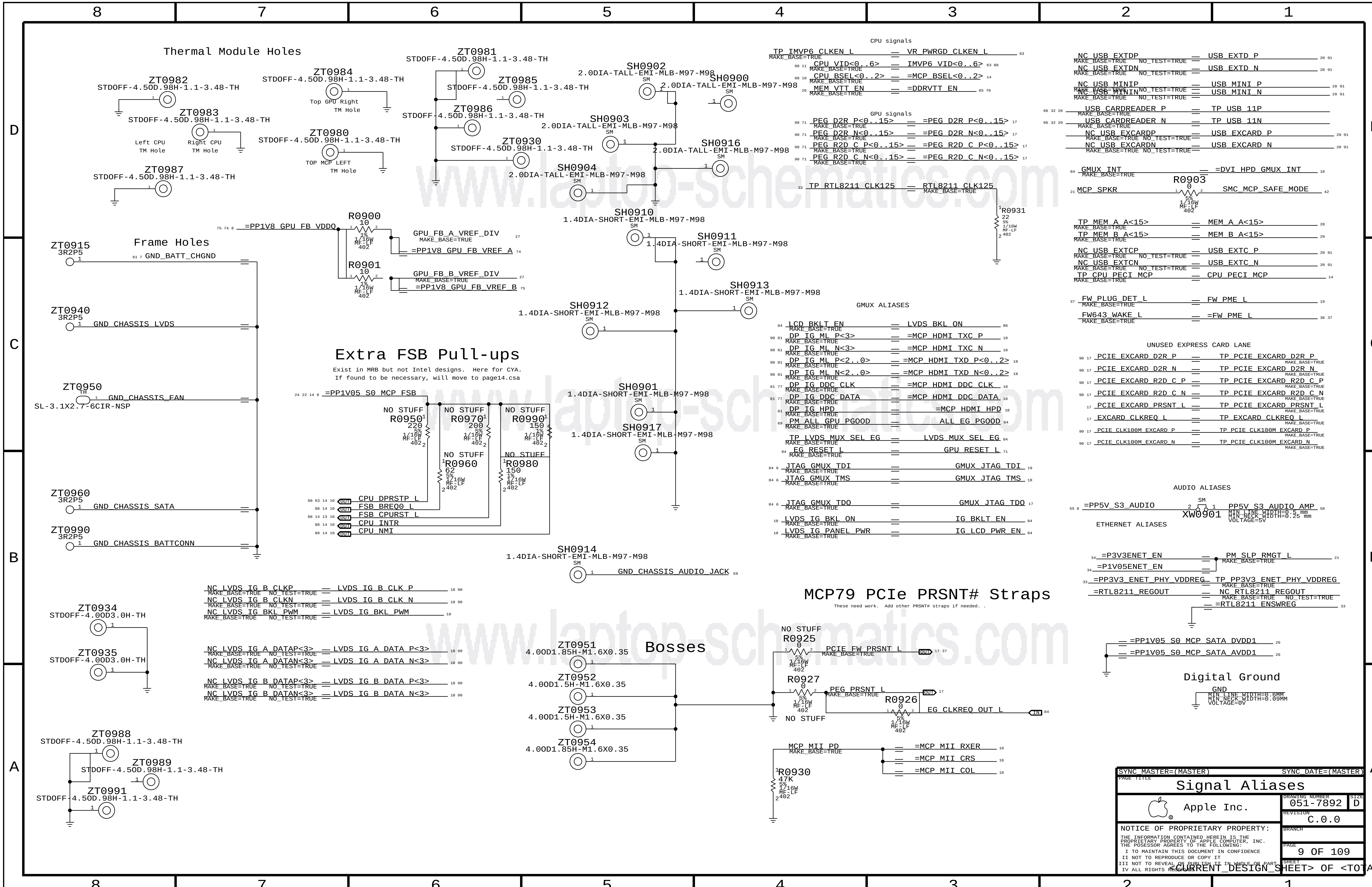
79 46 =PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
=PPVCORE_GPU 72

83 =PP1V8_GPU_REG
PP1V8_S0GPU_ISNS_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
=PP1V8_S0GPU_ISNS_R 47

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
PAGE TITLE
Power Aliases

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 8 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Thermal Module Holes
ZT0982 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0983 STDOFF-4.50D.98H-1.1-3.48-TH
Left CPU TM Hole
Right CPU TM Hole
ZT0987 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0984 STDOFF-4.50D.98H-1.1-3.48-TH
Top GPU Right TM Hole
ZT0980 STDOFF-4.50D.98H-1.1-3.48-TH
TOP MCP LEFT TM Hole
ZT0981 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0985 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0986 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0930 STDOFF-4.50D.98H-1.1-3.48-TH
SH0902 2.0DIA-TALL-EMI-MLB-M97-M98
SH0900 2.0DIA-TALL-EMI-MLB-M97-M98
SH0903 2.0DIA-TALL-EMI-MLB-M97-M98
SH0916 2.0DIA-TALL-EMI-MLB-M97-M98
SH0904 2.0DIA-TALL-EMI-MLB-M97-M98
SH0910 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0911 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0913 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0912 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0901 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0917 1.4DIA-SHORT-EMI-MLB-M97-M98
SH0914 1.4DIA-SHORT-EMI-MLB-M97-M98
GND_CHASSIS_AUDIO_JACK
=PP1V8_GPU_FB_VDDQ
R0900 10 1% 1/16W MF-LF 402
GPU_FB_A_VREF_DIV
=PP1V8_GPU_FB_VREF_A
R0901 10 1% 1/16W MF-LF 402
GPU_FB_B_VREF_DIV
=PP1V8_GPU_FB_VREF_B
Frame Holes
ZT0915 3R2P5 GND_BATT_CHGND
ZT0940 3R2P5 GND_CHASSIS_LVDS
ZT0950 SL-3.1X2.7-6CIR-NSP GND_CHASSIS_FAN
ZT0960 3R2P5 GND_CHASSIS_SATA
ZT0990 3R2P5 GND_CHASSIS_BATTCONN
Extra FSB Pull-ups
Exist in MRB but not Intel designs. Here for CYA.
If found to be necessary, will move to page14.csa
=PP1V05_S0_MCP_FSB
NO STUFF R0950 220 5% 1/16W MF-LF 402
NO STUFF R0970 200 5% 1/16W MF-LF 402
NO STUFF R0990 150 1% 1/16W MF-LF 402
NO STUFF R0960 62 5% 1/16W MF-LF 402
NO STUFF R0980 150 1% 1/16W MF-LF 402
CPU_DPRSTP_L
FSB_BREQ0_L
FSB_CPURST_L
CPU_INTR
CPU_NMI
ZT0934 STDOFF-4.00D3.0H-TH
ZT0935 STDOFF-4.00D3.0H-TH
ZT0988 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0989 STDOFF-4.50D.98H-1.1-3.48-TH
ZT0991 STDOFF-4.50D.98H-1.1-3.48-TH
NC_LVDS_IG_B_CLKP = LVDS_IG_B_CLK_P
NC_LVDS_IG_B_CLKN = LVDS_IG_B_CLK_N
NC_LVDS_IG_BKL_PWM = LVDS_IG_BKL_PWM
NC_LVDS_IG_A_DATAP<3> = LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3> = LVDS_IG_A_DATA_N<3>
NC_LVDS_IG_B_DATAP<3> = LVDS_IG_B_DATA_P<3>
NC_LVDS_IG_B_DATAN<3> = LVDS_IG_B_DATA_N<3>
Bosses
ZT0951 4.00D1.85H-M1.6X0.35
ZT0952 4.00D1.5H-M1.6X0.35
ZT0953 4.00D1.5H-M1.6X0.35
ZT0954 4.00D1.85H-M1.6X0.35
CPU signals
TP_IMVP6_CLKEN_L = VR_PWRGD_CLKEN_L
CPU_VID<0..6> = IMVP6_VID<0..6>
CPU_BSEL<0..2> = =MCP_BSEL<0..2>
MEM_VTT_EN = =DDRVTT_EN
GPU signals
PEG_D2R_P<0..15> = =PEG_D2R_P<0..15>
PEG_D2R_N<0..15> = =PEG_D2R_N<0..15>
PEG_R2D_C_P<0..15> = =PEG_R2D_C_P<0..15>
PEG_R2D_C_N<0..15> = =PEG_R2D_C_N<0..15>
TP_RTL8211_CLK125 = RTL8211_CLK125
R0931 22 5% 1/16W MF-LF 402
GMUX ALIASES
LCD_BKLT_EN = LVDS_BKL_ON
DP_IG_ML_P<3> = =MCP_HDMI_TXC_P
DP_IG_ML_N<3> = =MCP_HDMI_TXC_N
DP_IG_ML_P<2..0> = =MCP_HDMI_TXD_P<0..2>
DP_IG_ML_N<2..0> = =MCP_HDMI_TXD_N<0..2>
DP_IG_DDC_CLK = =MCP_HDMI_DDC_CLK
DP_IG_DDC_DATA = =MCP_HDMI_DDC_DATA
DP_IG_HPD = =MCP_HDMI_HPD
PM_ALL_GPU_PGOOD = ALL_EG_PGOOD
TP_LVDS_MUX_SEL_EG = LVDS_MUX_SEL_EG
EG_RESET_L = GPU_RESET_L
JTAG_GMUX_TDI = GMUX_JTAG_TDI
JTAG_GMUX_TMS = GMUX_JTAG_TMS
JTAG_GMUX_TDO = GMUX_JTAG_TDO
LVDS_IG_BKL_ON = IG_BKLT_EN
LVDS_IG_PANEL_PWR = IG_LCD_PWR_EN
MCP79 PCIe PRSNT# Straps
These need work. Add other PRSNT# straps if needed.
NO STUFF R0925 0 5% 1/16W MF-LF 402
PCIE_FW_PRSNT_L
R0927 0 5% 1/16W MF-LF 402 NO STUFF
PEG_PRSNT_L
R0926 0 5% 1/16W MF-LF 402
EG_CLKREQ_OUT_L
MCP_MII_PD
=MCP_MII_RXER
=MCP_MII_CRS
=MCP_MII_COL
R0930 47K 5% 1/16W MF-LF 402
NC_USB_EXTDP = USB_EXTD_P
NC_USB_EXTDN = USB_EXTD_N
NC_USB_MINIP = USB_MINI_P
NC_USB_MININ = USB_MINI_N
USB_CARDREADER_P = TP_USB_11P
USB_CARDREADER_N = TP_USB_11N
NC_USB_EXCARDP = USB_EXCARD_P
NC_USB_EXCARDN = USB_EXCARD_N
GMUX_INT = =DVI_HPD_GMUX_INT
R0903 0 5% 1/16W MF-LF 402
MCP_SPKR SMC_MCP_SAFE_MODE
TP_MEM_A_A<15> = MEM_A_A<15>
TP_MEM_B_A<15> = MEM_B_A<15>
NC_USB_EXTCP = USB_EXTC_P
NC_USB_EXTCN = USB_EXTC_N
TP_CPU_PECI_MCP = CPU_PECI_MCP
FW_PLUG_DET_L = FW_PME_L
FW643_WAKE_L = =FW_PME_L
UNUSED EXPRESS CARD LANE
PCIE_EXCARD_D2R_P = TP_PCIE_EXCARD_D2R_P
PCIE_EXCARD_D2R_N = TP_PCIE_EXCARD_D2R_N
PCIE_EXCARD_R2D_C_P = TP_PCIE_EXCARD_R2D_C_P
PCIE_EXCARD_R2D_C_N = TP_PCIE_EXCARD_R2D_C_N
PCIE_EXCARD_PRSNT_L = TP_PCIE_EXCARD_PRSNT_L
EXCARD_CLKREQ_L = TP_EXCARD_CLKREQ_L
PCIE_CLK100M_EXCARD_P = TP_PCIE_CLK100M_EXCARD_P
PCIE_CLK100M_EXCARD_N = TP_PCIE_CLK100M_EXCARD_N
AUDIO ALIASES
=PP5V_S3_AUDIO XW0901 SM PP5V_S3_AUDIO_AMP
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
ETHERNET ALIASES
=P3V3ENET_EN = PM_SLP_RMGT_L
=P1V05ENET_EN
=PP3V3_ENET_PHY_VDDREG = TP_PP3V3_ENET_PHY_VDDREG
=RTL8211_REGOUT = NC_RTL8211_REGOUT
=RTL8211_ENSWREG
=PP1V05_S0_MCP_SATA_DVDD1
=PP1V05_S0_MCP_SATA_AVDD1
Digital Ground
GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.09MM
VOLTAGE=0V
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
PAGE TITLE
Signal Aliases
Apple Inc.
DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 9 OF 109
SHEET
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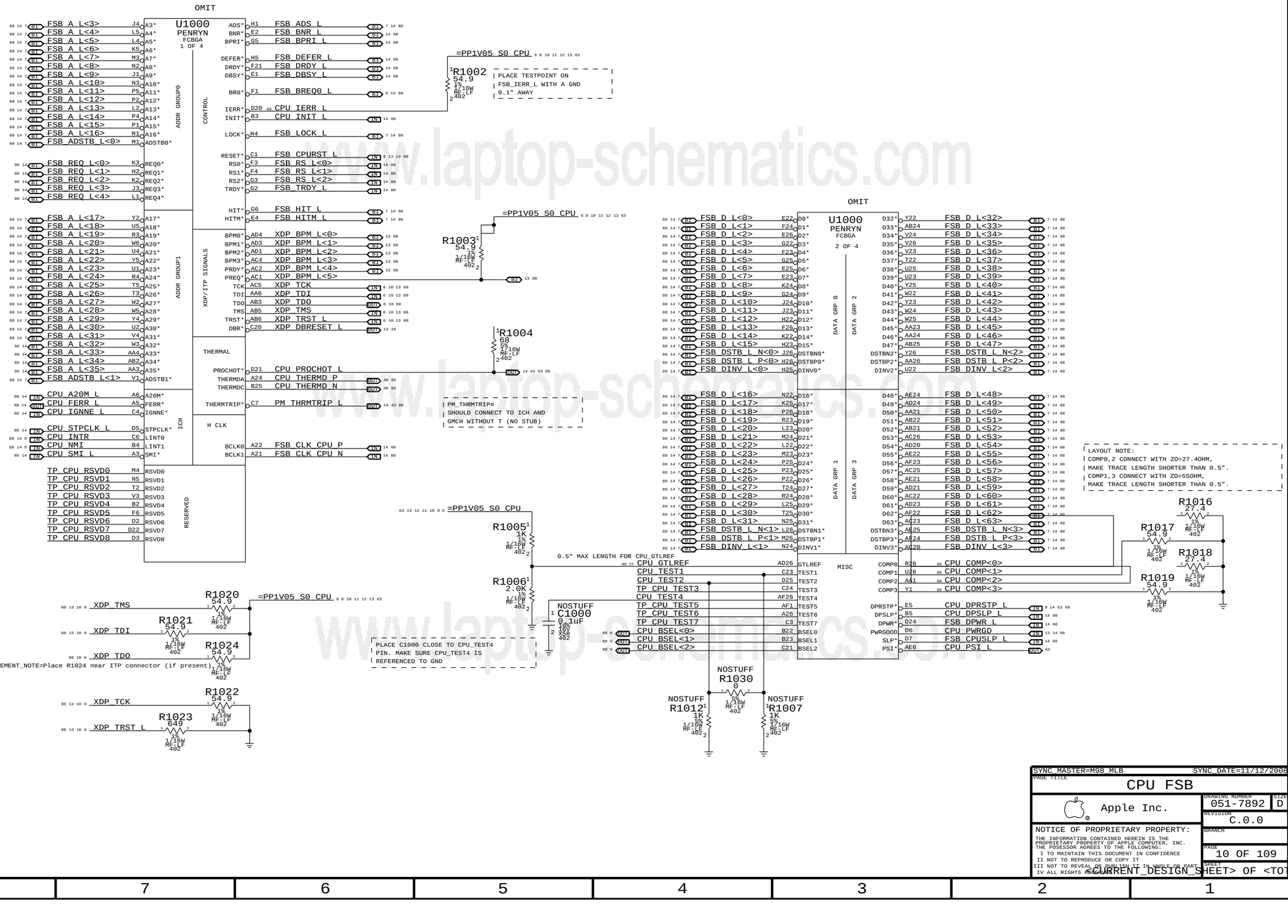

SYNC_MASTER=M98_MLB SYNC_DATE=11/12/2008

PAGE TITLE: CPU FSB

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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PAGE: 10 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

(CPU CORE POWER)

=PPVCORE_S0_CPU 8 11 12 46

Standard Voltage:

44.0 A (Design Target)

41.0 A (HFM)
30.4 A (LFM)
25.5 A (SuperLFM)

27.4 A (Auto-Halt/Stop-Grant HFM)
17.0 A (Auto-Halt/Stop-Grant SuperLFM)

27.4 A (Sleep HFM)
16.8 A (Sleep SuperLFM)

25.0 A (Deep Sleep HFM)
16.0 A (Deep Sleep SuperLFM)

11.5 A (Deeper Sleep)

9.4 A (Enhanced Deeper Sleep)

Low Voltage:

23.0 A (Design Target)

21.0 A (HFM)
18.7 A (LFM)
TBD A (SuperLFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant SuperLFM)

TBD A (Sleep HFM)
TBD A (Sleep SuperLFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep SuperLFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

17.0 A (Design Target)

TBD A (HFM)
TBD A (LFM)

TBD A (Auto-Halt/Stop-Grant HFM)
TBD A (Auto-Halt/Stop-Grant SuperLFM)

TBD A (Sleep HFM)
TBD A (Sleep SuperLFM)

TBD A (Deep Sleep HFM)
TBD A (Deep Sleep LFM)

TBD A (Deeper Sleep)

TBD A (Enhanced Deeper Sleep)

OMIT
U1000
PENRYN
FCBGA
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VCC: A7, A9, A10, A12, A13, A15, A17, A18, A20, B7, B9, B10, B12, B14, B15, B17, B18, B20, C9, C10, C12, C13, C15, C17, C18, D9, D10, D12, D14, D15, D17, D18, E7, E9, E10, E12, E13, E15, E17, E18, E20, F7, F9, F10, F12, F14, F15, F17, F18, F20, AA7, AA9, AA10, AA12, AA13, AA15, AA17, AA18, AA20, AB9, AC10, AB10, AB12, AB14, AB15, AB17, AB18

VCC: AB20, AB7, AC7, AC9, AC12, AC13, AC15, AC17, AC18, AD7, AD9, AD10, AD12, AD14, AD15, AD17, AD18, AE9, AE10, AE12, AE13, AE15, AE17, AE18, AE20, AF9, AF10, AF12, AF14, AF15, AF17, AF18, AF20

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU 6 8 10 12 13 63

4500 mA (before VCC stable)
2500 mA (after VCC stable)

VCCP: G21, V6, J6, K6, M6, J21, K21, M21, N21, N6, R21, R6, T21, T6, V21, W21

(CPU INTERNAL PLL POWER 1.5V)

=PP1V5_S0_CPU 8 12

130 mA

VCCA: B26, C26

VID0 AD6 CPU_VID<0> OUT 9 88
VID1 AF5 CPU_VID<1> OUT 9 88
VID2 AE5 CPU_VID<2> OUT 9 88
VID3 AF4 CPU_VID<3> OUT 9 88
VID4 AE3 CPU_VID<4> OUT 9 88
VID5 AF3 CPU_VID<5> OUT 9 88
VID6 AE2 CPU_VID<6> OUT 9 88

VCCSENSE AF7 CPU_VCCSENSE_P OUT 63 88

VSSSENSE AE7 CPU_VCCSENSE_N OUT 63 88

=PPVCORE_S0_CPU 8 11 12 46

R1100
100
1% 1/16W MF-LF
2 402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

R1101
100
1% 1/16W MF-LF
2 402
PLACEMENT_NOTE=Place within 1 inch of CPU, no stub.

OMIT
U1000
PENRYN
FCBGA
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VSS: A4, A8, A11, A14, A16, A19, A23, AF2, B6, B8, B11, B13, B16, B19, B21, B24, C5, C8, C11, C14, C16, C19, C2, C22, C25, D1, D4, D8, D11, D13, D16, D19, D23, D26, E3, E6, E8, E11, E14, E16, E19, E21, E24, F5, F8, F11, F13, F16, F19, F2, F22, F25, G4, G1, G23, G26, H3, H6, H21, H24, J2, J5, J22, J25, K1, K4, K23, K26, L3, L6, L21, L24, M2, M5, M22, M25, N1, N4, N23, N26, P3, B1

VSS: P6, P21, P24, R2, R5, R22, R25, T1, T4, T23, T26, U3, U6, U21, U24, V2, V5, V22, V25, W1, W4, W23, W26, Y3, Y6, Y21, Y24, AA2, AA5, AA8, AA11, AA14, AA16, AA19, AA22, AA25, AB1, AB4, AB8, AB11, AB13, AB16, AB19, AB23, AB26, AC3, AC6, AC8, AC11, AC14, AC16, AC19, AC21, AC24, AD2, AD5, AD8, AD11, AD13, AD16, AD19, AD22, AD25, AE1, AE4, AE8, AE11, AE14, AE16, AE19, AE23, AE26, A2, AF6, AF8, AF11, AF13, AF16, AF19, AF21, A25, AF25

Current numbers from Merom for Santa Rosa EMTS, doc #22221.

SYNC_MASTER=M98_MLB SYNC_DATE=11/12/2008

PAGE TITLE: CPU Power & Ground

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
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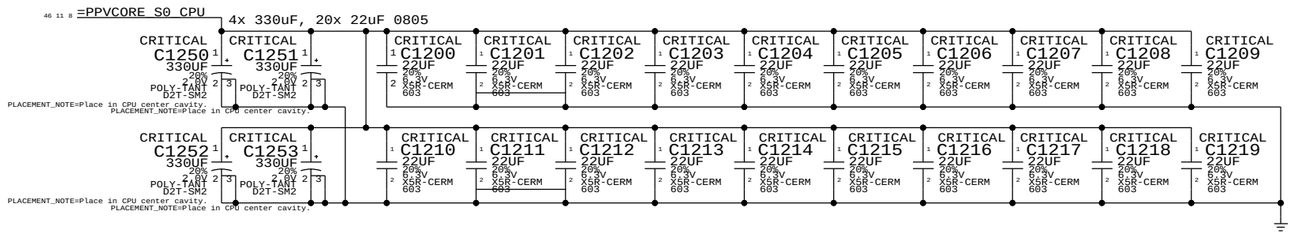
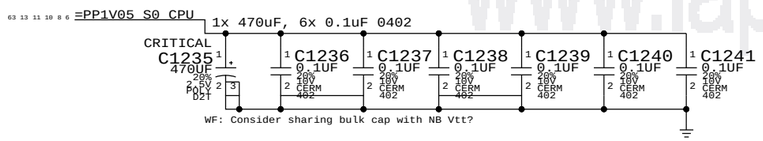
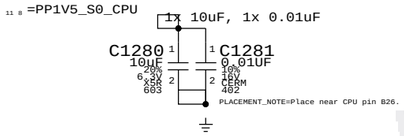
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

PAGE TITLE: CPU Decoupling & VID

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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PAGE: 12 OF 109

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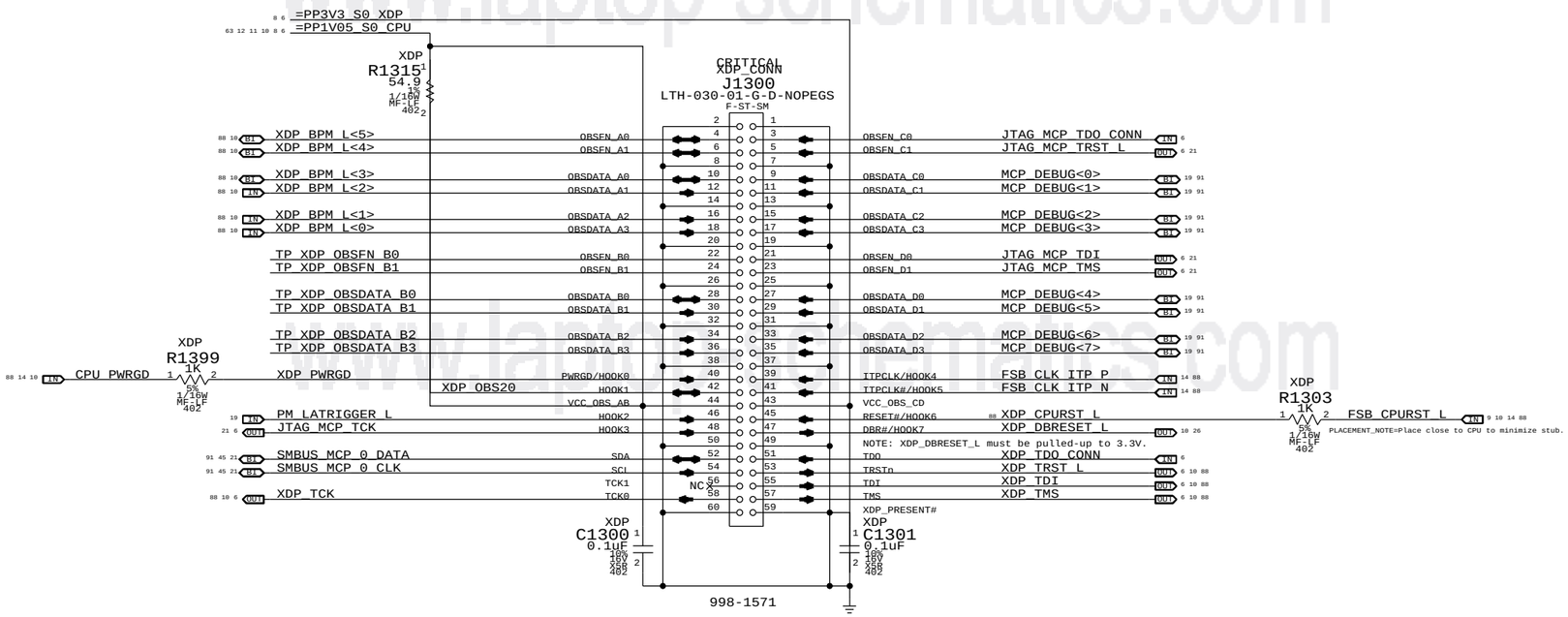
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout



Direction of XDP module

Please avoid any obstructions
on even-numbered side of J1300

SYNC_MASTER=M98_MLB SYNC_DATE=11/12/2008

PAGE TITLE: eXtended Debug Port(MiniXDP)

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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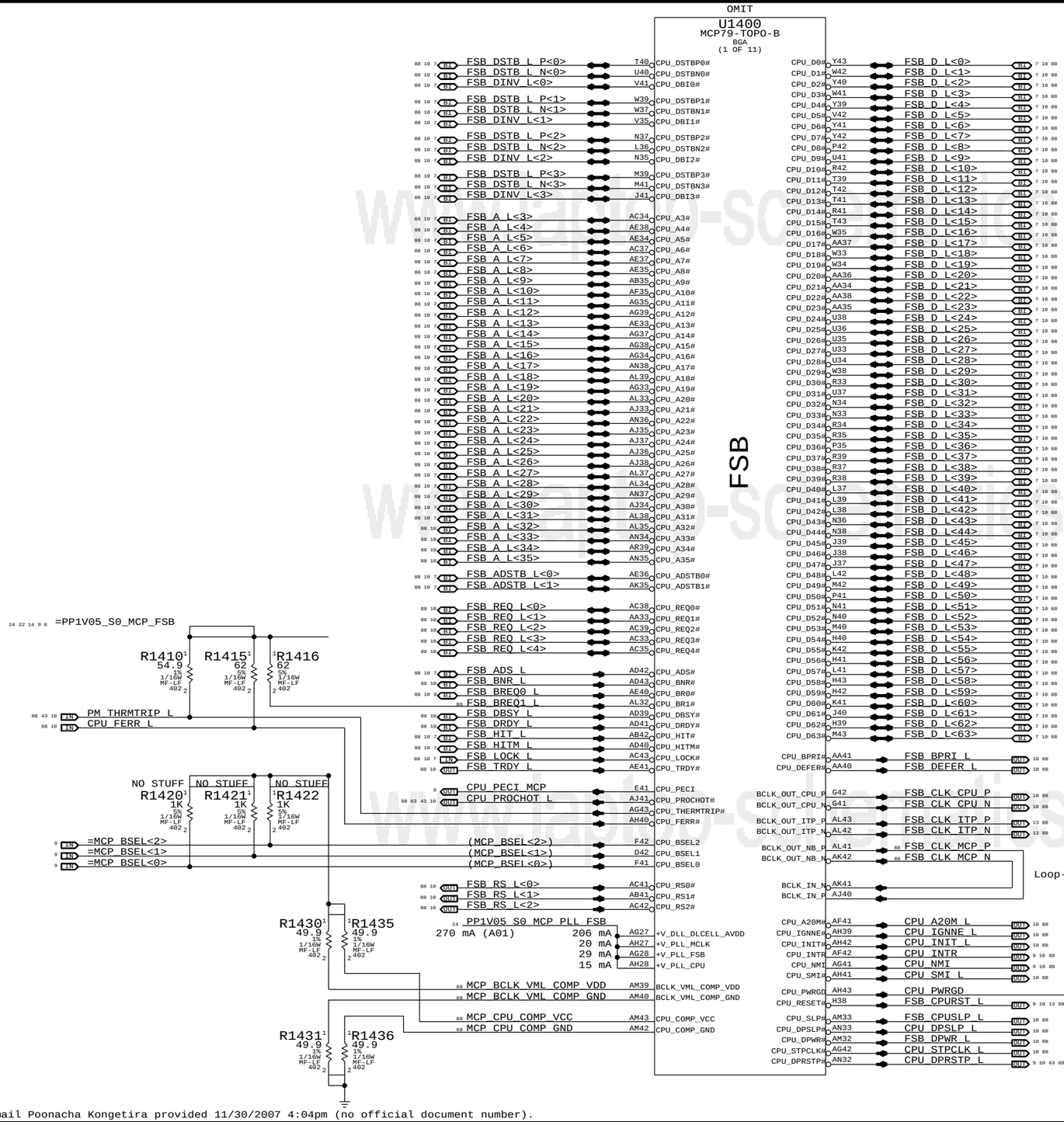
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE: MCP CPU Interface

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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PAGE: 14 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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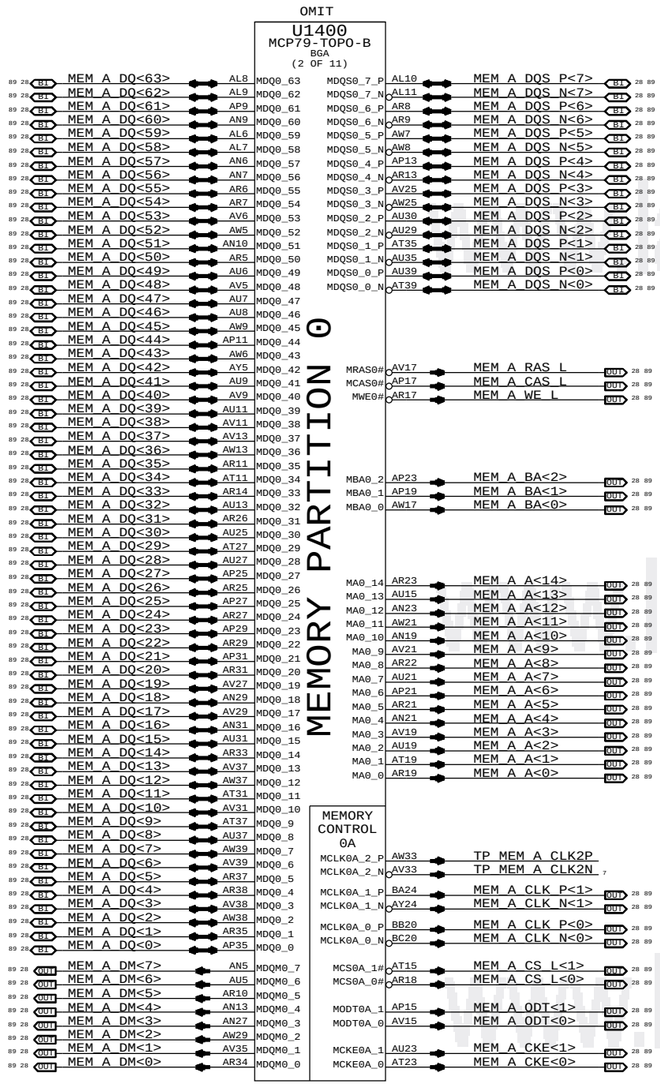

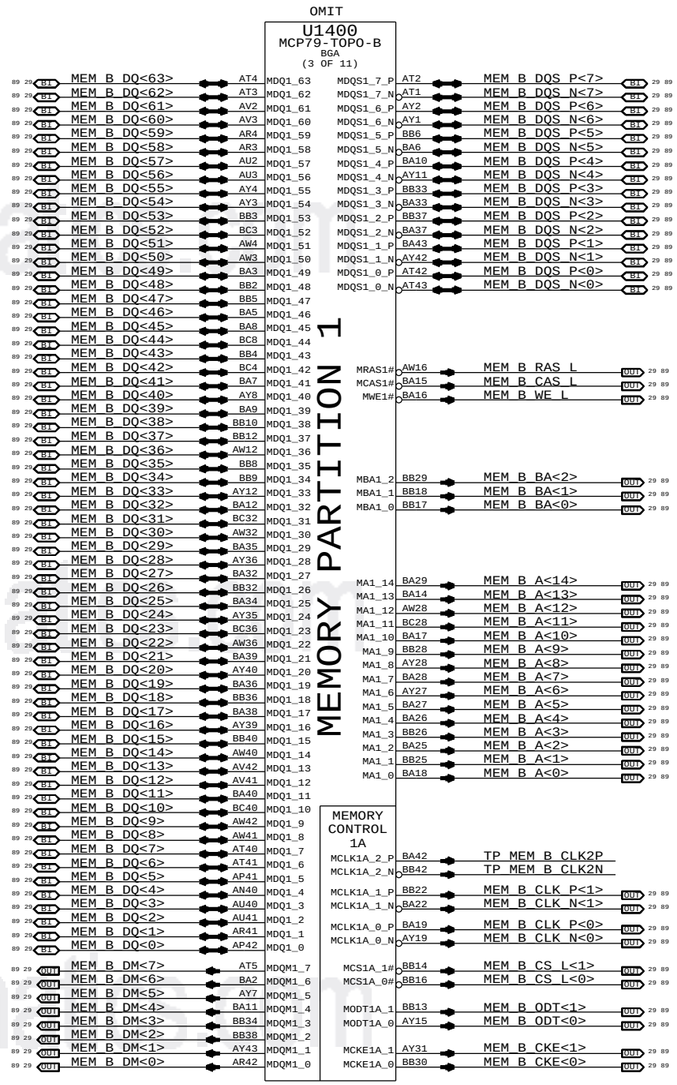

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE
MCP Memory Interface

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
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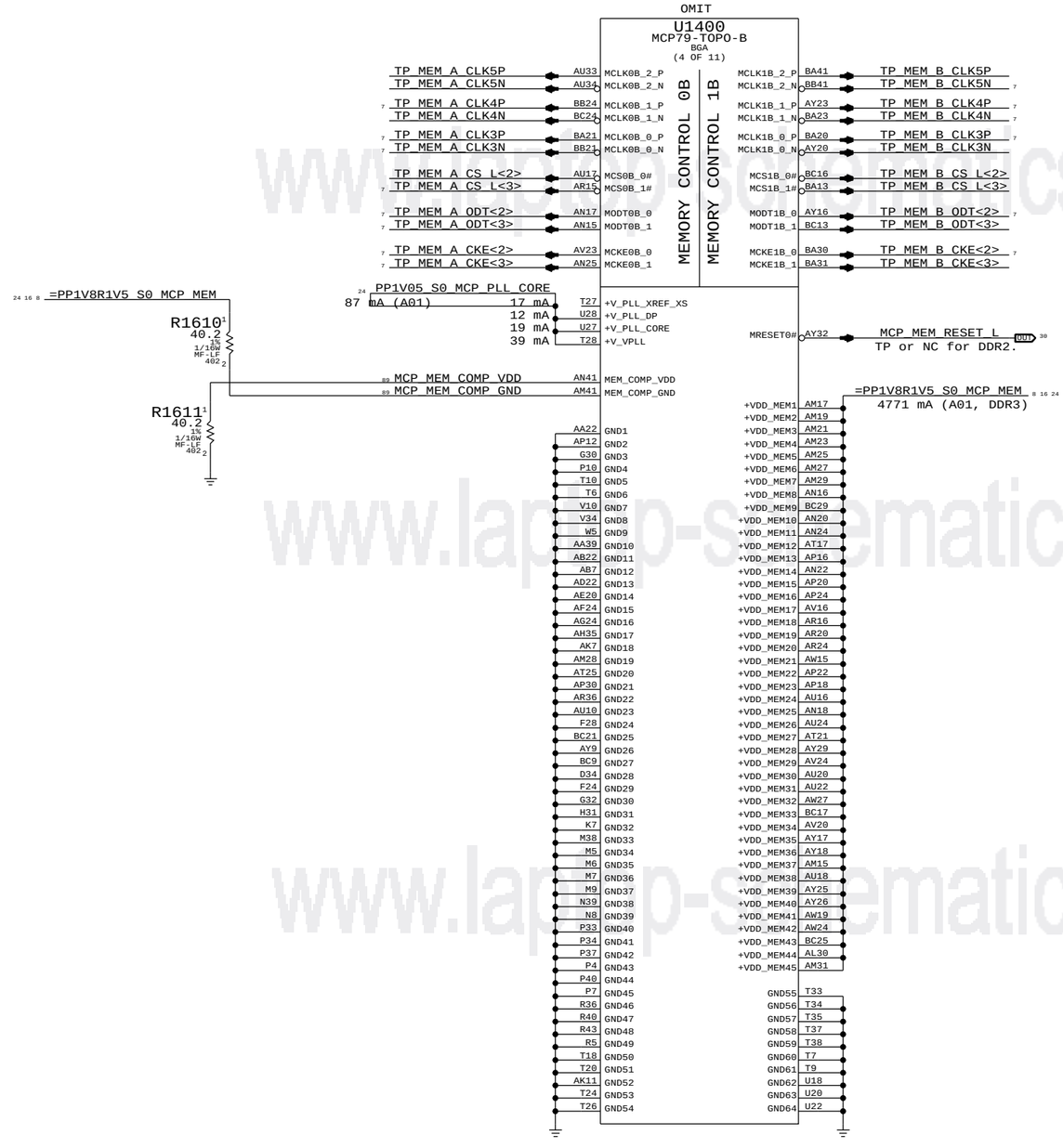
PAGE 15 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE: MCP Memory Misc

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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PAGE: 16 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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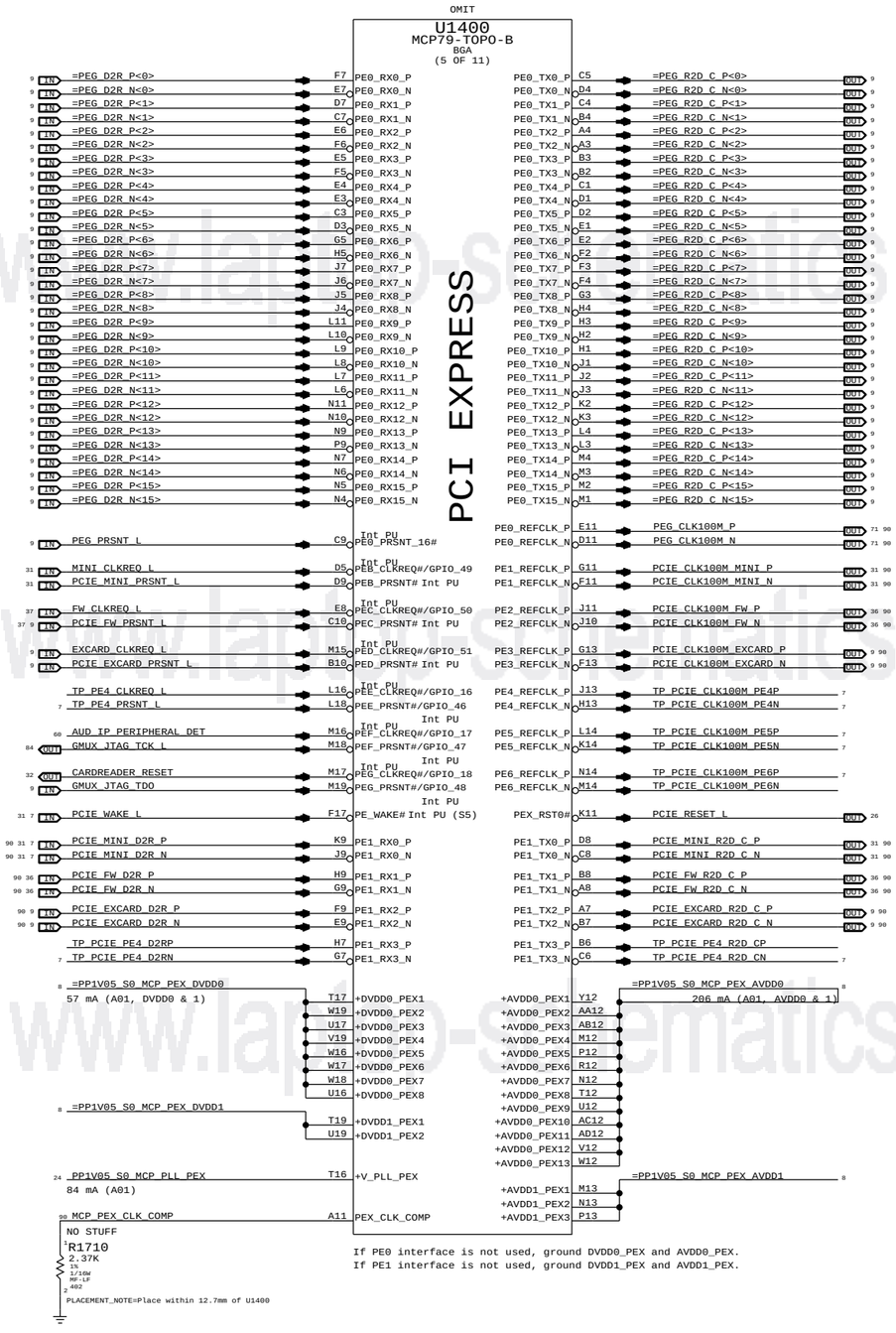

SYNC_MASTER=T18_MLB SYNC_DATE=04/04/2008

PAGE TITLE
MCP PCIe Interfaces

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 17 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

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OMIT

U1400
MCP79-TOPO-B
BGA
(6 OF 11)

LAN

ENET_RXD<0>	C23	RGMII_RXD0	
ENET_RXD<1>	B23	RGMII_RXD1	
ENET_RXD<2>	E24	RGMII_RXD2	
ENET_RXD<3>	A24	RGMII_RXD3	
ENET_CLK125M_RXCLK	A23	RGMII_RXC/MII_RXCLK	
ENET_RX_CTRL	C22	RGMII_RXCTL/MII_RXDV	
=MCP_MII_RXER	F23	MII_RXER/GPIO_36	
=MCP_MII_COL	B26	MII_COL/GPIO_20/MSMB_DATA	
=MCP_MII_CRS	B22	MII_CRS/GPIO_21/MSMB_CLK	
TP_ENET_INTR_L	J22	RGMII_INTR/GPIO_35	
PP1V05_ENET_MCP_PLL_MAC 5 mA (A01)	T23	+V_DUAL_MACPLL	
MCP_MII_COMP_VDD	C27	MII_COMP_VDD	
MCP_MII_COMP_GND	B27	MII_COMP_GND	

DACS

TP_MCP_RGB_DAC_RSET	C39	RGB_DAC_RSET	
TP_MCP_RGB_DAC_VREF	B38	RGB_DAC_VREF	
MCP_TV_DAC_RSET	E36	TV_DAC_RSET	
MCP_TV_DAC_VREF	A35	TV_DAC_VREF	
MCP_CLK27M_XTALIN	C38	XTALIN_TV	
MCP_CLK27M_XTALOUT	D38	XTALOUT_TV	

TV / Component
C / Pr
Y / Y
Comp / Pb

LPCPLUS_GPIO	E16	GPIO_6/FERR*/IGPU_GPIO_6	
DP_IG_CA_DET	B15	GPIO_7/NFERR*/IGPU_GPIO_7	
LVDS_IG_BKL_PWM (See below)	G39	LCD_BKL_CTL/GPIO_57	
LVDS_IG_BKL_ON	E37	LCD_BKL_ON/GPIO_59	
LVDS_IG_PANEL_PWR	F40	LCD_PANEL_PWR/GPIO_58	
=MCP_HDMI_TXC_P	D35	HDMI_TXC_P/ML0_LANE3_P	
=MCP_HDMI_TXC_N	E35	HDMI_TXC_N/ML0_LANE3_N	
=MCP_HDMI_TXD_P<0>	G35	HDMI_TXD0_P/ML0_LANE2_P	
=MCP_HDMI_TXD_N<0>	F35	HDMI_TXD0_N/ML0_LANE2_N	
=MCP_HDMI_TXD_P<1>	F33	HDMI_TXD1_P/ML0_LANE1_P	
=MCP_HDMI_TXD_N<1>	G33	HDMI_TXD1_N/ML0_LANE1_N	
=MCP_HDMI_TXD_P<2>	J33	HDMI_TXD2_P/ML0_LANE0_P	
=MCP_HDMI_TXD_N<2>	H33	HDMI_TXD2_N/ML0_LANE0_N	
DP_IG_AUX_CH_P	D43	DP_AUX_CH0_P	
DP_IG_AUX_CH_N	C43	DP_AUX_CH0_N	
=DVI_HPD_GMUX_INT (See below)	C31	HPLUG_DET2/GPIO_22	
=MCP_HDMI_HPD	F31	HPLUG_DET3	
=PP3V3R1V8_S0_MCP_IFP_VDD 190 mA (A01, 1.8V)	M27	+VDD_IFPA	
	M26	+VDD_IFPB	
PP3V3_S0_MCP_VPLL 16 mA (A01)	M28	+V_PLL_IFPAB 8 mA	
	M29	+V_PLL_HDMI 8 mA	
=PP1V05_S0_MCP_HDMI_VDD 95 mA (A01)	T25	+VDD_HDMI	
MCP_HDMI_RSET	J31	HDMI_RSET	
MCP_HDMI_VPROBE	J30	HDMI_VPROBE	

FLAT PANEL

=PP3V3_ENET_MCP_RMGT	J24, K24	+3.3V_DUAL_RMGT1, +3.3V_DUAL_RMGT2	83 mA (A01)
=PP1V05_ENET_MCP_RMGT	U23, V23	+V_DUAL_RMGT1, +V_DUAL_RMGT2	131 mA (A01)
MCP_MII_VREF	E28	MII_VREF	
ENET_TXD<0>	B24	RGMII_TXD0	
ENET_TXD<1>	C24	RGMII_TXD1	
ENET_TXD<2>	C25	RGMII_TXD2	
ENET_TXD<3>	D25	RGMII_TXD3	
ENET_CLK125M_TXCLK	D24	RGMII_TXC/MII_TXCLK	
ENET_TX_CTRL	C26	RGMII_TXCTL/MII_TXEN	
ENET_MDC	D21	RGMII_MDC	
ENET_MDIO	C21	RGMII_MDIO	
TP_ENET_PWRDWN_L	G23	RGMII_PWRDWN/GPIO_37	
MCP_CLK25M_BUF0_R	E23	BUF_25MHZ	
ENET_RESET_L	J23	MII_RESET#	
PP3V3_S0_MCP_DAC 103 mA 103 mA	J32, K32	+V_RGB_DAC, +V_TV_DAC	206 mA (A01)
MCP_DDC_CLK0	B31	DDC_CLK0	
MCP_DDC_DATA0	A31	DDC_DATA0	
TP_MCP_RGB_RED	B39	RGB_DAC_RED	
TP_MCP_RGB_GREEN	A39	RGB_DAC_GREEN	
TP_MCP_RGB_BLUE	B40	RGB_DAC_BLUE	
TP_MCP_RGB_HSYNC	A40	RGB_DAC_HSYNC	
TP_MCP_RGB_VSYNC	A41	RGB_DAC_VSYNC	
CRT_IG_R_C_PR	A36	TV_DAC_RED	
CRT_IG_G_Y_Y	B36	TV_DAC_GREEN	
CRT_IG_B_COMP_PB	C36	TV_DAC_BLUE	
CRT_IG_HSYNC	D36	TV_DAC_HSYNC/GPIO_44	
CRT_IG_VSYNC	C37	TV_DAC_VSYNC/GPIO_45	
LVDS_IG_A_CLK_P	B35	IFPA_TXC_P	
LVDS_IG_A_CLK_N	C35	IFPA_TXC_N	
LVDS_IG_A_DATA_P<0>	B32	IFPA_TXD0_P	
LVDS_IG_A_DATA_N<0>	A32	IFPA_TXD0_N	
LVDS_IG_A_DATA_P<1>	D32	IFPA_TXD1_P	
LVDS_IG_A_DATA_N<1>	C32	IFPA_TXD1_N	
LVDS_IG_A_DATA_P<2>	D33	IFPA_TXD2_P	
LVDS_IG_A_DATA_N<2>	C33	IFPA_TXD2_N	
LVDS_IG_A_DATA_P<3>	B34	IFPA_TXD3_P	
LVDS_IG_A_DATA_N<3>	C34	IFPA_TXD3_N	
LVDS_IG_B_CLK_P	L31	IFPB_TXC_P	
LVDS_IG_B_CLK_N	K31	IFPB_TXC_N	
LVDS_IG_B_DATA_P<0>	J29	IFPB_TXD4_P	
LVDS_IG_B_DATA_N<0>	H29	IFPB_TXD4_N	
LVDS_IG_B_DATA_P<1>	L29	IFPB_TXD5_P	
LVDS_IG_B_DATA_N<1>	K29	IFPB_TXD5_N	
LVDS_IG_B_DATA_P<2>	L30	IFPB_TXD6_P	
LVDS_IG_B_DATA_N<2>	K30	IFPB_TXD6_N	
LVDS_IG_B_DATA_P<3>	N30	IFPB_TXD7_P	
LVDS_IG_B_DATA_N<3>	M30	IFPB_TXD7_N	
LVDS_IG_DDC_CLK	C30	DDC_CLK2/GPIO_23	
LVDS_IG_DDC_DATA	B30	DDC_DATA2/GPIO_24	
=MCP_HDMI_DDC_CLK	D31	DDC_CLK3	
=MCP_HDMI_DDC_DATA	E31	DDC_DATA3	
MCP_IFPAB_RSET	E32	IFPAB_RSET	
MCP_IFPAB_VPROBE	G31	IFPAB_VPROBE	

R1850 10K 5% 1/10W MF-LF 402

R1810 49.9 1% 1/10W MF-LF 402
R1811 49.9 1% 1/10W MF-LF 402
R1820 47K 5% 1/10W MF-LF 402
R1860 100K 5% 1/10W MF-LF 402
R1861 100K 5% 1/10W MF-LF 402

=PP3V3_ENET_MCP_RMGT
=PP3V3_S5_MCP_GPIO
=PP3V3_S0_MCP_GPIO

Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:

Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:

Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CHP/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.

NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.
LVDS: Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

GPIOs 57-59 (if LCD panel is used):

In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:

Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

WF: IFP is capable of LVDS (1.8V) or TMDS (3.3V), need aliases

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE: MCP Ethernet & Graphics

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 18 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400
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PCI

PCI_REQ0 L	T2	PCI_REQ0#	
PCI_REQ1 L	V9	PCI_REQ1#/FANRPM2	
FW_PWR_EN	T3	PCI_REQ2#/GPIO_40/RS232_DSR#	
AUD_IPHS_SWITCH_EN	U9	PCI_REQ3#/GPIO_38/RS232_CTS#	
MCP_RS232_SIN_L	T4	PCI_REQ4#/GPIO_52/RS232_SIN#	
MCP_DEBUG<0>	AC3	PCI_AD0	
MCP_DEBUG<1>	AE10	PCI_AD1	
MCP_DEBUG<2>	AC4	PCI_AD2	
MCP_DEBUG<3>	AE11	PCI_AD3	
MCP_DEBUG<4>	AB3	PCI_AD4	
MCP_DEBUG<5>	AC6	PCI_AD5	
MCP_DEBUG<6>	AB2	PCI_AD6	
MCP_DEBUG<7>	AC7	PCI_AD7	
TP_PCI_AD<8>	AC8	PCI_AD8	
TP_PCI_AD<9>	AA2	PCI_AD9	
TP_PCI_AD<10>	AC9	PCI_AD10	
TP_PCI_AD<11>	AC10	PCI_AD11	
TP_PCI_AD<12>	AC11	PCI_AD12	
TP_PCI_AD<13>	AA1	PCI_AD13	
TP_PCI_AD<14>	AA5	PCI_AD14	
TP_PCI_AD<15>	Y5	PCI_AD15	
TP_PCI_AD<16>	W3	PCI_AD16	
TP_PCI_AD<17>	W6	PCI_AD17	
TP_PCI_AD<18>	W4	PCI_AD18	
TP_PCI_AD<19>	W7	PCI_AD19	
TP_PCI_AD<20>	V3	PCI_AD20	
TP_PCI_AD<21>	W8	PCI_AD21	
TP_PCI_AD<22>	V2	PCI_AD22	
TP_PCI_AD<23>	W9	PCI_AD23	
TP_PCI_AD<24>	U3	PCI_AD24	
TP_PCI_AD<25>	W11	PCI_AD25	
TP_PCI_AD<26>	U2	PCI_AD26	
TP_PCI_AD<27>	U5	PCI_AD27	
TP_PCI_AD<28>	U1	PCI_AD28	
TP_PCI_AD<29>	U6	PCI_AD29	
TP_PCI_AD<30>	T5	PCI_AD30	
TP_PCI_AD<31>	U7	PCI_AD31	
TP_PCI_INTW_L	P2	PCI_INTW#	
TP_PCI_INTX_L	N3	PCI_INTX#	
TP_PCI_INTY_L	N2	PCI_INTY#	
TP_PCI_INTZ_L	N1	PCI_INTZ#	
TP_PCI_TRDY_L	Y3	PCI_TRDY#	
PM_CLKRUN_L	AD11	PCI_CLKRUN#/GPIO_42	
FW_PME_L	AE2	LPC_DRQ1#/GPIO_19	Int PU
TP_LPC_DRQ0_L	AE1	LPC_DRQ0#	Int PU
LPC_SERIRQ	AE6	LPC_SERIRQ	Int PU

PCI_GNT0#	R3	TP_PCI_GNT0_L	
PCI_GNT1#/FANCTL2	U10	TP_PCI_GNT1_L	
PCI_GNT2#/GPIO_41/RS232_DTR#	R4	GMUX_JTAG_TMS	
PCI_GNT3#/GPIO_39/RS232_RTS#	U11	GMUX_JTAG_TDI	
PCI_GNT4#/GPIO_53/RS232_SOUT#	P3	MCP_RS232_SOUT_L	
PCI_CBE0#	AA3	TP_PCI_C_BE_L<0>	
PCI_CBE1#	AA6	TP_PCI_C_BE_L<1>	
PCI_CBE2#	AA11	TP_PCI_C_BE_L<2>	
PCI_CBE3#	W10	TP_PCI_C_BE_L<3>	
PCI_DEVSEL#	AA9	TP_PCI_DEVSEL_L	
PCI_FRAME#	Y4	TP_PCI_FRAME_L	
PCI_IRDY#	AA10	TP_PCI_IRDY_L	
PCI_PAR	Y1	TP_PCI_PAR	
PCI_PERR#/GPIO_43/RS232_DCD#	AB9	TP_PCI_PERR_L	
PCI_SERR#	AA7	TP_PCI_SERR_L	
PCI_STOP#	Y2	TP_PCI_STOP_L	
PCI_PME#/GPIO_30 Int PU (S5)	T1	PM_LATRIGGER_L	
PCI_RESET0#	R10	MEM_VTT_EN_R	
PCI_RESET1#	R11	TP_PCI_RESET1_L	
PCI_CLK0	R6	TP_PCI_CLK0	
PCI_CLK1	R7	TP_PCI_CLK1	
PCI_CLK2	R8	PCI_CLK33M_MCP_R	
PCI_CLKIN	R9	PCI_CLK33M_MCP	

R1910 22 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place close to pin R8

LPC

LPC_FRAME#	AD4	LPC_FRAME_R_L	R1960 22 5% 1/16W MF-LF 402	LPC_FRAME_L
LPC_PWRDWN#/GPIO_54/EXT_NMI#	AE12	LPC_PWRDWN_L		
LPC_RESET0#	AE5	LPC_RESET_L		
LPC_AD0	AD3	LPC_AD_R<0>	R1950 22 5% 1/16W MF-LF 402	LPC_AD<0>
LPC_AD1	AD2	LPC_AD_R<1>	R1951 22 5% 1/16W MF-LF 402	LPC_AD<1>
LPC_AD2	AD1	LPC_AD_R<2>	R1952 22 5% 1/16W MF-LF 402	LPC_AD<2>
LPC_AD3	AD5	LPC_AD_R<3>	R1953 22 5% 1/16W MF-LF 402	LPC_AD<3>
LPC_CLK0	AE9	LPC_CLK33M_SMC_R		

R1961 10K 5% 1/16W MF-LF 402

Strap for Boot ROM Selection (See HDA_SDOUT)

GND

U24	GND65	GND98	Y26
U26	GND66	GND99	Y27
U39	GND67	GND100	AB18
U4	GND68	GND101	H34
U8	GND69	GND102	AB20
V16	GND70	GND103	AB21
V17	GND71	GND104	AB23
V18	GND72	GND105	AB24
V20	GND73	GND106	AB25
V22	GND74	GND107	AB26
V24	GND75	GND108	AB27
V26	GND76	GND109	AB28
V27	GND77	GND110	AB34
V28	GND78	GND111	AB37
V33	GND79	GND112	AB4
V37	GND80	GND113	AB40
V4	GND81	GND114	AC22
V40	GND82	GND115	AC36
V7	GND83	GND116	AC40
W20	GND84	GND117	AB33
W22	GND85	GND118	AC5
W24	GND86	GND119	AD16
W36	GND87	GND120	AD17
W40	GND88	GND121	AD18
W43	GND89	GND122	AD19
Y16	GND90	GND123	AD20
Y17	GND91	GND124	AD24
Y18	GND92	GND125	AD25
Y19	GND93	GND126	AD26
Y20	GND94	GND127	AD27
Y22	GND95	GND128	AD28
Y24	GND96	GND129	AD33
Y25	GND97	GND130	AD34

=PP3V3_S0_MCP_GPIO

MCP_RS232_SOUT_L	R1989	8.2K 5% 1/16W MF-LF 402
PCI_REQ0_L	R1990	8.2K 5% 1/16W MF-LF 402
PCI_REQ1_L	R1991	8.2K 5% 1/16W MF-LF 402
FW_PWR_EN	R1992	8.2K 5% 1/16W MF-LF 402
MCP_RS232_SIN_L	R1994	8.2K 5% 1/16W MF-LF 402

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE: MCP PCI & LPC

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 19 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400
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SATA

SATA_HDD_R2D_C_P	AJ7	SATA_A0_TX_P	90 39 OUT
SATA_HDD_R2D_C_N	AJ6	SATA_A0_TX_N	90 39 OUT
SATA_HDD_D2R_N	AJ5	SATA_A0_RX_N	90 39 IN
SATA_HDD_D2R_P	AJ4	SATA_A0_RX_P	90 39 IN
SATA_ODD_R2D_C_P	AJ11	SATA_A1_TX_P	90 39 OUT
SATA_ODD_R2D_C_N	AJ10	SATA_A1_TX_N	90 39 OUT
SATA_ODD_D2R_N	AJ9	SATA_A1_RX_N	90 39 IN
SATA_ODD_D2R_P	AK9	SATA_A1_RX_P	90 39 IN
TP_SATA_C_R2D_CP	AK2	SATA_B0_TX_P	7
TP_SATA_C_R2D_CN	AJ3	SATA_B0_TX_N	7
TP_SATA_C_D2RN	AJ2	SATA_B0_RX_N	
TP_SATA_C_D2RP	AJ1	SATA_B0_RX_P	7
TP_SATA_D_R2D_CP	AM4	SATA_B1_TX_P	
TP_SATA_D_R2D_CN	AL3	SATA_B1_TX_N	
TP_SATA_D_D2RN	AL4	SATA_B1_RX_N	7
TP_SATA_D_D2RP	AK3	SATA_B1_RX_P	7
TP_SATA_E_R2D_CP	AN1	SATA_C0_TX_P	
TP_SATA_E_R2D_CN	AM1	SATA_C0_TX_N	
TP_SATA_E_D2RN	AM2	SATA_C0_RX_N	
TP_SATA_E_D2RP	AM3	SATA_C0_RX_P	
TP_SATA_F_R2D_CP	AP3	SATA_C1_TX_P	
TP_SATA_F_R2D_CN	AP2	SATA_C1_TX_N	
TP_SATA_F_D2RN	AN3	SATA_C1_RX_N	
TP_SATA_F_D2RP	AN2	SATA_C1_RX_P	
TP_MCP_SATALED_L	E12	SATA_LED#	

PP1V05_S0_MCP_PLL_SATA — AE16 +V_PLL_SATA — 24
84 mA (A01)

=PP1V05_S0_MCP_SATA_DVDD0 — 8
43 mA (A01, DVDD0 & 1)
Minimum 1.025V for Gen2 support

AF19	+DVDD0_SATA1
AG16	+DVDD0_SATA2
AG17	+DVDD0_SATA3
AG19	+DVDD0_SATA4

=PP1V05_S0_MCP_SATA_DVDD1 — 9

AH17	+DVDD1_SATA1
AH19	+DVDD1_SATA2

=PP1V05_S0_MCP_SATA_AVDD0 — 8
127 mA (A01, AVDD0 & 1)
Minimum 1.025V for Gen2 support

AJ12	+AVDD0_SATA1
AN11	+AVDD0_SATA2
AK12	+AVDD0_SATA3
AK13	+AVDD0_SATA4
AL12	+AVDD0_SATA5
AM11	+AVDD0_SATA6
AM12	+AVDD0_SATA7
AN12	+AVDD0_SATA8
AL13	+AVDD0_SATA9

=PP1V05_S0_MCP_SATA_AVDD1 — 9

AN14	+AVDD1_SATA1
AL14	+AVDD1_SATA2
AM13	+AVDD1_SATA3
AM14	+AVDD1_SATA4

MCP_SATA_TERMP — AE3 SATA_TERMP — 90

R2010
2.49K
1% 1/16W MF-LF
402

USB

External A

USB0_P	C29	USB_EXTA_P	91
USB0_N	D29	USB_EXTA_N	91

AirPort (PCIe Mini-Card)

USB1_P	C28	USB_MINI_P	91
USB1_N	D28	USB_MINI_N	91

External D

USB2_P	A28	USB_EXTD_P	91
USB2_N	B28	USB_EXTD_N	91

Camera

USB3_P	F29	USB_CAMERA_P	7 31 91
USB3_N	G29	USB_CAMERA_N	7 31 91

IR

USB4_P	K27	USB_IR_P	41 91
USB4_N	L27	USB_IR_N	41 91

Geyser Trackpad/Keyboard

USB5_P	J26	USB_TPAD_P	50 91
USB5_N	J27	USB_TPAD_N	50 91

Bluetooth

USB6_P	F27	USB_BT_P	7 31 91
USB6_N	G27	USB_BT_N	7 31 91

External B

USB7_P	D27	USB_EXTB_P	40 91
USB7_N	E27	USB_EXTB_N	40 91

ExpressCard

USB8_P	K25	USB_EXCARD_P	9 91
USB8_N	L25	USB_EXCARD_N	9 91

External C

USB9_P	H25	USB_EXTC_P	9 91
USB9_N	J25	USB_EXTC_N	9 91

USB10_P	F25	TP_USB_10P	7
USB10_N	G25	TP_USB_10N	7

SD Card Reader

USB11_P	K23	USB_CARDREADER_P	9 32 96
USB11_N	L23	USB_CARDREADER_N	9 32 96

USB_OC0#/GPIO_25	L21	USB_EXTA_OC_L — 40
USB_OC1#/GPIO_26	K21	USB_EXTB_OC_L — 40
USB_OC2#/GPIO_27/MGPIO	J21	USB_EXTC_OC_L
USB_OC3#/GPIO_28/MGPIO	H21	EXCARD_OC_L — 43

=PP3V3_S5_MCP_GPIO — 8 18

R2051 8.2K 5% 1/16W MF-LF 402
R2053 8.2K 5% 1/16W MF-LF 402
R2050 8.2K 5% 1/16W MF-LF 402
R2052 8.2K 5% 1/16W MF-LF 402

+V_PLL_USB — L28 PP3V3_S0_MCP_PLL_USB — 24
19 mA (A01)

USB_RBIAS_GND — A27 — 91 MCP_USB_RBIAS_GND

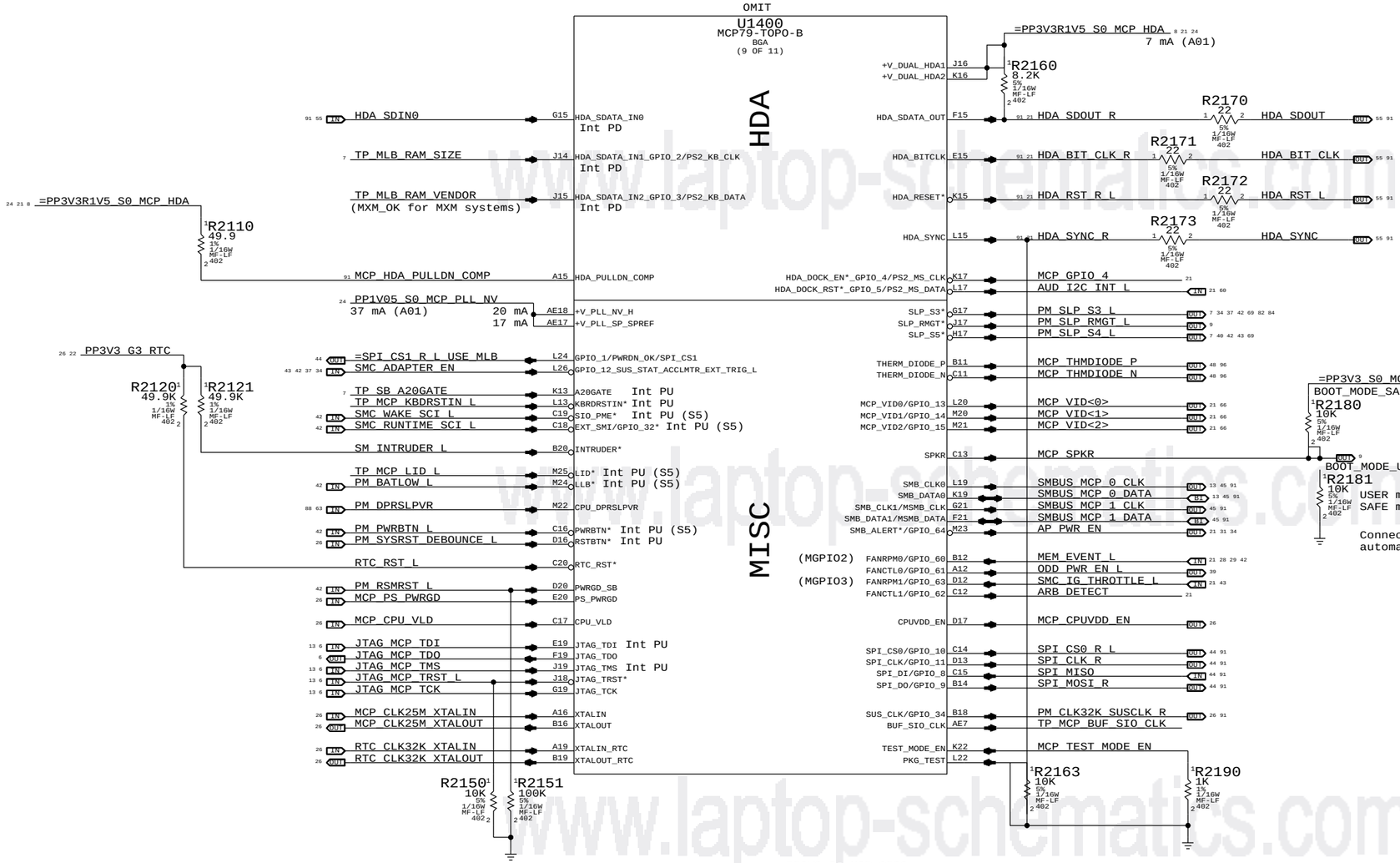
R2060
806
1% 1/16W MF-LF 402

GND131	AD35
GND132	AD37
GND133	AD38
GND134	AE22
GND135	AE24
GND136	AE39
GND137	AE4
GND138	AD6
GND139	AF16
GND140	AF17
GND141	AF18
GND142	AF20
GND143	AF22
GND144	AF26
GND145	AF27
GND146	AF28
GND147	AF33
GND148	AF34
GND149	AF37
GND150	AF40
GND151	AG18
GND152	AG20
GND153	AG22
GND154	AG26
GND155	AG36
GND156	AG40
GND157	AH18
GND158	AH20
GND159	AH22
GND160	AH24

If all SATA_Ax & Bx pins are not used, ground DVDD0_SATA and AVDD0_SATA.
If all SATA_Cx pins are not used, ground DVDD1_SATA and AVDD1_SATA.

SYNC_MASTER=T18_MLB	SYNC_DATE=12/12/2008
PAGE TITLE	MCP SATA & USB
Apple Inc.	DRAWING NUMBER 051-7892 · SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 20 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L

R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.

NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.

NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

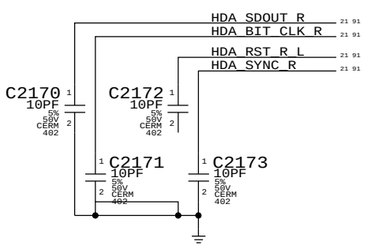
SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

HDA Output Caps

For EMI Reduction on HDA interface



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE: MCP HDA & MISC

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

OMIT

U1400
MCP79-TOPO-B
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GND

AH26	GND161	GND253	AV40
AH33	GND162	GND254	BA1
AH34	GND163	GND255	BA4
AH37	GND164	GND256	AW31
AH38	GND165	GND257	AY6
AJ39	GND166	GND258	L35
AJ8	GND167	GND259	BC33
AK10	GND168	GND260	BC37
AK33	GND169	GND261	BC41
AK34	GND170	GND262	AY14
AK37	GND171	GND263	BC5
AK4	GND172	GND264	C2
AK40	GND173	GND265	D10
AL36	GND174	GND266	D14
AL40	GND175	GND267	D15
AL5	GND176	GND268	D18
AM10	GND177	GND269	D19
AM16	GND178	GND270	D22
AM18	GND179	GND271	D23
AM20	GND180	GND272	D26
AM22	GND181	GND273	D30
AM24	GND182	GND274	D37
AM26	GND183	GND275	D6
AM30	GND184	GND276	E13
AM34	GND185	GND277	E17
AM35	GND186	GND278	E21
AM37	GND187	GND279	E25
AM38	GND188	GND280	E29
AM5	GND189	GND281	E33
AM6	GND190	GND282	F12
AM7	GND191	GND283	F16
AM9	GND192	GND284	F32
AP26	GND193	GND285	F8
AN28	GND194	GND286	G10
AN30	GND195	GND287	G12
AN39	GND196	GND288	G14
AN4	GND197	GND289	G16
Y7	GND198	GND290	BC12
AP10	GND199	GND291	G22
AU26	GND200	GND292	G24
AP14	GND201	GND293	AW20
AU14	GND202	GND294	G34
AP28	GND203	GND295	G4
AP32	GND204	GND296	G43
AP34	GND205	GND297	G6
AP36	GND206	GND298	G8
AP37	GND207	GND299	H11
AP4	GND208	GND300	H15
AP40	GND209	GND301	AW35
AP7	GND210	GND302	H23
AW23	GND211	GND303	AN8
AR28	GND212	GND304	G40
AR32	GND213	GND305	J12
AR40	GND214	GND306	J8
AT10	GND215	GND307	K10
AR12	GND216	GND308	K12
AT13	GND217	GND309	K18
AT29	GND218	GND310	K26
AT33	GND219	GND311	K37
AT6	GND220	GND312	K4
AT7	GND221	GND313	K40
AT9	GND222	GND314	K8
AY21	GND223	GND315	AU1
AY22	GND224	GND316	L40
L12	GND225	GND317	L43
AU12	GND226	GND318	L5
AU28	GND227	GND319	M10
AP33	GND228	GND320	M34
AU32	GND229	GND321	M35
AR30	GND230	GND322	M37
AU36	GND231	GND323	Y28
AU38	GND232	GND324	Y33
AU4	GND233	GND325	Y34
G28	GND234	GND326	Y35
F20	GND235	GND327	Y37
AV28	GND236	GND328	Y38
AV32	GND237	GND329	AB17
AV36	GND238	GND330	AB16
AV4	GND239	GND331	AN26
AV7	GND240	GND332	AD7
AW11	GND241	GND333	M11
G20	GND242	GND334	AA4
AR43	GND243	GND335	AB19
AW43	GND244	GND336	AY13
AY10	GND245	GND337	P11
AV12	GND246	GND338	Y6
AY30	GND247	GND339	T11
AY33	GND248	GND340	V11
AY34	GND249	GND341	Y11
AY37	GND250	GND342	AH16
AY38	GND251	GND343	T22
AY41	GND252		

OMIT

U1400
MCP79-TOPO-B
BGA
(10 OF 11)

POWER

46 24 8 =PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)

AA25	+VDD_CORE1	+VTT_CPU1	R32	=PP1V05_S0_MCP_FSB 8 9 14 24
AC23	+VDD_CORE2	+VTT_CPU2	AC32	1139 mA 1182 mA (A01)
U25	+VDD_CORE3	+VTT_CPU3	E40	
AH12	+VDD_CORE4	+VTT_CPU4	J36	
AG10	+VDD_CORE5	+VTT_CPU5	N32	
AG5	+VDD_CORE6	+VTT_CPU6	T32	
Y21	+VDD_CORE7	+VTT_CPU7	U32	
Y23	+VDD_CORE8	+VTT_CPU8	V32	
AA16	+VDD_CORE9	+VTT_CPU9	W32	
AA26	+VDD_CORE10	+VTT_CPU10	P31	
AA27	+VDD_CORE11	+VTT_CPU11	AF32	
AA28	+VDD_CORE12	+VTT_CPU12	AE32	
AC16	+VDD_CORE13	+VTT_CPU13	AH32	
AC17	+VDD_CORE14	+VTT_CPU14	AJ32	
AC18	+VDD_CORE15	+VTT_CPU15	AK31	
AC19	+VDD_CORE16	+VTT_CPU16	AK32	
AC20	+VDD_CORE17	+VTT_CPU17	AD32	
AC21	+VDD_CORE18	+VTT_CPU18	AL31	
AA17	+VDD_CORE19	+VTT_CPU19	AB32	
AC24	+VDD_CORE20	+VTT_CPU20	B41	
AC25	+VDD_CORE21	+VTT_CPU21	B42	
AC26	+VDD_CORE22	+VTT_CPU22	C40	
AC27	+VDD_CORE23	+VTT_CPU23	C41	
AC28	+VDD_CORE24	+VTT_CPU24	C42	
AD21	+VDD_CORE25	+VTT_CPU25	D39	
AD23	+VDD_CORE26	+VTT_CPU26	D40	
W27	+VDD_CORE27	+VTT_CPU27	D41	
V25	+VDD_CORE28	+VTT_CPU28	E38	
AA18	+VDD_CORE29	+VTT_CPU29	E39	
AE19	+VDD_CORE30	+VTT_CPU30	F37	
AE21	+VDD_CORE31	+VTT_CPU31	F38	
AE23	+VDD_CORE32	+VTT_CPU32	F39	
AE25	+VDD_CORE33	+VTT_CPU33	G36	
AE26	+VDD_CORE34	+VTT_CPU34	G37	
AE27	+VDD_CORE35	+VTT_CPU35	G38	
AE28	+VDD_CORE36	+VTT_CPU36	H35	
AF10	+VDD_CORE37	+VTT_CPU37	H37	
AF11	+VDD_CORE38	+VTT_CPU38	J34	
AA19	+VDD_CORE39	+VTT_CPU39	J35	
AF2	+VDD_CORE40	+VTT_CPU40	K33	
AF21	+VDD_CORE41	+VTT_CPU41	K34	
AF23	+VDD_CORE42	+VTT_CPU42	K35	
AF25	+VDD_CORE43	+VTT_CPU43	L32	
AF3	+VDD_CORE44	+VTT_CPU44	L33	
AF4	+VDD_CORE45	+VTT_CPU45	L34	
AF7	+VDD_CORE46	+VTT_CPU46	M31	
AH23	+VDD_CORE47	+VTT_CPU47	M32	
AF9	+VDD_CORE48	+VTT_CPU48	M33	
AA20	+VDD_CORE49	+VTT_CPU49	N31	
AG11	+VDD_CORE50	+VTT_CPU50	P32	
AG12	+VDD_CORE51	+VTT_CPU51	Y32	
AG21	+VDD_CORE52	+VTT_CPU52	AA32	
AG23	+VDD_CORE53			
AG25	+VDD_CORE54	+VTT_CPUCLK	AG32	43 mA
AG3	+VDD_CORE55			
AG4	+VDD_CORE56			
AA21	+VDD_CORE57			=PP3V3_S0_MCP 8 21 24
AG6	+VDD_CORE58	+3.3V_1	AD10	450 mA (A01)
AG7	+VDD_CORE59	+3.3V_2	AE8	
AG8	+VDD_CORE60	+3.3V_3	AB10	
AG9	+VDD_CORE61	+3.3V_4	AD9	
AH1	+VDD_CORE62	+3.3V_5	Y10	
AH10	+VDD_CORE63	+3.3V_6	AB11	
AH11	+VDD_CORE64	+3.3V_7	AA8	
W26	+VDD_CORE65	+3.3V_8	Y9	
AH2	+VDD_CORE66			
AA23	+VDD_CORE67			
W28	+VDD_CORE68			
AH25	+VDD_CORE69			=PP3V3_S5_MCP 8 24
AH21	+VDD_CORE70	+3.3V_DUAL1	G18	16 mA 266 mA (A01)
AH3	+VDD_CORE71	+3.3V_DUAL2	H19	
AH4	+VDD_CORE72	+3.3V_DUAL3	J20	
AH5	+VDD_CORE73	+3.3V_DUAL4	K20	
AH6	+VDD_CORE74			
AH7	+VDD_CORE75	+3.3V_DUAL_USB1	G26	250 mA
AH9	+VDD_CORE76	+3.3V_DUAL_USB2	H27	
AA24	+VDD_CORE77	+3.3V_DUAL_USB3	J28	
W21	+VDD_CORE78	+3.3V_DUAL_USB4	K28	
W23	+VDD_CORE79			
W25	+VDD_CORE80			
AF12	+VDD_CORE81			
		+VDD_AUXC1	T21	=PP1V05_S5_MCP_VDD_AUXC 8 24
		+VDD_AUXC2	U21	105 mA (A01)
A20	+VBAT	+VDD_AUXC3	V21	

26 21 PP3V3_G3_RTC
10 uA (G3)
80 uA (S0)

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC MASTER=T18_MLB	SYNC DATE=12/12/2008
PAGE TITLE	MCP Power & Ground
Apple Inc.	DRAWING NUMBER 051-7892 SIZE D
	REVISION C.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH
	PAGE 22 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

PAGE TITLE
MCP79 A01 Silicon Support

Apple Inc.

DRAWING NUMBER 051-7892
SIZE D
REVISION C.0.0
BRANCH
PAGE 24 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

MCP Core Power
=PPVCORE_S0_MCP
23065 mA (A01, 1.2V)
16996 mA (A01, 1.0V)
(No IG vs. EG data)
NV: 1x 10uF 0805, 2x 4.7uF 0402, 3x 1uF 0402, 9x 0.1uF 0402 (23.3 uF)
Apple: 4x 4.7uF 0402, 4x 1uF 0402, 6x 0.1uF 0402 (23.4 uF)
C2500 4.7UF 20% 25V X5R 402
C2501 4.7UF 20% 25V X5R 402
C2502 4.7UF 20% 25V X5R 402
C2503 4.7UF 20% 25V X5R 402
C2504 1UF 20% 10V X5R 402-1
C2505 1UF 20% 10V X5R 402-1
C2506 1UF 20% 10V X5R 402-1
C2507 1UF 20% 10V X5R 402-1
C2508 0.1UF 20% 10V CERM 402
C2509 0.1UF 20% 10V CERM 402
C2510 0.1UF 20% 10V CERM 402
C2511 0.1UF 20% 10V CERM 402
C2512 0.1UF 20% 10V CERM 402
C2513 0.1UF 20% 10V CERM 402

MCP PCIE (DVDD) Power
=PP1V05_S0_MCP_PEX_DVDD
57 mA (A01)
C2515 4.7UF 20% 25V X5R 402
C2516 1UF 20% 10V X5R 402-1
C2517 1UF 20% 10V X5R 402-1
C2518 0.1UF 20% 10V CERM 402
C2519 0.1UF 20% 10V CERM 402

MCP SATA (DVDD) Power
=PP1V05_S0_MCP_SATA_DVDD
43 mA (A01)
C2520 4.7UF 20% 25V X5R 402
C2521 0.1UF 20% 10V CERM 402

MCP 1.05V AUX Power
=PP1V05_S5_MCP_VDD_AUXC
105 mA (A01)
C2525 0.1UF 20% 10V CERM 402
C2526 0.1UF 20% 10V CERM 402

MCP 1.05V RMGT Power
=PP1V05_ENET_MCP_RMGT
131 mA (A01)
C2528 4.7UF 20% 25V X5R 402
C2529 0.1UF 20% 10V CERM 402

MCP FSB (VTT) Power
=PP1V05_S0_MCP_FSB
1182 mA (A01)
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 7x 2.2uF 0402 (15.4 uF)
C2530 2.2UF 20% 6.3V CERM 402-LF
C2531 2.2UF 20% 6.3V CERM 402-LF
C2532 2.2UF 20% 6.3V CERM 402-LF
C2533 2.2UF 20% 6.3V CERM 402-LF
C2534 2.2UF 20% 6.3V CERM 402-LF
C2535 2.2UF 20% 6.3V CERM 402-LF
C2536 2.2UF 20% 6.3V CERM 402-LF

MCP Memory Power
=PP1V8R1V5_S0_MCP_MEM
4771 mA (A01, DDR3)
C2540 4.7UF 20% 2V X5R 402
C2541 0.1UF 20% 10V CERM 402
C2542 0.1UF 20% 10V CERM 402
C2543 0.1UF 20% 10V CERM 402
C2544 0.1UF 20% 10V CERM 402
C2545 0.1UF 20% 10V CERM 402
C2546 0.1UF 20% 10V CERM 402
C2547 0.1UF 20% 10V CERM 402
C2548 0.1UF 20% 10V CERM 402
C2549 0.1UF 20% 10V CERM 402

MCP 3.3V Power
=PP3V3_S0_MCP
450 mA (A01)
NV: 1x 4.7uF 0603, 4x 0.1uF 0402 (5.1 uF)
Apple: 4x 2.2uF 0402 (8.8 uF)
C2550 2.2UF 20% 6.3V CERM 402-LF
C2551 2.2UF 20% 6.3V CERM 402-LF
C2552 2.2UF 20% 6.3V CERM 402-LF
C2553 2.2UF 20% 6.3V CERM 402-LF

=PP3V3_S0_MCP_PLL_UF
19 mA (A01)
L2555 30-OHM-1.7A 0402
PP3V3_S0_MCP_PLL_USB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
19 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2555 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V AUX/USB Power
=PP3V3_S5_MCP
266 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2560 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V Ethernet Power
=PP3V3_ENET_MCP_RMGT
83 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2564 2.2UF 20% 6.3V CERM 402-LF

MCP 3.3V/1.5V HDA Power
=PP3V3R1V5_S0_MCP_HDA
7 mA (A01)
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)
C2562 2.2UF 20% 6.3V CERM 402-LF

MCP79 Ethernet VRef
=PP3V3_ENET_MCP_RMGT
R2591 1.47K 1% 1/16W MF-LF 402
R2590 1.47K 1% 1/16W MF-LF 402
MCP_MII_VREF (OUT)
C2591 0.1UF 20% 10V CERM 402

=PP1V05_ENET_MCP_PLL_MAC
5 mA (A01)
L2595 30-OHM-1.7A 0402
PP1V05_ENET_MCP_PLL_MAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
5 mA (A01)
C2595 4.7UF 20% 2V X5R 402
C2596 0.1UF 20% 10V CERM 402

=PP1V05_S0_MCP_AVDD_UF
333 mA (A01)
L2570 30-OHM-5A 0603
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 1uF 0402, 2x 0.1uF 0402 (16.9 uF)
Apple: 5x 2.2uF 0402 (11 uF)
PP1V05_S0_MCP_PEX_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
206 mA (A01)
C2570 2.2UF 20% 6.3V CERM 402-LF
C2571 2.2UF 20% 6.3V CERM 402-LF
C2572 2.2UF 20% 6.3V CERM 402-LF
C2573 2.2UF 20% 6.3V CERM 402-LF
C2574 2.2UF 20% 6.3V CERM 402-LF

L2575 30-OHM-5A 0603
NV: 1x 10uF 0805, 1x 4.7uF 0402, 2x 0.1uF 0402 (14.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)
PP1V05_S0_MCP_SATA_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
127 mA (A01)
C2575 2.2UF 20% 6.3V CERM 402-LF
C2576 2.2UF 20% 6.3V CERM 402-LF

=PP1V05_S0_MCP_PLL_UF
562 mA (A01)
L2580 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_FSB
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
270 mA (A01)
C2580 4.7UF 20% 2V X5R 402
C2581 0.1UF 20% 10V CERM 402

L2582 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_PEX
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)
C2582 4.7UF 20% 2V X5R 402
C2583 0.1UF 20% 10V CERM 402

L2584 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_SATA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
84 mA (A01)
C2584 4.7UF 20% 2V X5R 402
C2585 0.1UF 20% 10V CERM 402

L2586 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_CORE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
87 mA (A01)
C2586 4.7UF 20% 2V X5R 402
C2587 0.1UF 20% 10V CERM 402

L2588 30-OHM-1.7A 0402
PP1V05_S0_MCP_PLL_NV
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
37 mA (A01)
C2588 4.7UF 20% 2V X5R 402
C2589 0.1UF 20% 10V CERM 402
C2590 0.1UF 20% 10V CERM 402

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

SYNC_MASTER=T18_MLB
SYNC_DATE=06/18/2008
PAGE TITLE
MCP Standard Decoupling
Apple Inc.
DRAWING NUMBER 051-7892
SIZE D
REVISION C.0.0
BRANCH
PAGE 25 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.

NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: 1x 2.2uF 0402 (2.2 uF)

18 8 =PP3V3R1V8_S0_MCP_IFP_VDD
190 mA (A01, 1.8V)

C2610
2.2UF
20%
6.3V
CERM
402-LF

18 8 =PP1V05_S0_MCP_HDMI_VDD
95 mA (A01)

C2615
4.7UF
20%
4V
X5R
402

C2616
2.2UF
20%
6.3V
CERM
402-LF

90 18 MCP_HDMI_RSET
90 18 MCP_HDMI_VPROBE

NO STUFF
C2620
0.1UF
10%
10V
CERM
402

R2620
1K
1%
1/10W
MF-LF
402

90 18 MCP_IFPAB_RSET
90 18 MCP_IFPAB_VPROBE

NO STUFF
C2630
0.1UF
10%
10V
CERM
402

NO STUFF
R2630
1K
1%
1/10W
MF-LF
402

WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
Apple: ???

8 =PP3V3_S0_MCP_VPLL_UF
16 mA (A01)

L2640
30-OHM-1.7A
0402

PP3V3_S0_MCP_VPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18
16 mA (A01)

C2640
4.7UF
20%
6.3V
CERM
603

C2641
0.1UF
10%
10V
CERM
402

NV: 1x 4.7uF 0603, 2x 0.1uF 0402 (4.9 uF)
Apple: 2x 2.2uF 0402 (4.4 uF)

PP3V3_S0_MCP_DAC
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
18
206 mA (A01)

R2651
0
5%
1/10W
MF-LF
402

18 TP_MCP_RGB_RED — NC_MCP_RGB_RED
18 TP_MCP_RGB_GREEN — NC_MCP_RGB_GREEN
18 TP_MCP_RGB_BLUE — NC_MCP_RGB_BLUE
18 TP_MCP_RGB_HSYNC — NC_MCP_RGB_HSYNC
18 TP_MCP_RGB_VSYNC — NC_MCP_RGB_VSYNC
90 18 CRT_IG_R_C_PR — NC_CRT_IG_R_C_PR
90 18 CRT_IG_G_Y_Y — NC_CRT_IG_G_Y_Y
90 18 CRT_IG_B_COMP_PB — NC_CRT_IG_B_COMP_PB
90 18 CRT_IG_HSYNC — NC_CRT_IG_HSYNC
90 18 CRT_IG_VSYNC — NC_CRT_IG_VSYNC
18 TP_MCP_RGB_DAC_RSET — NC_MCP_RGB_DAC_RSET
18 TP_MCP_RGB_DAC_VREF — NC_MCP_RGB_DAC_VREF
90 18 MCP_TV_DAC_RSET — NC_MCP_TV_DAC_RSET
90 18 MCP_TV_DAC_VREF — NC_MCP_TV_DAC_VREF
18 MCP_CLK27M_XTALIN — NC_MCP_CLK27M_XTALIN
18 MCP_CLK27M_XTALOUT — NC_MCP_CLK27M_XTALOUT

MAKE_BASE=TRUE NO_TEST=TRUE

Current numbers from email Xiaowei Lin provided 11/12/2007 3:22pm (no official document number).

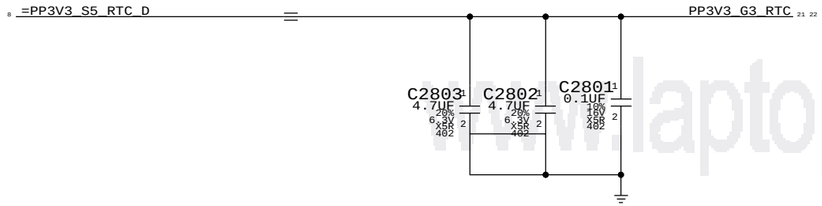
SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

PAGE TITLE: MCP Graphics Support

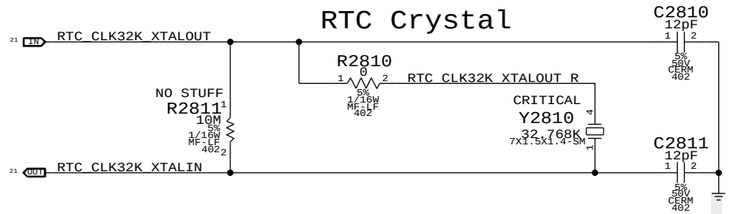
Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 26 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

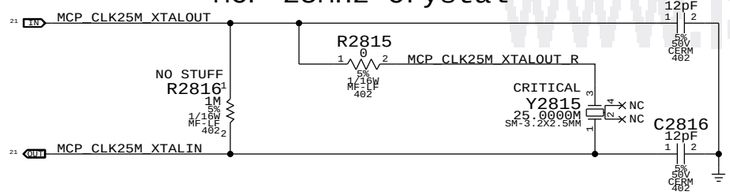
RTC Power Sources



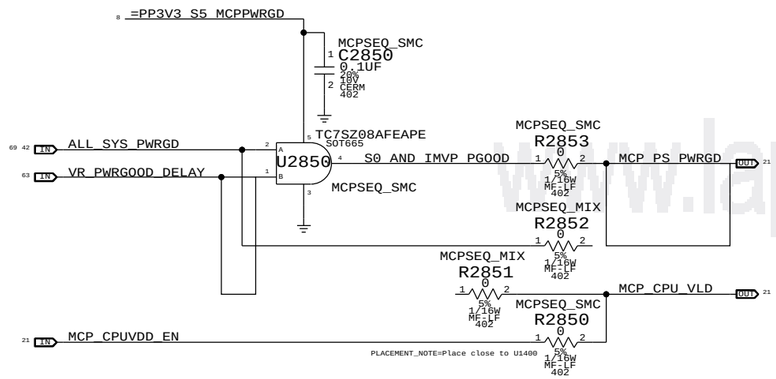
RTC Crystal



MCP 25MHz Crystal



MCP S0 PWRGD & CPU_VLD



MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up.

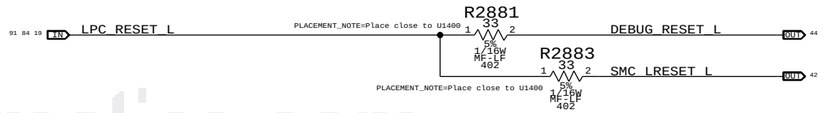
MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization.

SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).

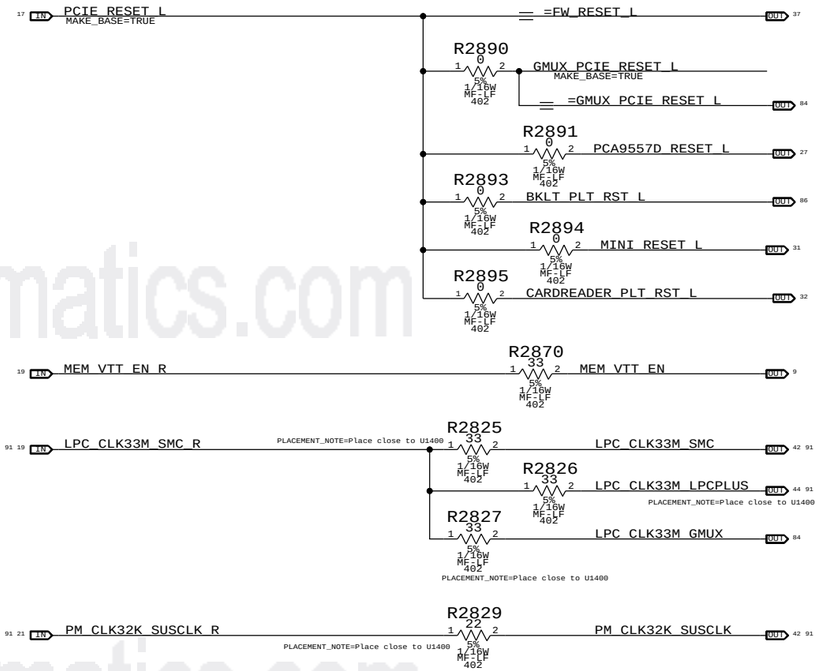
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Platform Reset Connections

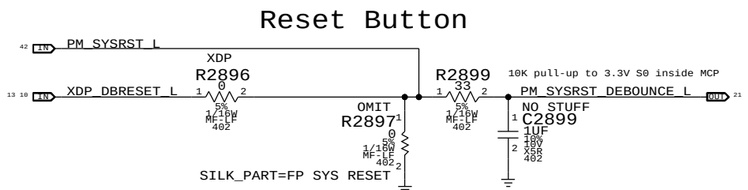
LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SYNC_MASTER=DDR	SYNC_DATE=12/15/2008
PAGE TITLE	SB Misc
Apple Inc.	DRAWING NUMBER 051-7892 SIZE D
	REVISION C.0.0
	BRANCH
	PAGE 28 OF 109
	SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PP3V3_S5_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN
NO_VREFMRGN

DAC channel	MEM A VREF DQ A	MEM A VREF CA B	MEM B VREF DQ A	MEM B VREF CA B	CPU FSB VREF C	FRAME BUFFER VREF D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately
(i.e. not simultaneously) due to current limitation of TPS51116 regulator.

=PP3V3_S3_VREFMRGN

=PPVTT_S3_DDR_BUF
10mA max load

VREFMRGN C2900 2.2UF 20% 6.3V CERM 402-LF
VREFMRGN C2901 0.1UF 20% 10V CERM 402
VREFMRGN C2902 0.1UF 20% 10V CERM 402
VREFMRGN C2903 0.1UF 20% 10V CERM 402
VREFMRGN C2904 0.1UF 20% 10V CERM 402
VREFMRGN C2905 0.1UF 20% 10V CERM 402

U2900 DAC5574 MSOP
VDD, SCL, SDA, A0, A1, GND
VOUTA VREFMRGN_DQ_SODIMM
VOUTB VREFMRGN_CA_SODIMM
VOUTC VREFMRGN_CPUFSB
VOUTD VREFMRGN_FRAMEBUF

=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA
ADDR=0x98(WR)/0x99(RD)

U2901 PCA9557 QFN
ADDR=0x30(WR)/0x31(RD)
A0, A1, A2, SCL, SDA, RESET*, VCC, THRM PAD, GND
P0 NC
P1 VREFMRGN_CPUFSB_EN
P2 VREFMRGN_CA_SODIMMA_EN
P3 VREFMRGN_DQ_SODIMMA_EN
P4 VREFMRGN_CA_SODIMMB_EN
P5 VREFMRGN_DQ_SODIMMB_EN
P6 VREFMRGN_FRAMEBUF_EN
P7 NC
RESET* PCA9557D_RESET_L

U2902 MAX4253 UCSP
VREFMRGN_DQ_SODIMMA_BUF
VREFMRGN_DQ_SODIMMA_EN
VREFMRGN_DQ_SODIMMB_BUF
VREFMRGN_DQ_SODIMMB_EN

U2903 MAX4253 UCSP
VREFMRGN_CA_SODIMMA_BUF
VREFMRGN_CA_SODIMMA_EN
VREFMRGN_CA_SODIMMB_BUF
VREFMRGN_CA_SODIMMB_EN

U2904 MAX4253 UCSP
VREFMRGN_FRAMEBUF_BUF
VREFMRGN_FRAMEBUF_EN
VREFMRGN_CPUFSB_BUF
VREFMRGN_CPUFSB_EN

R2901 100K 5% 1/16W MF-LF 402
R2902 100K 5% 1/16W MF-LF 402
R2907 100K 5% 1/16W MF-LF 402
R2908 100K 5% 1/16W MF-LF 402
R2913 100K 5% 1/16W MF-LF 402
R2915 100K 5% 1/16W MF-LF 402

R2903 200 1% 1/10W MF-LF 402 VREFMRGN → PP0V75_S3_MEM_VREFDQ_A
R2904 100 1% 1/10W MF-LF 402 VREFMRGN Place close to J3100.1
R2905 200 1% 1/10W MF-LF 402 VREFMRGN → PP0V75_S3_MEM_VREFDQ_B
R2906 100 1% 1/10W MF-LF 402 VREFMRGN Place close to J3200.1
R2909 200 1% 1/10W MF-LF 402 VREFMRGN → PP0V75_S3_MEM_VREFCA_A
R2910 100 1% 1/10W MF-LF 402 VREFMRGN Place close to J3100.126
R2911 200 1% 1/10W MF-LF 402 VREFMRGN → PP0V75_S3_MEM_VREFCA_B
R2912 100 1% 1/10W MF-LF 402 VREFMRGN Place close to J3200.126
R2916 49.9 1% 1/10W MF-LF 402 VREFMRGN → GPU_FB_A_VREF_DIV
R2917 49.9 1% 1/10W MF-LF 402 VREFMRGN → GPU_FB_B_VREF_DIV
R2914 100 1% 1/10W MF-LF 402 VREFMRGN → CPU_GTLREF
Place close to U8400, U8450
Place close to U8500, U8550
Place close to U1000.AD26

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES,MTL FILM,0,5%,0402,SM,LF	R2911	CRITICAL	NO_VREFMRGN

SYNC_MASTER=DDR SYNC_DATE=12/05/2008

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 29 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_A
8 =PP1V5_S3_MEM_A

C3100 10UF 20% 6.3V CERM 603
C3101 10UF 20% 6.3V CERM 603
C3110 0.1UF 10% 16V CERM 402
C3111 0.1UF 10% 16V CERM 402
C3112 0.1UF 10% 16V CERM 402
C3113 0.1UF 10% 16V CERM 402
C3114 0.1UF 10% 16V CERM 402
C3115 0.1UF 10% 16V CERM 402
C3116 0.1UF 10% 16V CERM 402
C3117 0.1UF 10% 16V CERM 402
C3118 0.1UF 10% 16V CERM 402
C3119 0.1UF 10% 16V CERM 402
C3120 0.1UF 10% 16V CERM 402
C3121 0.1UF 10% 16V CERM 402
C3122 0.1UF 10% 16V CERM 402
C3123 0.1UF 10% 16V CERM 402

27 PP0V75_S3_MEM_VREFDQ_A

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 10% 16V CERM 402

J3100 (DDR3-SODIMM-DUAL-M97-3, SYMBOL 2 OF 2)

MEM_A_CKE<0>	73 CKE0	74 CKE1	MEM_A_CKE<1>
	75 VDD	76 VDD	
	77 NC	78 A15	MEM_A_A<15>
MEM_A_BA<2>	79 BA2	80 A14	MEM_A_A<14>
	81 VDD	82 VDD	
MEM_A_A<12>	83 A12/BC*	84 A11	MEM_A_A<11>
MEM_A_A<9>	85 A9	86 A7	MEM_A_A<7>
	87 VDD	88 VDD	
MEM_A_A<8>	89 A8	90 A6	MEM_A_A<6>
MEM_A_A<5>	91 A5	92 A4	MEM_A_A<4>
	93 VDD	94 VDD	
MEM_A_A<3>	95 A3	96 A2	MEM_A_A<2>
MEM_A_A<1>	97 A1	98 A0	MEM_A_A<0>
	99 VDD	100 VDD	
MEM_A_CLK_P<0>	101 CK0	102 CK1	MEM_A_CLK_P<1>
MEM_A_CLK_N<0>	103 CK0*	104 CK1*	MEM_A_CLK_N<1>
	105 VDD	106 VDD	
MEM_A_A<10>	107 A10/AP	108 BA1	MEM_A_BA<1>
MEM_A_BA<0>	109 BA0	110 RAS*	MEM_A_RAS_L
	111 VDD	112 VDD	
MEM_A_WE_L	113 WE*	114 S0*	MEM_A_CS_L<0>
MEM_A_CAS_L	115 CAS*	116 ODT0	MEM_A_ODT<0>
	117 VDD	118 VDD	
MEM_A_A<13>	119 A13	120 ODT1	MEM_A_ODT<1>
MEM_A_CS_L<1>	121 S1*	122 NC	
	123 VDD	124 VDD	
	125 TEST	126 VREFCA	
	127 VSS	128 VSS	
MEM_A_DQ<33>	129 DQ32	130 DQ36	MEM_A_DQ<36>
MEM_A_DQ<32>	131 DQ33	132 DQ37	MEM_A_DQ<37>
	133 VSS	134 VSS	
MEM_A_DQS_N<4>	135 DQS4*	136 DM4	MEM_A_DM<4>
MEM_A_DQS_P<4>	137 DQS4	138 VSS	
	139 VSS	140 DQ38	MEM_A_DQ<38>
MEM_A_DQ<34>	141 DQ34	142 DQ39	MEM_A_DQ<39>
MEM_A_DQ<35>	143 DQ35	144 VSS	
	145 VSS	146 DQ44	MEM_A_DQ<47>
MEM_A_DQ<44>	147 DQ40	148 DQ45	MEM_A_DQ<40>
MEM_A_DQ<41>	149 DQ41	150 VSS	
	151 VSS	152 DQS5*	MEM_A_DQS_N<5>
MEM_A_DM<5>	153 DM5	154 DQS5	MEM_A_DQS_P<5>
	155 VSS	156 VSS	
MEM_A_DQ<45>	157 DQ42	158 DQ46	MEM_A_DQ<46>
MEM_A_DQ<42>	159 DQ43	160 DQ47	MEM_A_DQ<43>
	161 VSS	162 VSS	
MEM_A_DQ<52>	163 DQ48	164 DQ52	MEM_A_DQ<48>
MEM_A_DQ<51>	165 DQ49	166 DQ53	MEM_A_DQ<53>
	167 VSS	168 VSS	
MEM_A_DQS_N<6>	169 DQS6*	170 DM6	MEM_A_DM<6>
MEM_A_DQS_P<6>	171 DQS6	172 VSS	
	173 VSS	174 DQ54	MEM_A_DQ<50>
MEM_A_DQ<55>	175 DQ50	176 DQ55	MEM_A_DQ<49>
MEM_A_DQ<54>	177 DQ51	178 VSS	
	179 VSS	180 DQ60	MEM_A_DQ<57>
MEM_A_DQ<61>	181 DQ56	182 DQ61	MEM_A_DQ<56>
MEM_A_DQ<60>	183 DQ57	184 VSS	
	185 VSS	186 DQS7*	MEM_A_DQS_N<7>
MEM_A_DM<7>	187 DM7	188 DQS7	MEM_A_DQS_P<7>
	189 VSS	190 VSS	
MEM_A_DQ<58>	191 DQ58	192 DQ62	MEM_A_DQ<62>
MEM_A_DQ<59>	193 DQ59	194 DQ63	MEM_A_DQ<63>
	195 VSS	196 VSS	
MEM_A_SA<0>	197 SA0	198 EVENT*	MEM_EVENT_L (OUT 21 29 42)
	199 VDDSPD	200 SDA	=I2C_SODIMMA_SDA (BI 45)
MEM_A_SA<1>	201 SA1	202 SCL	=I2C_SODIMMA_SCL (IN 45)
	203 VTT	204 VTT	

KEY
516-0196
SPD ADDR=0xA0(WR)/0xA1(RD)

J3100 (DDR3-SODIMM-DUAL-M97-3, SYMBOL 1 OF 2) — CRITICAL

	1 VREFDQ	2 VSS	
	3 VSS	4 DQ4	MEM_A_DQ<4>
MEM_A_DQ<0>	5 DQ0	6 DQ5	MEM_A_DQ<5>
MEM_A_DQ<1>	7 DQ1	8 VSS	
	9 VSS	10 DQS0*	MEM_A_DQS_N<0>
MEM_A_DM<0>	11 DM0	12 DQS0	MEM_A_DQS_P<0>
	13 VSS	14 VSS	
MEM_A_DQ<3>	15 DQ2	16 DQ6	MEM_A_DQ<6>
MEM_A_DQ<2>	17 DQ3	18 DQ7	MEM_A_DQ<7>
	19 VSS	20 VSS	
MEM_A_DQ<9>	21 DQ8	22 DQ12	MEM_A_DQ<8>
MEM_A_DQ<13>	23 DQ9	24 DQ13	MEM_A_DQ<12>
	25 VSS	26 VSS	
MEM_A_DQS_N<1>	27 DQS1*	28 DM1	MEM_A_DM<1>
MEM_A_DQS_P<1>	29 DQS1	30 RESET*	MEM_RESET_L (IN 29 30)
	31 VSS	32 VSS	
MEM_A_DQ<11>	33 DQ10	34 DQ14	MEM_A_DQ<15>
MEM_A_DQ<14>	35 DQ11	36 DQ15	MEM_A_DQ<10>
	37 VSS	38 VSS	
MEM_A_DQ<16>	39 DQ16	40 DQ20	MEM_A_DQ<21>
MEM_A_DQ<18>	41 DQ17	42 DQ21	MEM_A_DQ<20>
	43 VSS	44 VSS	
MEM_A_DQS_N<2>	45 DQS2*	46 DM2	MEM_A_DM<2>
MEM_A_DQS_P<2>	47 DQS2	48 VSS	
	49 VSS	50 DQ22	MEM_A_DQ<17>
MEM_A_DQ<23>	51 DQ18	52 DQ23	MEM_A_DQ<22>
MEM_A_DQ<19>	53 DQ19	54 VSS	
	55 VSS	56 DQ28	MEM_A_DQ<29>
MEM_A_DQ<24>	57 DQ24	58 DQ29	MEM_A_DQ<28>
MEM_A_DQ<30>	59 DQ25	60 VSS	
	61 VSS	62 DQS3*	MEM_A_DQS_N<3>
MEM_A_DM<3>	63 DM3	64 DQS3	MEM_A_DQS_P<3>
	65 VSS	66 VSS	
MEM_A_DQ<27>	67 DQ26	68 DQ30	MEM_A_DQ<26>
MEM_A_DQ<25>	69 DQ27	70 DQ31	MEM_A_DQ<31>
	71 VSS	72 VSS	

KEY
516-0196

PP0V75_S3_MEM_VREFCA_A 27

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 10% 16V CERM 402

8 =PPSPD_S0_MEM_A

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF 402
R3141 10K 5% 1/16W MF 402

8 =PP0V75_S0_MEM_VTT_A

"Factory" (top) slot

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

PAGE TITLE: DDR3 SO-DIMM Connector A

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 31 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)

8 =PP1V5_S0_MEM_B
8 =PP1V5_S3_MEM_B

C3210 C3211 C3212 C3213 C3214 C3215 C3216 C3217 C3218 C3219 C3220 C3221 C3222 C3223
0.1UF 10% 10V CERM 402

C3200 C3201
10UF 20% 6.3V X5R 603

27 PP0V75_S3_MEM_VREFDQ_B

C3230
2.2UF 20% 6.3V CERM 402-LF

C3231
0.1UF 10% 10V CERM 402

J3200 DDR3-SODIMM (2 OF 2) F-RT-BGA3

89 15 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 15 89
		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 9
89 15 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 15 89
		81	VDD	VDD	82		
89 15 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 15 89
89 15 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 15 89
		87	VDD	VDD	88		
89 15 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 15 89
89 15 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 15 89
		93	VDD	VDD	94		
89 15 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 15 89
89 15 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 15 89
		99	VDD	VDD	100		
89 15 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 15 89
89 15 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 15 89
		105	VDD	VDD	106		
89 15 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 15 89
89 15 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 15 89
		111	VDD	VDD	112		
89 15 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 15 89
89 15 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 15 89
		117	VDD	VDD	118		
89 15 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 15 89
89 15 IN	MEM_B_CS_L<1>	121	S1*	NC	122		
		123	VDD	VDD	124		
		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
89 15 B1	MEM_B_DQ<32>	129	DQ32	DQ36	130	MEM_B_DQ<33>	B1 15 89
89 15 B1	MEM_B_DQ<37>	131	DQ33	DQ37	132	MEM_B_DQ<36>	B1 15 89
		133	VSS	VSS	134		
89 15 B1	MEM_B_DQS_N<4>	135	DQS4*	DM4	136	MEM_B_DM<4>	IN 15 89
89 15 B1	MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	MEM_B_DQ<38>	B1 15 89
89 15 B1	MEM_B_DQ<34>	141	DQ34	DQ39	142	MEM_B_DQ<39>	B1 15 89
89 15 B1	MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	MEM_B_DQ<44>	B1 15 89
89 15 B1	MEM_B_DQ<41>	147	DQ40	DQ45	148	MEM_B_DQ<45>	B1 15 89
89 15 B1	MEM_B_DQ<40>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	MEM_B_DQS_N<5>	B1 15 89
89 15 IN	MEM_B_DM<5>	153	DM5	DQS5	154	MEM_B_DQS_P<5>	B1 15 89
		155	VSS	VSS	156		
89 15 B1	MEM_B_DQ<43>	157	DQ42	DQ46	158	MEM_B_DQ<47>	B1 15 89
89 15 B1	MEM_B_DQ<42>	159	DQ43	DQ47	160	MEM_B_DQ<46>	B1 15 89
		161	VSS	VSS	162		
89 15 B1	MEM_B_DQ<55>	163	DQ48	DQ52	164	MEM_B_DQ<48>	B1 15 89
89 15 B1	MEM_B_DQ<49>	165	DQ49	DQ53	166	MEM_B_DQ<54>	B1 15 89
		167	VSS	VSS	168		
89 15 B1	MEM_B_DQS_N<6>	169	DQS6*	DM6	170	MEM_B_DM<6>	IN 15 89
89 15 B1	MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	MEM_B_DQ<53>	B1 15 89
89 15 B1	MEM_B_DQ<52>	175	DQ50	DQ55	176	MEM_B_DQ<50>	B1 15 89
89 15 B1	MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	MEM_B_DQ<60>	B1 15 89
89 15 B1	MEM_B_DQ<56>	181	DQ56	DQ61	182	MEM_B_DQ<61>	B1 15 89
89 15 B1	MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	MEM_B_DQS_N<7>	B1 15 89
89 15 IN	MEM_B_DM<7>	187	DM7	DQS7	188	MEM_B_DQS_P<7>	B1 15 89
		189	VSS	VSS	190		
89 15 B1	MEM_B_DQ<63>	191	DQ58	DQ62	192	MEM_B_DQ<58>	B1 15 89
89 15 B1	MEM_B_DQ<59>	193	DQ59	DQ63	194	MEM_B_DQ<62>	B1 15 89
		195	VSS	VSS	196		
MEM_B_SA<0>		197	SA0	EVENT*	198	MEM_EVENT_L	OUT 21 28 42
		199	VDDSPD	SDA	200	=I2C_SODIMMB_SDA	B1 45
MEM_B_SA<1>		201	SA1	SCL	202	=I2C_SODIMMB_SCL	IN 45
		203	VTT	VTT	204		
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

MTG PINS

516s0704

SPD ADDR=0xA2(WR)/0xA3(RD)

8 =PPSPD_S0_MEM_B

R3240 10K 5% 1/16W MF-LF 402

C3240 2.2UF 20% 6.3V CERM 402-LF

R3241 10K 5% 1/16W MF-LF 402

8 =PP0V75_S0_MEM_VTT_B

PP0V75_S3_MEM_VREFCA_B 27

C3235 2.2UF 20% 6.3V CERM 402-LF

C3236 0.1UF 10% 10V CERM 402

J3200 DDR3-SODIMM (1 OF 2) F-RT-BGA3 CRITICAL

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	MEM_B_DQ<4>	B1 15 89
89 15 B1	MEM_B_DQ<0>	5	DQ0	DQ5	6	MEM_B_DQ<5>	B1 15 89
89 15 B1	MEM_B_DQ<1>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_B_DQS_N<0>	B1 15 89
89 15 IN	MEM_B_DM<0>	11	DM0	DQS0	12	MEM_B_DQS_P<0>	B1 15 89
		13	VSS	VSS	14		
89 15 B1	MEM_B_DQ<2>	15	DQ2	DQ6	16	MEM_B_DQ<6>	B1 15 89
89 15 B1	MEM_B_DQ<3>	17	DQ3	DQ7	18	MEM_B_DQ<7>	B1 15 89
		19	VSS	VSS	20		
89 15 B1	MEM_B_DQ<28>	21	DQ8	DQ12	22	MEM_B_DQ<29>	B1 15 89
89 15 B1	MEM_B_DQ<24>	23	DQ9	DQ13	24	MEM_B_DQ<25>	B1 15 89
		25	VSS	VSS	26		
89 15 B1	MEM_B_DQS_N<3>	27	DQS1*	DM1	28	MEM_B_DM<3>	IN 15 89
89 15 B1	MEM_B_DQS_P<3>	29	DQS1	RESET*	30	MEM_RESET_L	IN 28 30
		31	VSS	VSS	32		
89 15 B1	MEM_B_DQ<31>	33	DQ10	DQ14	34	MEM_B_DQ<26>	B1 15 89
89 15 B1	MEM_B_DQ<30>	35	DQ11	DQ15	36	MEM_B_DQ<27>	B1 15 89
		37	VSS	VSS	38		
89 15 B1	MEM_B_DQ<9>	39	DQ16	DQ20	40	MEM_B_DQ<13>	B1 15 89
89 15 B1	MEM_B_DQ<8>	41	DQ17	DQ21	42	MEM_B_DQ<12>	B1 15 89
		43	VSS	VSS	44		
89 15 B1	MEM_B_DQS_N<1>	45	DQS2*	DM2	46	MEM_B_DM<1>	IN 15 89
89 15 B1	MEM_B_DQS_P<1>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	MEM_B_DQ<14>	B1 15 89
89 15 B1	MEM_B_DQ<15>	51	DQ18	DQ23	52	MEM_B_DQ<11>	B1 15 89
89 15 B1	MEM_B_DQ<10>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	MEM_B_DQ<20>	B1 15 89
89 15 B1	MEM_B_DQ<21>	57	DQ24	DQ29	58	MEM_B_DQ<16>	B1 15 89
89 15 B1	MEM_B_DQ<17>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	MEM_B_DQS_N<2>	B1 15 89
89 15 IN	MEM_B_DM<2>	63	DM3	DQS3	64	MEM_B_DQS_P<2>	B1 15 89
		65	VSS	VSS	66		
89 15 B1	MEM_B_DQ<18>	67	DQ26	DQ30	68	MEM_B_DQ<19>	B1 15 89
89 15 B1	MEM_B_DQ<22>	69	DQ27	DQ31	70	MEM_B_DQ<23>	B1 15 89
		71	VSS	VSS	72		

516s0704

"Expansion" (bottom) slot

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

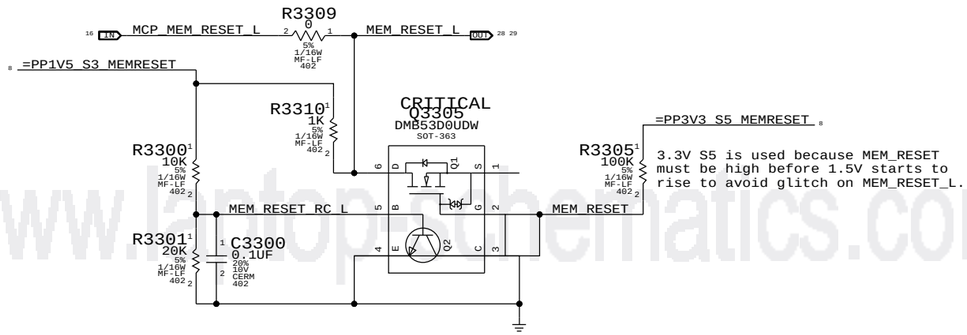
PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 32 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

DDR3 RESET Support

Required becaues MCP79 does not meet DDR3 spec power-up reset timing requirement.



SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE: DDR3 Support

Apple Inc.

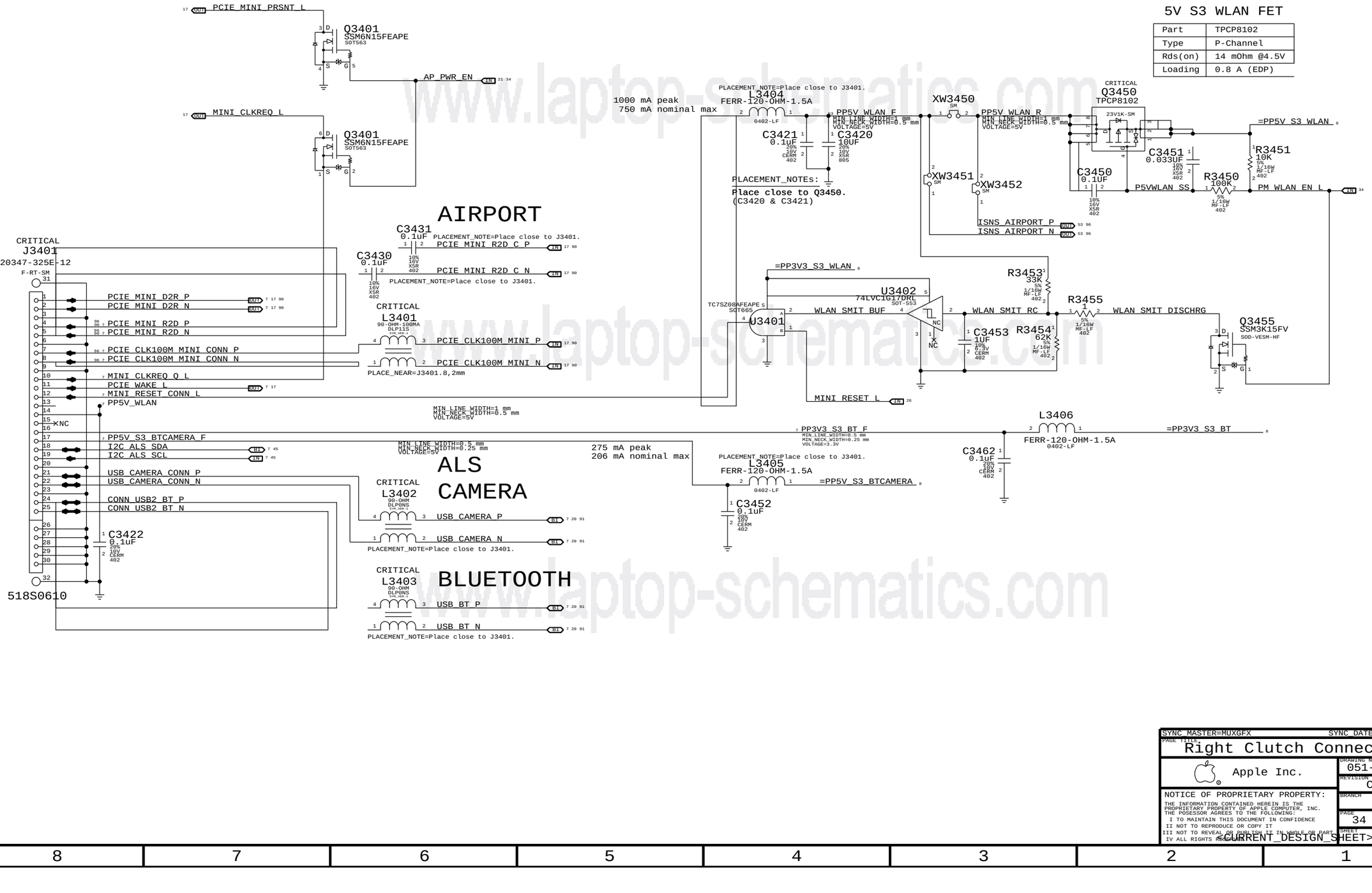
DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 33 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



5V S3 WLAN FET

Part	TPCP8102
Type	P-Channel
Rds(on)	14 mOhm @4.5V
Loading	0.8 A (EDP)

SYNC_MASTER=MUXGFX SYNC_DATE=12/08/2008

PAGE TITLE: Right Clutch Connector

Apple Inc.

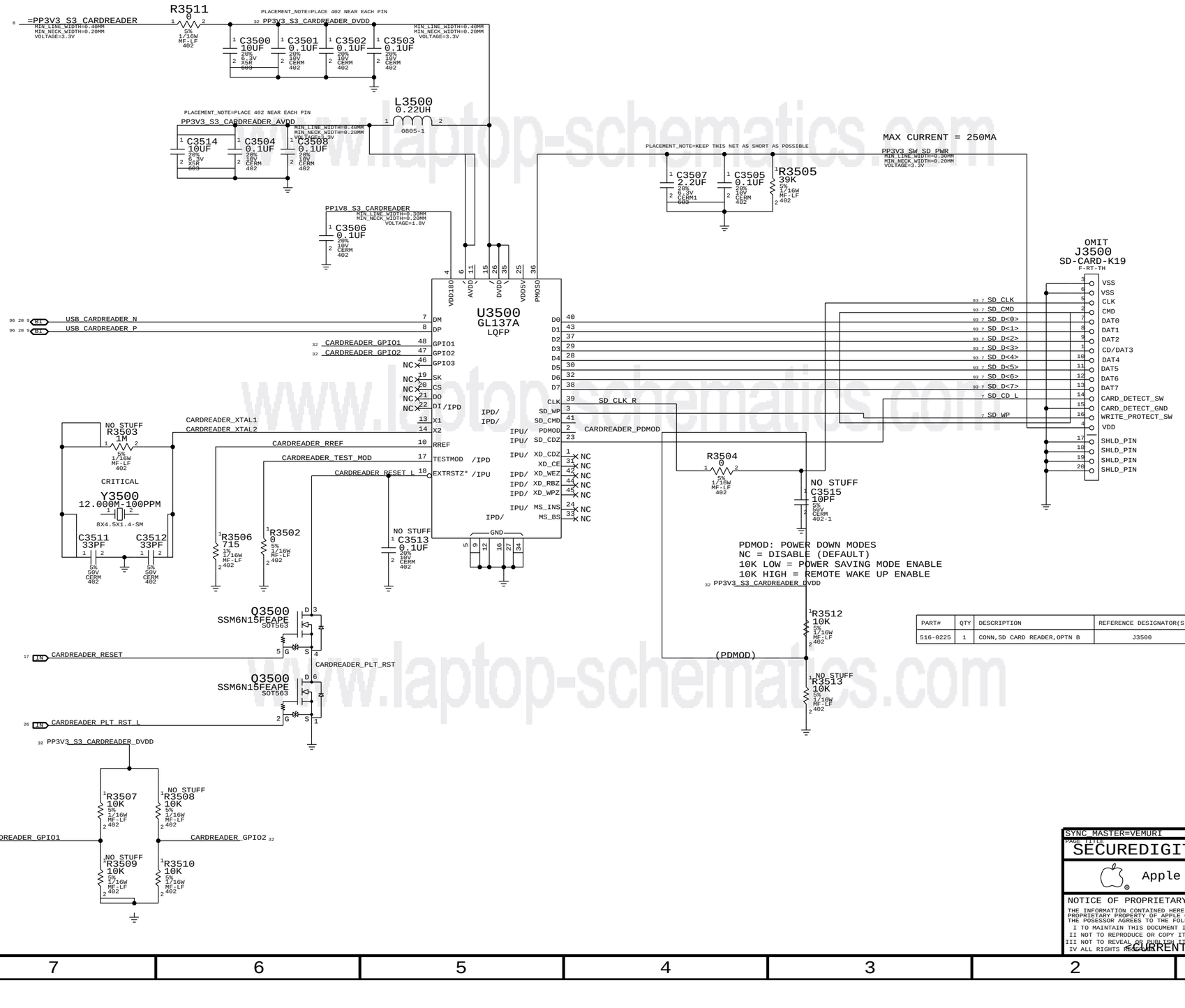
DRAWING NUMBER 051-7892 SIZE D

REVISION C.0.0

BRANCH

PAGE 34 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516-0225	1	CONN,SD CARD READER,OPTN B	J3500	CRITICAL	

SYNC_MASTER=VEMURI SYNC_DATE=01/30/2009

PAGE TITLE

SECUREDIGITAL CARD READER

Apple Inc.

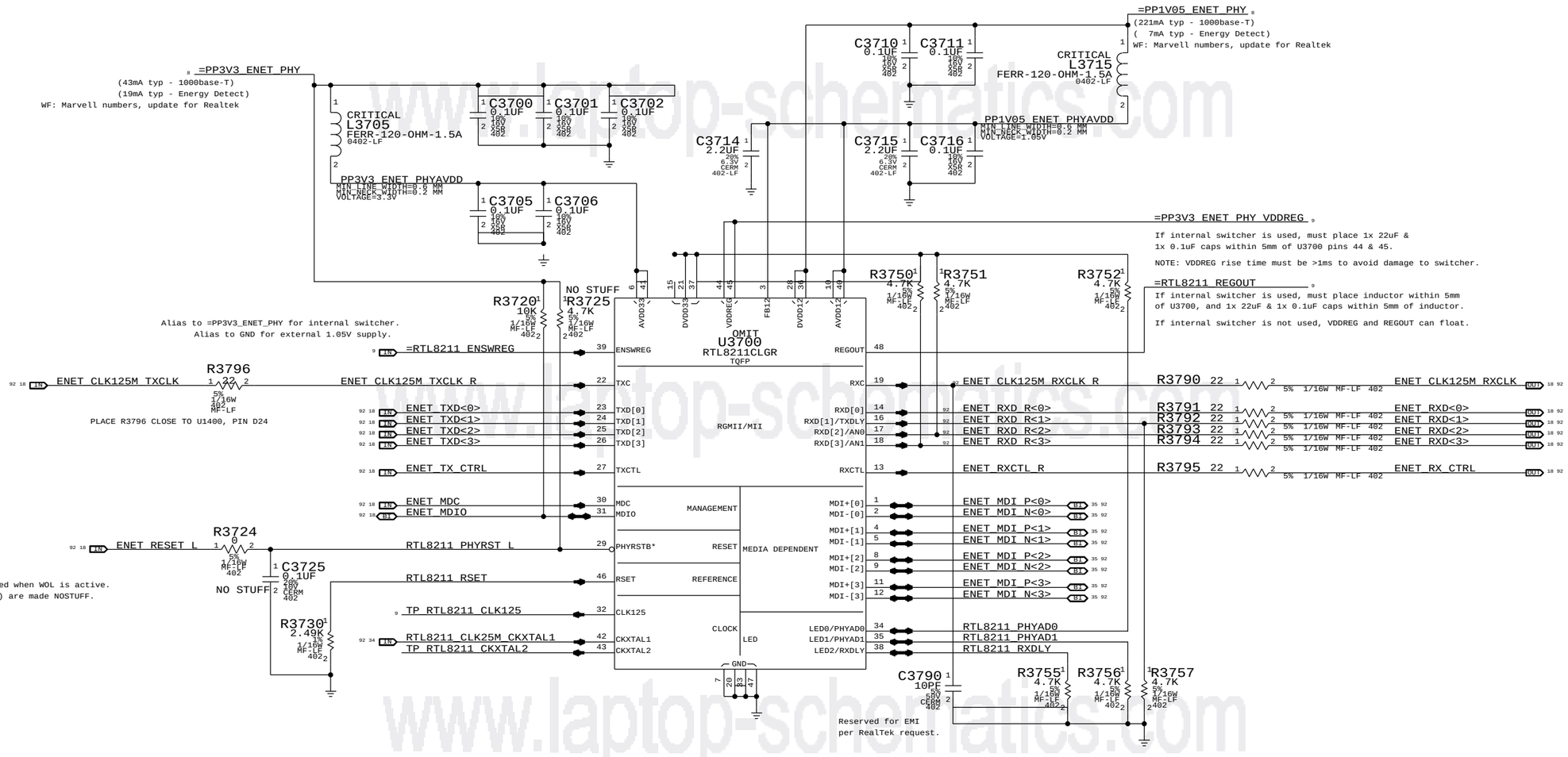
DRAWING NUMBER 051-7892 SIZE D

REVISION C.0.0

BRANCH

PAGE 35 OF 109

SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



Configuration Settings:

PHYAD = 01 (PHY Address 00001)
AN[1:0] = 11 (Full auto-negotiation)
RXDLY = 0 (RXCLK transitions with data)
TXDLY = 0 (No TXCLK Delay)

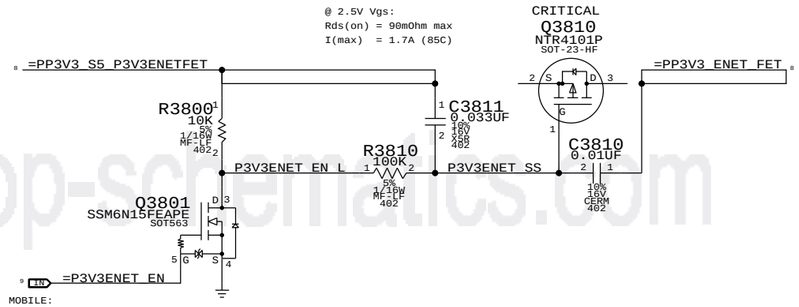
SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

PAGE TITLE: Ethernet PHY (RTL8211CL)

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 37 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

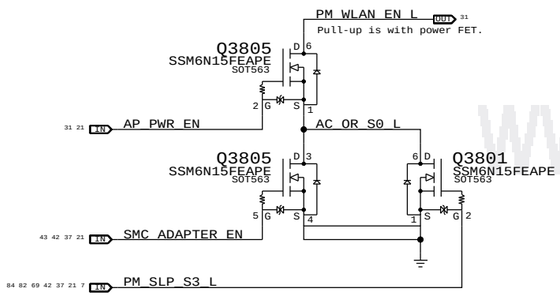
3.3V ENET FET



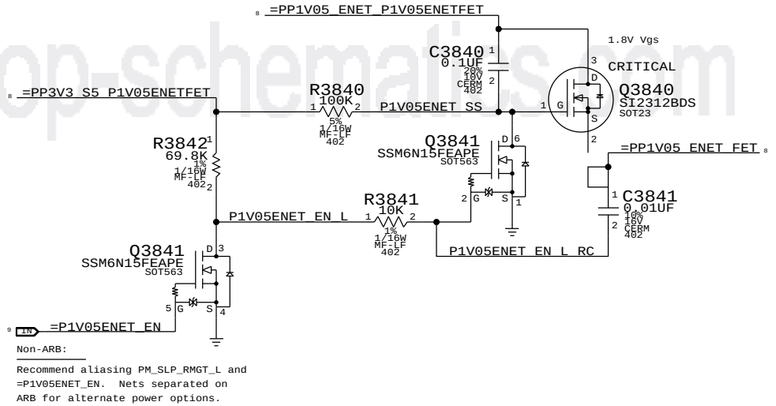
WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



1.05V ENET FET



RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered.
Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/07/2008

PAGE TITLE: Ethernet & AirPort Support

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 38 OF 109

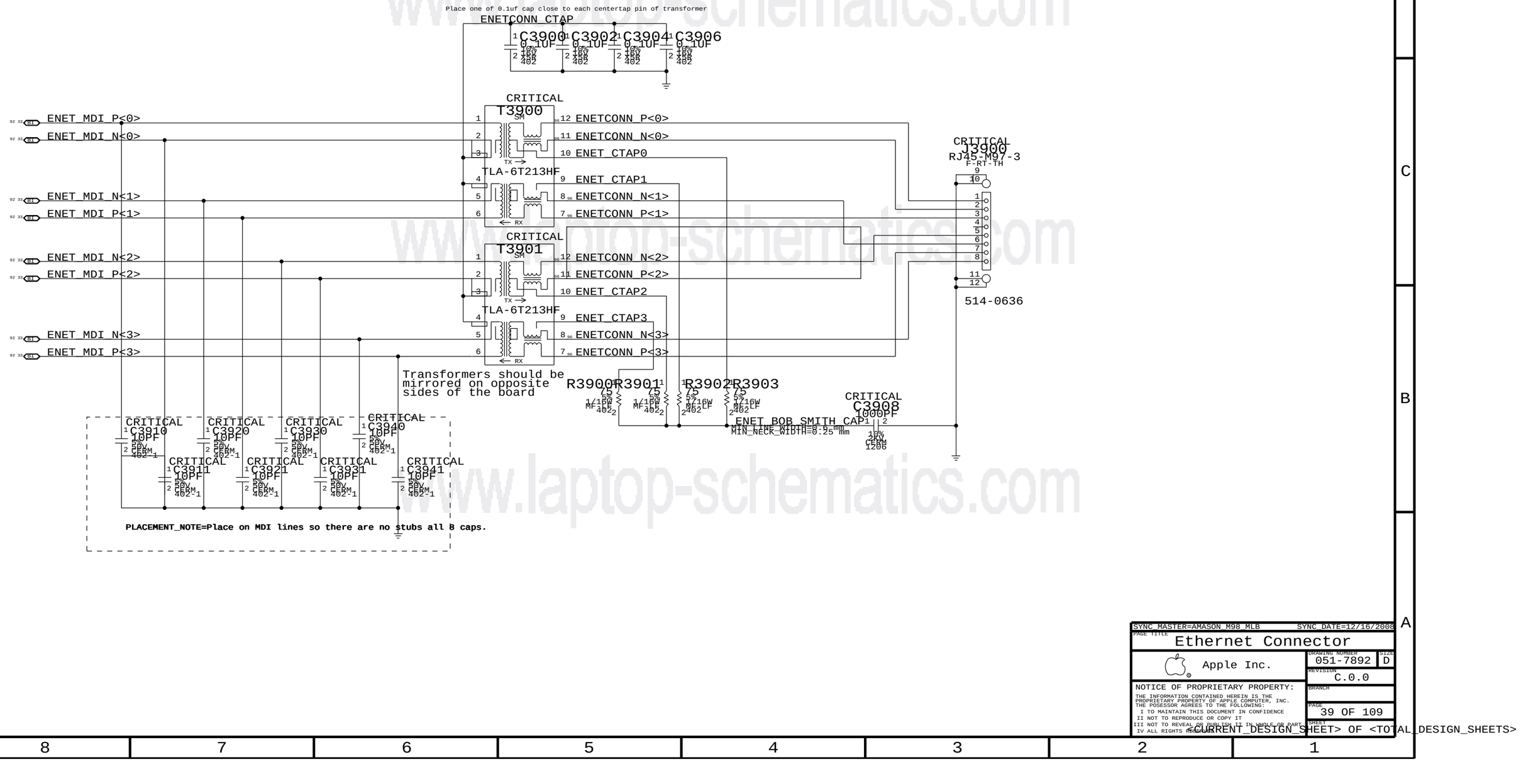
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/16/2008

PAGE TITLE: Ethernet Connector

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 39 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0557	1	RES,0.475 ohm,1%,1/16W,0402	R4100	CRITICAL	

OMIT
R4100
0.2
1%
1/16W
MF-LF
402

=PP1V0_FW_FWPHY
135 mA
PP1V0_FW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

L4110
120-OHM-0.3A-EMI
0402-LF
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V

25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402

110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402

7 mA I/O
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402

=PP3V3_FW_FWPHY
138 mA

L4130
120-OHM-0.3A-EMI
0402-LF

114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402

L4135
120-OHM-0.3A-EMI
0402-LF

17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402

0 mA VReg PWR
C4141 0.1UF 20% 16V CERM 402
C4140 1UF 10% 6.3V CERM 402

VDD10 VDD33 VDDH VP VP25 VREG_PWR

OMIT
CRITICAL
U4100
FW643
BGA

NC ATBUSB
NC ATBUSH
NC ATBUSN

=FW_PHY_DS0 → DS0 (IPD) NT-19
=FW_PHY_DS1 → DS1 (IPD) NT-20
=FW_PHY_DS2 → DS2 (IPD) NT-21

FW_P0_TPA_N → TPA0N
FW_P0_TPA_P → TPA0P
FW_P1_TPA_N → TPA1N
FW_P1_TPA_P → TPA1P
FW_P2_TPA_N → TPA2N
FW_P2_TPA_P → TPA2P
FW_P0_TPB_N → TPB0N
FW_P0_TPB_P → TPB0P
FW_P1_TPB_N → TPB1N
FW_P1_TPB_P → TPB1P
FW_P2_TPB_N → TPB2N
FW_P2_TPB_P → TPB2P

FW_P0_TPBIAS → TPBIAS0
FW_P1_TPBIAS → TPBIAS1
FW_P2_TPBIAS → TPBIAS2

FW643_R0 → R0
FW643_TPCPS → TPCPS

TP_FW643_NAND_TREE → NAND_TREE NT-OUT
FW643_REXT → REXT
FW_CLK24P576M_XO_R → XO
FW_CLK24P576M_XI → XI NT-9

NOTE: NT-xx notes show NAND tree order.

TP_FW643_SE → SE (IPD)
TP_FW643_SM → SM (IPD)
TP_FW643_MODE_A → MODE_A (IPD) NT-18
TP_FW643_CE → CE (IPD)
TP_FW643_FW620_L → FW620*(IPU)
TP_FW643_JASI_EN → JASI_EN (IPD) NT-11
TP_FW643_AVREG → AVREG
TP_FW643_VBUF → VBUF
FW643_PU_RST_L → FW_RESET* (IPU) NT-8
TP_FW643_OCR10_CTL → OCR_CTL_V10
NC OCR_CTL_V12 (Reserved)

VSS VREG_VSS

=PPVP_FW_PHY_CPS
R4160 200K 1% 1/16W MF-LF 402
R4161 2.94K 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402

C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
R4150 412 1% 1/16W MF-LF 402
CRITICAL
Y4150
24.576MHZ
SM-3.2X2.5MM
NC
NC

PCI EXPRESS PHY
PCIE_RXD0N → PCIE_FW_R2D_N
PCIE_RXD0P → PCIE_FW_R2D_P
PCIE_TXD0N → PCIE_FW_D2R_C_N
PCIE_TXD0P → PCIE_FW_D2R_C_P
REFCLKN → PCIE_CLK100M_FW_N
REFCLKP → PCIE_CLK100M_FW_P

PLACEMENT_NOTE=Place C4170 close to U1400
PLACEMENT_NOTE=Place C4171 close to U1400
C4170 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_N
C4171 0.1UF 10% 16V X5R 402 PCIE_FW_R2D_C_P
C4175 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_N
C4176 0.1UF 10% 16V X5R 402 PCIE_FW_D2R_P
PLACEMENT_NOTE=Place C4175 close to U4000
PLACEMENT_NOTE=Place C4176 close to U4000

1394 PHY

TEST CONTROLLER
NT-4 (IPU) TCK → TP_FW643_TCK
NT-3 (IPU) TDI → TP_FW643_TDI
(IPU) TDO → TP_FW643_TDO
NT-1 (IPU) TMS → TP_FW643_TMS
NT-2 (IPU) TRST* → FW643_TRST_L

POWER MANAGEMENT
FIXME!!! - TYPO IN SYMBOL REGCTL
NT-10 (IPD) WAKE* → =FW_PME_L
REGCLT → FW643_REGCTL
VAUX_DETECT → FW643_VAUX_DETECT
NT-12 (IPD) VAUX_DISABLE → TP_FW643_VAUX_ENABLE
NT-13 (OD) CLKREQN → =FW_CLKREQ_L

SCIF
NT-16 (IPD) SCIFCLK → TP_FW643_SCIFCLK
NT-14 (IPD) SCIFDAIN → TP_FW643_SCIFDAIN
NT-17 SCIFDOUT → TP_FW643_SCIFDOUT
NT-15 (IPD) SCIFMC → TP_FW643_SCIFMC

SERIAL EEPROM CONTROLLER
NT-7 SCL → FW643_SCL
NT-6 SDA → TP_FW643_SDA

MISCELLANEOUS
CHIP RESET
NT-5 PERST* → FW_RESET_L

=PP3V3_FW_FWPHY
FW643_LDO
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
R4163 10K 5% 1/16W MF-LF 402

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008
PAGE TITLE
FireWire LLC/PHY (FW643)
Apple Inc.
DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 41 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (system supply for bus power)
- =PP3V3_FW_LATEVG_ACTIVE
- =PPVP_FW_SUMNODE (power passthru summation node)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

3.3V FW FET

@ 2.5V Vgs:
Rds(on) = 90mOhm max
I(max) = 1.7A (85C)

=PP3V3_S0_P3V3FWFET
R4290 10K 5% 1/16W MF-LF 402
C4290 0.033UF 10% 16V X5R 402
CRITICAL Q4291 NTR4101P SOT-23-HF
=PP3V3_FW_FET
P3V3FW_EN_L
R4291 100K 5% 1/16W MF-LF 402
P3V3FW_SS
C4291 0.01UF 10% 16V CERM 402
Q4290 SSM6N15FEAPE SOT563
FW_PWR_EN

1.05V FW FET

=PP1V05_FW_P1V05FWFET
C4296 0.1UF 20% 10V CERM 402
=PP3V3_S0_P1V05FWFET
R4297 220K 5% 1/16W MF-LF 402
CRITICAL Q4295 SI2312BDS SOT23
P1V05FW_SS
Q4293 SSM6N15FEAPE SOT563
=PP1V0_FW_FET
NOSTUFF C4295 0.068UF 10% 16V CERM 402
=PP3V3_S5_P1V05FWFET
R4295 10K 5% 1/16W MF-LF 402
R4296 100K 5% 1/16W MF-LF 402
P1V05_FW_EN_L
P1V05_FW_EN_L_RC
Q4293 SSM6N15FEAPE SOT563
FW_PWR_EN

=PP3V3_FW_FWPHY
R4277 10K 5% 1/16W MF-LF 402
R4276 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
FW_WAKE
NOSTUFF C4276 0.1UF 10% 16V X5R 402
CRITICAL Q4276 DMB53D0UV SOT-563
=FW_PME_L
CRITICAL Q4276 DMB53D0UV SOT-563

PCIE_FW_PRSNT
MAKE_BASE=TRUE
Q4264 SSM6N15FEAPE SOT563
FW_CLKREQ_L
Q4264 SSM6N15FEAPE SOT563
FW_PWR_EN
=FW_CLKREQ_L
FW_CLKREQ_PHY_L
MAKE_BASE=TRUE

=PP3V3_S0_FWPWRCTL
R4281 100K 5% 1/16W MF-LF 402
R4280 10K 1% 1/16W MF-LF 402
=PP1V0_FW_FWPHY
C4281 1UF 10% 10V X5R 402
P1V0_FW_RC
CRITICAL Q4299 DMB53D0UV SOT-563
P1V0_RESET_GATE
R4283 10K 5% 1/16W MF-LF 402
=FW_RESET_L
CRITICAL Q4299 DMB53D0UV SOT-563
FW_RESET_L
PP1V05_FW PGOOD/FW_RESET_L

FireWire Port Power Switch

=PPBUS_S5_FWPWRSW
CRITICAL Q4260 NDS9407 SOI-HF
PPBUS_FW_FWPWRSW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL F4260 1.1A-24V MINISMDC110H24
PPBUS_FW_FWPWRSW_D
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL D4260 SM CRS08-1.5A-30V
=PPBUS_S5_FW_FET

Late-VG Event Detection

CRITICAL Q4262 DMB54D0UV SOT-563
R4265 10K 5% 1/16W MF-LF 402
LATEVG_FAULT_EVENT_PNP
NOSTUFF R4263 100 1% 1/16W MF-LF 402
LATEVG_FAULT_EVENT
LATEVG_RETRY_RC
NOSTUFF C4263 1UF 10% 10V X5R 402-1
R4260 470K 5% 1/16W MF-LF 402
C4260 0.1UF 10% 25V X5R 402
FWPWR_EN_L_DIV
R4261 330K 5% 1/16W MF-LF 402
FWPWR_EN_L
Q4261 SSM6N15FEAPE SOT563
Q4261 SSM6N15FEAPE SOT563
SMC_ADAPTER_EN
PM_SLP_S3_L
Enables port power when machine is running or on AC.

=PP3V3_FW_LATEVG_ACTIVE
PP2V4_FW_LATEVG
R4211 10K 5% 1/16W MF-LF 402
R4212 10K 1% 1/16W MF-LF 402
C4210 0.1UF 10% 10V CERM 402
U4210 LMC7211 SM-HF
FWLATEGV_3V_REF
P2V4_FWLATEVG_RC
LATEVG_EVENT
C4211 100pF 5% 50V CERM 402
R4213 80.6K 1% 1/16W MF-LF 402
R4210 200K 1% 1/16W MF-LF 402
FWLATEVG Hysteresis:
3.08V when port power is on
2.91V when late Vg event and port power is off

=PP1V05_FWPWRCTL
R4275 1K 5% 1/16W MF-LF 402
R4270 330K 5% 1/16W MF-LF 402
R4271 56K 5% 1/16W MF-LF 402
FW_PWR_EN_L
FW_DET_MIRROR
FW_PLUG_DET
CRITICAL Q4270 BC847CDXV6TXG SOT563
CRITICAL Q4270 BC847CDXV6TXG SOT563
C4270 0.1UF 10% 16V X5R 402
FW_P1_TPBIAS_R
FW_DET_EMIT
R4272 1K 5% 1/16W MF-LF 402
R4273 12K 5% 1/16W MF-LF 402
=PP3V3_S0_FWPWRCTL
R4274 100K 5% 1/16W MF-LF 402
FW_PLUG_DET_L
CRITICAL Q4275 DMB53D0UV SOT-563
CRITICAL Q4275 DMB53D0UV SOT-563
FW_PWR_EN
FW_P1_TPBIAS

SYNC_MASTER=YUN_K19_MLB SYNC_DATE=12/22/2008
PAGE TITLE: FireWire Port Power
Apple Inc.
DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 42 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:

- =PPVP_FW_PORT1
- =PP3V3_FW_LATEVG

- =GND_CHASSIS_FW_PORT1
- =GND_CHASSIS_FW_EMI_R

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

FireWire PHY Config Straps

Configures PHY for:

- 1-port Portable Power Class (0)

- Port "1" Bilingual (1394B)

38 37 36 8 =PP3V3_FW_FWPHY

R4382 10K 1% 1/16W MF-LF 402

R4380 10K 1% 1/16W MF-LF 402

FWPHY_DS0 MAKE_BASE=TRUE = =FW_PHY_DS0 36

FWPHY_DS2 MAKE_BASE=TRUE = =FW_PHY_DS2 36

FWPHY_DS1 MAKE_BASE=TRUE = =FW_PHY_DS1 36

R4381 10K 1% 1/16W MF-LF 402

36 FW_P0_TPBIAS = NC_FW0_TPBIAS MAKE_BASE=TRUE

36 FW_P2_TPBIAS = NC_FW2_TPBIAS MAKE_BASE=TRUE

93 36 FW_P0_TPA_N = NC_FW0_TPAN MAKE_BASE=TRUE

93 36 FW_P0_TPA_P = NC_FW0_TPAP MAKE_BASE=TRUE

36 FW_P2_TPA_N = NC_FW2_TPAN MAKE_BASE=TRUE

36 FW_P2_TPA_P = NC_FW2_TPAP MAKE_BASE=TRUE

93 36 FW_P0_TPB_N = NC_FW0_TPBN MAKE_BASE=TRUE

93 36 FW_P0_TPB_P = NC_FW0_TPBP MAKE_BASE=TRUE

36 FW_P2_TPB_N = NC_FW2_TPBN MAKE_BASE=TRUE

36 FW_P2_TPB_P = NC_FW2_TPBP MAKE_BASE=TRUE

Termination

Place close to FireWire PHY

37 36 FW_P1_TPBIAS

TI PHYs require 1uF even though FW spec calls out 0.33uF

C4360 0.33UF 10% 16V CERM-X5R 402

SIGNAL_MODEL=EMPTY

R4360 56.2 1% 1/16W MF-LF 402

R4361 56.2 1% 1/16W MF-LF 402

93 36 FW_P1_TPA_P MAKE_BASE=TRUE = FW_PORT1_TPA_P 38

93 36 FW_P1_TPA_N MAKE_BASE=TRUE = FW_PORT1_TPA_N 38

93 36 FW_P1_TPB_P MAKE_BASE=TRUE = FW_PORT1_TPB_P 38

93 36 FW_P1_TPB_N MAKE_BASE=TRUE = FW_PORT1_TPB_N 38

SIGNAL_MODEL=EMPTY

R4362 56.2 1% 1/16W MF-LF 402

R4363 56.2 1% 1/16W MF-LF 402

FW_PORT1_TPB_C

C4364 220pF 10% 25V CERM 402

R4364 4.99K 1% 1/16W MF-LF 402

8 =PPVP_FW_PHY_CPS_FET

Q4300 BSS8402DW (SOT-363)

PPVP_FW_CPS MAKE_BASE=TRUE = =PPVP_FW_PHY_CPS 36

MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V

R4311 470K 5% 1/16W MF-LF 402

CPS_EN_L_DIV

R4312 330K 5% 1/16W MF-LF 402

CPS_EN_L

38 37 36 8 =PP3V3_FW_FWPHY

Q4300 BSS8402DW SOT-363 (SYM-VER1)

"Snapback" & "Late VG" Protection

38 37 PP2V4_FW_LATEVG

CRITICAL DP4310 BAV99DW-X-G SOT-363

C4311 0.01uF 10% 16V X7R 402

CRITICAL DP4310 BAV99DW-X-G SOT-363

C4310 0.01uF 10% 16V X7R 402

38 FW_PORT1_TPB_N

38 FW_PORT1_TPB_P

38 FW_PORT1_TPA_N

38 FW_PORT1_TPA_P

CRITICAL DP4311 BAV99DW-X-G SOT-363

C4312 0.01uF 10% 16V X7R 402

C4313 0.01uF 10% 16V X7R 402

CRITICAL DP4311 BAV99DW-X-G SOT-363

C4319 0.1uF 10% 50V X7R 603-1

R4319 1M 5% 1/16W MF-LF 402

PLACEMENT_NOTE=Place C4319 close to connector pin 5.

Cable Power

8 =PPVP_FW_PORT1

CRITICAL L4310 FERR-250-OHM SM

Note: Trace PPVP_FW_PORT1 must handle up to 5A

PPVP_FW_PORT1_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=33V

C4314 0.01UF 10% 50V X7R 402

PORT 1

BILINGUAL

CRITICAL J4310 1394B-M97 F-RT-TH

TPB- TPB(R) TPB
TPB+ TPB(R) TPB
VP VP
NC/NC
VG VG
TPA- TPA(R) TPA
TPA+ TPA(R) TPA
CHASSIS GND

OUTPUT

INPUT

(FW_PORT1_BREF)

(GND_FW_PORT1_VG)

FW_PORT1_AREF

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

514S0605

Late-VG Protection Power

8 =PP3V3_FW_LATEVG

R4390 332 1% 1/16W MF-LF 402

PP2V4_FW_LATEVG 37 38
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.4V

CRITICAL D4390 MMBZ5227BLT1H SOT23

ESD and late-VG rail for snap-back diodes (Common to all ports)

PP2V4_FWLATEVG needs to be biased to at least 2.1V for FW signal integrity and should be biased to 2.4V for margin
R4390 should be 390 Ohms max for a 3.3V rail

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

PAGE TITLE: FireWire Ports

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 43 OF 109

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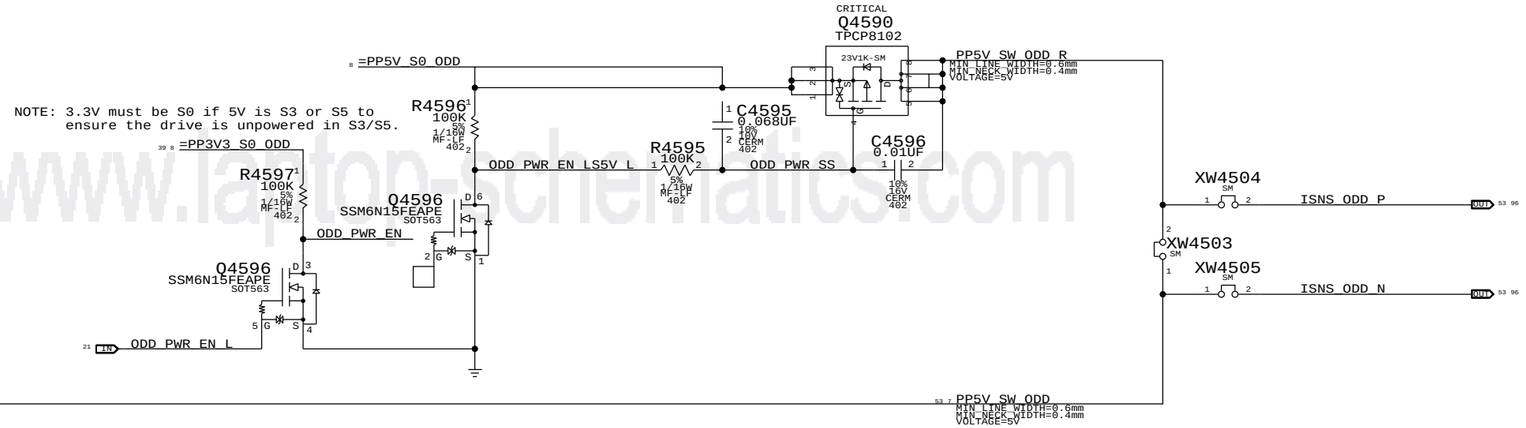
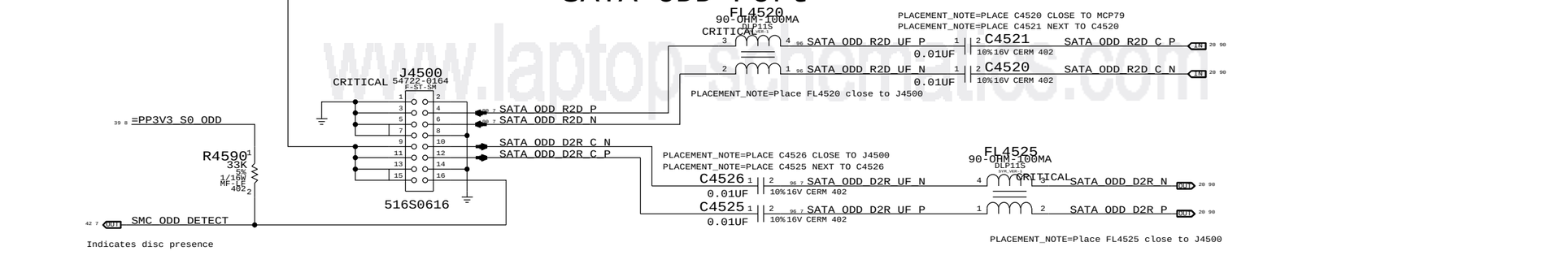
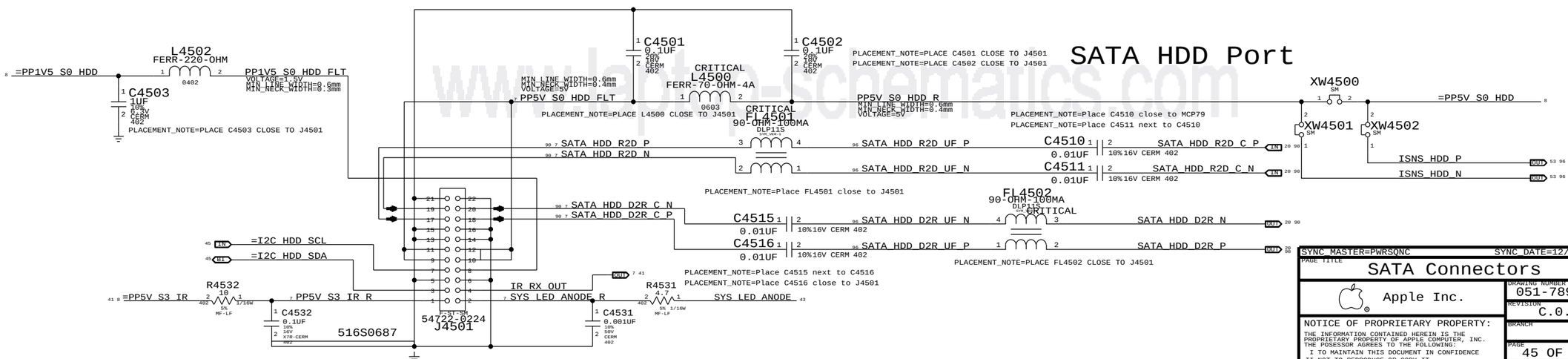
ODD Power Control



SATA ODD Port



SATA HDD Port



SYNC MASTER=PWRSQNC SYNC DATE=12/04/2008

PAGE TITLE

SATA Connectors

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D

REVISION C.0.0

BRANCH

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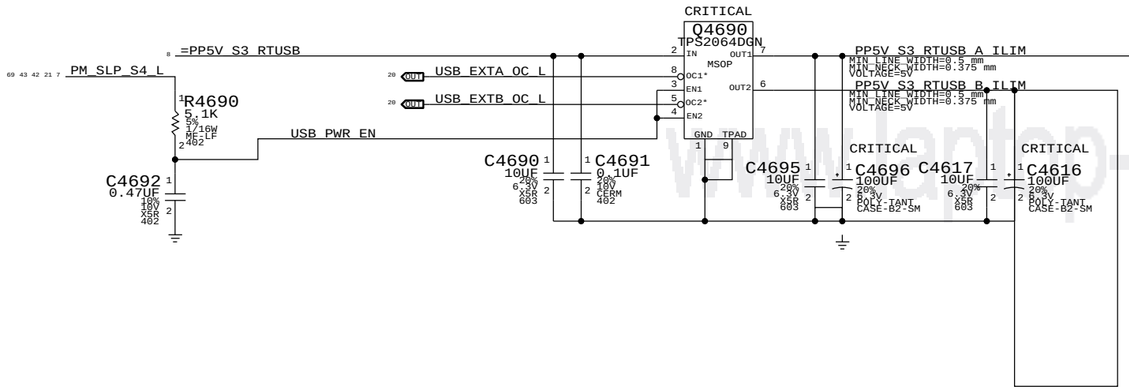
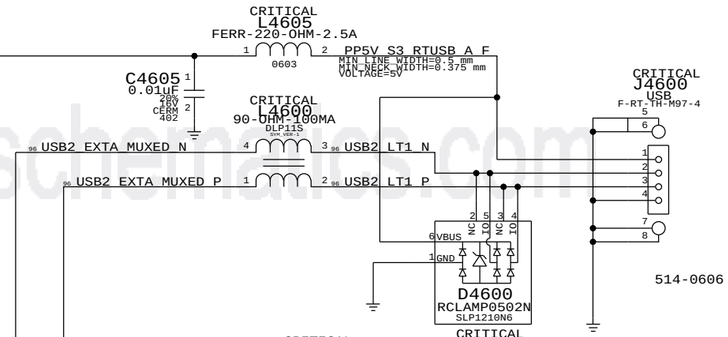
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

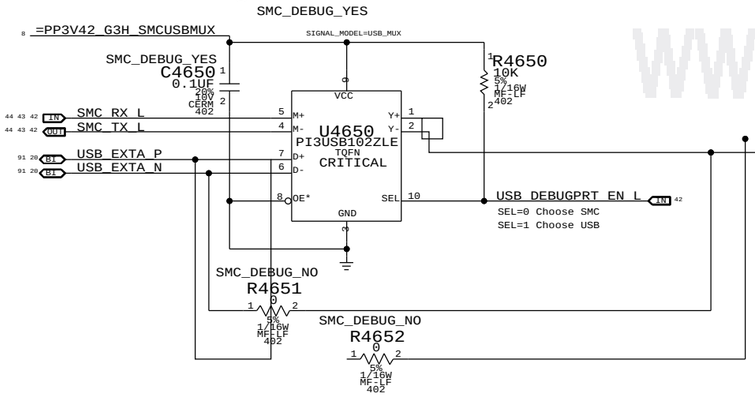
Port Power Switch



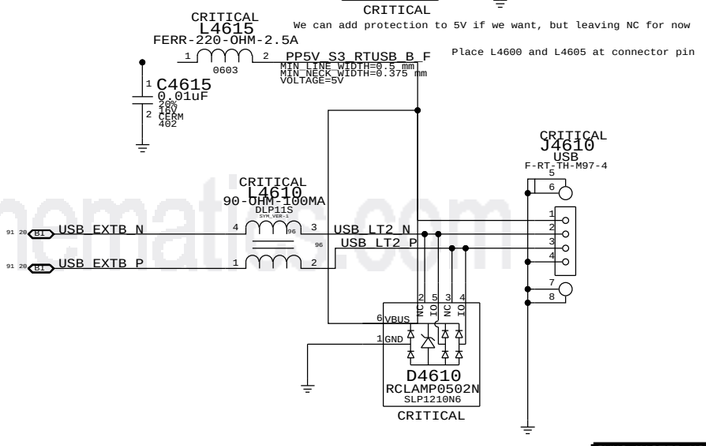
Left USB Port A



USB/SMC Debug Mux

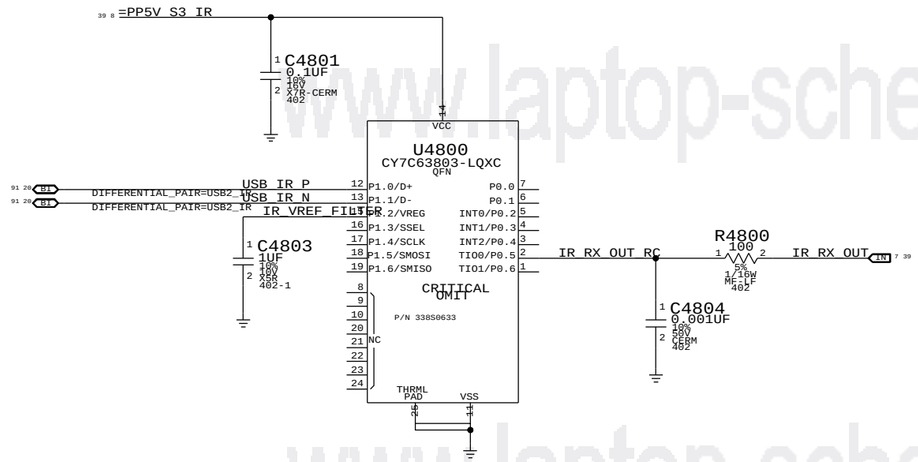


Left USB Port B



SYNC_MASTER=M98_MLB	SYNC_DATE=11/14/2008
PAGE TITLE: External USB Connectors	
Apple Inc.	DRAWING NUMBER: 051-7892 · SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 46 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

IR SUPPORT



SYNC_MASTER=PWRSONC SYNC_DATE=12/04/2008

PAGE TITLE
Front Flex Support

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D

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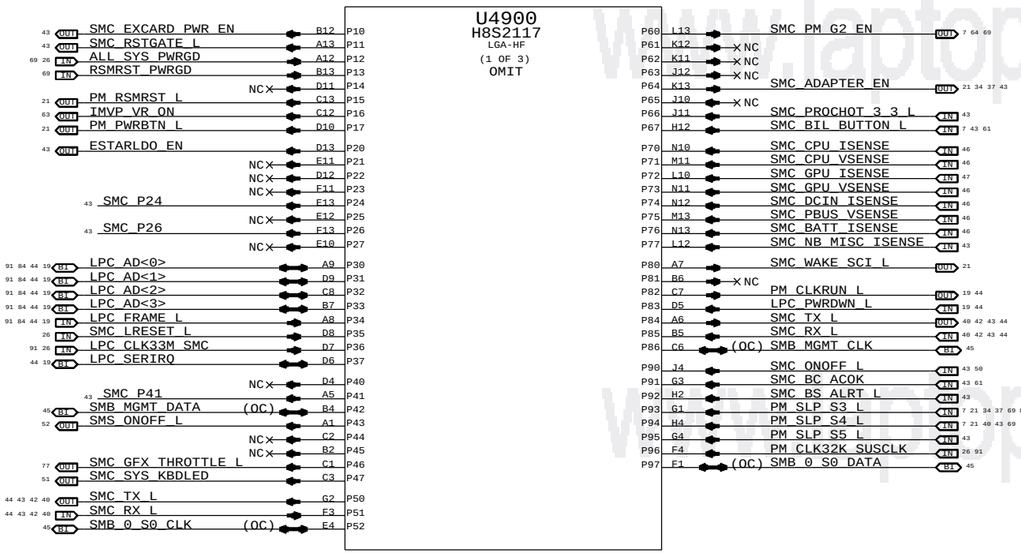
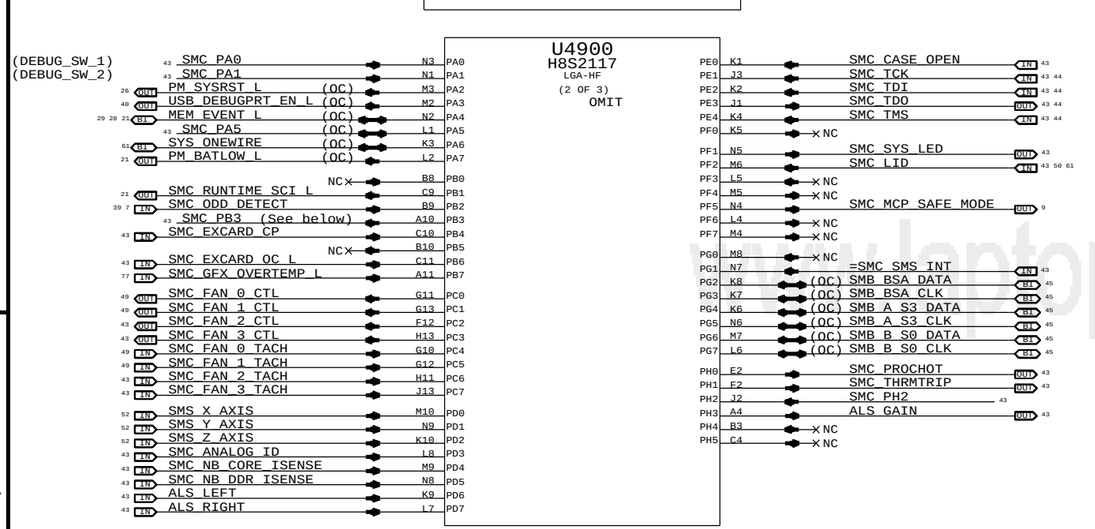
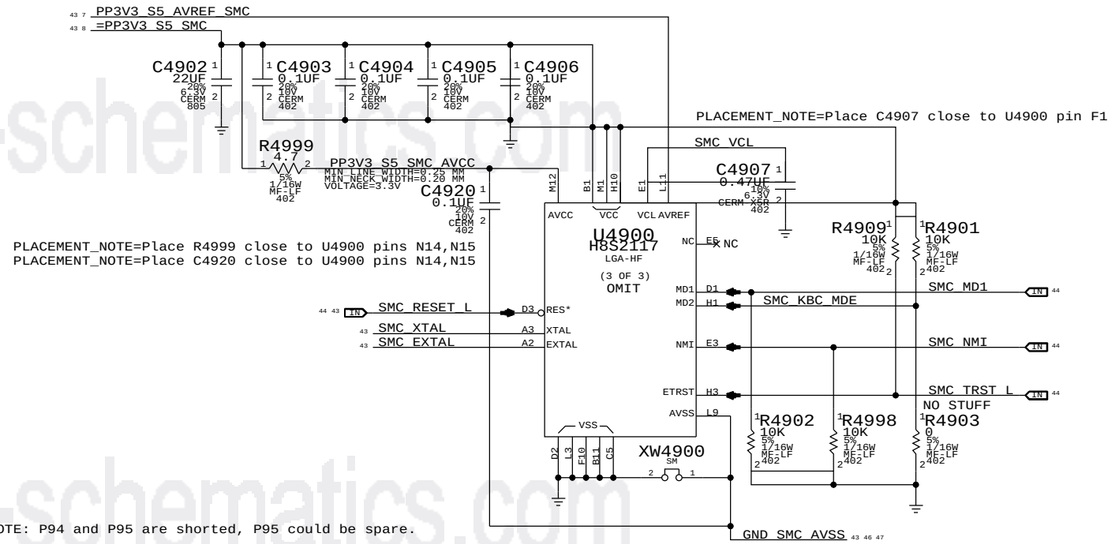
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2008

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
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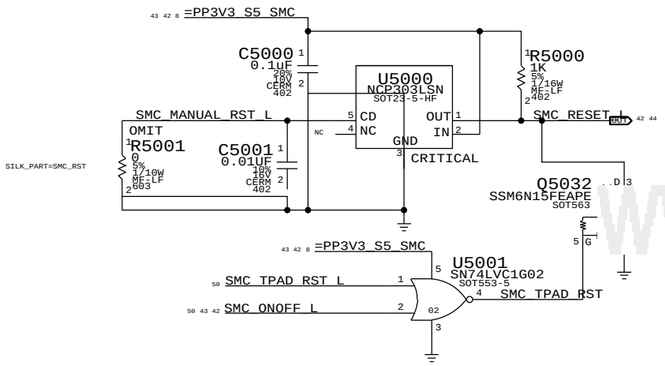
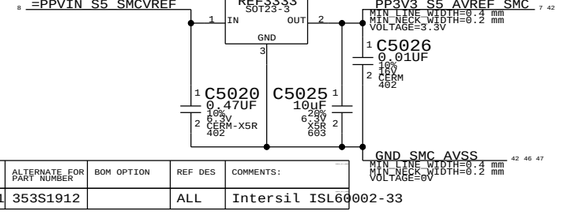
SMC Reset "Button" / Brownout Detect

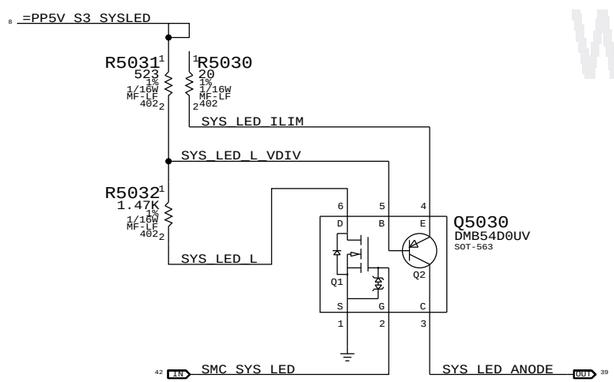


SMC AVREF Supply

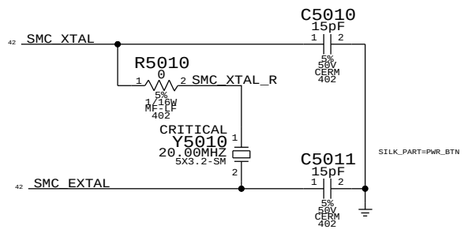


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

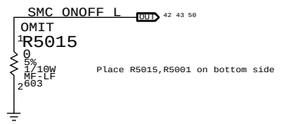
System (Sleep) LED Circuit

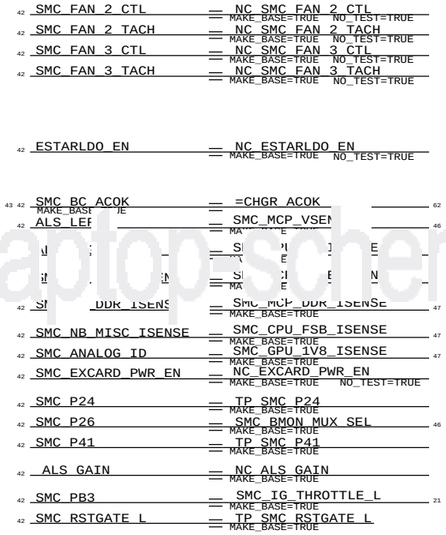


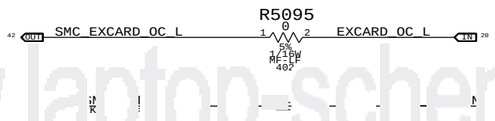
SMC Crystal uit



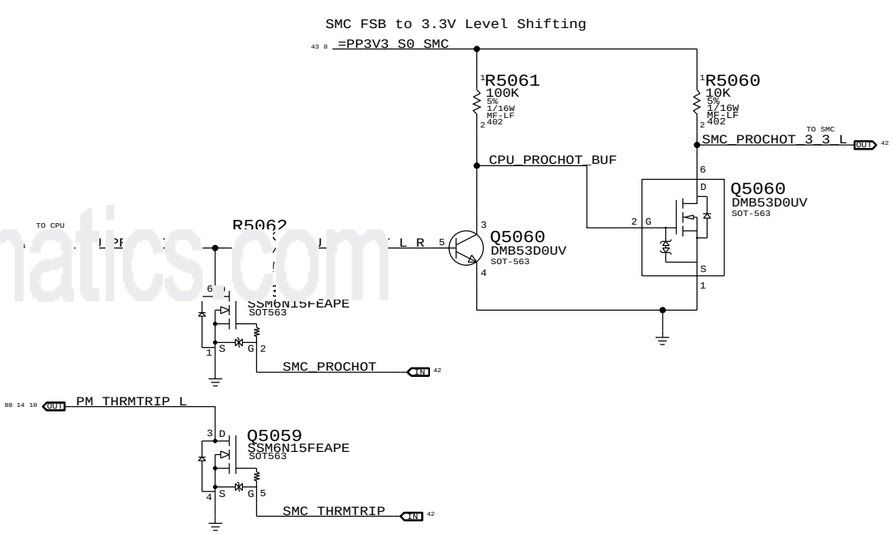
Debug Power "Button"

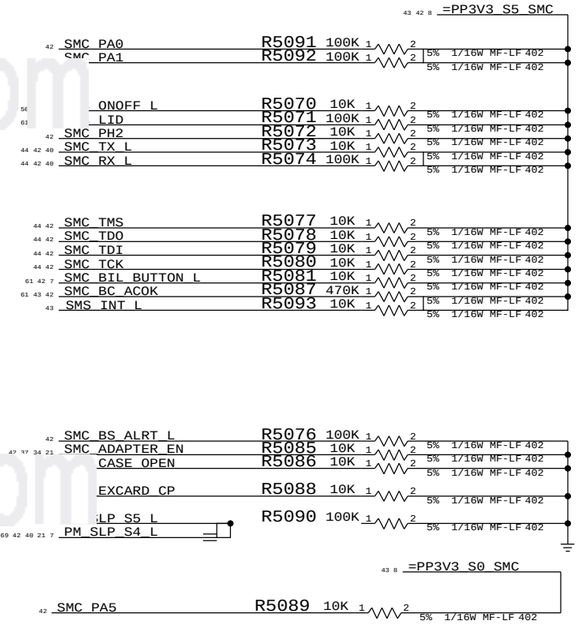






SMC FSB to 3.3V Level Shifting





SYNC_MASTER=DDR SYNC_DATE=12/19/2008

PAGE TITLE: **SMC Support**

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

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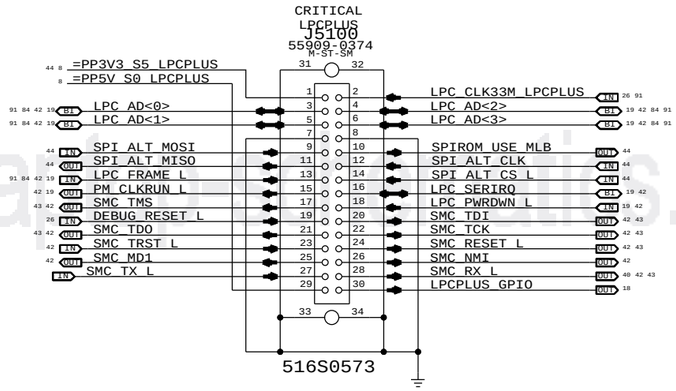
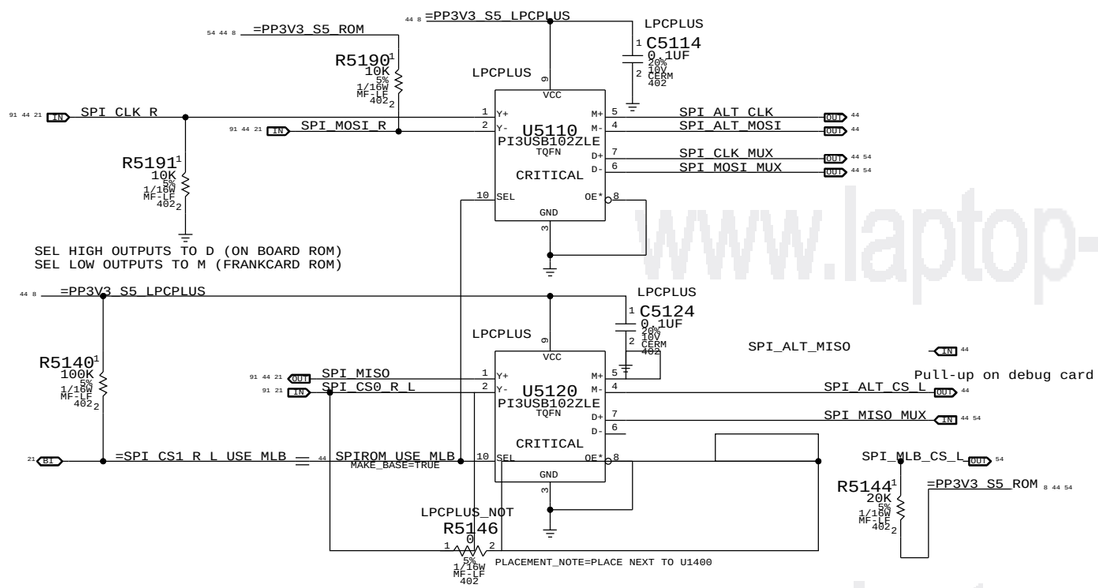
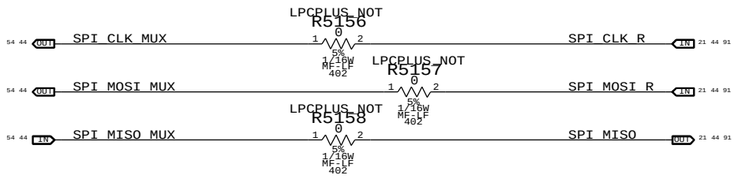
LPC+SPI Connector



Alternate SPI ROM Support



SPI MUX BYPASS



SYNC_MASTER=CHANGZHANG SYNC_DATE=05/09/2008

PAGE TITLE: LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

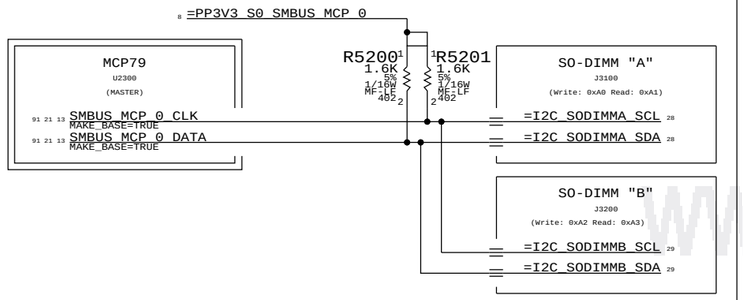
REVISION: C.0.0

BRANCH:

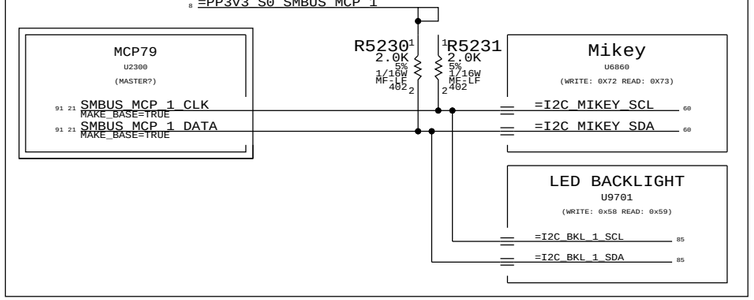
PAGE: 51 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

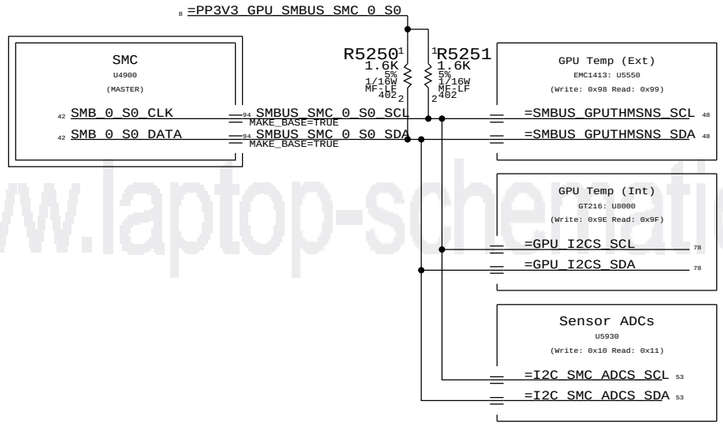
MCP79 SMBus "0" Connections



MCP79 SMBus "1" Connections

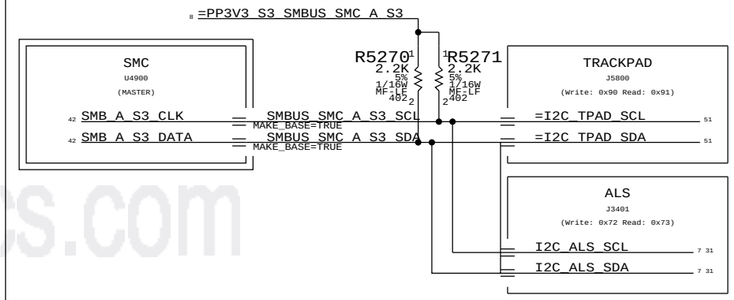


SMC "0" SMBus Connections

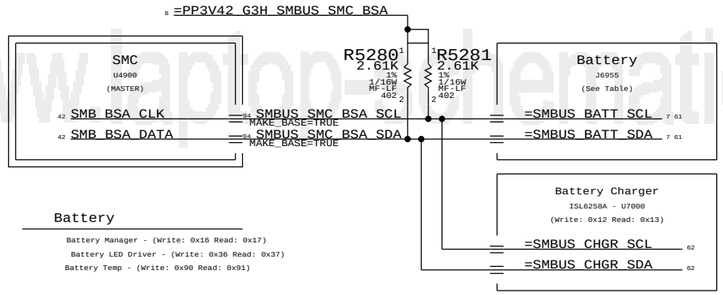


SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state

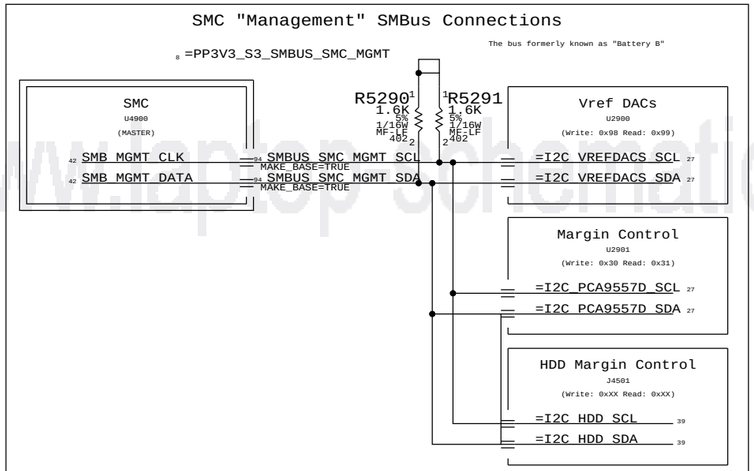


SMC "Battery A" SMBus Connections

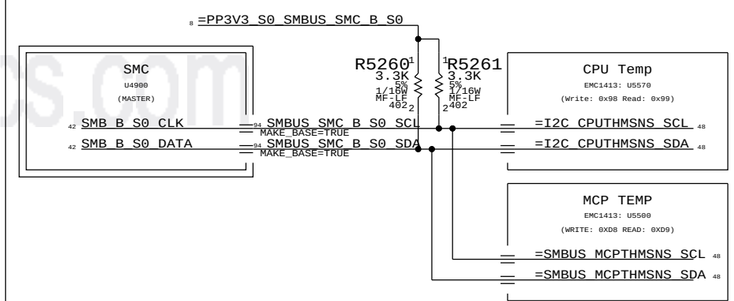


SMC "Management" SMBus Connections

The bus formerly known as "Battery B"



SMC "B" SMBus Connections



SYNC_MASTER=DDR SYNC_DATE=12/19/2008

PAGE TITLE

K19 SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D

REVISION C.0.0

BRANCH

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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU Voltage Sense / Filter

12 11 8 =PPVCORE_S0_CPU — XW5309 (SM) — CPUVSENSE_IN — R5309 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_VSENSE (OUT) 42

Place short near U1000 center

C5309 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

Place RC close to SMC

GPU Voltage Sense / Filter

79 8 =PPVCORE_GPU_REG — XW5359 (SM) — GPUVSENSE_IN — R5359 4.53K 1% 1/16W MF-LF 402 — SMC_GPU_VSENSE (OUT) 42

Place short near U8000 center

C5359 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

Place RC close to SMC

MCP Voltage Sense / Filter

24 22 8 =PPVCORE_S0_MCP — XW5399 (SM) — MCPVSENSE_IN — R5399 4.53K 1% 1/16W MF-LF 402 — SMC_MCP_VSENSE (OUT) 43

PLACEMENT_NOTE=Place near U1400 center

C5399 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

Place RC close to SMC

PBUS Voltage Sense & Filter

Q5315 FDG6332CG SC70-6 (P-CHN)

8 7 PPBUS_G3H — R5315 100K 5% 1/16W MF-LF 402 — PBUSVSENS_EN_DIV

PPBUS_G3H_VSENSE (MIN_LINE_WIDTH=0.20 mm, MIN_NECK_WIDTH=0.20 mm, VOLTAGE=18.5V)

R5385 27.4K 1% 1/16W MF-LF 402 — Rthevanin = 4573 ohms — SMC_PBUS_VSENSE (OUT) 42

R5316 100K 5% 1/16W MF-LF 402 — PBUSVSENS_EN_L

R5386 5.49K 1% 1/16W MF-LF 402 — C5385 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

Place RC close to SMC

69 =PBUSVSENS_EN — Q5315 FDG6332CG SC70-6 (N-CHN)

Enables PBUS VSense divider when high.

BMON Current Sense - Entire circuit must be near SMC (U4900)

8 =PP3V42_G3H_BMON_ISNS — C5318 0.1UF 20% 10V CERM 402 — BMON_ENG

REGULATOR SIDE:

U5303 INA213 SC70 — 96 62 CHGR_CSO_R_P (OUT) — 96 62 CHGR_CSO_R_N (IN)

LOAD SIDE:

Monitors battery discharge current from battery to PBUS

BMON_INA_OUT — U5313 NC7SB3157P6X SC70 — SMC_BMON_MUX_SEL (IN) 43

C5369 0.1UF 20% 10V CERM 402 — BMON_ENG

62 CHGR_BMON (IN) — BMON_AMUX_OUT — R5391 4.53K 1% 1/16W MF-LF 402 — SMC_BATT_ISENSE (OUT) 42

R5330 0 5% 1/16W MF-LF 402 — BMON_PROD

R5371 100K 5% 1/16W MF-LF 402 — BMON_ENG

C5390 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

INA213 has gain of 50V/V

DCIN Current Sense Filter

Place RC close to SMC

62 CHGR_AMON (IN) — R5380 4.53K 1% 1/16W MF-LF 402 — SMC_DCIN_ISENSE (OUT) 42

C5380 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

CPU VCore High Side Current Sensor

8 =PP3V42_G3H_CPUCOREISNS — C5388 0.1UF 20% 10V CERM 402

8 OUT =PPVIN_S5_CPU_IMVP_ISNS — CRITICAL R5388 0.001 1% 0.5W MF 1206 — 96 ISNS_CPU_N — 96 ISNS_CPU_P

8 IN =PPVIN_S5_CPU_IMVP_ISNS_R

U5388 INA210 SC70 — CPUVCORE_HISIDE_IOUT — R5335 4.53K 1% 1/16W MF-LF 402 — SMC_CPU_HI_ISENSE (OUT) 43

C5335 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

Place RC close to SMC

Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

CPU VCore Load Side Current Sense / Filter

Place RC close to SMC

63 IMVP6_IMON (IN) — R5331 6.19K 1% 1/16W MF-LF 402 — SMC_CPU_ISENSE (OUT) 42

R5332 17.4K 1% 1/16W MF-LF 402 — C5330 0.22UF 20% 6.3V X5R 402 — GND_SMC_AVSS 42 43 46 47

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

PAGE TITLE: Current & Voltage Sensing

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

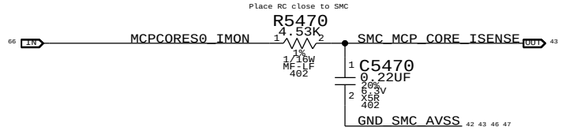
PAGE: 53 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

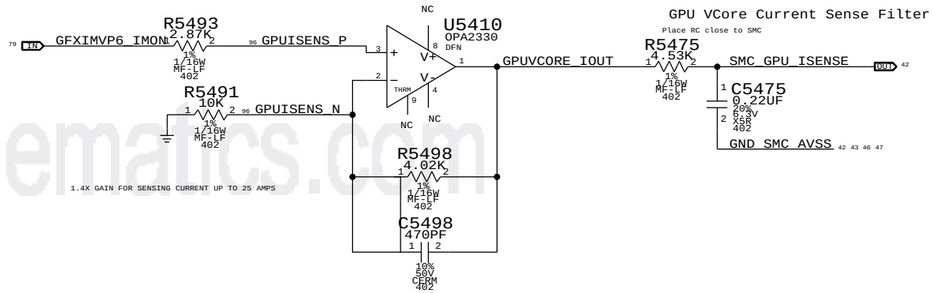
MCP VCore Current Sense

MCP VCore Current Sense Filter

Place RC close to SMC

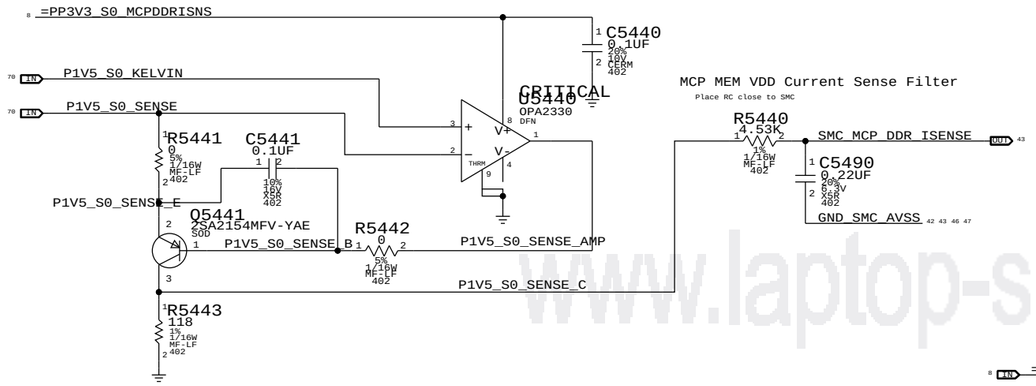


GPU VCore Current Sense



GPU VCore Current Sense and GPU 1.8V Current Sense share
dual package opamp U5410

MCP MEM VDD Current Sense

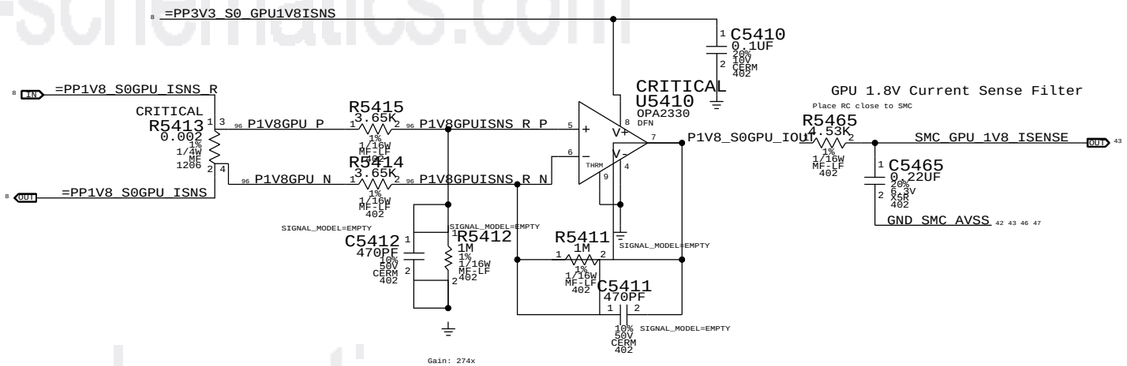


MCP MEM VDD Current Sense Filter

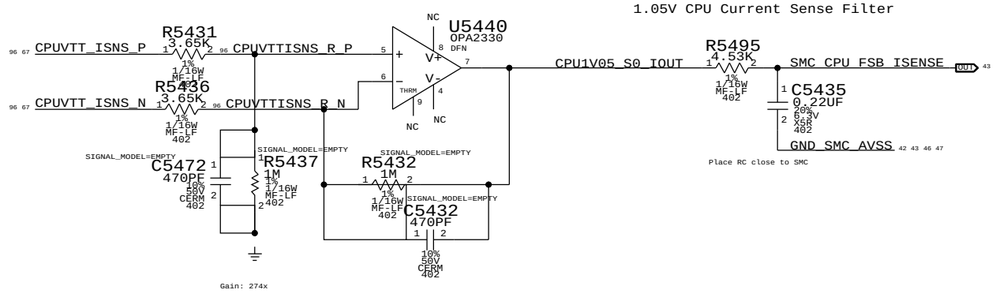
Place RC close to SMC

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share
dual package opamp U5440

GPU 1.8V Current Sense

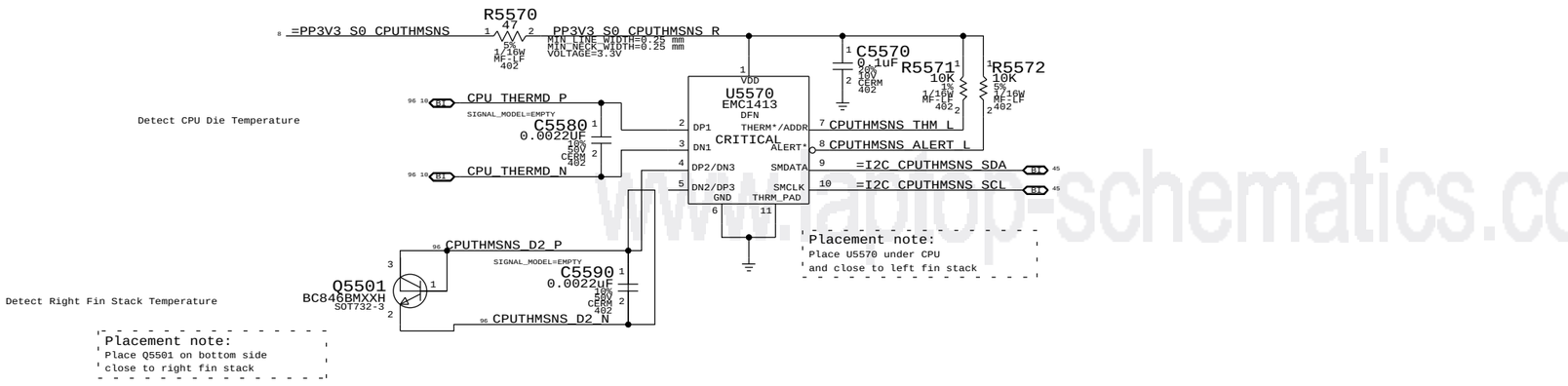


CPU FSB 1.05V Current Sense

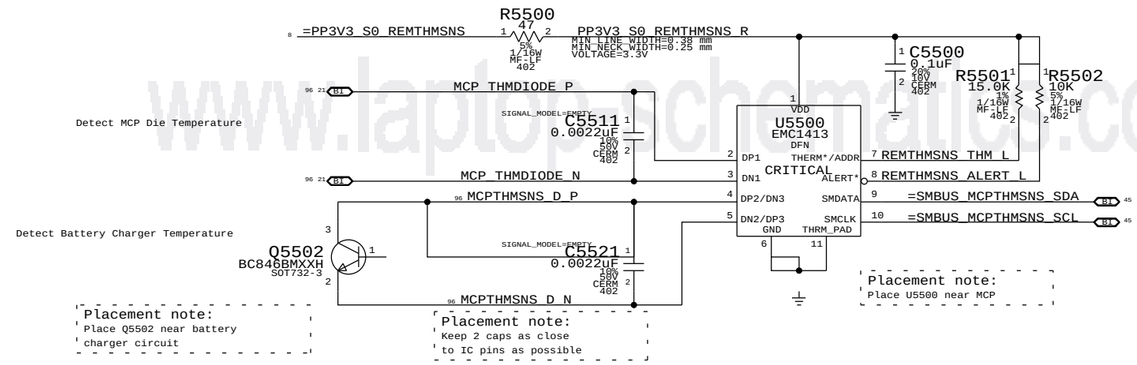


SYNC_MASTER=YUN_K19_MLB	SYNC_DATE=12/10/2008
PAGE TITLE: Current Sensing	
Apple Inc.	DRAWING NUMBER: 051-7892 SIZE: D
	REVISION: C.0.0
	BRANCH:
	PAGE: 54 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

CPU Proximity/CPU Die/Right Fin Stack

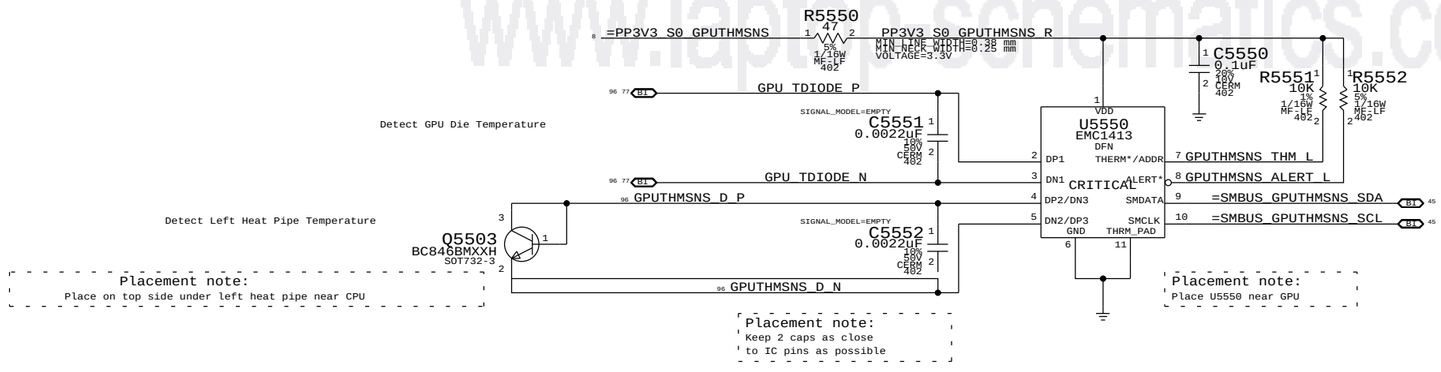


MCP Proximity/MCP Die/Battery Charger Proximity



Note: EMC1413 can perform Beta Compensation for External Diode 1 only

GPU Proximity/GPU Die/Left Heat Pipe



SYNC_MASTER=YUN_K19_MLB SYNC_DATE=12/22/2008

PAGE TITLE: Thermal Sensors

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

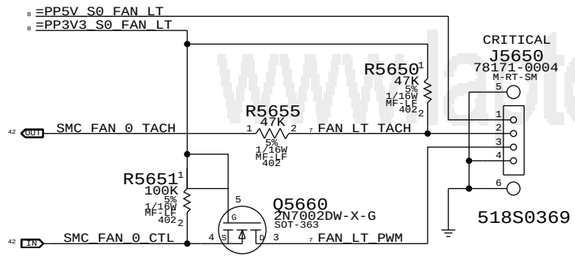
REVISION: C.0.0

BRANCH:

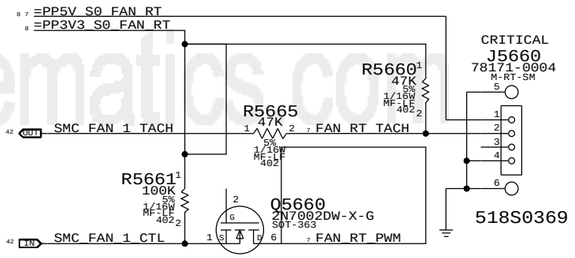
PAGE: 55 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Left Fan



Right Fan



SYNC MASTER=M87 MLB SYNC DATE=10/17/2007

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 56 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PSOC USB CONTROLLER

USB INTERFACES TO MLB
SPI HOST TO Z2

TRACKPAD PICK BUTTONS
KEYBOARD SCANNER

PP3V3_S3_PSOC

PICKB_L
BUTTON_DISABLE
Z2_HOST_INTN
WS_LEFT_SHIFT_KEY
WS_LEFT_OPTION_KEY

WS_KBD23 WS_KBD22 WS_KBD21 WS_KBD20 WS_KBD19 WS_KBD18

WS_CONTROL_KEY
Z2_KEY_ACT_L
TP_BOOT_CFG1
TP_P4_5
Z2_DEBUG3
Z2_RESET
PSOC_MISO
PSOC_F_CS_L
PSOC_MOSI
PSOC_SCLK
Z2_MISO
Z2_CS_L
Z2_MOSI
Z2_SCLK

CRITICAL
U5701
CY8C24794
MLF
(SYM-VER2)
APN 337S2983
OMIT

P2_3 P2_1 P4_7 P4_5 P4_3 P4_1 P3_7 P3_5 P3_3 P3_1 P5_7 P5_5 P5_3 P5_1
P2_2 P2_0 P4_6 P4_4 P4_2 P4_0 P3_6 P3_4 P3_2 P3_0 P5_6 P5_4 P5_2 P5_0
P1_7 P1_5 P1_3 P1_1 VSS VDD P7_7 P7_0 P1_0 P1_2 P1_4 P1_6
THRML PAD

WS_KBD17 WS_KBD16N WS_KBD15_C WS_KBD14 WS_KBD13 WS_KBD12 WS_KBD11 WS_KBD10 WS_KBD9 WS_KBD8 WS_KBD7 WS_KBD1 WS_KBD2 WS_KBD3

TP_PSOC_SCL
TP_PSOC_SDA
TP_PSOC_P1_3
ISSP_SCLK_P1_1
ISSP SCLK/I2C SCL
ISSP_SDATA_P1_0
ISSP SDATA/I2C SDA
Z2_CLKIN
TP_P7_7

WS_KBD4 WS_KBD5 WS_KBD6

DIFFERENTIAL_PAIR=USB2_TPAD
USB_TPAD_P — R5701 24 5% 1/16W MF-LF 402 — USB_TPAD_R_P
DIFFERENTIAL_PAIR=USB2_TPAD
NET_SPACING_TYPE=USB
NET_PHYSICAL_TYPE=USB_90D
PP3V3_S3_PSOC

TO MLB CONNECTOR

DIFFERENTIAL_PAIR=USB2_TPAD
USB_TPAD_N — R5702 24 5% 1/16W MF-LF 402 — USB_TPAD_R_N
DIFFERENTIAL_PAIR=USB2_TPAD
NET_SPACING_TYPE=USB
NET_PHYSICAL_TYPE=USB_90D

U5701 CHIP DECOUPLING

PLACE C5701, C5702 & C5703
CLOSE TO U5701 VDD PIN 22

PLACE C5704, C5705 & C5706
CLOSE TO U5701 VDD PIN 49

PP3V3_S3_PSOC
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM

C5701 4.7UF 20% 6.3V X5R 603
C5702 100PF 10% 50V CERM 402
C5703 0.1UF 10% 16V X7R-CERM 402
C5704 100PF 10% 50V CERM 402
C5705 0.1UF 10% 16V X7R-CERM 402
C5706 4.7UF 20% 6.3V X5R 603

R5704 1.5 5% 1/16W MF-LF 402 =PP3V3_S3_TPAD

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA MAX 60MA MAX	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

TEST POINTS ARE FOR ON BOARD PROGRAMMING

TPAD_DEBUG
APN 518S0430
J5702
FH19C-4S-0.5SH25
F-RT-SM1

NC
=PP3V3_S3_TPAD
ISSP_SCLK_P1_1
ISSP_SDATA_P1_0
ISSP CLOCK
ISSP DATA
NC

ISOLATION CIRCUIT

=PP3V42_G3H_TPAD
C5725 0.1UF 20% 16V CERM 402
CRITICAL
5 TC7SZ08AFEAPE SOT665
=PP3V3_S3_TPAD
U5725
WS_LEFT_SHIFT_KBD
WS_LEFT_SHIFT_KEY

=PP3V42_G3H_TPAD
CRITICAL
=PP3V3_S3_TPAD
U5726
WS_LEFT_OPTION_KBD
WS_LEFT_OPTION_KEY

=PP3V42_G3H_TPAD
CRITICAL
=PP3V3_S3_TPAD
U5727
WS_CONTROL_KBD
WS_CONTROL_KEY

TPAD BUTTONS DISABLE

BUTTON_DISABLE

PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

Q5701
SSM3K15FV
SOD-VESM-HF

SMC_LID

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

KEYBOARD CONNECTOR

J5713
APN 518S0637
=PP3V3_S3_TPAD
WS_KBD1 WS_KBD2 WS_KBD3 WS_KBD4 WS_KBD5 WS_KBD6 WS_KBD7 WS_KBD8 WS_KBD9 WS_KBD10 WS_KBD11 WS_KBD12 WS_KBD13 WS_KBD14 WS_KBD15_CAP WS_KBD16_NUM WS_KBD17 WS_KBD18 WS_KBD19 WS_KBD20 WS_KBD21 WS_KBD22 WS_KBD23 WS_KBD_ONOFF_L =PP3V42_G3H_TPAD WS_LEFT_SHIFT_KBD WS_LEFT_OPTION_KBD WS_CONTROL_KBD
F-RT-SM
FF14-30A-R11B-B-3H

R5714 470 1% 1/16W MF-LF 402 — WS_KBD15_C
R5715 10K 1% 1/16W MF-LF 402 — WS_KBD16N
R5710 1K 5% 1/10W MF-LF 402 — SMC_ONOFF_L
C5710 0.1UF 20% 16V CERM 402
PLACEMENT_NOTE=NEAR J5713

SMC_MANUAL_RESET LOGIC

=PP3V42_G3H_TPAD
C5758 0.1UF 10% 16V X5R-CERM 402

APN 311S0406
CRITICAL
SN74LVC1G10
SC70
U5703
WS_LEFT_SHIFT_KBD
WS_LEFT_OPTION_KBD
WS_CONTROL_KBD
SMC_TPAD_RST_L

R5769 33K 5% 1/16W MF-LF 402
R5770 33K 5% 1/16W MF-LF 402
R5771 33K 5% 1/16W MF-LF 402

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

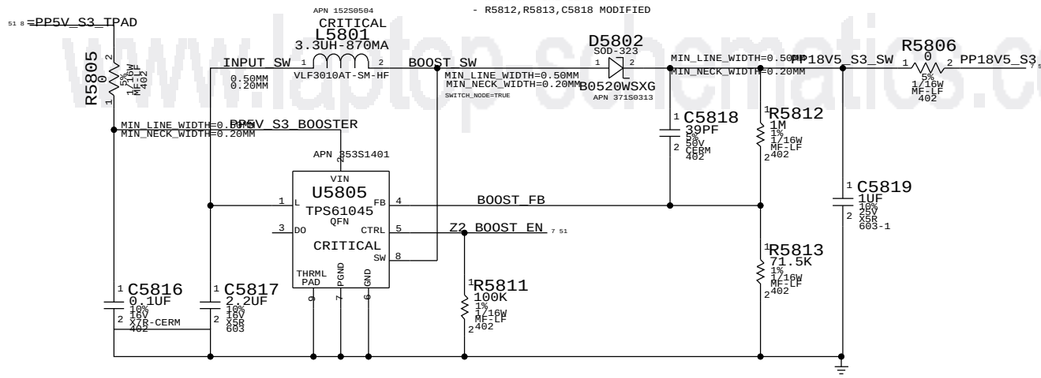
PAGE TITLE: WELLSPRING 1

Apple Inc.

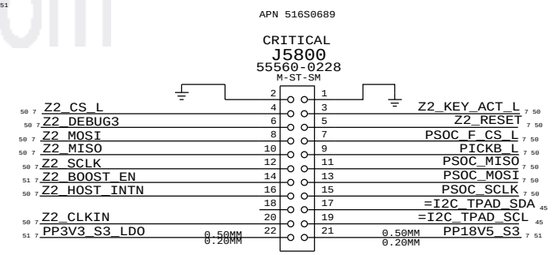
DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 57 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

BOOSTER +18.5VDC FOR SENSORS

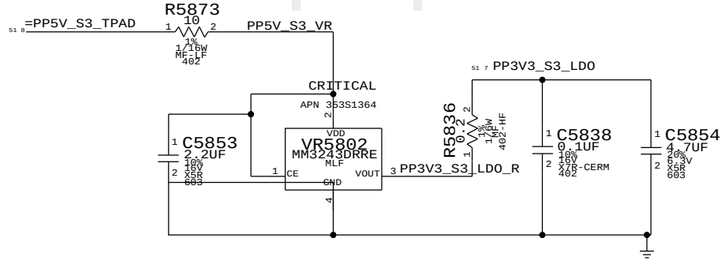
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD FLEX CONNECTOR



3V3 LDO FOR IPD

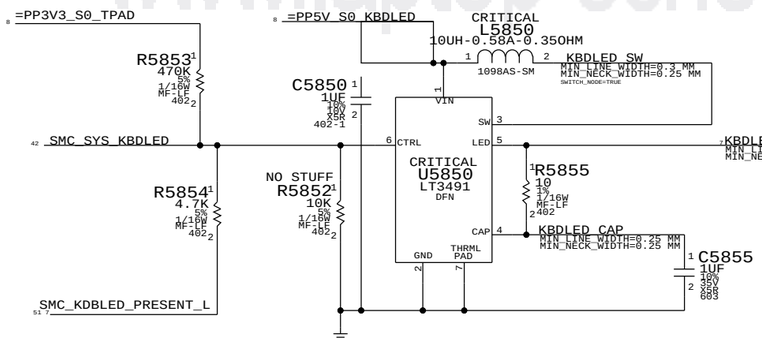


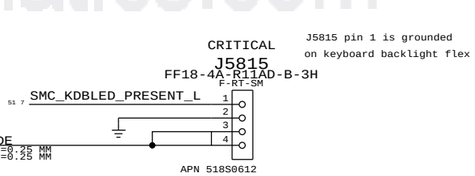
Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
LOW = keyboard backlight present
HIGH= keyboard backlight not present

BOM OPTION: KBDLED_YES

R5853 ALWAYS PRESENT





KBD BACKLIGHT CONNECTOR

SYNC_MASTER=PWRSQNC SYNC_DATE=01/05/2009

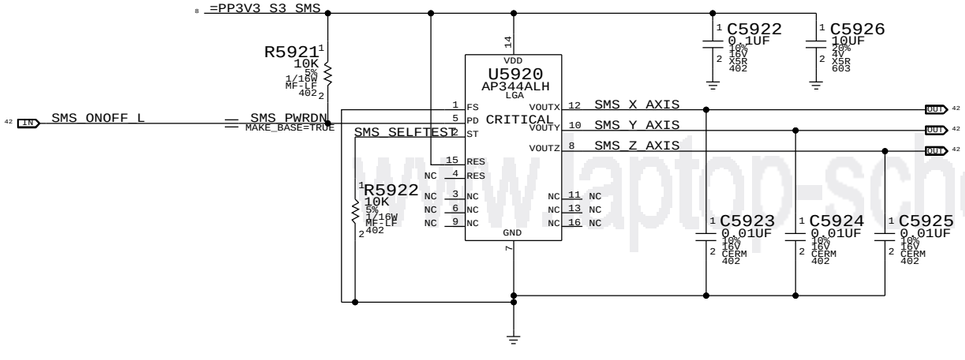
PAGE TITLE: WELLSPRING 2

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 58 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:

Front of system

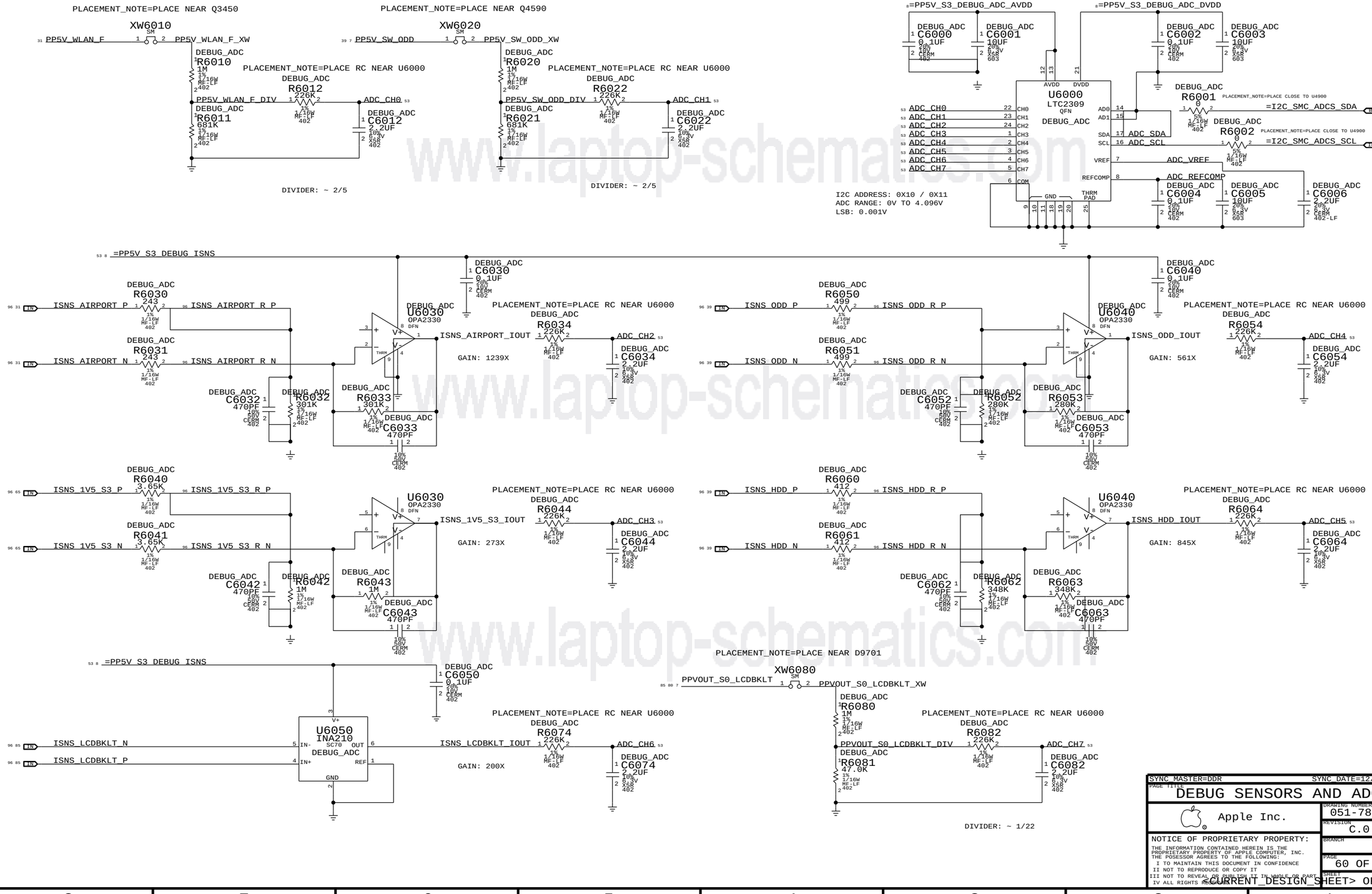
Circle indicates pin 1 location when placed in correct orientation

SYNC MASTER=SENSOR SYNC DATE=08/14/2008

PAGE TITLE
Sudden Motion Sensor (SMS)

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 59 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=DDR SYNC_DATE=12/19/2008

PAGE TITLE: DEBUG SENSORS AND ADC

Apple Inc.

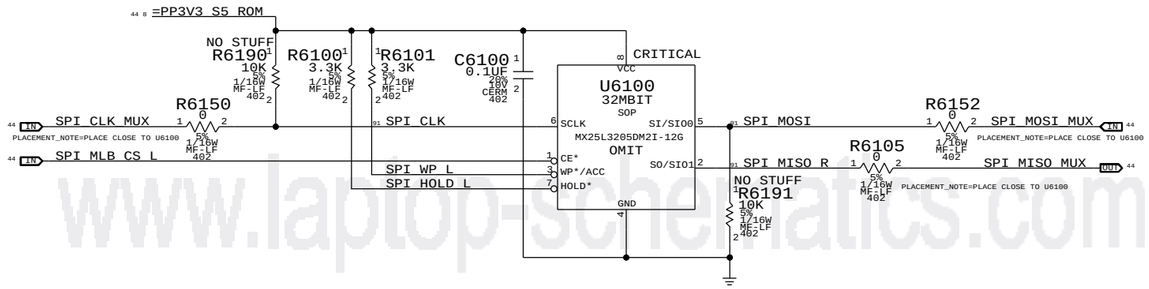
DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 60 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



MCP79 SPI Frequency Select

Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
Any of the 4 frequencies can be selected
with R6190, R6191, R5190 and R5191

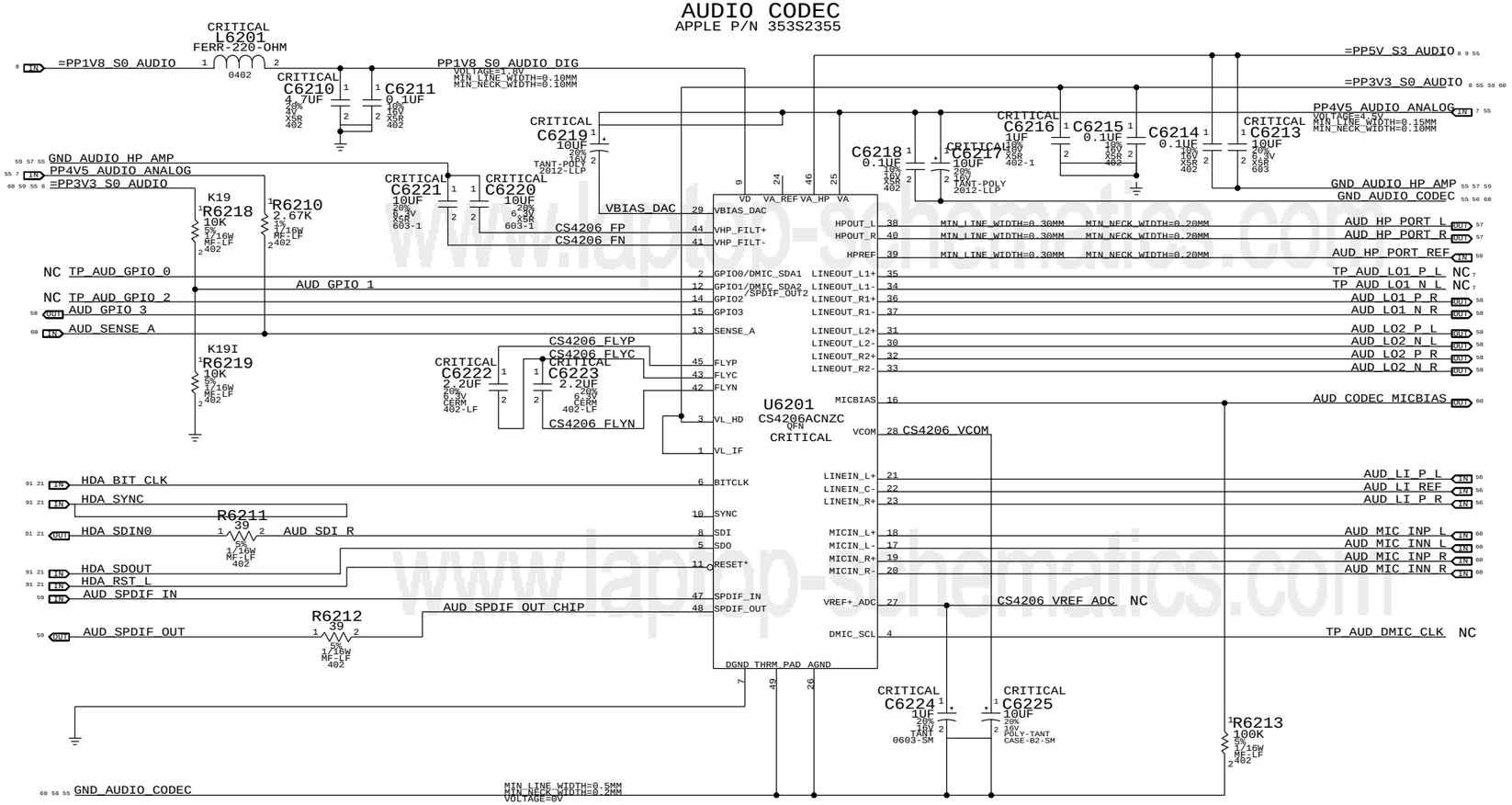
SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

PAGE TITLE: SPI ROM

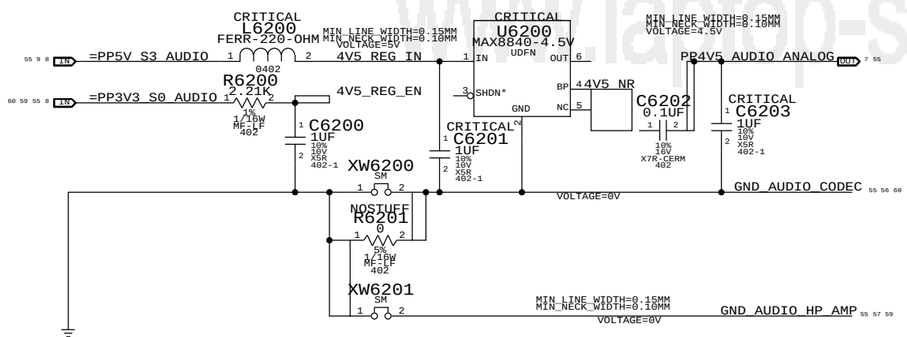
Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 61 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

AUDIO CODEC
APPLE P/N 353S2355



4.5V POWER SUPPLY FOR CODEC
APPLE P/N 353S2234



NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

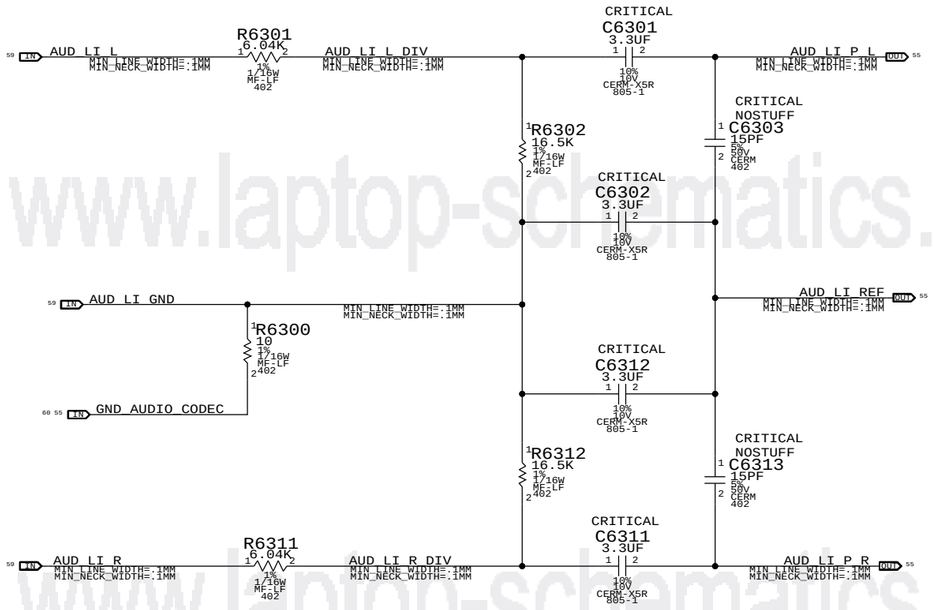
PAGE TITLE: AUDIO: CODEC/REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 62 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 20K OHMS
FC = 8 HZ
VIN = 2VRMS, CODEC VIN = 1.21 VRMS



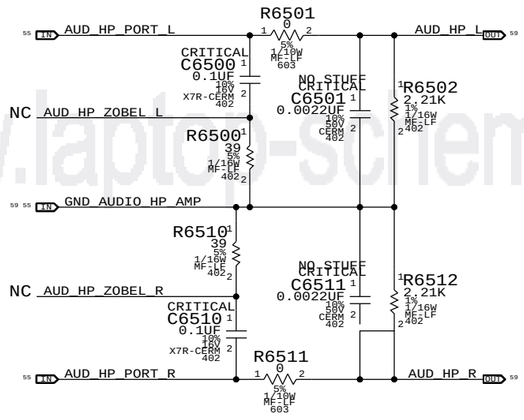
SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 63 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC MASTER=AUDIO SYNC DATE=03/16/2009

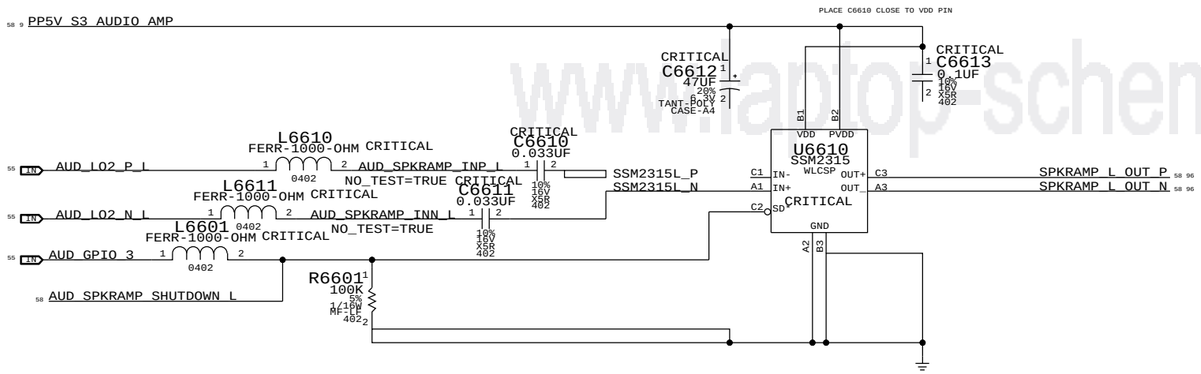
PAGE TITLE
AUDIO: HEADPHONE FILTER

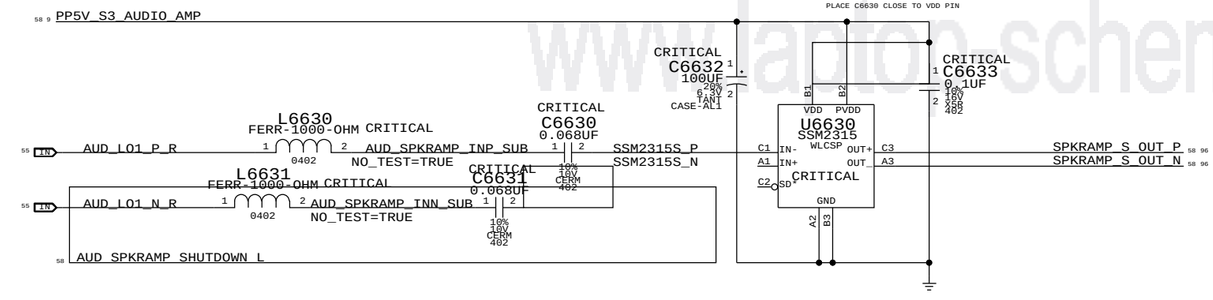
Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 65 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

3X MONO SPEAKER AMPLIFIERS (SSM2315)
APN: 353S2500

GAIN = 6DB
1ST ORDER FC (L&R) = 120 HZ +/- 30%
1ST ORDER FC (SUB) = 58HZ +/- 30%



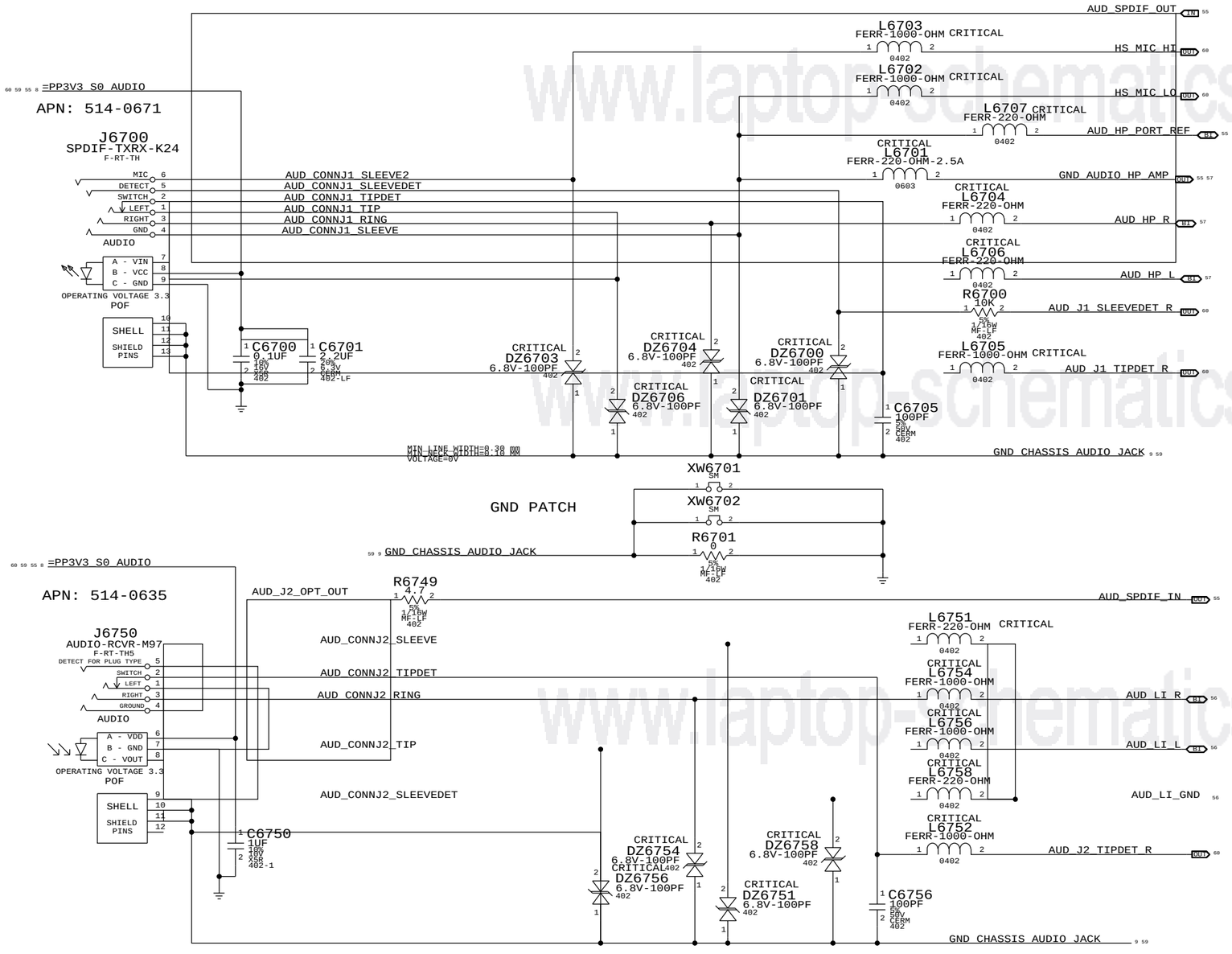


SPEAKER CHECKPOINTS

MIN_LINE_WIDTH=0.30 mm
MIN_NECK_WIDTH=0.20 MM
SPKRAMP_L_OUT_P — R6610 0 5% 1/16W MF-LF 402 — SPKRCONN_L_OUT_P
SPKRAMP_L_OUT_N — R6611 0 5% 1/16W MF-LF 402 — SPKRCONN_L_OUT_N
SPKRAMP_R_OUT_P — R6620 0 5% 1/16W MF-LF 402 — SPKRCONN_R_OUT_P
SPKRAMP_R_OUT_N — R6621 0 5% 1/16W MF-LF 402 — SPKRCONN_R_OUT_N
SPKRAMP_S_OUT_P — R6630 0 5% 1/16W MF-LF 402 — SPKRCONN_S_OUT_P
SPKRAMP_S_OUT_N — R6631 0 5% 1/16W MF-LF 402 — SPKRCONN_S_OUT_N

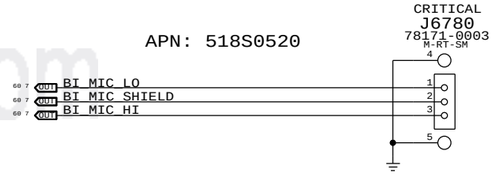
SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009
PAGE TITLE: AUDIO: SPEAKER AMP
Apple Inc.
DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 66 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

AUDIO JACK 1 LO/HP JACK, SPDIF TX

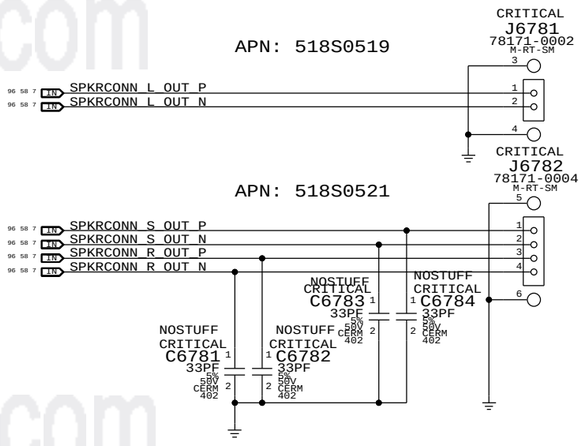


AUDIO JACK 2 LINE IN JACK, SPDIF RX

MIC CONNECTOR



SPEAKER CONNECTOR



SYNC_MASTER=AUDIO SYNC_DATE=03/16/2009

PAGE TITLE: AUDIO: JACKS

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

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SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

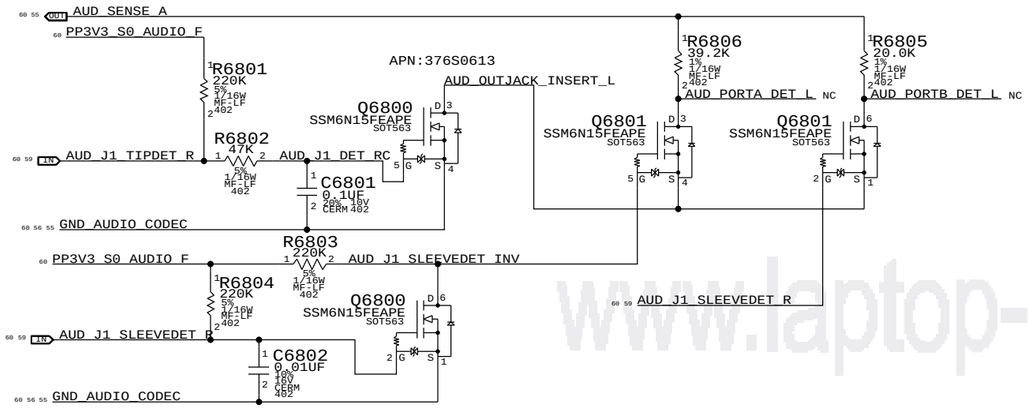
CODEC OUTPUT SIGNAL PATHS

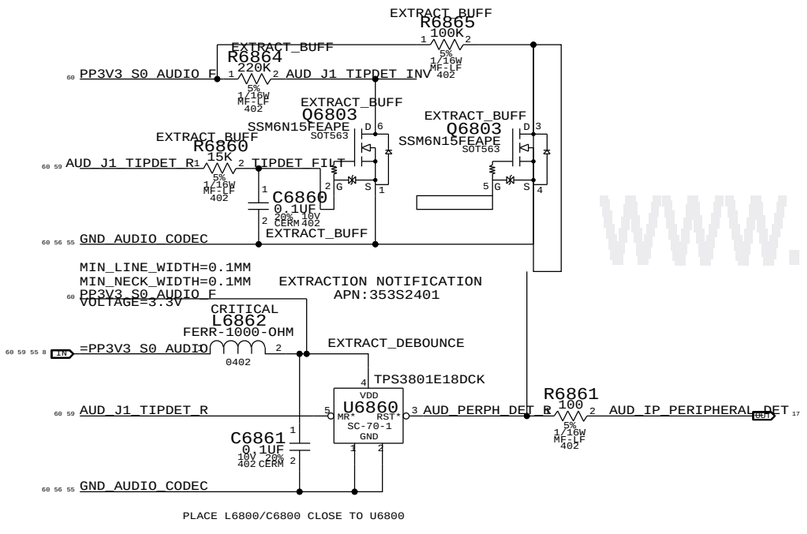
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0C (B)

CODEC INPUT SIGNAL PATHS

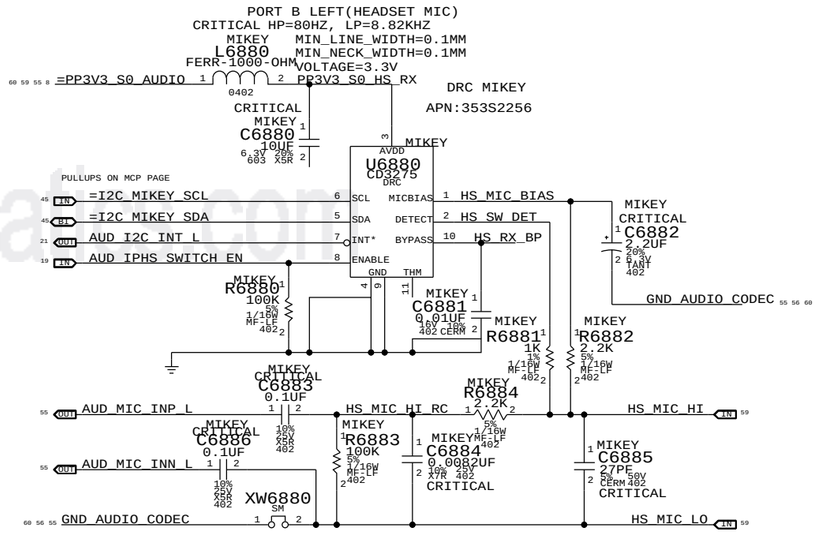
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X05 (5)	0X0C (12,C)	N/A	0X0C (12,C)
SPDIF IN	0X07 (7)	0X0F (15)	N/A	N/A
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

PORT A DETECT (HEADPHONES) PORT B DETECT(SPDIF DELEGATE)

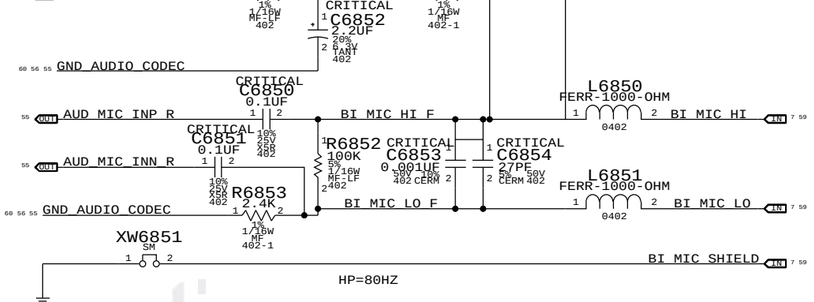




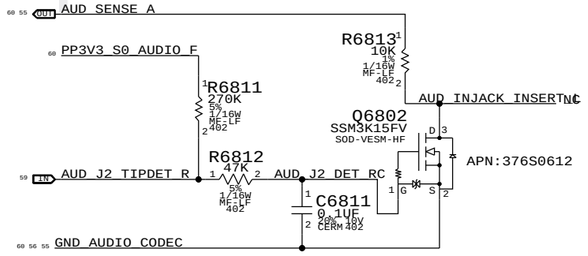
PORT B LEFT(HEADSET MIC)



PORT B RIGHT(BUILT-IN MIC)



PORT C DETECT (LINE-IN)



SYNC MASTER=AUDIO SYNC DATE=03/16/2009

PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
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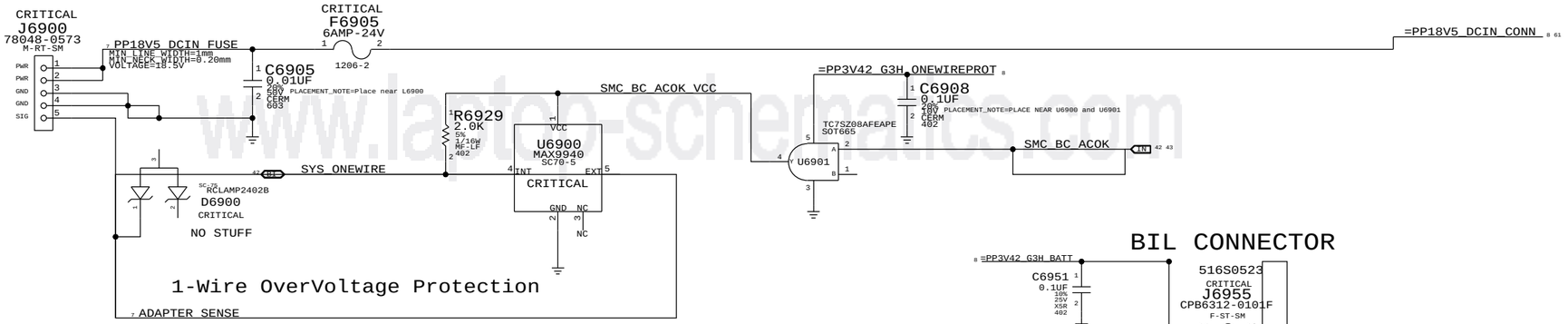
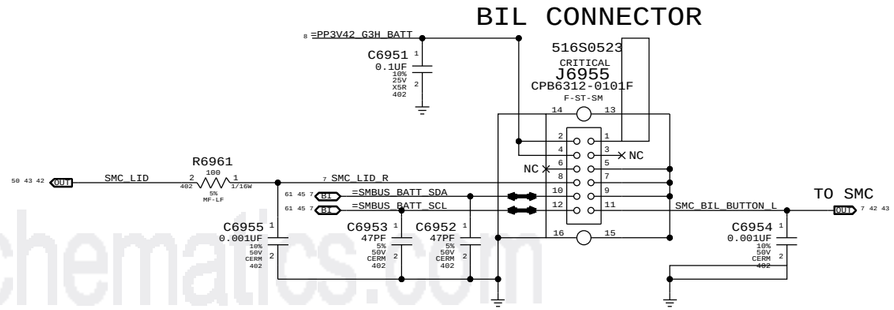
MagSafe DC Power Jack



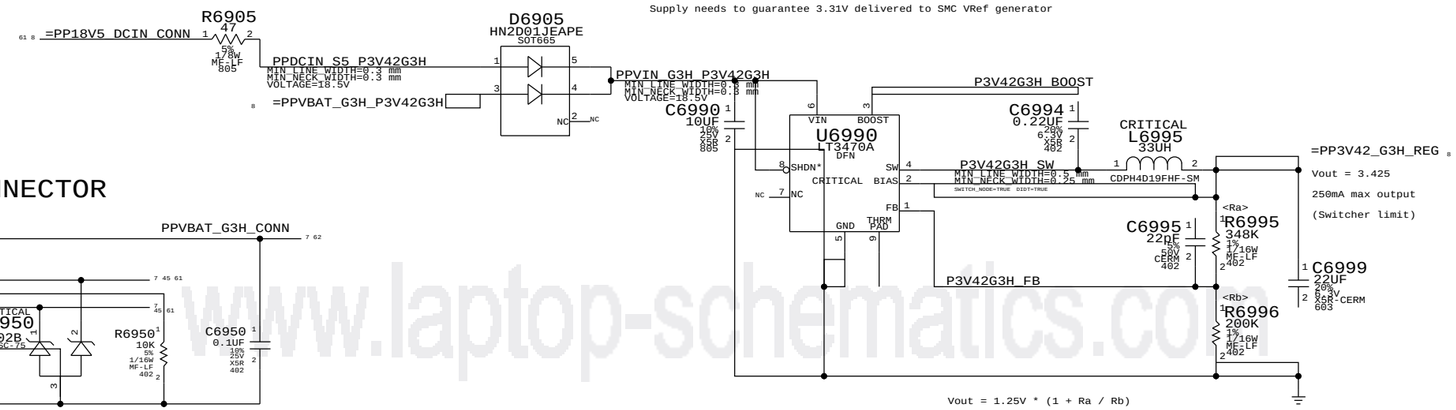
The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

BIL CONNECTOR

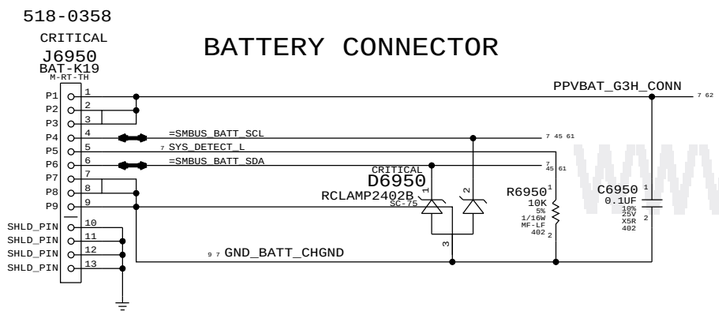


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=YUN_K19_MLB	SYNC_DATE=12/16/2008
PAGE TITLE: DC-In & Battery Connectors	
Apple Inc.	DRAWING NUMBER: 051-7892 SIZE: D
	REVISION: C.0.0
	BRANCH:
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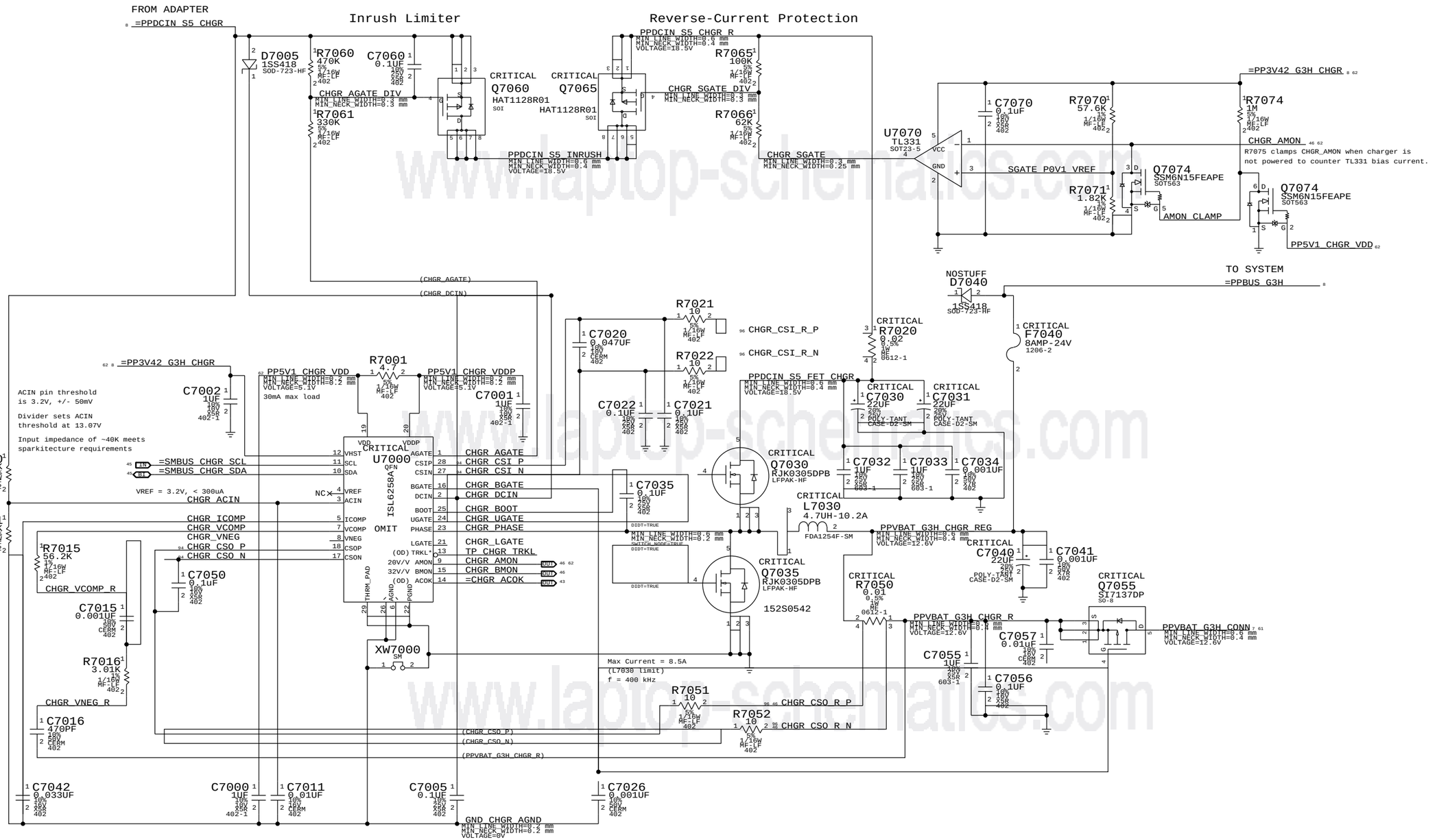

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
353S1811	1	IC,ISL6258,BAT CHARGER,28P,4X4,QFN,L	U7000	CRITICAL	ISL6258	2S Battery Default
353S1832	1	IC,ISL6258A,BAT CHARGER,4X4MM,QFN28	U7000	CRITICAL	ISL6258A	3S Battery Default

SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

These caps are for Q7100

These caps are for Q7102

LAYOUT NOTE:
Place R7126 in hot spot of reg circuit.

Place R7131 Between L7100,L7101 and CPU

NO STUFF

IMVP6_PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		

IMVP6_PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		
IMVP6_VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM		
IMVP6_VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM		

IMVP6_VR_ON	IMVP6_VR_ON_R			
IMVP6_OCSET	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VO	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_DROOP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_DFB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_SOFT	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_RBIAS	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VDIFF	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_FB2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_FB	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_COMP	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		
IMVP6_VW	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM		

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

PAGE TITLE
IMVP6 CPU VCore Regulator

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
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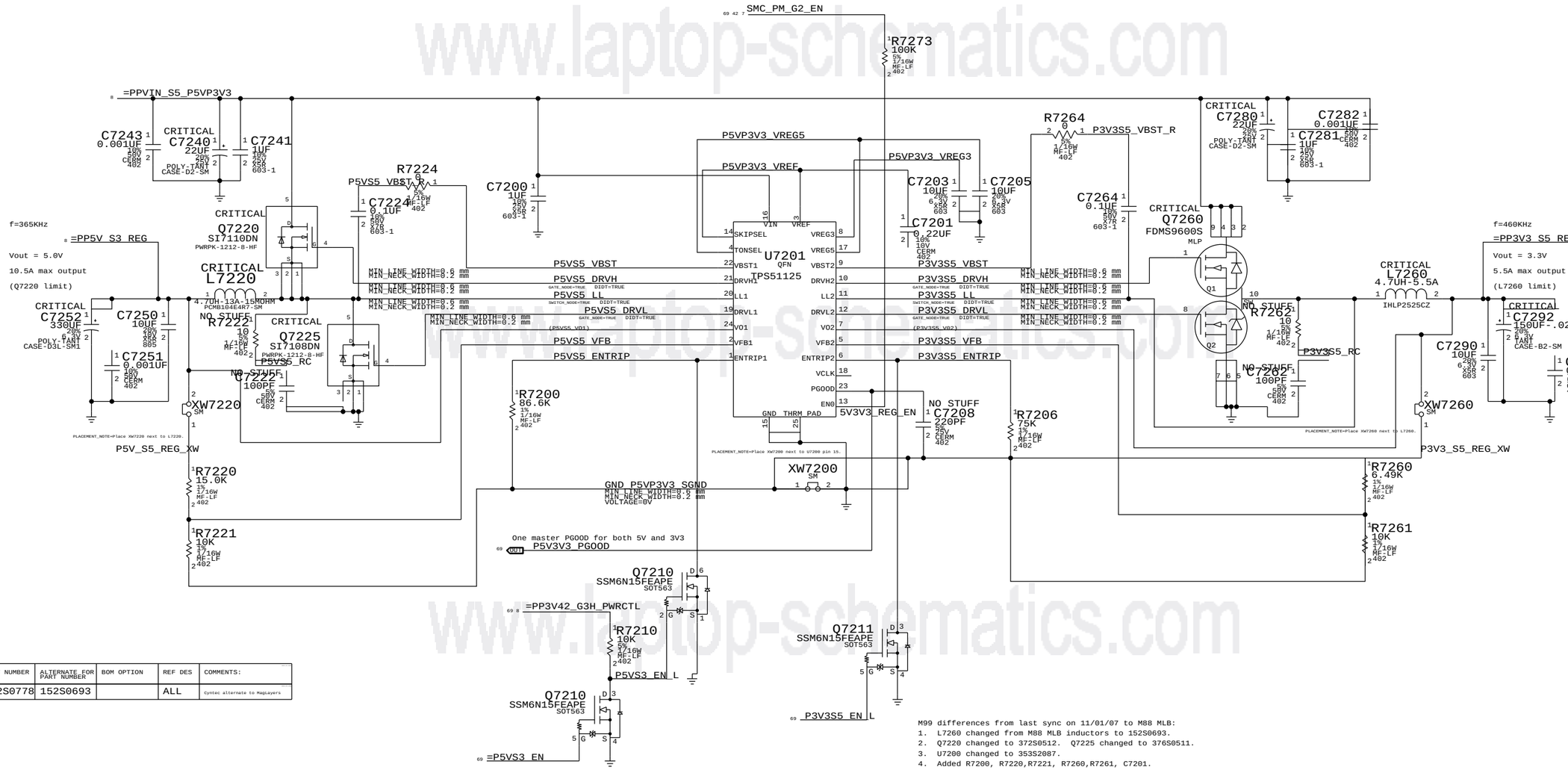

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S0778	152S0693		ALL	Cyntec alternate to MagLayers

M99 differences from last sync on 11/01/07 to M88 MLB:
1. L7260 changed from M88 MLB inductors to 152S0693.
2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
3. U7200 changed to 353S2087.
4. Added R7200, R7220,R7221, R7260,R7261, C7201.

SYNC_MASTER=PWRSQNC SYNC_DATE=12/17/2008

PAGE TITLE: 5V / 3.3V Power Supply

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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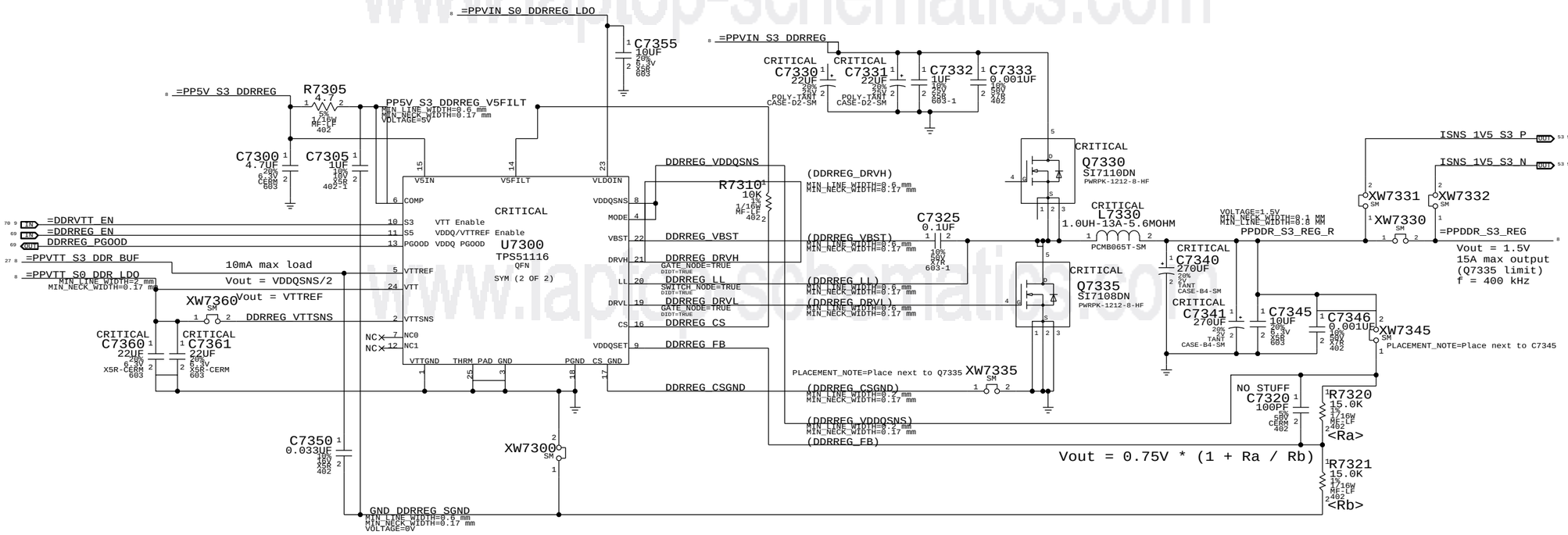
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



SYNC_MASTER=DDR SYNC_DATE=12/05/2008

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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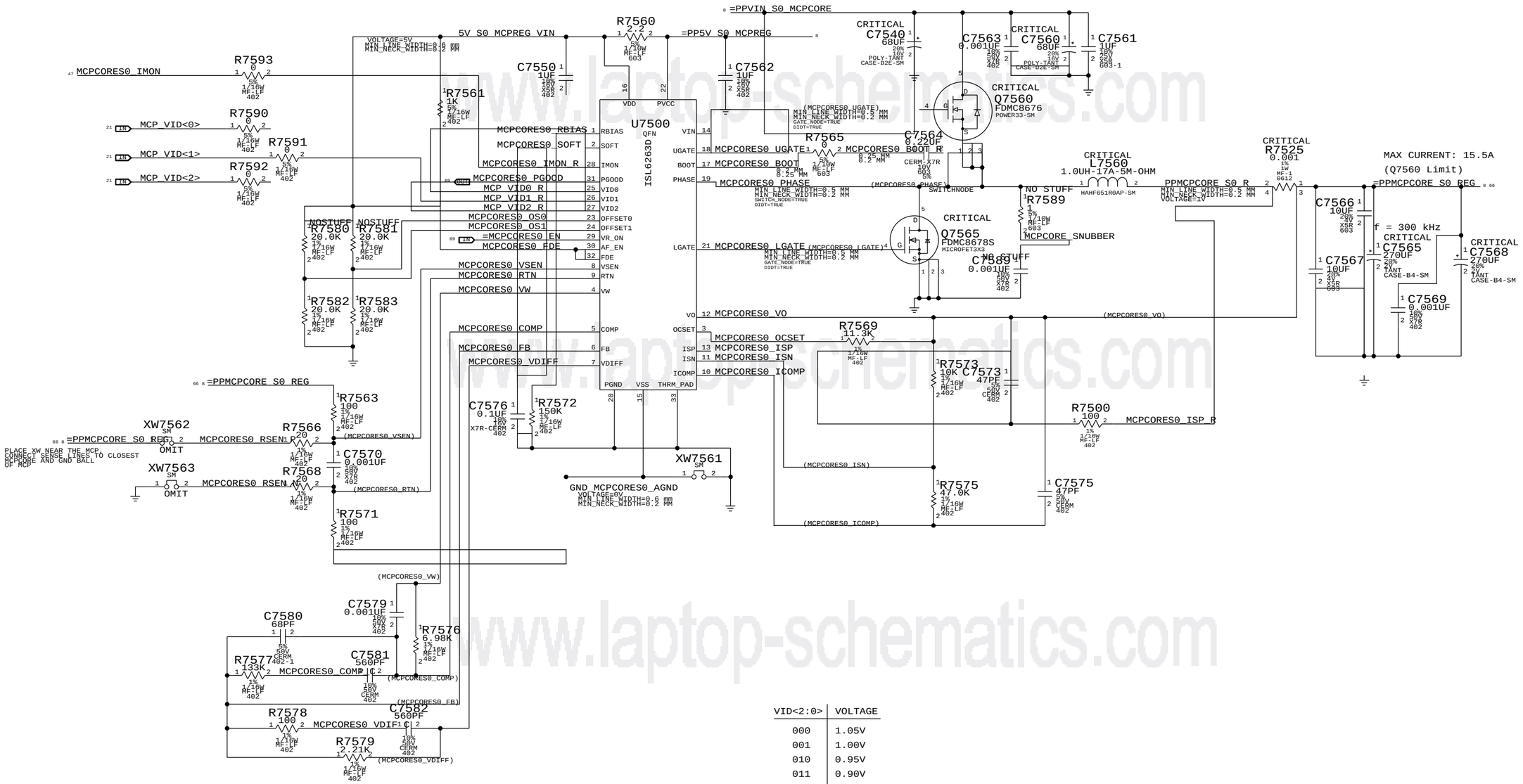

VID<2:0>	VOLTAGE
000	1.05V
001	1.00V
010	0.95V
011	0.90V
100	0.85V
101	0.80V
110	0.75V
111	0.70V

SYNC_MASTER=M98_MLB SYNC_DATE=11/14/2008

PAGE TITLE: MCP CORE REGULATOR

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

BRANCH:

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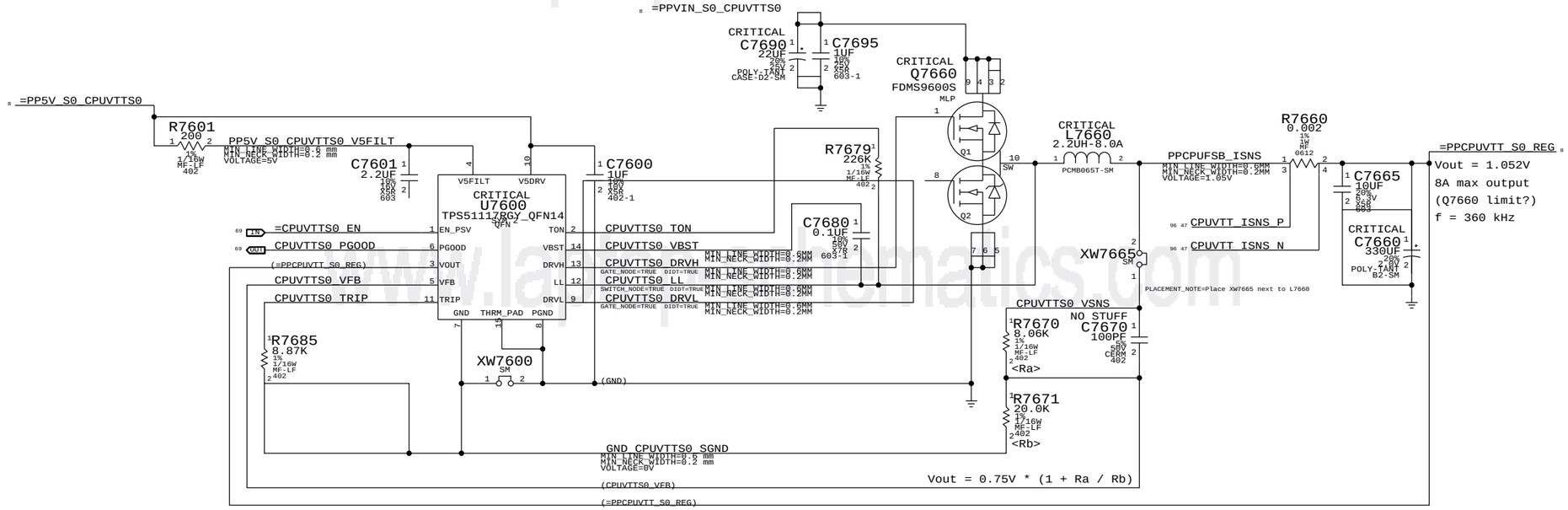
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



M99 differences from last sync on 12/03/07 to T18 MLB:
1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

PAGE TITLE
CPU VTT / 1V05 S0 Power Supply

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
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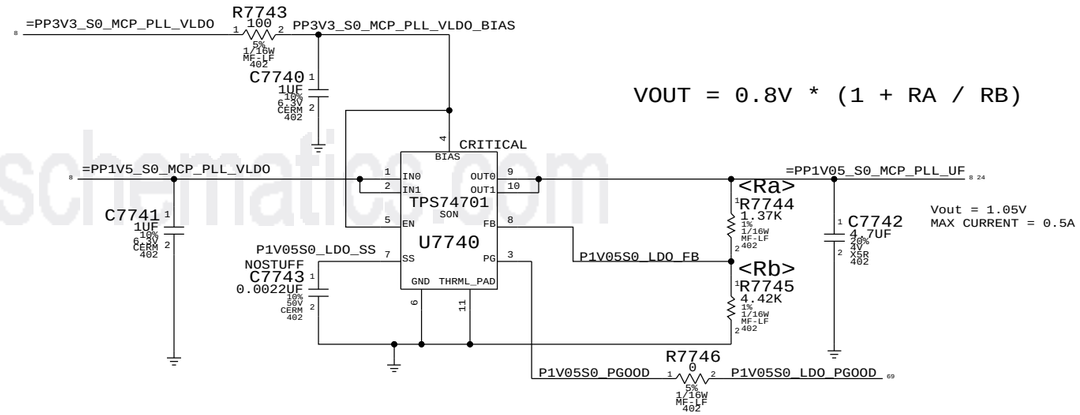
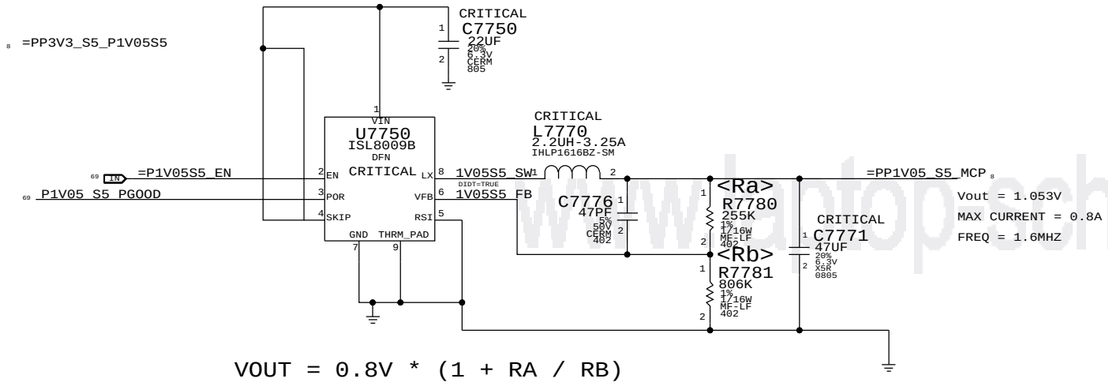
1.05V S0 PLL LDO



VOUT = 0.8V * (1 + RA / RB)

MCP 1.05V S5 (AUXC) SUPPLY



VOUT = 0.8V * (1 + RA / RB)

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

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3.3V 1,05V S5 ENABLE

=PP3V42_G3H_PWRCTL → R7802 100K → P3V3S5_EN_L

SMC_PM_G2_EN → R7858 100K; Q7800 SSM3K15FV (SOD-VESM-HF)

R7801 5.1K → PM_G2_P1V05S5_EN → =P1V05S5_EN (MAKE_BASE=TRUE)

C7801 0.47UF 10% 6.3V CERM-X5R 402

NO STUFF C7802 0.068UF 10% 16V CERM 402

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

S5 rail PWRGD

=PP3V42_G3H_PWRCTL, =PP3V3_S5_PWRCTL

C7840 0.1uF 20% 16V CERM 402; R7840 100K 5% 1/10W MF-LF 402

U7840 TPS3808G33DBVRG4 SOT23-6 (SENSE, CT, GND, VDD, RESET*, MR*)

C7841 0.0001UF 20% 50V CERM 402

RSMRST_PWRGD, P1V05_S5_PGOOD

TPS3808 MR* HAS INTERNAL PULLUP

3.3V,5V S3 ENABLE

PM_SLP_S4_L (MAKE_BASE=TRUE) → R7810 100K

R7811 5.1K; R7812 0

C7810 0.47UF 10% 6.3V CERM-X5R 402

NO STUFF C7812 0.47UF 10% 6.3V CERM-X5R 402

(PM_S4_STATE_L) → =P3V3S3_EN

P5VS3_EN → =P5VS3_EN (MAKE_BASE=TRUE)

DDRREG_EN → =DDRREG_EN (MAKE_BASE=TRUE)

S0 ENABLE

(PM_SLP_S3_L) → PM_SLP_S3_L → R7878 100

R7879 100K

PM_SLP_S3_L_R (MAKE_BASE=TRUE)

R7880 22K; R7881 33K; R7882 0; R7883 10K; R7884 0

=P5VS0_EN, =PBUSVSENS_EN

P3V3S0_EN → =P3V3S0_EN; P1V2R1V8S0_EN → =P1V2R1V8S0_EN; MCPDDR_EN → =MCPDDR_EN; CPUVTTS0_EN → =CPUVTTS0_EN; MCPCORES0_EN → =MCPCORES0_EN (MAKE_BASE=TRUE)

C7880 0.47UF; C7881 0.47UF; NO STUFF C7882 0.47UF; C7883 0.47UF; NO STUFF C7884 0.47UF (10% 6.3V CERM-X5R 402)

Unused PGOOD signal

TP_DDRREG_PGOOD → DDRREG_PGOOD (MAKE_BASE=TRUE)

Other S0 RAILS

	PM_ALL_GFX_PGOOD
IG	high
EG	PM_ALL_GPU_PGOOD

=PP3V3_S0_PWRCTL → R7892 10K

S0PGOOD_PWROK, MCPCORES0_PGOOD, CPUVTTS0_PGOOD, P1V05S0_LDO_PGOOD, P5V3V3_PGOOD → S0_PWR_PGOOD (MAKE_BASE=TRUE)

=PP3V3_S5_PWRCTL → R7894 0 → C7889 0.1UF 20% 16V CERM 402

U7880 TC7SZ08AFEAPE SOT665: PM_ALL_GPU_PGOOD, ALL_GFX_PGOOD → ALL_SYS_PWRGD

NO STUFF R7891 0

1.1V GPU ENABLE

EG_PWRSEQ_HW R7851 10K: =PP3V3_S0_PWRCTL → P1V1_GPU_EN_RC

R7850 100K: =PP3V3_S5_PWRCTL → Q7850 SSM6N15FEAPE SOT563

EG_PWRSEQ_HW R7852 0 → P1V1_GPU_EN → =P1V1GPU_EN (MAKE_BASE=TRUE)

NO STUFF C7850 0.022UF 20% 16V CERM 402

EXTGPU_PWR_EN → R7853 100K; Q7850

GPU_S0_EN_L (MAKE_BASE=TRUE) → GPUVCORE_EN_RC_L

Graphic MEM ENABLE

EG_PWRSEQ_HW R7868 100K: =PP3V3_GPU_PWRCTL, P1V8_S0GPU_EN → =P1V8FB_EN (MAKE_BASE=TRUE)

EG_PWRSEQ_HW R7869 0: GPUVCORE_PGOOD, P1V8_S0GPU_EN

Q7861 SSM6N15FEAPE SOT563

NO STUFF C7869 0.022UF 20% 16V CERM 402

G96 GPU requires rails to come up in the following order:
1) 1.1V
2) GPU_3.3V
3) GPUVcore
4) GDDR3 1.8V
BOMOPTION: EG

3.3V 1.05V AND 1.5V S0 RAILS MONITOR CIRCUIT

place XW0402 if needed to save trace space for pin 7,8

=PP3V3_S0_VMON → C7870 0.1UF 20% 16V CERM 402

U7870 ISL88042IRTEZ TDFN (APN: 353S2718, OMIT)

=PP1V5_S0_VMON → V2MON; =PP1V8_S0_VMON → V3MON; V4MON

MR* → NC; RST* → S0PGOOD_PWROK; GND_THRM_PAD

V2MON THRESHOLD IS 3.00V
V3MON THRESHOLD IS 0.6V
V4MON THRESHOLD IS 0.6V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2718	1	IC,ISL88042,4X V MONTR,2.78/2.86V,TDFN8	U7870	CRITICAL	

GPUVCORE ENABLE

EG_PWRSEQ_HW R7863 100K: =PP3V3_GPU_PWRCTL, GPUVCORE_EN_RC

EG_PWRSEQ_HW R7864 0 → GPUVCORE_EN → =GPUVCORE_EN (MAKE_BASE=TRUE)

Q7861 SSM6N15FEAPE SOT563

C7861 0.01UF 10% 16V CERM 402

GPUVCORE_EN_RC_L

EXT GPU PWRGD Pullup

=PP3V3_S0_PWRCTL → R7890 100K → P1V8FB_PGOOD → PM_ALL_GPU_PGOOD (MAKE_BASE=TRUE)

=PP3V3_S0_PWRCTL

EG_PWRSEQ_HW R7889 100K → EG_PWRSEQ_HW R7888 0 → P1V1GPU_PGOOD → P3V3GPU_EN

SYNC_MASTER=PWRSQNC SYNC_DATE=12/17/2008

PAGE TITLE: Power Control

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

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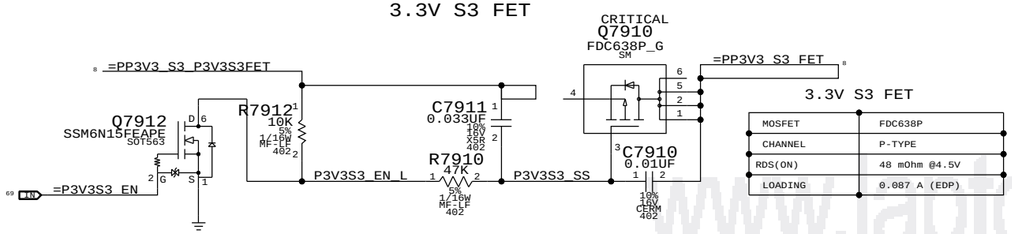
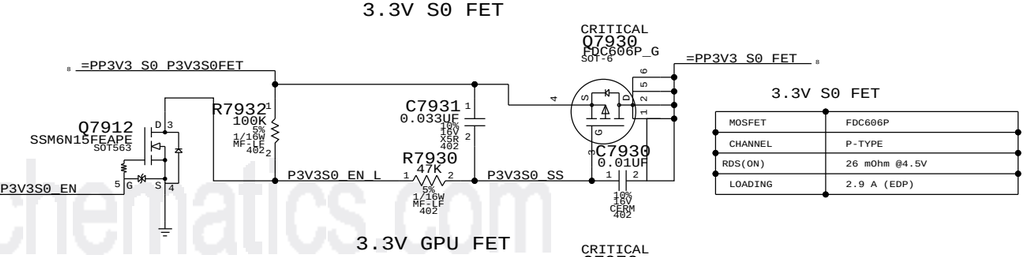
3.3V S3 FET



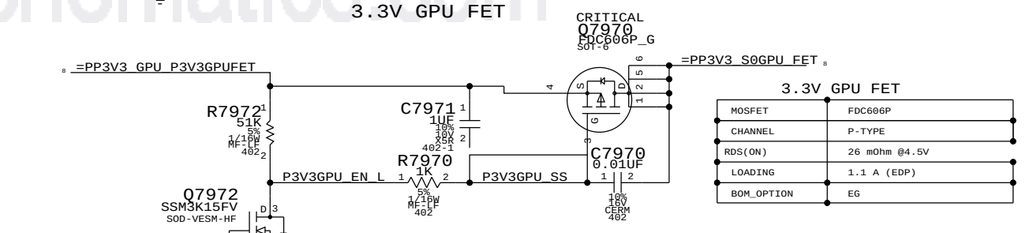
3.3V S3 FET	
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

3.3V S0 FET



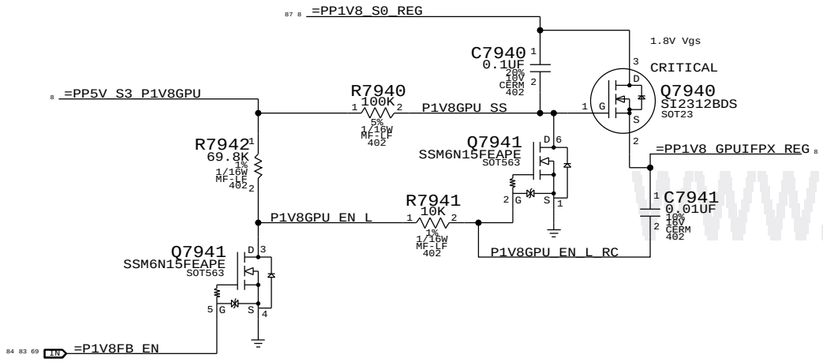
3.3V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

3.3V GPU FET

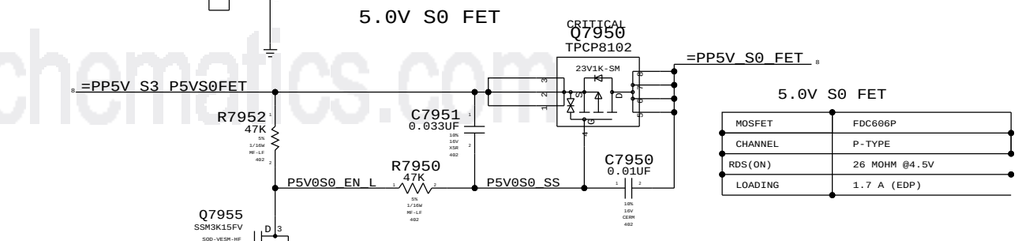


3.3V GPU FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

1.8V GPU FET

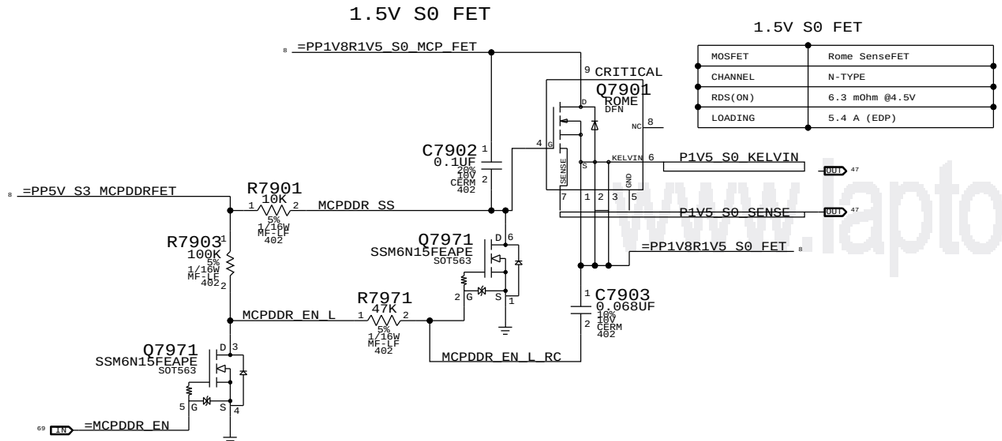


5.0V S0 FET



5.0V S0 FET	
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 MOHM @4.5V
LOADING	1.7 A (EDP)

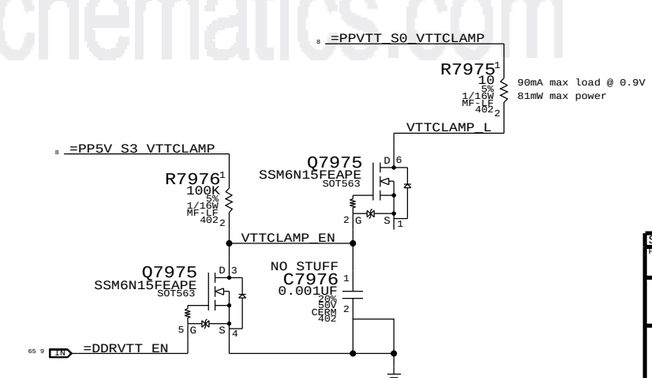
1.5V S0 FET



1.5V S0 FET	
MOSFET	Rome SenseFET
CHANNEL	N-TYPE
RDS(ON)	6.3 mOhm @4.5V
LOADING	5.4 A (EDP)

MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.



SYNC_MASTER=DDR SYNC_DATE=12/05/2008

PAGE TITLE

Power FETs

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D

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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_PEX_PLLXVDD
- =PP1V2_GPU_PEX_IOVDDQ
- =PP1V2_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V1_GPU_PEX_PLLXVDD
=PP1V1_GPU_PEX_IOVDDQ
=PP1V1_GPU_PEX_IOVDD

PEX 1.1V Current = 2A

250mA

C8002 1UF 10% 10V CERM 402
C8001 4.7UF 20% 6.3V CERM 603
C8000 22UF 20% 6.3V CERM-X5R 805
C8003 1UF 10% 10V CERM 402
C8004 0.1UF 10% 10V CERM 402
C8005 0.1UF 20% 10V CERM 402

NC_GPU_DFM
NO_TEST=TRUE

OMIT
U8000
NB9P-GS
BGA
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H32		
M7	PEX_IOVDD1	AK16
F6	PEX_IOVDD2	AK17
P7	PEX_IOVDD3	AK21
R7	PEX_IOVDD4	AK24
U7	PEX_IOVDD5	AK27
V6		
AB7		
AD6	PEX_IOVDDQ1	AG11
AF6	PEX_IOVDDQ2	AG12
AG6	PEX_IOVDDQ3	AG13
AJ5	PEX_IOVDDQ4	AG15
D35	PEX_IOVDDQ5	AG16
AK15	PEX_IOVDDQ6	AG17
AL7	PEX_IOVDDQ7	AG18
E7	PEX_IOVDDQ8	AG22
E35	PEX_IOVDDQ9	AG23
F7	PEX_IOVDDQ10	AG24
A2	PEX_IOVDDQ11	AG25
	PEX_IOVDDQ12	AG26
	PEX_IOVDDQ13	AJ14
	PEX_IOVDDQ14	AJ15
	PEX_IOVDDQ15	AJ19
	PEX_IOVDDQ16	AJ21
	PEX_IOVDDQ17	AJ22
	PEX_IOVDDQ18	AJ24
	PEX_IOVDDQ19	AJ25
	PEX_IOVDDQ20	AJ27
	PEX_IOVDDQ21	AK18
	PEX_IOVDDQ22	AK20
	PEX_IOVDDQ23	AK23
	PEX_IOVDDQ24	AK26
	PEX_IOVDDQ25	AL16
	PEX_PLLVDD	AG14
	VDD_SENSE	AD20
	GND_SENSE	AD19

1500mA

C8008 1UF 10% 10V CERM 402
C8007 4.7UF 20% 6.3V CERM 603
C8006 22UF 20% 6.3V CERM-X5R 805
C8009 1UF 10% 10V CERM 402
C8010 0.1UF 20% 10V CERM 402
C8011 0.1UF 20% 10V CERM 402

180mA

PP1V1_GPU_PEX_PLLVDD_F
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V

L8015 10NH-600MA 0603

C8017 0.1UF 20% 10V CERM 402
C8016 4.7UF 20% 6.3V CERM 603
C8015 4.7UF 20% 6.3V CERM 603

GPU_VDD_SENSE 79
GPU_GND_SENSE 79

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PEG_R2D_C_P<0>	C8020 0.1uF	PEG_R2D_P<0>	AP17	PEX_RX0
PEG_R2D_C_N<0>	C8021 0.1uF	PEG_R2D_N<0>	AN17	PEX_RX0*
PEG_R2D_C_P<1>	C8022 0.1uF	PEG_R2D_P<1>	AN19	PEX_RX1
PEG_R2D_C_N<1>	C8023 0.1uF	PEG_R2D_N<1>	AP19	PEX_RX1*
PEG_R2D_C_P<2>	C8024 0.1uF	PEG_R2D_P<2>	AR19	PEX_RX2
PEG_R2D_C_N<2>	C8025 0.1uF	PEG_R2D_N<2>	AR20	PEX_RX2*
PEG_R2D_C_P<3>	C8026 0.1uF	PEG_R2D_P<3>	AP20	PEX_RX3
PEG_R2D_C_N<3>	C8027 0.1uF	PEG_R2D_N<3>	AN20	PEX_RX3*
PEG_R2D_C_P<4>	C8028 0.1uF	PEG_R2D_P<4>	AN22	PEX_RX4
PEG_R2D_C_N<4>	C8029 0.1uF	PEG_R2D_N<4>	AP22	PEX_RX4*
PEG_R2D_C_P<5>	C8030 0.1uF	PEG_R2D_P<5>	AR22	PEX_RX5
PEG_R2D_C_N<5>	C8031 0.1uF	PEG_R2D_N<5>	AR23	PEX_RX5*
PEG_R2D_C_P<6>	C8032 0.1uF	PEG_R2D_P<6>	AP23	PEX_RX6
PEG_R2D_C_N<6>	C8033 0.1uF	PEG_R2D_N<6>	AN23	PEX_RX6*
PEG_R2D_C_P<7>	C8034 0.1uF	PEG_R2D_P<7>	AN25	PEX_RX7
PEG_R2D_C_N<7>	C8035 0.1uF	PEG_R2D_N<7>	AP25	PEX_RX7*
PEG_R2D_C_P<8>	C8036 0.1uF	PEG_R2D_P<8>	AR25	PEX_RX8
PEG_R2D_C_N<8>	C8037 0.1uF	PEG_R2D_N<8>	AR26	PEX_RX8*
PEG_R2D_C_P<9>	C8038 0.1uF	PEG_R2D_P<9>	AP26	PEX_RX9
PEG_R2D_C_N<9>	C8039 0.1uF	PEG_R2D_N<9>	AN26	PEX_RX9*
PEG_R2D_C_P<10>	C8040 0.1uF	PEG_R2D_P<10>	AN28	PEX_RX10
PEG_R2D_C_N<10>	C8041 0.1uF	PEG_R2D_N<10>	AP28	PEX_RX10*
PEG_R2D_C_P<11>	C8042 0.1uF	PEG_R2D_P<11>	AR28	PEX_RX11
PEG_R2D_C_N<11>	C8043 0.1uF	PEG_R2D_N<11>	AR29	PEX_RX11*
PEG_R2D_C_P<12>	C8044 0.1uF	PEG_R2D_P<12>	AP29	PEX_RX12
PEG_R2D_C_N<12>	C8045 0.1uF	PEG_R2D_N<12>	AN29	PEX_RX12*
PEG_R2D_C_P<13>	C8046 0.1uF	PEG_R2D_P<13>	AN31	PEX_RX13
PEG_R2D_C_N<13>	C8047 0.1uF	PEG_R2D_N<13>	AP31	PEX_RX13*
PEG_R2D_C_P<14>	C8048 0.1uF	PEG_R2D_P<14>	AR31	PEX_RX14
PEG_R2D_C_N<14>	C8049 0.1uF	PEG_R2D_N<14>	AR32	PEX_RX14*
PEG_R2D_C_P<15>	C8050 0.1uF	PEG_R2D_P<15>	AR34	PEX_RX15
PEG_R2D_C_N<15>	C8051 0.1uF	PEG_R2D_N<15>	AP34	PEX_RX15*
PEG_CLK100M_P			AR16	PEX_REFCLK
PEG_CLK100M_N			AR17	PEX_REFCLK*
GPU_RESET_L	R8020 0 5% 1/16W MF-LF 402	GPU_RESET_R_L	AM16	PEX_RST*
		TP_PEX_CLKREQ_L	AR13	PEX_CLKREQ*

PEX_TX0	AL17	PEG_D2R_C_P<0>	C8055 0.1uF	PEG_D2R_P<0>
PEX_TX0*	AM17	PEG_D2R_C_N<0>	C8056 0.1uF	PEG_D2R_N<0>
PEX_TX1	AM18	PEG_D2R_C_P<1>	C8057 0.1uF	PEG_D2R_P<1>
PEX_TX1*	AM19	PEG_D2R_C_N<1>	C8058 0.1uF	PEG_D2R_N<1>
PEX_TX2	AL19	PEG_D2R_C_P<2>	C8059 0.1uF	PEG_D2R_P<2>
PEX_TX2*	AK19	PEG_D2R_C_N<2>	C8060 0.1uF	PEG_D2R_N<2>
PEX_TX3	AL20	PEG_D2R_C_P<3>	C8061 0.1uF	PEG_D2R_P<3>
PEX_TX3*	AM20	PEG_D2R_C_N<3>	C8062 0.1uF	PEG_D2R_N<3>
PEX_TX4	AM21	PEG_D2R_C_P<4>	C8063 0.1uF	PEG_D2R_P<4>
PEX_TX4*	AM22	PEG_D2R_C_N<4>	C8064 0.1uF	PEG_D2R_N<4>
PEX_TX5	AL22	PEG_D2R_C_P<5>	C8065 0.1uF	PEG_D2R_P<5>
PEX_TX5*	AK22	PEG_D2R_C_N<5>	C8066 0.1uF	PEG_D2R_N<5>
PEX_TX6	AL23	PEG_D2R_C_P<6>	C8067 0.1uF	PEG_D2R_P<6>
PEX_TX6*	AM23	PEG_D2R_C_N<6>	C8068 0.1uF	PEG_D2R_N<6>
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PEX_TX7*	AM25	PEG_D2R_C_N<7>	C8070 0.1uF	PEG_D2R_N<7>
PEX_TX8	AL25	PEG_D2R_C_P<8>	C8071 0.1uF	PEG_D2R_P<8>
PEX_TX8*	AK25	PEG_D2R_C_N<8>	C8072 0.1uF	PEG_D2R_N<8>
PEX_TX9	AL26	PEG_D2R_C_P<9>	C8073 0.1uF	PEG_D2R_P<9>
PEX_TX9*	AM26	PEG_D2R_C_N<9>	C8074 0.1uF	PEG_D2R_N<9>
PEX_TX10	AM27	PEG_D2R_C_P<10>	C8075 0.1uF	PEG_D2R_P<10>
PEX_TX10*	AM28	PEG_D2R_C_N<10>	C8076 0.1uF	PEG_D2R_N<10>
PEX_TX11	AL28	PEG_D2R_C_P<11>	C8077 0.1uF	PEG_D2R_P<11>
PEX_TX11*	AK28	PEG_D2R_C_N<11>	C8078 0.1uF	PEG_D2R_N<11>
PEX_TX12	AK29	PEG_D2R_C_P<12>	C8079 0.1uF	PEG_D2R_P<12>
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PEX_TX13*	AM30	PEG_D2R_C_N<13>	C8082 0.1uF	PEG_D2R_N<13>
PEX_TX14	AM31	PEG_D2R_C_P<14>	C8083 0.1uF	PEG_D2R_P<14>
PEX_TX14*	AM32	PEG_D2R_C_N<14>	C8084 0.1uF	PEG_D2R_N<14>
PEX_TX15	AN32	PEG_D2R_C_P<15>	C8085 0.1uF	PEG_D2R_P<15>
PEX_TX15*	AP32	PEG_D2R_C_N<15>	C8086 0.1uF	PEG_D2R_N<15>
PEX_TSTCLK_OUT	AJ17	PEX_TSTCLK_P	R8060 200 1% 1/16W MF-LF 402	
PEX_TSTCLK_OUT*	AJ18	PEX_TSTCLK_N		
PEX_TERMP	AG21	PEX_TERMP_PD	R8050 2.49K 1% 1/16W MF-LF 402	
PEX_RFU1	AG19	XNC		
PEX_RFU2	AG20	XNC		

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

PAGE TITLE: NV G96 PCI-E

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 80 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PPVCORE_GPU
- =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

8 =PPVCORE_GPU

???A @ ???/???MHz Core/Mem Clk for VDD

C8100 4.7UF 20% 6.3V X5R-CERM 402
C8101 4.7UF 20% 6.3V X5R-CERM 402
C8102 4.7UF 20% 6.3V X5R-CERM 402

C8103 0.47UF 10% 6.3V CERM-X5R 402
C8104 0.47UF 10% 6.3V CERM-X5R 402
C8105 0.47UF 10% 6.3V CERM-X5R 402
C8106 0.47UF 10% 6.3V CERM-X5R 402
C8107 0.47UF 10% 6.3V CERM-X5R 402

C8108 0.47UF 10% 6.3V CERM-X5R 402
C8109 0.47UF 10% 6.3V CERM-X5R 402
C8110 0.47UF 10% 6.3V CERM-X5R 402
C8111 0.47UF 10% 6.3V CERM-X5R 402
C8112 0.47UF 10% 6.3V CERM-X5R 402

C8113 0.1UF 20% 10V CERM 402
C8114 0.1UF 20% 10V CERM 402
C8115 0.1UF 20% 10V CERM 402
C8116 0.1UF 20% 10V CERM 402
C8117 0.1UF 20% 10V CERM 402

C8118 0.1UF 20% 10V CERM 402
C8119 0.1UF 20% 10V CERM 402
C8120 0.1UF 20% 10V CERM 402
C8121 0.1UF 20% 10V CERM 402
C8122 0.1UF 20% 10V CERM 402

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VDD: L11 L12 L13 L14 L15 L16 L17 L18 L19 L20 L21 L22 L23 L24 L25 M12 M14 M16 M18 M20 M22 M24 P11 P13 P15 P17 P19 P21 P23 P25 R11 R12 R13 R14 R15 R16 R17 R18 R19 R20 R21 R22 R23 R24 R25 T12 T14 T16 T18 T20 T22 T24 V11 V13 V15 V17

VDD: V19 V21 V23 V25 W11 W12 W13 W14 W15 W16 W17 W18 W19 AD24 W21 W22 W23 W24 W25 Y12 Y14 Y16 Y18 Y20 Y22 Y24 AB11 AB13 AB15 AB17 AB19 AB21 AB23 AB25 AC11 AC12 AC13 AC14 AC15 AC16 AC17 AC18 AC19 AC20 AC21 AC22 AC23 AC24 AC25 AD12 AD14 AD16 AD18 AD22 W20

U8000
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GND: B3 B6 B9 B12 B15 B21 B24 B27 B30 B33 C2 C34 E6 E9 E12 E15 E18 E24 E27 E30 F2 F5 F31 F34 J2 J5 J31 J34 L9 M2 M5 M11 M13 M15 M17 M19 M21 M23 M25 M31 M34 N11 N12 N13 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N25 P12 P14 P16 P18 P20 P22 P24 R2 R5 R31 R34 T11 T13 T15 T17 T19 T21 T23 T25 U11 U12 U13 U14 U15 U16 U17 U18 U19 U20 U21 U22 U23 U24 U25 V2 V5 V9 V12 V14 V16

GND: V18 V20 V22 V24 V31 Y11 Y13 Y15 Y17 Y19 Y21 Y23 Y25 AA2 AA5 AA11 AA12 AA13 AA14 AA15 AA16 AA17 AA18 AA19 AA20 AA21 AA22 AA23 AA24 AA25 AA34 AB12 AB14 AB16 AB18 AB20 AB22 AB24 AC9 AD2 AD5 AD11 AD13 AD15 AD17 AD21 AD23 AD25 AD31 AD34 AE11 AE12 AE13 AE14 AE15 AE16 AE17 AE18 AE19 AE20 AE21 AE22 AE23 AE24 AE25 AG2 AG5 AG31 AG34 AK2 AK5 AP33 AK31 AK34 AL6 AL9 AL12 AL15 AL18 AL21 AL24 AL27 AL30 AN2 AN34 AP3 AP6 AP9 AP12 AP15 AP18 AP21 AP24 AP27 AP30

8 =PP1V8_GPU_FBVDDQ

Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF

???A @ ???MHz 1.8V GDDR3

C8150 4.7UF 20% 6.3V CERM 603
C8151 4.7UF 20% 6.3V CERM 603

C8156 0.1UF 20% 10V CERM 402
C8157 0.1UF 20% 10V CERM 402
C8158 0.1UF 20% 10V CERM 402
C8159 0.1UF 20% 10V CERM 402
C8160 0.47UF 10% 6.3V CERM-X5R 402
C8161 0.47UF 10% 6.3V CERM-X5R 402

C8162 0.1UF 20% 10V CERM 402
C8163 0.1UF 20% 10V CERM 402
C8164 0.1UF 20% 10V CERM 402
C8165 0.1UF 20% 10V CERM 402
C8166 0.47UF 10% 6.3V CERM-X5R 402
C8167 0.47UF 10% 6.3V CERM-X5R 402

C8168 0.47UF 10% 6.3V CERM-X5R 402
C8169 0.47UF 10% 6.3V CERM-X5R 402
C8170 0.47UF 10% 6.3V CERM-X5R 402
C8171 0.47UF 10% 6.3V CERM-X5R 402

OMIT

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FBVDDQ: B18 J17 U27 AB27 AB29 AC27 AD27 AE27 AJ28 E21 G8 G9 G17 G18 G22 H29 J14 J15 J16

FBVDDQ: J20 J21 J22 J23 J24 J29 N27 P27 R27 T27 U29 V27 V29 V34 W27 Y27 AA27 AA29 AA31

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

PAGE TITLE
NV G96 Core/FB Power

Apple Inc.

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SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8000
NB9P-GS
BGA
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OMIT
U8000
NB9P-GS
BGA
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PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

PLACEMENT_NOTE=Place close to U8000.

GPU_FB_VREF

NO STUFF

GPU_FB_VREF_UNTERM_L
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

NO STUFF

SYNC_MASTER=MUXGFX	SYNC_DATE=07/10/2008
PAGE TITLE	NV G96 Frame Buffer I/F
Apple Inc.	DRAWING NUMBER 051-7892 · SIZE D
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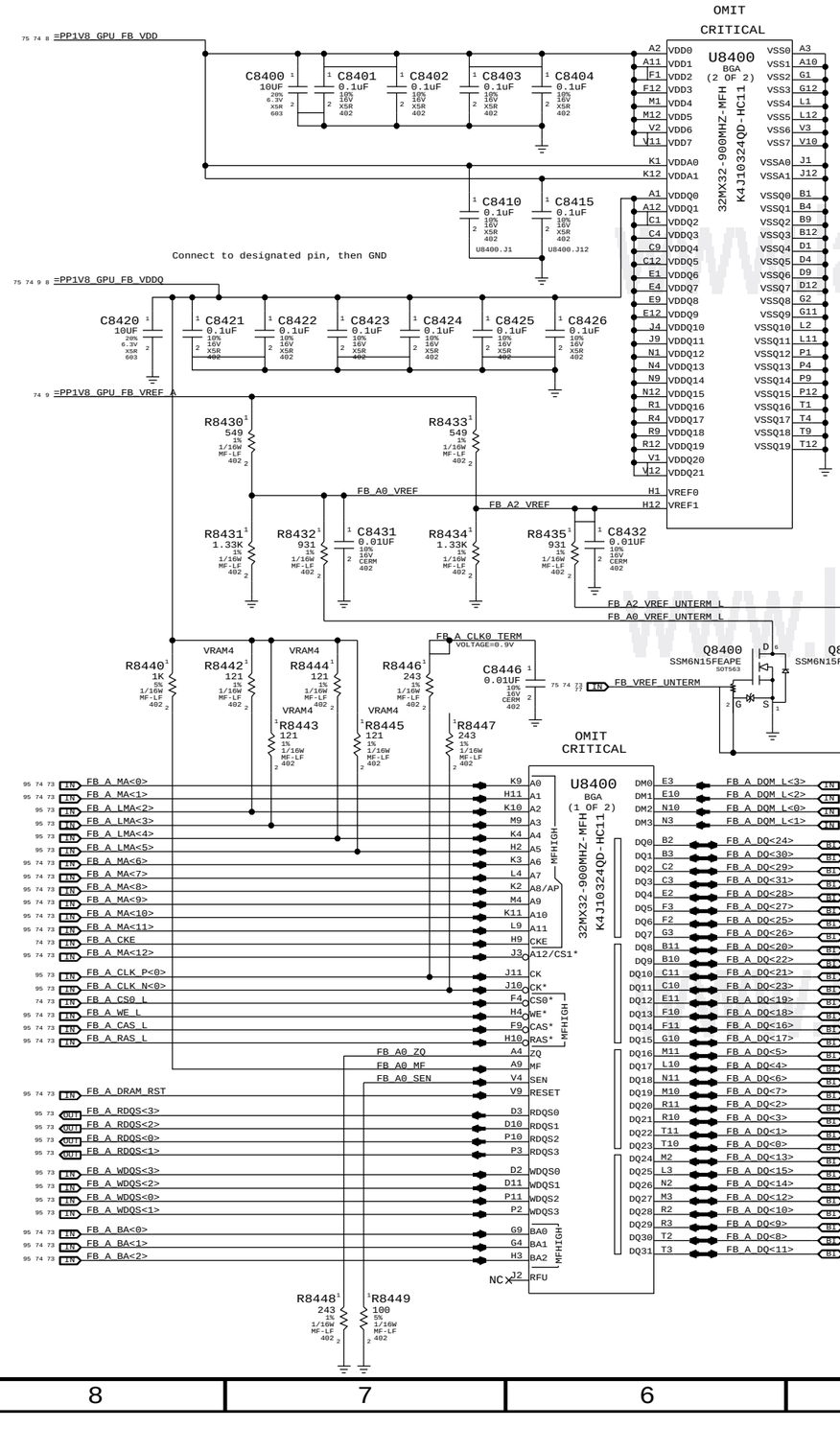
Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREFA

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4



SYNC MASTER=MUXGFX SYNC DATE=07/10/2008

PAGE TITLE
GDDR3 Frame Buffer A (Top)

Apple Inc.

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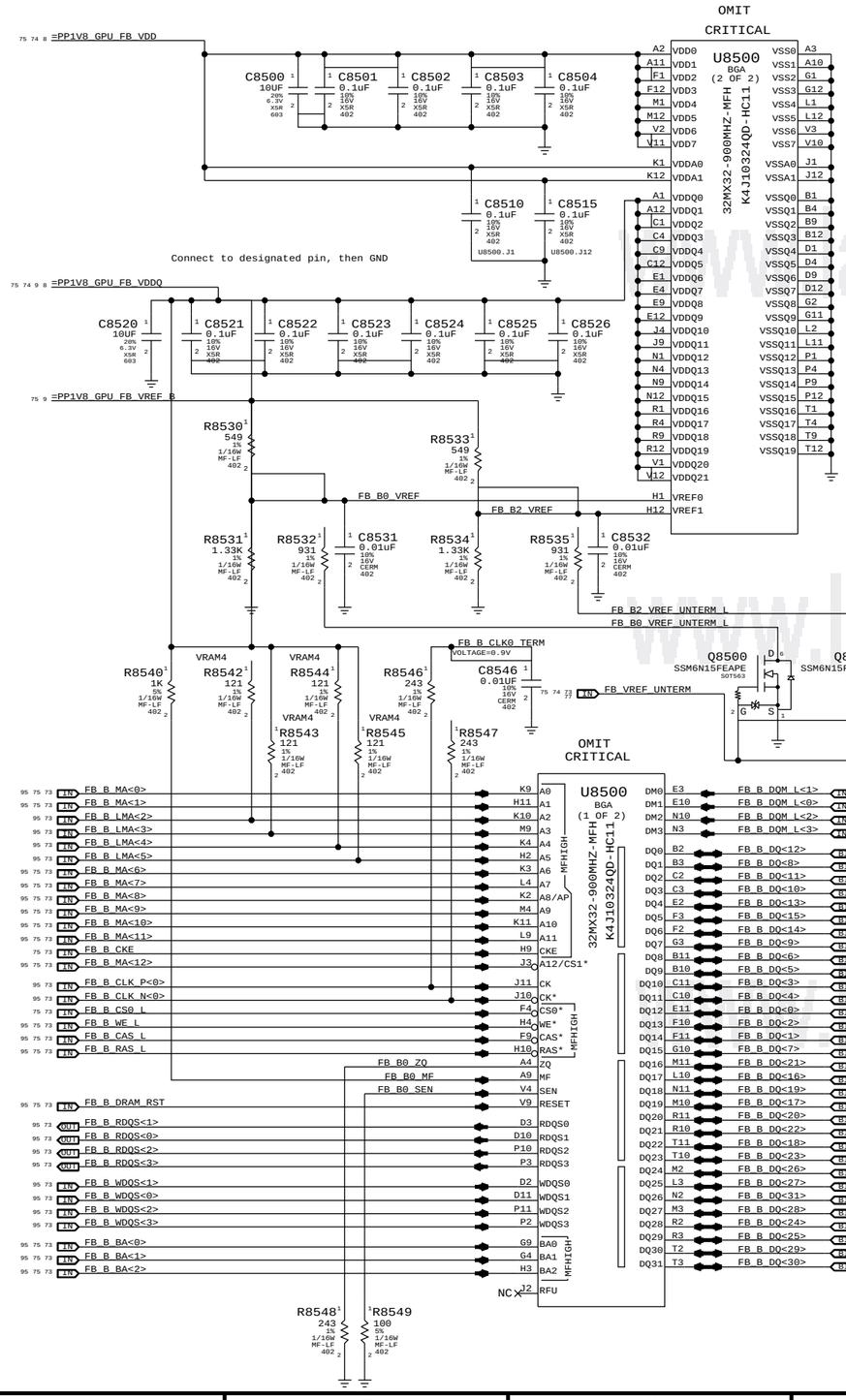

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VREF_B

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
VRAM4

SYNC MASTER=MUXGFX SYNC DATE=07/10/2008

PAGE TITLE
GDDR3 Frame Buffer B (Top)

Apple Inc.

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Page Notes

Power aliases required by this page:
- =PP3V3_GPU_VDD33
- =PP3V3_GPI_MIO
- =PP1V2_GPU_PLLVDD
- =PP1V2_GPU_H_PLLVDD
- =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

110mA
=PP3V3_GPU_VDD33

C8690 0.022UF 10% 16V CERM-X5R 402
C8692 0.022UF 10% 16V CERM-X5R 402
C8694 0.1UF 20% 10V CERM 402
C8696 0.47UF 10% 6.3V CERM-X5R 402
C8698 1UF 10% 6.3V CERM 402
C8691 0.022UF 10% 16V CERM-X5R 402
C8693 0.022UF 10% 16V CERM-X5R 402
C8695 0.1UF 20% 10V CERM 402
C8697 0.47UF 10% 6.3V CERM-X5R 402

=PP3V3_GPU_VDD33
Typically <??mA
C8600 0.47UF 10% 6.3V CERM-X5R 402
C8601 0.47UF 10% 6.3V CERM-X5R 402
C8602 0.47UF 10% 6.3V CERM-X5R 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 6 OF 9

J9 VDD33_1
J10 VDD33_2
J11 VDD33_3
J12 VDD33_4
J13 VDD33_5

J25 NCX RFU0
J26 NCX RFU1
AK14 RFU0_GND
K9 RFU1_GND

GPU_ROM_CS_L → C3 ROM_CS*
GPU_ROM_SCLK → D4 ROM_SCLK
GPU_ROM_SI → D3 ROM_SI
GPU_ROM_SO → C4 ROM_SO

R8696 40.2K 1% 1/16W MF-LF 402
R8697 40.2K 1% 1/16W MF-LF 402

GPU_STRAP_REF_3V3_PD → N9 STRAP_REF_3V3
GPU_STRAP_REF_MIOB_PD → M9 STRAP_REF_MIOB (IPD)

=PP3V3_GPU_MIO

R8620 49.9 1% 1/16W MF-LF 402
R8621 49.9 1% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ
GPU_MIOB_PD_VDDQ
GPU_MIOA_PU_GND
GPU_MIOB_PU_GND
R8622 49.9 1% 1/16W MF-LF 402
R8623 49.9 1% 1/16W MF-LF 402

C8610 1UF 10% 6.3V CERM 402
C8611 1UF 10% 6.3V CERM 402

P9 MIOA_VDDQ_1
R9 MIOA_VDDQ_2
T9 MIOA_VDDQ_3
U9 MIOA_VDDQ_4
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4

R8616 10K 5% 1/16W MF-LF 402
R8618 10K 5% 1/16W MF-LF 402
GPU_TESTMODE_PD → AP35 TESTMODE
GPU_MIOA_VREF → N5 MIOA_VREF
GPU_MIOB_VREF → AF1 MIOB_VREF
R8617 10K 5% 1/16W MF-LF 402
C8617 0.1UF 10% 16V X5R 402
R8619 10K 5% 1/16W MF-LF 402
C8619 0.1UF 10% 16V X5R 402
R8660 10K 5% 1/16W MF-LF 402
GPU_MIOA_PD_VDDQ → U5 MIOA_CAL_PD_VDDQ
GPU_MIOA_PU_GND → T5 MIOA_CAL_PU_GND
GPU_MIOB_PD_VDDQ → AA7 MIOB_CAL_PD_VDDQ
GPU_MIOB_PU_GND → AA6 MIOB_CAL_PU_GND

=PP1V1_GPU_PLLVDD
L8630 FERR-220-OHM 0402
PP1V1_GPU_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
65mA
C8633 4.7UF 20% 6.3V CERM 603
C8630 4.7UF 20% 6.3V CERM 603
C8631 0.1uF 10% 16V X5R 402

=PP1V1_GPU_H_PLLVDD
L8635 FERR-220-OHM 0402
PP1V1_GPU_H_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
25mA
C8637 4.7UF 20% 6.3V CERM 603
C8635 4.7UF 20% 6.3V CERM 603
C8636 0.1uF 10% 16V X5R 402

=PP1V1_GPU_VID_PLLVDD
L8640 FERR-220-OHM 0402
PP1V1_GPU_VID_PLLVDD_F MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm VOLTAGE=1.2V
50mA
C8643 4.7UF 20% 6.3V CERM 603
C8640 4.7UF 20% 6.3V CERM 603
C8641 0.1uF 10% 16V X5R 402

AF9 SP_PLLVDD
AE9 PLLVDD
AD9 VID_PLLVDD

GPU_XTALIN (IN) → B1 XTAL_IN
GPU_XTALOUT (OUT) → B2 XTAL_OUT
GPU_XTALOUTBUFF (OUT) → D1 XTAL_OUTBUFF
GPU_XTALSSIN (IN) → D2 XTAL_SSIN

GPIO0 K1 GPU_GPIO_0 (BI)
GPIO1 K2 GPU_GPIO_1 (BI)
GPIO2 K3 GPU_GPIO_2 (BI)
GPIO3 H3 GPU_GPIO_3 (BI)
GPIO4 H2 GPU_GPIO_4 (BI)
GPIO5 H1 GPU_GPIO_5 (BI)
GPIO6 H4 GPU_GPIO_6 (BI)
GPIO7 H5 GPU_GPIO_7 (BI)
GPIO8 H6 GPU_GPIO_8 (BI)
GPIO9 J7 GPU_GPIO_9 (BI)
GPIO10 K4 GPU_GPIO_10 (BI)
GPIO11 K5 GPU_GPIO_11 (BI)
GPIO12 H7 GPU_GPIO_12 (BI)
GPIO13 J4 GPU_GPIO_13 (BI)
GPIO14 J6 GPU_GPIO_14 (BI)
GPIO15 L1 GPU_GPIO_15 (BI)
GPIO16 L2 GPU_GPIO_16 (BI)
GPIO17 L4 GPU_GPIO_17 (BI)
GPIO18 M4 GPU_GPIO_18 (BI)
GPIO19 L7 GPU_GPIO_19 (BI)
GPIO20 L5 GPU_GPIO_20 (BI)
GPIO21 K6 GPU_GPIO_21 (BI)
GPIO22 L6 GPU_GPIO_22 (BI)
GPIO23 M6 GPU_GPIO_23 (BI)

HDA_SDI C7 GPU_HDA_SDI (OUT)
HDA_SDO B7 GPU_HDA_SDO (OUT)
HDA_SYNC A7 GPU_HDA_SYNC (OUT)
HDA_BCLK D7 GPU_HDA_BCLK (OUT)
HDA_RST* D6 GPU_HDA_RST_L (OUT)
SPDIF A5 GPU_SPDIF (IN)
BUFRST* A4 TP_GPU_BUFRST_L (OUT)

JTAG_TCK AP14 GPU_JTAG_TCK (IN)
JTAG_TDI AN14 GPU_JTAG_TDI (IN)
JTAG_TDO AN16 GPU_JTAG_TDO (OUT)
JTAG_TMS AR14 GPU_JTAG_TMS (IN)
JTAG_TRST* AP16 GPU_JTAG_TRST_L (IN)

MIOA_CLKIN N4 GPU_MIOA_CLKIN (IN)
MIOA_CLKOUT R4 GPU_MIOA_CLKOUT_P (BI)
MIOA_CLKOUT* T4 GPU_MIOA_CLKOUT_N (BI)
MIOA_CTL3 P5 GPU_MIOA_CTL3 (BI)
MIOA_DE N2 GPU_MIOA_DE (BI)
MIOA_D0 N1 GPU_MIOA_D<0> (BI)
MIOA_D1 P4 GPU_MIOA_D<1> (BI)
MIOA_D2 P1 GPU_MIOA_D<2> (BI)
MIOA_D3 P2 GPU_MIOA_D<3> (BI)
MIOA_D4 P3 GPU_MIOA_D<4> (BI)
MIOA_D5 T3 GPU_MIOA_D<5> (BI)
MIOA_D6 T2 GPU_MIOA_D<6> (BI)
MIOA_D7 T1 GPU_MIOA_D<7> (BI)
MIOA_D8 U4 GPU_MIOA_D<8> (BI)
MIOA_D9 U1 GPU_MIOA_D<9> (BI)
MIOA_D10 U2 GPU_MIOA_D<10> (BI)
MIOA_D11 U3 GPU_MIOA_D<11> (BI)
MIOA_D12 R6 GPU_MIOA_D<12> (BI)
MIOA_D13 T6 GPU_MIOA_D<13> (BI)
MIOA_D14 N6 GPU_MIOA_D<14> (BI)
MIOA_HSYNC N3 GPU_MIOA_HSYNC (BI)
MIOA_VSYNC L3 GPU_MIOA_VSYNC (BI)

MIOB_CLKIN AE1 GPU_MIOB_CLKIN (IN)
MIOB_CLKOUT V4 GPU_MIOB_CLKOUT_P (BI)
MIOB_CLKOUT* W4 GPU_MIOB_CLKOUT_N (BI)
MIOB_CTL3 W3 GPU_MIOB_CTL3 (BI)
MIOB_DE Y5 GPU_MIOB_DE (BI)
MIOB_D0 Y1 GPU_MIOB_D<0> (BI)
MIOB_D1 Y2 GPU_MIOB_D<1> (BI)
MIOB_D2 Y3 GPU_MIOB_D<2> (BI)
MIOB_D3 AB3 GPU_MIOB_D<3> (BI)
MIOB_D4 AB2 GPU_MIOB_D<4> (BI)
MIOB_D5 AB1 GPU_MIOB_D<5> (BI)
MIOB_D6 AC4 GPU_MIOB_D<6> (BI)
MIOB_D7 AC1 GPU_MIOB_D<7> (BI)
MIOB_D8 AC2 GPU_MIOB_D<8> (BI)
MIOB_D9 AC3 GPU_MIOB_D<9> (BI)
MIOB_D10 AE3 GPU_MIOB_D<10> (BI)
MIOB_D11 AE2 GPU_MIOB_D<11> (BI)
MIOB_D12 U6 GPU_MIOB_D<12> (BI)
MIOB_D13 W6 GPU_MIOB_D<13> (BI)
MIOB_D14 Y6 GPU_MIOB_D<14> (BI)
MIOB_D15 W5 GPU_STRAP<0> (BI)
MIOB_D16 W7 GPU_STRAP<1> (BI)
MIOB_D17 V7 GPU_STRAP<2> (BI)
MIOB_HSYNC W1 GPU_MIOB_HSYNC (BI)
MIOB_VSYNC W2 GPU_MIOB_VSYNC (BI)

THERMDP B5 GPU_THERMD_P (IN)
THERMDN B4 GPU_THERMD_N (OUT)
PGOOD_OUT* C5 TP_GPU_PGOOD_OUT_L (OUT)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008
PAGE TITLE: NV G96 GPIO/MIO/Misc
Apple Inc.
DRAWING NUMBER: 051-7892
SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 86 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

GPIOs

Native Func

GPU_GPIO_0	GP	NC_GPU_GPIO_0	MAKE_BASE=TRUE
GPU_GPIO_1	HPDC	DP_EG_HPD	MAKE_BASE=TRUE
GPU_GPIO_2	LCD0_BL_PWM	TP_LVDS_EG_BKL_PWM	MAKE_BASE=TRUE
GPU_GPIO_3	LCD0_VDD	EG_LCD_PWR_EN	MAKE_BASE=TRUE
GPU_GPIO_4	LCD0_BL_EN	EG_BKLT_EN	MAKE_BASE=TRUE
GPU_GPIO_5	VID0	TP_GPU_GSTATE<0>	MAKE_BASE=TRUE
GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	MAKE_BASE=TRUE
GPU_GPIO_7	VID2/MEM_VID	GPIO7_FBVDD_ALTVO	MAKE_BASE=TRUE
GPU_GPIO_8	THERM	SMC_GFX_OVERTEMP_R_L	MAKE_BASE=TRUE
GPU_GPIO_9	FAN_PWM	SMC_GFX_THROTTLE_R_L	MAKE_BASE=TRUE
GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	MAKE_BASE=TRUE
GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID0	MAKE_BASE=TRUE
GPU_GPIO_12	AC_DET	GPU_VCORE_VID1	MAKE_BASE=TRUE
GPU_GPIO_13	PWR_CTL0	GPU_VCORE_VID2	MAKE_BASE=TRUE
GPU_GPIO_14	PWR_CTL1	TP_GPU_VCORE_VID3	MAKE_BASE=TRUE

GPIOs

Native Func

GPU_GPIO_15	HPDE	NC_GPU_GPIO_15	MAKE_BASE=TRUE
GPU_GPIO_16	DVI_MODE0	EG_DP_CA_DET	
GPU_GPIO_17	HDMI_DETECT0	NC_GPU_GPIO_17	MAKE_BASE=TRUE
GPU_GPIO_18	DVI_MODE1	NC_GPU_GPIO_18	MAKE_BASE=TRUE
GPU_GPIO_19	HDMI_DETECT1	NC_GPU_GPIO_19	MAKE_BASE=TRUE
GPU_GPIO_20	HPDD	NC_GPU_GPIO_20	MAKE_BASE=TRUE
GPU_GPIO_21	HPDF	NC_GPU_GPIO_21	MAKE_BASE=TRUE
GPU_GPIO_22	SWAPRDY_A	NC_GPU_GPIO_22	MAKE_BASE=TRUE
GPU_GPIO_23	GP	NC_GPU_GPIO_23	MAKE_BASE=TRUE NO_TEST=TRUE

Renamed signals

GPU_XTALOUT	GPU_XTALOUT	MAKE_BASE=TRUE
GPU_CLK27M	GPU_XTALIN	MAKE_BASE=TRUE
GPU_CLK27M_SS	GPU_XTALSSIN	MAKE_BASE=TRUE
GPU_TDIODE_P	GPU_THERMD_P	MAKE_BASE=TRUE
GPU_TDIODE_N	GPU_THERMD_N	MAKE_BASE=TRUE

Unused signals

NC_GPU_SPDIF	GPU_SPDIF	MAKE_BASE=TRUE NO_TEST=TRUE
NC_CPU_HDA_SDI	GPU_HDA_SDI	MAKE_BASE=TRUE NO_TEST=TRUE
NC_CPU_HDA_SDO	GPU_HDA_SDO	MAKE_BASE=TRUE NO_TEST=TRUE
NC_CPU_HDA_SYNC	GPU_HDA_SYNC	MAKE_BASE=TRUE NO_TEST=TRUE
NC_CPU_HDA_BCLK	GPU_HDA_BCLK	MAKE_BASE=TRUE NO_TEST=TRUE
NC_CPU_HDA_RST_L	GPU_HDA_RST_L	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBA_MA<13>	FB_A_MA<13>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBB_MA<13>	FB_B_MA<13>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBA_CMD28	TP_FBA_CMD28	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBC_CMD28	TP_FBC_CMD28	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBA_CMD29	TP_FBA_CMD29	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBC_CMD29	TP_FBC_CMD29	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBA_CMD30	TP_FBA_CMD30	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FBC_CMD30	TP_FBC_CMD30	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_ROM_CS_L	GPU_ROM_CS_L	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FB_A_CS1_L	FB_A_CS1_L	MAKE_BASE=TRUE NO_TEST=TRUE
NC_FB_B_CS1_L	FB_B_CS1_L	MAKE_BASE=TRUE NO_TEST=TRUE

Unused I2C Buses

LVDS_EG_DDC_CLK	GPU_I2CA_SCL	MAKE_BASE=TRUE
LVDS_EG_DDC_DATA	GPU_I2CA_SDA	MAKE_BASE=TRUE
DP_EG_DDC_CLK	GPU_I2CB_SCL	MAKE_BASE=TRUE
DP_EG_DDC_DATA	GPU_I2CB_SDA	MAKE_BASE=TRUE
NC_GPU_I2CC_SCL	GPU_I2CC_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_I2CC_SDA	GPU_I2CC_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_I2CD_SCL	GPU_I2CD_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_I2CD_SDA	GPU_I2CD_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_I2CE_SCL	GPU_I2CE_SCL	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_I2CE_SDA	GPU_I2CE_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_I2CH_SCL	GPU_I2CH_SDA	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_I2CH_SDA	GPU_I2CH_SCL	MAKE_BASE=TRUE NO_TEST=TRUE

I2CS ties into SMBus connection page
(I2CS requires pullups even if not used)

TP_LVDS_EG_B_CLK_P	LVDS_EG_B_CLK_P	MAKE_BASE=TRUE
TP_LVDS_EG_B_CLK_N	LVDS_EG_B_CLK_N	MAKE_BASE=TRUE
NC_LVDS_EG_A_DATA_P<3>	LVDS_EG_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_A_DATA_N<3>	LVDS_EG_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_DATA_P<3>	LVDS_EG_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_LVDS_EG_B_DATA_N<3>	LVDS_EG_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE

Config Straps

=PP3V3_GPU_MIO

	OMIT	NO STUFF	NO STUFF
	R8707[1] 2.0K 5% 1/16W MF-LF 402	R8709[1] 4.99K 1% 1/16W MF-LF 402	R8711[1] 4.99K 1% 1/16W MF-LF 402
GPU_ROM_SI	OMIT		
GPU_ROM_SO	PU		
GPU_ROM_SCLK	PU		
	OMIT	NO STUFF	NO STUFF
	R8708[1] 45.3K 1% 1/16W MF-LF 402	R8710[1] 2.0K 5% 1/16W MF-LF 402	R8712[1] 15.0K 1% 1/16W MF-LF 402

Physical Strapping Pin

	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

Strap S1/S2 Bit[3:0] PU/PD Rval
0 0000 PD 5k
1 0001 PD 10k
2 0010 PD 15k
3 0011 PD 20k
4 0100 PD 25k
5 0101 PD 30k
6 0110 PD 35k
7 0111 PD 45k

Strap S1/S2 Bit[3:0] PU/PD Rval
8 1000 PU 5k
9 1001 PU 10k
A 1010 PU 15k
B 1011 PU 20k
C 1100 PU 25k
D 1101 PU 30k
E 1110 PU 35k
F 1111 PU 45k

=PP3V3_GPU_MIO

	NO STUFF	NO STUFF	
	R8701[1] 45.3K 1% 1/16W MF-LF 402	R8703[1] 10K 1% 1/16W MF-LF 402	R8705[1] 10K 1% 1/16W MF-LF 402
GPU_STRAP<0>	PD		
GPU_STRAP<1>	PD		
GPU_STRAP<2>	PD		
	NO STUFF		
	R8702[1] 2.0K 5% 1/16W MF-LF 402	R8704[1] 10K 1% 1/16W MF-LF 402	R8706[1] 45.3K 1% 1/16W MF-LF 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0368	1	RES,MTL FILM,1/16W,35.7K,1,0402,SMD,LF	R8708		VRAM_512_HYNIX
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES,MTL FILM,1/16W,20.0K,1,0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES,MTL FILM,1/16W,15.0K,1,0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES,MTL FILM,1/16W,45.3K,1,0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES,MTL FILM,1/16W,30.1K,1,0402,SMD,LF	R8707		VRAM_1024_QIMONDA

=PP3V3_S0_DDC_LCD
=PP3V3_GPU_VDD33

	R8750[1] 4.7K 5% 1/16W MF-LF 402	R8751[1] 4.7K 5% 1/16W MF-LF 402
DP_EG_DDC_CLK	IN	
DP_EG_DDC_DATA	IN	
DP_IG_DDC_CLK	IN	
DP_IG_DDC_DATA	IN	

	R8752[1] 4.7K 5% 1/16W MF-LF 402	R8753[1] 4.7K 5% 1/16W MF-LF 402

=PP3V3_GPU_VDD33

DP_CA_DET_EG_FET
R8742[1] 100K 1% 1/16W MF-LF 402
Q8742 SOD-VESM-HF SSM3K15FV

EG_DP_CA_DET — DP_CA_DET

R8743 0 5% 1/16W MF-LF 402
DP_CA_DET_EG_PLD

Isolation FETs for DP MUX inputs

G96 HDCP ROM APN is 341S2272, blank device is 335S0574.

GPU 27MHz Crystal

R8783 0 5% 1/16W MF-LF 402
GPU_CLK27M — GPU_CLK27M_XTALOUT_R
NO STUFF
R8782[1] 10M 5% 1/16W MF-LF 402
GPU_XTALOUT

CRITICAL
Y8780 27MHZ SM-2
NC NC

C8780 12pF 5% 50V CERM 402
C8781 12pF 5% 50V CERM 402

=PP3V3_GPU_VDD33

R8796[1] 2.2K 5% 1/16W MF-LF 402
R8797[1] 2.2K 5% 1/16W MF-LF 402

SMC_GFX_OVERTEMP_R_L	R8798 0 5% 1/16W MF-LF 402	SMC_GFX_OVERTEMP_L
SMC_GFX_THROTTLE_R_L	R8799 0 5% 1/16W MF-LF 402	SMC_GFX_THROTTLE_L

EG_LCD_PWR_EN
EG_BKLT_EN
GPIO7_FBVDD_ALTVO
FB_VREF_UNTERM

R8792[1] 10K 5% 1/16W MF-LF 402
R8793[1] 10K 5% 1/16W MF-LF 402
R8794[1] 10K 5% 1/16W MF-LF 402
NO STUFF
R8795[1] 10K 5% 1/16W MF-LF 402

Unused Clocks

GPU_XTALSSIN
GPU_XTALOUTBUFF
GPU_SS_INT

R8780[1] 10K 5% 1/16W MF-LF 402
R8781[1] 10K 5% 1/16W MF-LF 402

G96 MIOA_DE and MIOA_D<9..0> are used as Debug Port.

NC_GPU_MIOA_CLKOUT_P	GPU_MIOA_CLKOUT_P	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOA_CLKOUT_N	GPU_MIOA_CLKOUT_N	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOA_CTL3	GPU_MIOA_CTL3	MAKE_BASE=TRUE NO_TEST=TRUE
TP_GPU_MIOA_DE	GPU_MIOA_DE	MAKE_BASE=TRUE
TP_GPU_MIOA_D<9..0>	GPU_MIOA_D<9..0>	MAKE_BASE=TRUE
NC_GPU_MIOA_CLKIN	GPU_MIOA_CLKIN	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOA_D<14..10>	GPU_MIOA_D<14..10>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOA_HSYNC	GPU_MIOA_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOA_VSYNC	GPU_MIOA_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_CLKIN	GPU_MIOB_CLKIN	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_CLKOUT_P	GPU_MIOB_CLKOUT_P	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_CLKOUT_N	GPU_MIOB_CLKOUT_N	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_CTL3	GPU_MIOB_CTL3	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_DE	GPU_MIOB_DE	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_D<14..0>	GPU_MIOB_D<14..0>	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_VSYNC	GPU_MIOB_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
NC_GPU_MIOB_HSYNC	GPU_MIOB_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=MUXGFX SYNC_DATE=07/09/2008

PAGE TITLE
G96 GPIOs & Straps

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 87 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Page Notes

Power aliases required by this page:
- =PP1V8_GPU_IFPX
- =PP3V3_GPU_IFPCD_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Sum of peak currents: 240mA

8 =PP1V8_GPU_IFPX

L8800 FERR-220-OHM 0402 — ?mA peak per diff pair, ?mA peak for all pairs
C8800 4.7UF 20% 6.3V CERM 603 — C8801 0.1UF 20% 10V CERM 402 — C8803 0.1UF 20% 10V CERM 402
Place at AG9 — Place at AG10
PP1V8_GPU_IFPAB_IOVDD_F (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

L8805 FERR-220-OHM 0402 — 80mA peak
C8805 4.7UF 20% 6.3V CERM 603 — C8806 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPAB_PLLVDD_F (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

GPU_IFPEF_RSET
GPU_IFPCD_RSET
GPU_IFPAB_RSET
R8855 1K 1% 1/16W MF-LF 402
R8850 1K 1% 1/16W MF-LF 402
R8851 1K 1% 1/16W MF-LF 402

L8810 FERR-220-OHM 0402 — ?mA peak per diff pair, ?mA peak for all pairs
8 =PP1V1_GPU_IFPCD_IOVDD
C8810 4.7UF 20% 6.3V CERM 603 — C8811 0.1UF 20% 10V CERM 402 — C8813 0.1UF 20% 10V CERM 402
Place at AJ8 — Place at AK8
PP1V1_GPU_IFPCD_IOVDD_F (MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.1 mm, VOLTAGE=1.1V)

I2CS must be pulled up if not used
I2CS addr fixed at 0x9E,0x9F

L8815 FERR-220-OHM 0402 — 160mA peak
C8815 4.7UF 20% 6.3V CERM 603 — C8816 0.1UF 20% 10V CERM 402
PP1V8_GPU_IFPCD_PLLVDD_F (MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.8V)

I2CS must be pulled up if not used.
I2CS addr fixed at 0x9E,0x9F

PP1V1_GPU_IFPEF_IOVDD_F
PP1V8_GPU_IFPEF_PLLVDD_F
Power inputs must be pulled down if not used
R8856 10K 5% 1/16W MF-LF 402
R8857 10K 5% 1/16W MF-LF 402

R8852 10K 5% 1/16W MF-LF 402
R8853 10K 5% 1/16W MF-LF 402
R8854 10K 5% 1/16W MF-LF 402

OMIT
U8000
NB9P-GS
BGA
SYMBOL 5 OF 9

AG9	IFPA_IOVDD	IFPA_TXC	AM11
AG10	IFPB_IOVDD	IFPA_TXC*	AM12
AJ8	IFPC_IOVDD	IFPA_TXD0	AM8
AK8	IFPD_IOVDD	IFPA_TXD0*	AL8
AE7	IFPE_IOVDD	IFPA_TXD1	AM10
AD7	IFPF_IOVDD	IFPA_TXD1*	AM9
AK9	IFPAB_PLLVDD	IFPA_TXD2	AK10
AJ11	IFPAB_RSET	IFPA_TXD2*	AL10
AJ9	IFPCD_PLLVDD	IFPA_TXD3	AK11
AK7	IFPCD_RSET	IFPA_TXD3*	AL11
AJ6	IFPEF_PLLVDD	IFPB_TXC	AP13
AL1	IFPEF_RSET	IFPB_TXC*	AN13
		IFPB_TXD4	AN8
		IFPB_TXD4*	AP8
		IFPB_TXD5	AP10
		IFPB_TXD5*	AN10
		IFPB_TXD6	AR11
		IFPB_TXD6*	AR10
		IFPB_TXD7	AN11
		IFPB_TXD7*	AP11
G1	I2CA_SCL		
G4	I2CA_SDA		
E3	I2CC_SCL		
E4	I2CC_SDA		
E2	I2CS_SCL		
E1	I2CS_SDA		
F6	I2CH_SCL		
G6	I2CH_SDA		
G3	I2CB_SCL		
G2	I2CB_SDA		
F4	I2CD_SCL		
G5	I2CD_SDA		
D5	I2CE_SCL		
E5	I2CE_SDA		
AJ12	DACA_VDD		
AK12	DACA_VREF		
AK13	DACA_RSET		
AC6	DACB_VDD		
AC5	DACB_VREF		
AB6	DACB_RSET		
AG7	DACC_VDD		
AK6	DACC_VREF		
AK7	DACC_RSET		

		DACA_RED	AM16
		DACA_GREEN	AM15
		DACA_BLUE	AL14
		DACA_HSYNC	AM13
		DACA_VSYNC	AL13
		DACB_RED	AA4
		DACB_GREEN	AB4
		DACB_BLUE	Y4
		DACB_CSYNC	AB5
		DACC_RED	AK4
		DACC_GREEN	AL4
		DACC_BLUE	AJ4
		DACC_HSYNC	AM1
		DACC_VSYNC	AN2

LVDS_EG_A_CLK_P, LVDS_EG_A_CLK_N
LVDS_EG_A_DATA_P<0>, LVDS_EG_A_DATA_N<0>, LVDS_EG_A_DATA_P<1>, LVDS_EG_A_DATA_N<1>, LVDS_EG_A_DATA_P<2>, LVDS_EG_A_DATA_N<2>, LVDS_EG_A_DATA_P<3>, LVDS_EG_A_DATA_N<3>
LVDS_EG_B_CLK_P, LVDS_EG_B_CLK_N
LVDS_EG_B_DATA_P<0>, LVDS_EG_B_DATA_N<0>, LVDS_EG_B_DATA_P<1>, LVDS_EG_B_DATA_N<1>, LVDS_EG_B_DATA_P<2>, LVDS_EG_B_DATA_N<2>, LVDS_EG_B_DATA_P<3>, LVDS_EG_B_DATA_N<3>
DP_EG_AUX_CH_P, DP_EG_AUX_CH_N
DP_EG_ML_P<0>, DP_EG_ML_N<0>, DP_EG_ML_P<1>, DP_EG_ML_N<1>, DP_EG_ML_P<2>, DP_EG_ML_N<2>, DP_EG_ML_P<3>, DP_EG_ML_N<3>

R8861 1K 5% 1/16W MF-LF 402 — NO STUFF — R8860 1K 5% 1/16W MF-LF 402

SYNC_MASTER=MUXGFX	SYNC_DATE=07/10/2008
PAGE TITLE	NV G96 Video Interfaces
Apple Inc.	DRAWING NUMBER 051-7892 SIZE D
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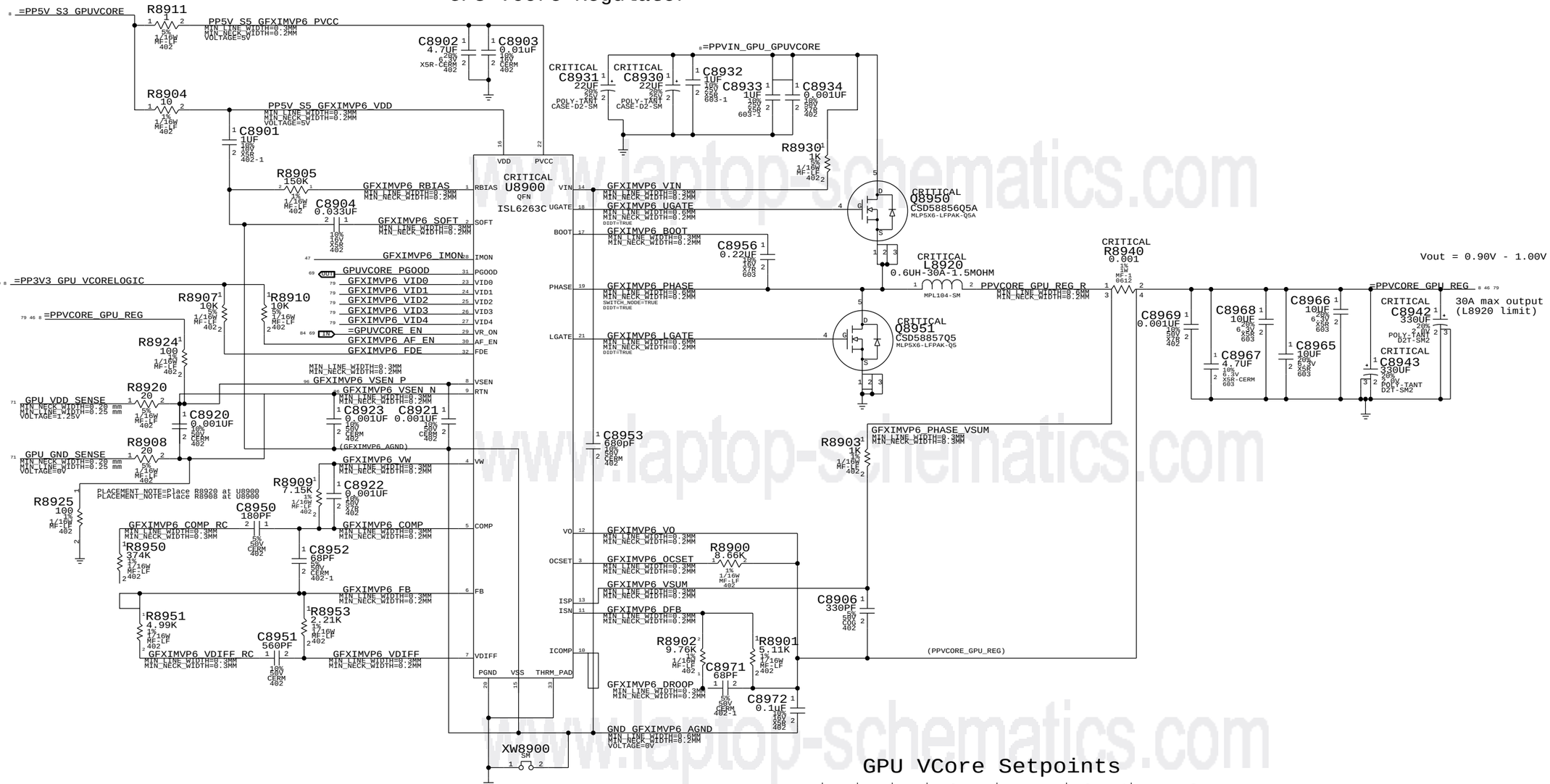
GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	K19		-
1	1	1	0	0.92700V	-	K19	-
1	0	1	1	1.00425V	-	-	K19

Other VID states may not be valid

K19 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1,GPUVID1_1,GPUVID0_1
GPUVID_1P00V	GPUVID2_0,GPUVID1_1,GPUVID0_1

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

PAGE TITLE: GPU (G96) CORE SUPPLY

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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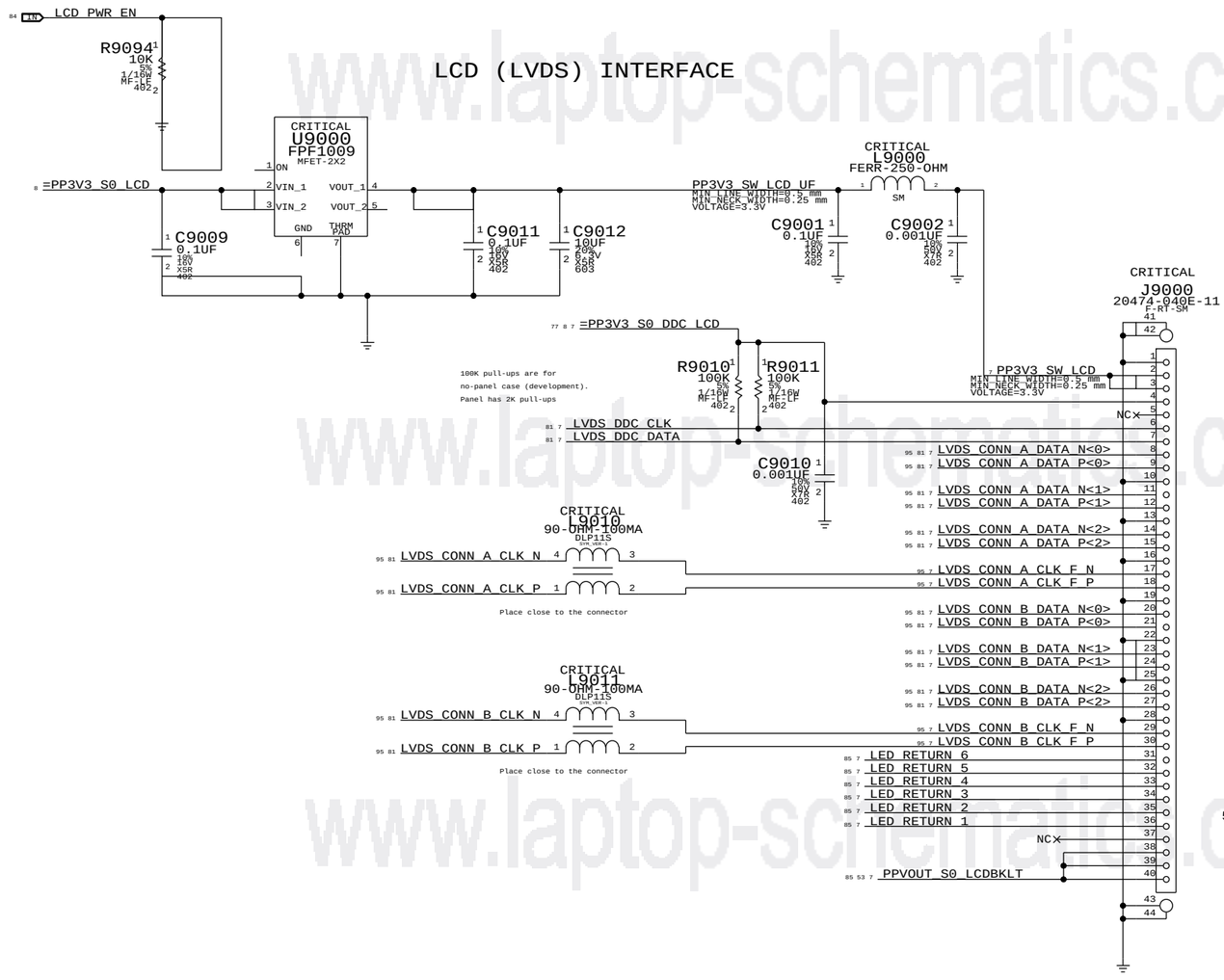
LCD (LVDS) INTERFACE



SYNC_MASTER=DDR SYNC_DATE=12/19/2008

PAGE TITLE
LVDS Display Connector

Apple Inc.

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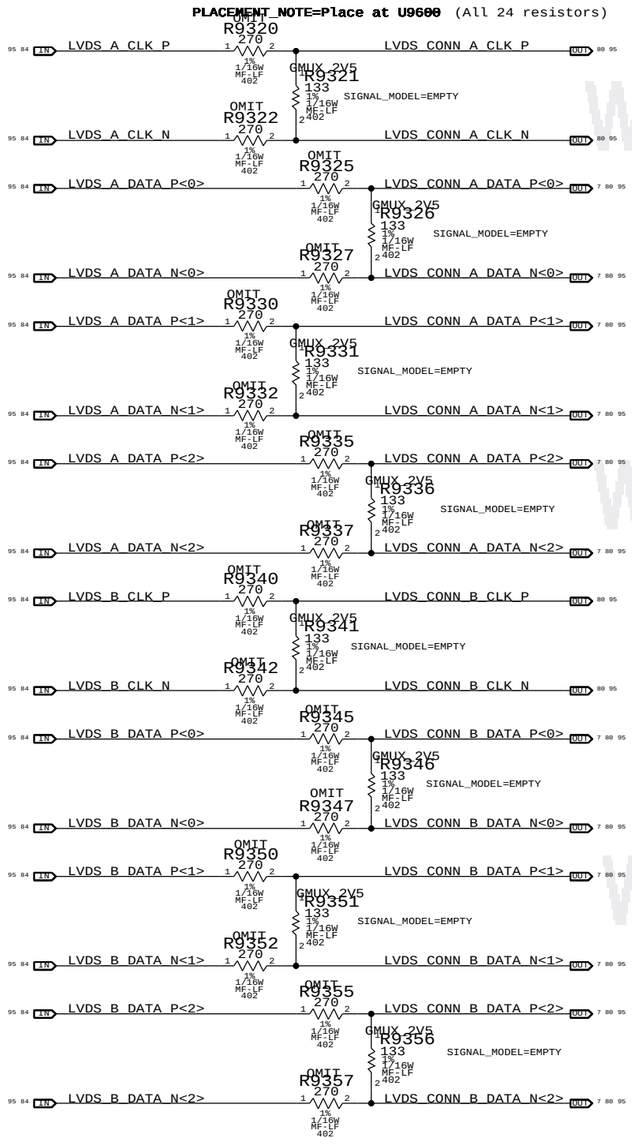
LVDS Transmitter Termination

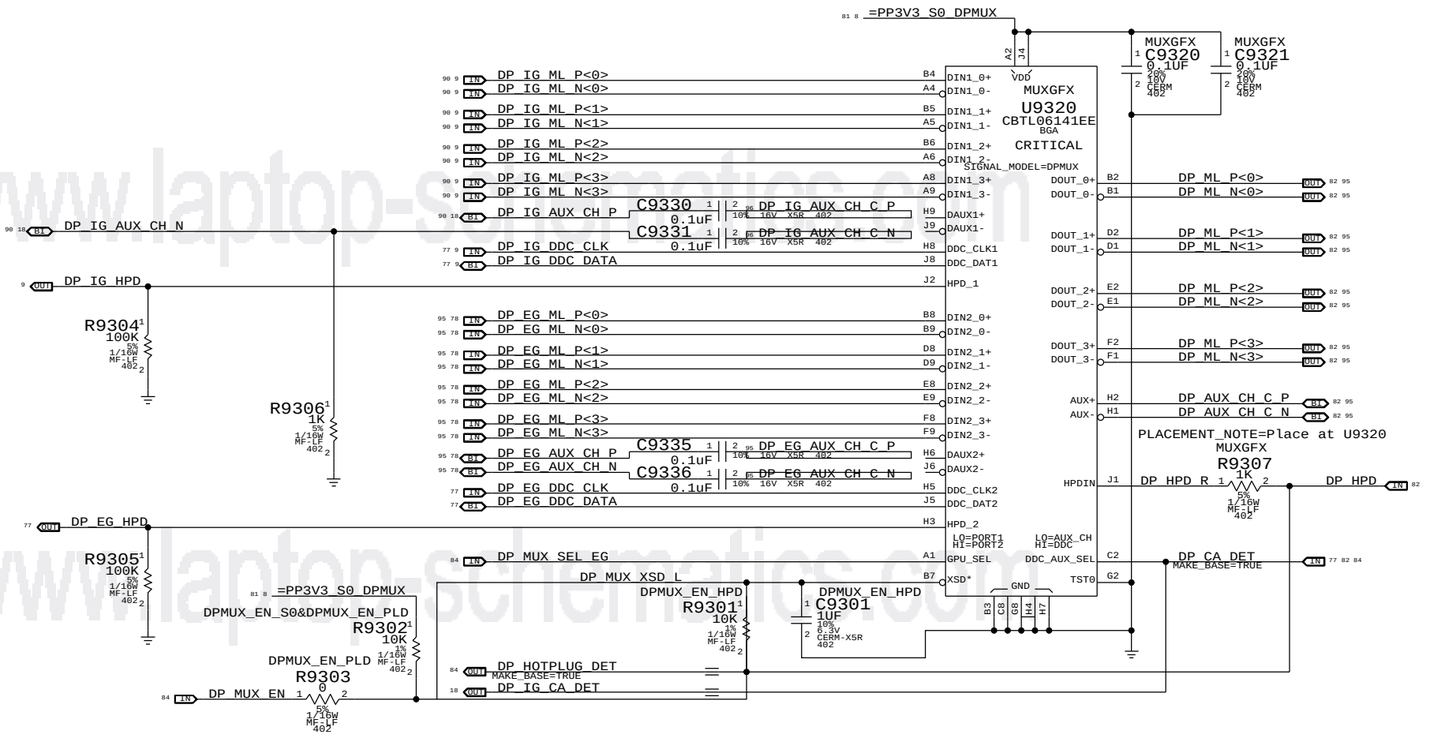
All emulated LVDS outputs require this termination

PLACEMENT_NOTE=Place at U9600 (All 24 resistors)

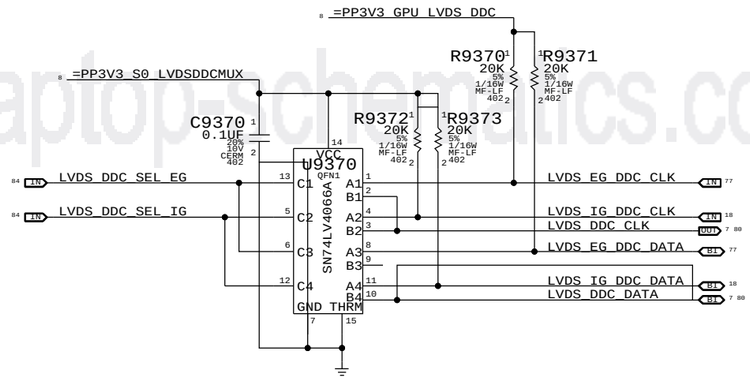


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S0517	16	RES,MTL FILM,270 OHM,1%,1/16W,0402,SMD,L			GMUX_2V5
114S0174	16	RES,MTL FILM,1/16W,357 OHM,1,0402,SMD,LF			GMUX_1V8

DisplayPort Mux



LVDS DDC MUX



SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=12/05/2008

PAGE TITLE: Muxed Graphics Support

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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Port Power Switch

CRITICAL
U9480
TPS2051B
SOT23
=PP3V3_S5_DP_PORT_PWR
PM_SLP_S3_L
PP3V3_S0_DPLIM
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
TP_DPPWR_OC_VOLTAGE=3.3V
C9480 22UF 20% 6.3V X5R-CERM 603
C9481 4.7UF 20% 6.3V X5R-CERM 402
C9485 4.7UF 20% 6.3V X5R-CERM 402
CRITICAL C9486 22UF 20% 6.3V X5R-CERM 603
L9400 FERR-120-0HM-3A 0603
CRITICAL C9400 22UF 20% 6.3V X5R-CERM 603
PP3V3_S0_DPPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V
R9420 100K 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8
DP_ESD CRITICAL D9410 RCLAMP0524P SLP2510P8

HDMI CEC

R9425 1M 5% 1/16W MF-LF 402

R9403 0 NO STUFF 5% 1/16W MF-LF 402
R9413 0 NO STUFF 5% 1/16W MF-LF 402
FL9403 12-OHM-100MA TCM1210-4SM

DP_ML_P<3> C9414 0.1UF 10% 16V X5R 402
DP_ML_N<3> C9415 0.1UF 10% 16V X5R 402
DP_AUX_CH_C_P
DP_AUX_CH_C_N

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	GND 1
4	CONFIG1	ML_LANE0P 3
6	CONFIG2	ML_LANE0N 5
8	GND	GND 7
10	ML_LANE3P	ML_LANE1P 9
12	ML_LANE3N	ML_LANE1N 11
14	GND	GND 13
16	AUX_CHP	ML_LANE2P 15
18	AUX_CHN	ML_LANE2N 17
20	DP_PWR	RETURN 19

SHIELD PINS 22 21

DP_ML_CONN_P<3>
DP_ML_CONN_N<3>

R9401 0 NO STUFF 5% 1/16W MF-LF 402
R9431 0 NO STUFF 5% 1/16W MF-LF 402
FL9401 12-OHM-100MA TCM1210-4SM

DP_ML_CONN_P<1>
DP_ML_CONN_N<1>
DP_ML_CONN_P<2>
DP_ML_CONN_N<2>

R9400 0 NO STUFF 5% 1/16W MF-LF 402
R9430 0 NO STUFF 5% 1/16W MF-LF 402
FL9400 12-OHM-100MA TCM1210-4SM

DP_ML_C_P<0> C9410 0.1UF 10% 16V X5R 402 DP_ML_P<0>
DP_ML_C_N<0> C9411 0.1UF 10% 16V X5R 402 DP_ML_N<0>
DP_ML_C_P<1> C9412 0.1UF 10% 16V X5R 402 DP_ML_P<1>
DP_ML_C_N<1> C9413 0.1UF 10% 16V X5R 402 DP_ML_N<1>
DP_ML_C_P<2> C9416 0.1UF 10% 16V X5R 402 DP_ML_P<2>
DP_ML_C_N<2> C9417 0.1UF 10% 16V X5R 402 DP_ML_N<2>

R9402 0 NO STUFF 5% 1/16W MF-LF 402
R9432 0 NO STUFF 5% 1/16W MF-LF 402
FL9402 12-OHM-100MA TCM1210-4SM

=PP3V3_S0_DPCONN
R9443 100K 5% 1/16W MF-LF 402
R9442 100K 5% 1/16W MF-LF 402
DP_CA_DET
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_L_Q
Q9440 2N7002DW-X-G SOT-363
DP_CA_DET_Q

Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm

R9421 100K 5% 1/16W MF-LF 402

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

DP_ESD CRITICAL D9400 RCLAMP0504F SC70-6-1

DP_ESD CRITICAL D9411 RCLAMP0524P SLP2510P8

R9422 1M 5% 1/16W MF-LF 402

DP to DVI/HDMI Cable Adapter (CA) has 100k pull-up to DP_PWR.

=PP3V3_S0_DPCONN
R9445 10K 5% 1/16W MF-LF 402
R9444 10K 5% 1/16W MF-LF 402
DP_HPD
Q9441 2N7002DW-X-G SOT-363
DP_HPD_L_Q
Q9441 2N7002DW-X-G SOT-363
DP_HPD_Q

R9423 100K 5% 1/16W MF-LF 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008
PAGE TITLE
DisplayPort Connector

Apple Inc.

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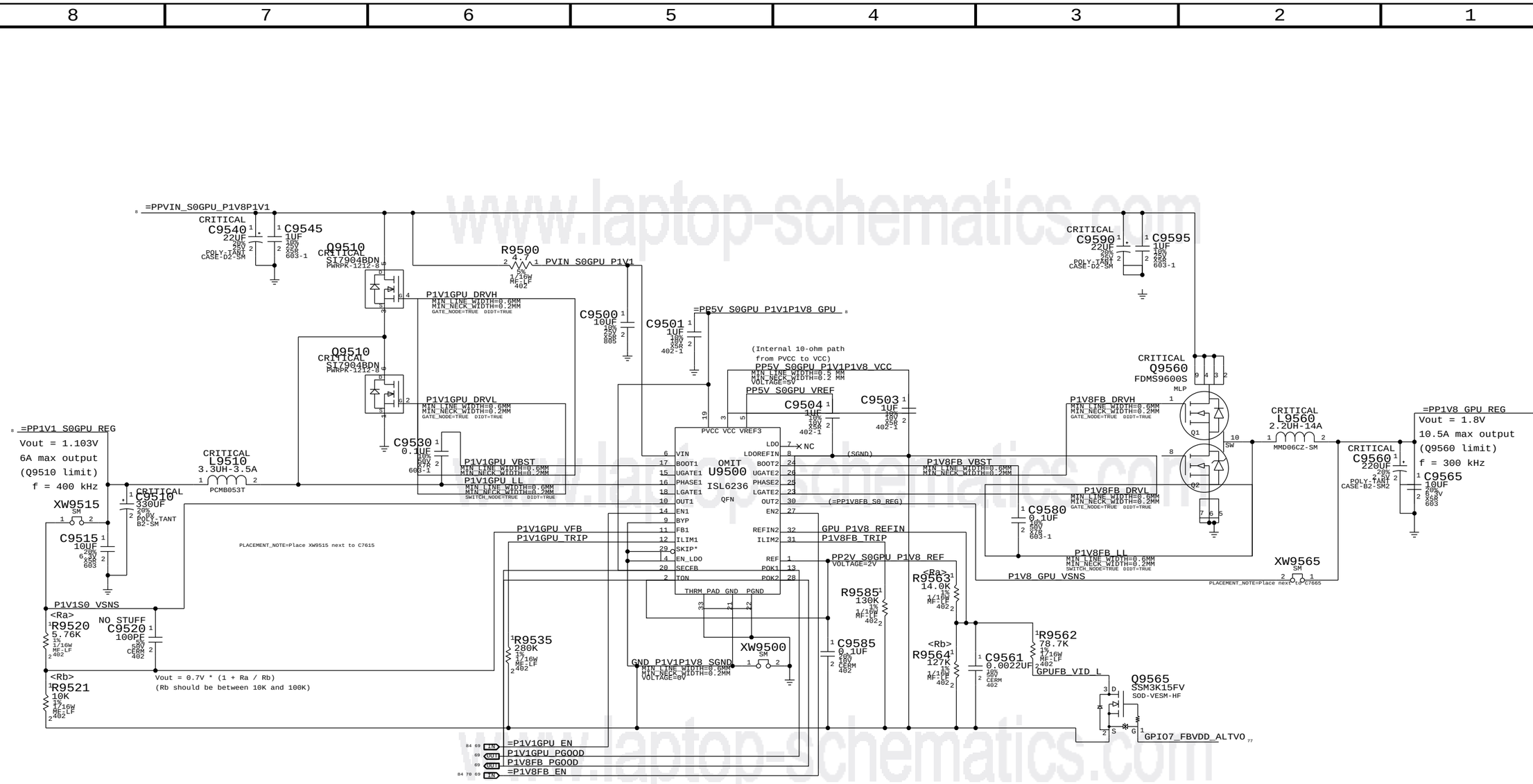
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S2312	1	IC,ISL6236,DUAL PWM CTRL,QFN32	U9500	CRITICAL	

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

PAGE TITLE: 1.1V / 1V8 FB Power Supply

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

REVISION: C.0.0

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GMUX CPLD

=PP3V3_S0_GMUX
=PP2V5_S0_GMUX
=PP1V2_S0_GMUX

C9610 C9621 C9622 C9623 C9624 C9625 C9626 C9628 C9629 C9630 0.1UF 20% 16V X7R CERM 402

C9611 C9612 C9613 C9614 C9615 C9616 C9617 0.1UF 20% 16V X7R CERM 402

C9600 4.7UF 20% 10V X5R 402

C9604 C9605 C9606 C9607 C9608 C9609 0.1UF 20% 16V X7R CERM 402

L9631 FERR-220-OHM 0402
PP3V3_S0_ULC_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C9631 0.1UF 20% 16V X7R CERM 402

L9627 FERR-220-OHM 0402
PP3V3_S0_LRC_F
MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C9627 0.1UF 20% 16V X7R CERM 402

R9640 10K 1% 1/16W MF-LF 402
R9645 10K 1% 1/16W MF-LF 402

NO STUFF
R9641 10K 1% 1/16W MF-LF 402
NO STUFF
R9646 10K 1% 1/16W MF-LF 402

NO STUFF
R9647 10K 1% 1/16W MF-LF 402

B11 C4 J3 J13 M11 P8 — VCC
C11 J2 J14 M8 — VCCAUX
B5 B7 A12 C14 F13 M12 M9 M3 N5 M1 C3 F2 K12 — VCCIO0 VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7
A4 P11 — VCCJ ULC_VCCPLL LRC_VCCPLL

OMIT CRITICAL

U9600
XP28
CSBGA-HF

JTAG_GMUX_TCK	K14	TCK	
JTAG_GMUX_TDI	L13	TDI	
JTAG_GMUX_TDO	K13	TDO	
JTAG_GMUX_TMS	L12	TMS	
GMUX_TOE	K2	TOE	
GMUX_CFG0	K1	CFG0	
LCD_BKLT_EN	P2	PB2A	BANK5
LCD_BKLT_PWM	N2	PB2B	
LVDS_DDC_SEL_EG	P4	PB14A	
LVDS_DDC_SEL_IG	N4	PB14B	
DP_MUX_EN	N3	PB15A (OD)	
DP_MUX_SEL_EG	M4	PB15B	
EG_RESET_L	P5	PB16A	
EG_RAIL1_EN	M5	PB16B	
EG_RAIL2_EN	P6	PB17A	
EG_RAIL3_EN	M6	PB17B	
EG_RAIL4_EN	P7	PB18A	
EG_CLKREQ_OUT_L	M7	PB18B (OD)	
DP_CA_DET_EG	N7	PB19A	
LCD_PWR_EN	N8	PB19B	
LPC_AD<0>	P9	PB20A	BANK4
LPC_AD<1>	N9	PB20B	
LPC_AD<2>	P10	PB30A	
LPC_AD<3>	M10	PB30B	
LPC_FRAME_L	P12	PB31A	
LPC_RESET_L	P13	PB31B	
LPC_CLK33M_GMUX	N12	PB32A	
GMUX_INT	P14	PB32B	
LVDS_IG_B_DATA_P<2>	B1	PL2A	BANK7
LVDS_IG_B_DATA_N<2>	B2	PL2B	
TP_GMUX_PL10A	C2	PL10A	
TP_GMUX_PL10B	D3	PL10B	
LVDS_IG_A_DATA_P<0>	D1	PL11A	
LVDS_IG_A_DATA_N<0>	E1	PL11B	
LVDS_IG_A_DATA_P<1>	D2	PL12A	
LVDS_IG_A_DATA_N<1>	E3	PL12B	
LVDS_IG_A_DATA_P<2>	F1	PL13A	
LVDS_IG_A_DATA_N<2>	G1	PL13B	
LVDS_IG_B_DATA_P<0>	F3	PL14A	
LVDS_IG_B_DATA_N<0>	G2	PL14B	
LVDS_IG_B_DATA_P<1>	H2	PL15A	
LVDS_IG_B_DATA_N<1>	G3	PL15B	
LVDS_IG_A_CLK_P	H1	PL16A	
LVDS_IG_A_CLK_N	H3	PL16B	
LVDS_MUX_SEL_EG	L1	PL18A	BANK6
TP_GMUX_PL18B_VSYNC	L3	PL18B	
=GMUX_PCIE_RESET_L	K3	PL19A	
GMUX_PM_SLP_S3_L	L2	PL19B	
ALL_EG_PGOOD	N1	PL32A	
EG_CLKREQ_IN_L	P1	PL32B	

(Tie/strap low if EGPU doesn't provide CLKREQ_L output, provide pullup to GPU rail if using CLKREQ_L output from EGPU)

GND — GNDIO0 GNDIO1 GNDIO2 GNDIO3 GNDIO4 GNDIO5 GNDIO6 GNDIO7 ULC_GNDPLL LRC_GNDPLL
J1 — B8 E6 C12 E13 M14 M10 N6 P3 M2 F1 F2 B4 M11

PT2A	A2	LVDS_B_DATA_P<0>	
PT2B	A3	LVDS_B_DATA_N<0>	
PT3A	A1	LVDS_B_DATA_P<1>	
PT3B	B3	LVDS_B_DATA_N<1>	
PT4A	C5	LVDS_B_DATA_P<2>	
PT4B	A5	LVDS_B_DATA_N<2>	
PT14A	B6	EG_PWRSEQ_EN	
PT14B	C7	GMUX_DEBUG_RESET_L	
PT15A	A6	LVDS_A_CLK_P	BANK0
PT15B	A7	LVDS_A_CLK_N	
PT16A	C8	LVDS_B_CLK_P	
PT16B	C9	LVDS_B_CLK_N	
PT17A	A8	LVDS_A_DATA_P<0>	
PT17B	B9	LVDS_A_DATA_N<0>	
PT18A	A9	LVDS_A_DATA_P<1>	
PT18B	C10	LVDS_A_DATA_N<1>	
PT19A	B10	LVDS_A_DATA_P<2>	
PT19B	A10	LVDS_A_DATA_N<2>	
PT20A	A11	TP_GMUX_PT20A	BANK1
PT20B	B12	TP_GMUX_PT20B	
PT32A	B13	TP_GMUX_PT32A	
PT32B	A13	TP_GMUX_PT32B	
PR2A	A14	DP_CA_DET	BANK2
PR2B	B14	DP_HOTPLUG_DET	
PR10A	D12	LVDS_EG_A_DATA_P<0>	
PR10B	D13	LVDS_EG_A_DATA_N<0>	
PR11A	D14	LVDS_EG_A_DATA_P<1>	
PR11B	E14	LVDS_EG_A_DATA_N<1>	
PR12A	E12	LVDS_EG_A_DATA_P<2>	
PR12B	F12	LVDS_EG_A_DATA_N<2>	
PR13A	F14	LVDS_EG_B_DATA_P<0>	
PR13B	G14	LVDS_EG_B_DATA_N<0>	
PR14A	G12	LVDS_EG_B_DATA_P<1>	
PR14B	G13	LVDS_EG_B_DATA_N<1>	
PR15A	H13	LVDS_EG_B_DATA_P<2>	
PR15B	H12	LVDS_EG_B_DATA_N<2>	
PR16A	H14	LVDS_EG_A_CLK_P	
PR16B	J12	LVDS_EG_A_CLK_N	
PR18A	L14	IG_LCD_PWR_EN	BANK3
PR18B	M13	EG_LCD_PWR_EN	
PR30A	N14	IG_BKLT_EN	
PR30B	N13	EG_BKLT_EN	

PM_SLP_S3_L Isolation

=PP3V3_S0_GMUX
Q9670 SSM6N15FEAPE SOT563
R9670 10K 1% 1/16W MF-LF 402
PM_SLP_S3_L → GMUX_PM_SLP_S3_L
MAKE_BASE=TRUE
EG_PWRSEQ_EN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0925	1	IC,XP2-5,HF,CPLD,BLANK	U9600	CRITICAL	GMUX_5K_BLANK
341S2479	1	IC,CPLD,LATTICE,132CSBGA,K19	U9600	CRITICAL	GMUX_PROG

GMUX_JTAG_TCK Inversion

JTAG_GMUX_TCK
Q9670 SSM6N15FEAPE SOT563
GMUX_JTAG_TCK_L

LVDS Receiver Termination

PLACEMENT_NOTE=Place at U9200 (All 14 resistors)

LVDS_IG_A_CLK_P	R9650	100	LVDS_IG_A_CLK_N	
LVDS_IG_A_DATA_P<0>	R9651	100	LVDS_IG_A_DATA_N<0>	
LVDS_IG_A_DATA_P<1>	R9652	100	LVDS_IG_A_DATA_N<1>	
LVDS_IG_A_DATA_P<2>	R9653	100	LVDS_IG_A_DATA_N<2>	
LVDS_IG_B_DATA_P<0>	R9654	100	LVDS_IG_B_DATA_N<0>	
LVDS_IG_B_DATA_P<1>	R9655	100	LVDS_IG_B_DATA_N<1>	
LVDS_IG_B_DATA_P<2>	R9656	100	LVDS_IG_B_DATA_N<2>	
LVDS_EG_A_CLK_P	R9660	100	LVDS_EG_A_CLK_N	
LVDS_EG_A_DATA_P<0>	R9661	100	LVDS_EG_A_DATA_N<0>	
LVDS_EG_A_DATA_P<1>	R9662	100	LVDS_EG_A_DATA_N<1>	
LVDS_EG_A_DATA_P<2>	R9663	100	LVDS_EG_A_DATA_N<2>	
LVDS_EG_B_DATA_P<0>	R9664	100	LVDS_EG_B_DATA_N<0>	
LVDS_EG_B_DATA_P<1>	R9665	100	LVDS_EG_B_DATA_N<1>	
LVDS_EG_B_DATA_P<2>	R9666	100	LVDS_EG_B_DATA_N<2>	

All: 1% 1/16W MF-LF 402

SIGNAL_MODEL=EMPTY

Required Pullups

=PP3V3_S0_GMUX

GMUX_DEBUG_RESET_L	R9680	1K	5% 1/16W MF-LF 402
JTAG_GMUX_TCK	R9690	4.7K	5% 1/16W MF-LF 402
EG_CLKREQ_OUT_L	R9695	10K	5% 1/16W MF-LF 402

NO STUFF
R9679 10K 1% 1/16W MF-LF 402
SILK_PART=GMUX_RST
PLACEMENT_NOTE=Place on top side at U9200

Required Pulldowns

DP_MUX_SEL_EG	R9681	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_IG	R9682	10K	5% 1/16W MF-LF 402
LVDS_DDC_SEL_EG	R9683	10K	5% 1/16W MF-LF 402
			NO STUFF
EG_RESET_L	R9691	100K	5% 1/16W MF-LF 402
GMUX_INT	R9692	20K	5% 1/16W MF-LF 402
LCD_BKLT_PWM	R9693	100K	5% 1/16W MF-LF 402
EG_CLKREQ_IN_L	R9694	100K	5% 1/16W MF-LF 402

(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

EG_PWRSEQ_HW

EG_RAIL1_EN	R9630	0	EXTGPU_PWR_EN
	R9631	0	=P1V1GPU_EN
EG_RAIL2_EN	R9632	0	P3V3GPU_EN
EG_RAIL3_EN	R9633	0	=GPUVCORE_EN
EG_RAIL4_EN	R9634	0	=P1V8FB_EN

EG_PWRSEQ_GMUX

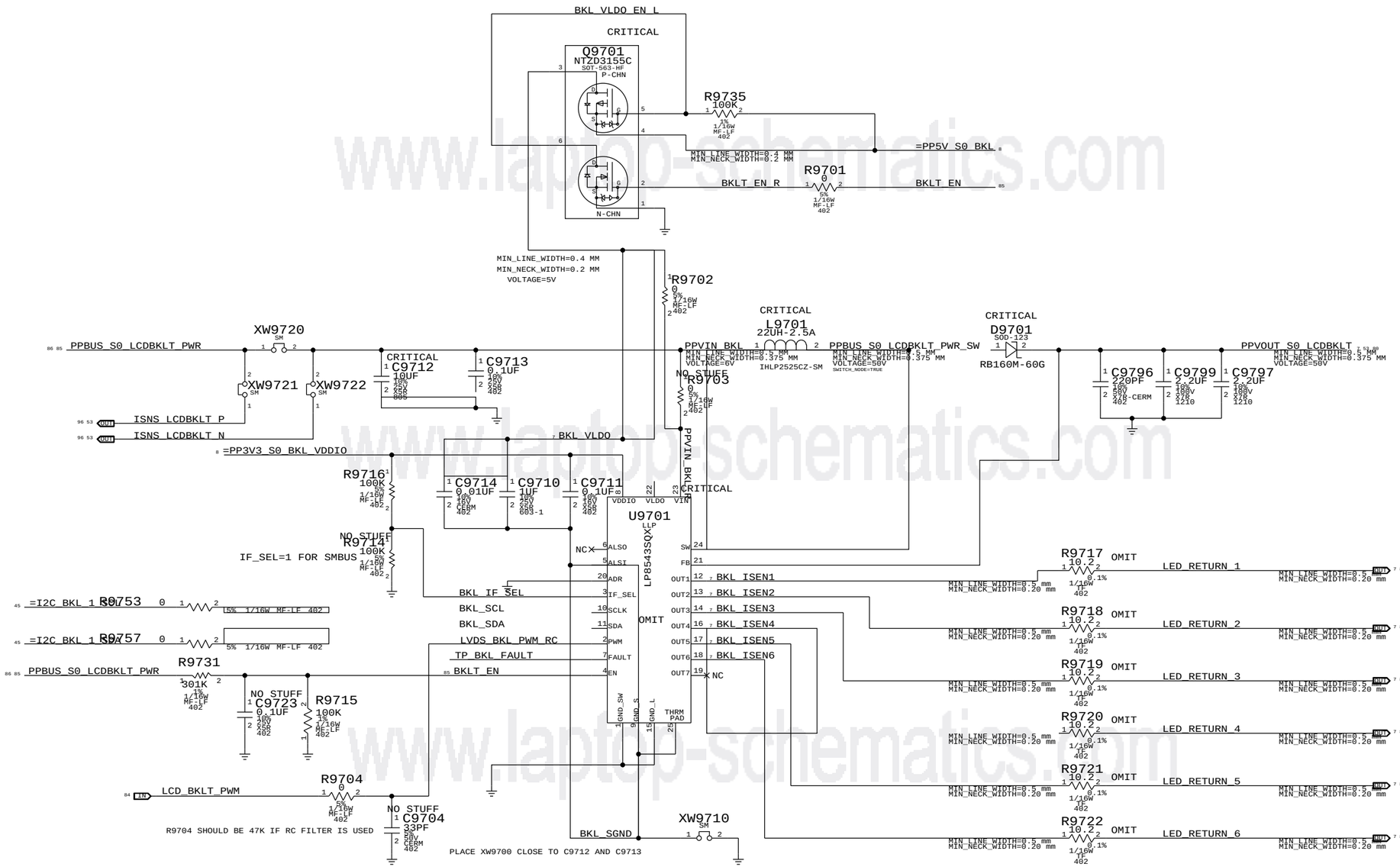
5% 1/16W MF-LF 402

The MAKE BASE properties for these signals are on the POWER CONTROL page.

NO STUFF C9691 0.1UF 20% 16V X7R CERM 402
NO STUFF C9693 0.1UF 20% 16V X7R CERM 402
NO STUFF C9692 0.1UF 20% 16V X7R CERM 402
NO STUFF C9694 0.1UF 20% 16V X7R CERM 402

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008
PAGE TITLE: Graphics MUX (GMUX)
Apple Inc.
DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 96 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

*L9701, D9701, C9796, C9797, C9799, C9712 AND C9713 SHOULD ALL BE PLACED NEAR EACHOTHER.
*PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
* LVDS_IG_BKL_PWM SHOULD BE AWAY FROM BOOST CIRCUIT



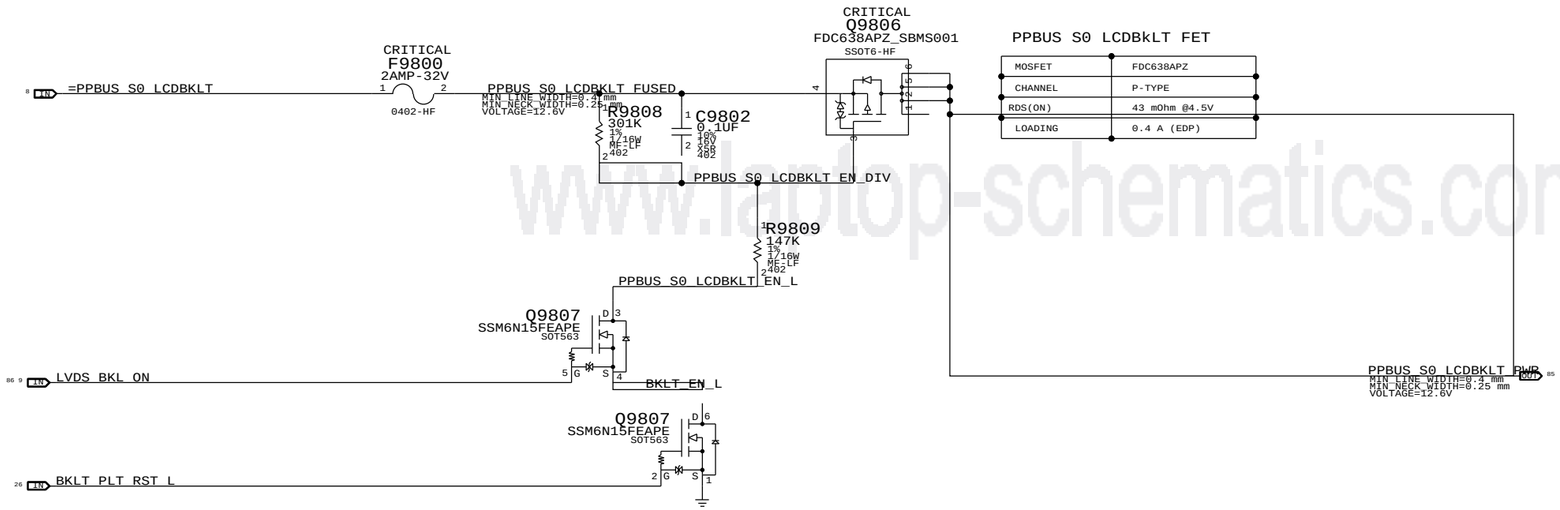
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S2670	1	IC,LP8543,WHT LED BKLT,PROD	U9701	CRITICAL	
116S0004	6	RES,1/16W,0 ohm,5%,0402,SM	R9717,R9718,R9719,R9720,R9721,R9722		

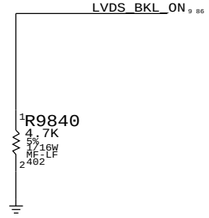
SYNC_MASTER=DDR SYNC_DATE=12/12/2008

PAGE TITLE
LCD BACKLIGHT DRIVER

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 97 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>





SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

PAGE TITLE: LCD Backlight Support

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D

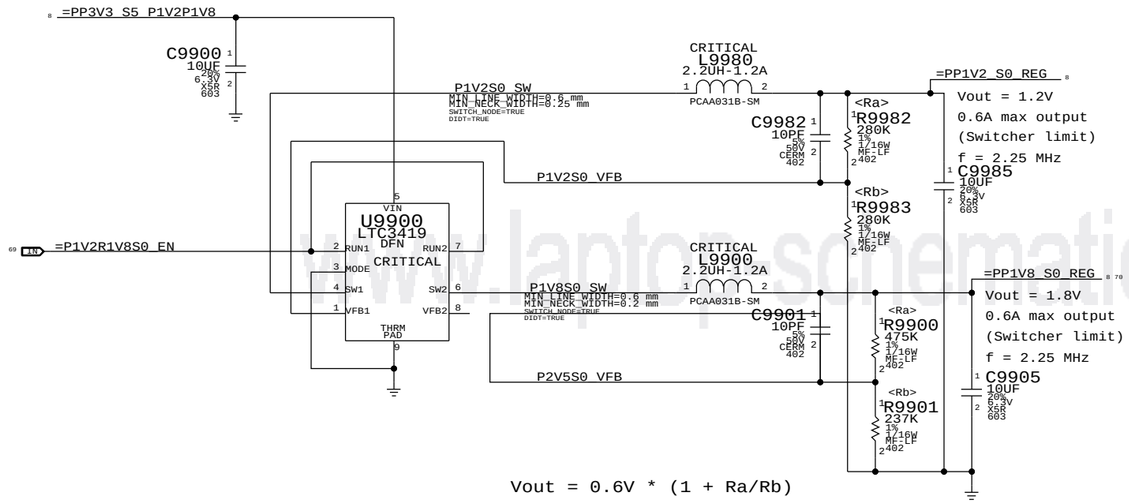
REVISION: C.0.0

BRANCH:

PAGE: 98 OF 109

SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

1.8V/1.2V S0 SWITCHER



SYNC_MASTER=MUXGFX	SYNC_DATE=02/01/2008
PAGE TITLE: Misc Power Supplies	
Apple Inc.	DRAWING NUMBER: 051-7892 SIZE: D
	REVISION: C.0.0
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	PAGE: 99 OF 109
	SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?
FSB_ADSTB	*	=2x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.
Signals within each 4x group should be matched within 5 ps of strobe.
DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.
Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.
Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/- 300 ps.
Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.
Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.
Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	25 MIL	?
CPU_GTLREF	*	25 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2
SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB 4X Signal Groups	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_D_L<15..0>	7 10 14
	FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB_DINV_L<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_D_L<31..16>	7 10 14
	FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB_DINV_L<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_D_L<47..32>	7 10 14
	FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB_DINV_L<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_D_L<63..48>	7 10 14
	FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB_DINV_L<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB 2X Signals	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_A_L<16..3>	7 10 14
	FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB_REQ_L<4..0>	10 14
	FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
	FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB_A_L<35..17>	7 10 14
	FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
FSB 1X Signals	FSB_1X	FSB_50S	FSB_1X	FSB_ADS_L	7 10 14
	FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9 10 14
	FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14
	FSB_1X	FSB_50S	FSB_1X	FSB_BNR_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_BPRI_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DBSY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DEFER_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_DRDY_L	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HIT_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_HITM_L	7 10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_LOCK_L	7 10 14
	FSB_CPURST_L	FSB_50S	FSB_1X	FSB_CPURST_L	9 10 13 14
	FSB_1X	FSB_50S	FSB_1X	FSB_RS_L<2..0>	10 14
	FSB_1X	FSB_50S	FSB_1X	FSB_TRDY_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_A20M_L	10 14
	CPU_BSEL	CPU_50S	CPU_AGTL	CPU_BSEL<2..0>	9 10
	CPU_FERR_L	CPU_50S	CPU_8MIL	CPU_FERR_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_IGNNE_L	10 14
	CPU_INIT_L	CPU_50S	CPU_AGTL	CPU_INIT_L	10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_INTR	9 10 14
	CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU_NMI	9 10 14
	CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 14 43 63
	CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 13 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_SMI_L	10 14
	CPU_ASYNC	CPU_50S	CPU_AGTL	CPU_STPCLK_L	10 14
	PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 14 43
	FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB_CPUSLP_L	10 14
	CPU_FROM_SB	CPU_50S	CPU_AGTL	CPU_DPSLP_L	10 14
	CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU_DPRSTP_L	9 10 14 63
	CPU_ASYNC	CPU_50S	CPU_AGTL	FSB_DPWR_L	10 14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_VDD	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_BCLK_VML_COMP_GND	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_VCC	14
	MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP_CPU_COMP_GND	14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	10 14
	FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	10 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_P	13 14
	FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB_CLK_ITP_N	13 14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_P	14
	FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB_CLK_MCP_N	14
	CPU_IERR_L	CPU_50S		CPU_IERR_L	10
	PM_DPRSLPVR	CPU_50S	CPU_AGTL	PM_DPRSLPVR	21 63
	(See above)	CPU_50S	CPU_AGTL	IMVP_DPRSLPVR	63
	CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU_GTLREF	10 27
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
	CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10
	CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
	XDP_TDI	CPU_50S	CPU_ITP	XDP_TDI	6 10 13
	XDP_TDO	CPU_50S	CPU_ITP	XDP_TDO	6 10
	XDP_TMS	CPU_50S	CPU_ITP	XDP_TMS	6 10 13
	XDP_TCK	CPU_50S	CPU_ITP	XDP_TCK	6 10 13
	XDP_TRST_L	CPU_50S	CPU_ITP	XDP_TRST_L	6 10 13
	XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<4..0>	10 13
	XDP_BPM_L5	CPU_50S	CPU_ITP	XDP_BPM_L<5>	10 13
	(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	13
		CPU_50S	CPU_8MIL	CPU_VID<6..0>	9 11
		CPU_50S	CPU_8MIL	IMVP6_VID<6..0>	9 63
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 63
	CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 63
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	63
	(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	63

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

PAGE TITLE: CPU/FSB Constraints

Apple Inc.

DRAWING NUMBER: 051-7892 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 100 OF 109
SHEET: <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR2:
DQ signals should be matched within 20 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
All DQS pairs should be matched within 100 ps of clocks.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:
DQ signals should be matched within 5 ps of associated DQS pair.
DQS intra-pair matching should be within 1 ps, inter-pair matching shoulw be within 180 ps
No DQS to clock matching requirement.
CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
A/BA/cmd signals should be matched within 5 ps of CLK pairs.
All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_P<5..0>	15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM_A_CLK_N<5..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CKE<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_CS_L<3..0>	15 28
MEM_A_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_A_ODT<3..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_A<14..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_BA<2..0>	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_RAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_CAS_L	15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM_A_WE_L	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DQ<7..0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DQ<15..8>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DQ<23..16>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DQ<31..24>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DQ<39..32>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DQ<47..40>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DQ<55..48>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DQ<63..56>	15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_A_DM<0>	15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_A_DM<1>	15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_A_DM<2>	15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_A_DM<3>	15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_A_DM<4>	15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_A_DM<5>	15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_A_DM<6>	15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_A_DM<7>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_P<5..0>	15 29
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM_B_CLK_N<5..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CKE<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_CS_L<3..0>	15 29
MEM_B_CNTL	MEM_40S_VDD	MEM_CTRL	MEM_B_ODT<3..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_A<14..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_BA<2..0>	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_RAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_CAS_L	15 29
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM_B_WE_L	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DQ<7..0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DQ<15..8>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DQ<23..16>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DQ<31..24>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DQ<39..32>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DQ<47..40>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DQ<55..48>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DQ<63..56>	15 29
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM_B_DM<0>	15 29
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM_B_DM<1>	15 29
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM_B_DM<2>	15 29
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM_B_DM<3>	15 29
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM_B_DM<4>	15 29
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM_B_DM<5>	15 29
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM_B_DM<6>	15 29
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM_B_DM<7>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	15 29
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	15 29
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	15 29
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	15 29
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	15 29
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	15 29
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	15 29
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	15 29
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	15 29
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_VDD	16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP_GND	16

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PAGE TITLE: Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	13.1 MM	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRT	CRT	*	CRT_2CRT

CRT signal single-ended impedence varies by location:
- 37.5-ohm from MCP to first termination resistor.
- 50-ohm from first to second termination resistor.
- 75-ohm from output of three-pole filter to connector (if possible).

R/G/B signals should be matched as close as possible and < 10 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_TERMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCIE_90D	PCIE	PEG_R2D_P<15..0>	71
	PCIE_90D	PCIE	PEG_R2D_N<15..0>	71
PEG_R2D	PCIE_90D	PCIE	PEG_R2D_C_P<15..0>	9 71
	PCIE_90D	PCIE	PEG_R2D_C_N<15..0>	9 71
PEG_D2R	PCIE_90D	PCIE	PEG_D2R_P<15..0>	9 71
	PCIE_90D	PCIE	PEG_D2R_N<15..0>	9 71
	PCIE_90D	PCIE	PEG_D2R_C_P<15..0>	71
	PCIE_90D	PCIE	PEG_D2R_C_N<15..0>	71
	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 31 96
	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 31 96
PCIE_MINI_R2D	PCIE_90D	PCIE	PCIE_MINI_R2D_C_P	17 31
	PCIE_90D	PCIE	PCIE_MINI_R2D_C_N	17 31
PCIE_MINI_D2R	PCIE_90D	PCIE	PCIE_MINI_D2R_P	7 17 31
	PCIE_90D	PCIE	PCIE_MINI_D2R_N	7 17 31
	PCIE_90D	PCIE	PCIE_FW_R2D_P	36
	PCIE_90D	PCIE	PCIE_FW_R2D_N	36
PCIE_FW_R2D	PCIE_90D	PCIE	PCIE_FW_R2D_C_P	17 36
	PCIE_90D	PCIE	PCIE_FW_R2D_C_N	17 36
PCIE_FW_D2R	PCIE_90D	PCIE	PCIE_FW_D2R_P	17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_N	17 36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_P	36
	PCIE_90D	PCIE	PCIE_FW_D2R_C_N	36
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	96
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	96
PCIE_EXCARD_R2D	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_P	9 17
	PCIE_90D	PCIE	PCIE_EXCARD_R2D_C_N	9 17
PCIE_EXCARD_D2R	PCIE_90D	PCIE	PCIE_EXCARD_D2R_P	9 17
	PCIE_90D	PCIE	PCIE_EXCARD_D2R_N	9 17
MCP_PE0_REFCLK	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_P	17 71
	CLK_PCIE_100D	CLK_PCIE	PEG_CLK100M_N	17 71
MCP_PE1_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	17 31
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	17 31
MCP_PE2_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	17 36
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	17 36
MCP_PE3_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	9 17
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	9 17
MCP_PEX_CLK_COMP		MCP_PEX_COMP	MCP_PEX_CLK_COMP	17
CRT_RED	CRT_50S	CRT	CRT_IG_R_C_PR	18 25
CRT_GREEN	CRT_50S	CRT	CRT_IG_G_Y_Y	18 25
CRT_BLUE	CRT_50S	CRT	CRT_IG_B_COMP_PB	18 25
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_HSYNC	18 25
CRT_SYNC	CRT_50S	CRT_SYNC	CRT_IG_VSYNC	18 25
MCP_DAC_RSET		MCP_DAC_COMP	MCP_TV_DAC_RSET	18 25
MCP_DAC_VREF		MCP_DAC_COMP	MCP_TV_DAC_VREF	18 25
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_P	
TMDS_IG_TXC	DP_100D	DISPLAYPORT	TMDS_IG_TXC_N	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_P<2..0>	
TMDS_IG_TXD	DP_100D	DISPLAYPORT	TMDS_IG_TXD_N<2..0>	
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_P<3..0>	9 81
DP_ML	DP_100D	DISPLAYPORT	DP_IG_ML_N<3..0>	9 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_P	18 81
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_N	18 81
MCP_HDMI_RSET	MCP_DV_COMP		MCP_HDMI_RSET	18 25
MCP_HDMI_VPROBE	MCP_DV_COMP		MCP_HDMI_VPROBE	18 25
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_P	18 84
LVDS_IG_A_CLK	LVDS_100D	LVDS	LVDS_IG_A_CLK_N	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<2..0>	18 84
LVDS_IG_A_DATA	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<2..0>	18 84
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_P<3>	9 18
LVDS_IG_A_DATA3	LVDS_100D	LVDS	LVDS_IG_A_DATA_N<3>	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_P	9 18
LVDS_IG_B_CLK	LVDS_100D	LVDS	LVDS_IG_B_CLK_N	9 18
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<2..0>	18 84
LVDS_IG_B_DATA	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<2..0>	18 84
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_P<3>	9 18
LVDS_IG_B_DATA3	LVDS_100D	LVDS	LVDS_IG_B_DATA_N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP		MCP_IFPAB_RSET	18 25
MCP_IFPAB_VPROBE			MCP_IFPAB_VPROBE	18 25
SATA_HDD_R2D	SATA_100D	SATA	SATA_HDD_R2D_C_P	20 39
	SATA_100D	SATA	SATA_HDD_R2D_C_N	20 39
	SATA_100D	SATA	SATA_HDD_R2D_P	7 39
	SATA_100D	SATA	SATA_HDD_R2D_N	7 39
SATA_HDD_D2R	SATA_100D	SATA	SATA_HDD_D2R_P	20 39
	SATA_100D	SATA	SATA_HDD_D2R_N	20 39
	SATA_100D	SATA	SATA_HDD_D2R_C_P	7 39
	SATA_100D	SATA	SATA_HDD_D2R_C_N	7 39
SATA_ODD_R2D	SATA_100D	SATA	SATA_ODD_R2D_C_P	20 39
	SATA_100D	SATA	SATA_ODD_R2D_C_N	20 39
	SATA_100D	SATA	SATA_ODD_R2D_P	7 39
	SATA_100D	SATA	SATA_ODD_R2D_N	7 39
SATA_ODD_D2R	SATA_100D	SATA	SATA_ODD_D2R_P	20 39
	SATA_100D	SATA	SATA_ODD_D2R_N	20 39
	SATA_100D	SATA	SATA_ODD_D2R_C_P	7 39
	SATA_100D	SATA	SATA_ODD_D2R_C_N	7 39
MCP_SATA_TERMP		SATA_TERMP	MCP_SATA_TERMP	20

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PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_5SS	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_DEBUG	PCI_5SS	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_5SS	PCI	PCI_AD<23..8>	
PCI_AD24	PCI_5SS	PCI	PCI_AD<24>	
PCI_AD	PCI_5SS	PCI	PCI_AD<31..25>	
PCI_AD	PCI_5SS	PCI	PCI_PAR	
PCI_C_BE_L	PCI_5SS	PCI	PCI_C_BE_L<3..0>	
PCI_CNTL	PCI_5SS	PCI	PCI_IRDY_L	
PCI_CNTL	PCI_5SS	PCI	PCI_DEVSEL_L	
PCI_CNTL	PCI_5SS	PCI	PCI_PERR_L	
PCI_CNTL	PCI_5SS	PCI	PCI_SERR_L	
PCI_CNTL	PCI_5SS	PCI	PCI_STOP_L	
PCI_CNTL	PCI_5SS	PCI	PCI_TRDY_L	
PCI_CNTL	PCI_5SS	PCI	PCI_FRAME_L	
PCI_REQ0_L	PCI_5SS	PCI	PCI_REQ0_L	19
PCI_GNT0_L	PCI_5SS	PCI	PCI_GNT0_L	
PCI_REQ1_L	PCI_5SS	PCI	PCI_REQ1_L	19
PCI_GNT1_L	PCI_5SS	PCI	PCI_GNT1_L	
PCI_INTW_L	PCI_5SS	PCI	PCI_INTW_L	
PCI_INTX_L	PCI_5SS	PCI	PCI_INTX_L	
PCI_INTY_L	PCI_5SS	PCI	PCI_INTY_L	
PCI_INTZ_L	PCI_5SS	PCI	PCI_INTZ_L	
MCP_PCI_CLK2	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP_R	19
	CLK_PCI_5SS	CLK_PCI	PCI_CLK33M_MCP	19
LPC_AD	LPC_5SS	LPC	LPC_AD<3..0>	19 42 44 B4
LPC_FRAME_L	LPC_5SS	LPC	LPC_FRAME_L	19 42 44 B4
LPC_RESET_L	LPC_5SS	LPC	LPC_RESET_L	19 26 B4
MCP_LPC_CLK0	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC_R	19 26
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_SMC	26 42
	CLK_LPC_5SS	CLK_LPC	LPC_CLK33M_LPCPLUS	26 44
USB_EXTA	USB_90D	USB	USB_EXTA_P	20 40
	USB_90D	USB	USB_EXTA_N	20 40
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 20 31
	USB_90D	USB	USB_CAMERA_N	7 20 31
USB_BT	USB_90D	USB	USB_BT_P	7 20 31
	USB_90D	USB	USB_BT_N	7 20 31
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 50
	USB_90D	USB	USB_TPAD_N	20 50
USB_IR	USB_90D	USB	USB_IR_P	20 41
	USB_90D	USB	USB_IR_N	20 41
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 40
	USB_90D	USB	USB_EXTB_N	20 40
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	9 20
	USB_90D	USB	USB_EXCARD_N	9 20
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 20
	USB_90D	USB	USB_EXTC_N	9 20
MCP_USB_RBIAS	MCP_USB_RBIAS		MCP_USB_RBIAS_GND	20
SMBUS_MCP_0_CLK	SMB_5SS	SMB	SMBUS_MCP_0_CLK	13 21 45
SMBUS_MCP_0_DATA	SMB_5SS	SMB	SMBUS_MCP_0_DATA	13 21 45
SMBUS_MCP_1_CLK	SMB_5SS	SMB	SMBUS_MCP_1_CLK	21 45
SMBUS_MCP_1_DATA	SMB_5SS	SMB	SMBUS_MCP_1_DATA	21 45
HDA_BIT_CLK	HDA_5SS	HDA	HDA_BIT_CLK	21 55
	HDA_5SS	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_5SS	HDA	HDA_SYNC	21 55
	HDA_5SS	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_5SS	HDA	HDA_RST_R_L	21
	HDA_5SS	HDA	HDA_RST_L	21 55
HDA_SDIN0	HDA_5SS	HDA	HDA_SDIN0	21 55
	HDA_5SS	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_5SS	HDA	HDA_SDOUT	21 55
	HDA_5SS	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP		MCP_HDA_COMP	MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 26
	CLK_SLOW_5SS	CLK_SLOW	PM_CLK32K_SUSCLK	26 42
SPI_CLK	SPI_5SS	SPI	SPI_CLK_R	21 44
	SPI_5SS	SPI	SPI_CLK	54
SPI_MOSI	SPI_5SS	SPI	SPI_MOSI_R	21 44
	SPI_5SS	SPI	SPI_MOSI	54
SPI_MISO	SPI_5SS	SPI	SPI_MISO	21 44
	SPI_5SS	SPI	SPI_MISO_R	54
SPI_CS0	SPI_5SS	SPI	SPI_CS0_R_L	21 44
	SPI_5SS	SPI	SPI_CS0_L	

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MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_VDD	18
MCP_MII_COMP	MCP_MII_COMP		MCP_MII_COMP_GND	18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP_CLK25M_BUF0_R	18 34
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211_CLK25M_CKXTAL1	33 34
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET_INTR_L	
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET_MDIO	18 33
ENET_MDC	ENET_MII_55S	ENET_MII	ENET_MDC	18 33
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET_PWRDWN_L	
	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK_R	33
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_RXCLK	18 33
	ENET_MII_55S	ENET_MII	ENET_RXD_R<3..0>	33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RXD<0>	18 33
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET_RXD<3..1>	18 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET_RX_CTRL	18 33
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET_CLK125M_TXCLK	18 33
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET_TXD<0>	18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TXD<3..1>	18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET_TX_CTRL	18 33
	ENET_MII_55S	ENET_MII	ENET_RESET_L	18 33
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET_MDI_P<3..0>	33 35
	ENET_MDI_100D	ENET_MDI	ENET_MDI_N<3..0>	33 35

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

SD CARD INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SD_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_INTERFACE	*	=3X_DIELECTRIC	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	36 38
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	36 38
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	36 38
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	36 38
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	36 38
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	36 38
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	36 38
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	36 38
Port 2 Not Used				

SD CARD NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
I32 SD_DATA	SD_55S	SD_INTERFACE	SD_D<0>	7 32
I31 SD_DATA	SD_55S	SD_INTERFACE	SD_D<1>	7 32
I30 SD_DATA	SD_55S	SD_INTERFACE	SD_D<2>	7 32
I29 SD_DATA	SD_55S	SD_INTERFACE	SD_D<3>	7 32
I28 SD_DATA	SD_55S	SD_INTERFACE	SD_D<4>	7 32
I27 SD_DATA	SD_55S	SD_INTERFACE	SD_D<5>	7 32
I26 SD_DATA	SD_55S	SD_INTERFACE	SD_D<6>	7 32
I25 SD_DATA	SD_55S	SD_INTERFACE	SD_D<7>	7 32
I23 SD_CLK	SD_55S	SD_INTERFACE	SD_CLK	7 32
I24 SD_CMD	SD_55S	SD_INTERFACE	SD_CMD	7 32

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5S	SMB	SMBUS_SMC_A_S3_SCL	7 45
SMBUS_SMC_A_S3_SDA	SMB_5S	SMB	SMBUS_SMC_A_S3_SDA	7 45
SMBUS_SMC_B_S0_SCL	SMB_5S	SMB	SMBUS_SMC_B_S0_SCL	45
SMBUS_SMC_B_S0_SDA	SMB_5S	SMB	SMBUS_SMC_B_S0_SDA	45
SMBUS_SMC_0_S0_SCL	SMB_5S	SMB	SMBUS_SMC_0_S0_SCL	45
SMBUS_SMC_0_S0_SDA	SMB_5S	SMB	SMBUS_SMC_0_S0_SDA	45
SMBUS_SMC_BSA_SCL	SMB_5S	SMB	SMBUS_SMC_BSA_SCL	45
SMBUS_SMC_BSA_SDA	SMB_5S	SMB	SMBUS_SMC_BSA_SDA	45
SMBUS_SMC_MGMT_SCL	SMB_5S	SMB	SMBUS_SMC_MGMT_SCL	45
SMBUS_SMC_MGMT_SDA	SMB_5S	SMB	SMBUS_SMC_MGMT_SDA	45

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	62
	1TO1_DIFFPAIR		CHGR_CSI_N	62
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	62
	1TO1_DIFFPAIR		CHGR_CSO_N	62

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=GG_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFX Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T148 LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_P	81 84
T149 LVDS_A_CLK	LVDS_100D	LVDS	LVDS_A_CLK_N	81 84
T199 LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_P<2..0>	81 84
T198 LVDS_A_DATA	LVDS_100D	LVDS	LVDS_A_DATA_N<2..0>	81 84
T152 LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_P	81 84
T153 LVDS_B_CLK	LVDS_100D	LVDS	LVDS_B_CLK_N	81 84
T151 LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_P<2..0>	81 84
T200 LVDS_B_DATA	LVDS_100D	LVDS	LVDS_B_DATA_N<2..0>	81 84
T183	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_P	7 80
T182	LVDS_100D	LVDS	LVDS_CONN_A_CLK_F_N	7 80
T184	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_P	7 80
T185	LVDS_100D	LVDS	LVDS_CONN_B_CLK_F_N	7 80
T187	LVDS_100D	LVDS	LVDS_CONN_A_CLK_P	80 81
T186	LVDS_100D	LVDS	LVDS_CONN_A_CLK_N	80 81
T192	LVDS_100D	LVDS	LVDS_CONN_A_DATA_P<2..0>	7 80 81
T193	LVDS_100D	LVDS	LVDS_CONN_A_DATA_N<2..0>	7 80 81
T194	LVDS_100D	LVDS	LVDS_CONN_B_CLK_P	80 81
T195	LVDS_100D	LVDS	LVDS_CONN_B_CLK_N	80 81
T196	LVDS_100D	LVDS	LVDS_CONN_B_DATA_P<2..0>	7 80 81
T197	LVDS_100D	LVDS	LVDS_CONN_B_DATA_N<2..0>	7 80 81
T181 DP_ML	DP_100D	DISPLAYPORT	DP_ML_C_P<3..0>	7 82
T180	DP_100D	DISPLAYPORT	DP_ML_C_N<3..0>	82
T155 DP_ML	DP_100D	DISPLAYPORT	DP_ML_P<3..0>	81 82
T157	DP_100D	DISPLAYPORT	DP_ML_N<3..0>	81 82
T202 DP_ML	DP_100D	DISPLAYPORT	DP_ML_CONN_P<3..0>	82
T203	DP_100D	DISPLAYPORT	DP_ML_CONN_N<3..0>	82
T159 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_P	81 82
T158 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX_CH_C_N	81 82

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_A_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<0>	73 74
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<0>	73 74
FB_B_CLK_P	GDDR3_80D	GDDR3_CLK	FB_A_CLK_P<1>	73 74
	GDDR3_80D	GDDR3_CLK	FB_A_CLK_N<1>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<1..0>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_MA<12..6>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_BA<2..0>	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_RAS_L	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_CAS_L	73 74
FB_AB_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_A_WE_L	73 74
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_UCKE	
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCKE	
T205 FB_AB_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_A_LCS0_L	
FB_AB_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_A_DRAM_RST	73 74
FB_A_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_LMA<5..2>	73 74
FB_B_CMD	GDDR3_40SE	GDDR3_CMD	FB_A_UMA<5..2>	73 74
FB_A_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<0>	73 74
FB_A_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<1>	73 74
FB_A_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<2>	73 74
FB_A_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<3>	73 74
FB_A_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<0>	73 74
FB_A_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<1>	73 74
FB_A_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<2>	73 74
FB_A_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<3>	73 74
FB_A_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<7..0>	73 74
FB_A_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<15..8>	73 74
FB_A_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<23..16>	73 74
FB_A_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<31..24>	73 74
FB_A_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<0>	73 74
FB_A_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<1>	73 74
FB_A_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<2>	73 74
FB_A_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<3>	73 74
FB_B_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<4>	73 74
FB_B_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<5>	73 74
FB_B_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<6>	73 74
FB_B_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_WDQS<7>	73 74
FB_B_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<4>	73 74
FB_B_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<5>	73 74
FB_B_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<6>	73 74
FB_B_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_A_RDQS<7>	73 74
FB_B_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<39..32>	73 74
FB_B_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<47..40>	73 74
FB_B_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<55..48>	73 74
FB_B_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_A_DQ<63..56>	73 74
FB_B_DQM0	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<4>	73 74
FB_B_DQM1	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<5>	73 74
FB_B_DQM2	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<6>	73 74
FB_B_DQM3	GDDR3_40SE	GDDR3_DATA	FB_A_DQM_L<7>	73 74

G96 Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
(CK505_DOT96)	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M	77
CK505_CLK27MSS	CLK_SLOW_55S	CLK_SLOW	GPU_CLK27M_SS	77
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_P	78 84
LVDS_EG_A_CLK	LVDS_100D	LVDS	LVDS_EG_A_CLK_N	78 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_P<2..0>	78 84
LVDS_EG_A_DATA	LVDS_100D	LVDS	LVDS_EG_A_DATA_N<2..0>	78 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_P<2..0>	78 84
LVDS_EG_B_DATA	LVDS_100D	LVDS	LVDS_EG_B_DATA_N<2..0>	78 84
T142 DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_P<3..0>	78 81
T144 DP_ML	DP_100D	DISPLAYPORT	DP_EG_ML_N<3..0>	78 81
T145 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_P	78 81
T143 DP_AUX_CH	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_N	78 81
T139	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_P	81
T138	DP_100D	DISPLAYPORT	DP_EG_AUX_CH_C_N	81

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FB_C_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<0>	73 75
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<0>	73 75
FB_D_CLK_P	GDDR3_80D	GDDR3_CLK	FB_B_CLK_P<1>	73 75
	GDDR3_80D	GDDR3_CLK	FB_B_CLK_N<1>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<1..0>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_MA<12..6>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_BA<2..0>	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_RAS_L	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_CAS_L	73 75
FB_CD_CMD	GDDR3_40R55SE	GDDR3_CMD	FB_B_WE_L	73 75
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_UCKE	
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCKE	
T204 FB_CD_CS0	GDDR3_40R55SE	GDDR3_CMD	FB_B_LCS0_L	
FB_CD_CMD_PD	GDDR3_40R55SE	GDDR3_CMD	FB_B_DRAM_RST	73 75
FB_C_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_LMA<5..2>	73 75
FB_D_CMD	GDDR3_40SE	GDDR3_CMD	FB_B_UMA<5..2>	73 75
FB_C_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<0>	73 75
FB_C_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<1>	73 75
FB_C_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<2>	73 75
FB_C_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<3>	73 75
FB_C_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<0>	73 75
FB_C_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<1>	73 75
FB_C_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<2>	73 75
FB_C_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<3>	73 75
FB_C_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<7..0>	73 75
FB_C_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<15..8>	73 75
FB_C_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<23..16>	73 75
FB_C_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<31..24>	73 75
FB_C_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<0>	73 75
FB_C_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<1>	73 75
FB_C_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<2>	73 75
FB_C_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<3>	73 75
FB_D_WDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<4>	73 75
FB_D_WDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<5>	73 75
FB_D_WDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<6>	73 75
FB_D_WDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_WDQS<7>	73 75
FB_D_RDQS0	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<4>	73 75
FB_D_RDQS1	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<5>	73 75
FB_D_RDQS2	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<6>	73 75
FB_D_RDQS3	GDDR3_40SE	GDDR3_DQS	FB_B_RDQS<7>	73 75
FB_D_DQ_BYTE0	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<39..32>	73 75
FB_D_DQ_BYTE1	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<47..40>	73 75
FB_D_DQ_BYTE2	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<55..48>	73 75
FB_D_DQ_BYTE3	GDDR3_40SE	GDDR3_DATA	FB_B_DQ<63..56>	73 75
FB_D_DQM0	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<4>	73 75
FB_D_DQM1	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<5>	73 75
FB_D_DQM2	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<6>	73 75
FB_D_DQM3	GDDR3_40SE	GDDR3_DATA	FB_B_DQM_L<7>	73 75

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

PAGE TITLE
GPU (G96) CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-7892 SIZE D
REVISION C.0.0
BRANCH
PAGE 107 OF 109
SHEET <CURRENT_DESIGN_SHEET> OF <TOTAL_DESIGN_SHEETS>

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

PGA CONSTRAINT RELAXATIONS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PGA_50SE	*	Y	=50_OHM_SE	0.073 MM	=50_OHM_SE	=1:1_DIFFPAIR	0.073 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FSB_50S	PGA	PGA_50SE
FSB_DSTB_50S	PGA	PGA_50SE
CPU_50S	PGA	PGA_50SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_DATA	*	PGA	PGA_CPU
FSB_DSTB	*	PGA	PGA_CPU
FSB_ADDR	*	PGA	PGA_CPU
FSB_ADSTB	*	PGA	PGA_CPU
FSB_1X	*	PGA	PGA_CPU
CPU_AGTL	*	PGA	PGA_CPU
CPU_SM1L	*	PGA	PGA_CPU

K19 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_MDI_100D	ENETCONN	ENETCONN_P<3..0>	35
	ENET_MDI_100D	ENETCONN	ENETCONN_N<3..0>	35
J140	SATA_100D	SATA	SATA_ODD_R2D_UF_P	39
J145	SATA_100D	SATA	SATA_ODD_R2D_UF_N	39
J144	SATA_100D	SATA	SATA_ODD_D2R_UF_P	7 39
J142	SATA_100D	SATA	SATA_ODD_D2R_UF_N	7 39
J143	SATA_100D	SATA	SATA_HDD_D2R_UF_P	39
J140	SATA_100D	SATA	SATA_HDD_D2R_UF_N	39
J141	SATA_100D	SATA	SATA_HDD_R2D_UF_P	39
J139	SATA_100D	SATA	SATA_HDD_R2D_UF_N	39
	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_P	79
	SENSE_1TO1_55S	SENSE	GFXIMVP6_VSEN_N	79
J32	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	48
J31	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	48
J37	THERM_1TO1_55S	THERM	CPU_THERMD_P	10 48
J36	THERM_1TO1_55S	THERM	CPU_THERMD_N	10 48
J34	THERM_1TO1_55S	THERM	GPUTHMSNS_D_P	48
J33	THERM_1TO1_55S	THERM	GPUTHMSNS_D_N	48
J35	THERM_1TO1_55S	THERM	GPU_TDIODE_P	48 77
J38	THERM_1TO1_55S	THERM	GPU_TDIODE_N	48 77
K38	THERM_1TO1_55S	THERM	MCPTHMSNS_D_P	48
K37	THERM_1TO1_55S	THERM	MCPTHMSNS_D_N	48
K35	THERM_1TO1_55S	THERM	MCP_THMDIODE_P	21 48
K36	THERM_1TO1_55S	THERM	MCP_THMDIODE_N	21 48
E156	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_P	47
E157	SENSE_1TO1_55S	SENSE	CPUVTTISNS_R_N	47
E153	SENSE_1TO1_55S	SENSE	GPUISENS_P	47
E152	SENSE_1TO1_55S	SENSE	GPUISENS_N	47
E151	SENSE_1TO1_55S	SENSE	CPUVTT_ISNS_P	47 67
E150	SENSE_1TO1_55S	SENSE	CPUVTT_ISNS_N	47 67
E158	SENSE_1TO1_55S	SENSE	P1V8GPU_P	47
E147	SENSE_1TO1_55S	SENSE	P1V8GPU_N	47
E146	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	46
E145	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	46
		SB_POWER	PP3V3_S5	7 8
		SB_POWER	PP3V3_S0	7 8
E44	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_P	47
E43	SENSE_1TO1_55S	SENSE	P1V8GPUISNS_R_N	47
E24	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_P	31 53
E20	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_N	31 53
E23	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_P	53
E24	SENSE_1TO1_55S	SENSE	ISNS_AIRPORT_R_N	53
E21	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_P	53
E17	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_R_N	53
E16	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_P	53 65
E41	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_N	53 65
E19	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	53 85
E13	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	53 85
E19	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_P	
E22	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_R_N	

K19 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
E164 (PCIE EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P	90
E165 (PCIE EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N	90
E163	PCIE_90D	PCIE	PCIE_MINI_R2D_P	7 31 90
E161 (PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_N	7 31 90
E160 (PCIE_MINI)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P	7 31
E159	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N	7 31
E168	1TO1_DIFFPAIR		CHGR_CSI_R_P	62
E166	1TO1_DIFFPAIR		CHGR_CSI_R_N	62
E167	1TO1_DIFFPAIR		CHGR_CSO_R_P	46 62
E165	1TO1_DIFFPAIR		CHGR_CSO_R_N	46 62
E182 (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_P	40
E181 (USB_EXTA)	USB_90D	USB	USB2_EXTA_MUXED_N	40
E179 (USB_EXTA)	USB_90D	USB	USB2_LT1_P	40
E180 (USB_EXTA)	USB_90D	USB	USB2_LT1_N	40
E177 (USB_EXTD)	USB_90D	USB	USB_TPAD_R_P	50
E178 (USB_EXTD)	USB_90D	USB	USB_TPAD_R_N	50
E176 (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P	7 31
E175 (USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N	7 31
E174	USB_90D	USB	CONN_USB2_BT_P	7 31
E172	USB_90D	USB	CONN_USB2_BT_N	7 31
E173	USB_90D	USB	USB_LT2_P	40
E171	USB_90D	USB	USB_LT2_N	40
E189 USB_CARDREADER	USB_90D	USB	USB_CARDREADER_P	9 20 32
E170	USB_90D	USB	USB_CARDREADER_N	9 20 32
E183	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_P	81
E184	DP_100D	DISPLAYPORT	DP_IG_AUX_CH_C_N	81
E198 SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P	7 58 59
E197	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N	7 58 59
E201 SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_P	7 58 59
E200	DIFFPAIR	AUDIO	SPKRCONN_S_OUT_N	7 58 59
E199 SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P	7 58 59
E202	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N	7 58 59
E206	DIFFPAIR	AUDIO	SPKRAMP_L_OUT_P	58
E207	DIFFPAIR	AUDIO	SPKRAMP_L_OUT_N	58
E204	DIFFPAIR	AUDIO	SPKRAMP_R_OUT_P	58
E205	DIFFPAIR	AUDIO	SPKRAMP_R_OUT_N	58
E208	DIFFPAIR	AUDIO	SPKRAMP_S_OUT_P	58
E203	DIFFPAIR	AUDIO	SPKRAMP_S_OUT_N	58
E222 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	39 53
E223	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	39 53
E220 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	53
E221	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	53
E218 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	39 53
E219	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	39 53
E216 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	53
E217	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	53
		GND	GND	

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	5.8 MM OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE
USB_90D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MEM_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_MII_COMP OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_USB_RBIAS OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
MCP_DV_COMP OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.25 MM OVERRIDE	250 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	BOTTOM OVERRIDE	OVERRIDE	OVERRIDE	0.23 MM OVERRIDE	100 MIL OVERRIDE	OVERRIDE	OVERRIDE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_40S_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	ISL4,ISL9 OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D_VDD OVERRIDE	ISL3,ISL10 OVERRIDE	N OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island.
Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

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PAGE TITLE: Project Specific Constraints

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K19 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,PGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	33.6 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?
PGA_CPU	*	0.073 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE:From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9,ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2,ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2,ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2,ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

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