1. All resistance values are in ohms; 0.1 watt or less.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.

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**Revision History**

- **07/23/2010**
  - Initial version

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- 051-8467

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**www.vinafix.vn**
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Revision History
Profo 0 (ECO #0000876215, v1.0.0, P4 change #210266, 03/16/2010)

v1.1.0 (P4 change #211539, 03/24/2010)
- 7754205 - Asked NC to DCC pass FETs to avoid glitch (pp. 7, 93).
- 7781316 - Added feedback divider and BOM tables for more VSSC loads (pp. 4, 25).
- 7754217 - Added resistors to connect TCON to DMB or MCP SMBus (pp. 4, 54, 90).
- 7754221 - Added support for DP MDP mode / FT state (pp. 8, 10, 19, 45, 50, 76, 94).
- 7754246 - Added SI pull-up to SMB_IOL to prevent leakage path (pp. 50, 59).
- 7754251 - Unstuffed BOM circuit (pp. 8).
- 7754279 - Property/page files to reduce SeekPlus warning/errors (pp. 7, 9, 12, 17, 74, 93, 108).

v2.0.0 (P4 change #211673, 03/24/2010)
- 7754626 - Changed port switch from TP20528 to TP20548 (pp. 44).
- 7883293 - Added BLACK从来没 property on R5022 to avoid side effects.

v2.1.0 (P4 change #211978, 03/26/2010)
- 7754658 - Changed DP and LCD power from supply power supply (pp. 8, 90).
- 7754685 - Changed backlight driver to E0 version (pp. 97).
- 7754694 - Added SMBUSREN property to SMBUS device (pp. 44).
- 7754695 - Added SMBUSREN property to SMBUS device (pp. 44).
- 7754696 - Added SMBUSREN property to SMBUS device (pp. 44).
- 7754697 - Added alternate PBT and unstuffed series N's on TCON I2C for now (pp. 4, 90, 108).

Power Supply:
- 7754641 - Removed alternate PBT, made some PBTs primary to other APs (pp. 4, 72, 73, 74).
- 7754642 - Reflux changes for 5.12V CNN power supply (pp. 45).
- 7754649 - A reflux changes for 5.12V CNN power supply (pp. 45).
- 7754650 - A reflux changes for 5.12V CNN power supply (pp. 45).
- 7754657 - A reflux changes for 5.12V CNN power supply (pp. 45).
- 7754660 - Changed backlight driver to non-E00 version (pp. 4, 97).

v1.3.0 (P4 change #212175, 03/30/2010)
- 7754706 - Changed HSYNC to 25 MHz bus frequency (pp. 4).
- 7764331 - Added VREF connection to BBUS alias page (pp. 15, 52).
- 7764350 - Changed VREF "SMBUS" SMBUS pull-ups from 0.12 to 2K (pp. 52).
- 7764351 - Documented SMBUS addresses for panel (pp. 52).
- 7764352 - Changed SD Card discharge R to more standard value (pp. 48).

Power Supply:
- 7754736 - Changed 5V/3.3 regulator output from 5.02V to 5.12V nominal (pp. 48).
- 7754748 - Added SDSD circuit and clarified tables/BOM tables around these parts (pp. 45).
- 7754750 - Changed OMI to OMITp tables (pp. 10-11, 14-20, 24, 31-36, 45, 61).

v2.1.0 (P4 change #212175, 03/30/2010)
- 7754649 - Changed OMI to OMITp tables (pp. 10-11, 14-20, 24, 31-36, 45, 61).

REVISION HISTORY

type: v1.1.0 (P4 change #210439, 03/04/2010)
- 7787897 - Property/page files to reduce SeekPlus warning/errors (pp. 7, 9, 12, 17, 74, 93, 108).

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NOTE: All page numbers are .cda, not PDF. See page 1 for .cda -> PDF mapping.
Micro2-XDP Connector

Note: This is not the standard XDP pinout.

Use with 500-0782 Adapter Flex to support chipset debug.

Direction of XDP adapter flex

Place close to CPU to minimize stub.

PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
PE1 ports are Gen1-only. 2 RCs: x1, x1

+VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND if PE0[3:0] are not used.
+VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND if PE0[4:5] and PE1[0:1] are not used.
NOTE: No Composite/S-Video/Component Video support on MCP89

Connect +3.3V_RGBDAC pin to GND.

Okay to float all RGB_DAC signals.

RGB DAC Disable:

TMDS: Power +VDD_IFPx at 3.3V
LVDS: Power +VDD_IFPx at 1.8V

DDC Mode Pull-downs
NOTE: DP_MODE only required pull-downs if used for
dual-mode displayport (DP++) - if unused no pulls
are necessary. If used for TMDS/NODE only then
only pull-ups are necessary.

GPIO Pull-Ups


Connect RGMII_MDIO to 10K pull-down.
All other pins can be left TP or NC.
Connect RGMII_RXCTL to 10K pull-down.
Connect RGMII_VREF to 10K pull-down.
RGMII_COMP_VDD/_GND must remain connected as shown.
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
Connect RGMII_INTR to 10K pull-down (if not used as GPIO).
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXD<0:3> together to 10K pull-down.
Internal MAC Disable:
Connect RGMII_RGMII to 10K pull-down.
Connect RGMII_RGMII to 10K pull-down (if not used as GPIO).
+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
RGMII_COMP_VDD/_GND must remain connected as shown.
Connect RGMII_RXCLK to 10K pull-down.
Connect RGMII_RXD2 to 10K pull-down.
All other pins can be left TP or NC.

MCP SATA, USB & Ethernet
NOTE: "SW" rails are dynamically switched in the S0 state as needed, controlled by MCP89 GPIOs.
NO STUBS on CKE signals!

CKE must be held low to keep memory in self-refresh.

Clamps enable when MCP89 MEMVDD rail switched off.

Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.

Clamps are chosen for low output capacitance.

Approx. Ramp Time (VCC to 1.35V, uS): 7.91 + 0.0678 * R1 (Kohms)

Approx. Ramp Time (VCC to 1.35V, uS): 7.91 + 0.0678 * R1 (Kohms)

Gated Rail Savings: 120mW

**DIMM CKE Clamps**

- Q2355/Q2356 chosen for low output capacitance.
- Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
- Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.

**Clamp Requirements:**

- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

**Loading (G driven to VCC):**

- C2300 helps reduce input rail droop during Q2300 turn-on.
- C2300 helps reduce input rail droop during Q2300 turn-on.

**NOTE:** nVidia recommends Infineon BSC030N03MS for Q2300.

- **Ramp-Up Time:** Min: 20 uS (10% to 90%)
- Max: 65 uS (90% to 100%)
- **FET Ron:** <= 3.8 mOhms

**4250 mA (OR 1.35V)**

**Q2300**

- **Type:** N-Channel
- **Part:** STMFS4854N
- **N-Channel**
- **Rds(on):** 10 mOhms @3.2V
- **4.3 A (EDP)**

**44**

**44**

**MF**

**560K**

**1%1/20W**

**201**

**R2305**

Approx. Ramp Time (VCC to 1.35V, uS): 7.91 + 0.0678 * R1 (Kohms)

**19 58**

**0.1UF**

**402CERM10V20%**

**C2305**

**CRITICAL**

**PLACE_NEAR=Q2300.9:2 mm**

**1206-1CERM-X5R 6.3V20%**

**100UF**

**C2300**

**CRITICAL**

**TDFN**

**SLG5AP031**

**NTUD3170NZXXG**

**Q2350**

**SOT-963**

**CRITICAL**

**PLACE_NEAR=Q2300.9:2 mm**

**1206-1CERM-X5R 6.3V20%**

**100UF**

**C2300**

**CRITICAL**

**TDFN**

**SLG5AP031**

**NTUD3170NZXXG**

**Q2355**

**SOT-963**

**CRITICAL**

**PLACE_NEAR=Q2300.9:2 mm**

**1206-1CERM-X5R 6.3V20%**

**100UF**

**C2300**

**CRITICAL**

**TDFN**

**SLG5AP031**

**NTUD3170NZXXG**

**Q2356**

**SOT-963**

**CRITICAL**

**PLACE_NEAR=Q2300.9:2 mm**

**1206-1CERM-X5R 6.3V20%**

**100UF**

**C2300**

**CRITICAL**

**TDFN**

**SLG5AP031**

**NTUD3170NZXXG**

**Q2300**
Approx. Ramp Time (EN to 1V, uS): \(43.9 + 0.6943 \times C1(pF)\)

- Min Ramp-Up Time: 100 uS (10% to 90%)
- Max Ramp-Up Time: 1500 uS (ENABLE to 90%)
- FET Ron <= 2.5 mOhms

**NOTE:** nVidia recommends Infineon BSC020N03MS for Q2400.

- C2400 helps reduce input rail droop during Q2400 turn-on.
- MCPCORES0_VSEN_P
- MCPCORES0_VSEN_N

- Gated Rail Savings: 860mW

The NV Requirements:
- Place Near=C2400.1:1 mm
- PLACE_NEAR=C2400.2:1 mm

**Critical Components:**
- XW2400
- XW2401
- SI4838BDY
- SLG5AP033

**NOTE:** Infineon recommends ROHS4BBMS2 for Q2400.

**MCP89 GFX Core Rail Gating**

- PPVCORE_S0_MCPGSBFET
- PPVCORE_SW_MCP_GFX
- S0_PP_MCP_GFX
- PP5V_S0_MCPFSBFET
- SLG5AP033
- XW2400
- XW2401
- SI4838BDY
- UC405
- UC405
- SLG5AP033

**MCPGFX_GATE**

- PPVCORE_S0_MCPGSBFET
- PPVCORE_SW_MCP_GFX
- S0_PP_MCP_GFX
- PP5V_S0_MCPFSBFET

**PPVCORE_S0_MCPGSBFET**

- PPVCORE_S0_MCPGSBFET
- PP5V_S0_MCPFSBFET
- S0_PP_MCP_GFX
- PP5V_S0_MCPFSBFET

**PPVCORE_SW_MCP_GFX**

- PPVCORE_S0_MCPGSBFET
- PP5V_S0_MCPFSBFET
- S0_PP_MCP_GFX
- PP5V_S0_MCPFSBFET

**SLG5AP033**

- SLG5AP033
- XW2400
- XW2401
- SI4838BDY
- UC405
- UC405
- SLG5AP033

**XW2400**

- XW2400
- XW2401
- SI4838BDY
- UC405
- UC405
- SLG5AP033

**SI4838BDY**

- SI4838BDY
- XW2400
- XW2401
- UC405
- UC405
- SLG5AP033

**UC405**

- UC405
- UC405
- SLG5AP033
- XW2400
- XW2401
- SI4838BDY

**SLG5AP033**

- SLG5AP033
- XW2400
- XW2401
- SI4838BDY
- UC405
- UC405

**UC405**

- UC405
- UC405
- SLG5AP033
- XW2400
- XW2401
- SI4838BDY

**SI4838BDY**

- SI4838BDY
- XW2400
- XW2401
- UC405
- UC405
- SLG5AP033

**UC405**

- UC405
- UC405
- SLG5AP033
- XW2400
- XW2401
- SI4838BDY

**SLG5AP033**

- SLG5AP033
- XW2400
- XW2401
- SI4838BDY
- UC405
- UC405

www.vinafix.vn
JEDEC recommends 30 Ohm term to VTT for CS, CKE, ODT and 36 Ohm for BA, A, RAS, CAS, WE.
K4805 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4805 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4804 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4803 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4802 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4801 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4800 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4797 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4796 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4795 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4794 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4793 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4792 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4791 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4790 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4789 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4788 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!

R4787 is for rail discharge. GL137 may cycle PMOS to recover from card error. DEF duration is 1ms and reset voltage must be less than 0.5V for at least 10us per spec. Keep this net short!
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
SMC Reset “Button”, Supervisor & AVREF Supply

SMC Crystal Circuit

System (Sleep) LED Circuit

Debug Power “Buttons”

SMC Aliases

SMC Pull-ups

SMC Pull-downs

Unused Pins

SMC Support

Apple Inc.

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Another slave port is available at 0x10/0x11, probably not used.

MCP89 SMBus "0" Connections

SMC "0" SMBus Connections

SMC "Battery A" SMBus Connections

SMC "Management" SMBus Connections

Left I/O Board

Internal DP

Battery

Trackpad

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FAN CONNECTOR
NOTE: If HOLD* is asserted, ROM will ignore SPI cycles.

NOTE: SPI ROM

SYNC_MASTER=K99_MLB
SYNC_DATE=04/08/2010

==PP3V3_S5_ROM==

SPI_ROM

MCP89 SPI Frequency Select:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
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</thead>
<tbody>
<tr>
<td>25.0 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>31.2 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>41.7 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>62.5 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

NOTE: 42 & 62 MHz use FAST_READ command.
Vin = 5.0V
F = 400KHz

CRITICAL POLY-TANT 150UF 6.3V

PLACE_NEAR = L7220.1:3mm

X7R16V 10%
C7250
P5VS3_VFB1-R 805

CRITICAL PCMC063T-SM L7220

PLACE_NEAR = L7220.2:3mm

R7221
R7220 201 MF 1/20W 1%

C7240 62UF XW7222 11V ELEC 20%

MIN_NECK_WIDTH = 0.2 mm
MIN_LINE_WIDTH = 0.6 mm DIDT = TRUE

MF-LF 52

C7200
C7236 0.01UF 5% 201 1%

52 52

1UF 402 16V X5R 10%
Q7220 HWSON-8

GATE_NODE = TRUE DIDT = TRUE
MIN_NECK_WIDTH = 0.2 mm
MIN_LINE_WIDTH = 0.6 mm

MIN_LINE_WIDTH = 0.6 mm DIDT = TRUE
SWITCH_NODE = TRUE

58 58

P3V3S5_PGOOD
P5VS3_PGOOD

58 58

IN

C7201

5% R7237 20K

NO STUFF 201 1/20W 1%

100PF 1UF 402 16V X5R 10%

58 58

5.3A MAX OUTPUT Vout = 3.3V

= PP3V3_S5_REG

SYNC_DATE = 04/08/2010

Apple Inc.
NOTE: Pulled up to 5V on DP connector page.

FET spec'ed for 1.5V Vgs operation.

6.3V 0.1UF 10% X5R C9300

6.3V 0.1UF 10% X5R C9301

SSM6N37FEAPE SOT563 SIGNAL_MODEL=DP_AUXCH_FET Q9302

SSM6N37FEAPE SOT563 SIGNAL_MODEL=DP_AUXCH_FET Q9300

CKPLUS_WAIVE=PdifPr_badTerm SIGNAL_MODEL=DP_AUXCH_FET

SYNC_DATE=04/08/2010 SYNCHRONIZED=K99_MLB

External DisplayPort Support
### CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
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<tbody>
<tr>
<td>FSB_55S</td>
<td>100 Ohm</td>
<td>55 Ohm</td>
<td>25 Mil</td>
<td>&gt;50 Mil</td>
</tr>
<tr>
<td>FSB_1X</td>
<td>27 OhmSE</td>
<td>27 OhmSE</td>
<td>25 Mil</td>
<td>&gt;50 Mil</td>
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</table>

### CPU Signal Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_55S</td>
<td>55 OhmSE</td>
<td>55 OhmSE</td>
<td>25 Mil</td>
<td>&gt;50 Mil</td>
</tr>
<tr>
<td>CPU_8MIL</td>
<td>8 Mil</td>
<td>8 Mil</td>
<td>25 Mil</td>
<td>&gt;50 Mil</td>
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</tbody>
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### MCP FSB COMP Signal Constraints

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<thead>
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<th>Name</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
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</thead>
<tbody>
<tr>
<td>MCP_CPU_COMP</td>
<td>55 OhmSE</td>
<td>55 OhmSE</td>
<td>25 Mil</td>
<td>&gt;50 Mil</td>
</tr>
<tr>
<td>MCP_CPU_COMP_VCC</td>
<td>55 OhmSE</td>
<td>55 OhmSE</td>
<td>25 Mil</td>
<td>&gt;50 Mil</td>
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### FSB Clock Constraints

<table>
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<th>Name</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_MCP</td>
<td>15 Ohm</td>
<td>15 Ohm</td>
<td>10 Mil</td>
<td>&gt;25 Mil</td>
</tr>
<tr>
<td>FSB_CLK_ITP</td>
<td>15 Ohm</td>
<td>15 Ohm</td>
<td>10 Mil</td>
<td>&gt;25 Mil</td>
</tr>
</tbody>
</table>

### Source Information

- MCP89 Interface DG (DG-04625-001_v0.9), Section 2.1.4
- Intel Design Guide allows closer spacing if signal lengths can be shortened.
- Intel Design Guide recommends FSB signals be routed only on internal layers.
Digital Video Signal Constraints

- R/G/B signals should be matched as close as possible and < 10 inches.
- 50-ohm from first to second termination resistor.

Analog Video Signal Constraints

- CRT signals single-ended impedance varies by location:
  - 50-ohm from first to second termination resistor.
  - 75-ohm from output of three-pole filter to connector (if possible).
- CRT signals should be matched as close as possible and ~10 inches.

NEED PCIe Gen1/Gen2 notes!

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.3

SOURCE: MCP89 Interface DG (DG-04625-001_v0.9), Section 2.4.2

Max trace length: 12 inches for SATA Gen1/Gen2, TBD for SATA Gen3.

SATA intra-pair matching should be 1 ps.

DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 100 ps.

Max trace length: LVDS 10 inches, DP 8.5 inches.

NOTE: NV DG recommends 90 ohm differential for LVDS, but cable/display assume 100 ohm.
### LPC Bus Constraints

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### USB 2.0 Interface Constraints

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<th>Layer</th>
<th>USB Min/Max</th>
<th>Line-to-Line Spacing</th>
<th>Physical Rule Set</th>
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<tbody>
<tr>
<td>A</td>
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<tr>
<td>B</td>
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<tr>
<td>D</td>
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### SMBus Interface Constraints

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<th>Physical Rule Set</th>
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<tbody>
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### HD Audio Interface Constraints

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<th>Layer</th>
<th>HD Min/Max</th>
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<td>D</td>
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### SIO Signal Constraints

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<th>Physical Rule Set</th>
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### SPI Interface Constraints

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<th>Physical Rule Set</th>
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**MCP89 Net Properties**

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<th>Layer</th>
<th>Min/Max</th>
<th>Net Name</th>
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<tr>
<td>SMC SMBus Net Properties</td>
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<td>---------------------------</td>
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<tr>
<td>NET_ID</td>
<td>PROPERTIES</td>
<td>VALUE</td>
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<td>SMBUS_MGMT_SDA</td>
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<td>0.1 MM</td>
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<tr>
<td>SMBUS_MGMT_SCL</td>
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</tr>
<tr>
<td>SMBUS_A_S3_SCL</td>
<td>PHYSICAL_SPACING</td>
<td>0.1 MM</td>
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<td>SMBUS_A_S3_SDA</td>
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<td>0.1 MM</td>
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<td>SMBUS_B_S0_SCL</td>
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<td>SMBUS_B_S0_SDA</td>
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<td>SMBUS_B_SA_SDA</td>
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<td>SMBUS_A_SA_SDA</td>
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<td>SMBUS_A_SA_SCL</td>
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<td>0.1 MM</td>
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</table>

| SMBus Charger Net Properties | | |
|-----------------------------|-------------------|
| NET_ID | PROPERTIES | VALUE |
| CHGR_CSI | 1TO1_DIFFPAIR | |
### Graphics Net Properties

<table>
<thead>
<tr>
<th>Net_Name</th>
<th>Type</th>
<th>Position</th>
<th>Net type</th>
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<tbody>
<tr>
<td>DP_90D</td>
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<tr>
<td>DP_EXT_ML_N&lt;3..0&gt;</td>
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<td>DP_EXT_AUX_CH_C_P</td>
<td>PHYSICAL</td>
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### Audio Net Properties

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### Power Net Properties

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### SD CARD READER LAYOUT RELAXATIONS

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### MCP Fanout Constraint Relaxations

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# Capacitor Vendor Tables for Acoustics

## 1UF 0402

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<th>Part Number</th>
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