SCHEMATIC, "ANGEL ISLAND", MLB
Rev.A 02/23/10

1. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
2. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
### Bar Code Labels / EEEE #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>SUPPLIER REF</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>826-5132</td>
<td>2</td>
<td>376S0887</td>
<td>Kemet</td>
<td>CRITICAL</td>
<td>EEE_5132y</td>
</tr>
<tr>
<td>826-5132</td>
<td>2</td>
<td>376S0749</td>
<td>Taiyo Yuden</td>
<td>CRITICAL</td>
<td>EEE_5132y</td>
</tr>
<tr>
<td>127S0111</td>
<td>12</td>
<td>155S0457</td>
<td>Rohm</td>
<td>CRITICAL</td>
<td>EEE_127S0111</td>
</tr>
<tr>
<td>138S0603</td>
<td>1</td>
<td>155S0329</td>
<td>Taiyo Yuden</td>
<td>CRITICAL</td>
<td>EEE_138S0603</td>
</tr>
<tr>
<td>155S0329</td>
<td>2</td>
<td>152S0915</td>
<td>Murata</td>
<td>CRITICAL</td>
<td>EEE_155S0329</td>
</tr>
<tr>
<td>152S0796</td>
<td>2</td>
<td>152S0518</td>
<td>Murata</td>
<td>CRITICAL</td>
<td>EEE_152S0796</td>
</tr>
<tr>
<td>157S0058</td>
<td>2</td>
<td>157S0055</td>
<td>Murata</td>
<td>CRITICAL</td>
<td>EEE_157S0058</td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>REF DES</th>
<th>ALTERNATE FOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>127S0060</td>
<td>12</td>
<td>127S0060</td>
<td>Rohm alt to Kemet</td>
</tr>
<tr>
<td>138S0602</td>
<td>12</td>
<td>138S0602</td>
<td>Taiyo Yuden alt to Samsung</td>
</tr>
<tr>
<td>138S0602</td>
<td>12</td>
<td>138S0612</td>
<td>Fairchild 8 in alt to 6 in wafer</td>
</tr>
<tr>
<td>138S0602</td>
<td>12</td>
<td>138S0612</td>
<td>Delta alt to TDK Magnetics</td>
</tr>
<tr>
<td>138S0602</td>
<td>12</td>
<td>138S0612</td>
<td>Murata alt to Samsung</td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE REF</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>2772812</td>
<td>1</td>
<td>341T0229</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>FPGA,2.66GHZ,512SAM_VRAM,K17</td>
</tr>
<tr>
<td>2772845</td>
<td>1</td>
<td>337S3849</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>IC,ASIC,BCM5764M,ENET CONTROLLER,8x8,64 QFN</td>
</tr>
<tr>
<td>2772845</td>
<td>1</td>
<td>337S3849</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>LBL,P/N LABEL,PCB,28MM X 6 MM</td>
</tr>
<tr>
<td>2772845</td>
<td>1</td>
<td>337S3849</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>LBL,P/N LABEL,PCB,28MM X 6 MM</td>
</tr>
<tr>
<td>2772845</td>
<td>1</td>
<td>337S3849</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>LBL,P/N LABEL,PCB,28MM X 6 MM</td>
</tr>
<tr>
<td>2772845</td>
<td>1</td>
<td>337S3849</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>LBL,P/N LABEL,PCB,28MM X 6 MM</td>
</tr>
<tr>
<td>2772812</td>
<td>1</td>
<td>343S0493</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>I/O,ENCORE II, CY7C63833-LFXC</td>
</tr>
<tr>
<td>2772812</td>
<td>1</td>
<td>343S0493</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>IC,XP2-5,HF,CPLD,BLANK</td>
</tr>
<tr>
<td>2772812</td>
<td>1</td>
<td>343S0493</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>ARD,SLBPE,PRQ,2.66,35W,C2,4M,BGA</td>
</tr>
<tr>
<td>2772812</td>
<td>1</td>
<td>343S0493</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>ARD,SLBPF,PRQ,2.53,35W,C2,3M,BGA</td>
</tr>
<tr>
<td>2772812</td>
<td>1</td>
<td>343S0493</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>IBEX (HM55),SLGZS,PRQ,B3</td>
</tr>
<tr>
<td>2772812</td>
<td>1</td>
<td>343S0493</td>
<td>K17MLB</td>
<td>CRITICAL</td>
<td>IC,TP PSOC,K17,K18</td>
</tr>
</tbody>
</table>

### BOM Options

<table>
<thead>
<tr>
<th>BOM NUMBER</th>
<th>PART NUMBER</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>826-4393</td>
<td>826-4393</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>826-4393</td>
<td>826-4393</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>826-4393</td>
<td>826-4393</td>
<td>CRITICAL</td>
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<td>CRITICAL</td>
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<td>CRITICAL</td>
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<td>826-4393</td>
<td>826-4393</td>
<td>CRITICAL</td>
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<tr>
<td>826-4393</td>
<td>826-4393</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>
NOTE: VCAP1 is sourced by CPU
but provide bypass caps on PCB.

Do not connect to power supply,
NOTE: VCAP2 is sourced by CPU but provide bypass caps on PCB.
VCAK2 (CPU BSC Package) DECOUPLING

PLACEMENT NOTE (C2524-C2539):
Place on bottom side of U1000.

PLACEMENT NOTE (C2500-C2506):
GFX (CPU VCCAXG) DECOUPLING

C2510
1UF
10V
X5R

C2511
1UF
10V
X5R

C2513
1UF
10V
X5R

C2526
1UF
10V
X5R

C2530
1UF
10V
X5R

C2532
1UF
10V
X5R

C2533
1UF
10V
X5R

C2534
1UF
10V
X5R

C2536
1UF
10V
X5R

C2537
1UF
10V
X5R

C2538
1UF
10V
X5R

C2539
1UF
10V
X5R

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SYNC_MASTER=K17_WFERRY
SYNC_DATE=06/09/2009
PLACEMENT NOTE=Place R2601 close to R2600 to minimize stubs.

NOTE: This is not the standard XDP pinout. Use with 925-0762 adapter flex to support PCH debugging.

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

34 37 40 42 47 48 49 52 53

PP3V3_S0

516s0806

SPD ADDR=0xA4(WR)/0xA5(RD)

VDD

VSS

VSS

VSS

VDD

F-RT-BGA6
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's GPU power output from the S0-DIMM when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

MEMVTT Clamp
Enables CRE signals are held low in S3

1V5 S0 "PGOOD" for CPU

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SYNC_MASTER=K18_MLB

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CPU Memory S3 Support

Apple Inc.

NOTE: In the event of a S3->S0 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.
Page Notes

BOM options provided by this page:
- PPBUS_S5_FWPWRSW (system supply for bus power)
- PPVP_FW_SUMNODE (power passthru summation node)
- PP3V3_FW_LATEVG_ACTIVE

Signal aliases required by this page:
101 39 40 41 7

Page Notes
Port Power Switch

Enable tied low so input power source must be 5V!!!

LEFT USB PORT C

PROJECT SPECIFIC CONNS

SYNC_MASTER=K20A_MLB
SYNC_DATE=03/26/2009

USB_EXTC_P
USB_EXTC_N

VOLTAGE=5V
MIN_NECK_WIDTH=0.375 mm
MIN_LINE_WIDTH=0.5 mm

PP5V_S3_RTUSB_C_F
PP5V_S3_RTUSB_C_ILIM
PP5V_S3

6 99 6 99

CRITICAL

C4720
0.1uF
CERM402
16V

PLACE_NEAR=J4720.2:8mm

C4725
0.01uF
CERM402
16V

PLACE_NEAR=J4720.1:8mm

L4725
FERR-220-OHM-2.5A
0603

CRITICAL

L4720
90-OHM-100MA
DLP11S

D4720
CRITICAL
RCLAMP0502N
SLP1210N6

U4780
CRITICAL
MSOP
TPS2068

J4720
USB

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**CPU Proximity/CPU Die/PCH Proximity/Battery Charger Proximity**

Detect CPU Die Temperature
- Place Q5502 on bottom side
- Close to battery charger circuit

Detect Battery Charger Proximity Temperature
- Place Q5501 on bottom side
- Close to the right fin stack

Detect PCH Proximity Temperature
- Place Q5504 under PCH

**GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack**

Detect GPU Die Temperature
- Place U5570 under CPU
- Close to GPU Proximity/GPU Die/Left Heat Pipe/Right Fin Stack

Detect Right Fin Stack Temperature
- Place Q5503 on bottom side
- Close to the right fin stack

Detect Left Heat Pipe Temperature
- Place Q5501 on bottom side
- Close to battery charger circuit

**Thermal Sensors**

- CPU Proximity
- CPU Die
- PCH Proximity
- Battery Charger Proximity

**Note:** EMC1414 can perform Beta Compensation for External Diode 1 only.

**Read Address:** 0x99
**Write Address:** 0x98

**Sync Master:** K17 CHENG
**Sync Date:** 07/08/2009
BOoster +18.5Vdc for sensors

To detect keyboard backlight, SMC will.

LOW = keyboard backlight present

HIGH = keyboard backlight not present

R5853 ALWAYS PRESENT

PP5v_S3

R5801 1 2

1/10W 5%

C5800 0.1UF 402

CERM 10V

R5802

1 2

1/10W 5%

PLACE_NEAR = J5800.2:5mm

PP3V3_S0

C5816 0.1UF 16V 402 X7R-CERM 10%

MF-LF 1/16W 5%

470K

INPUT_SW

C5817 603 X5R 16V 10%

0.20MM 0.50MM

NO STUFF

PP5v_S0

MF-LF 402 1/16W 10K

3.3UH - 870MA

THRM

VLF3010AT-SM-HF 1 2

PAD

TPS61045

APN 353S1401

APN 152S0504

U5805 CRITICAL

9

L5801 CRITICAL

2

QFN

VIN

1UF 603 X5R 16V 10%

7

2

4

8

4

10UH - 0.58A - 0.35OHM

DFN VIN

THRML PAD

7 1 2

MIN_LINE_WIDTH = 0.50MM

SWITCH_NODE = TRUE

MIN_NECK_WIDTH = 0.20MM

BOOST_FB

R5811 100K MF-LF 402 1/16W 1% 1%

R5812, R5813, C5818 MODIFIED

R5813 71.5K 1M 402 MF-LF 1/16W 1% 1%

R5812

KBDLED_ANODE

C5819 1UF 603-1 X5R 25V 10%

CRITICAL

J5815 F-RT-SM

APN 518S0691

KBD BACKLIGHT CONNECTOR

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WELLSPRING 2

PAGE TITLE

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BRANCH

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Analog SMS

R5921 pulls up SMS_PWRDN to turn off SMS when pin is not being driven by SMC.

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation.

Sudden Motion Sensor (SMS)
NOTE: If HOLD* is asserted, the ROM will ignore SPI cycles.
Input impedance of ~40K meets sparkitecture requirements.

Divider sets ACIN threshold at 13.55V.

Reverse-Current Protection

Max Current = 15A (L7030/L7031 limit) f = 400 kHz

Inrush Limiter

Min. Current = 175mA

NO STUFF

Min. Neck Width = 0.2 mm

Min. Line Width = 0.3 mm

Min. Neck Width = 0.4 mm

Min. Line Width = 0.6 mm
1.8V S0 Regulator

Vout = 0.8V * (1 + Ra / Rb)

1.5V S0 Regulator

Vout = 0.8V * (1 + Ra / Rb)

1.2V ENET Regulator

Vout = 0.8V * (1 + Ra / Rb)

1.05V to 1.0V FW Drop

Vout = 0.8V * (1 + Ra / Rb)

FW 10V Boost Regulator

Vout = 1.794V

1.05V S5 LDO

Vout = 1.05V

Misc Power Supplies

Vout = 0.8V * (1 + Ra / Rb)

OUT

IN
LVDS Transmitter Termination

All emulated LVDS outputs require this termination.

PLACE_NEAR=U9600.C10:7mm
PLACE_NEAR=U9600.A9:7mm
PLACE_NEAR=U9600.A10:7mm
PLACE_NEAR=U9600.B9:7mm
PLACE_NEAR=U9600.A7:7mm

DisplayPort Mux

LVDS DDC MUX
17 Inch Panel (14 LEDs per string)

Target: ISET = 25mA, OVP = 50V
Actual: ISET = 24.7mA, OVP = 49.5V

0V = Vop + (1 + Ra/Rb) * VUV
VUV = 4.9V +/- 0.3V

Kv: C9716 AND C9719 FOR 17” PANEL

PLACEMENT_NOTE: PLACE R9700 FAR FROM THE NOISE PINS 3 AND 4

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## CPU Signal Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEG_D2R</td>
<td>12</td>
<td>17</td>
<td>25</td>
<td>20</td>
<td>18</td>
<td>CPU_BOX_R2M</td>
</tr>
<tr>
<td>GFX_VSENSE</td>
<td>13</td>
<td>70</td>
<td>13</td>
<td>70</td>
<td>13</td>
<td>CPU_BOX_R2M</td>
</tr>
<tr>
<td>GFX_VR_EN</td>
<td>10</td>
<td>47</td>
<td>10</td>
<td>69</td>
<td>10</td>
<td>CPU_BOX_R2M</td>
</tr>
<tr>
<td>PM_EXT_TS_L&lt;0&gt;</td>
<td>10</td>
<td>71</td>
<td>10</td>
<td>71</td>
<td>10</td>
<td>CPU_BOX_R2M</td>
</tr>
</tbody>
</table>

NOTE: All gaps are in the solution part, which must be equal to 1 mil opening without specifying a target impedance.

### PCI-Express

<table>
<thead>
<tr>
<th>Name</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Distance (mil)</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>PEG_R2D</td>
<td>8</td>
<td>7</td>
<td>5</td>
<td>4</td>
<td>2</td>
<td>CPU_BOX_R2M</td>
</tr>
<tr>
<td>PEG_R2D</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>CPU_BOX_R2M</td>
</tr>
<tr>
<td>PEG_R2D</td>
<td>2</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>CPU_BOX_R2M</td>
</tr>
</tbody>
</table>

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SYNC_DATE=06/09/2009

SHEET D
**Memory Bus Constraints**

**Memory Net Properties**

---

**Table:**

<table>
<thead>
<tr>
<th>Net Spacing Type 1</th>
<th>Net Spacing Type 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_DATA to MEM</td>
<td>MEM_DQS to MEM</td>
</tr>
<tr>
<td>MEM_CMD to MEM</td>
<td>MEM_CLK to MEM</td>
</tr>
<tr>
<td>MEM_CTRL to MEM</td>
<td>MEM_DQS to MEM</td>
</tr>
<tr>
<td>MEM_CLK to MEM</td>
<td>MEM_DQS to MEM</td>
</tr>
</tbody>
</table>

---

**Legend:**

- **Layer:**
  - LAYER 1: 1.5:1 SPACING
  - LAYER 2: 2.5:1 SPACING
  - LAYER 3: 3:1 SPACING

---

**Notes:**

- Maximum length of any signal from die pad to SODIMM pad is 139.7mm, from processor ball to SODIMM pad is 114.3mm.
- **SOURCE:** Calpella SFF Platform DG, Rev 1.5 (#407364), Section 2.2
### SMBus Interface Constraints

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### HD Audio Interface Constraints

<table>
<thead>
<tr>
<th>Source</th>
<th>Connecting board</th>
<th>Layer</th>
<th>Min. Line Width</th>
<th>Min. Neck Width</th>
<th>Max. Neck Length</th>
<th>Diffpair Primary Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SIO Signal Constraints

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### SPI Interface Constraints

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**PCH Net Properties**

```
<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Type</th>
<th>neighbouring Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
Ethernet Net Properties

<table>
<thead>
<tr>
<th>ELECTRIC_CONSTRAINT_SET</th>
<th>PHYSICAL_CONSTRAINT</th>
<th>PROPERTIES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ethernet Net Properties</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CAESAR II (Ethernet) Constraints

<table>
<thead>
<tr>
<th>SOURCE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CAESAR II (Ethernet PHY) Constraints

<table>
<thead>
<tr>
<th>SOURCE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Ethernet Constraints

<table>
<thead>
<tr>
<th>SOURCE</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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Apple Inc.

SYNC_DATE=06/09/2009
SYNC_MASTER=K17_WFERRY
### FireWire Interface Constraints

<table>
<thead>
<tr>
<th>Port</th>
<th>TLB</th>
<th>SLL</th>
<th>SRL</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### FireWire Net Properties

#### Electrical Constraints

- **Port 2 Not Used**
- **Sync Master:** K17_WFerry
- **Sync Date:** 06/09/2009

#### FireWire Net Properties

- **FW_TP:** 110_OHM_DIFF
- **FW_110D:** 110_OHM_DIFF
- **FW_PORT1_TPA_P:** Port 1 TP A
- **FW_PORT1_TPA_N:** Port 1 TP N
- **FW_PORT1_TPB_P:** Port 1 TP B
- **FW_PORT1_TPB_N:** Port 1 TP B
- **FW_P0_TPA:** Port 0 TP A
- **FW_P0_TPB:** Port 0 TP B
- **NC_FW0_TPBP:** New Class for TP B
- **NC_FW0_TPBN:** New Class for TP N

---

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<table>
<thead>
<tr>
<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**SMC SMBus Net Properties**

<table>
<thead>
<tr>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>PHYSICAL_CONSTRAINT_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>TABLE_PHYSICAL_RULE_HEAD</th>
<th>TABLE_PHYSICAL_RULE_ITEM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SMBus Charger Net Properties**

<table>
<thead>
<tr>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>PHYSICAL_CONSTRAINT_SET</th>
<th>PHYSICAL_RULE_SET</th>
<th>TABLE_PHYSICAL_RULE_HEAD</th>
<th>TABLE_PHYSICAL_RULE_ITEM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**SMC Constraints**

Apple Inc.
### Memory Constraint Relaxations

Allow 0.127 mm space for 30.127 mm lines for 80% fault.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width</td>
<td>0.127</td>
</tr>
<tr>
<td>Space</td>
<td>30.127</td>
</tr>
</tbody>
</table>

### Graphics, SATA Constraint Relaxations

Alternate diffpair width/gap through MTA fanout areas (50-70m diff)

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Width</td>
<td>50-70m</td>
</tr>
<tr>
<td>Gap</td>
<td>50-70m</td>
</tr>
</tbody>
</table>

---

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<table>
<thead>
<tr>
<th>BOARD LAYERS</th>
<th>ALLOW ROUTE</th>
<th>ON LAYER?</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP, BOTTOM</td>
<td>Y</td>
<td>Y</td>
</tr>
<tr>
<td>ISL2, ISL11</td>
<td>Y</td>
<td>Y</td>
</tr>
</tbody>
</table>

**Minimum Line Width**

- Standard: 0.075 mm
- 2x Dielectric: 0.089 mm

**Minimum Neck Width**

- Standard: 0.115 mm
- Diffpair Neck Gap: 0.110 mm

**Maximum Neck Length**

- Standard: 0.220 mm
- Diffpair Neck Gap: 0.180 mm

**Diffpair Primary Gap**

- Standard: 0.200 mm
- Diffpair Neck Gap: 0.190 mm

**Spacing Rule Set**

- 2.5:1 Spacing
- 1.5:1 Spacing

**Net Spacing Type**

- Type 1
- Type 2

**BGA P2MM**

- Standard

**BGA P1MM**

- Weight

NOTE: From T18 MLB, changed to reflect K17 mlb stackup.

NOTE: ISL2, ISL11 PWR, GND, GND is differential impedance on outer layers and 100 ohms on inner layers.

MEM_CLK = DEFAULT

REFERENCES

- Table Physical Rule Item
- Table Spacing Rule Item
- Table Spacing Assignment Item
- Table Physical Rule Head
- Table Spacing Rule Head
- Table Board Info
Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

- **PCH "S0" Rails**
- **PCH "S5" Rail**

- **Current Numbers**
  - XMC100
  - XMC110
  - XMC120
  - XMC130
  - XMC135
  - XMC140

- **Power Aliases**
  - PP3V3_S0
  - PP3V3_S0M_PCH
  - PP3V3R1V5_S0_PCH
  - PP3V3R1V8_S0_PCH
  - PP3V3_S0_PCH
  - PP3V3_S0_PCH_VCCALVDS
  - PP1V8_S0_PCH
  - PP1V05_S0_PCH
  - PPVTT_S0_PCH

- **Current Values**
  - 6 mA (3.3V)
  - 156 mA (1.8V)
  - 777 mA (1.05V)
  - 357 mA
  - 165 mA
  - 345678

- **NOTES**
  -WF: Estimate 300 mA for budget purposes
  - MAKE_BASE=TRUE
  - MIN_LINE_WIDTH=0.2 mm
  - MIN_NECK_WIDTH=0.2 mm
  - MIN_LINE_WIDTH=0.6 mm
  - MIN_NECK_WIDTH=0.25 mm
  - VOLTAGE=1.05V
  - VOLTAGE=3.3V
  - VOLTAGE=1.5V
  - VOLTAGE=3.3V
  - VOLTAGE=3.3V

- **Other Details**
  - Sync Master=K17_REF
  - Sync Date=06/17/2009
  - Drawing Number
  - Sheet 101 of 103
  - Size D