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**Revision History**

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<tr>
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<th>Page</th>
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<td>1</td>
<td>Update to reflect changes in the design.</td>
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<tr>
<td>02/16/2010</td>
<td>10</td>
<td>Add new section on CPU Power &amp; Ground.</td>
</tr>
<tr>
<td>02/16/2010</td>
<td>27</td>
<td>Update to reflect changes in the power supply section.</td>
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## Development BOM

### Module Parts

<table>
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<th>PART NUMBER</th>
<th>DESCRIPTION</th>
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<tr>
<td>353S2988</td>
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<td>353S2987</td>
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<td>353S2811</td>
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<tr>
<td>152S0874</td>
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<tr>
<td>152S0693</td>
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### BOM Options

#### K86_K87_DEBUG:PROD

<table>
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<td>337S3797</td>
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### BOM Groups (always-present)

#### All

<table>
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<tbody>
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### BOM Groups (project phase-dependent)

#### All

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### BOM Variance

#### Module Parts

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### BOM Configuration

<table>
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<td>1</td>
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<td>D</td>
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### Bar Code Labels / EEE #'s

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<th>REFERENCE DES</th>
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<td>LBL,P/N LABEL,PCB,28MM X 6 MM</td>
<td></td>
</tr>
</tbody>
</table>

### Board Stack-Up

#### Top

1. **SIGNAL**
2. **GROUND**
3. **SIGNAL (High Speed)**
4. **SIGNAL (High Speed)**
5. **GROUND**
6. **POWER**
7. **POWER**
8. **GROUND**
9. **SIGNAL (High Speed)**
10. **SIGNAL (High Speed)**
11. **GROUND**

#### Bottom

12. **SIGNAL**

### Part Substitutions (Differences with K6/K69)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
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<tbody>
<tr>
<td>ALL</td>
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</tr>
</tbody>
</table>

### Schematic / PCB #'s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
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<tbody>
<tr>
<td>ALL</td>
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</tr>
</tbody>
</table>
### Revision History

#### 2010-01-22: 2.6.0
- csa 2: Updated CPU block text to include CPU description for both K86 and K87
- csa 8: Deleted net properties for the following nets: 
  - Added R4585, R4586 (51.1 ohm, 1%, 114S0093) and OMITted
- Changed BOM group structure to match that in the radar (see PDF attached to radar)
- Reverted back to ENG BOM, no longer PROD BOM (i.e. reverted much of 2.2.0 changes)
- Changed C4585, C4586 to 131S4713 (47pF, 5%)
- Added BOM table entry for MCP83M (337S3876)
- Per <rdar://problem/7544629> K86/K87: Update MCP83 description on csa 4
- Changed 085-1093 to call out K87_DEVEL_PVT instead of K87_DEVEL_ENG
- Changed R3440 color to green, deleted WF text note about needing PU
- LPC_SERIRQ
  - This is for K86 ONLY. Adding entry to minimize delta on csa 4 between K87 and K86
- Keeping K86 and K87 pgs identical for CSA 74, modifying BOM table for IMVP 1 phase on K87's schematic to reflect changes for K86.
- Deleted BOM table for Hall effect assembly
- csa 69: Per <rdar://problem/7494087> K87: remove OMIT from J6955 and delete BOM table
- Updated table to add new values for 1phase (PWM freq., Max current, Load line)
- Added IMVP6:2PHASE to the following components:
  - Changed BOOTROM:PROG to call out 341T0251 (SUBASSY, IC, BOOT ROM, K86/K87)
- csa 34: Changed U3440 from AP002 part to AP016 (343S0511) per <radar:7459498> BOM: APN updates for FPF1009 and SAK parts
- csa 54: Began syncing from T27 per <radar:7432091 > BATT_ISENSE filter change to address lower max sink current on ISL6259 BMON pin (K17 auto-shutdown issue)
- csa 57: Began syncing from T27 per <radar:7304029 > T27 schematic bom option for R5714 & R5030 to keep K87 in sync
- Per <rdar://problem/7495116> K87: remove ON Semi alternate for Q2300 (376S0624)
- csa 4: Per <rdar://problem/7571786> K86/K87: Add E3T EEE code for K86 to schematic
- csa 97: Per <rdar://problem/7589365> K86/k87: Compensation settings change to provide more phase margin, reduce ripple
- Added L4530, L4531 (APN 155S0137) to SIL connector pins
- CSA 25: Changed R2600 refdes to R2550 to match with page#.
- Per <rdar://7685202> K86/K87 schematic: change U9700 to 353S2965 for Freescale backlight issue
- Per <rdar://7644836> K87 power component update
- Per <rdar://7488543> K86/K86 Task: Measure each Power supply in MLB
- Per <rdar://7683852> K87 Proto1: 5 of 6 systems failing graphics noise (Underwater) acoustic spec by up to 3.1dB
- CSA 25,49,50: Changed Q2592 gate control pin to SMC_P24 from SMC_P10.
- Nets MCP_PLL_LDO_EN and PP3V3_S0_LDO_R added.
- Summary of changes for MLB_LDO:
- CSA 97: R9725 changed to 200ohm, C9799 of 47pF added.  R9726.1 connection moved to LVDS_IG_BKLPWM
- CSA 69: C6970, C6971, C6972 of 1000pF (APN 131S0222) added
- CSA 74: R7417 changed to 5.90K, C7428 changed to 0.47uF, C7434 changed to 0.033uF
- CSA 8: 5.1.1
- CSA 90: Deleted net properties for =PP5V_S3_CAMERA
- Added IMVP6:2PHASE to the following components:
  - Changed BOOTROM:PROG to call out 341T0251 (SUBASSY, IC, BOOT ROM, K86/K87)
- csa 34: Changed U3440 from AP002 part to AP016 (343S0511) per <radar:7459498> BOM: APN updates for FPF1009 and SAK parts
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- CSA 25,49,50: Changed Q2592 gate control pin to SMC_P24 from SMC_P10.
- Nets MCP_PLL_LDO_EN and PP3V3_S0_LDO_R added.
- Summary of changes for MLB_LDO:
<table>
<thead>
<tr>
<th>Voltage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.75V</td>
<td>LVDDR VRef/VTT (0.75V/0.675V) Rails</td>
</tr>
<tr>
<td>1.05V</td>
<td>MAKE_BASE=TRUE</td>
</tr>
<tr>
<td>1.25V</td>
<td>MIN_NECK_WIDTH=0.2 mm</td>
</tr>
<tr>
<td>3.3V</td>
<td>MIN_LINE_WIDTH=0.6 mm</td>
</tr>
</tbody>
</table>

**Power Aliases**

Apple Inc. 001-03611

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Current numbers from Merom for Santa Rosa EMTS, doc #20905.

44 A (5V Design Target)
31 A (5V PPM)
30.4 A (5V LPP)
22 A (5V Design Target)

2500 mA (after VCC stable)
4500 mA (before VCC stable)

CPU Power & Ground

Apple Inc.

SYNC_DATE=02/16/2010

PAGE 11 OF 109
CPU VCore HF and Bulk Decoupling

4x 330μF, 30x 22μF 0402

Placement Note (C1230-C1239):

- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.
- Place inside socket cavity on secondary side.

VCC (CPU AVdd) Decoupling

1x 10μF, 1x 0.01μF

VCCP (CPU I/O) Decoupling

1x 330μF, 6x 0.1μF 0402
Mini-XDP Connector

NOTE: This is not the standard XDP pinout. Use with 920-0782 adapter flex to support CPU, MCP debugging.

Please avoid any obstructions on the odd-numbered side of J1300.

SYNC_MASTER=(K84_MLB)
SYNC_DATE=(02/25/2009)

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The extended debug port (MiniXDP)

100K pull-downs required if MIKEY_MIC_LOAD_DET or FLAT PANEL.

NOTE: +3.3V_RGBDAC pin to GND.

DDC Mode Pull-downs

NOTE: If DDC is not required pull-downs if used for dual-mode DisplayPort (DP+). If unused no pull-downs are necessary. If used for TMDS/HMI only then only pull-downs are necessary.

GPIO Pull-Ups

The 100K pull-up resistors for GPIO_39 and GPIO_42 are 1/16W.

NOTE: DDC_CLK3/DP_AUX_CH1_P is 1/16W.

NOTE: 100K pull-downs required if MIKEY_MIC_LOAD_DET or FLAT PANEL.

NOTE: +3.3V_RGBDAC pin to GND.

USB DAC disabled.

Only to float all USB DAC signals.

DDC/Composite/Component Video support on MCP99.

Interface Mode

MCP Signal

TMDS/HMI

+VDD_IFPB

+VIO_DP0_3

+VIO_PLL_NV_1

+VIO_PLL_SPPLL0_2

+VIO_PLL_V

+3.3V_PLL_USB_1

DDC_CLK3/DP_AUX_CH1_P

DDC_CLK2/DP_AUX_CH0_P

DDC_DATA2/DP_AUX_CH0_N

DP0_3_P/TMDS0_TXC_P

DP1_1_P/TMDS0_TX4_P

DP_IG_ML0_P<3>

DP_IG_ML0_N<3>

DP_IG_ML0_P<2>

DP_IG_ML0_N<2>

LCDC_CLK0/DDC_DATA0 pull-ups still required (or use as GPIOs).

Connect +3.3V_RGBDAC pin to GND.

NOTE: TMDS/HMI not supported on IFPA/B for MCP99 A01.

Connect RGMII_RXCLK to 10K pull-down.

Connect RGMII_RXD<0:3> together to 10K pull-down.

All other pins can be left TP or NC.

+3.3V_PLL_MAC_DUAL must remain connected to 3.3V RMGT rail.
NOTE: "SM" rails are dynamically switched in the SO state as needed, controlled by MCP89 GPIOs.
Approx. Ramp Time (EN to 1.35V, μS): 7.91 + 0.0678 * R1(Kohms)

Clamps enable before MCP89 MEMVDD rail switched off. Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89. Q2355/Q2356 chosen for low output capacitance.

NO STUBS on CKE signals!
Approx. Ramp Time (EN to 1V, uS): 43.9 + 0.6943 * C1(pF)

Max Ramp-Up Time: 1500 uS (ENABLE to 90%)

Min Ramp-Up Time: 100 uS (10% to 90%)

FET Ron <= 2.5 mOhms

Gated Rail Savings: 860mW

C2400 helps reduce input rail droop during Q2400 turn-on.

C2405 helps reduce input rail droop during Q2400 turn-on.

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

LOADING

C19...8

C20...7

C21...6

C22...5

C23...4

C24...3

C25...2

C26...1

C27...0

C28...9

C29...8

C30...7

C31...6

C32...5

C33...4

C34...3

C35...2

C36...1

C37...0

C38...9

C39...8

C40...7

C41...6

C42...5

C43...4

C44...3

C45...2

C46...1

C47...0

C48...9

C49...8

C50...7

C51...6

C52...5

C53...4

C54...3

C55...2

C56...1

C57...0

C58...9

C59...8

C60...7

C61...6

C62...5

C63...4

C64...3

C65...2

C66...1

C67...0

C68...9

C69...8

C70...7

C71...6

C72...5

C73...4

C74...3

C75...2

C76...1

C77...0

C78...9

C79...8

C80...7

C81...6

C82...5

C83...4

C84...3

C85...2

C86...1

C87...0

C88...9

C89...8

C90...7

C91...6

C92...5

C93...4

C94...3

C95...2

C96...1

C97...0

C98...9

C99...8

C100...7

C101...6

C102...5

C103...4

C104...3

C105...2

C106...1

C107...0

C108...9

C109...8

C110...7

C111...6

C112...5

C113...4

C114...3

C115...2

C116...1

C117...0

C118...9

C119...8

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C167...0

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C184...3

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C186...1

C187...0

C188...9

C189...8

C190...7

C191...6

C192...5

C193...4

C194...3

C195...2

C196...1

C197...0

C198...9

C199...8

C200...7

C201...6

C202...5

C203...4

C204...3

C205...2

C206...1

C207...0

C208...9

C209...8

C210...7

MCP 3.3V/1.8V IFP Interface Power
- 160 mA
- 180 mA (1.8V LVDS)

MCP GFX Core Power
- 15350 mA (0.85V)

MCP 1.05V DisplayPort Power
- PP1V05_S0_MCP_DP0_VDD
- PP3V3R1V8_S0_MCP_IFP_VDD
- PPVCORE_SW_MCP_GFX

MCP TMDS0_RSET
MCP TMDS0_VPROBE

NO STUFF
- 0.1UF
- 4.7UF
- 10UF

CERM
- 402
- 20%
- 603-1

4.7UF
- X5R
- 20%

1UF
- X5R
- 10V
- 10%

PP3V3_S0_MCP_DAC

If RGBDAC is used, requires ferrite (1550382)
Plus 1x 4.7uF 0603 & 1x 0.1uF 0402 cap.

If RGBDAC is not used, tie to GND.

SYNC_MASTER=T27_MLB
SYNC_DATE=02/16/2010
Page 5

- Proper APN(s) required elsewhere.
- Signal aliases required by this page:
  - PPDDRVTT_S0_MEM_A
  - I2C_SODIMMA_SDA
  - I2C_SODIMMA_SCL

NOTE: J3100 is OMITted on this page.

**DDR3 Plane Stitching Caps (Space evenly across plane split)**

**"Factory" (top) slot**

- SPD Addr: 0xA0(Wr)/0xA1(Rd)
- SPD Addr: 0xA1(Wr)/0xA0(Rd)
- SPD Addr: 0xA2(Wr)/0xA3(Rd)
- SPD Addr: 0xA3(Wr)/0xA2(Rd)
- SPD Addr: 0xA4(Wr)/0xA5(Rd)
- SPD Addr: 0xA5(Wr)/0xA4(Rd)

- **MEM_A_CKE<0>** = **MEM_A_DQ<57>**
- **MEM_A_DQ<56>**
- **MEM_A_DQ<49>**
- **MEM_A_DQ<43>**
- **MEM_A_DQ<41>**
- **MEM_A_CLK_P<0>**
- **MEM_A_SA<0>**
- **MEM_A_A<1>**
- **MEM_A_A<3>**
- **MEM_A_RAS_L**
- **MEM_A_ODT<1>**
- **MEM_A_BA<1>**
- **MEM_A_CLK_N<1>**
- **MEM_A_CS_L<0>**
- **MEM_A_CLK_P<1>**

- **CERM** 20%10V
- **0.1UF**
- **402**

- **PPVREF_S3_MEM_VREFDQ_A**
  - 6.3V
  - 0.1UF
  - **CERM**

- **DDR3 Plane Stitching Caps (Space evenly across plane split)**
  - 20%
  - 10V
DDR3 Plane Stitching Caps (Space evenly across plane split)

"Expansion" (bottom) slot

Molex: 516s0790

Apple Inc.

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BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROP LINE REGULATION
- RIPPLE TO WENT ABS
- START TIME LESS THAN 15MS
- 80002-8417, TC4418 MODIFIED

BOOSTER +18.5VDC FOR SENSORS

IPD Flex Connector

DO NOT SYNC FROM T27. REMOVED KEYBOARD BACKLIGHT CIRCUIT

MIN LINE WIDTH=0.50MM
MIN NECK WIDTH=0.20MM
VOLTAGE=5V
VOLTAGE=5V
MIN NECK WIDTH=0.20MM
MIN LINE WIDTH=0.50MM
VOLTAGE=18.5V
MIN NECK WIDTH=0.20MM
MIN LINE WIDTH=0.50MM

RIPPLE TO MEET ERS
DO NOT SYNC WITH K84. REMOVED NO STUFF ON C5923, C5924, C5925. ADDED PLACE NEARS.
NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
DAC1 FSOUTPUT= 1.34VRMS
SATELLITE  796Hz < HPF FC < 936Hz
SUB  80 Hz < HPF FC < 94 Hz
GAIN  6DB (2V/V)

SPRK AMP. INPUT REFERRED CLIP POINT = ~-6dBFS

APN:353S2621

SPKRAMP_SHDN

ALIAS OF PPSV_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

AUD_LO2_R_N

SPKRAMP_INR_N

FERR-1000-OHM

L6610

SPKRAMP_INSUB_P

C6607

APN:353S2621

ALIAS OF PPSV_S3_REG, MIN_LINE_WIDTH=0.60MM, MIN_NECK_WIDTH=0.20MM

AUD_LO2_R_P

L6610

FERR-1000-OHM

SPKRAMP_INR_P

C6607

CRITICAL

1 2

MIN_LINE_WIDTH=0.30 mm

MIN_NECK_WIDTH=0.20 mm

SPKRAMP_SUB_P_OUT

SPKRAMP_SUB_N_OUT

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APPLE INC.
5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2
VOUT = (2 * RC / RD) + 2

NOTE: DONT SYNC THIS PAGE FROM T27

Place XW7203 by Pin1 OF L7260.

ROUTING NOTE:

Place XW7202 by C7292.

ELEC 6.3V D1A-SM 20%

C7280 39UF-0.027OHM CRITICAL

16V 20%
B1A-SM POLY

4.7UH-13A-15MOHM PWRPK-1212-8-SM

L7260 SIS424DN CRITICAL

Q7260 Q7261 CRITICAL

1UF 603-1 25V 10%

IN =P3V3S5_EN_L

MAX CURRENT = 13.3A
PWM FREQ. = 300 KHZ

=PP3V3_S5_REG

MAX CURRENT = 9.1A
PWM FREQ. = 375 KHZ

5V3V3_REG_EN

3V3S5_VFB

VFB1

DRVL1

DRVH1

VBST1

ENTRIP1

<RB>

<RD>

IN

DIDT=TRUE

MIN_NECK_WIDTH=0.2 MM

MIN_LINE_WIDTH=0.6 MM

PLACE_NEAR=U7200.6:1 MM

PLACE_NEAR=U7200.25:1 MM

4.7UH-10A

RJK0384DPA

Q7220 WPAK

C7241 7UF X5R 25V 10%

CRITICAL

Place XW7205 by C7252.

ROUTING NOTE:

Place XW7201 between Pin 15 and Pin 25 of U7200.

MAX CURRENT = 9.1A
PWM FREQ. = 375 KHZ

=PP5V_S5_LDO

3V3S5_VO2

3V3S5_LL

3V3S5_DRVH

MIN_LINE_WIDTH=0.5 MM
VOLTAGE=5V
MIN_NECK_WIDTH=0.25 MM
MIN_LINE_WIDTH=0.6 MM

RJK0384DPA

Q7220 WPAK

C7241 7UF X5R 25V 10%

CRITICAL

Place XW7205 by C7252.

ROUTING NOTE:

Place XW7201 between Pin 15 and Pin 25 of U7200.
1.05V ENET Switcher

\[ \text{VOUT} = 0.6V \times (1 + \frac{R_A}{R_B}) \]

1.8V S0 Switcher

\[ \text{VOUT} = 1.8V \]
\[ \text{Max Current} = 0.3A \]
\[ f = 1MHz \]

1.05V S0 MCP PLL LDO

\[ \text{VOUT} = 1.05V \]
\[ \text{Max Current} = 0.5A \]
\[ f = 1.6MHz \]

MCP 0.9V S5 (AUXC) Switcher

\[ \text{VOUT} = 0.902V \]
\[ \text{Max Current} = 1.5A \]
\[ f = 1.6MHz \]

Misc Power Supplies

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- NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
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DO NOT SYNC FROM K84. ADDED ENET CIRCUITS, REMOVED 1V05 ENET CIRCUIT
**FSB (Front-Side Bus) Constraints**

- Intel Design Guide recommends FSB signals be routed only on internal layers.
- FSB signals / groups shown in signal table on right.
- Signals within each 4x group should be matched within 5 ps of strobe.
- Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.
- All DSSTB#s matched to +/- 135 ps.
- DSTB# complementary pairs should be matched within 1 ps of each other.

**CPU Signal Constraints**

- Blocking 2x dielectric spacing to the DSTB#s.

**SPACING_RULE_SET**

- **CLK_FSB_100D**
- **CPU_27P4S**
- **CPU_AGTL**
- **MCP_FSB_COMP**
- **CPU_DPRSTP_L**
- **CPU_PWRGD**
- **CPU_ASYNC**
- **CPU_VCCSENSE**
- **XDP_TDO**
- **CPU_BSEL<2..0>**
- **CPU_INTR**
- **PM_DPRSLPVR**
- **CPU_COMP<1>**
- **CPU_COMP<3>**
- **CPU_DPSLP_L**
- **CPU_IGNNE_L**
- **IMVP6_VSEN_P**
- **XDP_BPM_L<5>**
- **FSB_ADSTB_L<1>**
- **FSB_ADSTB_L<0>**
- **FSB_CPURST_L**
- **FSB_TRDY_L**
- **FSB_LOCK_L**
- **FSB_DRDY_L**
- **FSB_BPRI_L**
- **FSB_HIT_L**
- **FSB_BNR_L**
- **FSB_DINV_L<2>**
- **PM_THRMTRIP_L**
- **FSB_D_L<47..32>**
- **FSB_DSTB_50S**
- **FSB_DSTB_L_N<2>**

**NET_TYPE**

- **FSB_1X**
- **CPU_GTLREF**
- **CPU_IERR_L**
- **CPU_FERR_L**
- **CPU_DPRSTP_L**
- **CPU_PWRGD**
- **CPU_ASYNC**
- **CPU_VCCSENSE**
- **XDP_TDO**
- **CPU_BSEL<2..0>**
- **CPU_INTR**
- **PM_DPRSLPVR**
- **CPU_COMP<1>**
- **CPU_COMP<3>**
- **CPU_DPSLP_L**
- **CPU_IGNNE_L**
- **IMVP6_VSEN_P**
- **XDP_BPM_L<5>**
- **FSB_ADSTB_L<1>**
- **FSB_ADSTB_L<0>**
- **FSB_CPURST_L**
- **FSB_TRDY_L**
- **FSB_LOCK_L**
- **FSB_DRDY_L**
- **FSB_BPRI_L**
- **FSB_HIT_L**
- **FSB_BNR_L**
- **FSB_DINV_L<2>**
- **PM_THRMTRIP_L**
- **FSB_D_L<47..32>**
- **FSB_DSTB_50S**
- **FSB_DSTB_L_N<2>**

**SOURCE:**

- **MCP99 Interface DS ID=006425-001_v1.9**, Section 2.1
- **Intel Design Guide**

**NOTE:**

- Intel Design Guide only recommends routing if signal lengths can be shortened.
- CPU signals should be routed only on internal layers.
- Blocking 2x dielectric spacing to the DSTB#s.

**CPU / FSB Net Properties**

- **Spacing**
- **Line-to-Line Spacing**
- **Minimum Line Width**
- **Weight**
- **Allow Route**
- **On Layer?**
- **TABLE_SPACING_RULE_ITEM**
- **TABLE_SPACING_RULE_HEAD**
- **TABLE_SPACING_RULE_SET**
- **TABLE_PHYSICAL_RULE_ITEM**
- **TABLE_PHYSICAL_RULE_SET**

**FSB Clock Constraints**

- FSB signals with impedance requirements are 35-Ohm single-ended.
- FSB signals require 27-4-ohm single-ended impedance.

**MCP FSB COMP Signal Constraints**

- Source: **MCP99 Interface DS ID=006425-001_v1.9**, Section 2.1

**SYNC_DATE=02/16/2010**

**REVISION**

**C.0.0**

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**APPLE INC.**

- **051-8561**
- **C.0.0**
**Memory Bus Constraints**

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<tr>
<th>SPACING_RULE_SET</th>
<th>NET_SPACING_TYPE1</th>
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<td><strong>MEM_CLK2MEM</strong></td>
<td><strong>MEM_2OTHER</strong></td>
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<td><strong>MEM_40S</strong></td>
<td><strong>MEM_CTRL</strong></td>
<td><strong>MEM_DQS</strong></td>
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<td><strong>MEM_CLK</strong></td>
<td><strong>MEM_DQS</strong></td>
<td><strong>MEM_CMD</strong></td>
</tr>
</tbody>
</table>

**MINIMUM NECK WIDTH**

- NV DG says 2x inner, 4x outer

**DIFFPAIR PRIMARY GAP**

- MINIMUM NECK WIDTH
- DIFFPAIR PRIMARY GAP

**Memory Net Properties**

<table>
<thead>
<tr>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>MEM_B_DQS7</th>
<th>MEM_B_DQS6</th>
<th>MEM_B_DQS5</th>
<th>MEM_B_DQS4</th>
<th>MEM_B_DQS3</th>
<th>MEM_B_DQS2</th>
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<td>MEM_B_CMD</td>
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<table>
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<tr>
<th>AREA_TYPE</th>
<th>NV DG says 2x inner, 4x outer</th>
<th>NV DG says 2x inner, 4x outer</th>
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<tr>
<td><strong>MEM_DATA</strong></td>
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<td><strong>MEM_DQS</strong></td>
<td><strong>MEM_CMD</strong></td>
<td><strong>MEM_DLL</strong></td>
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</tbody>
</table>

**Line-to-Line Spacing**

- 3:1_SPACING
- 2:1_SPACING

**Spacing Rule Item**

- TABLE_SPACING_RULE_ITEM
- TABLE_SPACING_ASSIGNMENT_ITEM

**Physical Rule Item**

- TABLE_PHYSICAL_RULE_ITEM
NEBD PCIe Gen1/Gen2 notes!

LVDS intra-pair matching should be 5 mils. Pairs should be matched within 100 mils.

CRT signal single-ended impedance varies by location:

Max trace length: LVDS 10 inches, DP 8.5 inches.
<table>
<thead>
<tr>
<th>Layer</th>
<th>Line-to-Line Spacing</th>
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<tbody>
<tr>
<td>L1</td>
<td>=2x_DIELECTRIC</td>
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<tr>
<td>L2</td>
<td>=55_OHM_SE</td>
</tr>
<tr>
<td>L3</td>
<td>=55_OHM_SE</td>
</tr>
<tr>
<td>L4</td>
<td>=55_OHM_SE</td>
</tr>
<tr>
<td>L5</td>
<td>=55_OHM_SE</td>
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<tr>
<td>L6</td>
<td>=55_OHM_SE</td>
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<tr>
<th>Minimum Neck Width</th>
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<td>=90_OHM_DIFF</td>
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<table>
<thead>
<tr>
<th>Maximum Neck Length</th>
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<td>=90_OHM_DIFF</td>
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<tr>
<th>Differential Pair Primary Gap</th>
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<tr>
<th>Physical Rule Set</th>
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### MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

**88E1116R (Ethernet PHY) Constraints**

<table>
<thead>
<tr>
<th>Parameter</th>
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<td>ENET_MDI_100D</td>
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<tr>
<td>MCP_BUF0_CLK</td>
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<td>MCP_MII_COMP</td>
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<td>ENET_TXD</td>
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<td>ENET_RXD&lt;0&gt;</td>
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**MCP RGMII (Ethernet) Constraints**

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**SPACING RULES**

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**Physical Rules**

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### SMC SMBus Net Properties

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### SMBus Charger Net Properties

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Apple Inc.

C.O.O.

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www.laptop-schematics.com
## MCP Fanout Constraint Relaxations

| Net | Net Type | SPACING_RULE_SET | NET_SPACING_TYPE1 | NET_SPACING_TYPE2 |Override |Override |Override |Override |Override |Override |Override |Override |Override |Override |Override |
|-----|----------|------------------|-------------------|-------------------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|
| SB_POWER | 500 MIL | STANDARD | STAND | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR |
| PCIE | 5.8 MM | AREA_TYPE | AREA | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR |
| USB | 7 8 5 4 2 1 | GND | DIFFPAIR PRIMARY GAP | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR |
| DP_90D | 30 | GND | DIFFPAIR PRIMARY GAP | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR |
| USB_90D | 30 | GND | DIFFPAIR PRIMARY GAP | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR |
| SATA_90D | 30 | GND | DIFFPAIR PRIMARY GAP | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR |

## Misc Net Properties

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## Power Net Properties

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## Misc Net Properties

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| THERM | THERM_1TO1_55S | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR | 1:1_DIFFPAIR |