1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K75F MLB_MEMSWAP

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0000892544	PRODUCTION RELEASED	2010-04-15

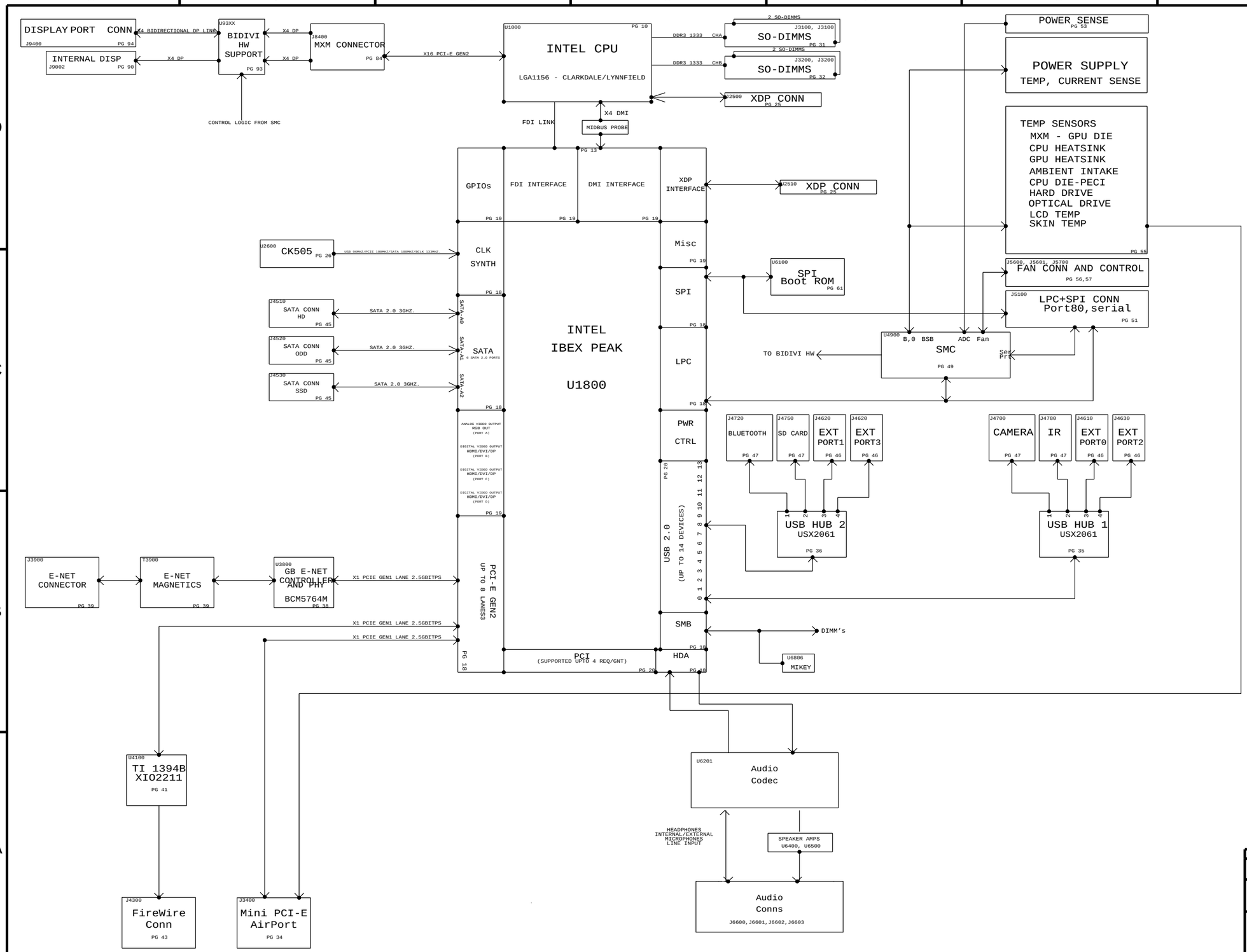
LAST_MODIFIED=Thu Apr 15 11:21:16 2010

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Thu Apr 15 11:21:16 2010

DRAWING TITLE
SCH,K75F,MLB_MEMSWAP

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D
REVISION A.0.0
BRANCH
PAGE 1 OF 110
SHEET 1 OF 92



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

System Block Diagram

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

BRANCH

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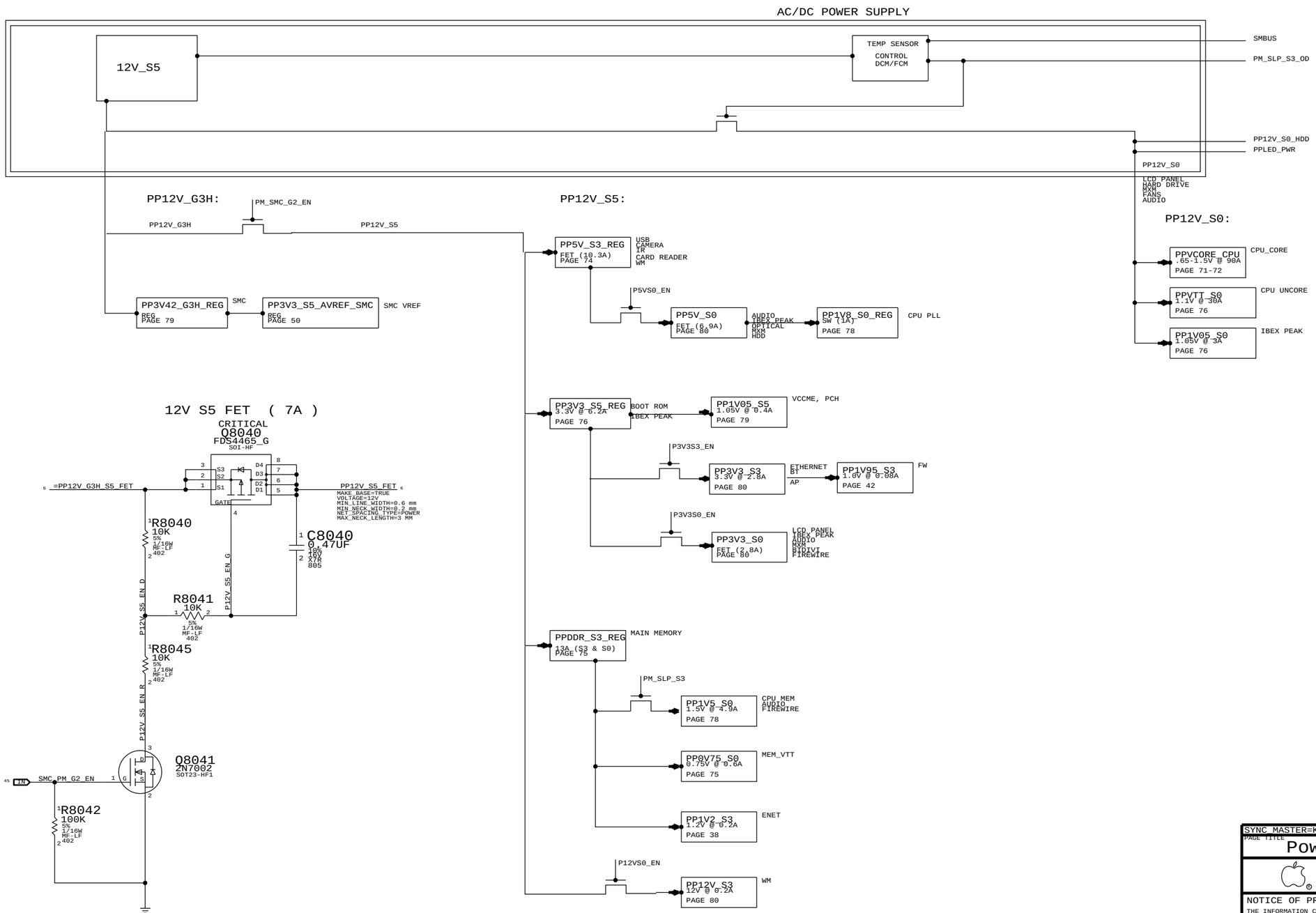

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Power Block Diagram

Apple Inc.

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
085-1609	PCBA,MLB,DEV,K75F	DEVELOPMENT,DEV_GROUP
639-1103	PCBA,MLB,K75F,3.20GHZ,CKD	K75F,3P20GHZ_CKD_CPU,BASIC,CPUPOC_IMAX_100_120
639-1105	PCBA,MLB,K75F,3.60GHZ,CKD	K75F,3P60GHZ_CKD_CPU,BASIC,CPUPOC_IMAX_100_120
639-1104	PCBA,MLB,K75F,2.66GHZ,LFD	K75F,2P66GHZ_LFD_CPU,BASIC,CPUPOC_IMAX_100_120
639-1106	PCBA,MLB,K75F,2.93GHZ,LFD	K75F,2P93GHZ_LFD_CPU,BASIC,CPUPOC_IMAX_100_120

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,XDP,BETTER,MXM,XDP_CPU_BPM,INT_VREF,PCH_VRM,BUF_CLK,PRODUCTION
DEV_GROUP	XDP_CONN,LPCPLUS,MOJOMUX,CPU_TDIODE

CPU SOCKET & ILM SUB-BOMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0063	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	MOLEX_SOCKET
604-0942	1	ASSY,PURCHASED,ILM,MOLEX,K75	ILM	CRITICAL	MOLEX_SOCKET
511S0069	1	SOCKET,LGA1156,CPU-LF	U1000	CRITICAL	FOXCONN_SOCKET
604-0988	1	ASSY,PURCHASED,ILM,FOXCONN,K75	ILM	CRITICAL	FOXCONN_SOCKET

ALTERNATE SOCKET VENDORS MUST USE MATCHING ILM

BOM NUMBER	BOM NAME	BOM OPTIONS
607-6876	SUB ASSY,CPU SOCKET,K75F,MOLEX	MOLEX_SOCKET
607-6877	SUB ASSY,CPU SOCKET,K75F,FOXCONN	FOXCONN_SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
607-6876	1	MOLEX CPU SOCKET AND ILM	SKT_ILM	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
607-6877	607-6876		SKT_ILM	FOXCONN ALTERNATIVE

BOARD STACK-UP

TOP	SIGNAL
2	GROUND
3	SIGNAL
4	POWER
5	POWER
6	SIGNAL
7	GROUND
BOTTOM	SIGNAL

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	337S3828	1	IC,IBEX PEAK B3 PRQ,DESKTOP,FCBGA,P425	U1800	CRITICAL	
	359S0157	1	IC,SLG2AP108,CLK GEN,CK505,QFN3	U2600	CRITICAL	BUF_CLK
	341T0230	1	IC,EFI BOOTROM,K74/K75	U6100	CRITICAL	
	338S0765	1	IC,XIO2211ZAY,1394B_PCIE,PHY/LINK	U4100	CRITICAL	
	343S0485	1	IC,BCM5764M,68PIN QFN	U3700	CRITICAL	
RAW: 335S0663	341T0269	1	ENET 1MBIT FLASH,CII,K74/K75F	U3701	CRITICAL	
	825-7122	1	MLB LABEL,48.0X4.8	X14	CRITICAL	

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3911	1	CKD,SLBUD,PRQ,3.20,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P20GHZ_CKD_CPU
337S3910	1	CKD,SLBTM,PRQ,3.60,73W,1333,K0,4M,LGA	CPU	CRITICAL	3P60GHZ_CKD_CPU
337S3810	1	LFD,SLBLC,PRQ,2.66,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P66GHZ_LFD_CPU
337S3861	1	LFD,SLBJG,PRQ,2.93,95W,1333,B1,8M,LGA	CPU	CRITICAL	2P93GHZ_LFD_CPU

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0298	128S0293		C7460,C7461,C7462,C7463	
518S0811	518S0685		J9002	

K75F PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-8600	1	SCH,K75F,MLB_MEMSWAP	SCH1		K75F
	820-2901	1	PCBF,K75F,MLB_MEMSWAP	MLB1		K75F
(338S0489 - BLNK)	341T0273	1	IC,SMC,K75F	U4900	CRITICAL	K75F

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
BOM Configuration

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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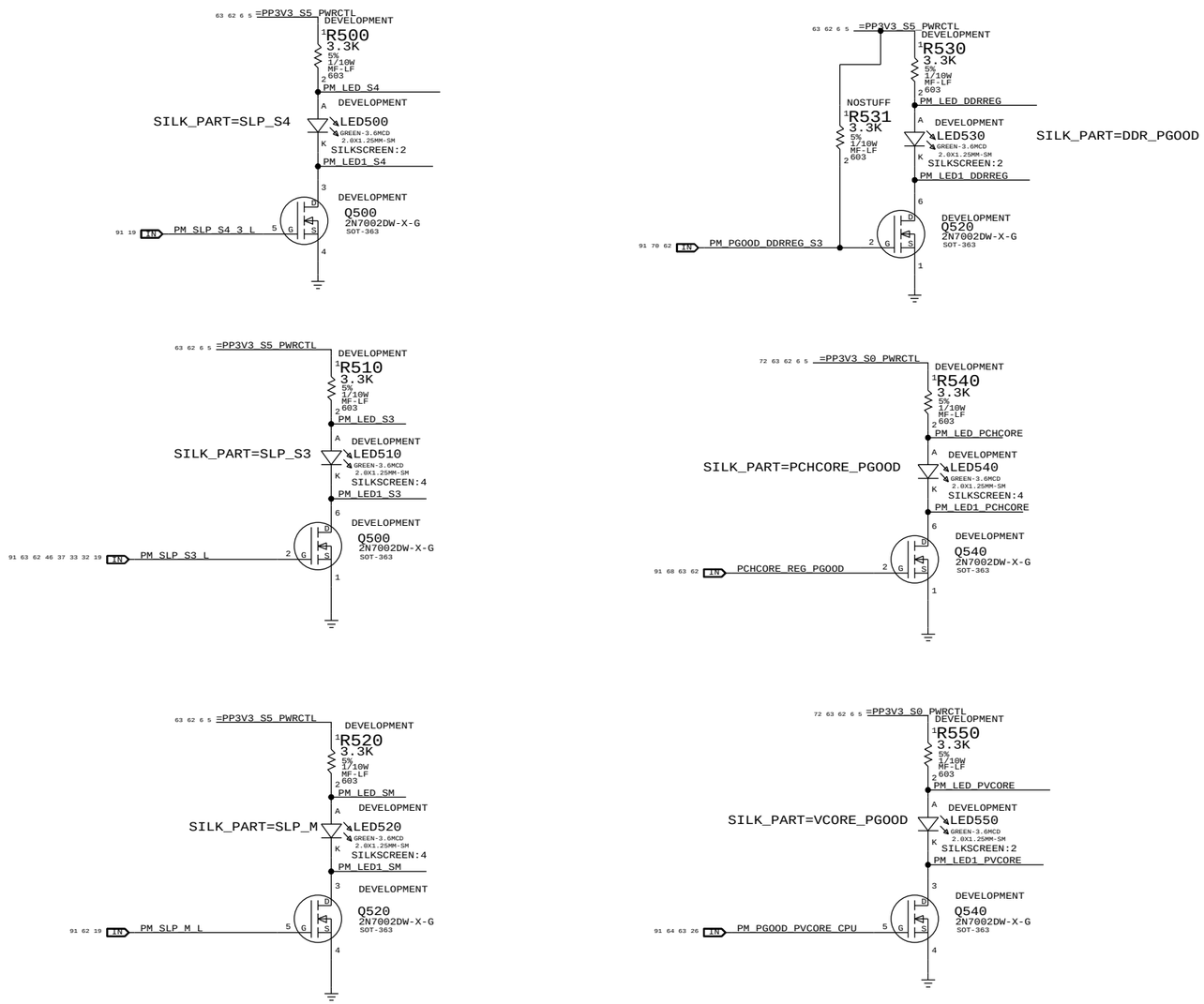
CAN DELETE THESE FOR PROTO1 AND BEYOND



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
PROTO 0 DEBUG LEDS

Apple Inc.

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EMC: C600,C626,C627,C628,C629,C630,C631

PLACE AT J600.

518-0352
CRITICAL
J600
76833-0100
M-RT-TH

=SMB_ACDC_SCL
=PP5V_S0_SATA
PP12V_G3H
LCD_PWM
=SMB_ACDC_SDA
PP12V_S0
LCD_BKL_ON

C623 10UF 20% 16V X5R 805
C631 0.001UF 10% 50V X7R 402
C627 0.001UF 10% 50V X7R 402
C626 0.001UF 10% 50V X7R 402
C630 0.001UF 10% 50V X7R 402
C624 10UF 10% 16V X5R-CERM 1210

PM_ACDC_PS_ON
Q610 2N7002 SOT23-HF1
C600 0.001UF 10% 50V X7R 402
IN PM_SLPS3_BUF2_L

PP3V3_S3
DEVELOPMENT R600 1K 5% 1/16W MF-LF 402
ITS_ALIVE
DEVELOPMENT LED605 GREEN-3.6MCD 2.0X1.25MM-SM

PP3V3_S5_REG
R601 1K 5% 1/16W MF-LF 402
ITS_PLUGGED_IN
LED601 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:1

PP3V3_S3
R602 1K 5% 1/16W MF-LF 402
CORE_VOLTAGES_ON_R
LED602 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:2
CORE_VOLTAGES_ON
Q602 2N7002DW-X-G SOT-363
IN ALL_SYS_PWRGD_R

PP3V3_S0
MXM R604 1K 5% 1/16W MF-LF 402
GPU_PRESENT_R
MXM LED604 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:3
GPU_PRESENT_DRAIN
Q602 2N7002DW-X-G SOT-363
IN MXM_GOOD

PP3V3_S0
R603 1K 5% 1/16W MF-LF 402
LCD_SHOULD_ON_R
LED603 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN:4
VIDEO_ON_L

"S0" RAILS

ONLY ON IN RUN

PPVTT_S0_DDR — MAKE_BASE=TRUE, VOLTAGE=0.75V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PPVTT_S0_DDR_FET 32
- =PP0V75_S0_MEM_VTT_B 31
- =PP0V75_S0_MEM_VTT_A 30

PPVCORE_S0_CPU — MAKE_BASE=TRUE, VOLTAGE=1.1V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.3MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PPVCORE_S0_CPU_REG 64 65 66
- =PPVCORE_S0_CPU 13 16

PPVTT_S0_CPU — MAKE_BASE=TRUE, VOLTAGE=1.1V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- =PPVTT_S0_CPU 11 13 16 46 64

PPVTT_S0 — MAKE_BASE=TRUE, VOLTAGE=1.1V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PPVTT_S0_CPU_REG 49 67
- =PPVTT_S0_PCH_VCC_DMI 22 24
- =PPVTT_S0_XDP 25
- =PPVTT_S0_PCH_VCCP_CPU 22 24

PP1V5_CPU_MEM — MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- =PP1V5_CPU_MEM 13 16 29

PP1V5_S0 — MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP1V5_S0_FET 49 72
- =PP1V5_S0_AUD_DIG 55
- =PP1V5_FWRS0_FWXIO 39
- =PP1V5_S0_CK505 26

PP1V8_S0_CPU — MAKE_BASE=TRUE, VOLTAGE=1.8V, MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- =PP1V8_S0_CPU_PLL 13 16 63

PP1V8_S0 — MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP1V8_S0_REG 49 70
- =PP3V3R1V8_S0_PCH_VCCPNAND 22 24
- =PP1V8R1V5_S0_PCH_VCCVRM 24

PPVAXG_S0_CPU — MAKE_BASE=TRUE, VOLTAGE=0V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.3MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- =PPVAXG_S0_CPU 13 17

PP3V3_S0 — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP3V3_S0_FET 72
- =PP3V3_S0_PCH 18 21 24 68
- =PP3V3_S0_FAN 52 53
- =PP3V3_S0_PCH_VCCADAC 17
- =PPSPD_S0_MEM_A 30 46
- =PPSPD_S0_MEM_B 31
- =PP3V3_S0_VRD 64
- =PP3V3_S0_AUDIO 55 57 58 59 60 61
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 22 24
- =PP3V3_S0_SMBUS 48
- =PP3V3_S0_SMC_LS 46 51
- =PP3V3_S0_SMBUS_SMC_0_S0 48
- =PP3V3_S0_SMBUS_SMC_B_S0 48
- =PP3V3_S0_SMBUS_SMC_MGMT 48
- =PP3V3_S0_DPCONN 80
- =PP3V3_S0_TSENS 51
- =PP3V3_S0_MXM 63 73 74
- =PP3V3_S0_XDP 25
- =PP3V3_S0_ODD 42
- =PP3V3_S0_SATALED 18 42
- =PP3V3_S0_SMC 46 49 50
- =PP3V3_S0_PWRCTL 5 62 63 72
- =PP3V3_S0_PCH_VCC3_3_CORE 22 24
- =PP3V3_S0_VIDEO 77
- =PP3V3_FW_FWPHY 39 40 41
- =PP3V3_FWRS0_FWXIO 39
- =PP3V3_S0_DP 77 78 79 81
- =PP3V3_S0_PCH_VCC3_3_PCI 22 24
- =PP3V3_S0_CK505 26
- =PP3V3_S0_PCH_GPIO 20
- =PP3V3_S0_PCH_STRAPS 15
- =PP3V3_S0_PCH_VCC3_3_SATA 22 24
- =PP3V3_S0_RSTBUF 27
- =PP3V3_S0_ME 72
- =PP3V3_S0_ENET 36
- =PP3V3_S0_PCH_PM 27
- =PP3V3_S0_SMBUS_SMC_BSA 48

PP5V_S0 — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP5V_S0_FET 72
- =PP5V_S0_AUDIO 55 61
- =PP5V_S0_SATA 6 42
- =PP5V_S0_MXM 73
- =PP5V_S0_VRD 64
- =PP5V_S0_ISENSE 49
- =PP5V_S0_P1V8_VREG 70
- =PP5V_S0_PCH 24
- =PP5V_S0_CPU_VTT_VREG 67
- =PP5V_S0_LPCPLUS 47
- =PP5V_S0_PCH_CORE_VREG 68

PP1V05_S0 — MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP1V05_S0_REG 68
- =PP1V05_S0_PCH_VCCADPLL 17
- =PP1V05_S0_PCH_VCCIO_DMI 22 24
- =PP1V05_S0_PCH 24
- =PP1V05_S0_SM_FET 72
- =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
- =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
- =PP1V05_S0_PCH_VCC_CORE 22 24
- =PP1V05_S0_PCH_VCCIO_USB 22 24
- =PP1V05_S0_CK505 26

PP1V05_SM_PCH_LAN — MAKE_BASE=TRUE, VOLTAGE=1.05V, THIS NET IS NOT CONNECTED TO ANY VOLTAGE RAIL. INSTEAD ON PAGE 24 IT IS CONNECTED TO GND THROUGH A RESISTOR
- =PP1V05_SM_PCH_VCC_LAN 22 24

PP0V75_S0 — MAKE_BASE=TRUE, VOLTAGE=0.75V, MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PPVTT_S0_DDR_LDO 70
- =PP0V75_S0_MEM_VTT_S0FET 32

PP12V_S0 — MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- =PP12V_S0_FAN 52 53
- =PP12V_S0_AUDIO_SPKRAMP 60
- =PP12V_S0_VRD 64
- =PPV_S0_MXM_PWR 50
- =PP12V_S0_LCD 77
- =PP12V_S0_PCH_CORE_VREG 68
- =PP12V_S0_CPU_VTT_VREG 67
- =PP12V_S0_PWRCTL 63

"S3" RAILS

ON IN RUN AND SLEEP

PP1V5_S3 — MAKE_BASE=TRUE, VOLTAGE=1.5V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP1V5_S3_REG 49 50 70
- =PP1V5_S3_MEMRESET 32
- =PPDDR_S3_S0FET 72
- =PP1V5_S3_MEM_A 28 29 30
- =PP1V5_S3_MEM_B 28 29 31

PP12V_S3 — MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP12V_S3_FET 72
- =PP12V_S3_WM 44

PP3V3_S3 — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP3V3_S3_FET 72
- =PP3V3_S3_VREFMRGN 28
- =PP3V3_S3_BT 44
- =PP3V3_S3_PCH_STRAPS 15
- =PP3V3_S3_SDCARD 44
- =PP3V3_S3_SMBUS_SMC_A_S3 48
- =PP3V3_S3_MINI 33
- =PP3V3_S3_PWRCTL 63 72
- =PP3V3_S3_WM 44
- =PP3V3_S3_SMBUS 48
- =PP3V3_S3_MEMRESET 32
- =PP3V3_S3_BRCRYPT 44
- =PP3V3_S3_ENET 37
- =PP3V3_S3_USB_HUB 34 35
- =PP3V3_S3_USB_RESET 34

PP5V_S3 — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP5V_S3_REG 69 92
- =PP5V_S3_USB 43
- =PP5V_S3_S0FET 72
- =PP5V_S3_CAMERA 44
- =PP5V_S3_IR 44
- =PP5V_S3_VREFMRGN 28
- =PP5V_S3_PWRCTL 62
- =PP5V_S3_MEMRESET 32
- =PP5V_S3_DDR_VREG 70
- =PP5V_S3_BRAY 44

PP3V3_S0M — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP3V3_SM_FET 72
- =PP3V3_SM_PCH_VCC_ME 22 24
- =PP3V3_SM_PWRCTL 63 72

PP1V05_SM — MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP1V05_SM_FET 72
- =PP1V05_SM_PCH_VCC_ME 22 24
- =PP1V05_SM_ME 63

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN S5

PP1V05_S5 — MAKE_BASE=TRUE, VOLTAGE=1.05V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP1V05_S5_REG 71
- =PP1V05_S5_SM_FET 72

PP3V3_S5 — MAKE_BASE=TRUE, VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP3V3_S5_REG 6 69
- =PP3V3_S5_PCH 18 19 24
- =PP3V3_S5_PCH_GPIO 20
- =PP3V3_S5_ROM 47 54
- =PP3V3_S5_PCH_VCCSUS3_3_USB 22 24
- =PP3V3_S5_PWRCTL 5 62 63
- =PP3V3_S5_S3FET 72
- =PP3V3_S5_S0FET 72
- =PP3V3_S5_P1V05S5_VREG 71
- =PP3V3_S5_SM_FET 72
- =PP3V3_S5_PCH_STRAPS 15
- =PP3V3_S5_CPURESET 11
- =PP3V3_S5_XDP 25
- =PP3V3_S5_MEMRESET 32
- =PP3V3_S5_LPCPLUS 47

PP5V_S5 — MAKE_BASE=TRUE, VOLTAGE=5V, MIN_LINE_WIDTH=0.4 MM, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP5V_S5_LDO 69
- =PP5V_S5_PCH 24

PP12V_S5 — MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.2 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP12V_S5_FET 3
- =PP12V_S5_DDR_VREG 70
- =PP12V_S5_P3V3S5_VREG 69
- =PP12V_S5_P5VS3_VREG 69
- =PP12V_S5_S3_FET 72
- =PP12V_S5_PWRCTL 63 72
- =PP12V_S5_FW 41

"G3H" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER AND IN G3HOT PER SMC

G3H: ALIASES

PP3V42_G3H — MAKE_BASE=TRUE, VOLTAGE=3.42V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- PP3V42_G3H_REG 71
- =PP3V3_S5_RTC_D 27
- =PP3V3_G3H_SMC 45 46
- =PP3V3_G3H_SMCUSBMUX 43
- =PP3V42_G3H_AVREF 46
- =PP3V3_G3H_LPCPLUS 47

PP12V_G3H — MAKE_BASE=TRUE, VOLTAGE=12V, MIN_LINE_WIDTH=0.6 mm, MIN_NECK_WIDTH=0.4 mm, NET_SPACING_TYPE=POWER, MAX_NECK_LENGTH=3 MM
- =PP12V_G3H_S5_FET 3

GND RAILS

GND — MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V, NET_SPACING_TYPE=GND, MAKE_BASE=TRUE, MAX_NECK_LENGTH=4.1 MM

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Power Conn / Alias

Apple Inc.

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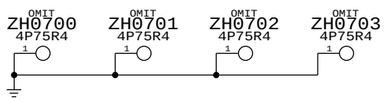
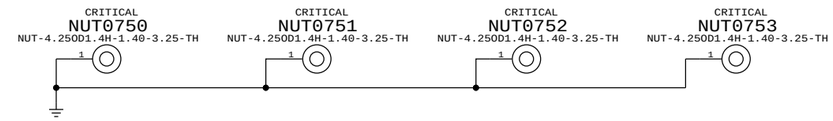
CPU Heatsink

4mm Plated Holes (998-0850)



DIMM CONNECTOR NUTS

Nuts (805-9582)



PCH HEATSINK

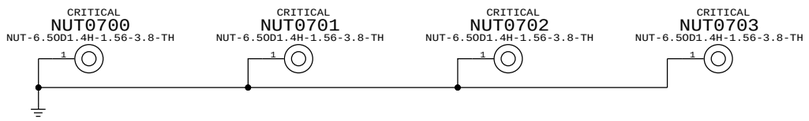
EMC Springs (870-1125) Removed 2009-10-05

Rear Cover

Standoffs (860-1255)

Backer Plate

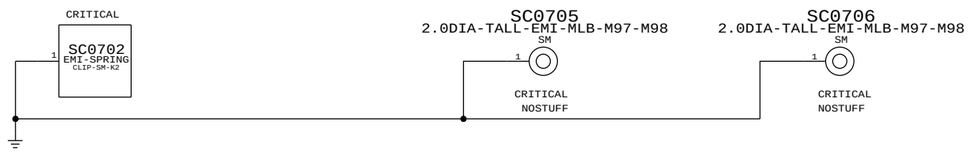
Nuts (835-0269)



For EMC

EMC Spring (870-1577); Near DIMMs

EMC POGO Pins (870-1698); Near DIMMs



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Holes

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UNUSED CPU SIGNALS

10	TP_CPU_RSVD<41..29>	NC_CPU_RSVD<41..29>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<26..1>	NC_CPU_RSVD<26..1>	MAKE_BASE=TRUE NO_TEST=TRUE
13	TP_CPU_FC_AE38	NC_CPU_FC_AE38	MAKE_BASE=TRUE NO_TEST=TRUE
13	TP_CPU_FC_AG40	NC_CPU_FC_AG40	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED PCI ALIASES

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_XDPP	NC_PCIE_CLK100M_XDPP	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_XDPN	NC_PCIE_CLK100M_XDPN	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_DMI_CLK100M_LAP	NC_DMI_CLK100M_LAP	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_DMI_CLK100M_LAN	NC_DMI_CLK100M_LAN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ1_L	NC_LPC_DREQ1_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED NAND ALIASES

20	TP_NV_CE_L<3..0>	NC_NV_CE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_NV_DQS<1..0>	NC_NV_DQS<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_NV_DQ<15..0>	NC_NV_DQ<15..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_NV_RB_L	NC_NV_RB_L	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_NV_WR_RE_L<1..0>	NC_NV_WR_RE_L<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_NV_WE_CK_L<1..0>	NC_NV_WE_CK_L<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MISC ALIASES

25	TP_JTAG_XDP_TRST_L	NC_JTAG_XDP_TRST_L	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED MEM ALIASES

12	TP_MEM_A_CS_L<7..4>	NC_MEM_A_CS_L<7..4>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
83 12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQS_N<8>	MAKE_BASE=TRUE NO_TEST=TRUE
83 12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQS_P<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_CS_L<7..4>	NC_MEM_B_CS_L<7..4>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
83 12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQS_N<8>	MAKE_BASE=TRUE NO_TEST=TRUE
83 12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQS_P<8>	MAKE_BASE=TRUE NO_TEST=TRUE

	TP_PCI_T28_D2R_N<3..0>	NC_PCI_T28_D2R_N<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_PCI_T28_D2R_P<3..0>	NC_PCI_T28_D2R_P<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_PCI_T28_R2D_C_N<3..0>	NC_PCI_T28_R2D_C_N<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
	TP_PCI_T28_R2D_C_P<3..0>	NC_PCI_T28_R2D_C_P<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_NV_RCOMP	NC_NV_RCOMP	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCIE_CLK100M_EXCARD_P	NC_PCIE_CLK100M_EXCARD_P	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCIE_CLK100M_EXCARD_N	NC_PCIE_CLK100M_EXCARD_N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7N	NC_USB_7N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_7P	NC_USB_7P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6N	NC_USB_6N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_6P	NC_USB_6P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_1N	NC_USB_1N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_1P	NC_USB_1P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3N	NC_USB_3N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_3P	NC_USB_3P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5N	NC_USB_5N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_5P	NC_USB_5P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_9N	NC_USB_9N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_9P	NC_USB_9P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10N	NC_USB_10N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_10P	NC_USB_10P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11N	NC_USB_11N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_11P	NC_USB_11P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12N	NC_USB_12N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_12P	NC_USB_12P	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13N	NC_USB_13N	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_USB_13P	NC_USB_13P	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCIE_EXCARD_D2R_P	NC_PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCIE_EXCARD_D2R_N	NC_PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCIE_EXCARD_R2D_C_P	NC_PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCIE_EXCARD_R2D_C_N	NC_PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTP	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED SATA ALIASES

18	TP_SATA_D_D2RN	NC_SATA_D_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RP	NC_SATA_D_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RN	NC_SATA_E_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RP	NC_SATA_E_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RN	NC_SATA_F_D2RN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RP	NC_SATA_F_D2RP	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CP	MAKE_BASE=TRUE NO_TEST=TRUE

NC ON UNUSED DISPLAY ALIASES

19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_N	NC_DP_IG_B_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_AUX_P	NC_DP_IG_B_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_N	NC_DP_IG_C_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_AUX_P	NC_DP_IG_C_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLN<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLP<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXN	NC_DP_IG_D_AUXN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_AUXP	NC_DP_IG_D_AUXP	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
13	TP_GFX_VID<0..6>	NC_GFX_VID<0..6>	MAKE_BASE=TRUE NO_TEST=TRUE
13	TP_GFX_VSENSE_N	NC_GFX_VSENSE_N	MAKE_BASE=TRUE NO_TEST=TRUE
13	TP_GFX_VSENSE_P	NC_GFX_VSENSE_P	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
UNUSED SIGNAL ALIAS

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PEG Slot Support

THIS SIGNAL NAME IS CONNECTED TO MXM

10 IN	PEG_CLK100M_P	84	GPU_CLK100M_PCIE_P (MAKE_BASE=TRUE)	CLK_100M_MXM_P	OUT 73
10 IN	PEG_CLK100M_N	84	GPU_CLK100M_PCIE_N (MAKE_BASE=TRUE)	CLK_100M_MXM_N	OUT 73
10 IN	=PEG_R2D_C_P<0..15>		PEG_R2D_C_P<0..15> (MAKE_BASE=TRUE)		OUT 75 84
10 IN	=PEG_R2D_C_N<0..15>		PEG_R2D_C_N<0..15> (MAKE_BASE=TRUE)		OUT 75 84
10 OUT	=PEG_D2R_P<0..15>		PEG_D2R_P<0..15> (MAKE_BASE=TRUE)		IN 75 84
10 OUT	=PEG_D2R_N<0..15>		PEG_D2R_N<0..15> (MAKE_BASE=TRUE)		IN 75 84
10 IN	PEG_CLKREQ_L		MXM_CLKREQ_L (MAKE_BASE=TRUE)		OUT 73
73	MXM_RESET_L		PEG_RESET_L (MAKE_BASE=TRUE)		27 91

91 85 19 IN PM_CLK32K_SUSCLK_R — R929 22 5% 1/10W MF-LF 402 (1, 2) — PM_CLK32K_SUSCLK OUT 45 85 91

PLACEMENT_NOTE=PLACE CLOSE TO U1800

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Signal Aliases

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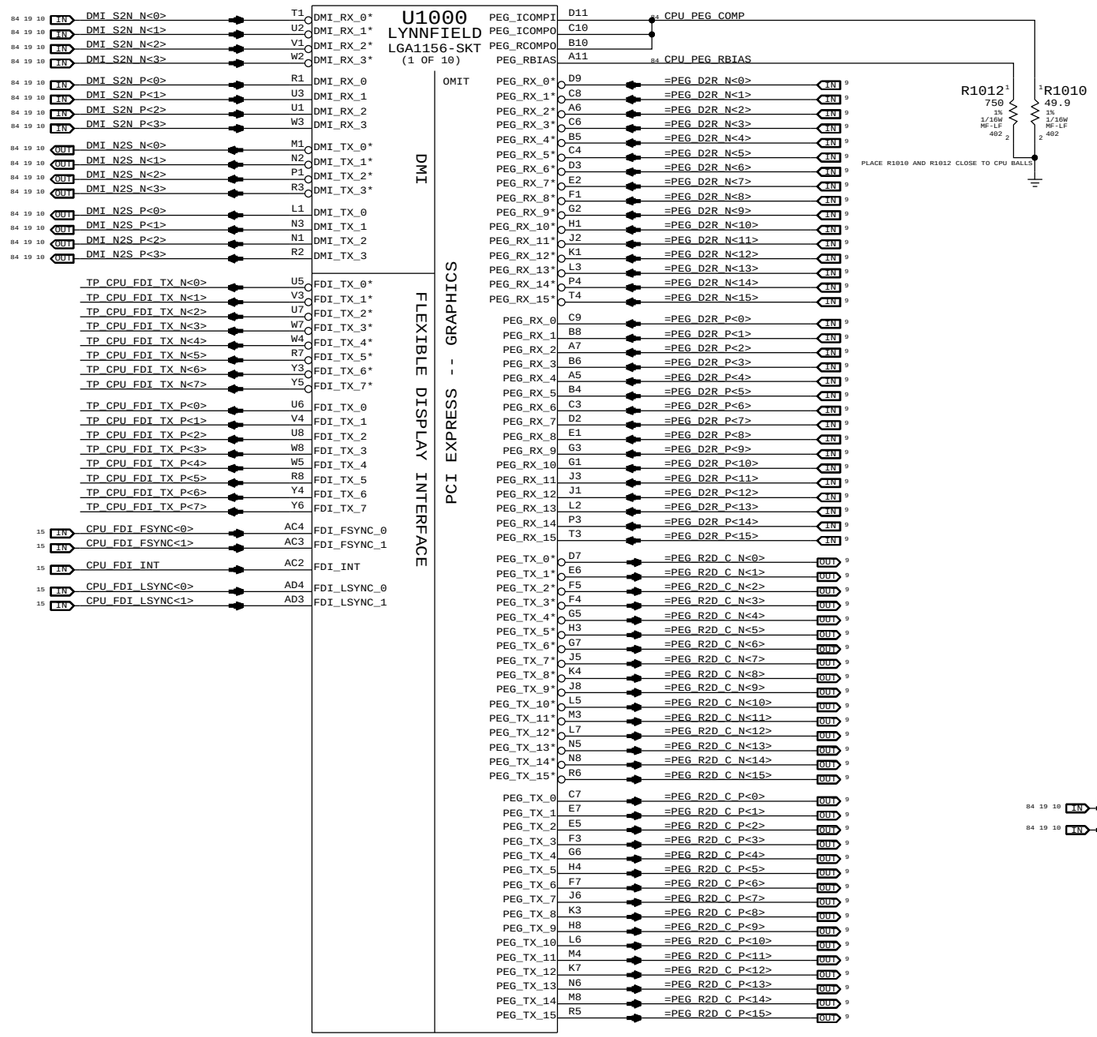
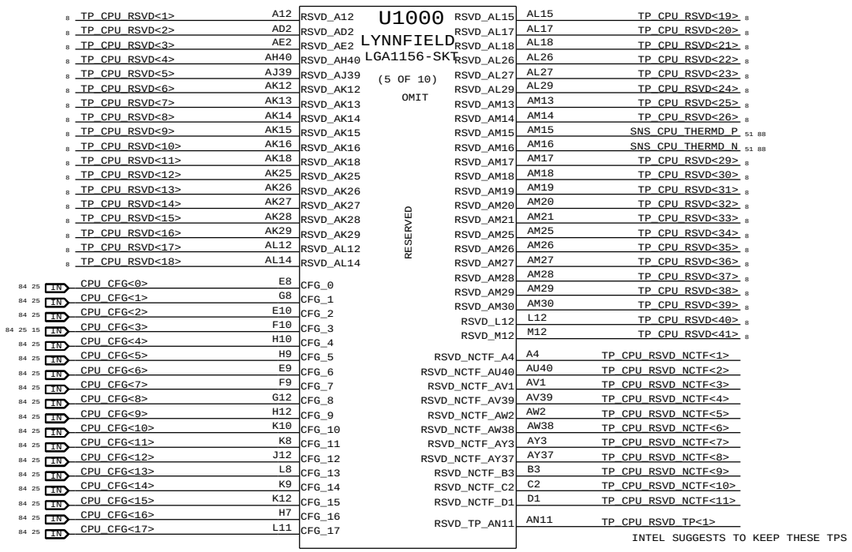
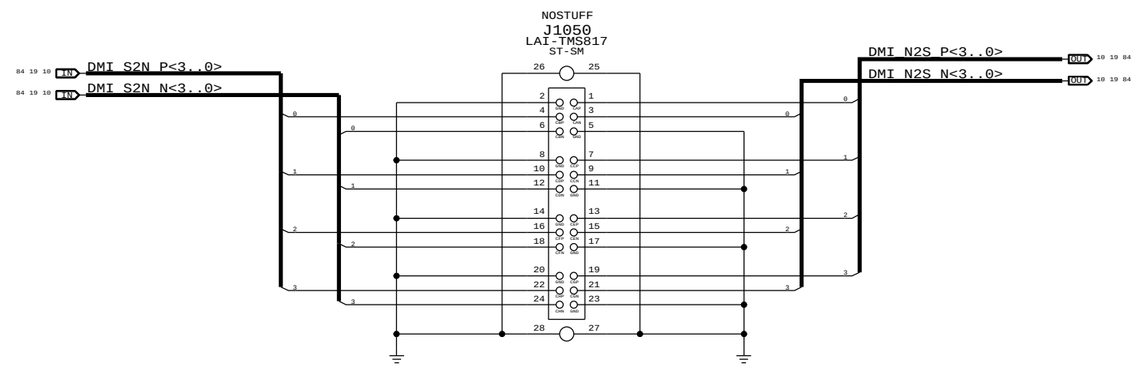
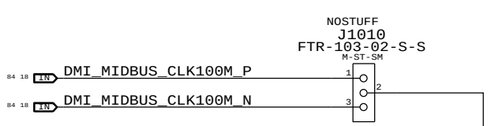




FOR LYNNFIELD PROCESSOR
CFG [1:0] :PCIE CONFIGURATION SELECT 11 = 1 X16 PCI EXPRESS 10 = 2 X8 PCI EXPRESS
FOR CLARKDALE PROCESSOR
CFG3 :PCIE LANE REVERSAL 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG4 :NOT USED ON DESKTOP



DMI MID-BUS PROBE



CLK

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

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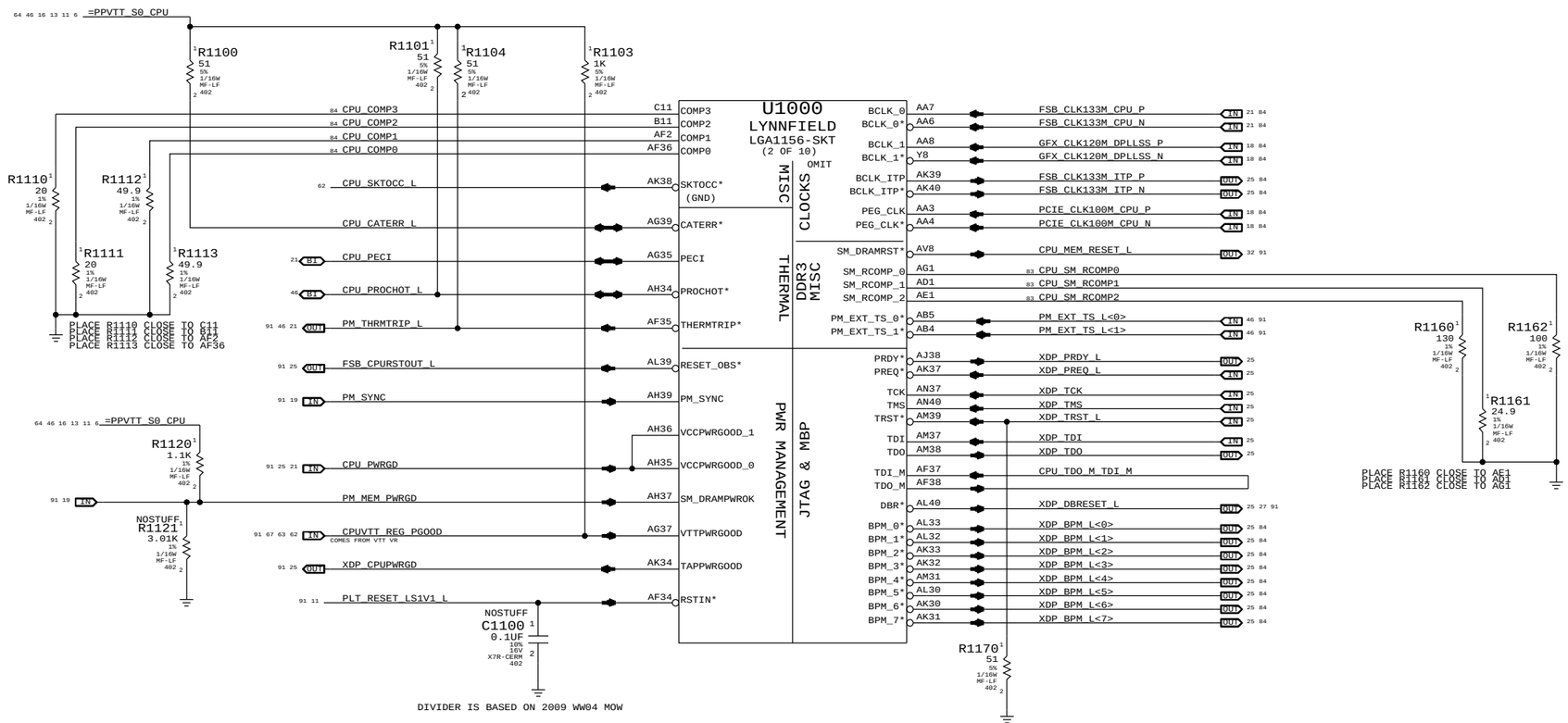

PAGE TITLE	CPU CLOCK/MISC/JTAG
Apple Inc.	DRAWING NUMBER 051-8600 SIZE D
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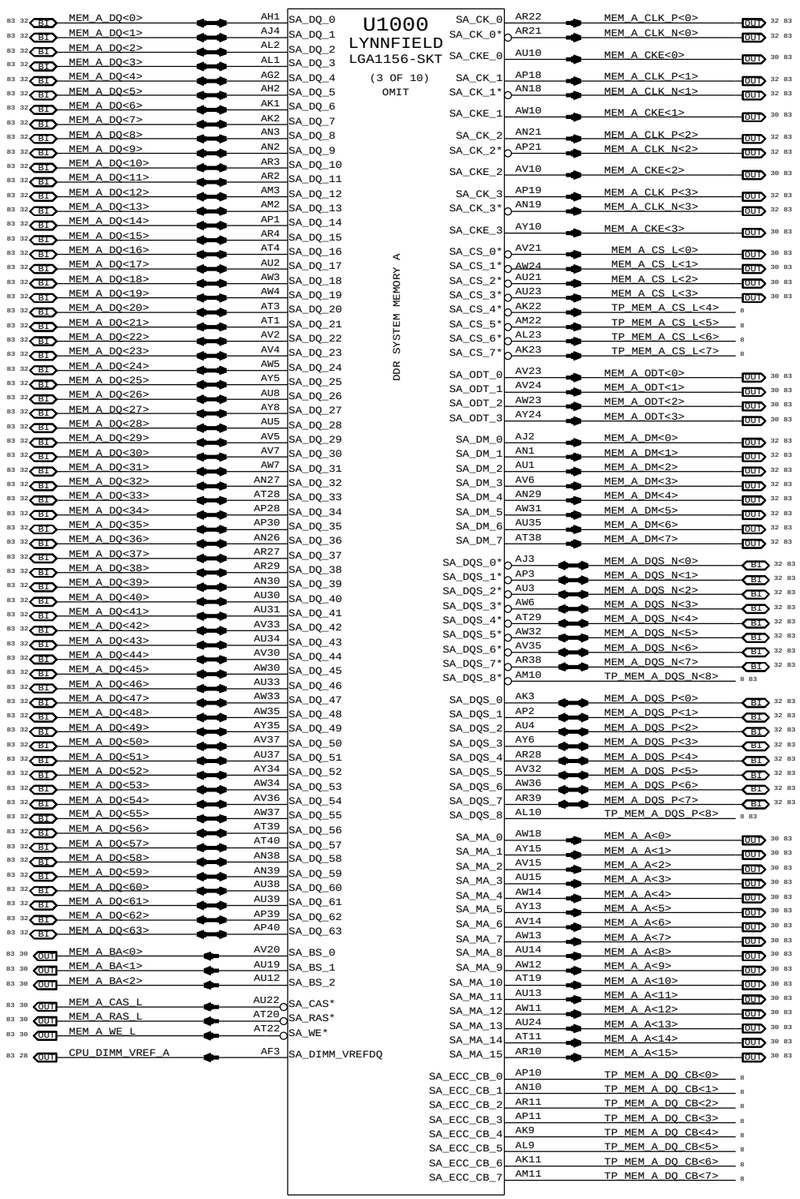

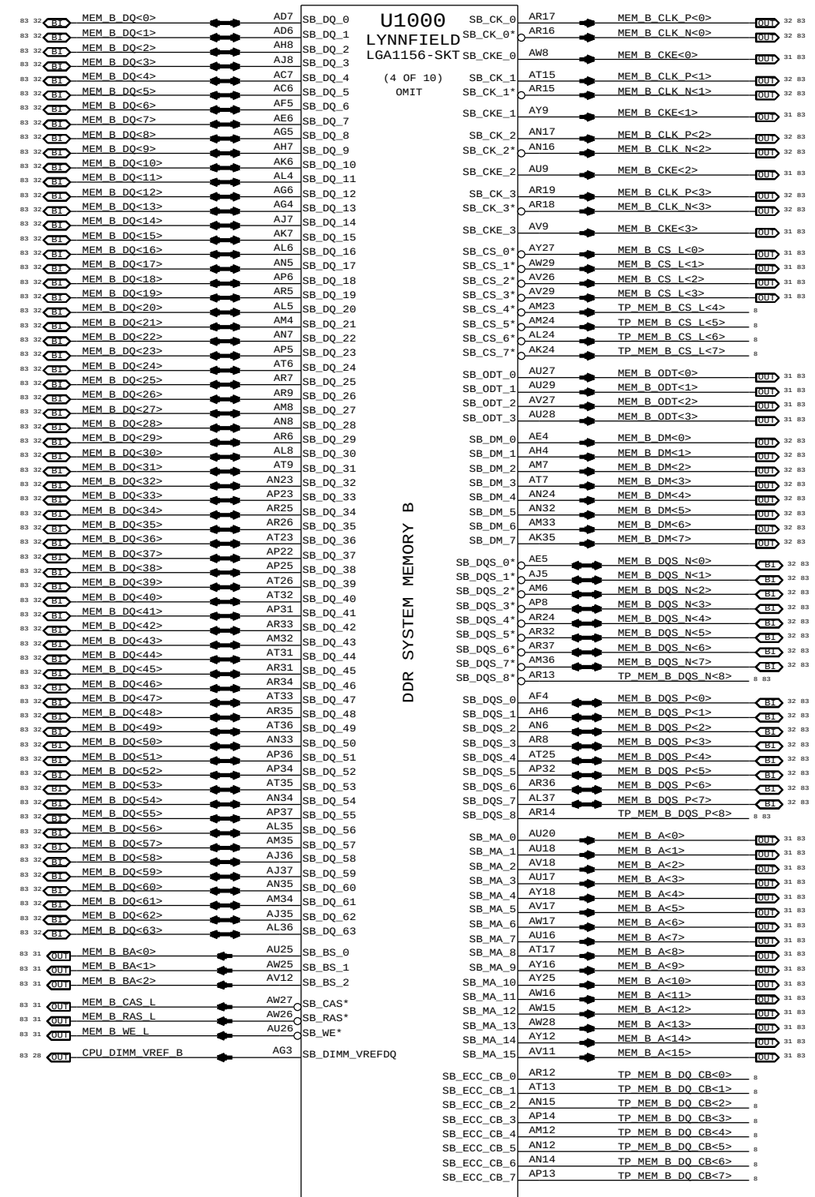

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CPU DDR3 INTERFACES

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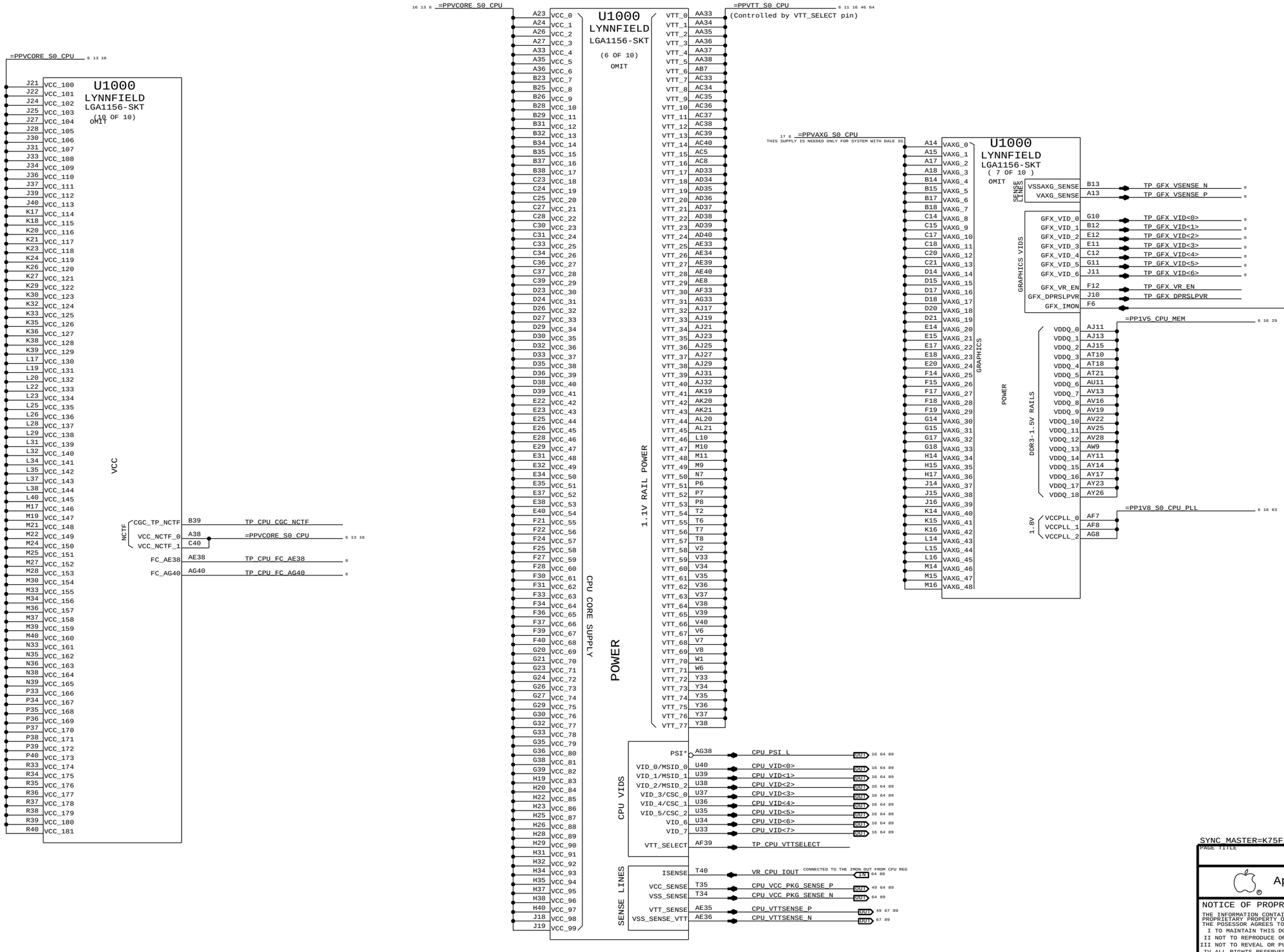

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE	CPU POWER
Apple Inc.	DRAWING NUMBER 051-8600 SIZE D
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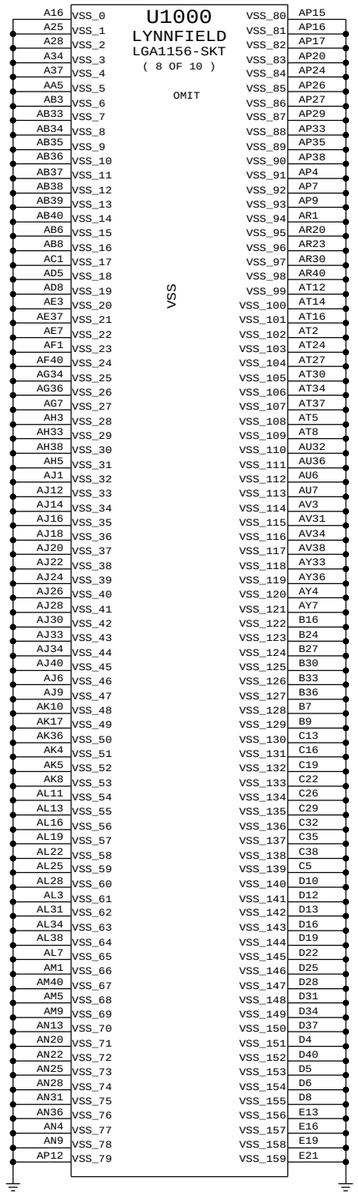

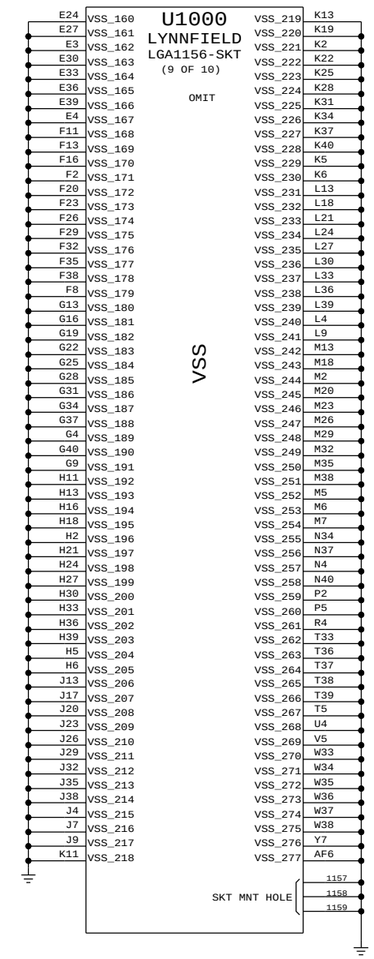

PAGE TITLE

CPU GROUNDS

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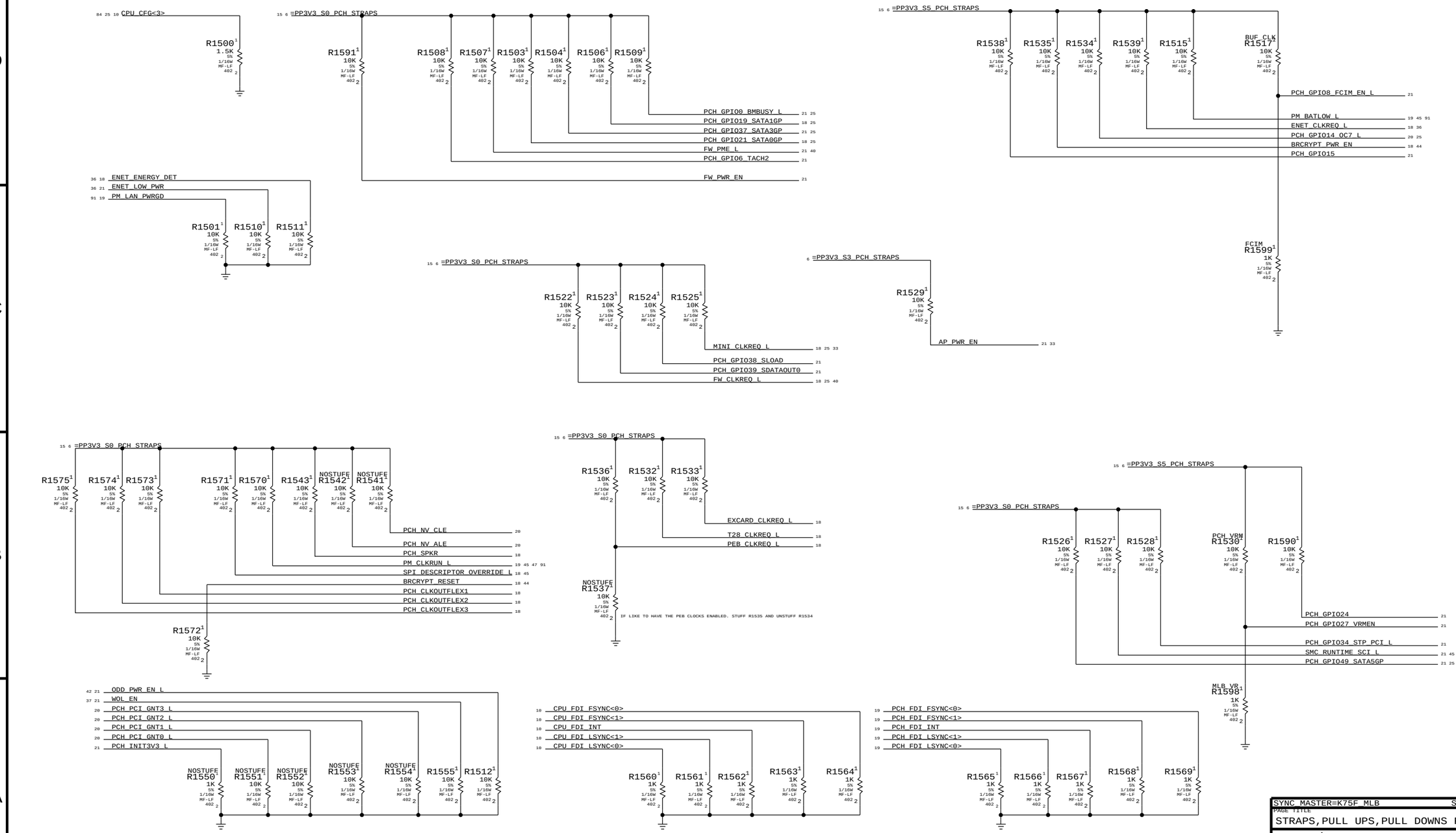

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
STRAPS,PULL UPS,PULL DOWNS FOR PCH AND CPU

Apple Inc.

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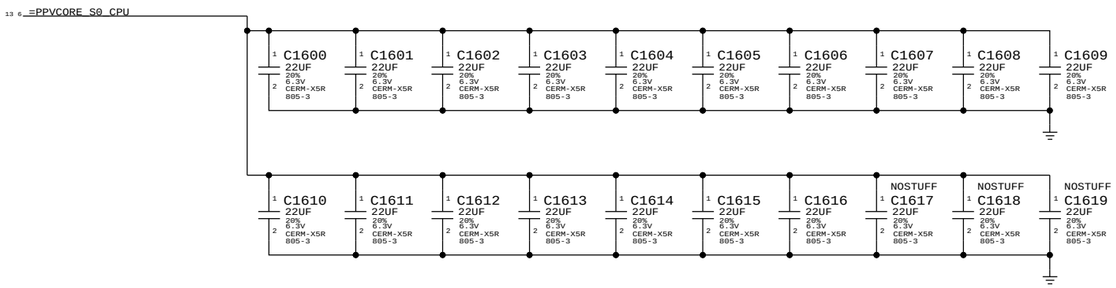
CPU VCORE DECOUPLING

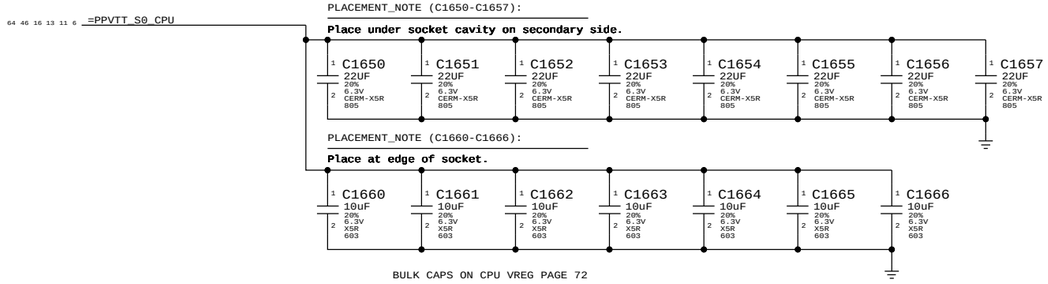
INTEL RECOMMENDATION 17X 22UF 0805



BULK CAPS ON CPU VREG PAGE 74

VTT (CPU Uncore) DECOUPLING

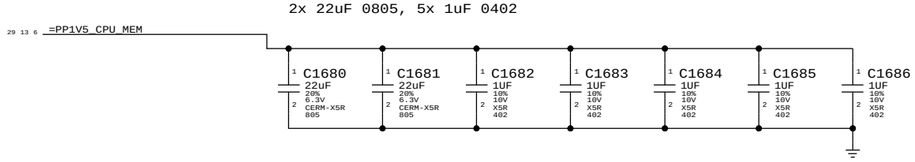
8X 22UF 0805, 7X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805



BULK CAPS ON CPU VREG PAGE 72

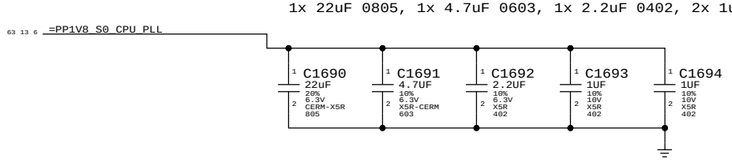
Memory (CPU VCCDDR) DECOUPLING

2x 22uF 0805, 5x 1uF 0402



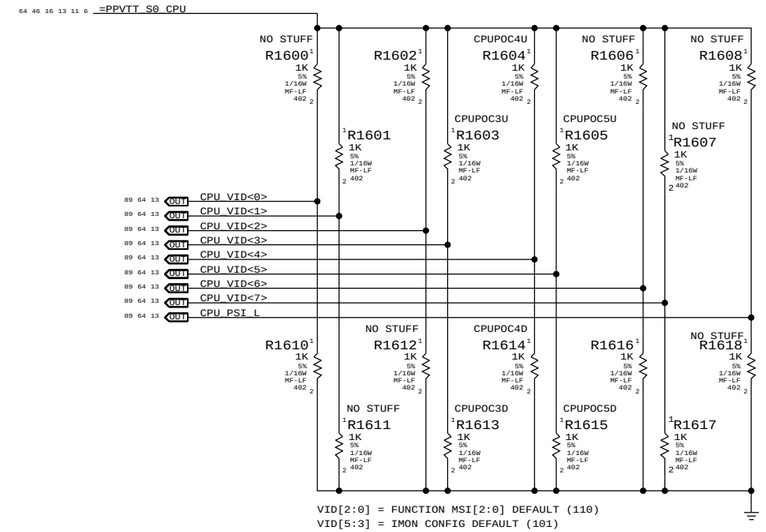
PLL (CPU VCCSFR) DECOUPLING

1x 22uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402



CPU Power On Configuration (POC) Straps

Intel recommends all option straps should be provided in layout



VID[2:0] = FUNCTION MSI[2:0] DEFAULT (110)
VID[5:3] = IMON CONFIG DEFAULT (101)
VID[6] = Reserved (0)
VID[7] = VRD SELECT (0)
PSI# = Reserved (0)

MSI - MARKET SEGMENT IDENTIFICATION
PREVENTS THE PLATFORM BOOTING USING A HIGHER POWERED CPU

BOM GROUP	IMAX @ 900mV	CPU Gain Setting	BOM OPTIONS	Equivalent Gain
CPUPOC_IMAX_DIS		000	CPUPOC3D,CPUPOC4D,CPUPOC5D	
CPUPOC_IMAX_0_40	40A	001	CPUPOC3D,CPUPOC4D,CPUPOC5U	45
CPUPOC_IMAX_40_60	60A	010	CPUPOC3D,CPUPOC4U,CPUPOC5D	30
CPUPOC_IMAX_60_80	80A	011	CPUPOC3D,CPUPOC4U,CPUPOC5U	22.5
CPUPOC_IMAX_80_100	100A	100	CPUPOC3U,CPUPOC4D,CPUPOC5D	18
CPUPOC_IMAX_100_120	120A	101	CPUPOC3U,CPUPOC4D,CPUPOC5U	15
CPUPOC_IMAX_120_140	140A	110	CPUPOC3U,CPUPOC4U,CPUPOC5D	12.857
CPUPOC_IMAX_140_180	180A	111	CPUPOC3U,CPUPOC4U,CPUPOC5U	10

NOTE: BOM Configurations should not call out CPUPOCnU/D BOMOPTIONs directly.
Instead call out appropriate BOM GROUP defined in tables above.

SYNC MASTER=K75F_MLB SYNC DATE=04/14/2010

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

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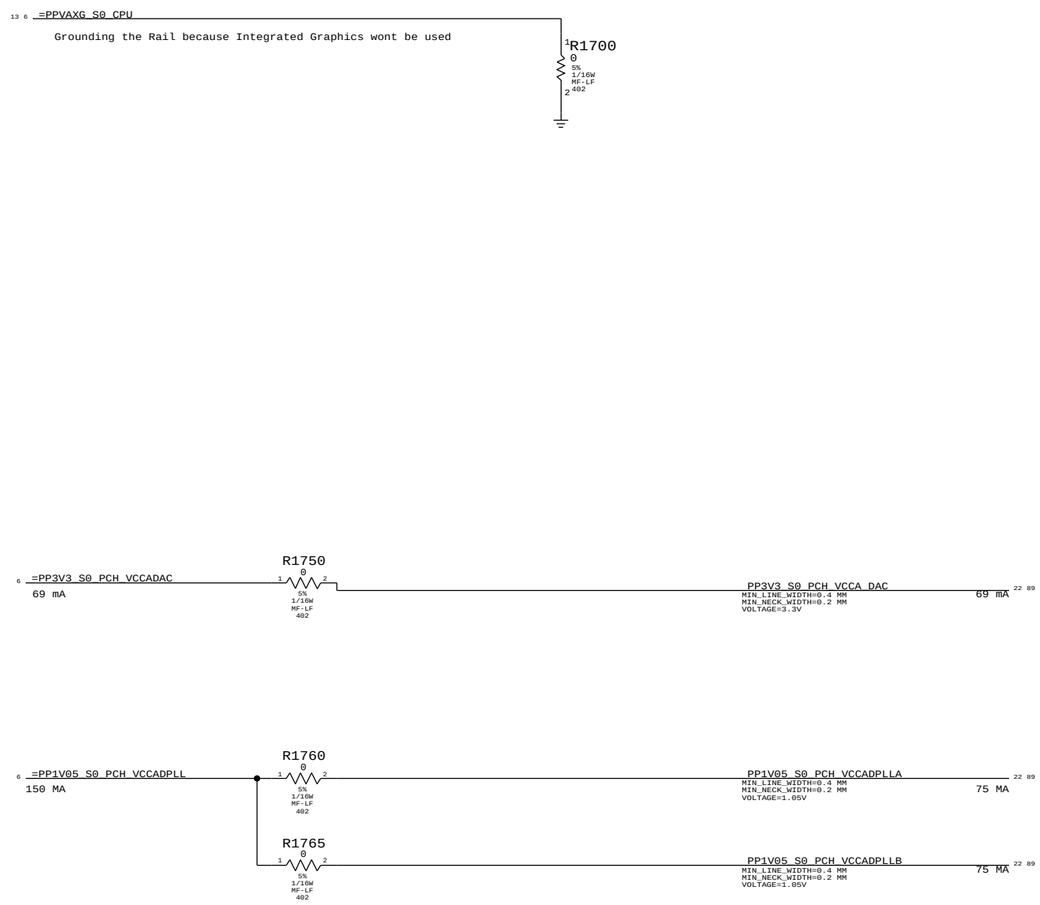

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CPU/PCH GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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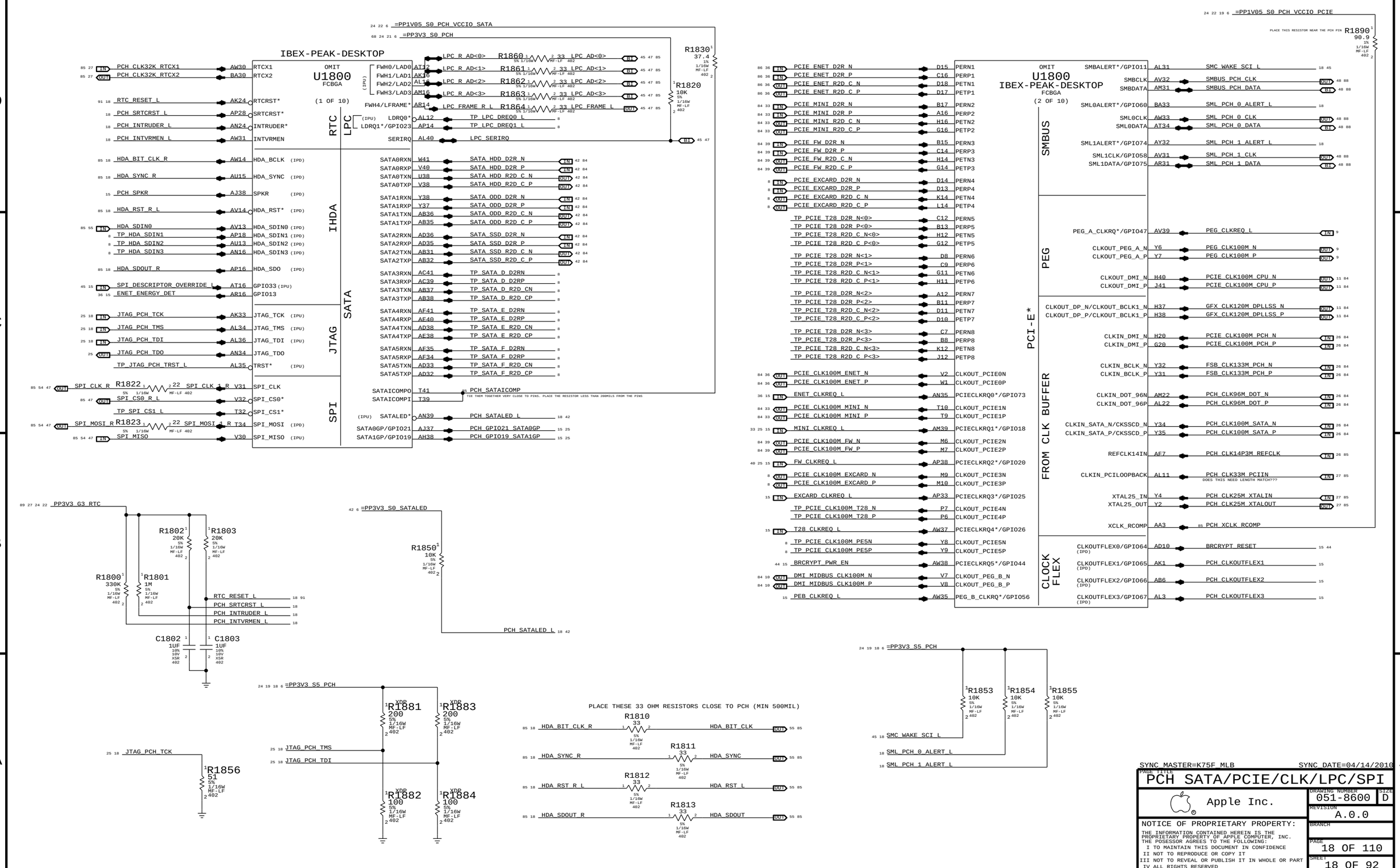

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

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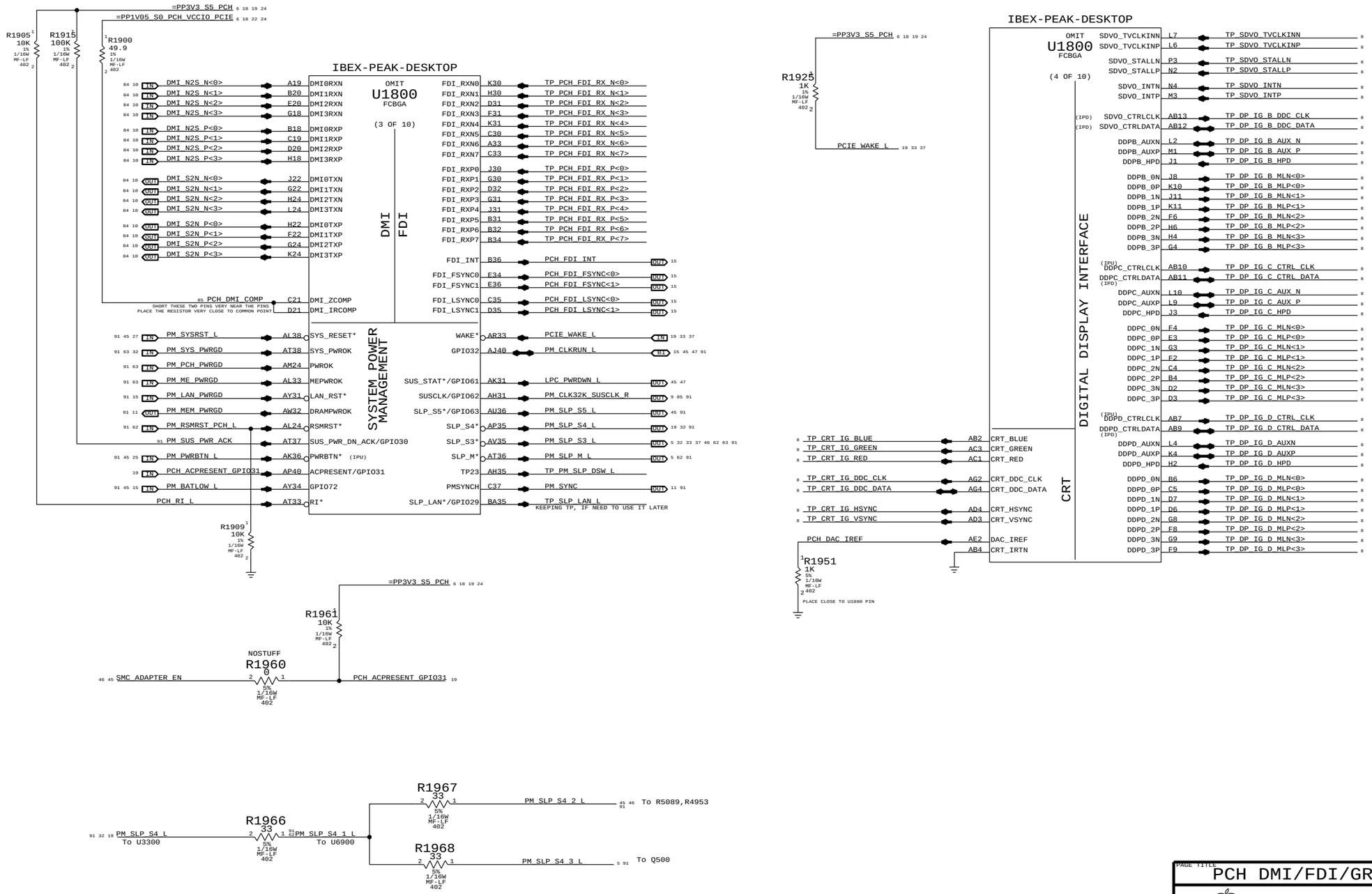

PAGE TITLE	PCH DMI/FDI/GRAPHICS
Apple Inc.	DRAWING NUMBER 051-8600 SIZE D
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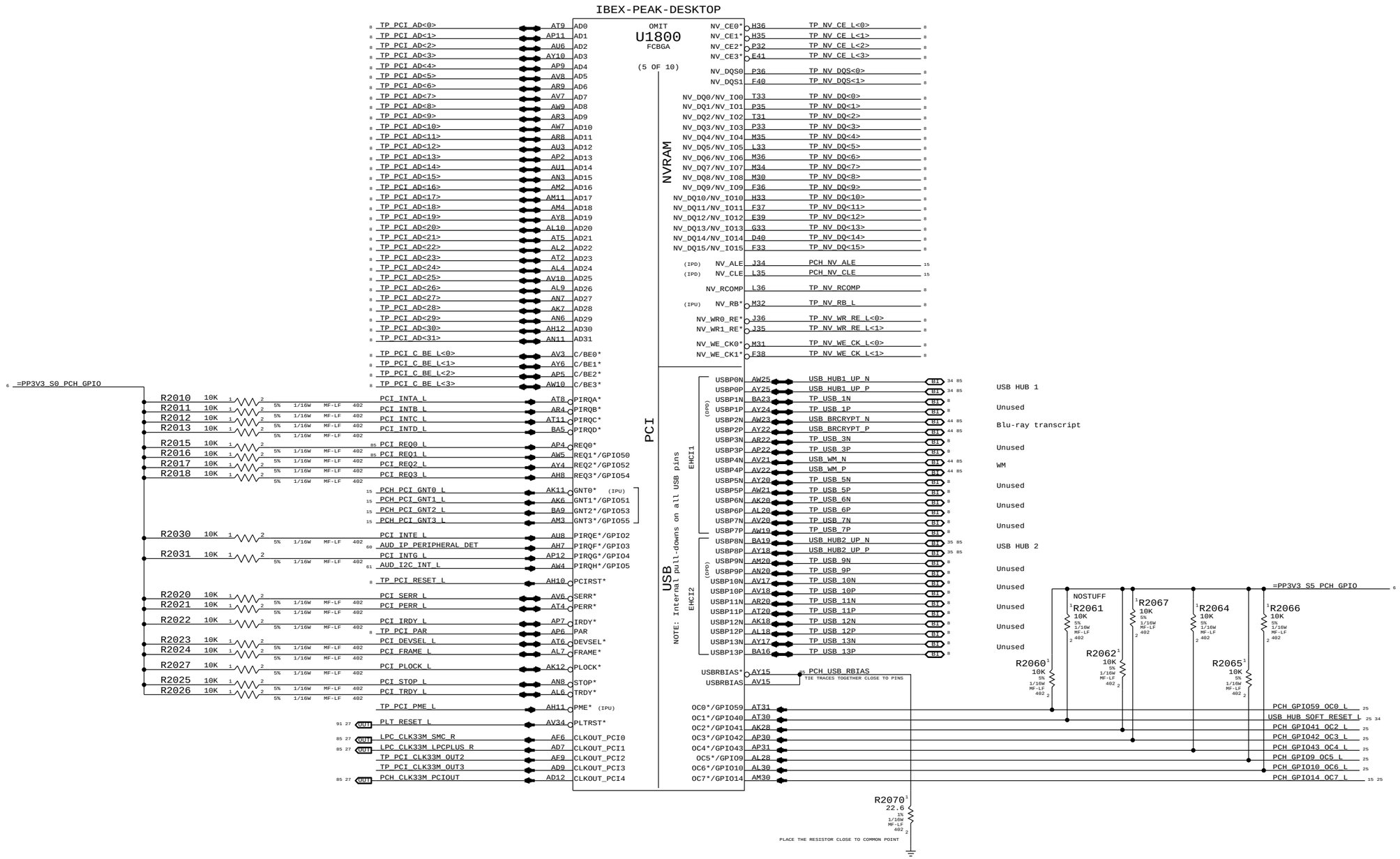

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
PCH PCI/FLASHCACHE/USB

Apple Inc.

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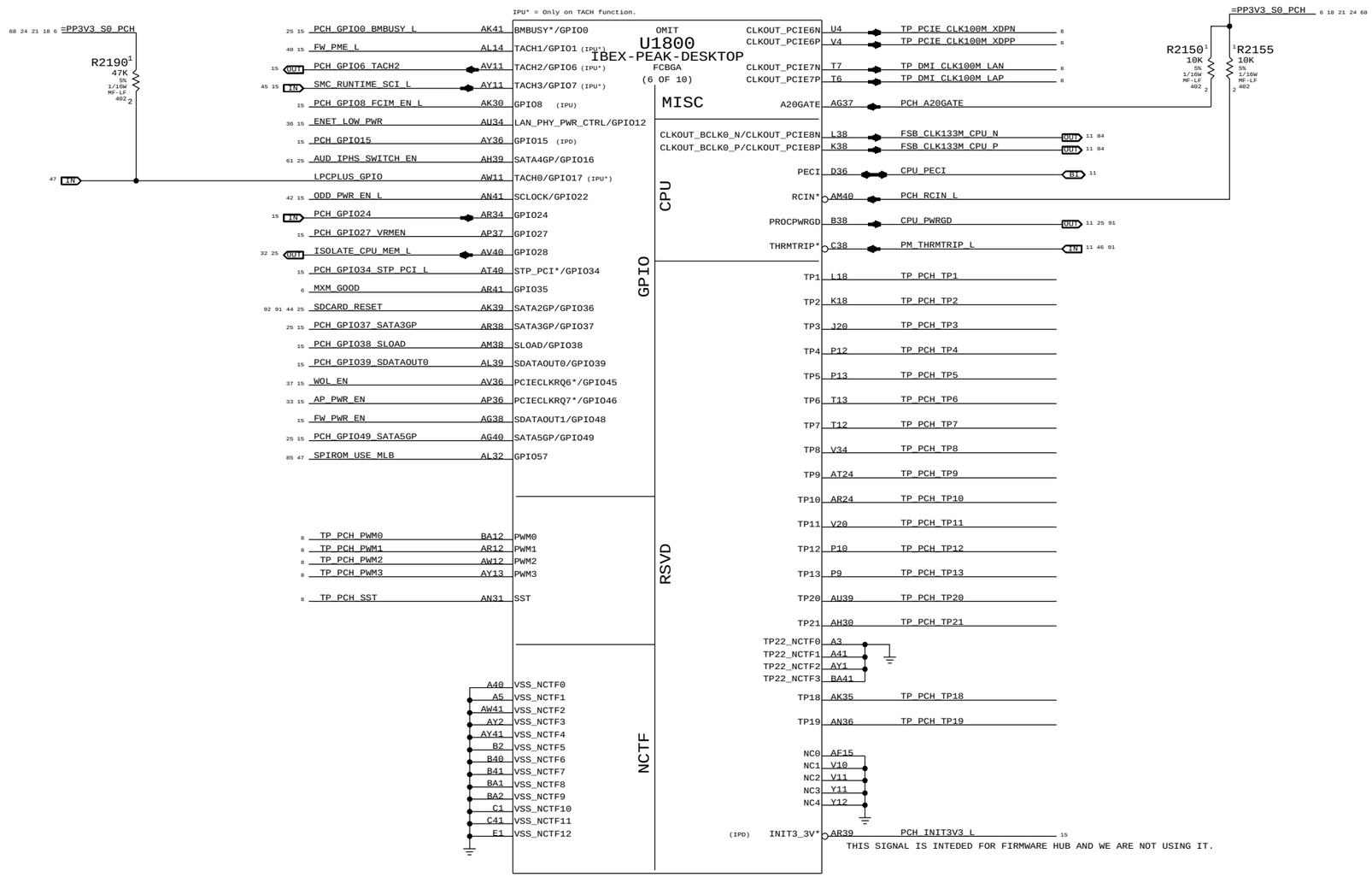

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
PCH MISC

Apple Inc.

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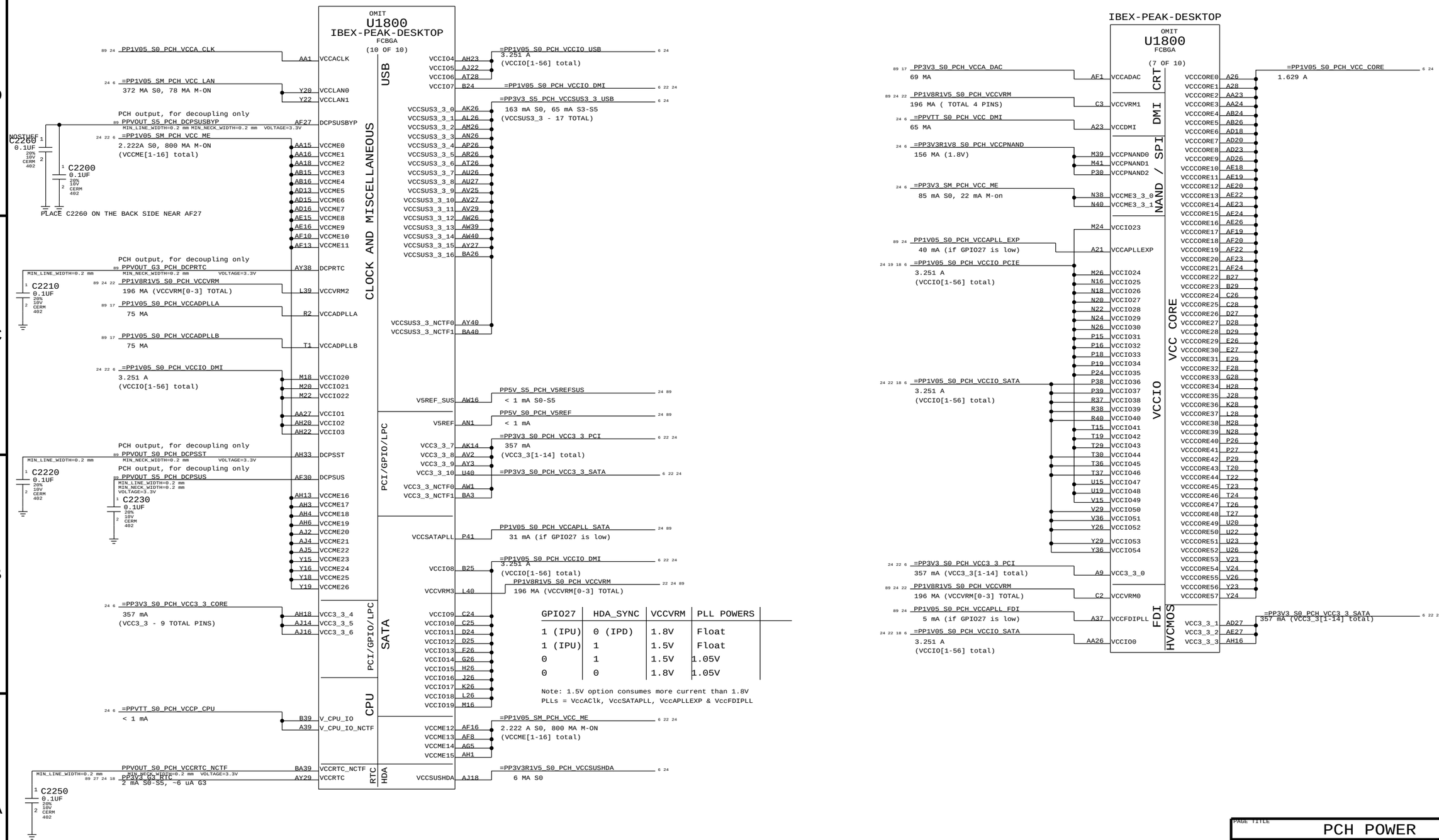

GPIO27	HDA_SYNC	VCCVRM	PLL POWERS
1 (IPU)	0 (IPD)	1.8V	Float
1 (IPU)	1	1.5V	Float
0	1	1.5V	1.05V
0	0	1.8V	1.05V

Note: 1.5V option consumes more current than 1.8V
PLLs = VccAClk, VccSATAPLL, VccAPLLEXP & VccFDIPLL

PAGE TITLE	
PCH POWER	
Apple Inc.	DRAWING NUMBER 051-8600 / SIZE D
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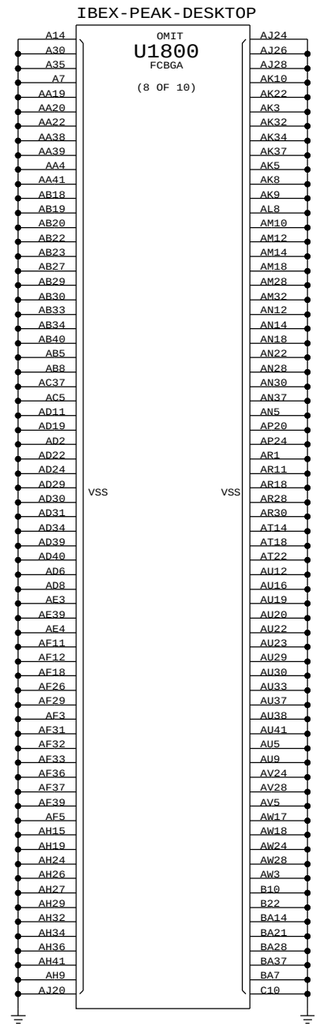

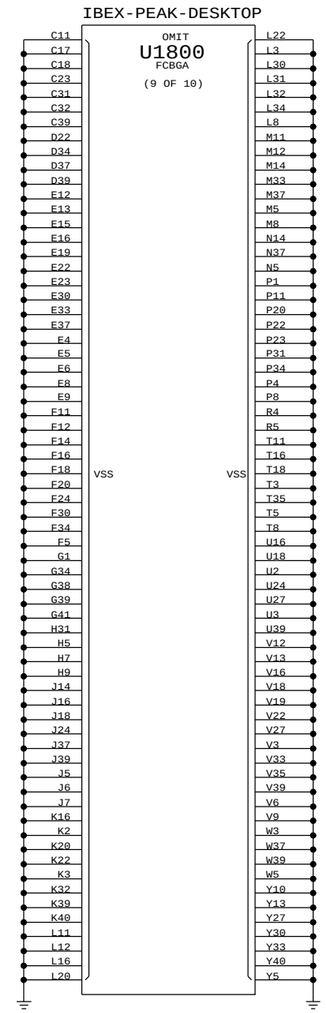

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
PCH GROUNDS

Apple Inc.

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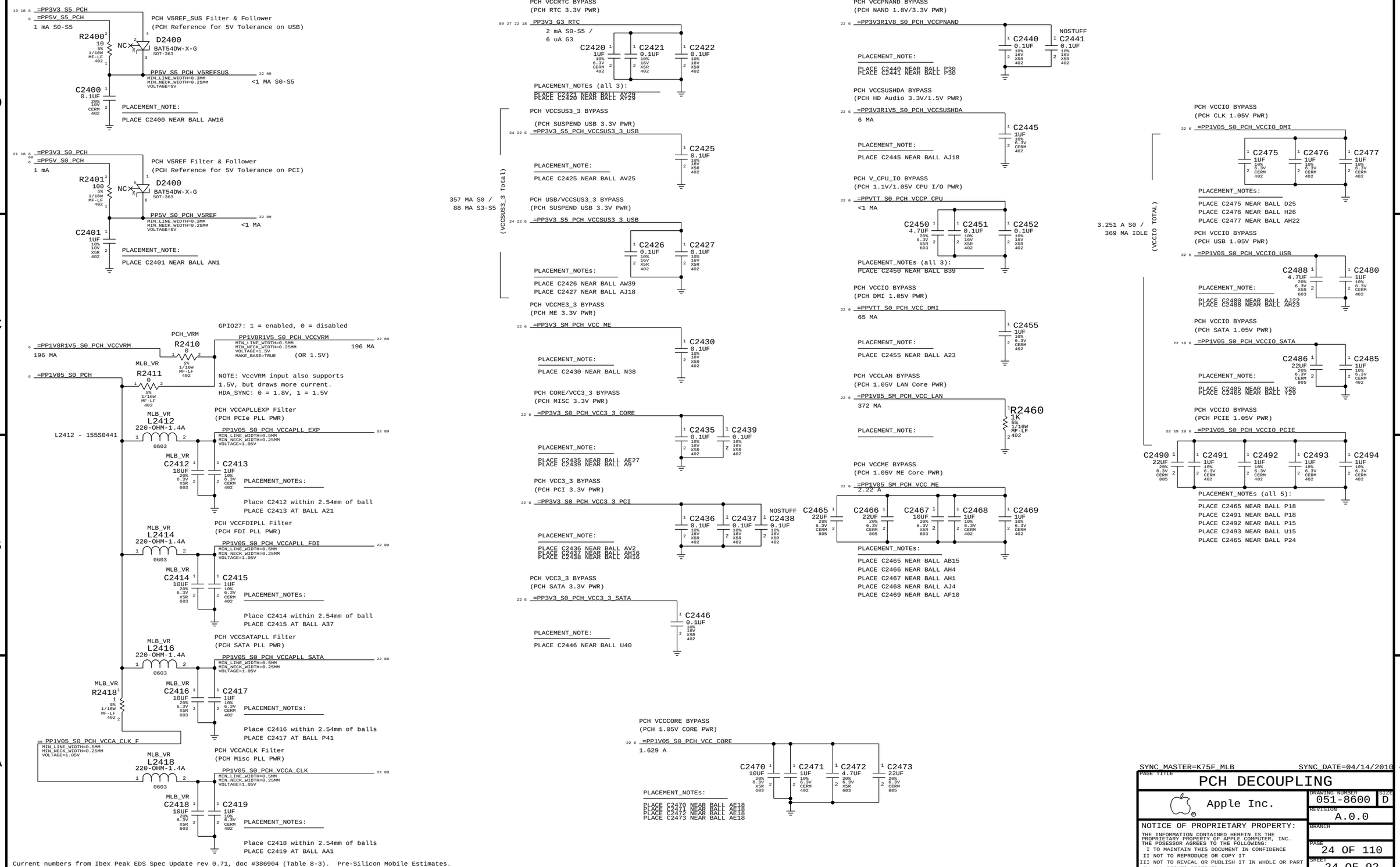

Current numbers from Ibex Peak EDS Spec Update rev 0.71, doc #386904 (Table 8-3). Pre-Silicon Mobile Estimates.

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE	PCH DECOUPLING
Apple Inc.	DRAWING NUMBER 051-8600 SIZE D
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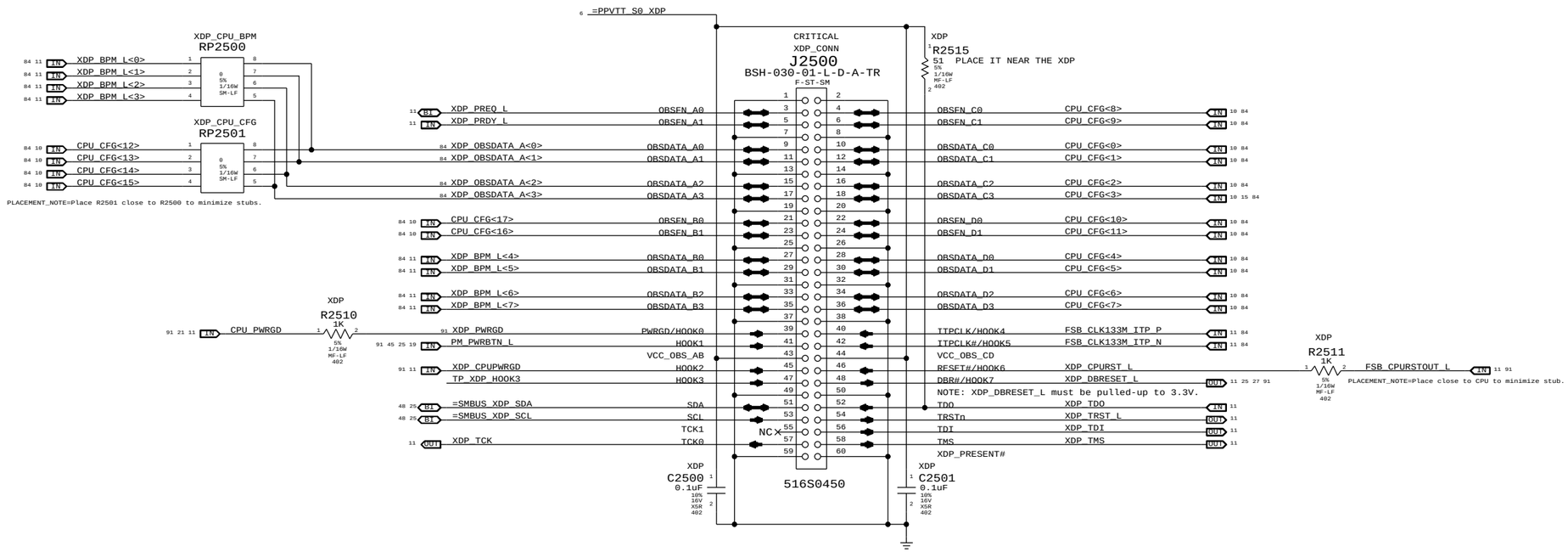
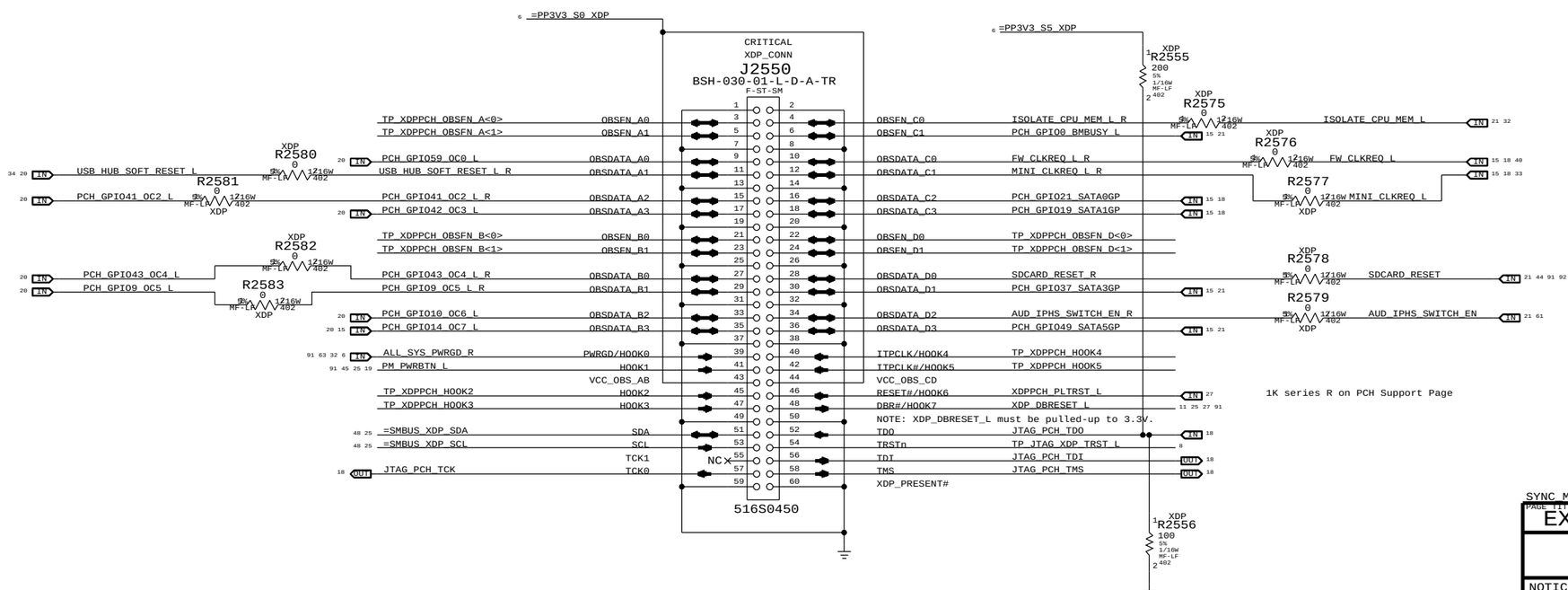
PROCESSOR XDP



PCH XDP



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE	EXTENDED DEBUG PORT(XDP)
Apple Inc.	DRAWING NUMBER 051-8600 / SIZE D
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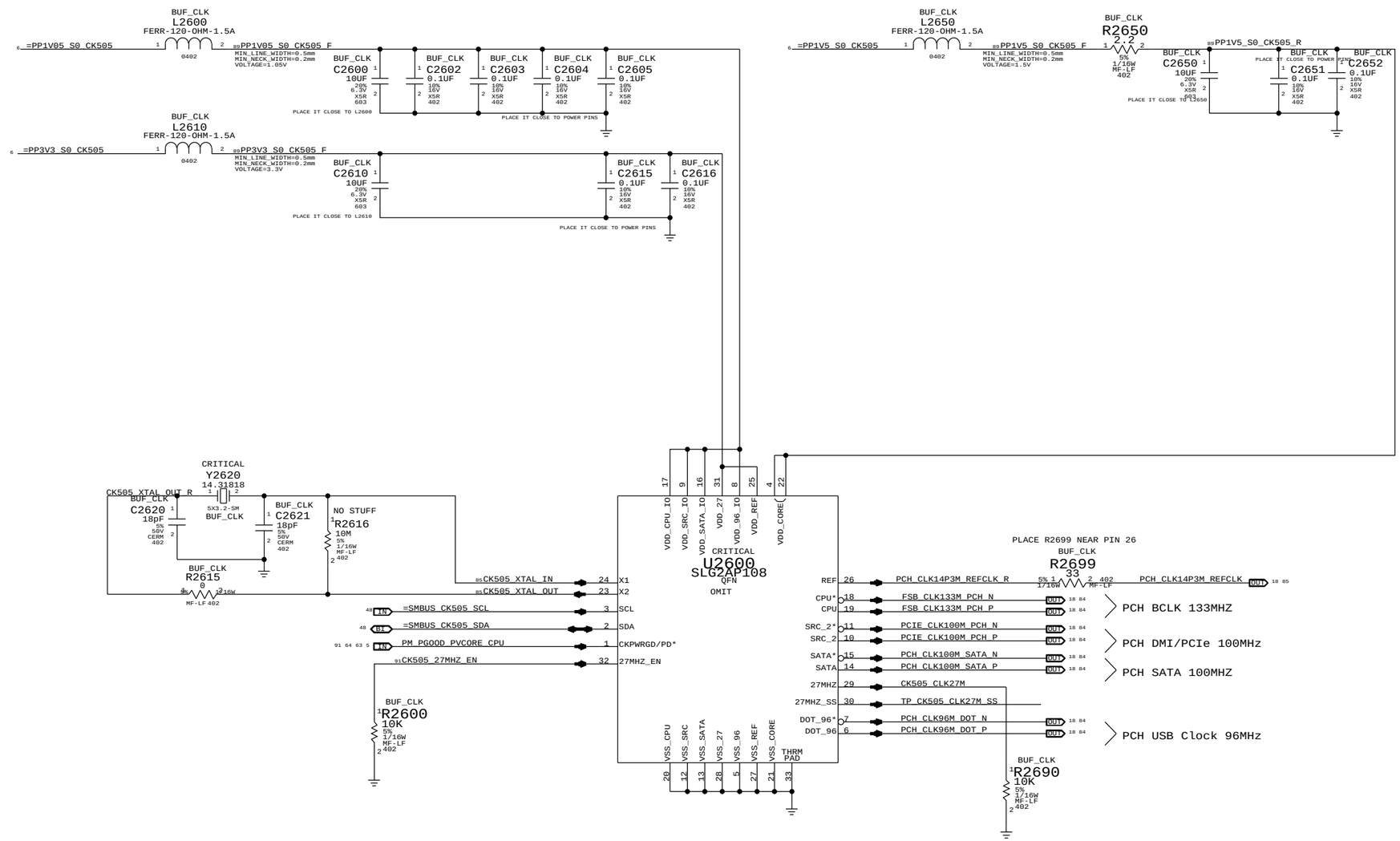

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

CLOCK (CK505)

Apple Inc.

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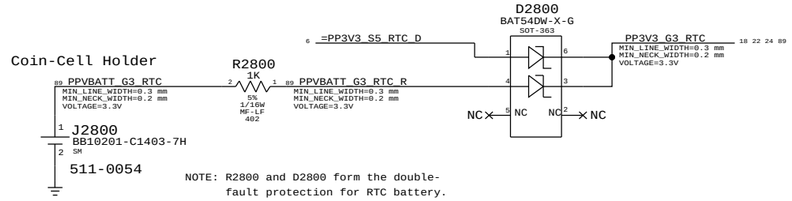
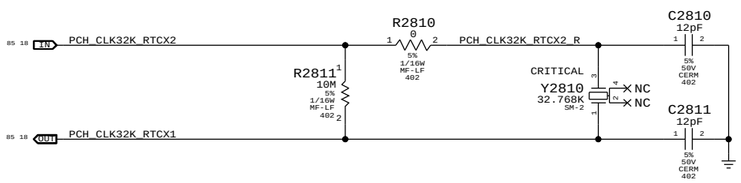
RTC Power Sources

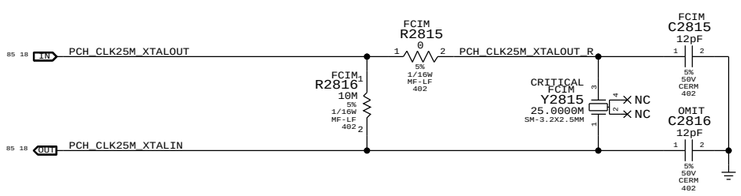


NOTE: R2800 and D2800 form the double-fault protection for RTC battery.

PCH RTC Crystal

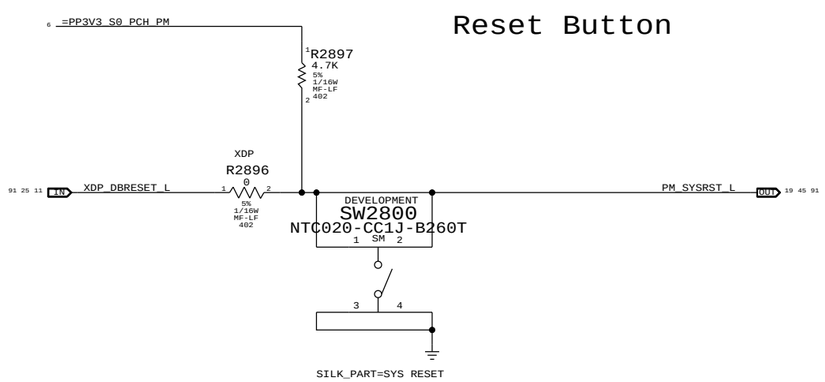


PCH 25MHz Crystal



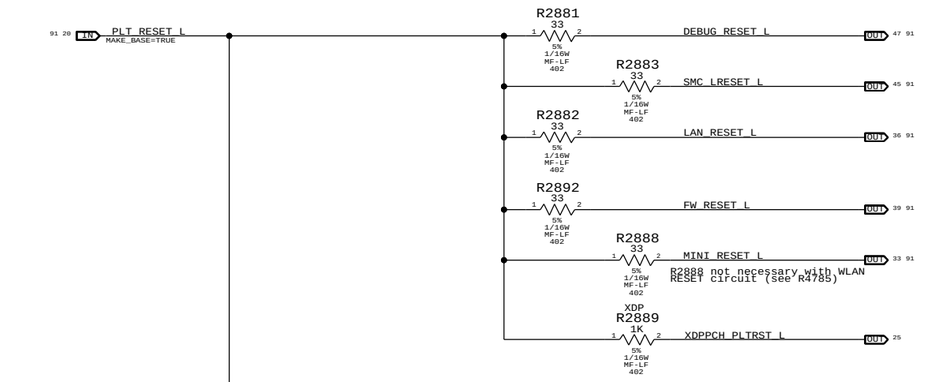
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	1	RES,0,5%,0402	C2816	

Reset Button

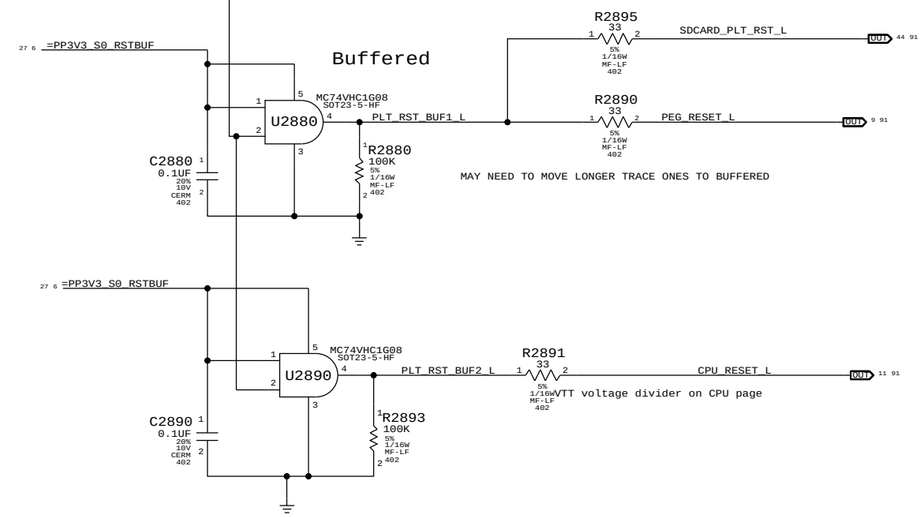


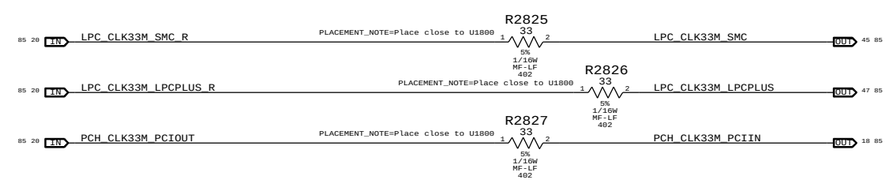
Platform Reset Connections

Unbuffered



Buffered





SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

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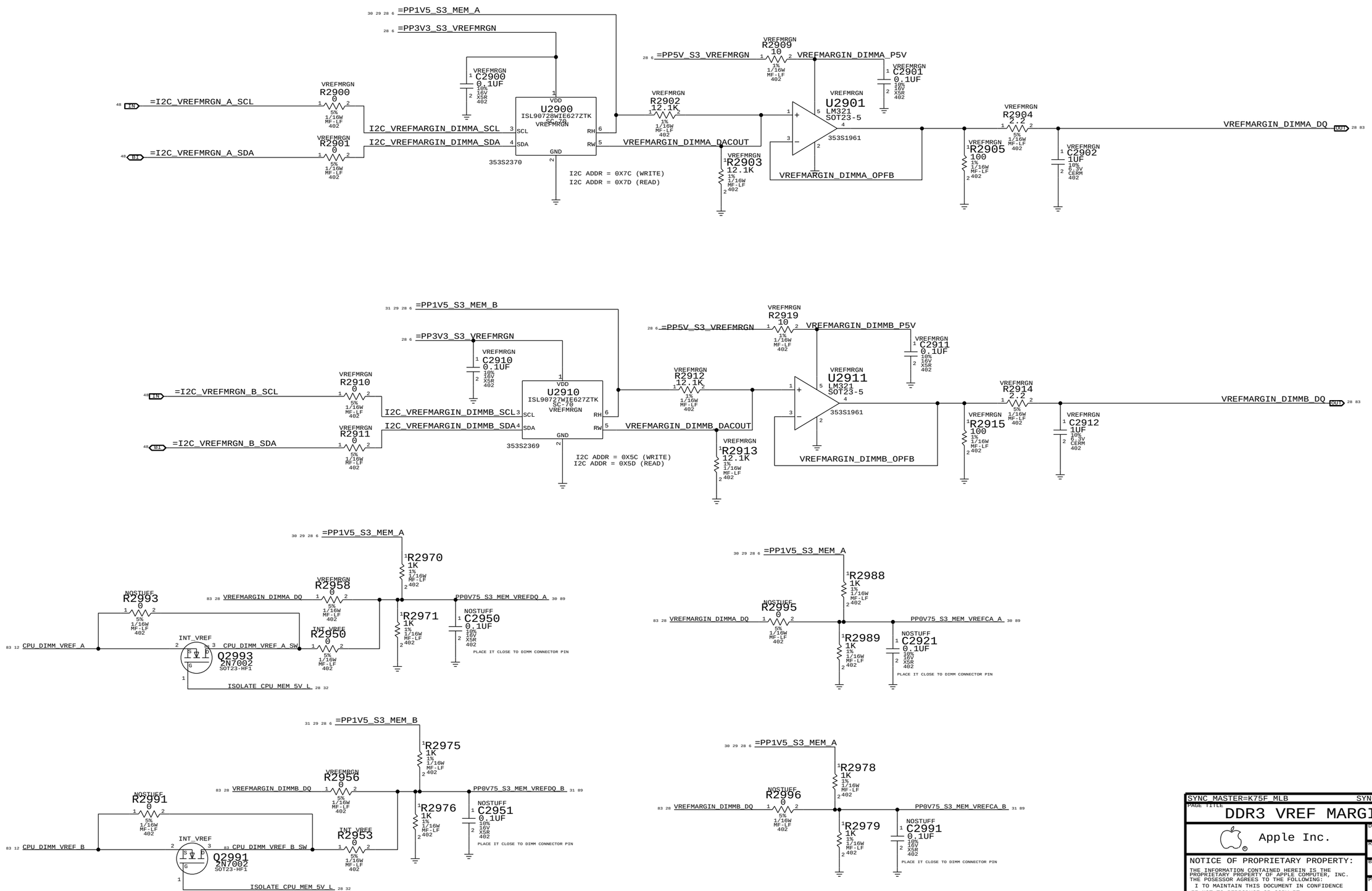

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
DDR3 VREF MARGINING

Apple Inc.

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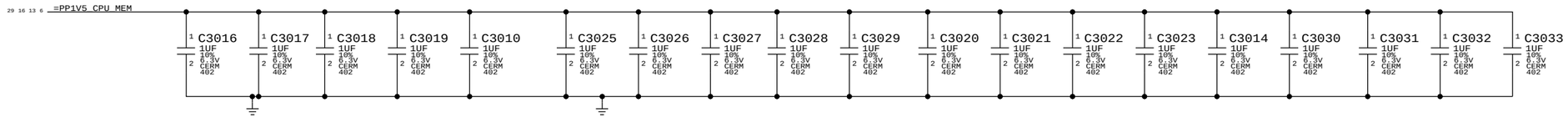
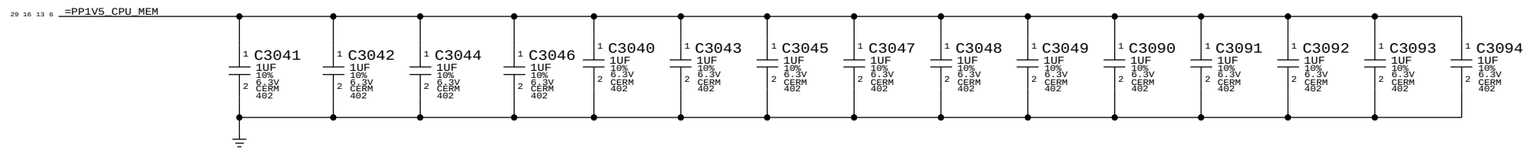
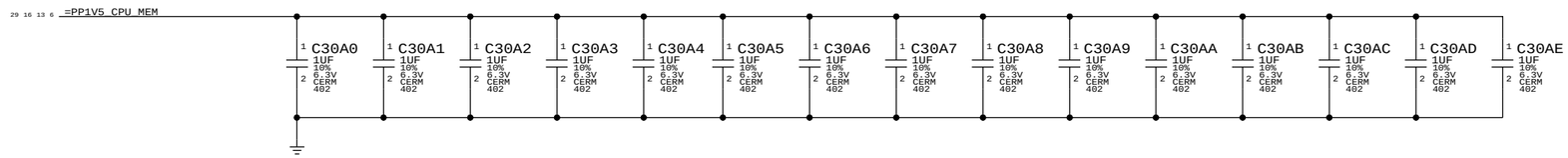
DIMM A (FURTHER FROM CPU) CAPS TO COUPLE CPU 1V5_MEM DIMM B (CLOSER TO CPU)

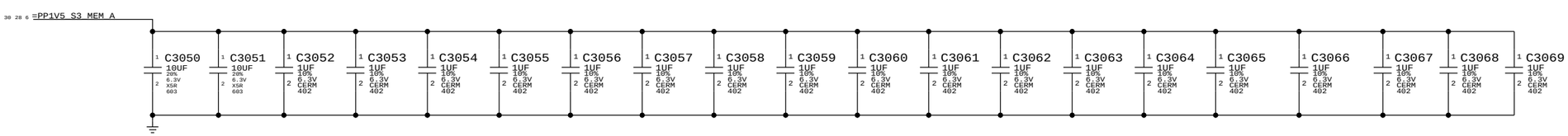


EXTRA DECOUPLING CAPS FOR CPU MEM RAIL

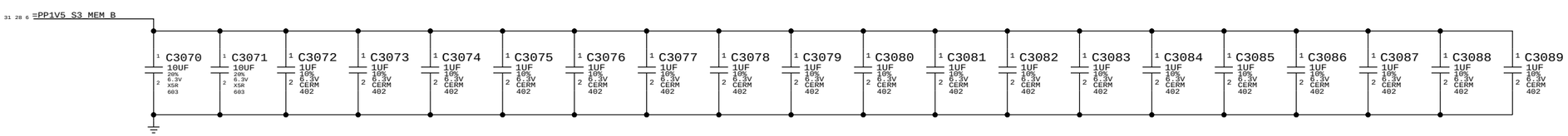




DECOUPLING CAPS FOR DIMM ON CHANNEL A - AT CONNECTOR



DECOUPLING CAPS FOR DIMM ON CHANNEL B - AT CONNECTOR



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
MEMORY CAPS

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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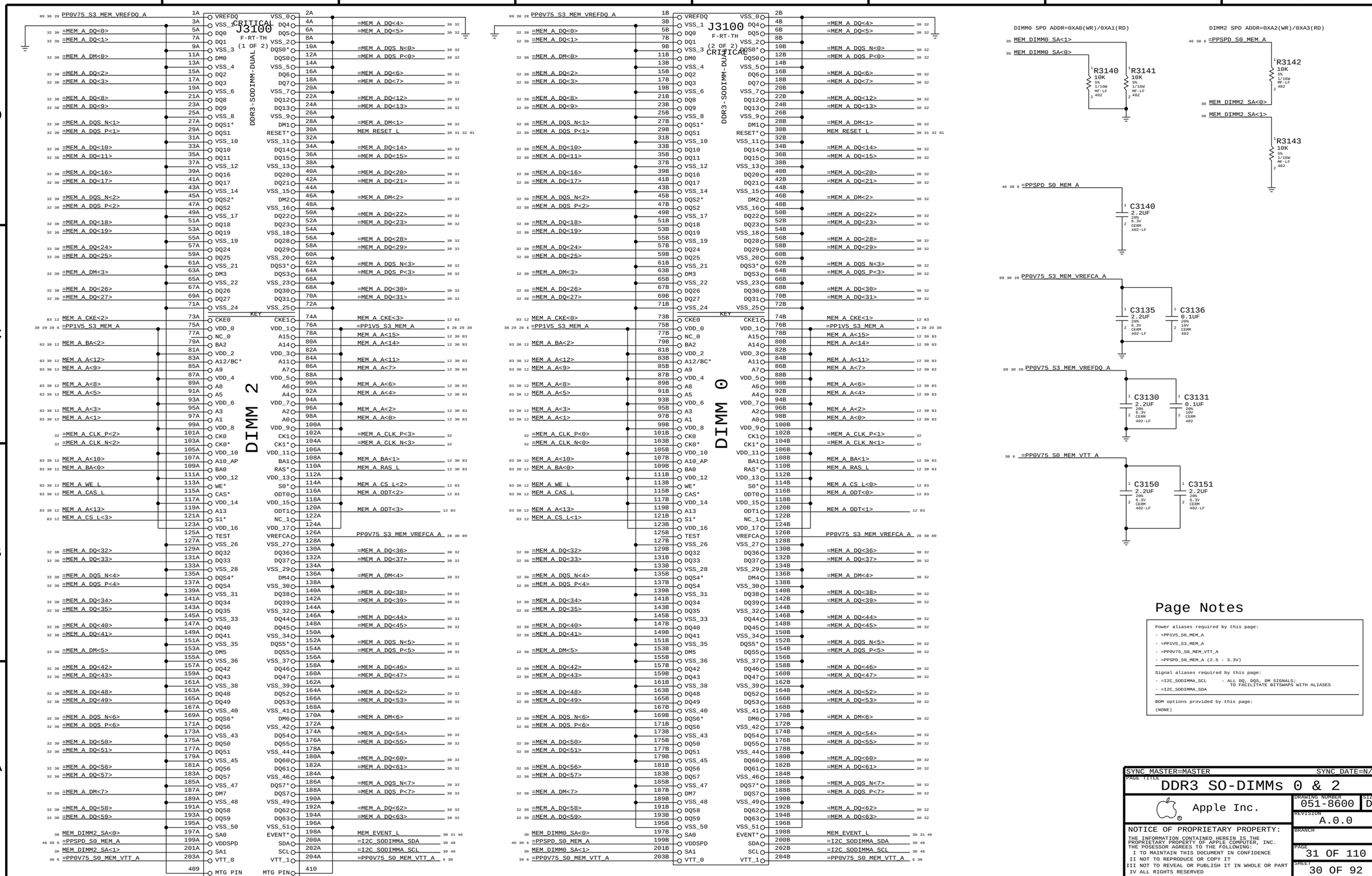


Page Notes

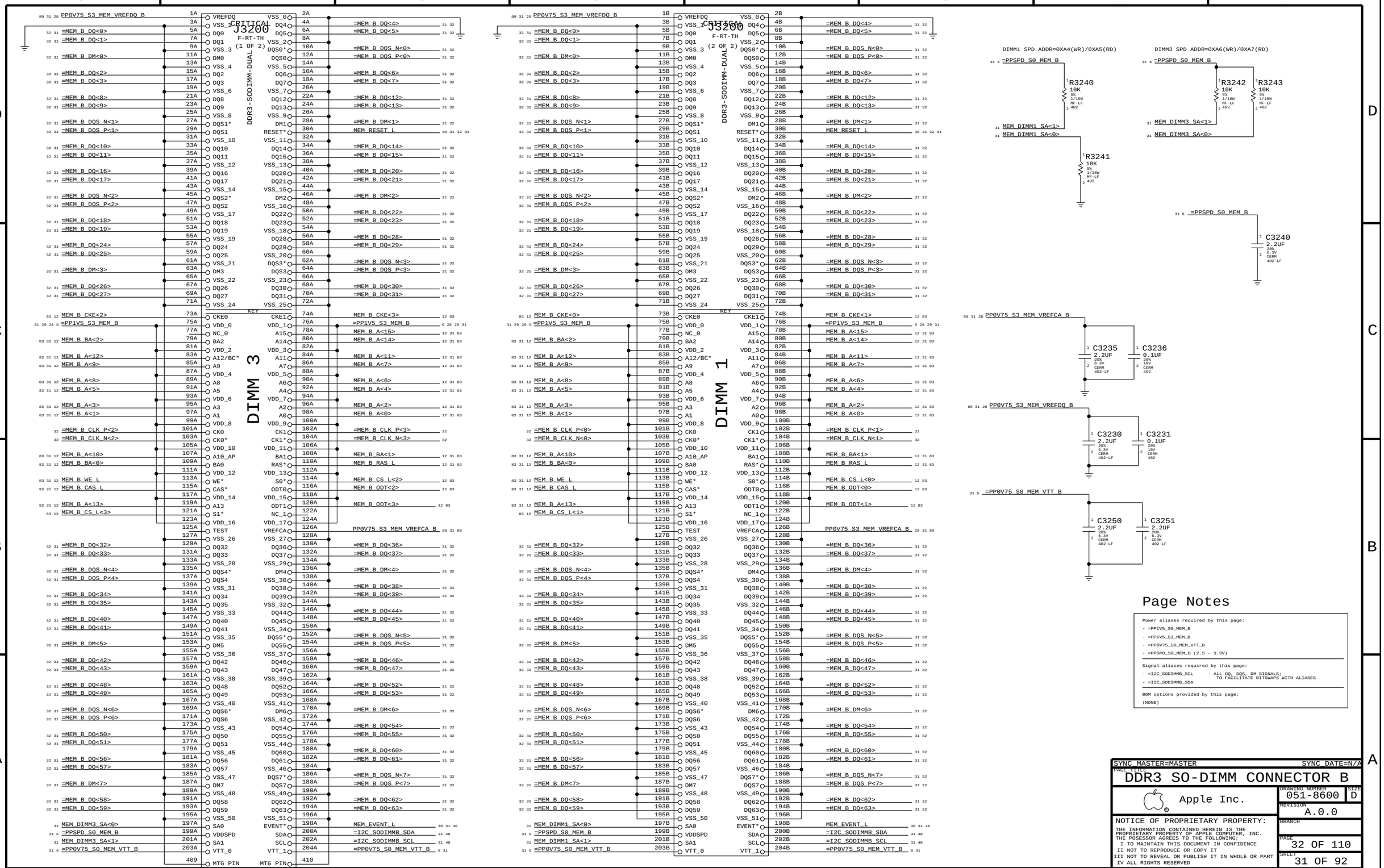
Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC MASTER=MASTER	SYNC DATE=N/A
PAGE TITLE: DDR3 SO-DIMMs 0 & 2	
Apple Inc.	DRAWING NUMBER 051-8600 / SIZE D
	REVISION A.0.0
NOTICE OF PROPRIETARY PROPERTY:	BRANCH
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	PAGE 31 OF 110
	SHEET 30 OF 92



Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

- ALL DQ, DQS, DM SIGNALS: TO FACILITATE BITSWAPS WITH ALIASES

BOM options provided by this page:
(NONE)

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B

Apple Inc.

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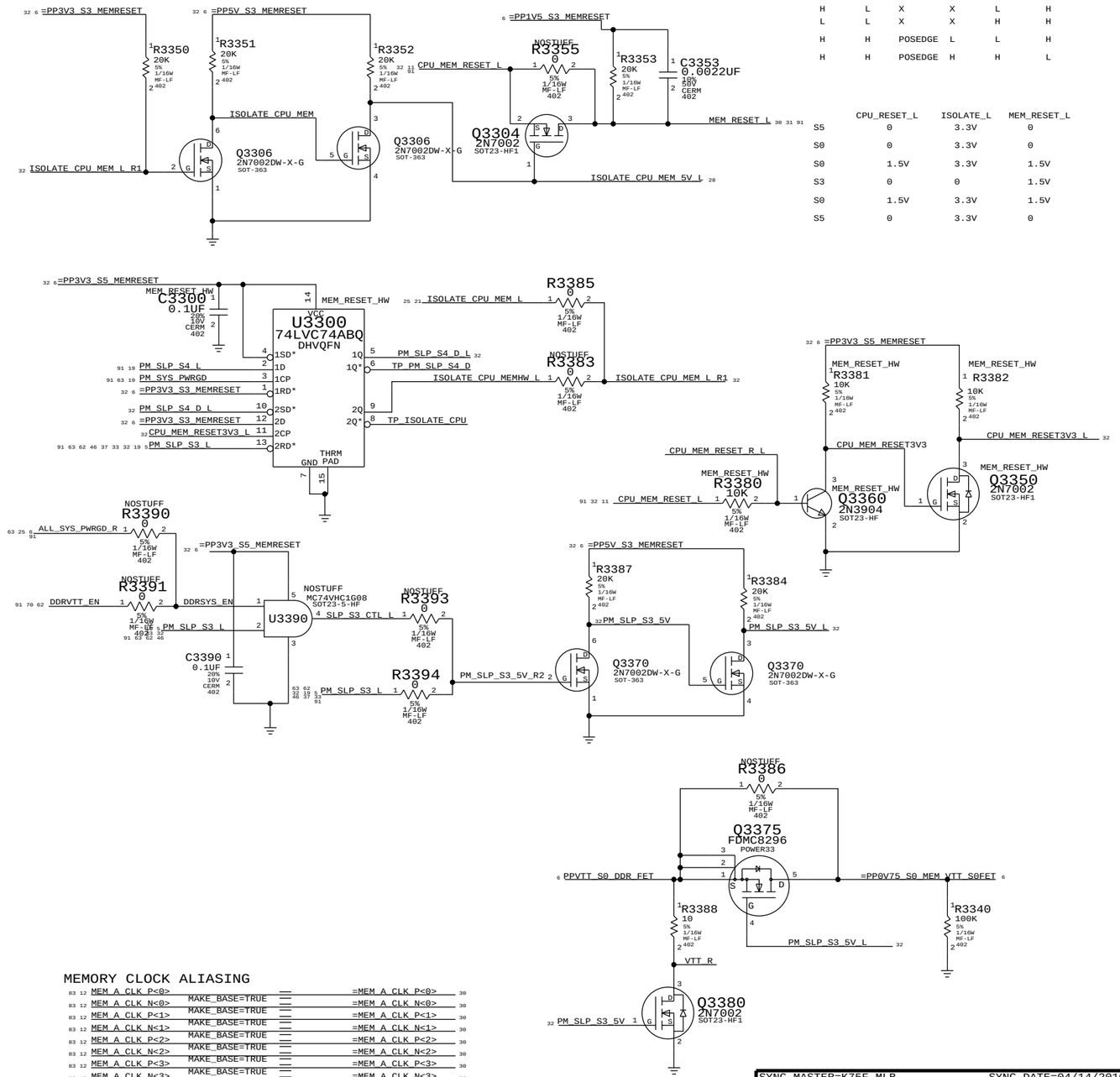
DDR3 RESET Support

LFD CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.

S	R	CLK	D	Q	QB
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	POSEDGE	L	L	H
H	H	POSEDGE	H	H	L

	CPU_RESET_L	ISOLATE_L	MEM_RESET_L
S5	0	3.3V	0
S0	0	3.3V	0
S0	1.5V	3.3V	1.5V
S3	0	0	1.5V
S0	1.5V	3.3V	1.5V
S5	0	3.3V	0



CPU CHANNEL A DQS 0 -> DIMM A DQS 7

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>
MEM_A_DM<0>	MAKE_BASE=TRUE	=MEM_A_DM<7>
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<57>
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<56>
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<58>
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<59>
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<60>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<61>
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<62>
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<63>

CPU CHANNEL A DQS 1 -> DIMM A DQS 6

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>
MEM_A_DM<1>	MAKE_BASE=TRUE	=MEM_A_DM<6>
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<49>
MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<52>
MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<51>
MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<50>
MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<48>
MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<53>
MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<55>
MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<54>

CPU CHANNEL A DQS 2 -> DIMM A DQS 5

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>
MEM_A_DM<2>	MAKE_BASE=TRUE	=MEM_A_DM<5>
MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<40>
MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<45>
MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<46>
MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<47>
MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<41>
MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<44>
MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<43>
MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<42>

CPU CHANNEL A DQS 3 -> DIMM A DQS 4

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>
MEM_A_DM<3>	MAKE_BASE=TRUE	=MEM_A_DM<4>
MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<37>
MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<33>
MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<35>
MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<34>
MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<36>
MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<32>
MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<38>
MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<39>

CPU CHANNEL A DQS 4 -> DIMM A DQS 3

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>
MEM_A_DM<4>	MAKE_BASE=TRUE	=MEM_A_DM<3>
MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<28>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<29>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<27>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<31>
MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<25>
MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<24>
MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<26>
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<30>

CPU CHANNEL A DQS 5 -> DIMM A DQS 2

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>
MEM_A_DM<5>	MAKE_BASE=TRUE	=MEM_A_DM<2>
MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<17>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<16>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<22>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<23>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<21>
MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<20>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<18>
MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<19>

CPU CHANNEL A DQS 6 -> DIMM A DQS 1

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>
MEM_A_DM<6>	MAKE_BASE=TRUE	=MEM_A_DM<1>
MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<12>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<13>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<10>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<15>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<8>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<9>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<11>
MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<14>

CPU CHANNEL A DQS 7 -> DIMM A DQS 0

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>
MEM_A_DM<7>	MAKE_BASE=TRUE	=MEM_A_DM<0>
MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<5>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<4>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<3>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<2>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<1>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<0>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<7>
MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<6>

CPU CHANNEL B DQS 0 -> DIMM B DQS 7

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>
MEM_B_DM<0>	MAKE_BASE=TRUE	=MEM_B_DM<7>
MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<61>
MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<60>
MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<62>
MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<63>
MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<56>
MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<57>
MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<58>
MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<59>

CPU CHANNEL B DQS 1 -> DIMM B DQS 6

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>
MEM_B_DM<1>	MAKE_BASE=TRUE	=MEM_B_DM<6>
MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<51>
MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<54>
MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<53>
MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<52>
MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<48>
MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<49>
MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<50>
MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<55>

CPU CHANNEL B DQS 2 -> DIMM B DQS 5

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>
MEM_B_DM<2>	MAKE_BASE=TRUE	=MEM_B_DM<5>
MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<45>
MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<40>
MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<42>
MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<47>
MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<44>
MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<41>
MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<46>
MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<43>

CPU CHANNEL B DQS 3 -> DIMM B DQS 4

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>
MEM_B_DM<3>	MAKE_BASE=TRUE	=MEM_B_DM<4>
MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<32>
MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<39>
MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<37>
MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<38>
MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<35>
MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<34>
MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<36>
MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<33>

CPU CHANNEL B DQS 4 -> DIMM B DQS 3

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>
MEM_B_DM<4>	MAKE_BASE=TRUE	=MEM_B_DM<3>
MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<28>
MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<24>
MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<31>
MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<30>
MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<29>
MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<25>
MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<27>
MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<26>

CPU CHANNEL B DQS 5 -> DIMM B DQS 2

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>
MEM_B_DM<5>	MAKE_BASE=TRUE	=MEM_B_DM<2>
MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<18>
MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<20>
MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<23>
MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<22>
MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<19>
MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<21>
MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<17>
MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<16>

CPU CHANNEL B DQS 6 -> DIMM B DQS 1

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>
MEM_B_DM<6>	MAKE_BASE=TRUE	=MEM_B_DM<1>
MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<8>
MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<14>
MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<10>
MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<11>
MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<9>
MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<15>
MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<12>
MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<13>

CPU CHANNEL B DQS 7 -> DIMM B DQS 0

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>
MEM_B_DM<7>	MAKE_BASE=TRUE	=MEM_B_DM<0>
MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<2>
MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<1>
MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<3>
MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<7>
MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<4>
MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<5>
MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<6>
MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<0>

MEMORY CLOCK ALIASING

MEM_A_CLK_P<0>	MAKE_BASE=TRUE	=MEM_A_CLK_P<0>
MEM_A_CLK_N<0>	MAKE_BASE=TRUE	=MEM_A_CLK_N<0>
MEM_A_CLK_P<1>	MAKE_BASE=TRUE	=MEM_A_CLK_P<1>
MEM_A_CLK_N<1>	MAKE_BASE=TRUE	=MEM_A_CLK_N<1>
MEM_A_CLK_P<2>	MAKE_BASE=TRUE	=MEM_A_CLK_P<2>
MEM_A_CLK_N<2>	MAKE_BASE=TRUE	=MEM_A_CLK_N<2>
MEM_A_CLK_P<3>	MAKE_BASE=TRUE	=MEM_A_CLK_P<3>
MEM_A_CLK_N<3>	MAKE_BASE=TRUE	=MEM_A_CLK_N<3>
MEM_B_CLK_P<0>	MAKE_BASE=TRUE	=MEM_B_CLK_P<0>
MEM_B_CLK_N<0>	MAKE_BASE=TRUE	=MEM_B_CLK_N<0>
MEM_B_CLK_P<1>	MAKE_BASE=TRUE	=MEM_B_CLK_P<1>
MEM_B_CLK_N<1>	MAKE_BASE=TRUE	=MEM_B_CLK_N<1>
MEM_B_CLK_P<2>	MAKE_BASE=TRUE	=MEM_B_CLK_P<2>
MEM_B_CLK_N<2>	MAKE_BASE=TRUE	=MEM_B_CLK_N<2>
MEM_B_CLK_P<3>	MAKE_BASE=TRUE	=MEM_B_CLK_P<3>
MEM_B_CLK_N<3>	MAKE_BASE=TRUE	=MEM_B_CLK_N<3>

SYNC MASTER=K75F_MLB SYNC DATE=04/14/2010

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DDR3 SUPPORT AND BITSWAPS

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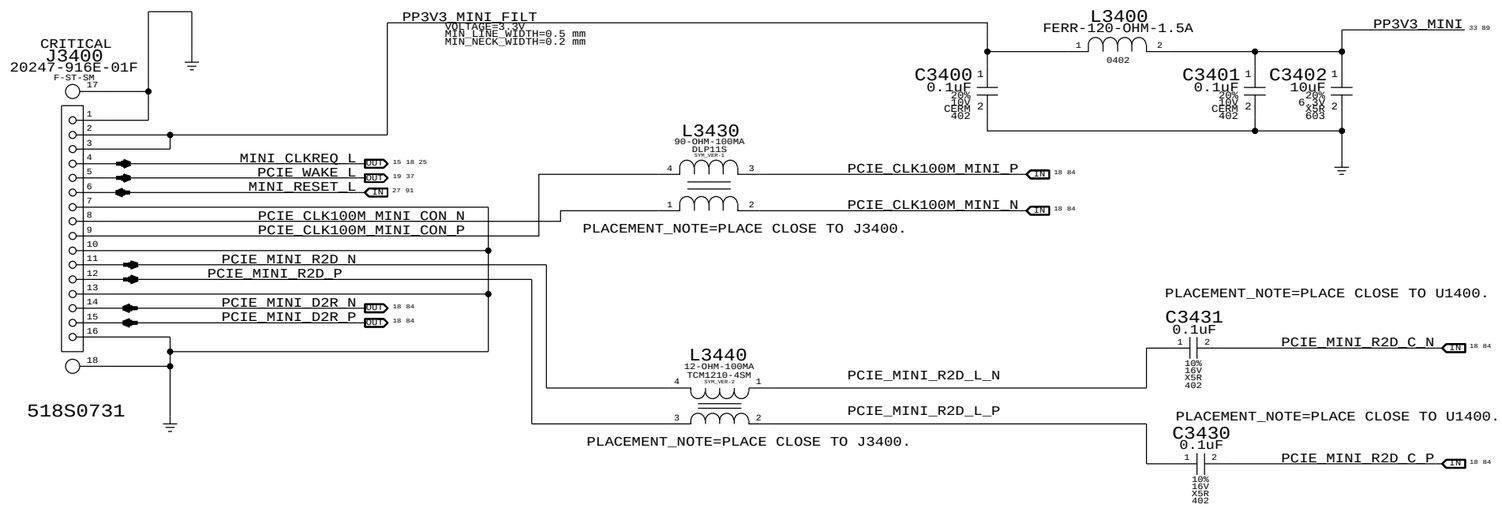
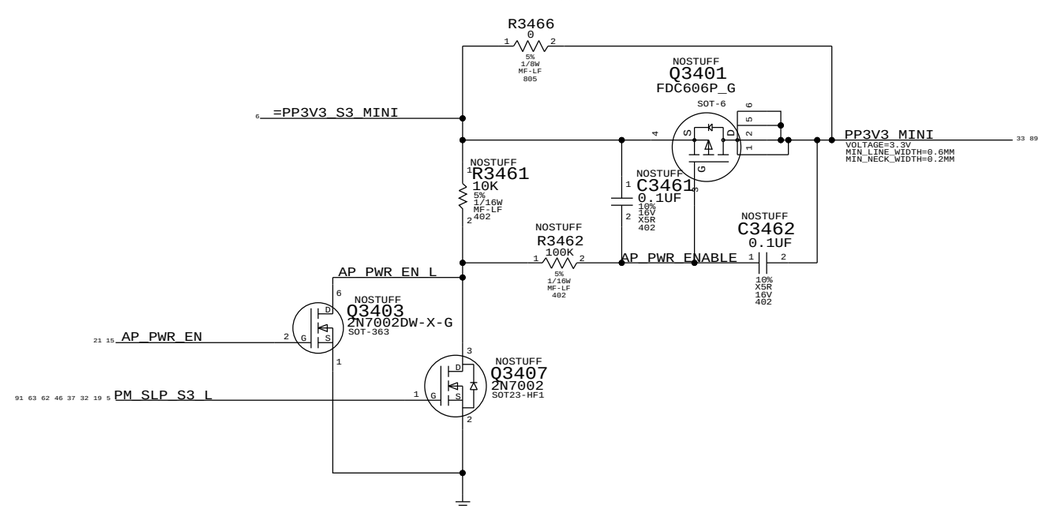


AP POWER ENABLE CIRCUIT

AP_PWR_ON = S0 || (S3 && AP_EN)



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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PCI-E Wireless Connector

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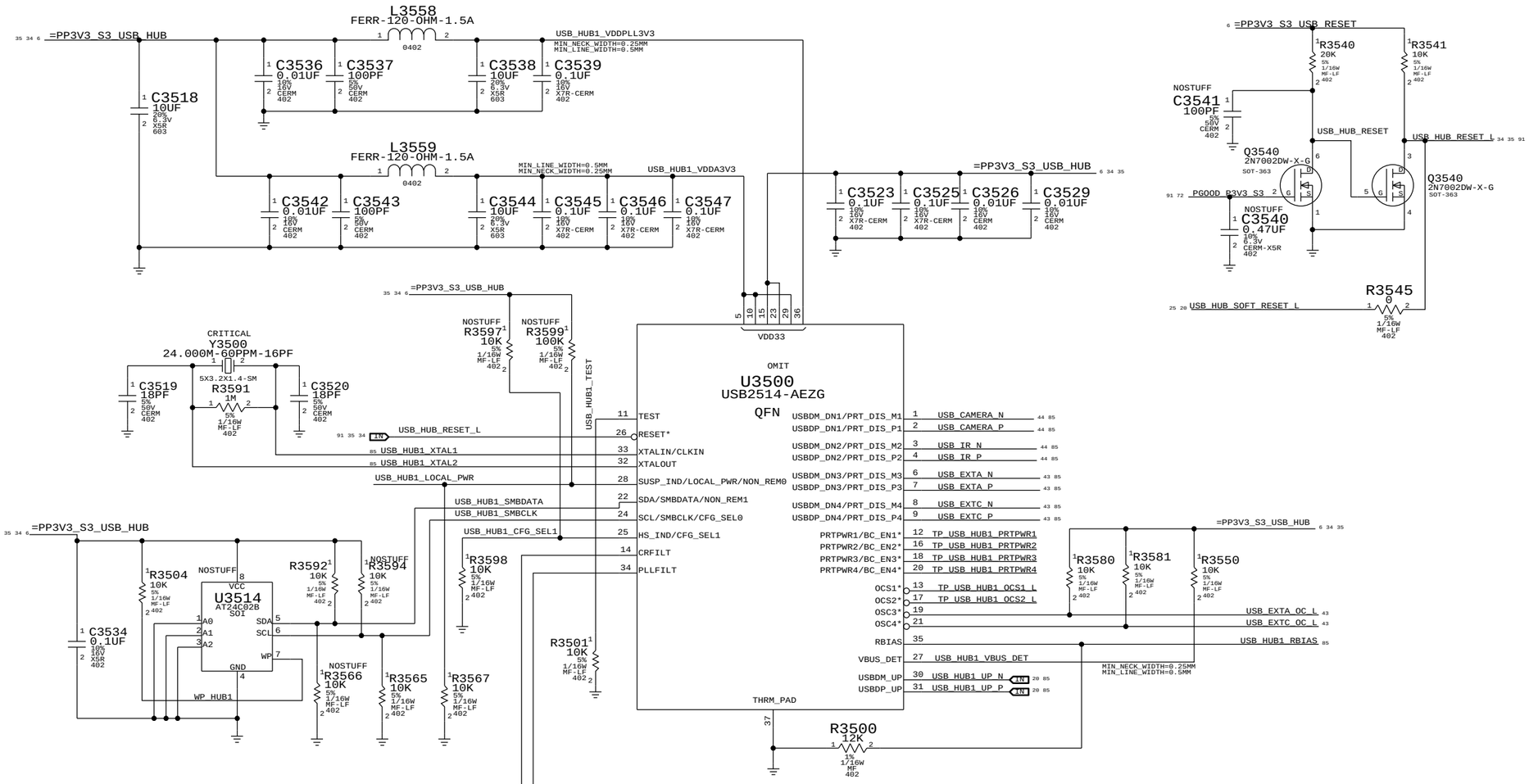
USB HUB-1



	SEL1	SEL0	DESCRIPTION
DEFAULT K23F ==>	0	0	Internal Default with Self powered Operation
	0	1	SMBUS Slave Config
	1	0	Internal Default with Bus powered Operation
	1	1	EEPROM Supported

	NON_REM1	NON_REM0	DESCRIPTION
	0	0	All ports are Non removable
	0	1	Port1 is non removable
DEFAULT K23F ==>	1	0	Port 1 and 2 are non removable
	1	1	Port1,2 and 3 are non Removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0721	2	SMSC USX2061-AEZG	U3500,U3600	CRITICAL	

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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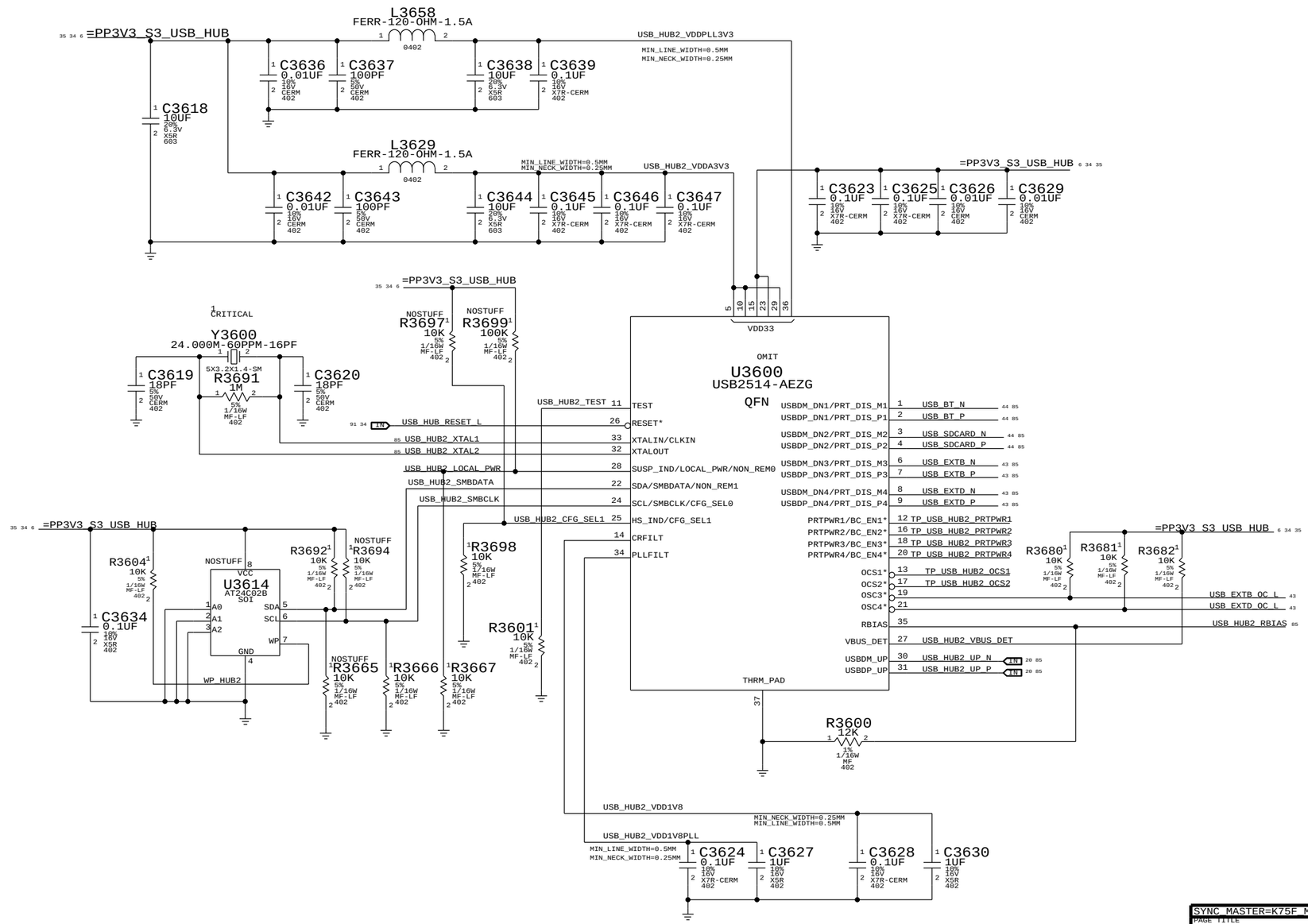
USB HUB-2



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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USB HUB 2

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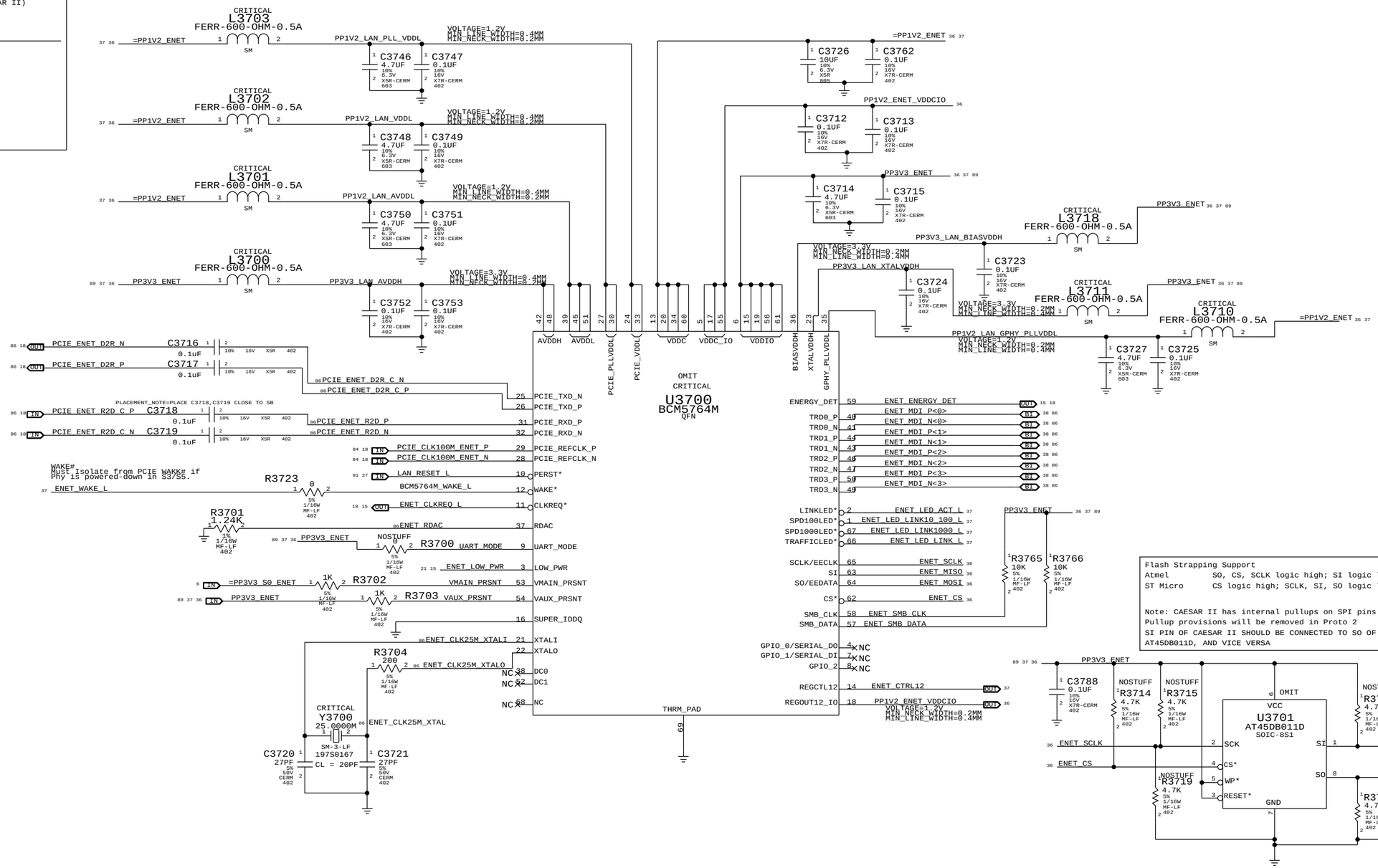
Page Notes

Power aliases required by this page:
- PP3V3_ENET (CAESAR II)
- =PP1V2_ENET



SYNC MASTER=K75F MLB SYNC DATE=04/14/2010

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ETHERNET (CAESAR II)

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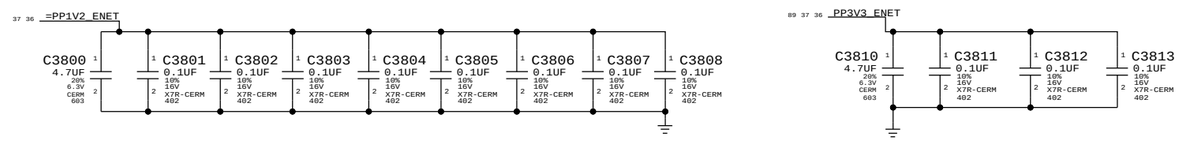
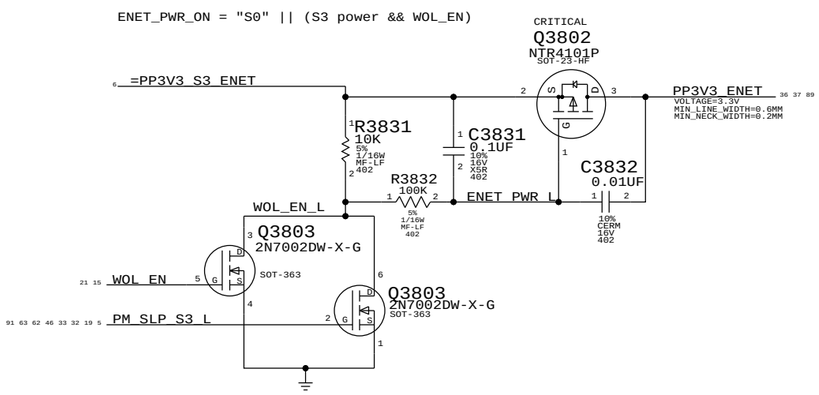
CAESAR II DECOUPLING

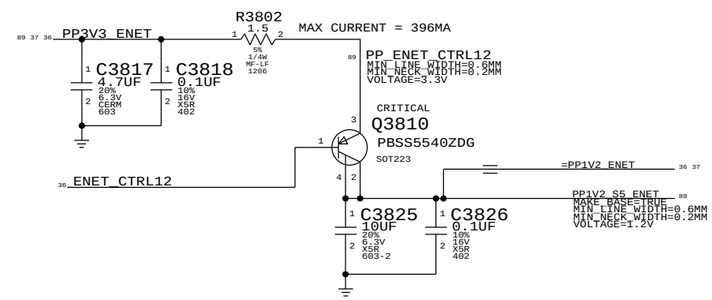


ENET POWER ENABLE CIRCUIT

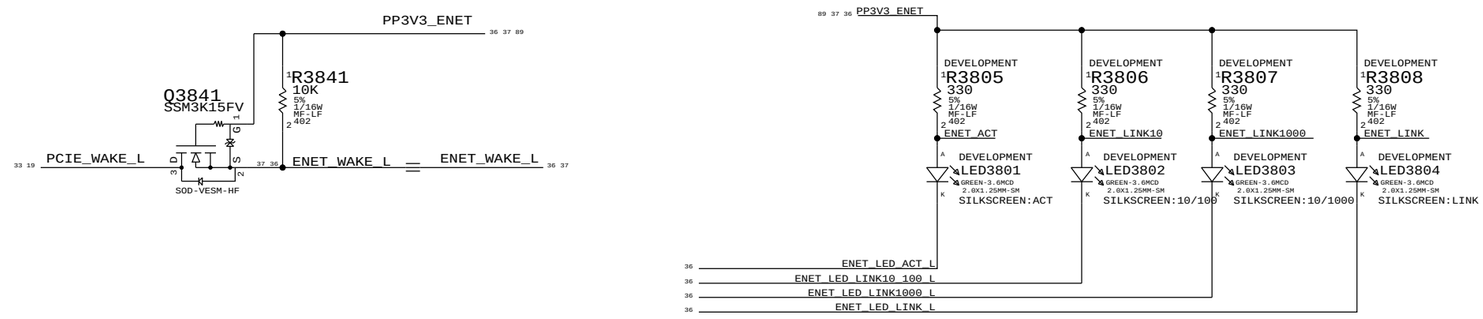
ENET_PWR_ON = "S0" || (S3 power && WOL_EN)



CAESAR II 1V2 RAIL SUPPLY



CAESAR II LED SUPPORT



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CAESAR II SUPPORT

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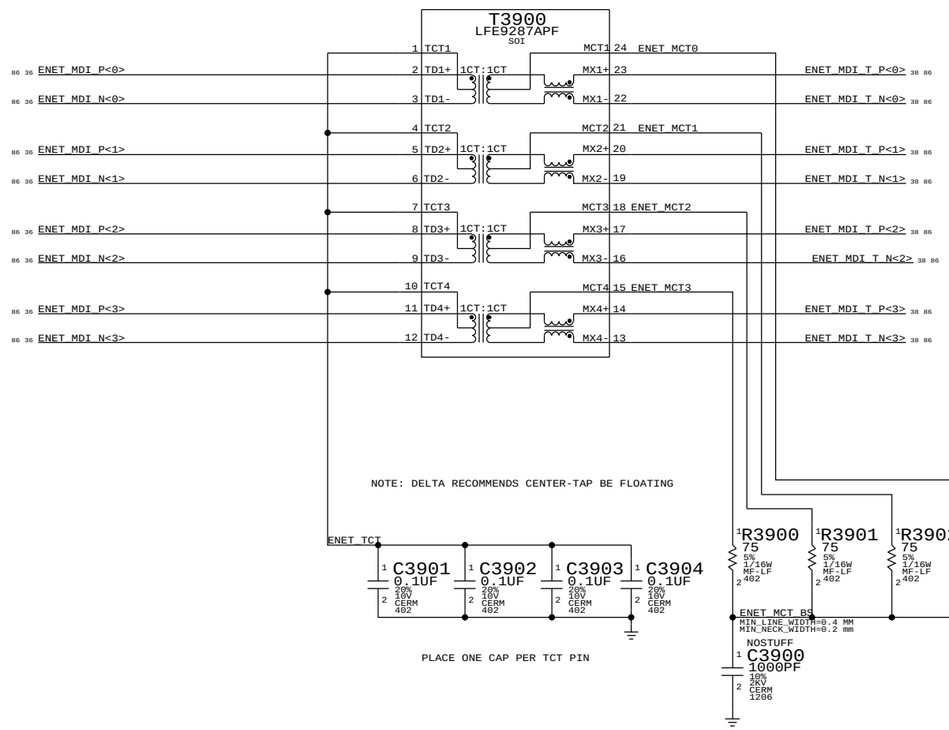

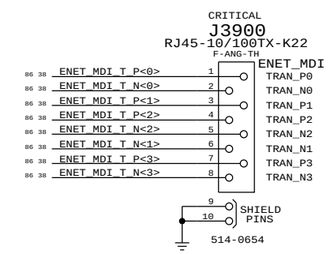

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
ETHERNET CONNECTOR

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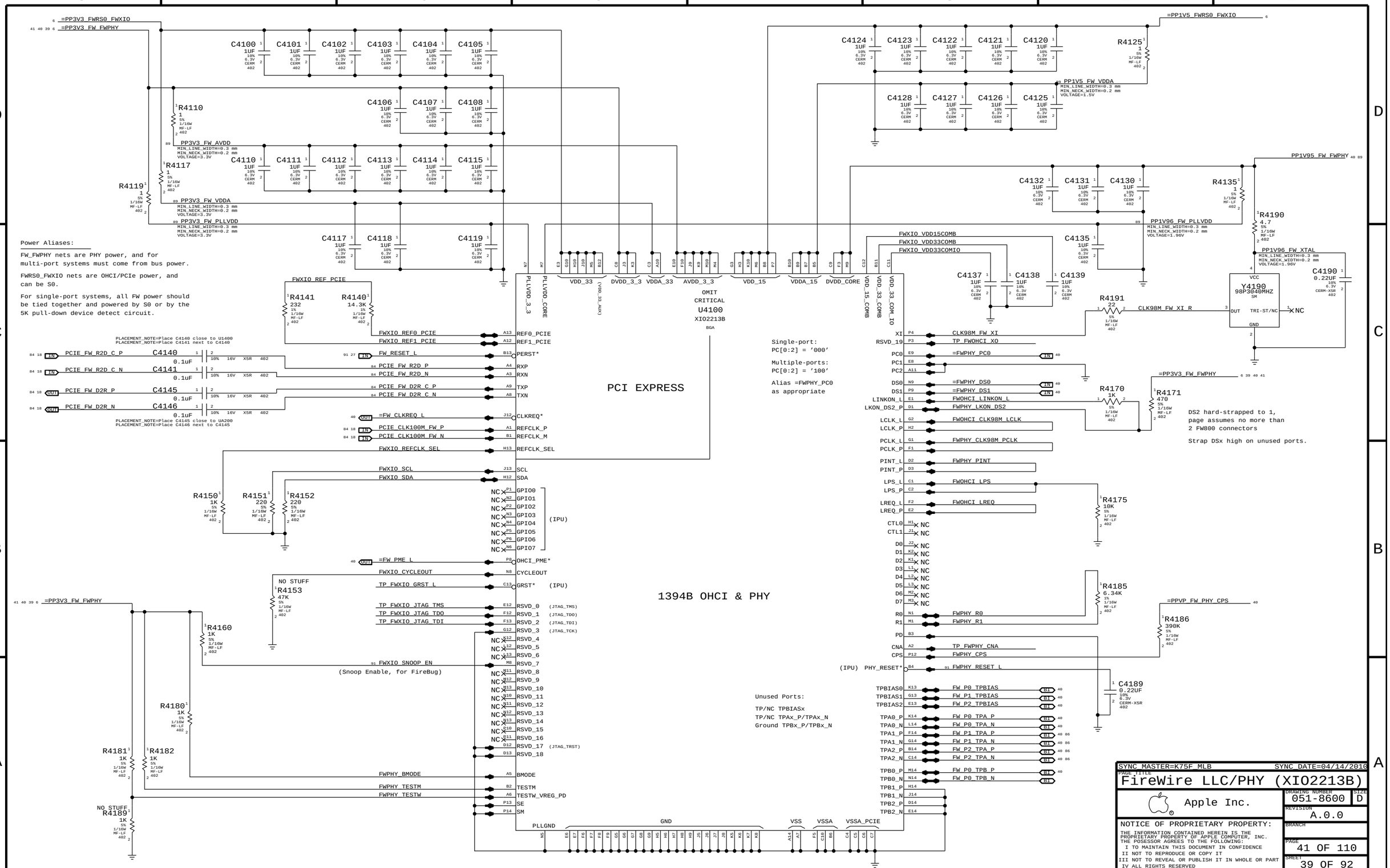
=PP3V3_FWRS0_FWXIO
=PP3V3_FW_FWPHY
=PP1V5_FWRS0_FWXIO
PP1V5_FW_VDDA
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
PP3V3_FW_AVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
PP3V3_FW_VDDA
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
PP3V3_FW_PLLVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
PP1V95_FW_FWPHY
PP1V96_FW_PLLVDD
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.96V
PP1V96_FW_XTAL
MIN_LINE_WIDTH=0.3 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.96V
Power Aliases:
FW_FWPHY nets are PHY power, and for multi-port systems must come from bus power.
FWRS0_FWXIO nets are OHCI/PCIe power, and can be S0.
For single-port systems, all FW power should be tied together and powered by S0 or by the 5K pull-down device detect circuit.
FWXIO_REF_PCIE
PLACEMENT_NOTE=Place C4140 close to U1400
PLACEMENT_NOTE=Place C4141 next to C4140
PLACEMENT_NOTE=Place C4145 close to UA200
PLACEMENT_NOTE=Place C4146 next to C4145
PCIE_FW_R2D_C_P
PCIE_FW_R2D_C_N
PCIE_FW_D2R_P
PCIE_FW_D2R_N
FW_RESET_L
PCIE_FW_R2D_P
PCIE_FW_R2D_N
PCIE_FW_D2R_C_P
PCIE_FW_D2R_C_N
=FW_CLKREQ_L
PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N
FWXIO_REFCLK_SEL
FWXIO_SCL
FWXIO_SDA
=FW_PME_L
FWXIO_CYCLEOUT
TP_FWXIO_GRST_L
TP_FWXIO_JTAG_TMS
TP_FWXIO_JTAG_TDO
TP_FWXIO_JTAG_TDI
FWXIO_SNOOP_EN
(Snoop Enable, for FireBug)
FWPHY_BMODE
FWPHY_TESTM
FWPHY_TESTW
PCI EXPRESS
1394B OHCI & PHY
OMIT CRITICAL
U4100
XIO2213B
BGA
Single-port:
PC[0:2] = '000'
Multiple-ports:
PC[0:2] = '100'
Alias =FWPHY_PC0 as appropriate
Unused Ports:
TP/NC TPBIASx
TP/NC TPAx_P/TPAx_N
Ground TPBx_P/TPBx_N
DS2 hard-strapped to 1, page assumes no more than 2 FW800 connectors
Strap DSx high on unused ports.
CLK98M_FW_XI_R
Y4190
98P3040MHZ
SM
=PPVP_FW_PHY_CPS
NO STUFF
SYNC_MASTER=K75F_MLB
SYNC_DATE=04/14/2010
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FireWire LLC/PHY (XIO2213B)
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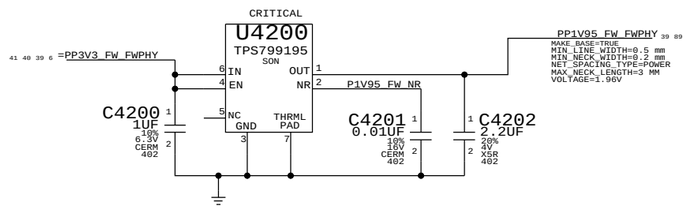
1394 PHY 1.95V SUPPLY



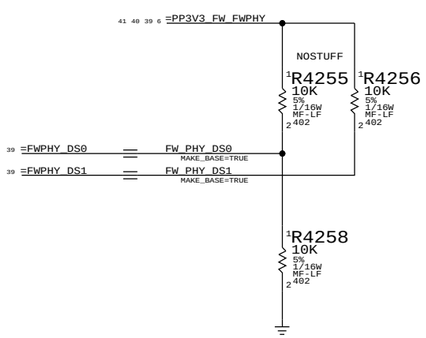
FireWire Aliases For Connectivity

=FW_CLKREQ_L — FW_CLKREQ_L (MAKE_BASE=TRUE)

=FW_PME_L — FW_PME_L (MAKE_BASE=TRUE)

=PPVP_FW_PHY_CPS — PPVP_FW_PHY_CPS (MAKE_BASE=TRUE)

1394 PHY STRAPPING OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE.

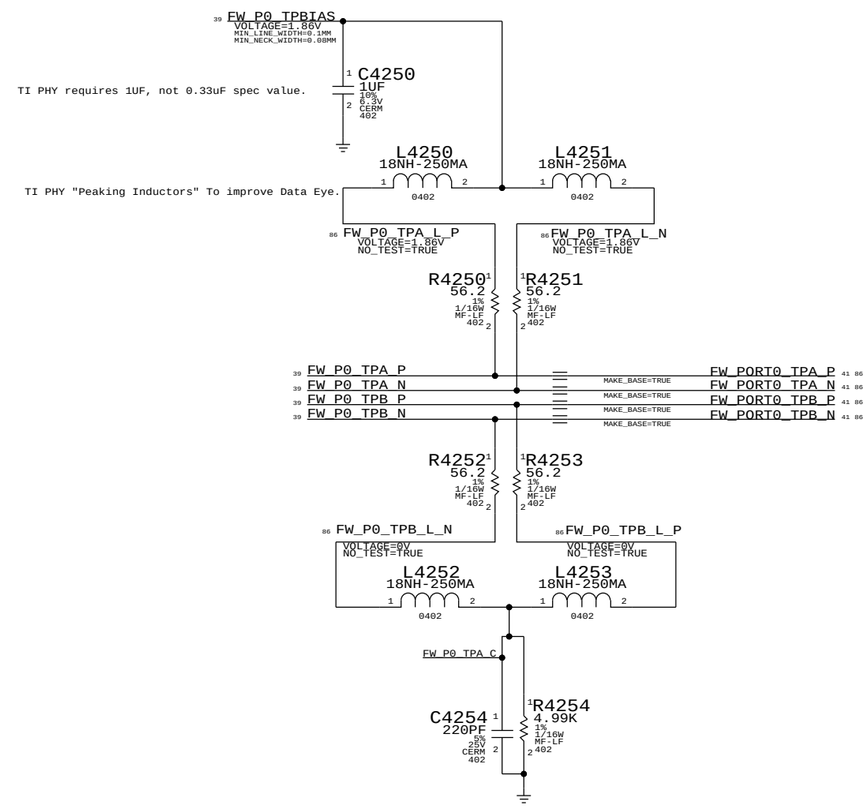
=FWPHY_PC0 — FW_PHY_PC0 (MAKE_BASE=TRUE)

R4257 10K 5% 1/16W MF-LF 402

iMacs are now one port only and have Power Code "000"

Termination

Place close to FireWire PHY



2ND & 3RD TPA/TPB PAIR UNUSED

FW_P1_TPBIAS — NC_FW_PORT1_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P1_TPA_P — NC_FW_PORT1_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P1_TPA_N — NC_FW_PORT1_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPBIAS — NC_FW_PORT2_TPBIAS (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPA_P — NC_FW_PORT2_TPA_P (MAKE_BASE=TRUE, NO_TEST=TRUE)

FW_P2_TPA_N — NC_FW_PORT2_TPA_N (MAKE_BASE=TRUE, NO_TEST=TRUE)

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: FW: 1394B MISC

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

BRANCH:

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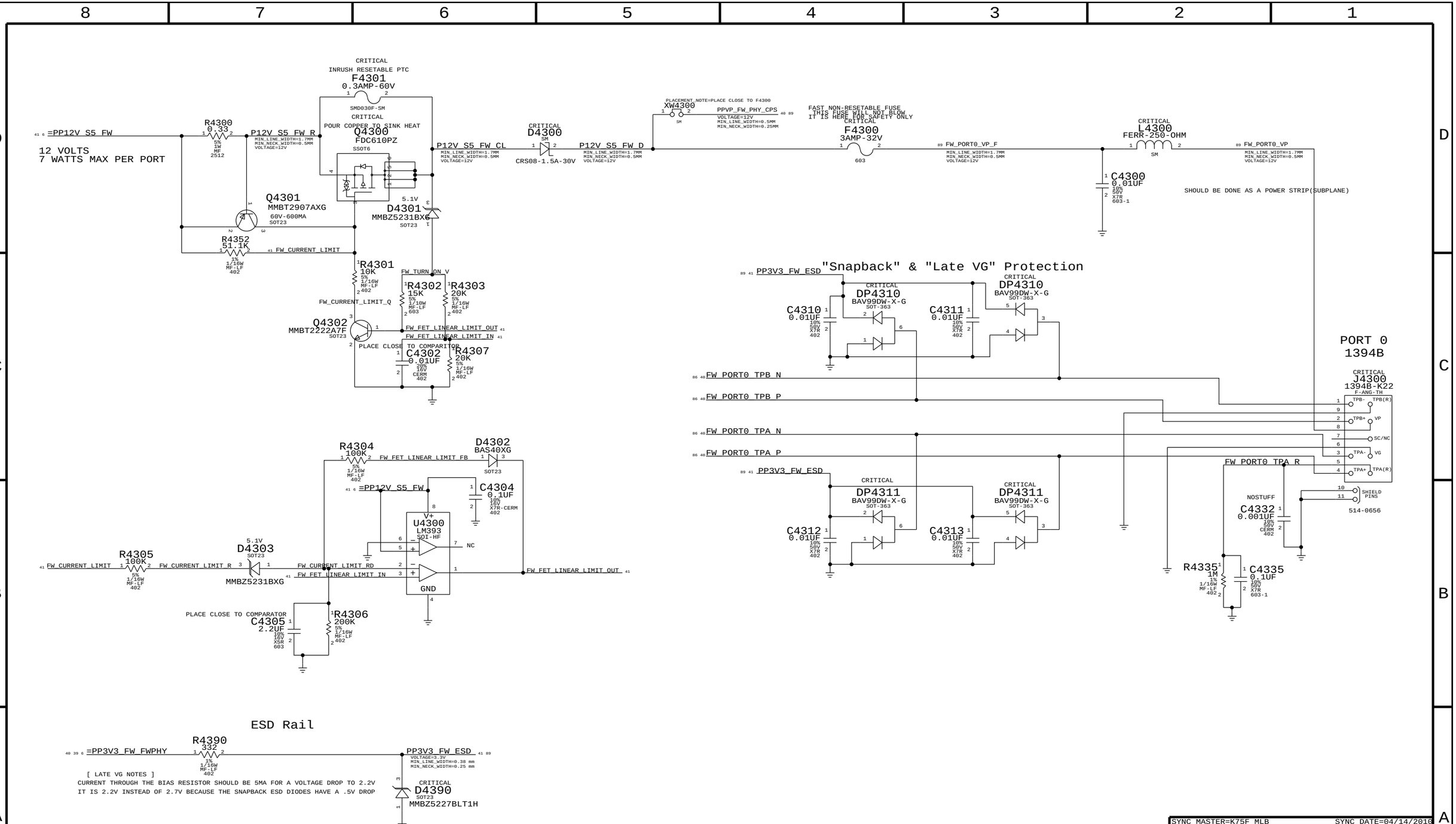

SYNC MASTER=K75F_MLB SYNC DATE=04/14/2010

PAGE TITLE
FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

BRANCH

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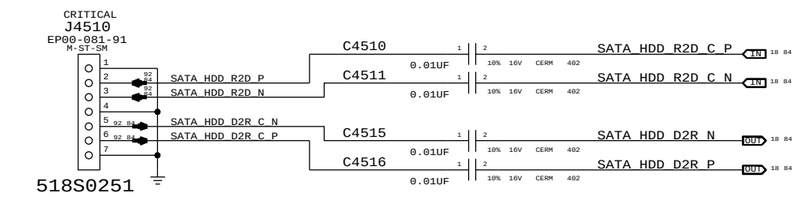
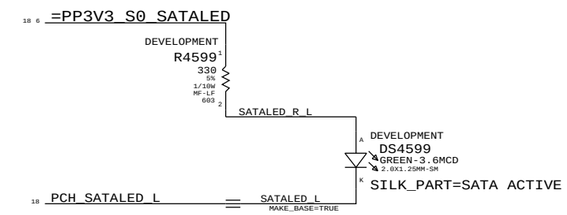
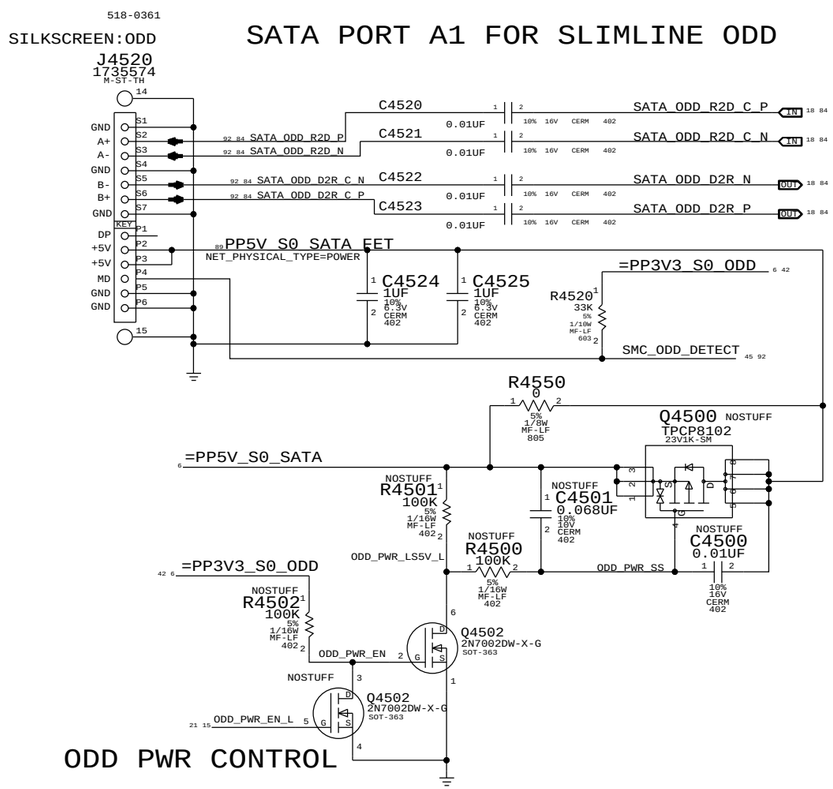
SATA PORT A0 FOR HDD



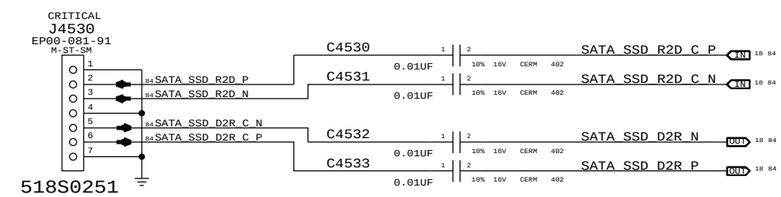
SATA Activity LED



SATA PORT A1 FOR SLIMLINE ODD



SATA PORT A2 FOR SSD



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
SATA Connectors

Apple Inc.

DRAWING NUMBER	051-8600
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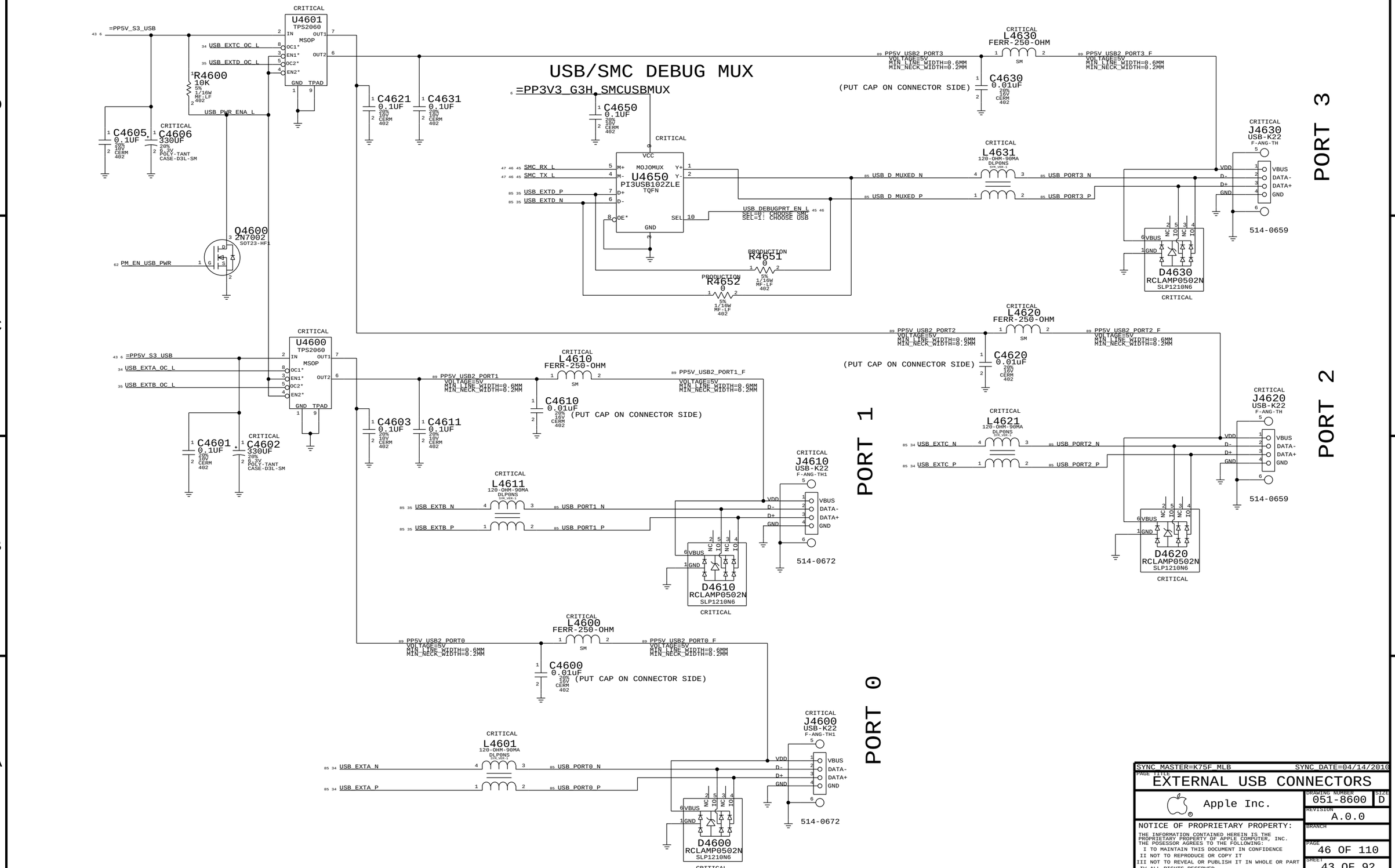
USB/SMC DEBUG MUX
=PP3V3_G3H_SMCUSBMUX
PORT 3
PORT 2
PORT 1
PORT 0
U4601 TPS2060 MSOP
U4600 TPS2060 MSOP
U4650 PI3USB102ZLE TQFN
MOJOMUX
Q4600 2N7002 SOT23-HF1
R4600 10K
R4651 0
R4652 0
C4605 0.1UF
C4606 330UF
C4621 0.1UF
C4631 0.1UF
C4650 0.1UF
C4630 0.01UF
C4601 0.1UF
C4602 330UF
C4603 0.1UF
C4611 0.1UF
C4610 0.01UF
C4620 0.01UF
C4600 0.01UF
L4630 FERR-250-OHM
L4631 120-OHM-90MA DLP0NS
L4620 FERR-250-OHM
L4621 120-OHM-90MA DLP0NS
L4610 FERR-250-OHM
L4611 120-OHM-90MA DLP0NS
L4600 FERR-250-OHM
L4601 120-OHM-90MA DLP0NS
J4630 USB-K22 F-ANG-TH
J4620 USB-K22 F-ANG-TH
J4610 USB-K22 F-ANG-TH1
J4600 USB-K22 F-ANG-TH1
514-0659
514-0672
D4630 RCLAMP0502N SLP1210N6
D4620 RCLAMP0502N SLP1210N6
D4610 RCLAMP0502N SLP1210N6
D4600 RCLAMP0502N SLP1210N6
(PUT CAP ON CONNECTOR SIDE)
CRITICAL
USB_PWR_ENA_L
PM_EN_USB_PWR
USB_DEBUGPRT_EN_L
SEL=0: CHOOSE SMC
SEL=1: CHOOSE USB
PRODUCTION
SYNC_MASTER=K75F_MLB
SYNC_DATE=04/14/2010
PAGE TITLE
EXTERNAL USB CONNECTORS
Apple Inc.
DRAWING NUMBER
051-8600
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REVISION
A.0.0
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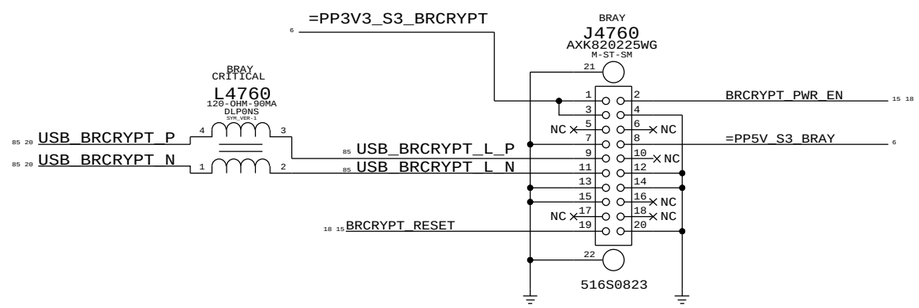
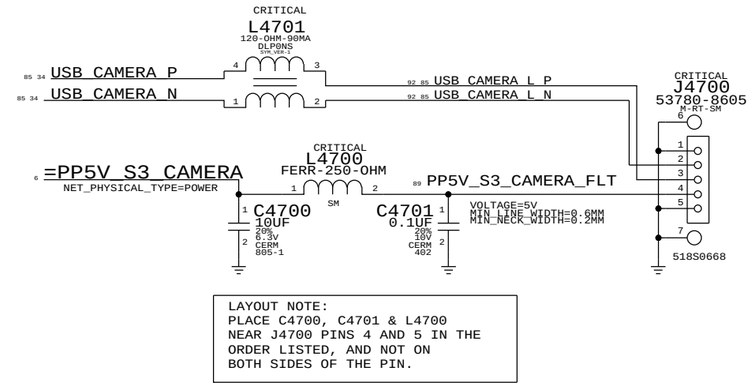
BLURAY DECRYPTOR CONN & FLTR

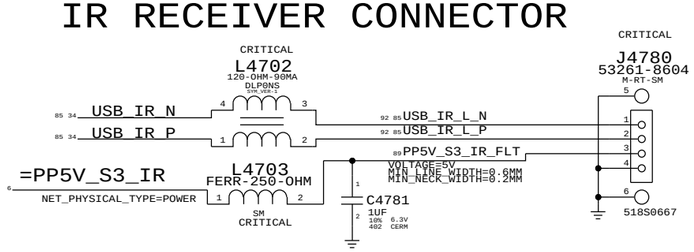


CAMERA CONNECTOR & FILTER

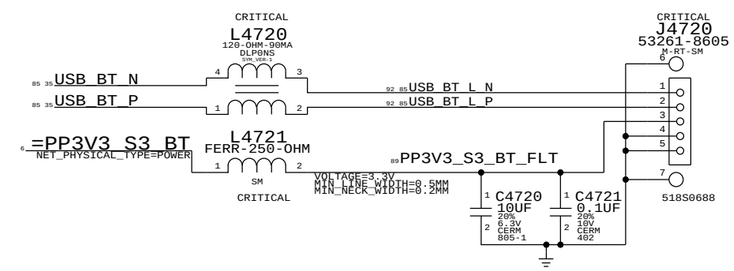


LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

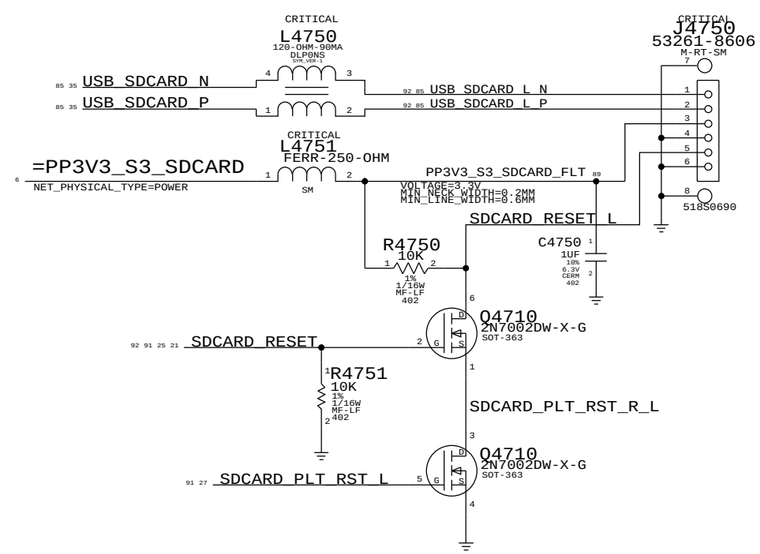
IR RECEIVER CONNECTOR



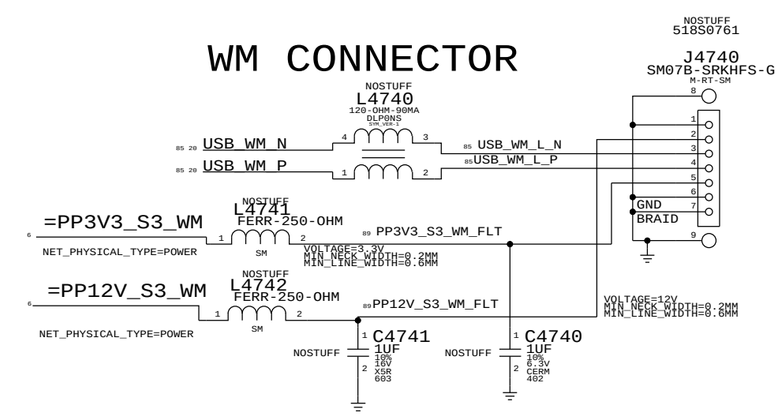
K37L (BLUETOOTH) CONNECTOR



SD Card Reader Board Connector



WM CONNECTOR



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Internal USB Connections

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

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NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

Remove R4950,R4951 after Proto-1

=PP3V3_G3H_SMC — NOSTUFF R4951 10K 5% 1/16W MF-LF 402 — R4950 0 5% 1/16W MF-LF 402 — SMC_PM_G2_EN

U4900 H8S2117 TQFP (1 OF 3) OMIT

Pin	Signal	Dir	Net
112	P10	OUT	SMC_EXCARD_PWR_EN
110	P11	OUT	SMC_RSTGATE_L
109	P12	IN	ALL_SYS_PWRGD_SMC
108	P13	IN	RSMRST_PWRGD
107	P14	NC	
106	P15	OUT	PM_RSMRST_L
105	P16	OUT	CPUIMVP_VR_ON
104	P17	OUT	PM_PWRBTN_L
103	P20	OUT	ESTARLDO_EN
102	P21	IN	SMC_VIDEO_ON
101	P22	IN	AUXCH_P_STATE
100	P23	IN	AUXCH_N_STATE
99	P24	NC	
98	P25	IN	SMC_DP_HPD
97	P26	OUT	BIDIVI_AUDIO_MUX_SEL
96	P27	OUT	DPMUX_VIDEO_IN_SEL
121	P30	BI	LPC_AD<0>
122	P31	BI	LPC_AD<1>
123	P32	BI	LPC_AD<2>
124	P33	BI	LPC_AD<3>
125	P34	IN	LPC_FRAME_L
126	P35	IN	SMC_LRESET_L
127	P36	IN	LPC_CLK33M_SMC
128	P37	BI	LPC_SERIRQ
136	P40	NC	
137	P41		SMC_P41
138	P42	BI (OC)	SMB_MGMT_DATA
2	P43	OUT	SMS_ONOFF_L
3	P44	NC	
4	P45	NC	
5	P46	OUT	SMC_GFX_THROTTLE_L
6	P47	NC	
16	P50	OUT	SMC_TX_L
15	P51	IN	SMC_RX_L
14	P52	BI (OC)	SMB_0_S0_CLK
78	P60		SMC_PM_G2_R
79	P61	NC	
80	P62	NC	
81	P63	NC	
82	P64		SMC_ADAPTER_EN
83	P65	NC	
84	P66		SMC_PROCHOT_3_3_L
85	P67		SMC_BIL_BUTTON_L
68	P70	IN	SMC_CPU_ISENSE
69	P71	IN	SMC_CPU_VSENSE
70	P72	IN	SMC_GPU_ISENSE
71	P73	IN	SMC_GPU_VSENSE
72	P74	IN	SMC_DCIN_ISENSE
73	P75	IN	SMC_PBUS_VSENSE
74	P76	IN	SMC_BATT_ISENSE
75	P77	IN	SMC_NB_MISC_ISENSE
129	P80	OUT	SMC_WAKE_SCI_L
130	P81	NC	
131	P82	OUT	PM_CLKRUN_L
132	P83	IN	LPC_PWRDWN_L
133	P84	OUT	SMC_TX_L
134	P85	IN	SMC_RX_L
135	P86	BI (OC)	SMB_MGMT_CLK
24	P90	IN	SMC_ONOFF_L
23	P91	IN	SMC_BC_ACOK
22	P92	IN	SMC_BS_ALRT_L
21	P93	IN	PM_SLPS3_BUF2_L
20	P94		SMC_P94
19	P95		PM_SLP_S4_S5
18	P96	IN	PM_CLK32K_SUSCLK
17	P97	BI (OC)	SMB_0_S0_DATA

NOTE: P94 and P95 are shorted, P95 could be spare.

NOTE: Rename to BaseArch

U4900 H8S2117 TQFP (2 OF 3) OMIT

Pin	Signal	Dir	Net
41	PA0		SMC_PA0 (DEBUG_SW_1) (DEBUG_SW_2)
40	PA1	OUT	SPI_DESCRIPTOR_OVERRIDE_L (OC)
39	PA2	OUT	PM_SYSRST_L (OC)
38	PA3	OUT	USB_DEBUGPRT_EN_L (OC)
37	PA4	IN	MEM_EVENT_A_L (OC)
35	PA5	IN	MEM_EVENT_B_L (OC)
34	PA6	BI	SYS_ONEWIRE (OC)
33	PA7	OUT	PM_BATLOW_L (OC)
120	PB0	NC	
119	PB1	OUT	SMC_RUNTIME_SCI_L
118	PB2	IN	SMC_ODD_DETECT
117	PB3		SMC_PB3 (See below)
116	PB4	IN	SMC_EXCARD_CP
115	PB5	NC	
114	PB6	IN	SMC_EXCARD_OC_L
113	PB7	IN	SMC_GFX_OVERTEMP_L
94	PC0	OUT	SMC_FAN_0_CTL
93	PC1	OUT	SMC_FAN_1_CTL
92	PC2	OUT	SMC_FAN_2_CTL
91	PC3	OUT	SMC_FAN_3_CTL
90	PC4	IN	SMC_FAN_0_TACH
89	PC5	IN	SMC_FAN_1_TACH
88	PC6	IN	SMC_FAN_2_TACH
87	PC7	IN	SMC_FAN_3_TACH
66	PD0	IN	SMS_X_AXIS
65	PD1	IN	SMS_Y_AXIS
64	PD2	IN	SMS_Z_AXIS
63	PD3	IN	SMC_ANALOG_ID
62	PD4	IN	SMC_NB_CORE_ISENSE
61	PD5	IN	SMC_NB_DDR_ISENSE
60	PD6	IN	ALS_LEFT
59	PD7	IN	ALS_RIGHT
32	PE0	IN	SMC_CASE_OPEN
31	PE1*	IN	SMC_TCK
30	PE2*	IN	SMC_TDI
29	PE3*	OUT	SMC_TDO
28	PE4*	IN	SMC_TMS
50	PF0	IN	G3_POWERON_L
49	PF1	OUT	SMC_SYS_LED
48	PF2	OUT	SMC_LID
47	PF3	OUT	BIDIVI_AUX_TERM_EN
46	PF4	OUT	BIDIVI_PNL_PWR_EN
45	PF5		SMC_PF5
44	PF6	OUT	BIDIVI_BKL_ON
43	PF7	OUT	BIDIVI_BKL_PWM
58	PG0	IN	SMC_PNL_BL_PWM
57	PG1	IN	=SMC_SMS_INT
56	PG2	BI (OC)	SMB_BSA_DATA
55	PG3	BI (OC)	SMB_BSA_CLK
54	PG4	BI (OC)	SMB_A_S3_DATA
53	PG5	BI (OC)	SMB_A_S3_CLK
52	PG6	BI (OC)	SMB_B_S0_DATA
51	PG7	BI (OC)	SMB_B_S0_CLK
10	PH0	OUT	SMC_PROCHOT
12	PH1	OUT	SMC_THRMTRIP
26	PH2		SMC_PH2
140	PH3	OUT	ALS_GAIN
141	PH4	NC	
142	PH5	NC	

SMC_PB3:

SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)

Power

PP3V3_G3H_AVREF_SMC — Peak/Ave/Standby = 2mA/1mA/5uA
=PP3V3_G3H_SMC — Peak/Ave/Sleep/Standby = 40mA/25mA/20mA/50uA

C4902 22UF 20% 6.3V CERM 805 — C4903 0.1UF 20% 10V CERM 402 — C4904 0.1UF 20% 10V CERM 402 — C4905 0.1UF 20% 10V CERM 402 — C4906 0.1UF 20% 10V CERM 402

R4999 4.7 5% 1/16W MF-LF 402 — Peak/Ave/Standby= 2mA/1mA/5uA — PP3V3_G3H_SMC_AVCC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.4V

PLACEMENT_NOTE=Place C4907 close to U4900 pin 13

C4920 0.1UF 20% 10V CERM 402

PLACEMENT_NOTE=Place R4909 close to U4900 pin 76
PLACEMENT_NOTE=Place C4920 close to U4900 pin 76

C4907 0.47UF 10% 6.3V CERM-X5R 402

U4900 H8S2117 TQFP (3 OF 3) OMIT

Pin	Signal	Dir	Net
76	AVCC		
1, 36, 86	VCC		
13	VCL		SMC_VCL
77	AVREF		
8	RES*	IN	SMC_RESET_L
143	XTAL		SMC_XTAL
144	EXTAL		SMC_EXTAL
9	MD1		SMC_MD1
25	MD2		SMC_KBC_MDE
11	NMI	IN	SMC_NMI
27	ETRST*	IN	SMC_TRST_L
67	AVSS		
7, 42, 95, 111, 139	VSS		

R4909 10K 5% 1/16W MF-LF 402 — R4901 10K 5% 1/16W MF-LF 402

XW4900 SM

R4902 10K 5% 1/16W MF-LF 402 — R4998 10K 5% 1/16W MF-LF 402 — R4903 0 5% 1/16W MF-LF 402

GND_SMC_AVSS

=PP3V3_G3H_SMC — NOSTUFF R4952 10K 5% 1/16W MF-LF 402

R4954 0 5% 1/16W MF-LF 402 — PM_SLP_S4_2_L — PM_SLP_S5_L

NOSTUFF R4953 0 5% 1/16W MF-LF 402

R4955 0 5% 1/16W MF-LF 402

REMOVE R4953/4/5 AFTER PROTO-1

NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC MASTER=K75F MLB	SYNC DATE=04/14/2010
PAGE TITLE: SMC	
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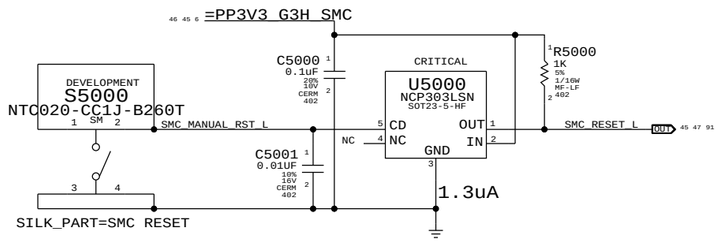
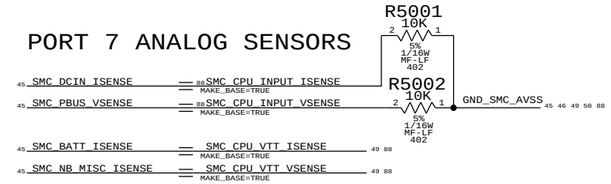
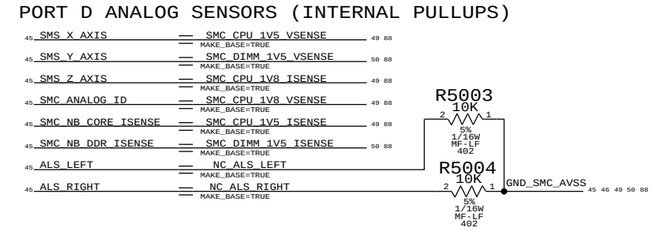
SMC Reset Button / Brownout Detect



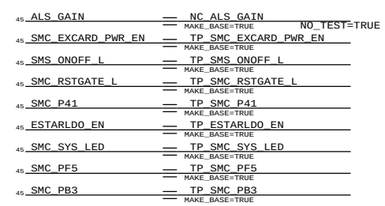
PORT 7 ANALOG SENSORS



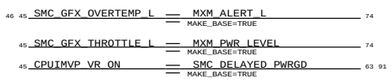
PORT D ANALOG SENSORS (INTERNAL PULLUPS)



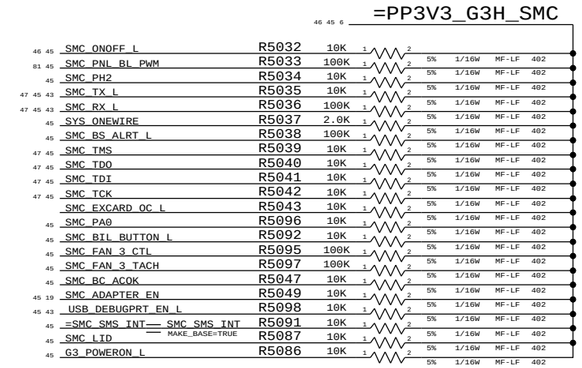
UNUSED TP/NC ALIASES



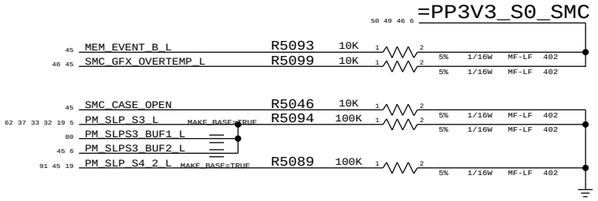
MISC. SIGNAL ALIASES



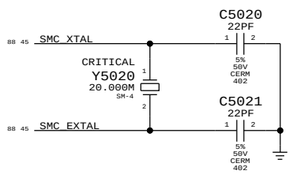
=PP3V3_G3H_SMC



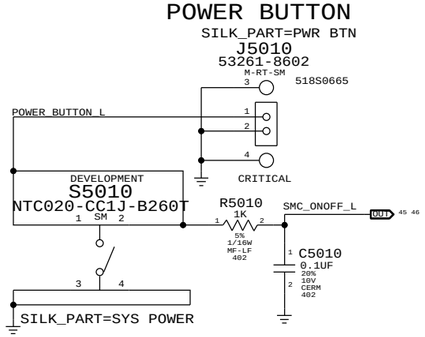
=PP3V3_S0_SMC



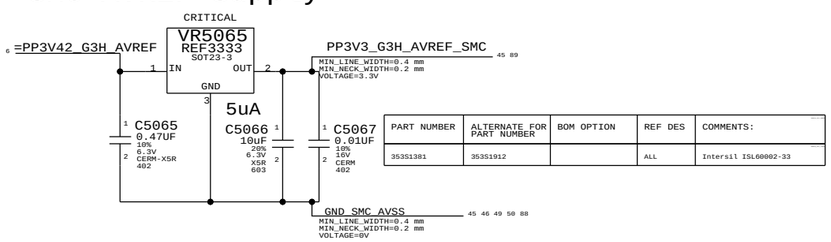
SMC Crystal Circuit



POWER BUTTON

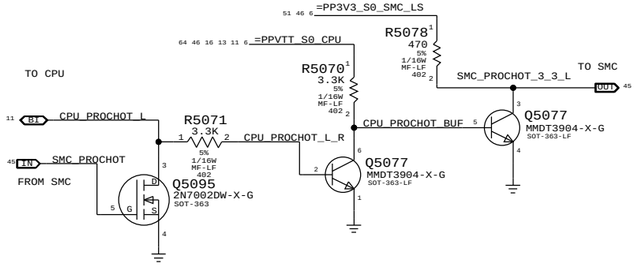


SMC AVREF Supply

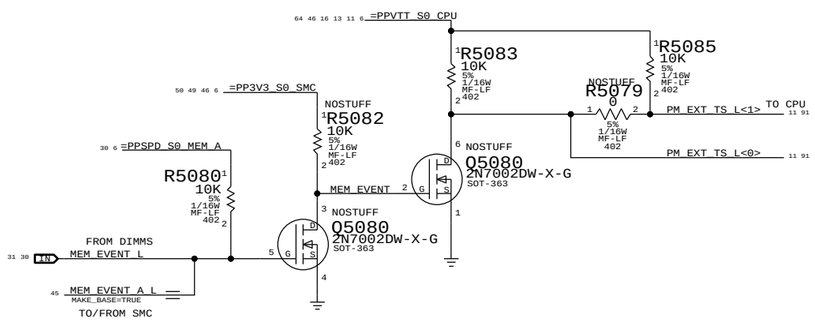


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1912		ALL	Intersil ISL60002-33

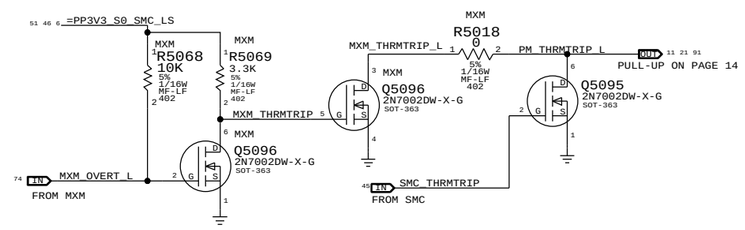
SMC PROCHOT 3.3V LEVEL SHIFTING



PM_EXTTS_L / MEM_EVENT LEVEL SHIFTING

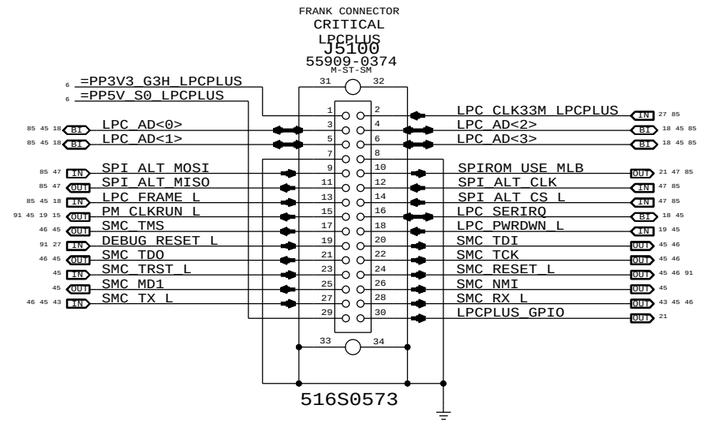


SMC & MXM THERMTRIP LEVEL SHIFTING

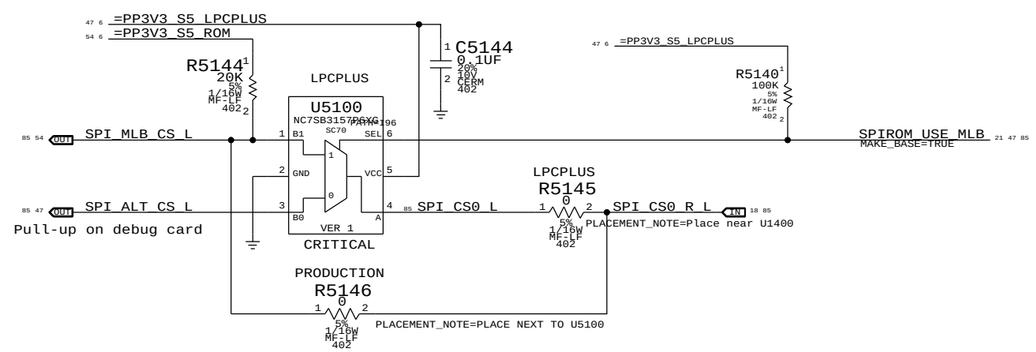


SYNC MASTER=K75F_MLB	SYNC DATE=04/14/2010
PAGE TITLE: SMC Support	
Apple Inc.	DRAWING NUMBER: 051-8600 SIZE: D
	REVISION: A.0.0
	BRANCH
	PAGE: 50 OF 110
	SHEET: 46 OF 92

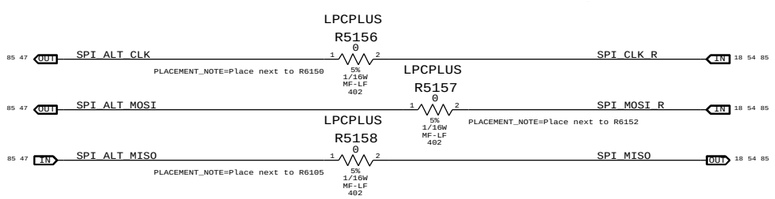
LPC+SPI Connector



Alternate SPI ROM Support



SPI Bus Series Resistance Option



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

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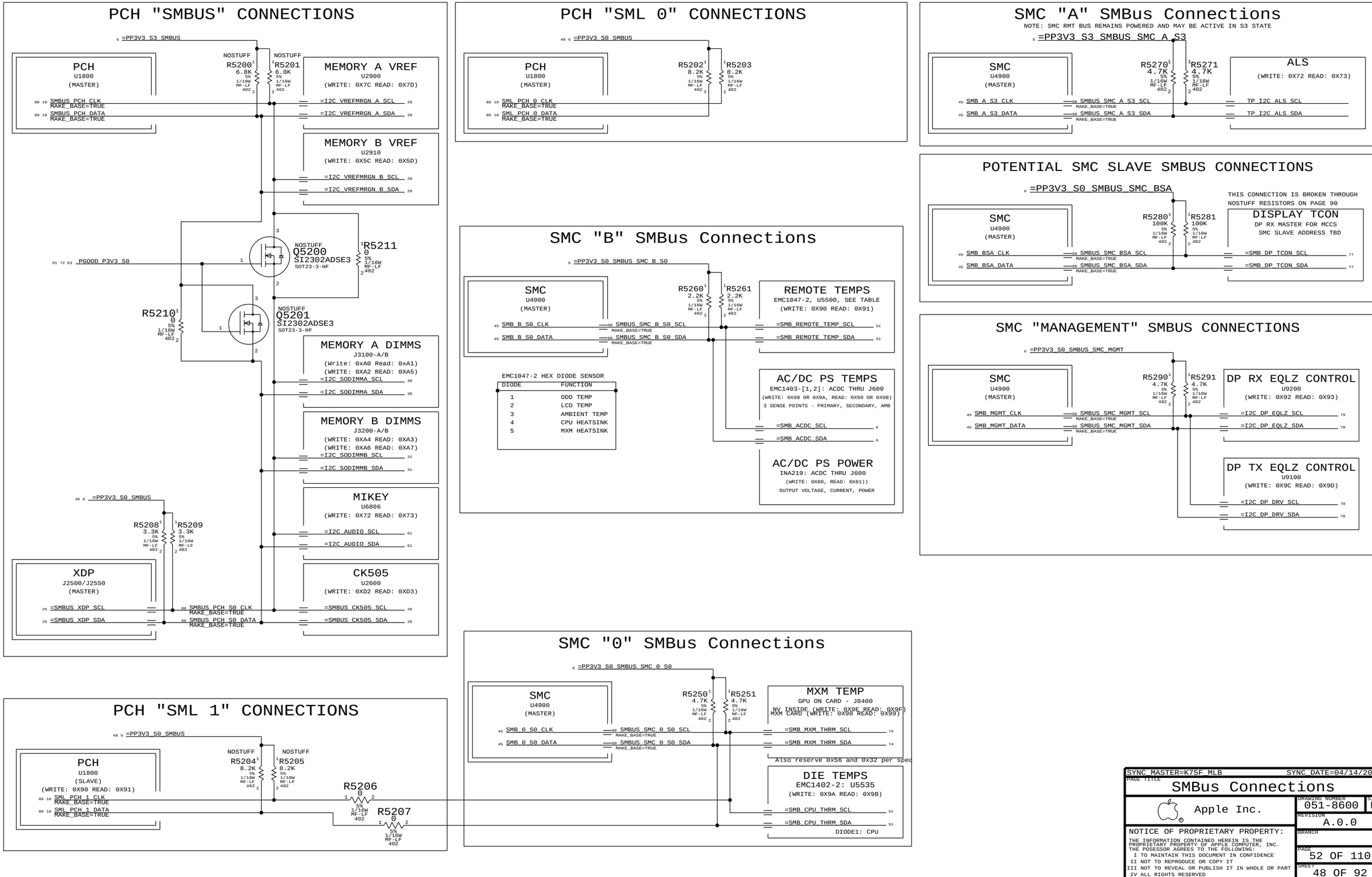
SHEET 47 OF 92



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
SMBus Connections

Apple Inc.

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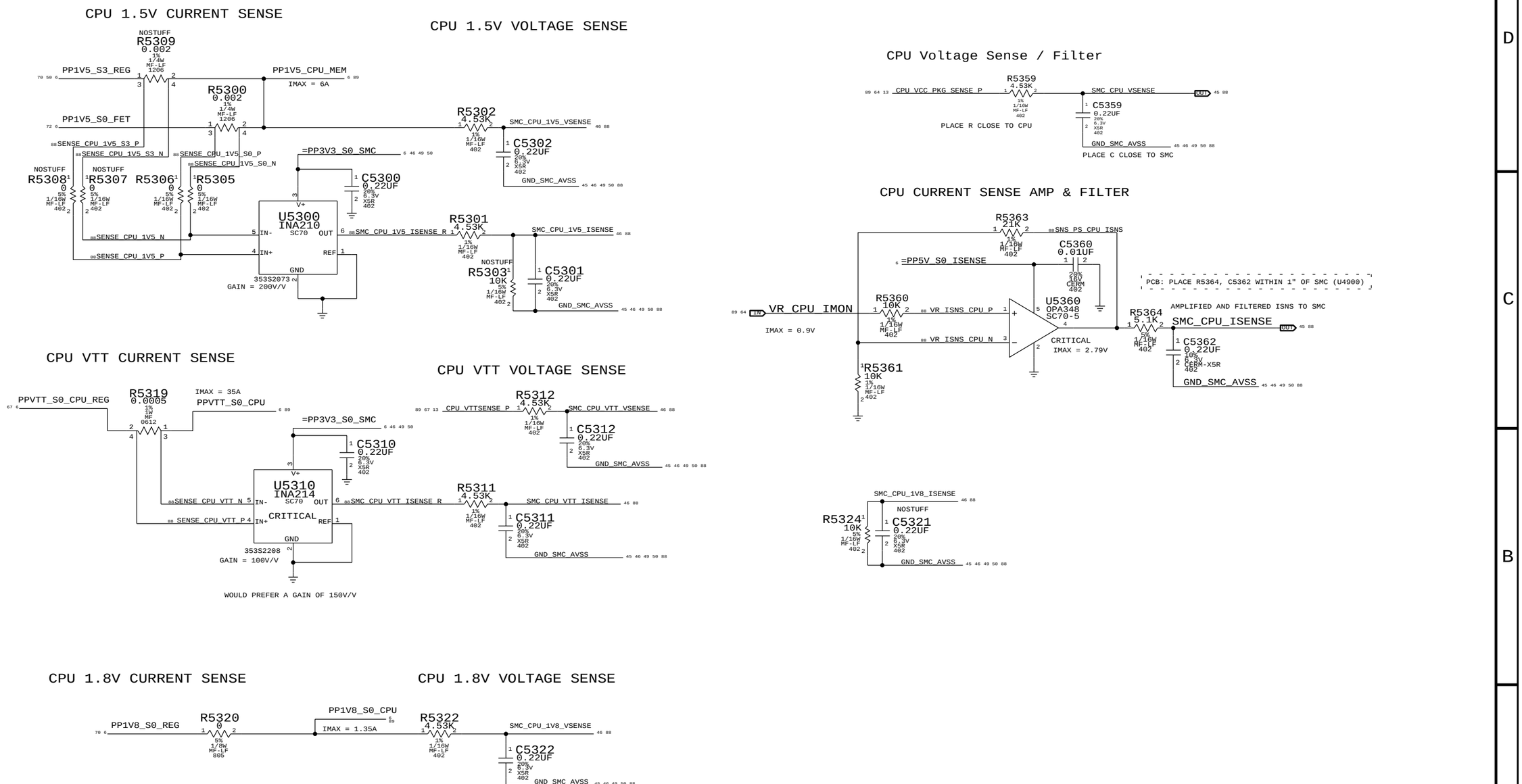

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CPU POWER SENSE

Apple Inc.

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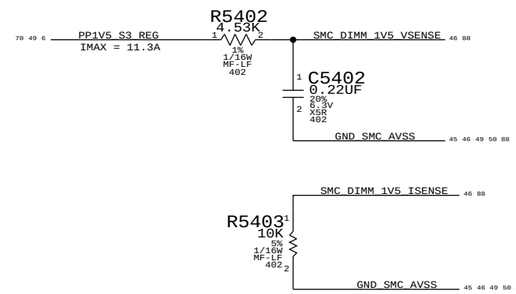
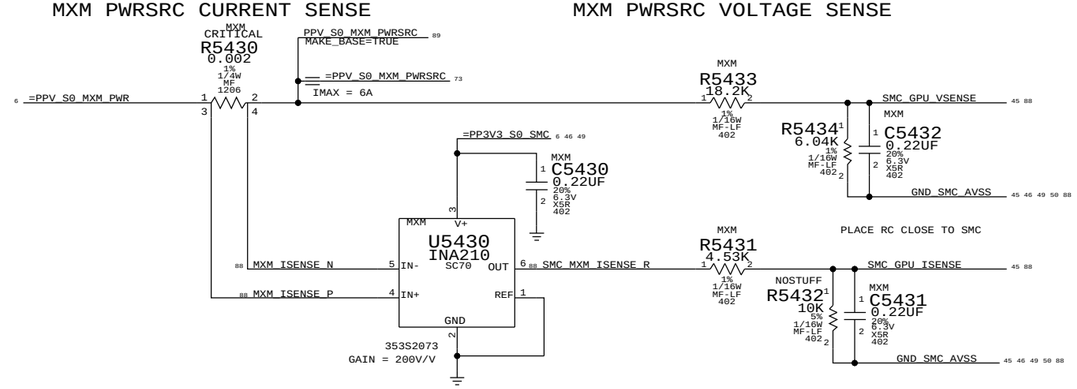
1.5V S3 VOLTAGE SENSE



MXM PWRSRC CURRENT SENSE

MXM PWRSRC VOLTAGE SENSE



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
GRAPHICS / DIMM POWER SENSE

Apple Inc.

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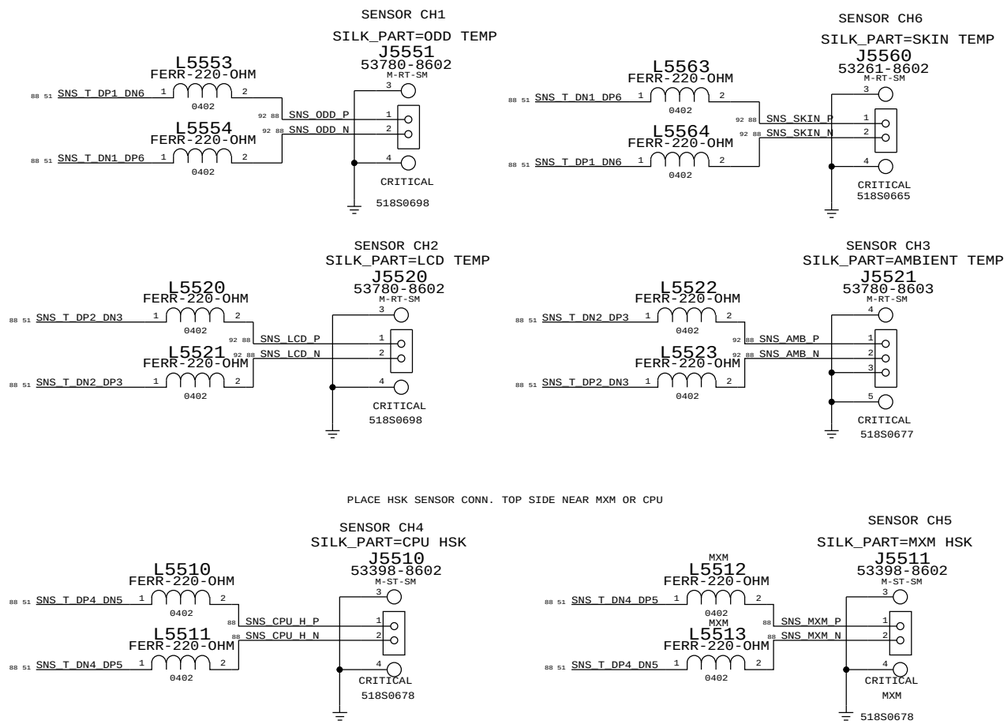
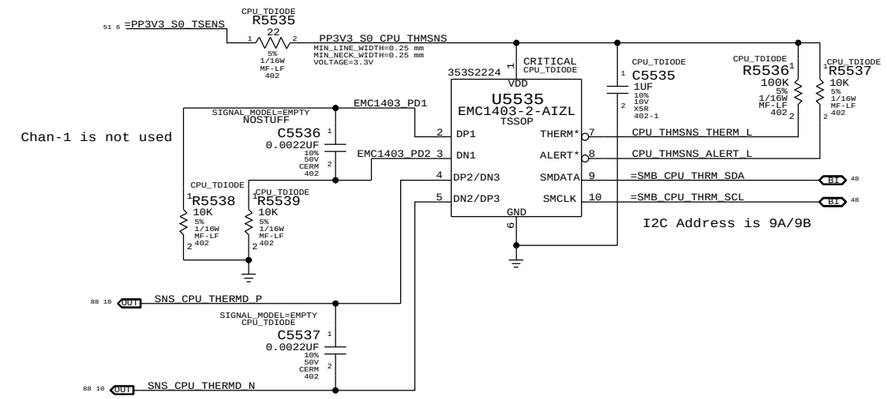
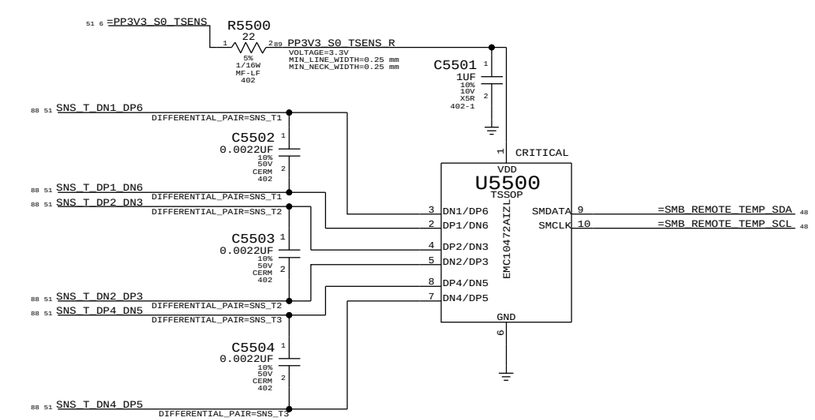
REMOTE THERMAL SENSORS
HEATSINKS, AMBIENT, PANEL AND ODD



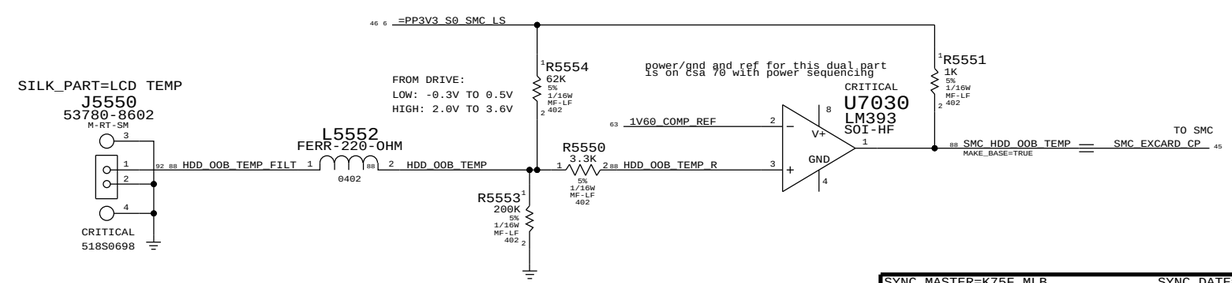
CPU T-DIODE THERMAL SENSOR



REMOTE THERMAL SENSORS (HEATSINKS AND ODD)



HDD OUT OF BAND TEMPERATURE SENSING LEVEL SHIFTING



Drive active = valid signal protocol
Drive asleep = HDD drives HDD_OOB_TEMP low
Drive disconnected = pulled high

Cannot pull low because some drives use this bit to determine 1.5 Gbps vs. 3.0 Gbps SATA

Must pull high to 2.5V for compatibility with all drives

SYNC MASTER=K75F_MLB	SYNC DATE=04/14/2010
PAGE TITLE: Thermal Sensors	
Apple Inc.	DRAWING NUMBER: 051-8600 SIZE: D
	REVISION: A.0.0
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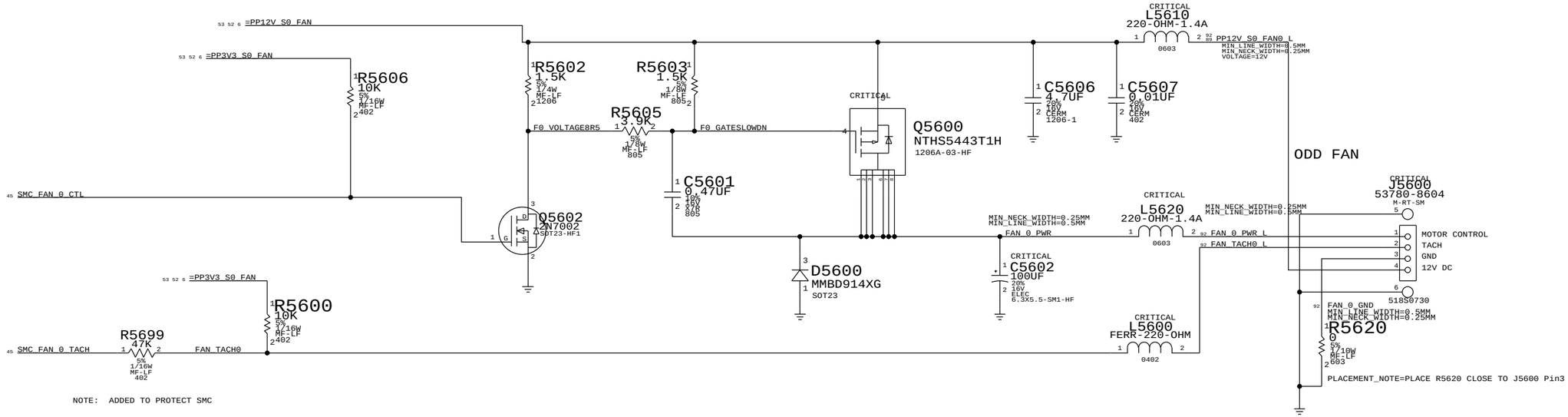
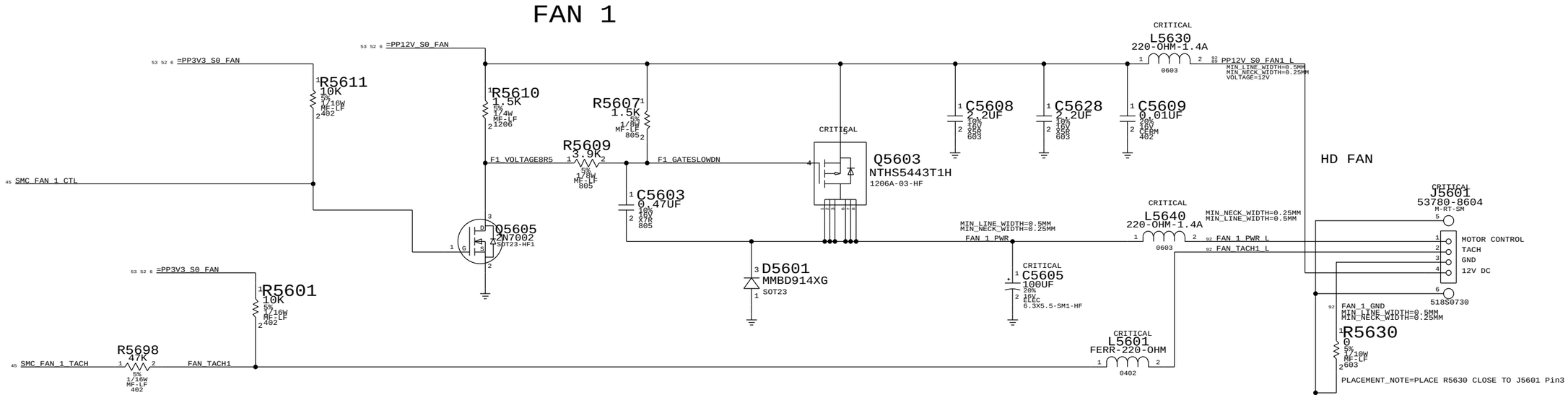
	SHEET: 51 OF 92

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
PAGE TITLE: HD AND OD FAN	
Apple Inc.	DRAWING NUMBER: 051-8600 SIZE: D
	REVISION: A.0.0
	BRANCH
	PAGE: 56 OF 110
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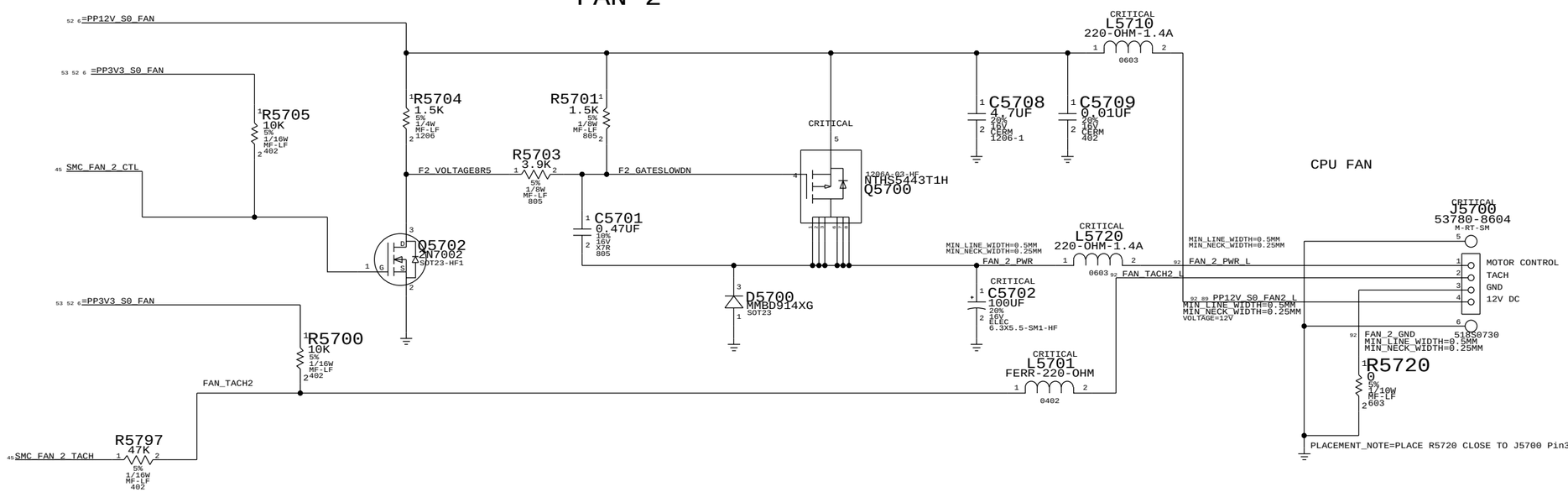
FAN 2



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: CPU FAN

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

BRANCH:

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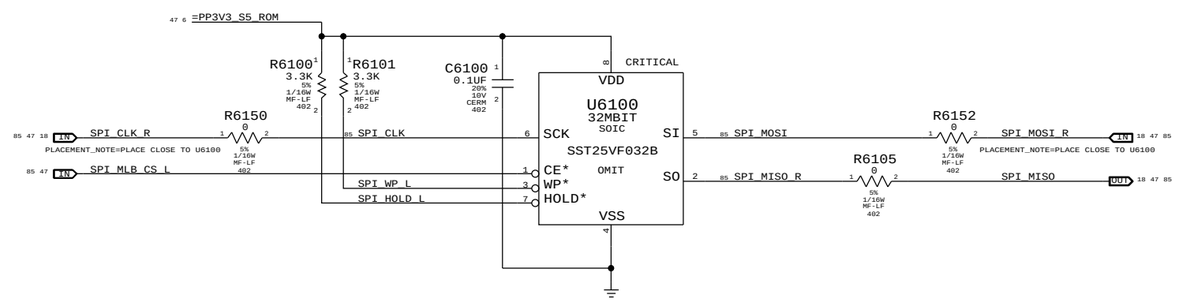

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PAGE TITLE

SPI ROM

Apple Inc.

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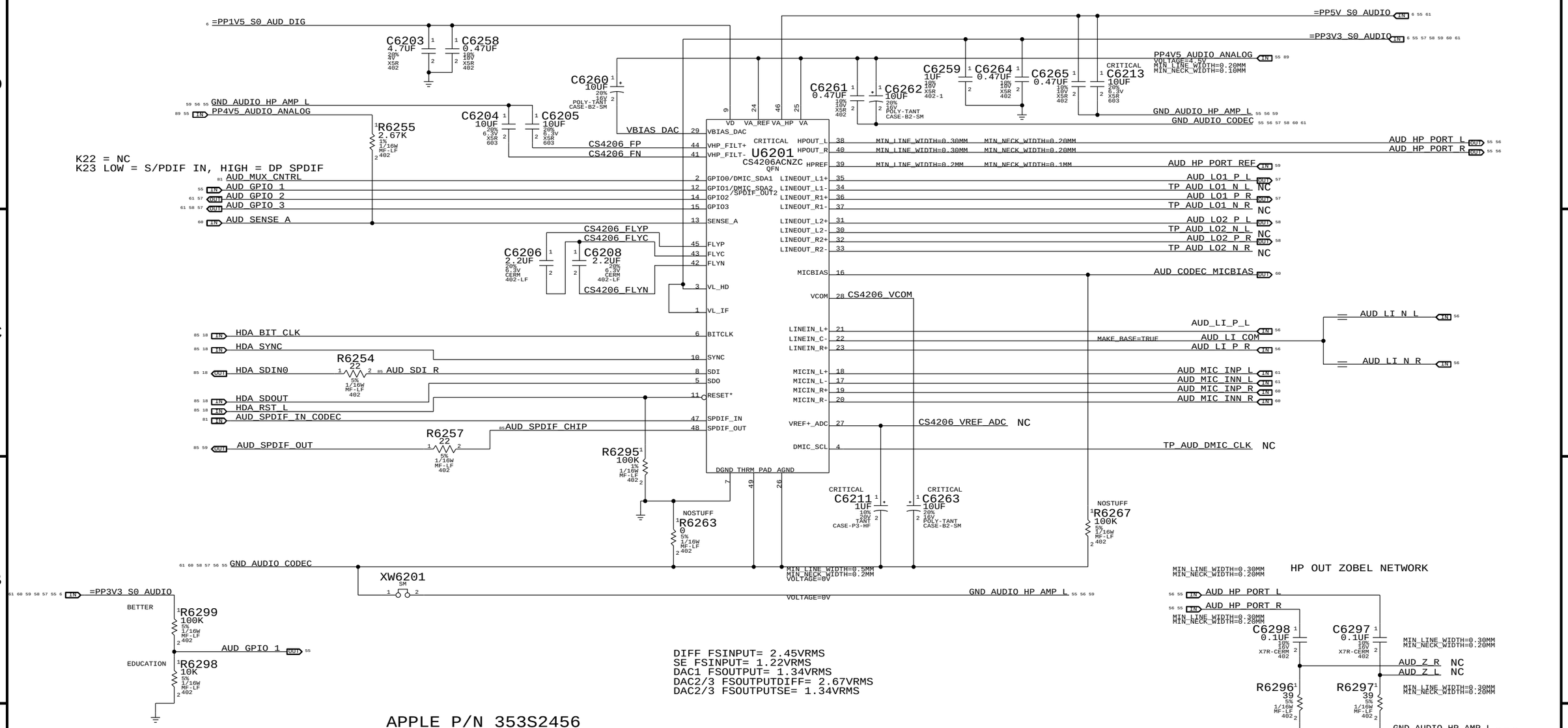
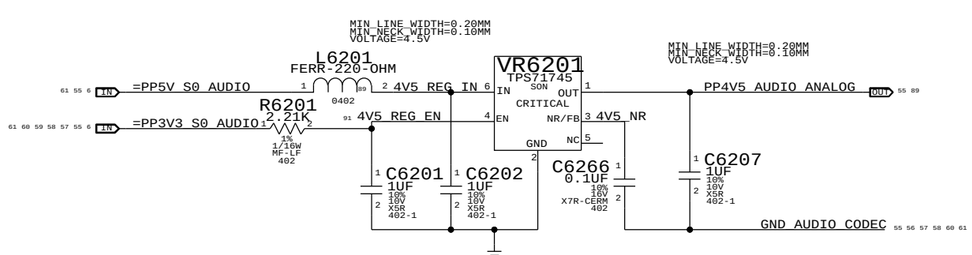
AUDIO CODEC
APPLE P/N 353S2592



APPLE P/N 353S2456
4.5V POWER SUPPLY FOR CODEC



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
AUDIO: CODEC/REGULATOR

Apple Inc.

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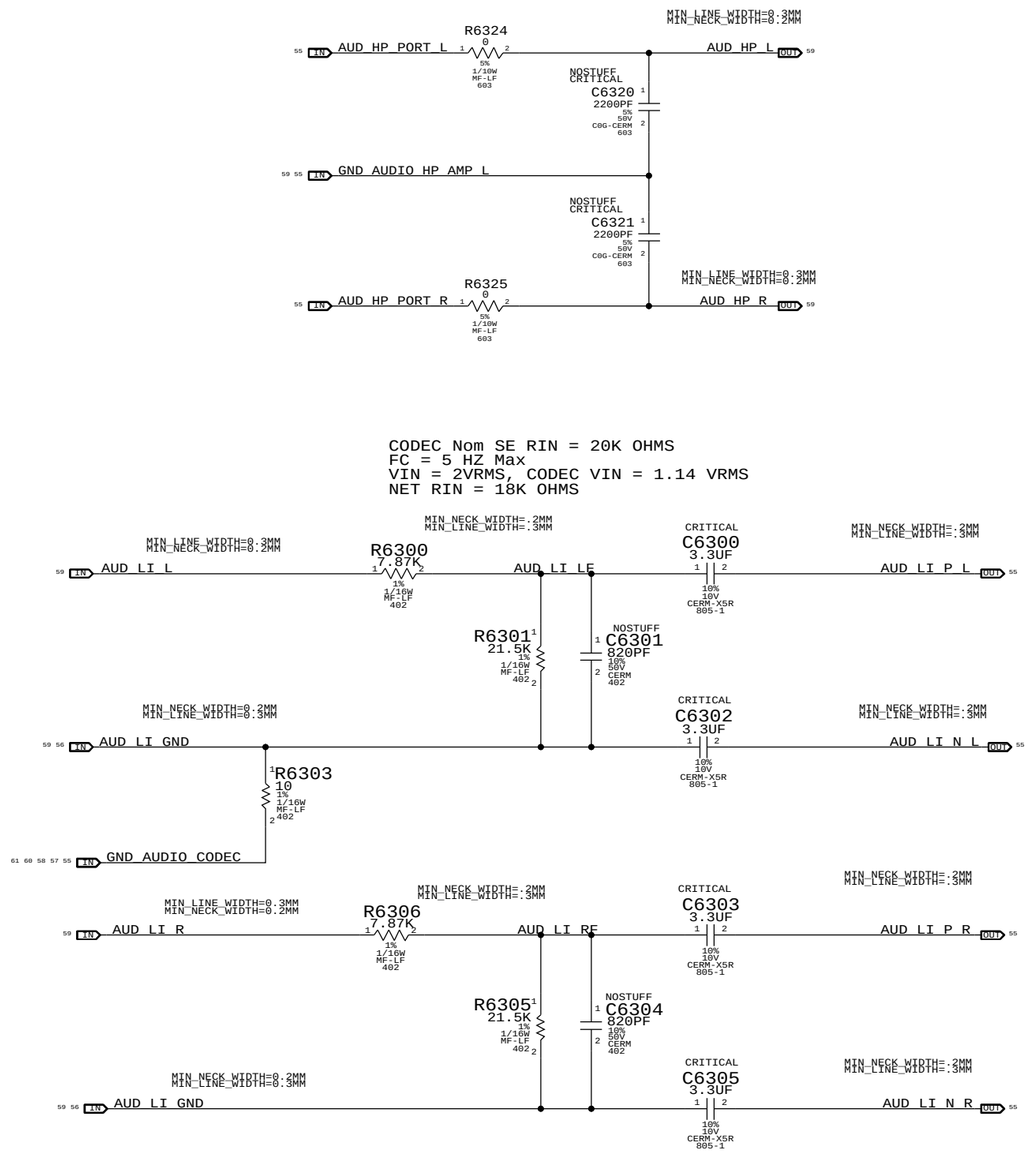
1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
AUDIO: FILTER/BUFFER

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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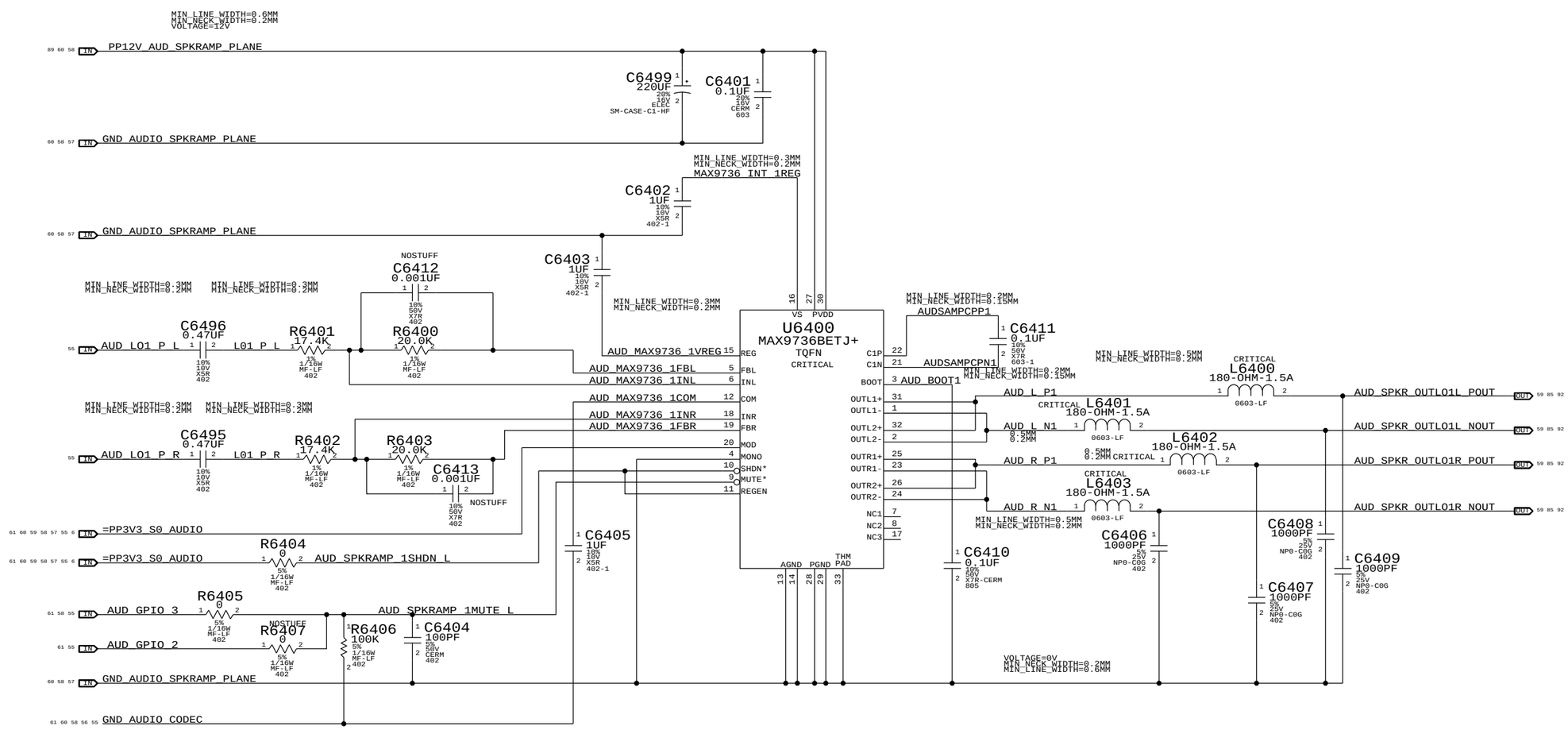
TWEETER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ

POUT = 6.76 W INTO 8 OHMS @ 1% THD+N



SYNC_MASTER=K75F_MLB	SYNC_DATE=04/14/2010
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Apple Inc.	DRAWING NUMBER: 051-8600 SIZE: D
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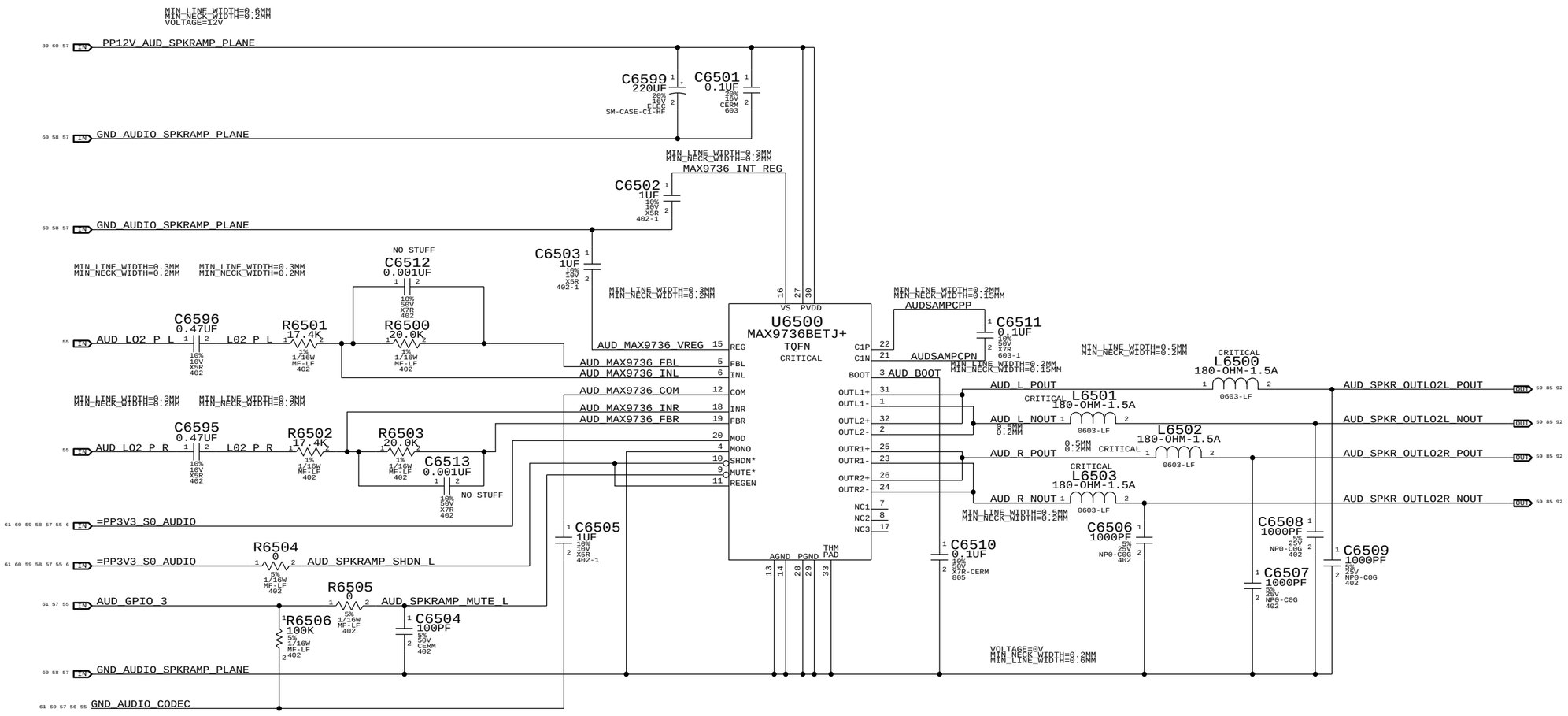
WOOFER SPEAKER AMPLIFIER

MAX9736B APN:353S2042

GAIN = -4.8(20K/17.4K)
CODEC OUT = 1.335VRMS
AMP VOUT = 7.355VRMS
POUT = 6.76 W INTO 8 OHMS @ 1% THD+N

TURN ON TIME: 110MS
TURN ON DELAY: 150MS
RIN = 17.4 OHMS
FC = 19.5 HZ



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Apple Inc.	DRAWING NUMBER: 051-8600 SIZE: D
	REVISION: A.0.0
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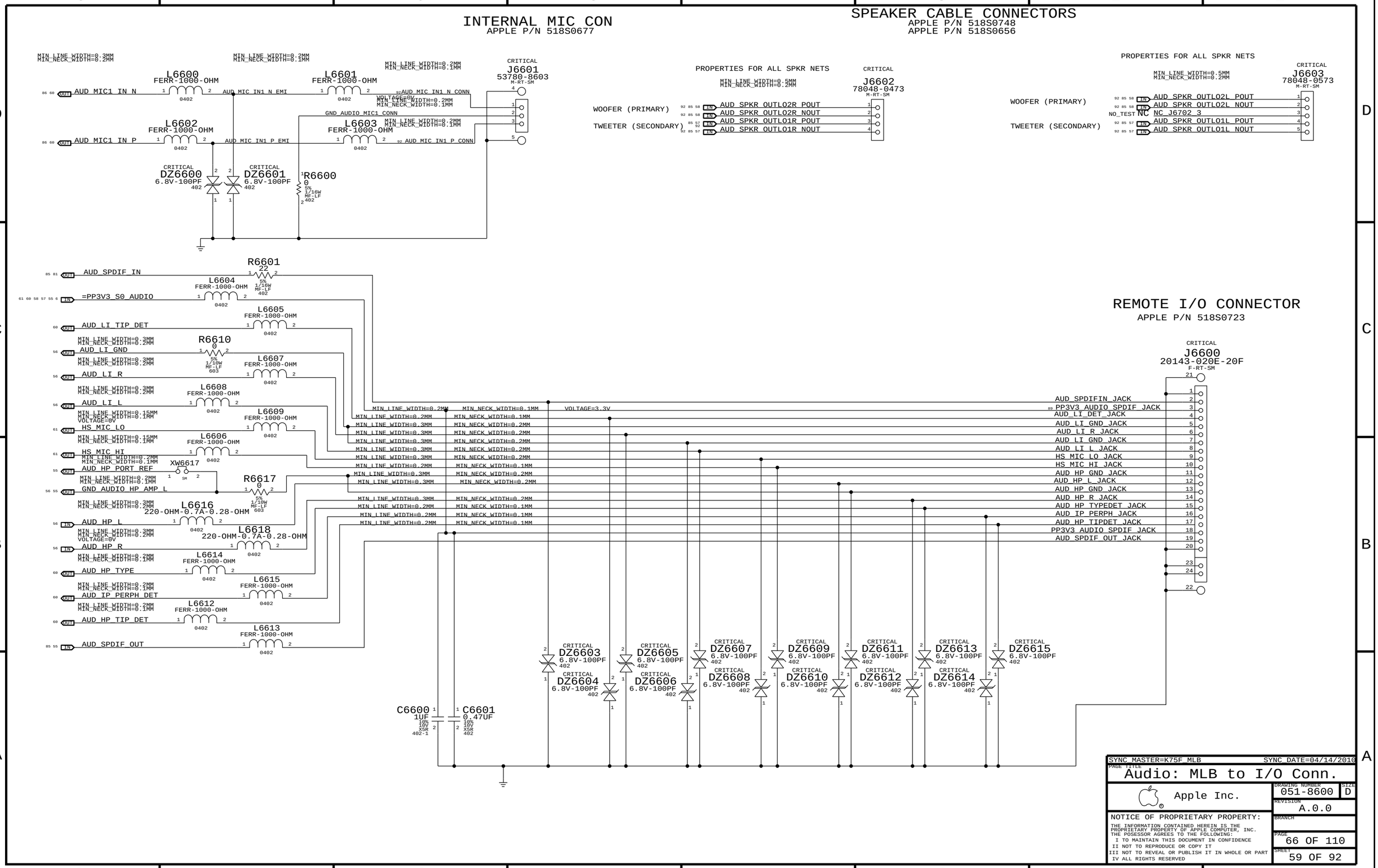
INTERNAL MIC CON
APPLE P/N 518S0677
SPEAKER CABLE CONNECTORS
APPLE P/N 518S0748
APPLE P/N 518S0656
REMOTE I/O CONNECTOR
APPLE P/N 518S0723
J6601 53780-8603
J6602 78048-0473
J6603 78048-0573
J6600 20143-020E-20F
L6600 FERR-1000-OHM
L6601 FERR-1000-OHM
L6602 FERR-1000-OHM
L6603 FERR-1000-OHM
DZ6600 6.8V-100PF
DZ6601 6.8V-100PF
R6600 0
R6601 22
L6604 FERR-1000-OHM
L6605 FERR-1000-OHM
R6610 0
L6607 FERR-1000-OHM
L6608 FERR-1000-OHM
L6609 FERR-1000-OHM
L6606 FERR-1000-OHM
XW6617
R6617 0
L6616 220-OHM-0.7A-0.28-OHM
L6618 220-OHM-0.7A-0.28-OHM
L6614 FERR-1000-OHM
L6615 FERR-1000-OHM
L6612 FERR-1000-OHM
L6613 FERR-1000-OHM
C6600 1UF
C6601 0.47UF
AUD_MIC1_IN_N
AUD_MIC1_IN_P
AUD_MIC_IN1_N_EMI
AUD_MIC_IN1_P_EMI
AUD_MIC_IN1_N_CONN
AUD_MIC_IN1_P_CONN
GND_AUDIO_MIC1_CONN
AUD_SPDIF_IN
=PP3V3_S0_AUDIO
AUD_LI_TIP_DET
AUD_LI_GND
AUD_LI_R
AUD_LI_L
HS_MIC_LO
HS_MIC_HI
AUD_HP_PORT_REF
GND_AUDIO_HP_AMP_L
AUD_HP_L
AUD_HP_R
AUD_HP_TYPE
AUD_IP_PERPH_DET
AUD_HP_TIP_DET
AUD_SPDIF_OUT
AUD_SPDIFIN_JACK
PP3V3_AUDIO_SPDIF_JACK
AUD_LI_DET_JACK
AUD_LI_GND_JACK
AUD_LI_R_JACK
AUD_LI_GND_JACK
AUD_LI_L_JACK
HS_MIC_LO_JACK
HS_MIC_HI_JACK
AUD_HP_GND_JACK
AUD_HP_L_JACK
AUD_HP_GND_JACK
AUD_HP_R_JACK
AUD_HP_TYPEDET_JACK
AUD_IP_PERPH_JACK
AUD_HP_TIPDET_JACK
PP3V3_AUDIO_SPDIF_JACK
AUD_SPDIF_OUT_JACK
WOOFER (PRIMARY)
TWEETER (SECONDARY)
AUD_SPKR_OUTLO2R_POUT
AUD_SPKR_OUTLO2R_NOUT
AUD_SPKR_OUTLO1R_POUT
AUD_SPKR_OUTLO1R_NOUT
AUD_SPKR_OUTLO2L_POUT
AUD_SPKR_OUTLO2L_NOUT
NC_J6702_3
AUD_SPKR_OUTLO1L_POUT
AUD_SPKR_OUTLO1L_NOUT
PROPERTIES FOR ALL SPKR NETS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
VOLTAGE=0V
SYNC MASTER=K75F MLB
SYNC DATE=04/14/2010
PAGE TITLE
Audio: MLB to I/O Conn.
Apple Inc.
DRAWING NUMBER 051-8600
SIZE D
REVISION A.0.0
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PAGE 66 OF 110
SHEET 59 OF 92
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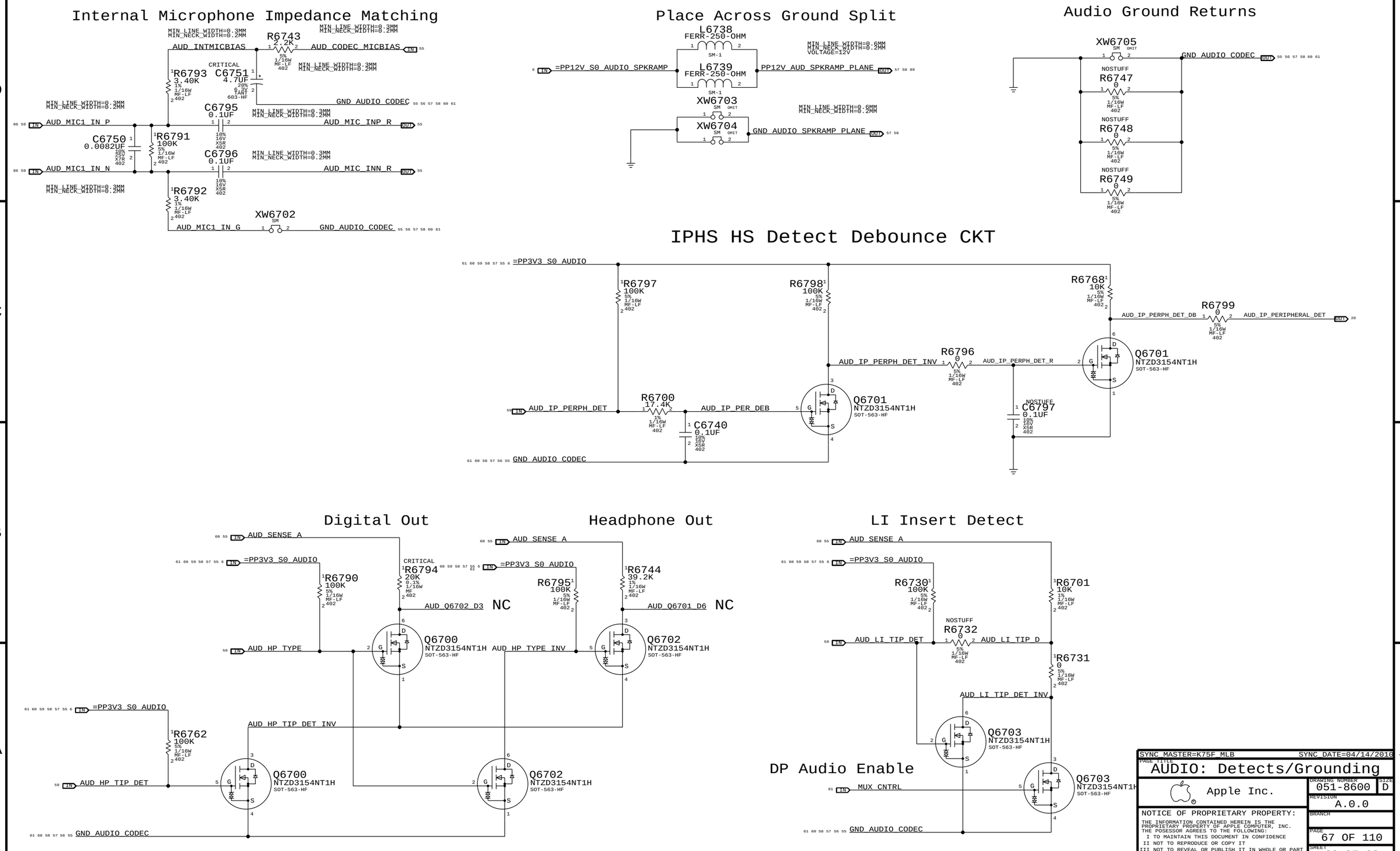

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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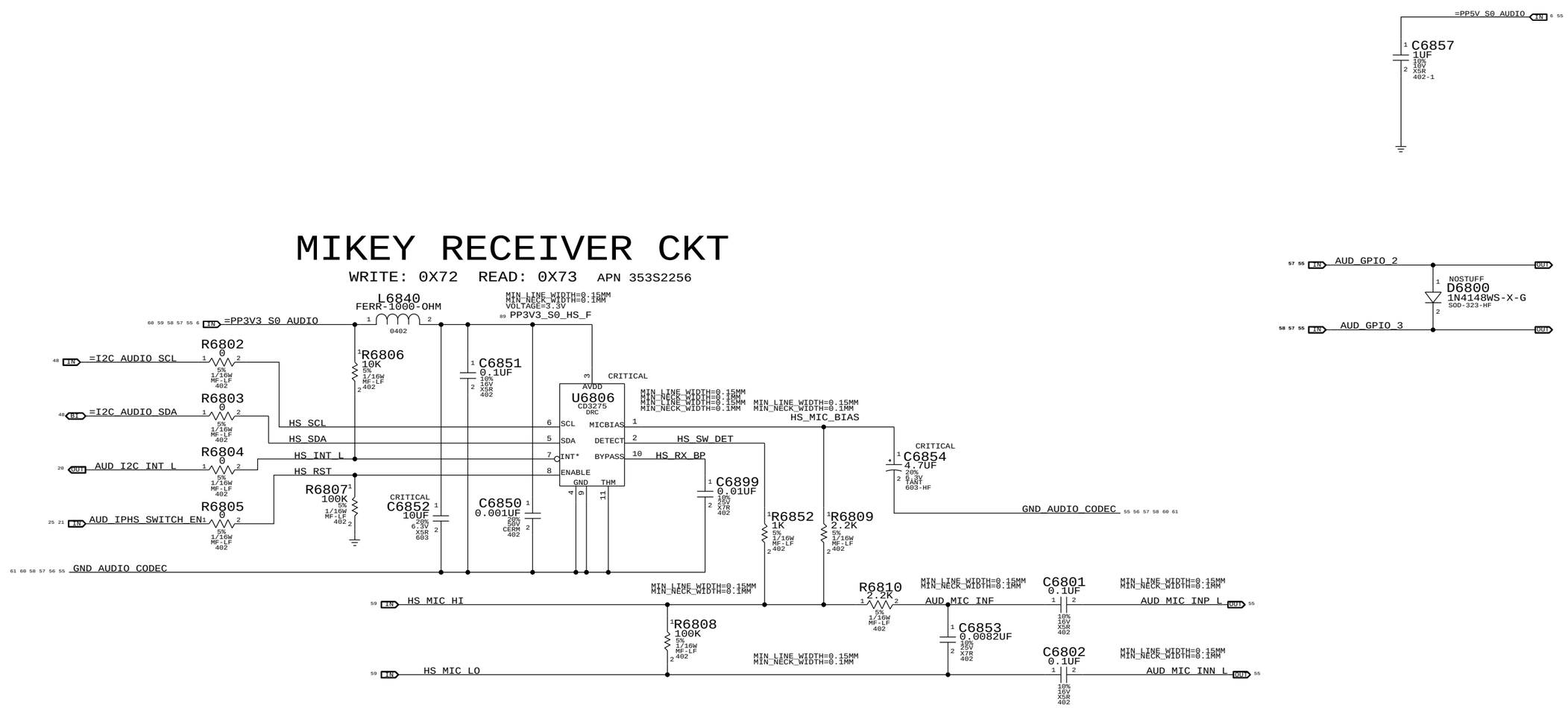
FUNCTION	PIN	CONVERTER	VOLUME	ENABLE/ CNTRL TYPE	DETECT/INTERRUPT
PRIMARY	0X0B	0X04	0X04	GPIO 3	N/A
SECONDARY	0X0A	0X03	0X03	GPIO 3	N/A
HEADPHONES	0X09	0X02	0X02	N/A	0X09 (A)
LINE INPUT	0X0C	0X05	0X05	N/A	LINE IN
BUILT-IN MICROPHONE	0X0D(13,B,RIGHT)	0X06	0X06	MICBIAS 80%	N/A
HEADSET MICROPHONE	0X0D (13,V22,B,LEFT)	0X06	0X06	MIKEY	MIKEY
SPDIF OUT	0X10	0X08	N/A	N/A	0X0C (B)
SPDIF IN	0X0F	0X07	N/A	N/A	N/A
MIKEY	N/A	N/A	N/A	MCP GPIO_38	MCP GPIO_5



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: AUDIO: Mikey

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

REVISION: A.0.0

BRANCH:

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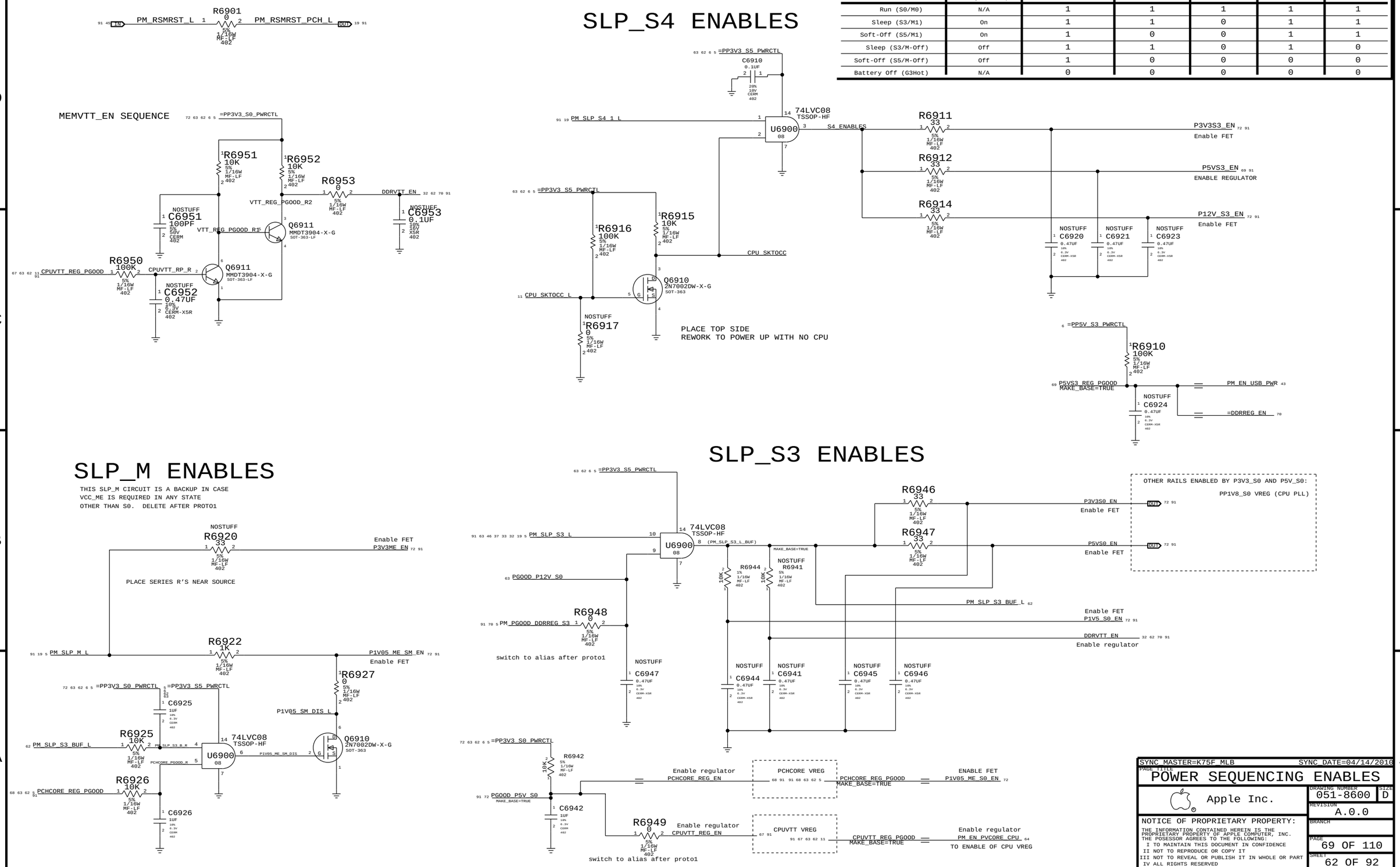
SHEET: 61 OF 92

SLP_S4 ENABLES

State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
POWER SEQUENCING ENABLES

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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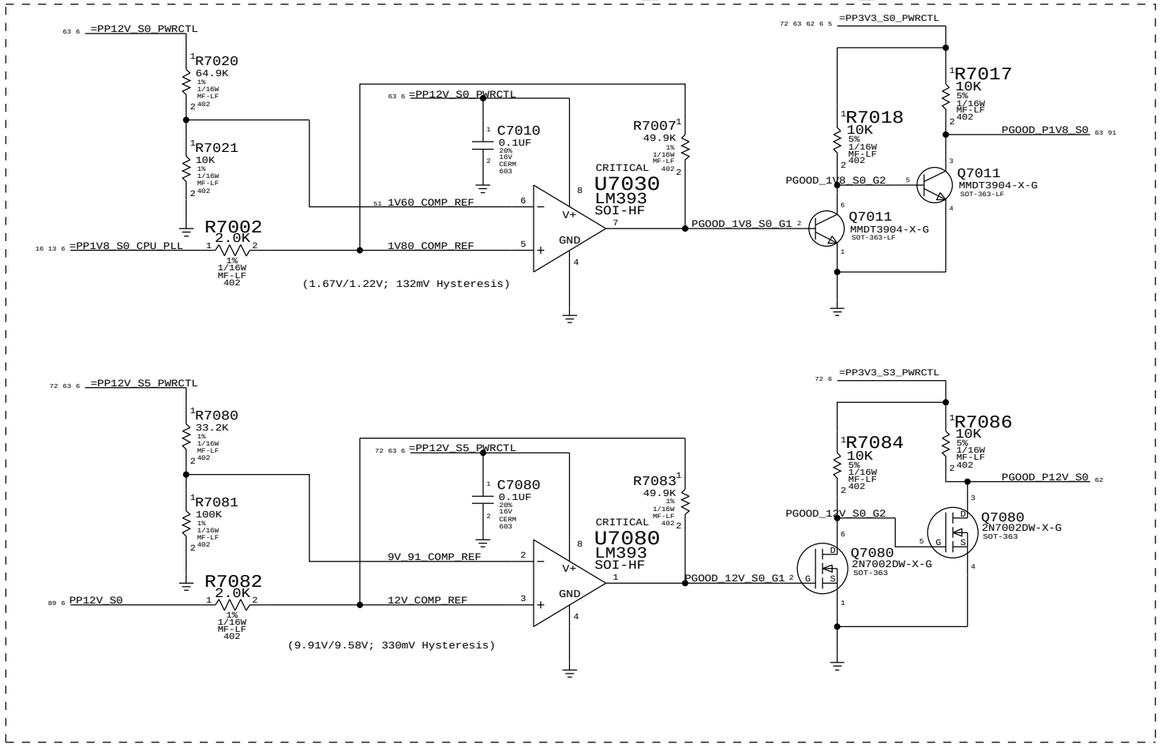
PGOOD COMPARATORS FOR PP1V8_S0 AND PP12V_S0

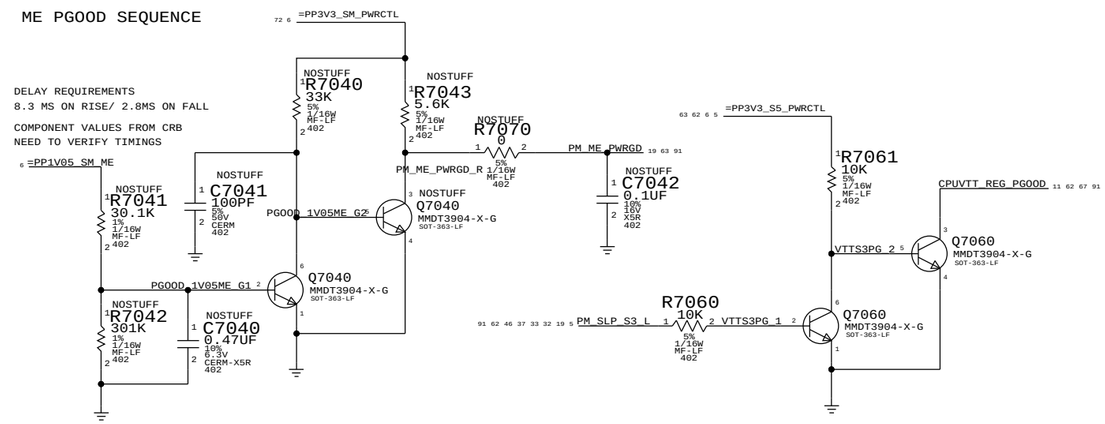


S0 RAILS PGOOD

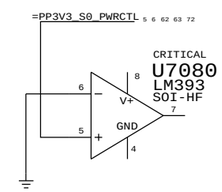
ME PGOOD SEQUENCE

DELAY REQUIREMENTS
8.3 MS ON RISE/ 2.8MS ON FALL

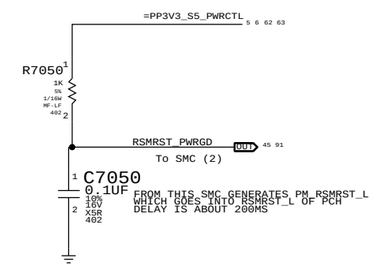
COMPONENT VALUES FROM CRB
NEED TO VERIFY TIMINGS

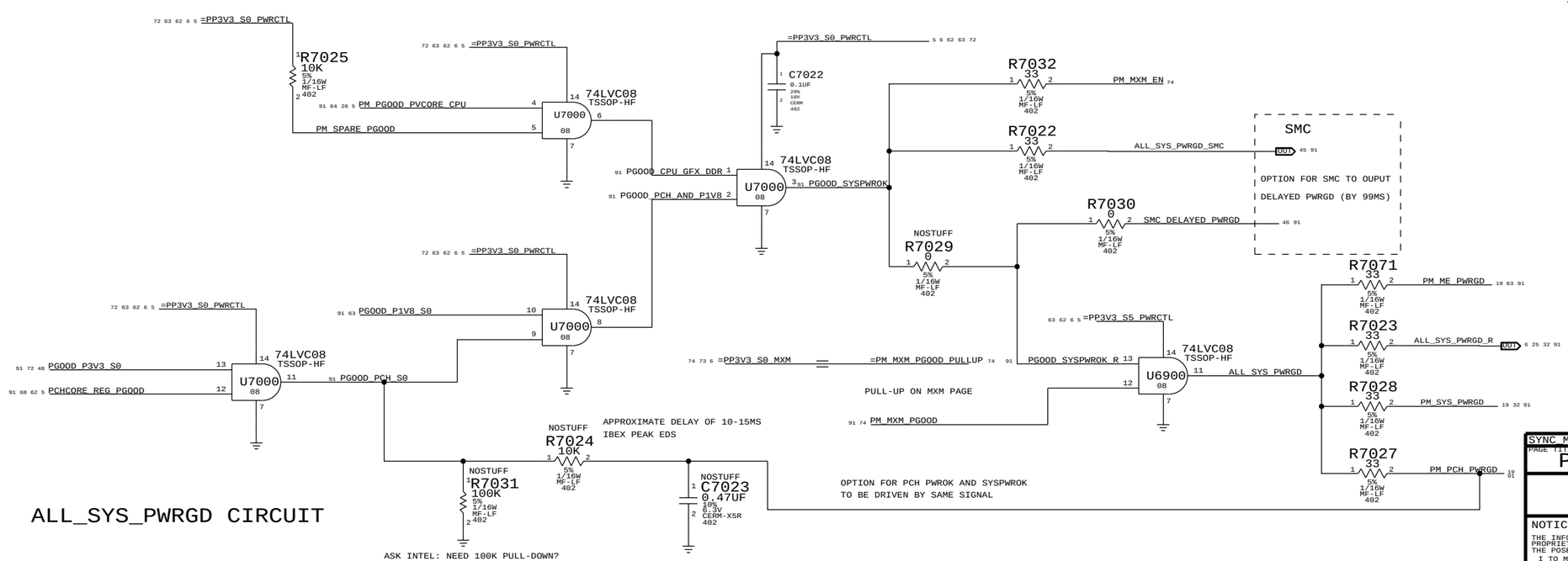


DISABLE CPUVTT_REG_PGOOD WHEN SLP_S3_L = 0 (PER PIKETON PDG)



SPARE





ALL_SYS_PWRGD CIRCUIT

SYNC MASTER=K75F MLB SYNC DATE=04/14/2010

PAGE TITLE
POWER SEQUENCING PGOOD

Apple Inc.

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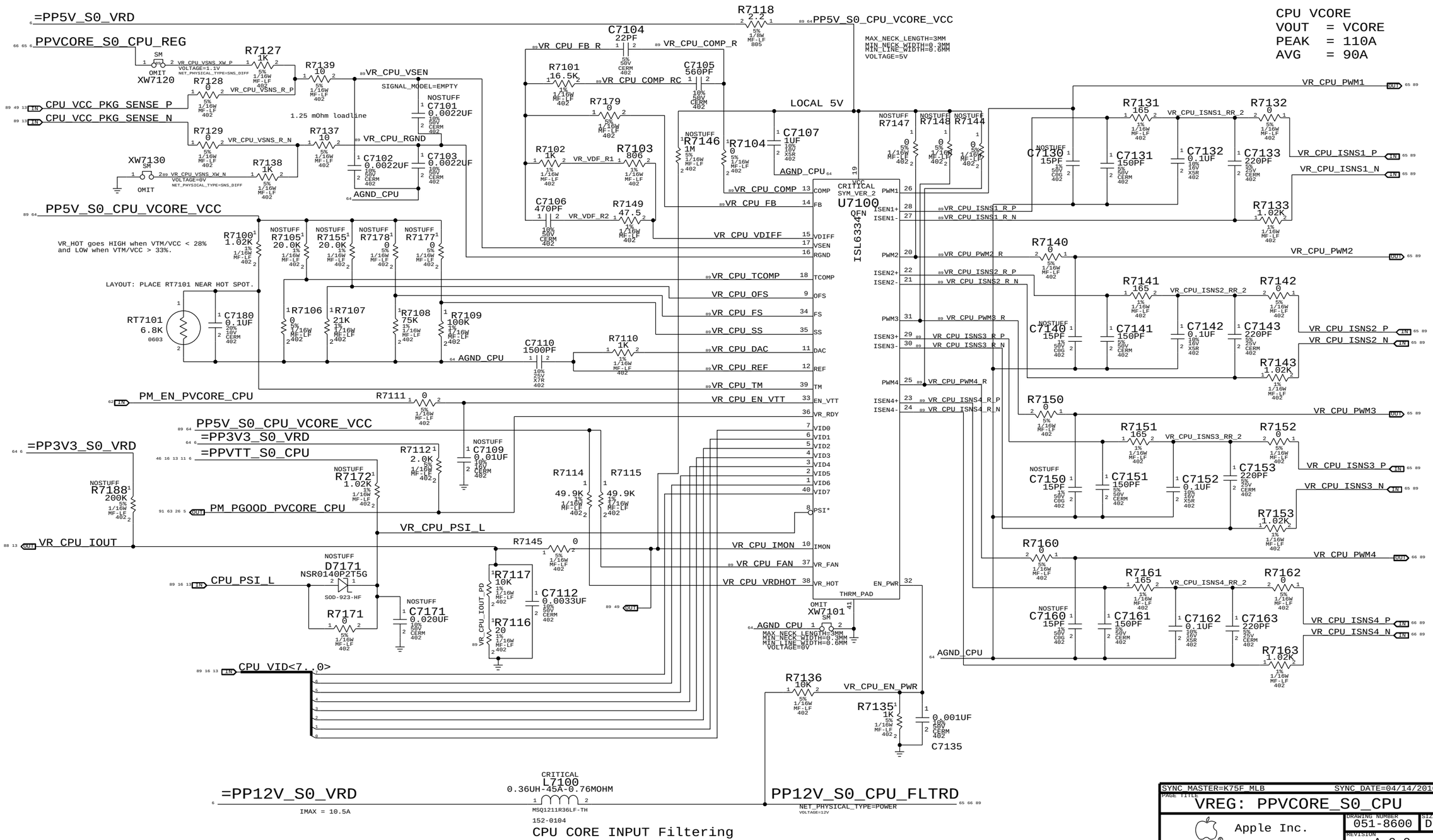
CPU CORE REG 1.1V/110A O/P= PPVCORE_S0_CPU_REG



CPU CORE INPUT Filtering

SYNC MASTER=K75F_MLB SYNC DATE=04/14/2010

PAGE TITLE
VREG: PPVCORE_S0_CPU

Apple Inc.

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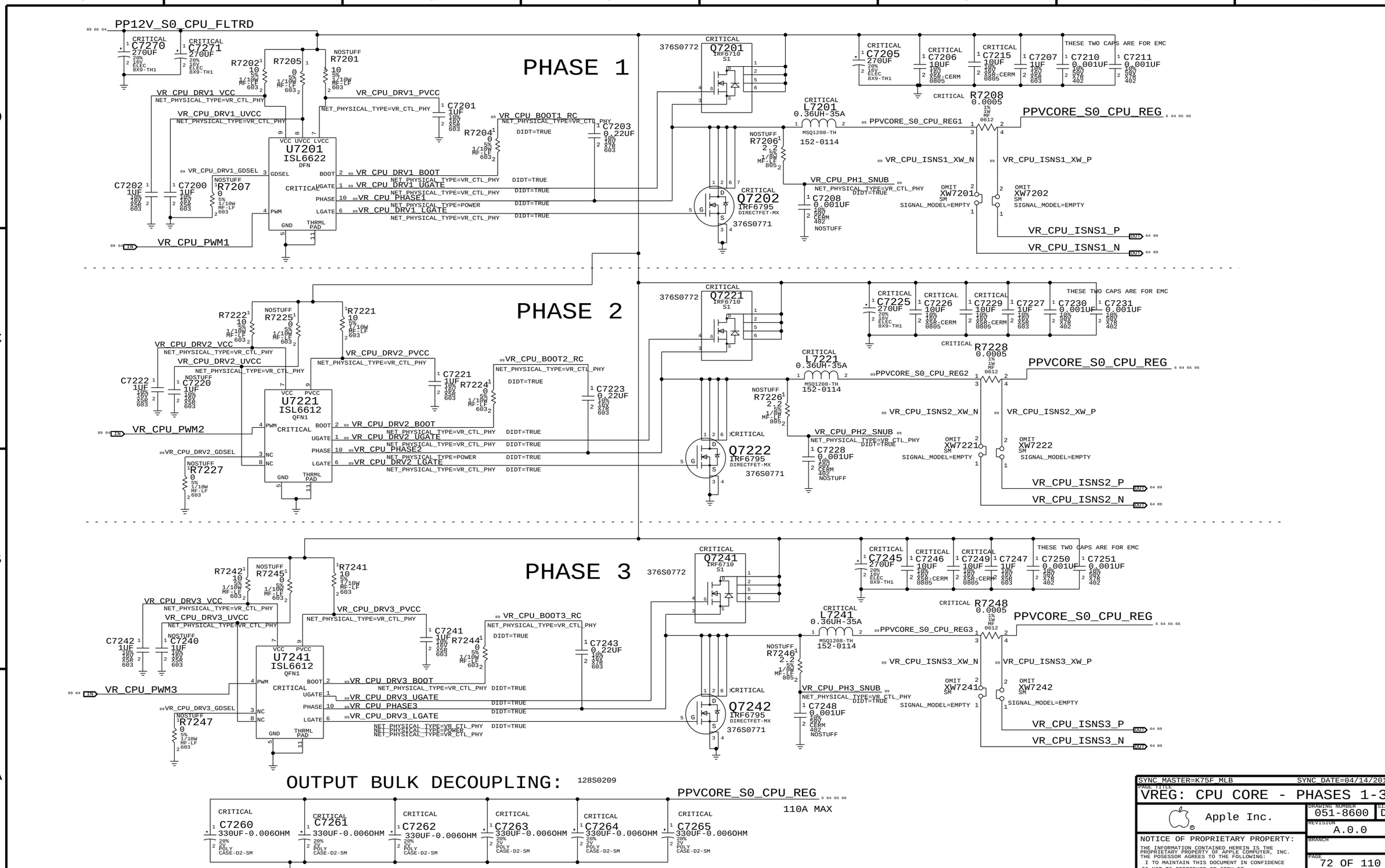

SYNC MASTER=K75F MLB SYNC DATE=04/14/2010

PAGE TITLE
VREG: CPU CORE - PHASES 1-3

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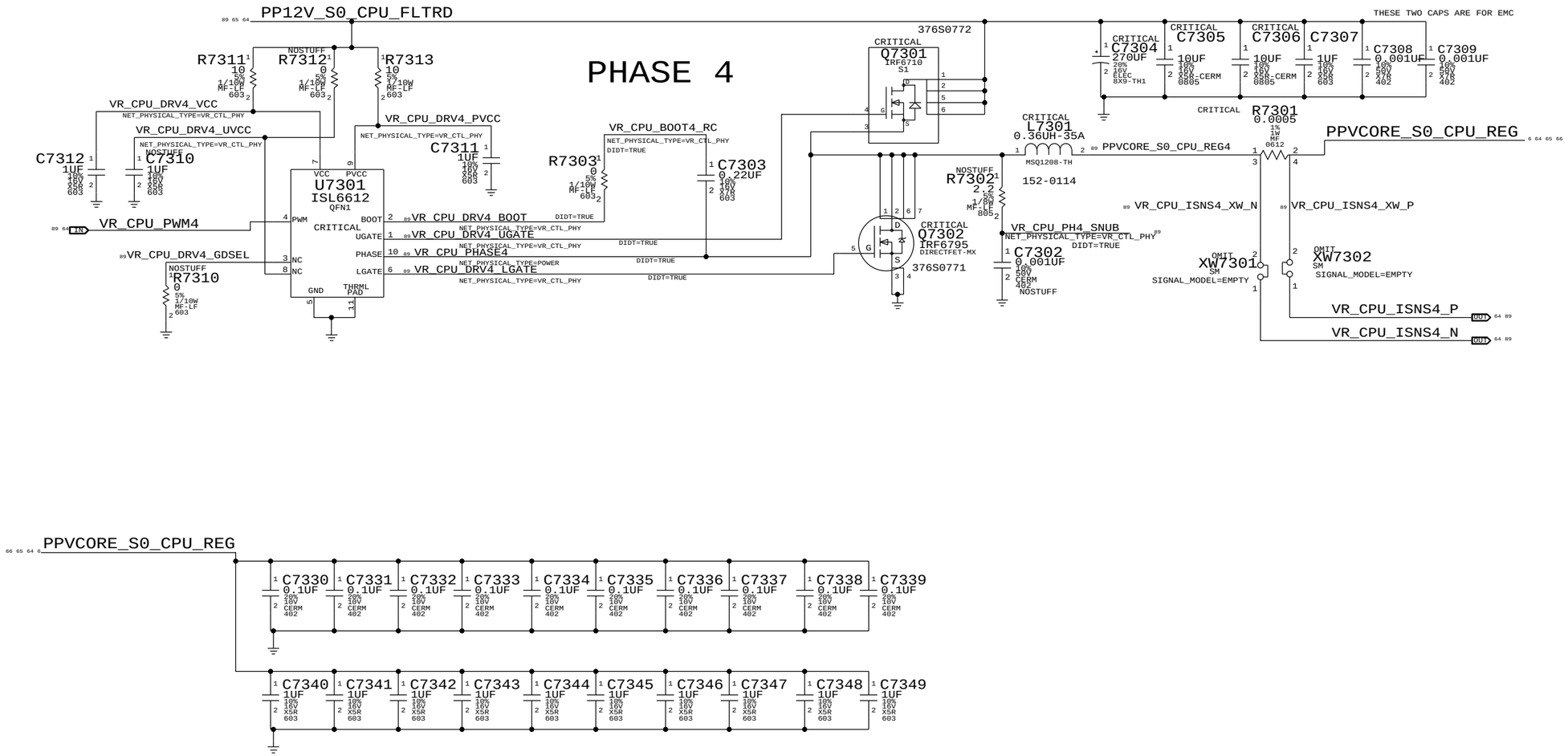

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
VREG: CPU CORE - PHASE 4

Apple Inc.

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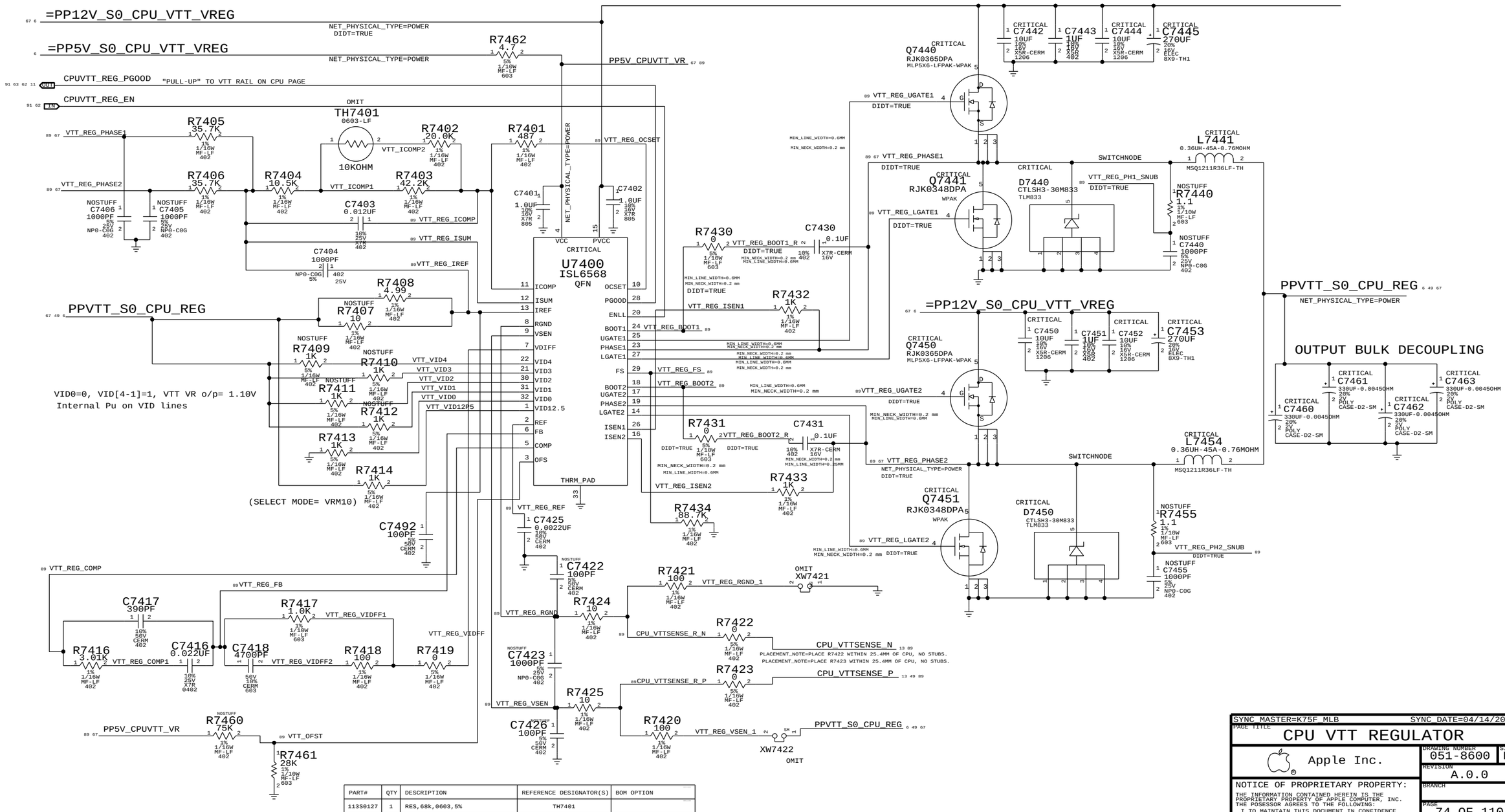
CPU VTT REG 1.1V/30A O/P= PPVTT_S0_CPU_REG

CPU VTT
VOUT = 1.1V OR 1.05V
PEAK = 35A
AVG = 30A



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S0127	1	RES,68k,0603,5%	TH7401	

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
CPU VTT REGULATOR

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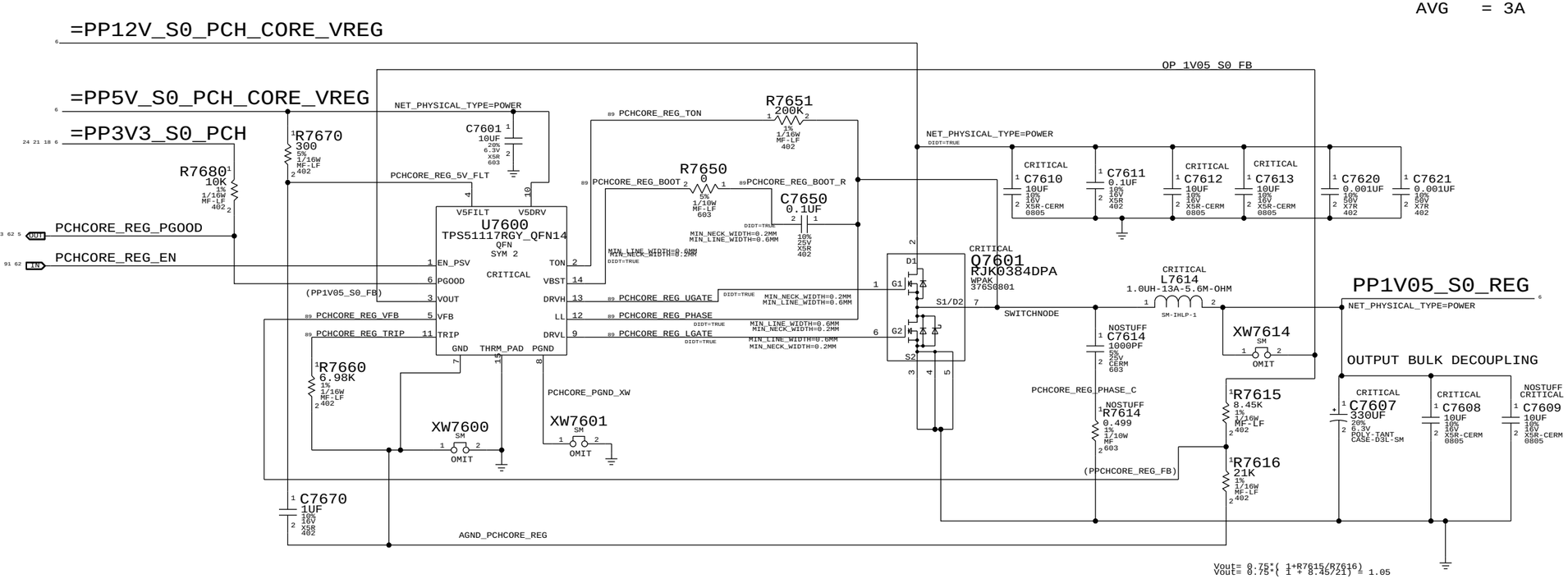
IBEX PEAK CORE REG 1.05V OUTPUT = PP1V05_S0_REG

PP1V05_S0_REG
VOUT = 1.05V
PEAK = 7.5A
AVG = 3A



PAGE TITLE	IBEX PEAK CORE
Apple Inc.	DRAWING NUMBER 051-8600 SIZE D
	REVISION A.0.0
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	PAGE 76 OF 110
	SHEET 68 OF 92

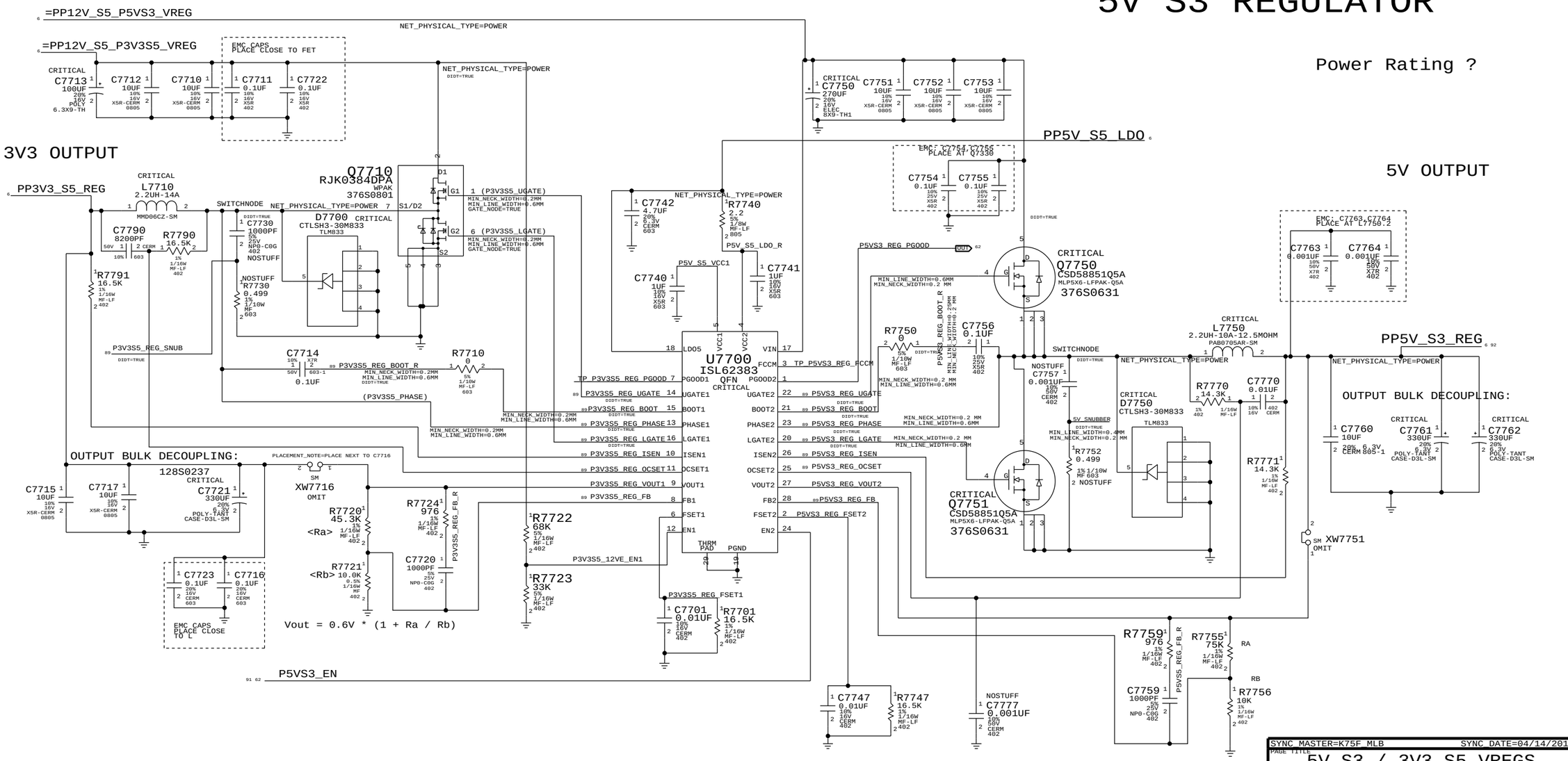
3V3 S5 REGULATOR

5V S3 REGULATOR

Power Rating ?

3V3 OUTPUT

5V OUTPUT



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2016

PAGE TITLE: 5V_S3 / 3V3_S5 VREGS

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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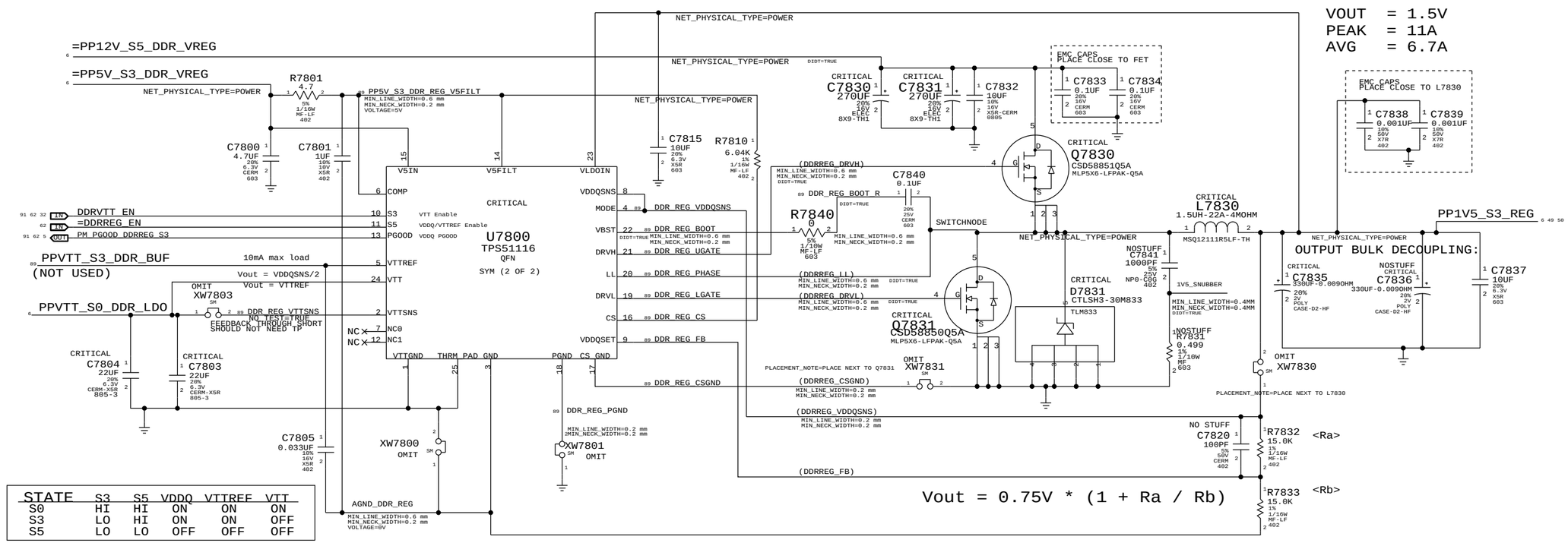
1.5 V DDR SUPPLY

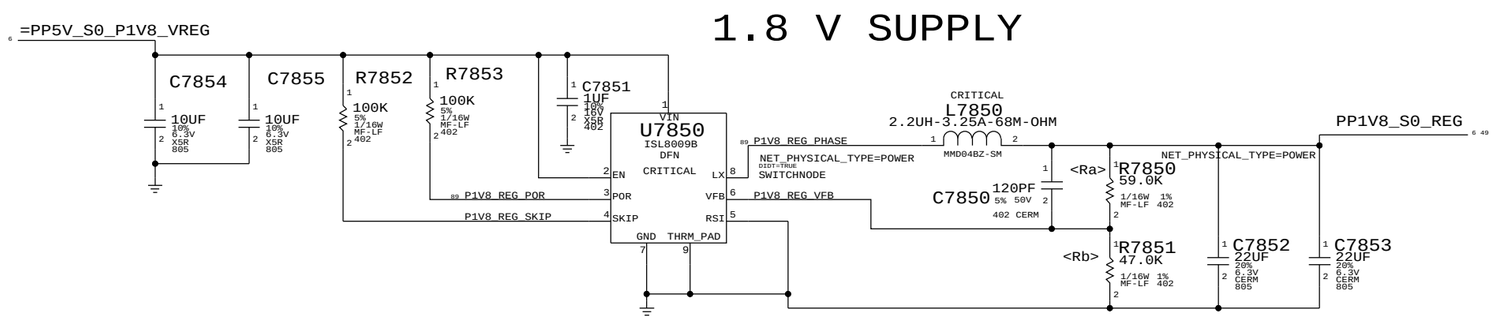
PPDDR_S3_REG
VOUT = 1.5V
PEAK = 11A
AVG = 6.7A



STATE	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON
S3	LO	HI	ON	ON	OFF
S5	LO	LO	OFF	OFF	OFF

Vout = 0.75V * (1 + Ra / Rb)

1.8 V SUPPLY



Vo=0.8*(1+ Ra/Rb)
Vo=0.8*(1+ 59/47)=1.804V

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: 1.5V / 1.8V VREGS

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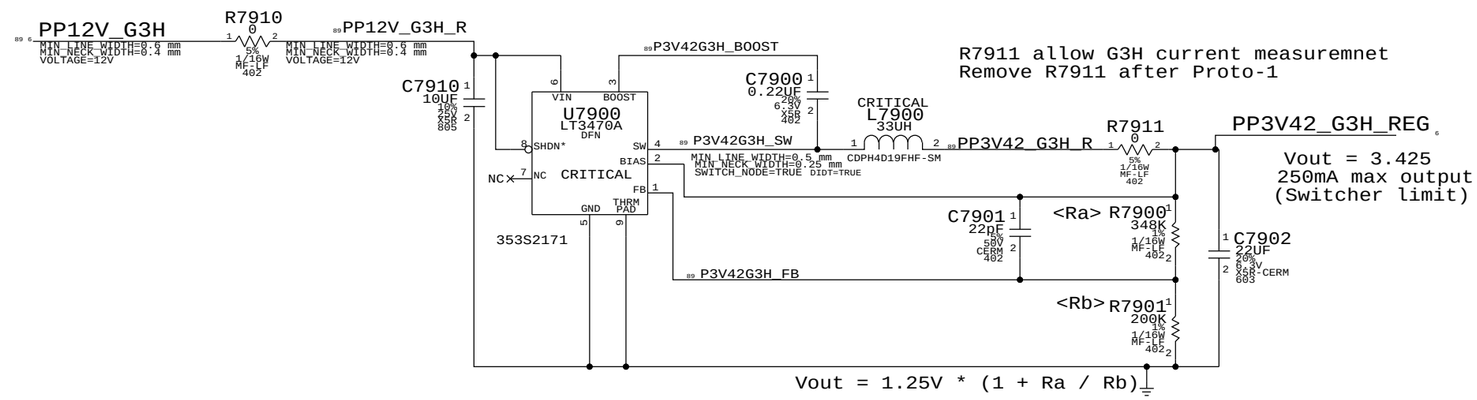
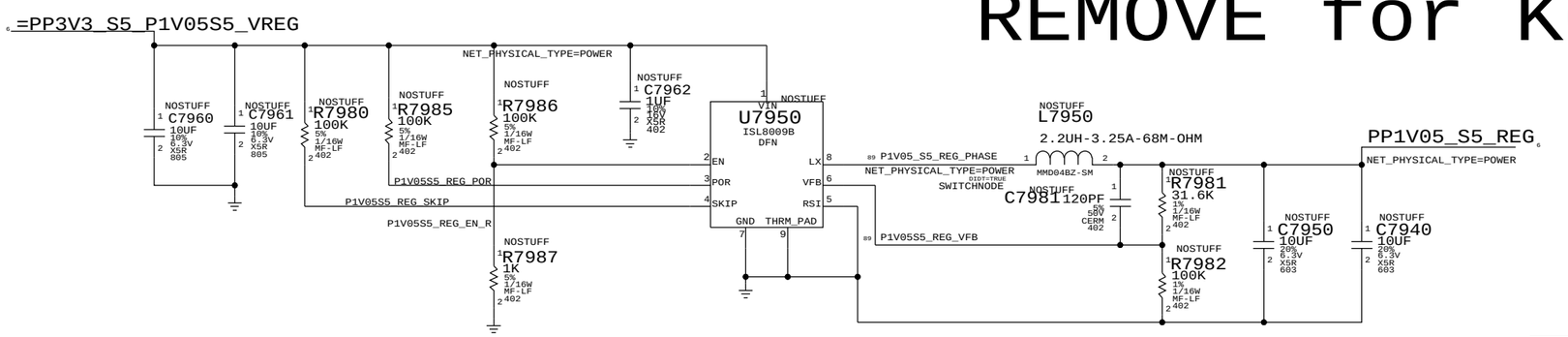
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



1.05V S5 SUPPLY

REMOVE for K60/K61



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: 1.05 S5 SUPPLY

Apple Inc.

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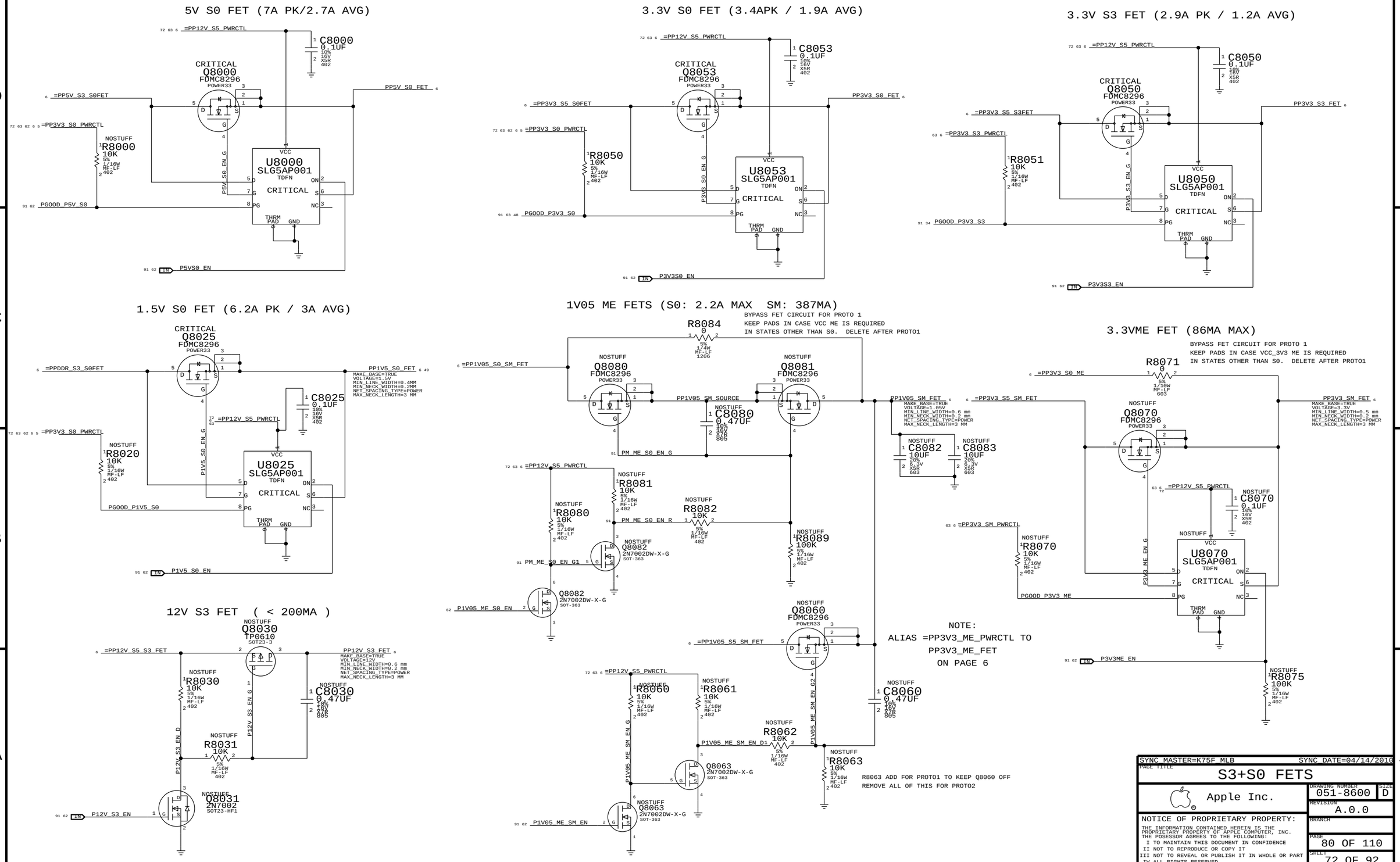

SYNC MASTER=K75F_MLB SYNC DATE=04/14/2010

PAGE TITLE

S3+S0 FETS

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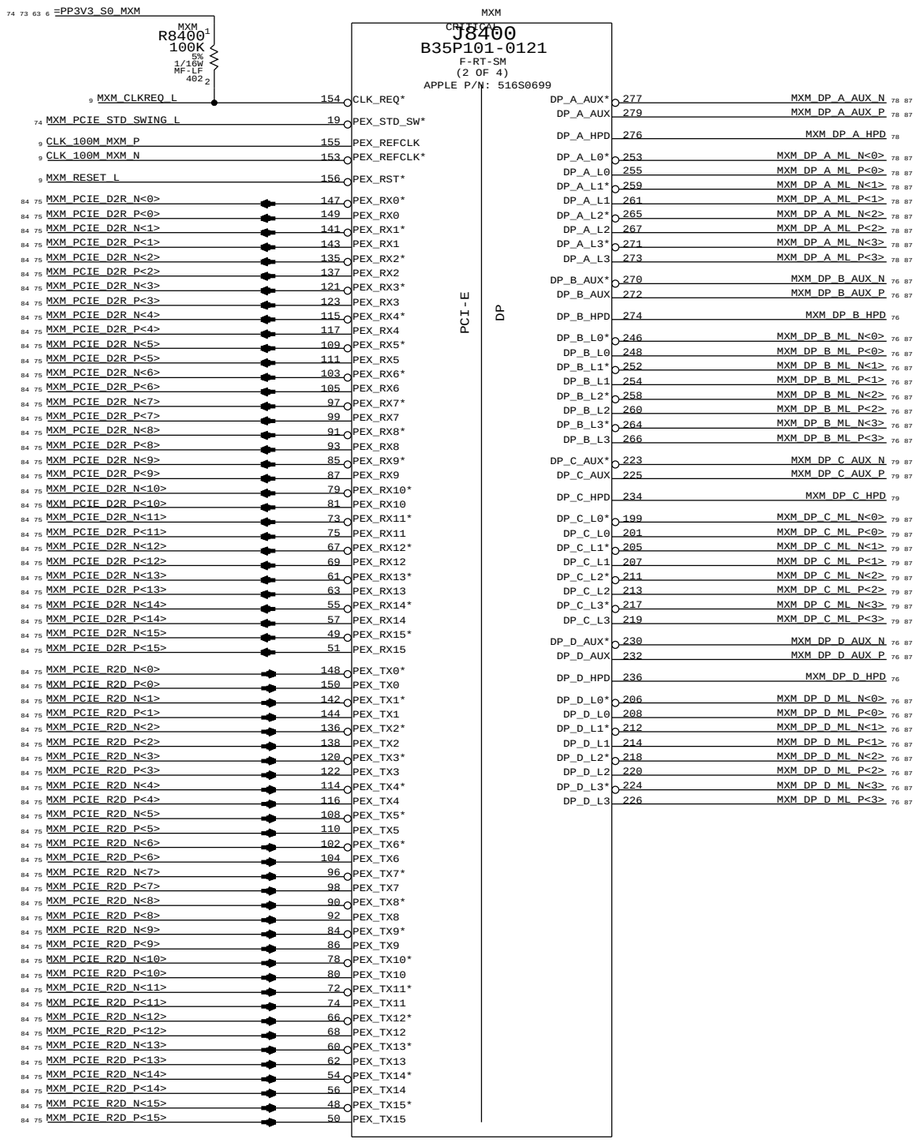
Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP5V_S0_MXM
- =PPV_S0_MXM_PWRSRC

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- MXM



MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.0 A	3.3 W
5V	2.5 A	12.5 W
PWR (7-20V)	UP TO 10 A	PLATFORM DEPENDENT

SYNC MASTER=K75F_MLB SYNC DATE=04/14/2010

PAGE TITLE
MXM PCIe, DP & Power

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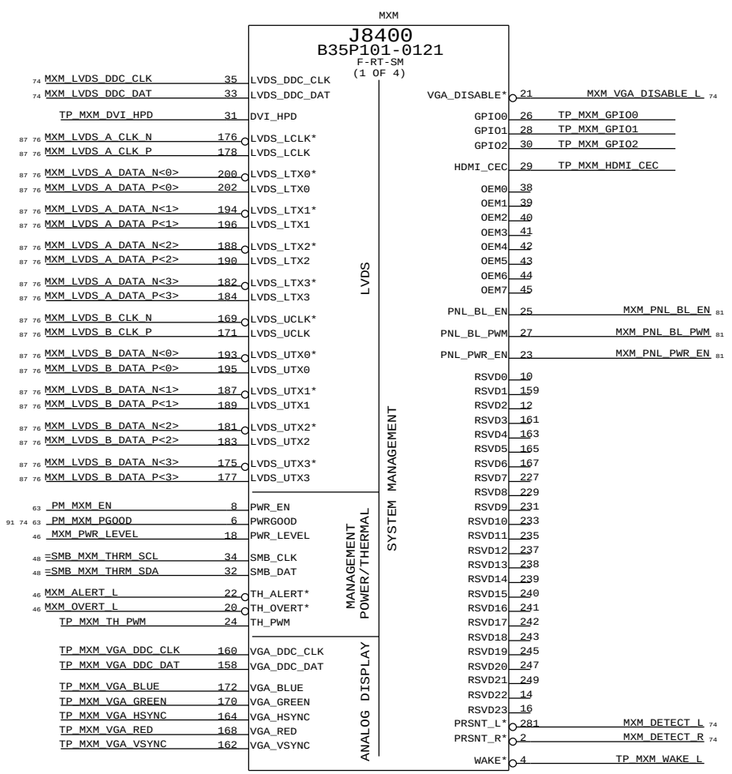
Page Notes

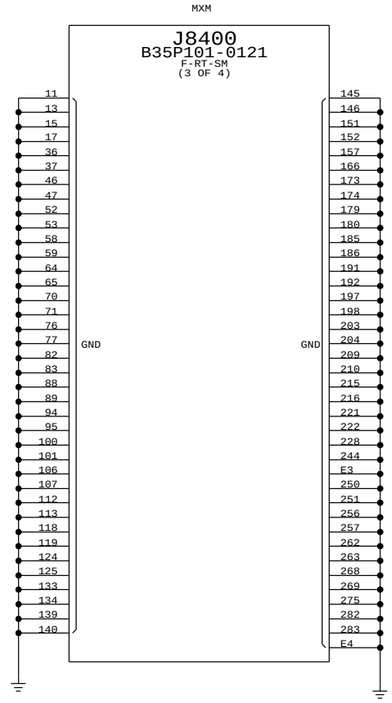
Power aliases required by this page:
- =PP3V3_S0_MXM

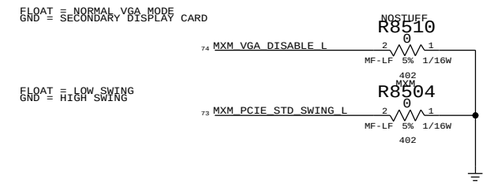
Signal aliases required by this page:
- =SMB_MXM_THRM_DATA - =PM_MXM_PGOOD_PULLUP
- =SMB_MXM_THRM_CLK

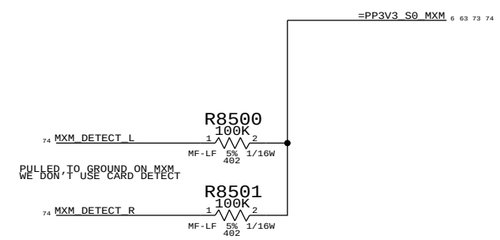
BOM options provided by this page:

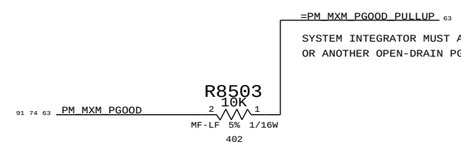
PULLUPS & PULLDOWNS AT MXM CONNECTOR







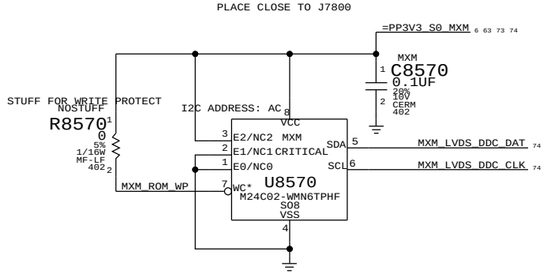




SYSTEM INTEGRATOR MUST ALIAS THIS EITHER TO A VOLTAGE RAIL,
OR ANOTHER OPEN-DRAIN PGOOD SIGNAL DEPENDING ON DESIRED BEHAVIOR

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J7800



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
MXM I/O

Apple Inc.

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MXM TX CAPS

84 9	IN	PEG_R2D_C_P<0>	MXM	C8600	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<15>	OUT 73 84
84 9	IN	PEG_R2D_C_N<0>	MXM	C8601	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<15>	OUT 73 84
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84 9	IN	PEG_R2D_C_P<9>	MXM	C8618	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_P<6>	OUT 73 84
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84 9	IN	PEG_R2D_C_P<15>	MXM	C8631	0.1UF	1	2 10% 16V X5R 402	MXM_PCIE_R2D_N<0>	OUT 73 84

MXM RX CAPS

84 73	IN	MXM_PCIE_D2R_P<15>	MXM	C8632	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<0>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<15>	MXM	C8633	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<0>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<14>	MXM	C8634	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<1>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<14>	MXM	C8635	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<1>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<13>	MXM	C8636	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<2>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<13>	MXM	C8637	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<2>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<12>	MXM	C8638	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<3>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<12>	MXM	C8639	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<3>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<11>	MXM	C8640	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<4>	OUT 9 84
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84 73	IN	MXM_PCIE_D2R_P<8>	MXM	C8646	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<7>	OUT 9 84
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84 73	IN	MXM_PCIE_D2R_P<7>	MXM	C8648	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<8>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<7>	MXM	C8649	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<8>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<6>	MXM	C8650	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<9>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<6>	MXM	C8651	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<9>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<5>	MXM	C8652	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<10>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<5>	MXM	C8653	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<10>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<4>	MXM	C8654	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<11>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<4>	MXM	C8655	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<11>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<3>	MXM	C8656	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<12>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<3>	MXM	C8657	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<12>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<2>	MXM	C8658	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<13>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<2>	MXM	C8659	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<13>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<1>	MXM	C8662	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<14>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<1>	MXM	C8663	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<14>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_P<0>	MXM	C8660	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_N<15>	OUT 9 84
84 73	IN	MXM_PCIE_D2R_N<0>	MXM	C8661	0.1UF	1	2 10% 16V X5R 402	PEG_D2R_P<15>	OUT 9 84

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
MXM PCIE CAPS

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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Page Notes

Power aliases required by this page:
- =PP3V3_S0_DP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Unused MXM Interfaces

87 74	MXM_LVDS_A_CLK_N	NC_MXM_LVDS_A_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_CLK_P	NC_MXM_LVDS_A_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<0>	NC_MXM_LVDS_A_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<0>	NC_MXM_LVDS_A_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<1>	NC_MXM_LVDS_A_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<1>	NC_MXM_LVDS_A_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<2>	NC_MXM_LVDS_A_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<2>	NC_MXM_LVDS_A_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_N<3>	NC_MXM_LVDS_A_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_A_DATA_P<3>	NC_MXM_LVDS_A_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_N	NC_MXM_LVDS_B_CLK_N	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_CLK_P	NC_MXM_LVDS_B_CLK_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<0>	NC_MXM_LVDS_B_DATA_N<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<0>	NC_MXM_LVDS_B_DATA_P<0>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<1>	NC_MXM_LVDS_B_DATA_N<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<1>	NC_MXM_LVDS_B_DATA_P<1>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<2>	NC_MXM_LVDS_B_DATA_N<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<2>	NC_MXM_LVDS_B_DATA_P<2>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_N<3>	NC_MXM_LVDS_B_DATA_N<3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 74	MXM_LVDS_B_DATA_P<3>	NC_MXM_LVDS_B_DATA_P<3>	MAKE_BASE=TRUE NO_TEST=TRUE

Unused MXM DP Interfaces

87 73	MXM_DP_B_ML_P<0..3>	NC_MXM_DP_B_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_ML_N<0..3>	NC_MXM_DP_B_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_AUX_P	NC_MXM_DP_B_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_B_AUX_N	NC_MXM_DP_B_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
73	MXM_DP_B_HPD	NC_MXM_DP_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_ML_P<0..3>	NC_MXM_DP_D_ML_P<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_ML_N<0..3>	NC_MXM_DP_D_ML_N<0..3>	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_AUX_P	NC_MXM_DP_D_AUX_P	MAKE_BASE=TRUE NO_TEST=TRUE
87 73	MXM_DP_D_AUX_N	NC_MXM_DP_D_AUX_N	MAKE_BASE=TRUE NO_TEST=TRUE
73	MXM_DP_D_HPD	NC_MXM_DP_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE

Display: Aliases

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8600	3.0.0

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Page Notes

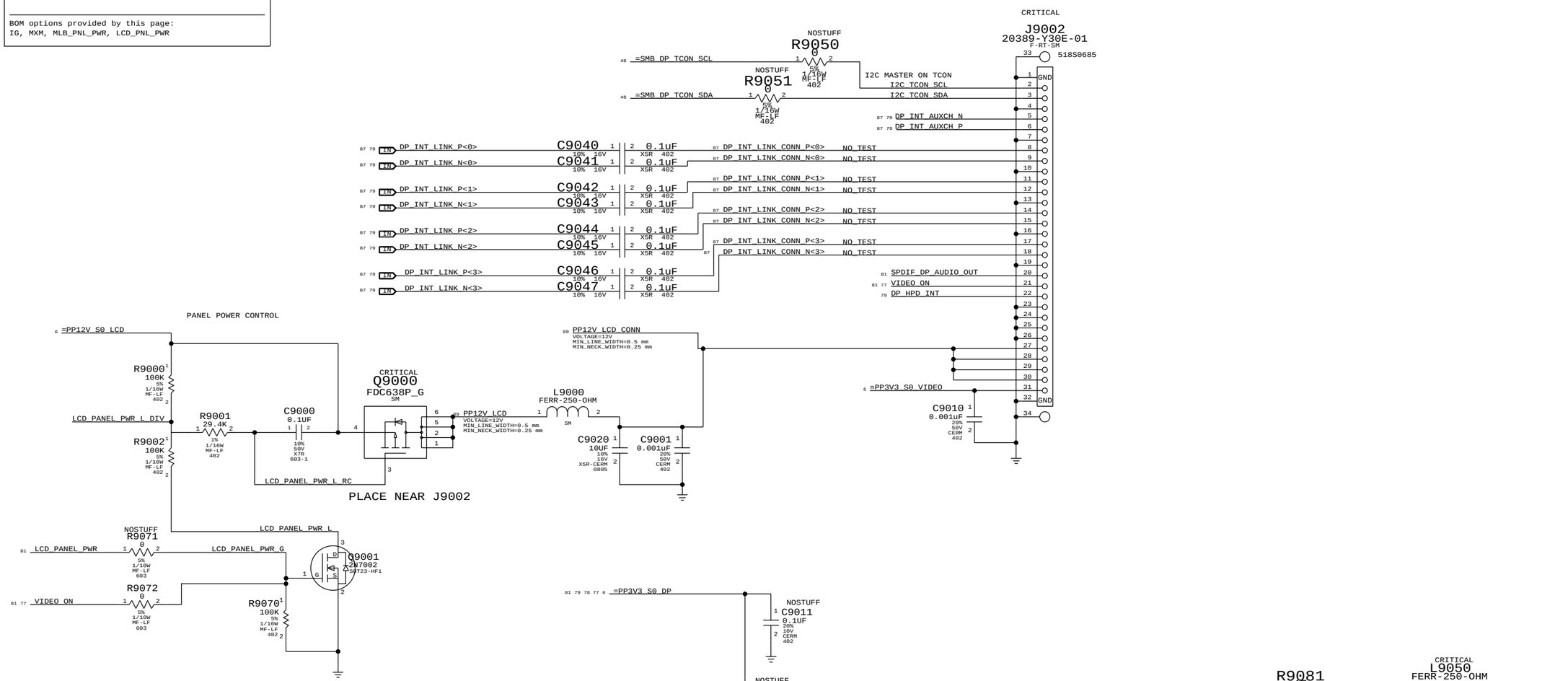
Power aliases required by this page:

- =PP12V_S0_LCD
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
IG, MXM, MLB_PNL_PWR, LCD_PNL_PWR

INTERNAL DP INTERFACE



buffers are multiple parts, other parts are on csa 95

SYNC MASTER=K75F MLB SYNC DATE=04/14/2010

PAGE TITLE
Display: Int DP Connector

Apple Inc.

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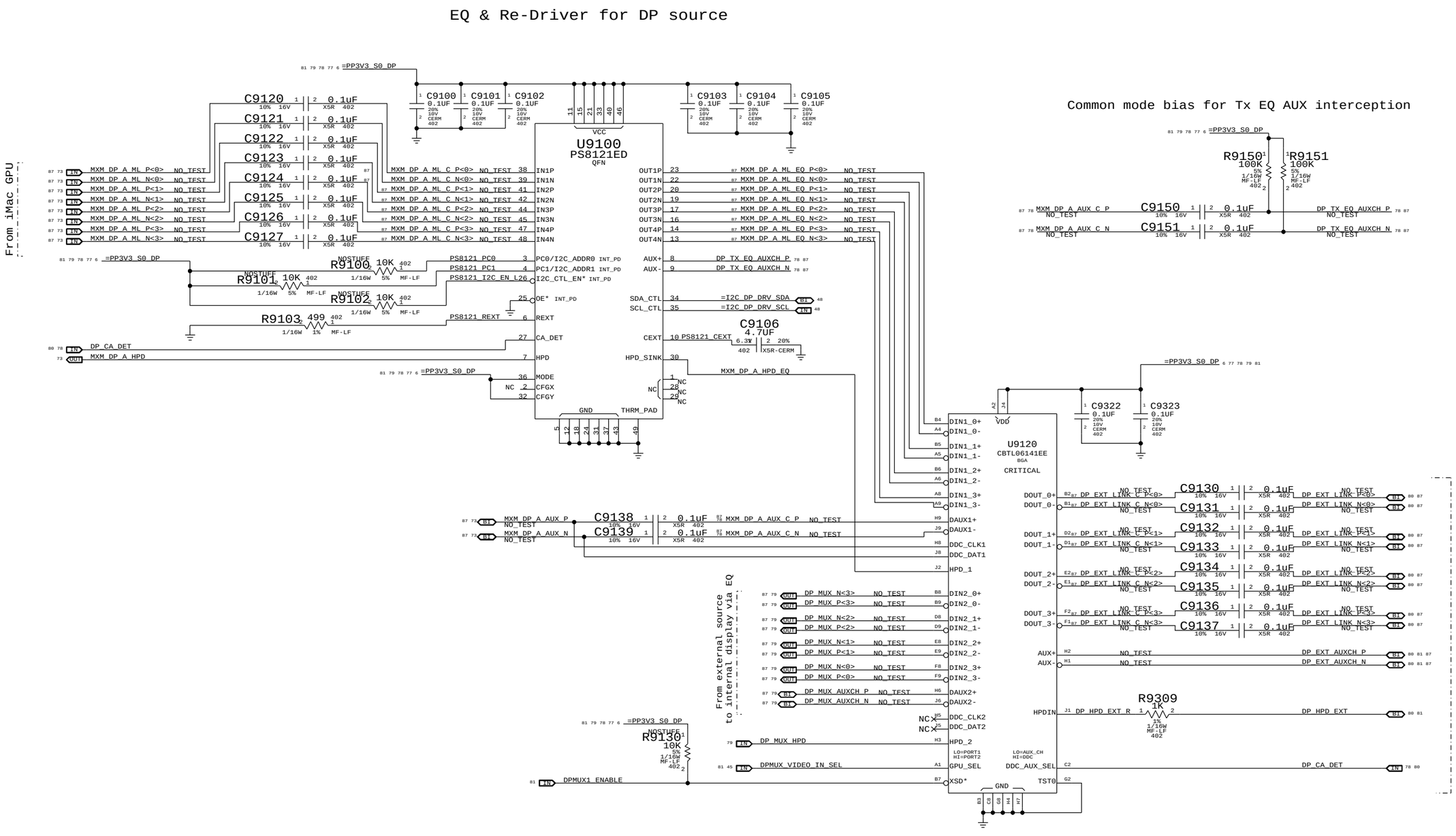

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

Display: BiDiVi Mux1

Apple Inc.

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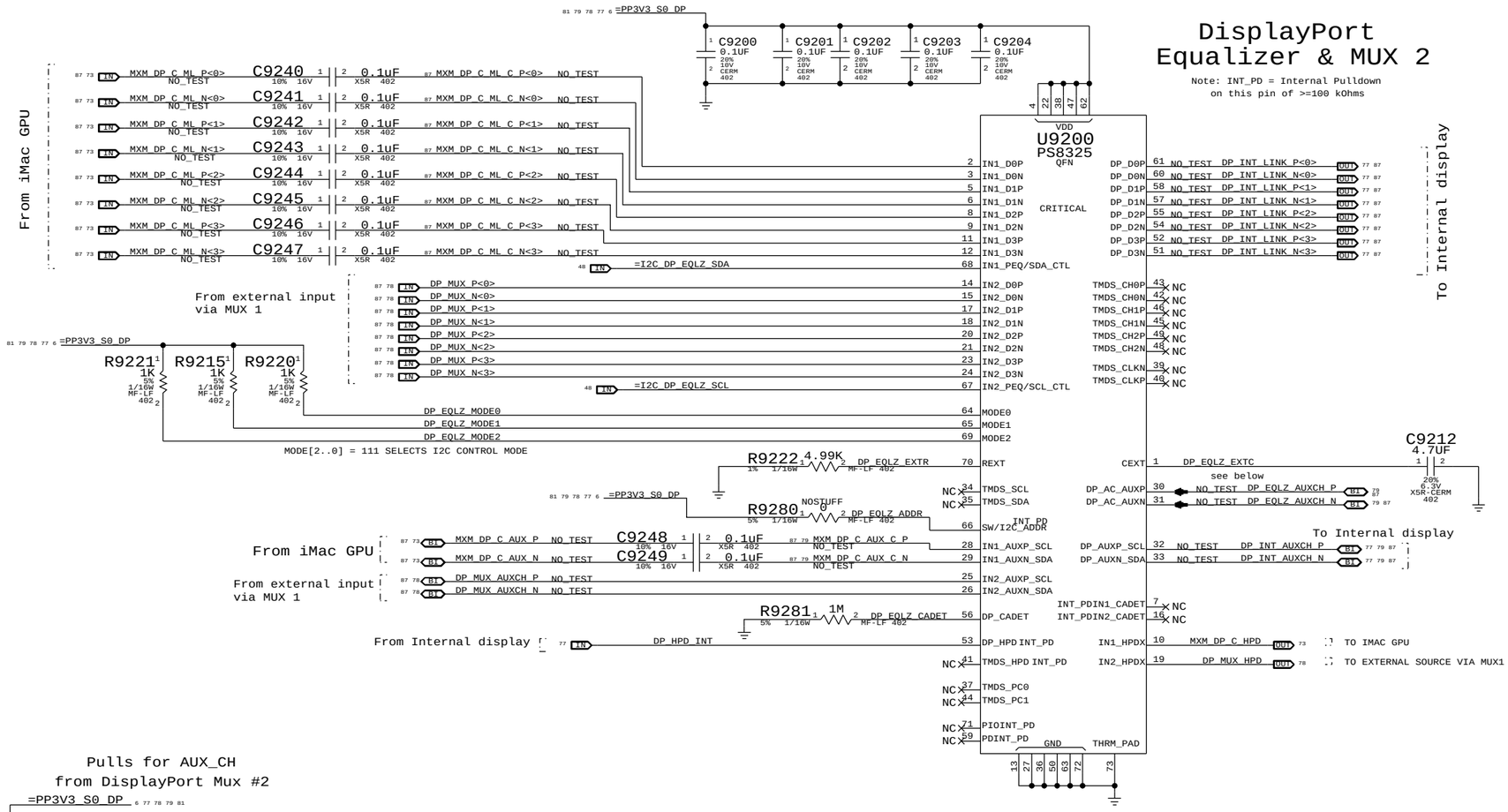
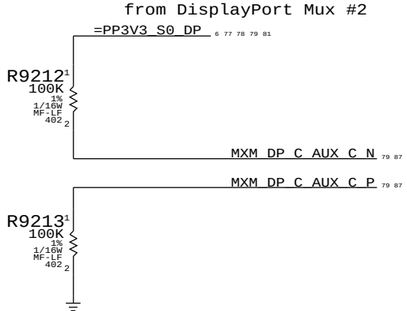
DisplayPort Equalizer & MUX 2

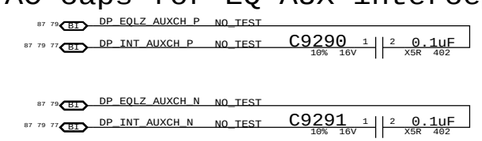
Note: INT_PD = Internal Pulldown on this pin of >=100 kOhms



Pulls for AUX_CH from DisplayPort Mux #2



AC caps for EQ AUX interception



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: BIDIVI DP MUX2

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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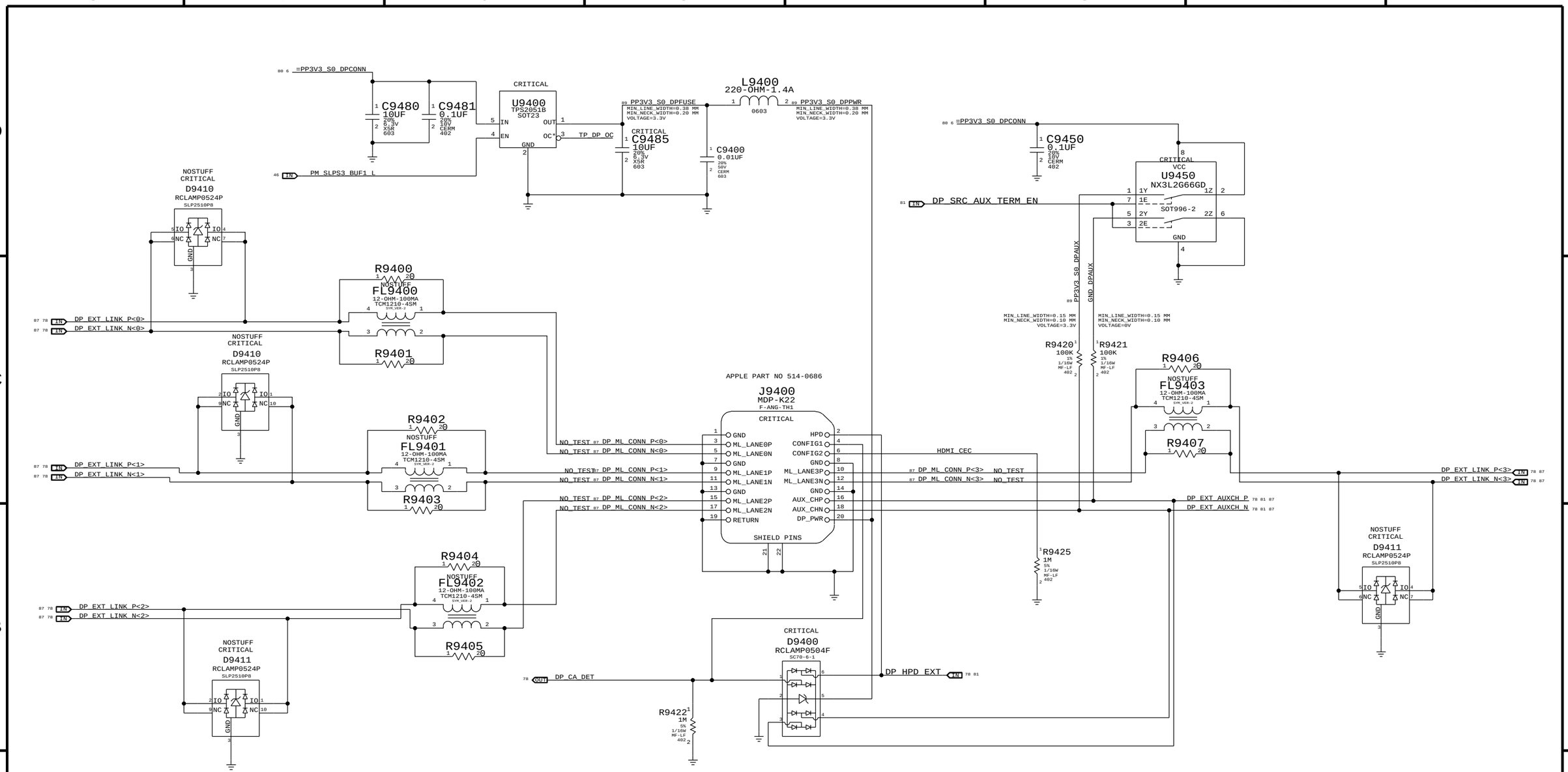

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
Display: Ext DP Connector

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

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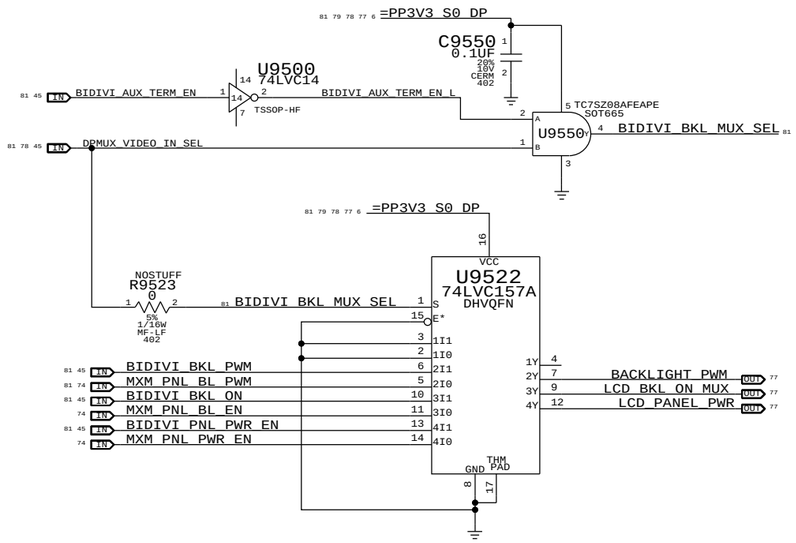
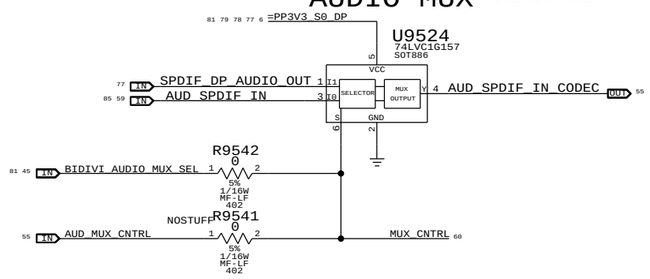
PANEL/BACKLIGHT CONTROL MUX

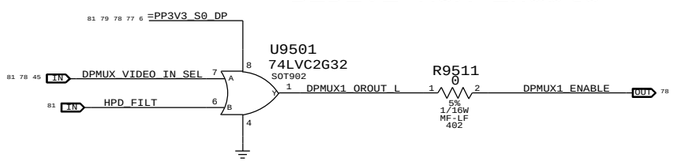


DisplayPort AUDIO MUX

PLACE NEAR U6201

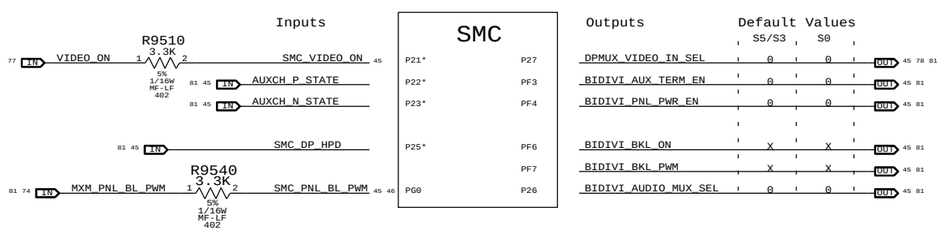


BiDiVi MUX Enable

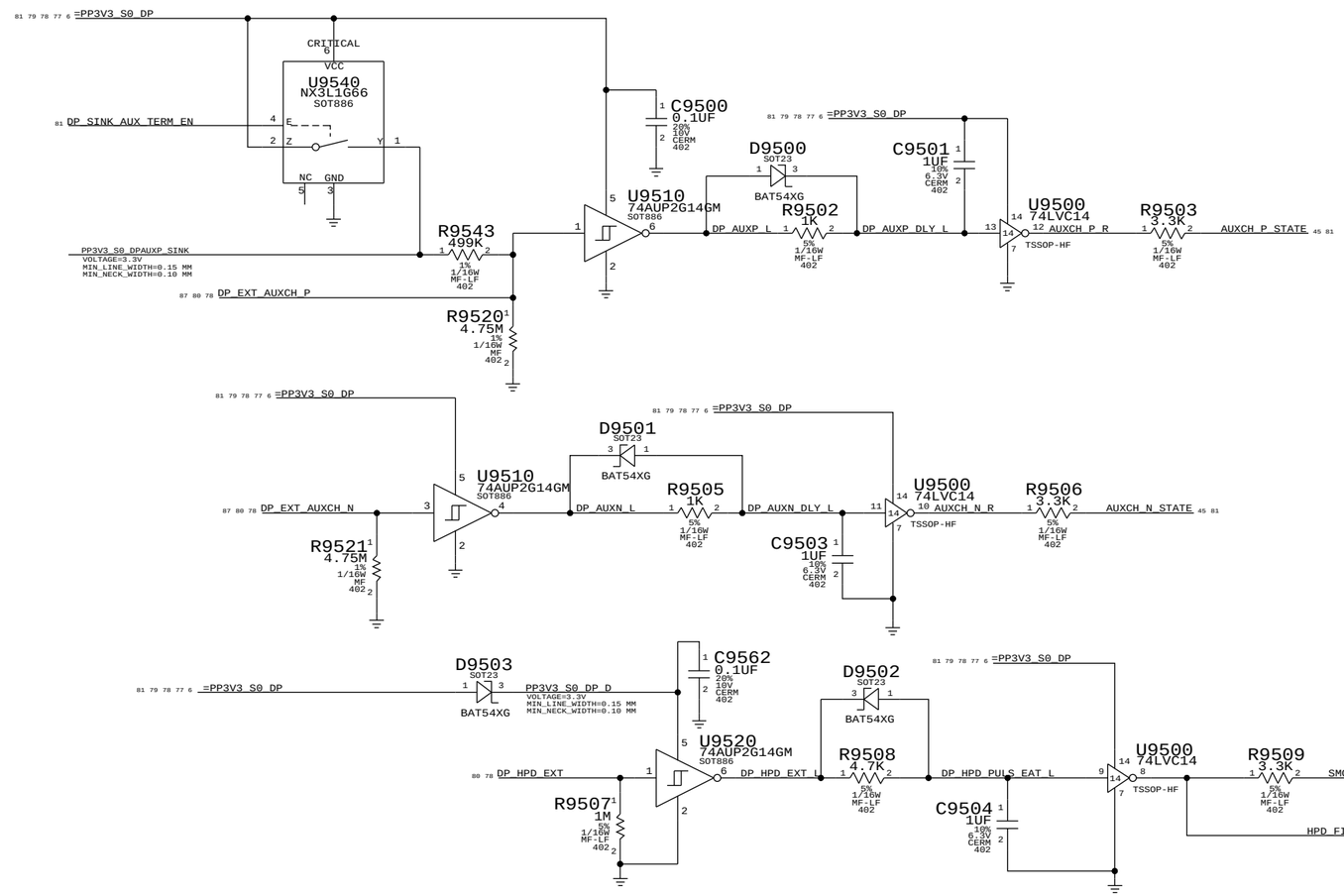


*Some inputs listed below come up as outputs driven low under the SMC flasher
Series R should prevent any issues on the inputs
Ouptuts are OK as low by default

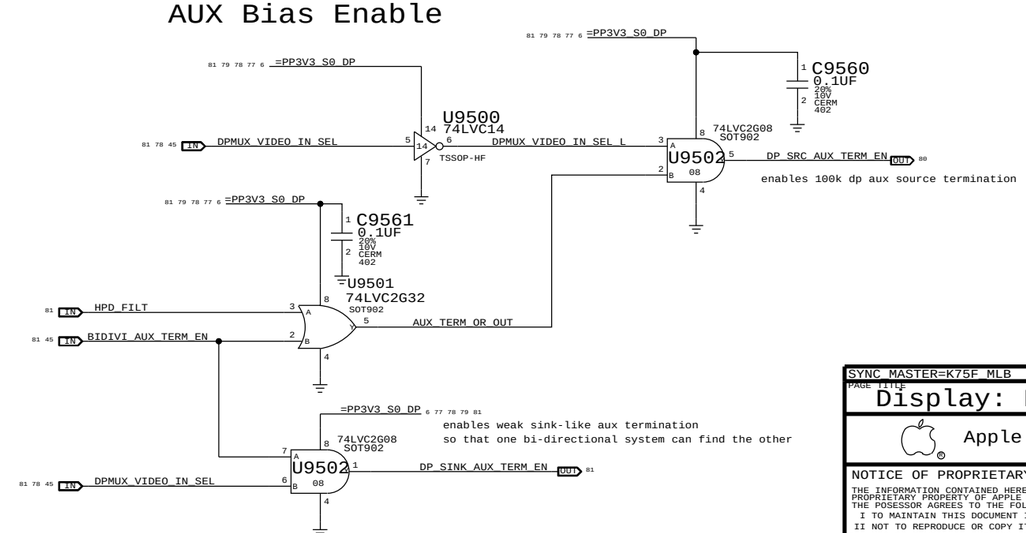
SMC Signals for BiDiVi



External AUX Channel and HPD Buffers & filters



AUX Bias Enable



SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE: Display: BiDiVi Support

Apple Inc.

DRAWING NUMBER: 051-8600 SIZE: D

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K60/K61 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	100 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.21 MM	0.085 MM	=STANDARD		
35_OHM_SE	*	Y	0.19 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD		
39_OHM_SE	*	Y	0.16 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD		
45_OHM_SE	*	Y	0.12 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.1 MM	0.085 MM	15 MM		
50_OHM_SE	*	Y	0.1 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD		
55_OHM_SE	*	Y	0.076 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.155 MM	0.085 MM	=STANDARD	0.135 MM	0.1 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.2 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.085 MM	12 MM	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.110 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.085 MM	=STANDARD	0.25 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.085 MM	=STANDARD	0.320 MM	0.15 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
POWER_WIDTH	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_CTL	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER	BGA_P1MM	POWER_CTL
POWER	*	POWER_WIDTH
VR_CTL_PHY	BGA_P1MM	DEFAULT
VR_CTL_PHY	*	POWER_CTL

SPACING RULE SET

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?
6:1_SPACING	*	0.6 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
GND_P2MM	*	0.2 MM	1000
PWR_P2MM	*	0.2 MM	1000
SWITCHNODE	*	0.8 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.150 MM	?
2X_DIELECTRIC	TOP,BOTTOM	0.160 MM	?
3X_DIELECTRIC	*	0.220 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.240 MM	?
4X_DIELECTRIC	*	0.300 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.320 MM	?
5X_DIELECTRIC	*	0.380 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.400 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	*	*	STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	STANDARD

CONSTRAINTS FOR BGA AREA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	0.2 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P1MM
CLK_LPC	*	BGA_P1MM	BGA_P1MM
CLK_PCI	*	BGA_P1MM	BGA_P1MM

K60/K61 RULE DEFINITIONS

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-8600	3.0.0

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
MEM_35S	*	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=35_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DQ_ODD2DQ_ODD	*	=3:1_SPACING	?
MEM_DQ_ODD2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_EVEN	*	=3:1_SPACING	?
MEM_DQ_EVEN2MEM	*	=3:1_SPACING	?
MEM_DQ_EVEN2DQ_ODD	*	=5:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	=3:1_SPACING	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_ODD	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM
MEM_CLK	MEM_DQ_EVEN	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_ODD	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM
MEM_DQS	MEM_DQ_EVEN	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_ODD	MEM_CLK	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CTRL	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_CMD	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_ODD	*	MEM_DQ_ODD2DQ_ODD
MEM_DQ_ODD	MEM_DQS	*	MEM_DQ_ODD2MEM
MEM_DQ_ODD	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQ_EVEN	MEM_CLK	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CTRL	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_CMD	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_EVEN	*	MEM_DQ_EVEN2DQ_EVEN
MEM_DQ_EVEN	MEM_DQS	*	MEM_DQ_EVEN2MEM
MEM_DQ_EVEN	MEM_DQ_ODD	*	MEM_DQ_EVEN2DQ_ODD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_ODD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQ_EVEN	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DQ_ODD	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM
MEM_CMD	MEM_DQ_EVEN	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DQ_ODD	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER
MEM_DQ_EVEN	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_POWER_WIDTH	*	Y	0.500 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_POWER_PHY	*	MEM_POWER_WIDTH

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_POWER	*	0.2 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_RCOMP_PHY	*	Y	0.175 MM	0.175 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_RCOMP	*	0.2 MM	?

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_CLK	MEM_A_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_A_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_A_CKE<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_CS_L<3..0>	12 30
	MEM_39S	MEM_CTRL	MEM_A_ODT<3..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_A<15..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_BA<2..0>	12 30
	MEM_35S	MEM_CMD	MEM_A_RAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_CAS_L	12 30
	MEM_35S	MEM_CMD	MEM_A_WE_L	12 30
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_A_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_A_DM<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_A_DQS_N<7>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_P<3..0>	12 32
	MEM_70D	MEM_CLK	MEM_B_CLK_N<3..0>	12 32
	MEM_39S	MEM_CTRL	MEM_B_CKE<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_CS_L<3..0>	12 31
	MEM_39S	MEM_CTRL	MEM_B_ODT<3..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_A<15..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_BA<2..0>	12 31
	MEM_35S	MEM_CMD	MEM_B_RAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_CAS_L	12 31
	MEM_35S	MEM_CMD	MEM_B_WE_L	12 31
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<7..0>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<0>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<15..8>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<1>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<23..16>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<2>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<31..24>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<3>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<39..32>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<4>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<47..40>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<5>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DQ<55..48>	12 32
	MEM_45S	MEM_DQ_EVEN	MEM_B_DM<6>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DQ<63..56>	12 32
	MEM_45S	MEM_DQ_ODD	MEM_B_DM<7>	12 32

MEMORY POWER PROPERTIES

VOLTAGE	NET_TYPE PHYSICAL	NET_TYPE SPACING		
H150	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A	12 28
H154	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B	12 28
H160	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMA_DQ	28
H167	MEM_POWER_PHY	MEM_POWER	VREFMARGIN_DIMMB_DQ	28
H169	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_A_SW	28
H168	MEM_POWER_PHY	MEM_POWER	CPU_DIMM_VREF_B_SW	28

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MEM_70D	MEM_DQS	MEM_B_DQS_P<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<0>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<1>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<2>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<3>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<4>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<5>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<6>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_P<7>	12 32
	MEM_70D	MEM_DQS	MEM_B_DQS_N<7>	12 32
H150	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP0	11
H150	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP1	11
H150	MEM_RCOMP_PHY	MEM_RCOMP	CPU_SM_RCOMP2	11
H162	MEM_70D	MEM_DQS	TP_MEM_B_DQS_P<8>	8 12
H162	MEM_70D	MEM_DQS	TP_MEM_B_DQS_N<8>	8 12
H162	MEM_70D	MEM_DQS	TP_MEM_A_DQS_P<8>	8 12
H162	MEM_70D	MEM_DQS	TP_MEM_A_DQS_N<8>	8 12

ADD RULES TO NC_DQS<8>
TO CLEAR CHECK_PLUS ERRORS

SYNC MASTER=K75F MLB SYNC DATE=04/14/2010

PAGE TITLE
Memory Constraints

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PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=4X_DIELECTRIC	?
CLK_PCIE	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

CPU

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_ITP	*	0.2 MM	?
CPU_RCOMP	*	0.2 MM	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=5X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=5X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FDI_MISC				
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	
	CPU_50S	CPU_AGTL	FDI_INT	
SATA SSD				
	SATA_85D	SATA	SATA_SSD_R2D_C_P	18 42
	SATA_85D	SATA	SATA_SSD_R2D_C_N	18 42
	SATA_85D	SATA	SATA_SSD_R2D_P	42
	SATA_85D	SATA	SATA_SSD_R2D_N	42
	SATA_85D	SATA	SATA_SSD_D2R_P	18 42
	SATA_85D	SATA	SATA_SSD_D2R_N	18 42
	SATA_85D	SATA	SATA_SSD_D2R_C_P	42
	SATA_85D	SATA	SATA_SSD_D2R_C_N	42
CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_P	10 18
	CLK_PCIE_100D	CLK_PCIE	DMI_MIDBUS_CLK100M_N	10 18
CPU ITP				
	CPU_50S	CPU_ITP	XDP_BPM_L<7..0>	11 25
	CPU_50S	CPU_ITP	CPU_CFG<17..0>	10 15 25
	CPU_50S	CPU_ITP	XDP_OBSDATA_A<3..0>	25
CPU_MISC				
	CPU_50S	CPU_RCOMP	CPU_PEG_COMP	10
	CPU_50S	CPU_RCOMP	CPU_PEG_RBIAS	10
	CPU_50S	CPU_RCOMP	CPU_COMP3	11
	CPU_50S	CPU_RCOMP	CPU_COMP2	11
	CPU_50S	CPU_RCOMP	CPU_COMP1	11
	CPU_50S	CPU_RCOMP	CPU_COMP0	11

ANY OTHER LYNNFIELD CONSTRAINTS NOT COVERED ON PAGES 101 AND 107 SHOULD GO ON THIS PAGE TOO

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE GRAPHICS				
	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	9 75
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	9 75
	PCIE_85D	PCIE	PEG_D2R_P<15..0>	9 75
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	9 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_P<15..0>	73 75
	PCIE_85D	PCIE	MXM_PCIE_R2D_N<15..0>	73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_P<15..0>	73 75
	PCIE_85D	PCIE	MXM_PCIE_D2R_N<15..0>	73 75
PCIE I/O				
	PCIE_85D	PCIE	PCIE_MINI_R2D_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_N	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_C_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_P	18 33
	PCIE_85D	PCIE	PCIE_MINI_D2R_N	18 33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_P	33
	PCIE_85D	PCIE	PCIE_MINI_R2D_L_N	33
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	18 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_P	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	18 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
DMI				
	PCIE_85D	PCIE	DMI_S2N_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_S2N_N<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_P<3..0>	10 19
	PCIE_85D	PCIE	DMI_N2S_N<3..0>	10 19
FDI				
	PCIE_85D	PCIE	FDI_DATA_N<7..0>	
	PCIE_85D	PCIE	FDI_DATA_P<15..0>	
PCIE REF CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	9
	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	9
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_P	33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CON_N	33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	18 33
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	18 39
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	18 39
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_P	18 36
	ENET_100D	ENET_MII	PCIE_CLK100M_ENET_N	18 36
SATA				
	SATA_85D	SATA	SATA_HDD_R2D_C_P	18 42
	SATA_85D	SATA	SATA_HDD_R2D_C_N	18 42
	SATA_85D	SATA	SATA_HDD_R2D_P	42 92
	SATA_85D	SATA	SATA_HDD_R2D_N	42 92
	SATA_85D	SATA	SATA_HDD_D2R_P	18 42
	SATA_85D	SATA	SATA_HDD_D2R_N	18 42
	SATA_85D	SATA	SATA_HDD_D2R_C_P	42 92
	SATA_85D	SATA	SATA_HDD_D2R_C_N	42 92
	SATA_85D	SATA	SATA_ODD_R2D_C_P	18 42
	SATA_85D	SATA	SATA_ODD_R2D_C_N	18 42
	SATA_85D	SATA	SATA_ODD_R2D_P	42 92
	SATA_85D	SATA	SATA_ODD_R2D_N	42 92
	SATA_85D	SATA	SATA_ODD_D2R_P	18 42
	SATA_85D	SATA	SATA_ODD_D2R_N	18 42
	SATA_85D	SATA	SATA_ODD_D2R_C_P	42 92
	SATA_85D	SATA	SATA_ODD_D2R_C_N	42 92
CLOCKS				
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_P	11 21
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_CPU_N	11 21
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	11 18
	CLK_PCIE_100D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	11 18
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_P	11 25
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_ITP_N	11 25
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_P	11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_CPU_N	11 18
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_P	18 26
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_PCH_N	18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_P	18 26
	CLK_PCIE_100D	CLK_PCIE	FSB_CLK133M_PCH_N	18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_P	18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK96M_DOT_N	
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_P	18 26
	CLK_PCIE_100D	CLK_PCIE	PCH_CLK100M_SATA_N	18 26

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
PCIE/DMI/FDI/SATA CONSTRAINTS

Apple Inc.

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PCH CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH	*	0.2 MM	?
COMP_PCH	*	0.2 MM	?

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	0.2 MM	?

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	0.15 MM	?
CLK_LPC	*	0.2 MM	?

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	0.2 MM	?

XTAL Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL	*	=4X_DIELECTRIC	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_REQ0_L	20
	PCI_55S	PCI	PCI_REQ1_L	20
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIOUT	20 27
	CLK_PCI_55S	CLK_PCI	PCH_CLK33M_PCIIN	18 27
	LPC_55S	LPC	LPC_AD<3..0>	18 45 47
	LPC_55S	LPC	LPC_FRAME_L	18 45 47
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC_R	20 27
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_SMC	27 45
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS	27 47
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK_R	9 19 91
	CLK_LPC_55S	PM	PM_CLK32K_SUSCLK	9 45 91
	CLK_LPC_55S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 27
	USB_90D	USB	USB_EXTA_P	34 43
	USB_90D	USB	USB_EXTA_N	34 43
	USB_90D	USB	USB_PORT0_P	43
	USB_90D	USB	USB_PORT0_N	43
	USB_90D	USB	USB_EXTB_P	35 43
	USB_90D	USB	USB_EXTB_N	35 43
	USB_90D	USB	USB_PORT1_P	43
	USB_90D	USB	USB_PORT1_N	43
	USB_90D	USB	USB_EXTC_P	34 43
	USB_90D	USB	USB_EXTC_N	34 43
	USB_90D	USB	USB_PORT2_P	43
	USB_90D	USB	USB_PORT2_N	43
	USB_90D	USB	USB_EXTD_P	35 43
	USB_90D	USB	USB_EXTD_N	35 43
	USB_90D	USB	USB_D_MUXED_P	43
	USB_90D	USB	USB_D_MUXED_N	43
	USB_90D	USB	USB_PORT3_P	43
	USB_90D	USB	USB_PORT3_N	43
	USB_90D	USB	USB_CAMERA_P	34 44
	USB_90D	USB	USB_CAMERA_N	34 44
	USB_90D	USB	USB_CAMERA_L_P	44 92
	USB_90D	USB	USB_CAMERA_L_N	44 92
	USB_90D	USB	USB_BT_P	35 44
	USB_90D	USB	USB_BT_N	35 44
	USB_90D	USB	USB_BT_L_P	44 92
	USB_90D	USB	USB_BT_L_N	44 92
	USB_90D	USB	USB_IR_P	34 44
	USB_90D	USB	USB_IR_N	34 44
	USB_90D	USB	USB_IR_L_P	44 92
	USB_90D	USB	USB_IR_L_N	44 92
	USB_90D	USB	USB_SDCARD_P	35 44
	USB_90D	USB	USB_SDCARD_N	35 44
	USB_90D	USB	USB_SDCARD_L_P	44 92
	USB_90D	USB	USB_SDCARD_L_N	44 92
	USB_90D	USB	USB_WM_P	20 44
	USB_90D	USB	USB_WM_N	20 44
	USB_90D	USB	USB_WM_L_P	44
	USB_90D	USB	USB_WM_L_N	44
	USB_90D	USB	USB_MINI_P	
	USB_90D	USB	USB_MINI_N	
	USB_90D	USB	USB_BRCRYPT_P	20 44
	USB_90D	USB	USB_BRCRYPT_N	20 44
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 27
	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 27
	CLK_XTAL	XTAL	CK505_XTAL_IN	26
	CLK_XTAL	XTAL	CK505_XTAL_OUT	26
	CLK_PCH_55S	CLK_PCH	PCH_CLK14P3M_REFCLK	18 26
	USB_90D	USB	USB_BRCRYPT_L_P	44
	USB_90D	USB	USB_BRCRYPT_L_N	44
	USB_90D	USB	USB_HUB1_UP_P	20 34
	USB_90D	USB	USB_HUB1_UP_N	20 34
	USB_90D	USB	USB_HUB2_UP_P	20 35
	USB_90D	USB	USB_HUB2_UP_N	20 35

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SPI_55S	SPI	SPI_CLK_R	18 47 54
	SPI_55S	SPI	SPI_CLK	54
	SPI_55S	SPI	SPI_MOSI_R	18 47 54
	SPI_55S	SPI	SPI_MOSI	54
	SPI_55S	SPI	SPI_MISO	18 47 54
	SPI_55S	SPI	SPI_MISO_R	54
	SPI_55S	SPI	SPI_CS0_R_L	18 47
	SPI_55S	SPI	SPI_CS0_L	47
	SPI_55S	SPI	SPI_MLB_CS_L	47 54
	SPI_55S	SPI	SPI_ALT_CS_L	47
	SPI_55S	SPI	SPIROM_USE_MLB	21 47
	SPI_55S	SPI	SPI_ALT_MOSI	47
	SPI_55S	SPI	SPI_ALT_MISO	47
	SPI_55S	SPI	SPI_ALT_CLK	47
	HDA_55S	HDA	HDA_BIT_CLK	18 55
	HDA_55S	HDA	HDA_BIT_CLK_R	18
	HDA_55S	HDA	HDA_RST_L	18 55
	HDA_55S	HDA	HDA_RST_R_L	18
	HDA_55S	HDA	HDA_SDOUT	18 55
	HDA_55S	HDA	HDA_SDOUT_R	18
	HDA_55S	HDA	HDA_SYNC	18 55
	HDA_55S	HDA	HDA_SYNC_R	18
	HDA_55S	HDA	HDA_SDIN0	18 55
	HDA_55S	HDA	AUD_SDI_R	55
		HDA	AUD_SPDIF_IN	59 81
		HDA	AUD_SPDIF_OUT	55 59
		HDA	AUD_SPDIF_CHIP	55
	HDA_55S	HDA	AUD_SPKR_OUTL01L_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL01L_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL01R_NOUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL01R_POUT	57 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02L_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02L_POUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02R_NOUT	58 59 92
	HDA_55S	HDA	AUD_SPKR_OUTL02R_POUT	58 59 92
	CLK_XTAL	XTAL	PCH_CLK25M_XTALOUT	18 27
	CLK_XTAL	XTAL	PCH_CLK25M_XTALIN	18 27
	PCH_55S	COMP_PCH	PCH_USB_RBIAS	20
	PCH_55S	COMP_PCH	PCH_SATAICOMP	18
	PCH_55S	COMP_PCH	PCH_XCLK_RCOMP	18
	PCH_55S	COMP_PCH	PCH_DMI_COMP	19
	CLK_XTAL	XTAL	USB_HUB1_XTAL1	34
	CLK_XTAL	XTAL	USB_HUB1_XTAL2	34
	PCH_55S	COMP_PCH	USB_HUB1_RBIAS	34
	CLK_XTAL	XTAL	USB_HUB2_XTAL1	35
	CLK_XTAL	XTAL	USB_HUB2_XTAL2	35
	PCH_55S	COMP_PCH	USB_HUB2_RBIAS	35

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE
IBEX PEAK CONSTRAINTS

Apple Inc.

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CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	0.3 MM	?
ENET_SE	*	=STANDARD	?

SOURCE:BROADCOM 5764M-DS04-RDS. PAGE 38

CAESAR II (ETHERNET) CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF	*	0.6 MM	?

SOURCE: BROADCOM 5764-DS04-RDS. PAGE 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_PHY	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=STANDARD	?

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_SE	ENET_RDAC	36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTALI	36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTALO	36
	ENET_50S	BUF0_CLK	ENET_CLK25M_XTAL	36
	ENET_100D	ENET_DIFF	ENET_MDI_P<3..0>	36 38
	ENET_100D	ENET_DIFF	ENET_MDI_N<3..0>	36 38
	ENET_100D	ENET_DIFF	ENET_MDI_T_P<3..0>	38
	ENET_100D	ENET_DIFF	ENET_MDI_T_N<3..0>	38
	ENET_100D	ENET_MII	PCIE_ENET_R2D_P	36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_N	36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_P	18 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_N	18 36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_P	18 36
	ENET_100D	ENET_MII	PCIE_ENET_R2D_C_N	18 36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_P	36
	ENET_100D	ENET_MII	PCIE_ENET_D2R_C_N	36

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	FW_110D	FW_TP	FW_PORT0_TPA_P	40 41
	FW_110D	FW_TP	FW_PORT0_TPA_N	40 41
	FW_110D	FW_TP	FW_PORT0_TPB_P	40 41
	FW_110D	FW_TP	FW_PORT0_TPB_N	40 41
PORT 1 & 2 NOT USED				
	FW_110D	FW_TP	FW_P0_TPA_L_P	40
	FW_110D	FW_TP	FW_P0_TPA_L_N	40
	FW_110D	FW_TP	FW_P0_TPB_L_P	40
	FW_110D	FW_TP	FW_P0_TPB_L_N	40

UNUSED FW NETS PHYSICAL PROPERTIES

	FW_110D	FW_TP	FW_P1_TPA_P	39 40
	FW_110D	FW_TP	FW_P1_TPA_N	39 40
	FW_110D	FW_TP	FW_P2_TPA_P	39 40
	FW_110D	FW_TP	FW_P2_TPA_N	39 40

AUDIO MIC PHYSICAL PROPERTIES

	AUDIO_PHY	AUDIO	AUD_MIC1_IN_N	59 60
	AUDIO_PHY	AUDIO	AUD_MIC1_IN_P	59 60

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2016

PAGE TITLE
ENET/FIREWIRE CONSTRAINTS

Apple Inc.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3:1_SPACING	?

PAIRS SHOULD BE WITHIN 100 MILS OF CLOCK LENGTH.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
ASSINGED IN CONT. MGR.				
	DP_85D	DISPLAYPORT	DP_ML_CONN_P<3..0>	80
	DP_85D	DISPLAYPORT	DP_ML_CONN_N<3..0>	80
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_P<3..0>	77
	DP_85D	DISPLAYPORT	DP_INT_LINK_CONN_N<3..0>	77
	DP_85D	DISPLAYPORT	DP_INT_LINK_P<3..0>	77 79
	DP_85D	DISPLAYPORT	DP_INT_LINK_N<3..0>	77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_P	77 79
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_N	77 79
	DP_85D	DISPLAYPORT	DP_EXT_LINK_P<3..0>	78 80
	DP_85D	DISPLAYPORT	DP_EXT_LINK_N<3..0>	78 80
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_P	78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_AUXCH_N	78 80 81
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_P<3..0>	78
	DP_85D	DISPLAYPORT	DP_EXT_LINK_C_N<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_P<3..0>	73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_N<3..0>	73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_P	78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_C_N	78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_P	73 78
	DP_85D	DISPLAYPORT	MXM_DP_A_AUX_N	73 78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_P<3..0>	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_N<3..0>	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_P	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_N	73 79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_P	79
	DP_85D	DISPLAYPORT	MXM_DP_C_AUX_C_N	79
	DP_85D	DISPLAYPORT	DP_MUX_P<3..0>	78 79
	DP_85D	DISPLAYPORT	DP_MUX_N<3..0>	78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_P	78 79
	DP_85D	DISPLAYPORT	DP_MUX_AUXCH_N	78 79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_P	79
	DP_85D	DISPLAYPORT	DP_EQLZ_AUXCH_N	79
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_P<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_C_N<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_P<3..0>	79
	DP_85D	DISPLAYPORT	MXM_DP_C_ML_C_N<3..0>	79
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_P	78
	DP_85D	DISPLAYPORT	DP_TX_EQ_AUXCH_N	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_P<3..0>	78
	DP_85D	DISPLAYPORT	MXM_DP_A_ML_EQ_N<3..0>	78

UNUSED VIDEO NET PHYSICAL CONSTRAINTS

	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_P	73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_AUX_N	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_P	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_AUX_N	73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_P	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_CLK_N	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_P	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_CLK_N	74 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_P<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_DP_B_ML_N<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_P<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_DP_D_ML_N<3..0>	73 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_P<3..0>	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_A_DATA_N<3..0>	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_P<3..0>	74 76
	DP_85D	DISPLAYPORT	MXM_LVDS_B_DATA_N<3..0>	74 76

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

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GRAPHICS CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

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SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	4:1_SPACING
THERMAL	POWER	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR
SNS_DIFF	*	1:1_DIFFPAIR

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	48
	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	48
	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	48
	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	48
	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	48
	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	48
	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	48
	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	48
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	48 88
	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	48 88
I130	SMB_55S	SMB	SMBUS_PCH_S0_CLK	48
I131	SMB_55S	SMB	SMBUS_PCH_S0_DATA	48
I160	SMB_55S	SMB	SMBUS_PCH_CLK	18 48
I161	SMB_55S	SMB	SMBUS_PCH_DATA	18 48
I137	SMB_55S	SMB	SML_PCH_0_CLK	18 48
I139	SMB_55S	SMB	SML_PCH_0_DATA	18 48
I138	SMB_55S	SMB	SML_PCH_1_CLK	18 48
I140	SMB_55S	SMB	SML_PCH_1_DATA	18 48
I197	CLK_XTAL	XTAL	SMC_EXTAL	45 46
I198	CLK_XTAL	XTAL	SMC_XTAL	45 46

SMC THERMAL NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I87	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I88	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I89	THERM_DIFF	THERMAL	SNS_T_DP2_DN3	51
I90	THERM_DIFF	THERMAL	SNS_T_DN2_DP3	51
I200	THERM_DIFF	THERMAL	SNS_T_DN1_DP6	51 88
I201	THERM_DIFF	THERMAL	SNS_T_DP1_DN6	51 88
I93	THERM_DIFF	THERMAL	SNS_T_DP4_DN5	51
I94	THERM_DIFF	THERMAL	SNS_T_DN4_DP5	51
I101	THERM_DIFF	THERMAL	SNS_LCD_P	51 92
I102	THERM_DIFF	THERMAL	SNS_LCD_N	51 92
I103	THERM_DIFF	THERMAL	SNS_ODD_P	51 92
I105	THERM_DIFF	THERMAL	SNS_ODD_N	51 92
I104	THERM_DIFF	THERMAL	SNS_CPU_H_P	51
I106	THERM_DIFF	THERMAL	SNS_CPU_H_N	51
I191	THERM_DIFF	THERMAL	SNS_SKIN_P	51 92
I195	THERM_DIFF	THERMAL	SNS_SKIN_N	51 92
I109	THERM_DIFF	THERMAL	SNS_AMB_P	51 92
I110	THERM_DIFF	THERMAL	SNS_AMB_N	51 92
I111	THERM_DIFF	THERMAL	SNS_MXM_P	51
I112	THERM_DIFF	THERMAL	SNS_MXM_N	51
I192	THERM_DIFF	THERMAL	SNS_CPU_THERMD_P	10 51
I193	THERM_DIFF	THERMAL	SNS_CPU_THERMD_N	10 51
I115		THERMAL	HDD_OOB_TEMP_FILT	51 92
I133		THERMAL	HDD_OOB_TEMP	51
I134		THERMAL	HDD_OOB_TEMP_R	51
I132		THERMAL	SMC_HDD_OOB_TEMP	51

SMC VOLTAGE/CURRENT NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I07	THERM_DIFF	THERMAL	MXM_ISENSE_P	50
I08	THERM_DIFF	THERMAL	MXM_ISENSE_N	50
I09	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_P	49
I160	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S3_N	49
I148	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_P	49
I149	THERM_DIFF	THERMAL	SENSE_CPU_1V5_S0_N	49
I150	THERM_DIFF	THERMAL	SENSE_CPU_1V5_P	49
I151	THERM_DIFF	THERMAL	SENSE_CPU_1V5_N	49
I152	THERM_DIFF	THERMAL	SENSE_CPU_VTT_P	49
I153	THERM_DIFF	THERMAL	SENSE_CPU_VTT_N	49
I181	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_P	
I182	THERM_DIFF	THERMAL	SENSE_CPU_VTT1_N	
I183	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_P	
I184	THERM_DIFF	THERMAL	SENSE_CPU_VTT2_N	
I160		THERMAL	GND_SMC_AVSS	45 46 49 50
I162		THERMAL	SMC_CPU_1V5_ISENSE	46 49
I163		THERMAL	SMC_CPU_1V5_ISENSE_R	49
I172		THERMAL	SMC_CPU_1V5_VSENSE	46 49
I165		THERMAL	SMC_CPU_VTT_ISENSE	46 49
I166		THERMAL	SMC_CPU_VTT_ISENSE_R	49
I168		THERMAL	SMC_CPU_VTT_VSENSE	46 49
I169		THERMAL	SMC_CPU_1V8_ISENSE	46 49
I167		THERMAL	SMC_CPU_1V8_ISENSE_R	
I170		THERMAL	SMC_CPU_1V8_VSENSE	46 49
I120		THERMAL	SMC_CPU_VSENSE	45 49
I118	VID_PHY	VR_CTL	VR_CPU_IOUT	13 64
I131	THERM_DIFF	THERMAL	VR_ISNS_CPU_P	49
I130	THERM_DIFF	THERMAL	VR_ISNS_CPU_N	49
I125		THERMAL	SNS_PS_CPU_ISNS	49
I114		THERMAL	SMC_CPU_ISENSE	45 49
I160		THERMAL	SMC_CPU_INPUT_ISENSE	46
I171		THERMAL	SMC_CPU_INPUT_VSENSE	46
I172		THERMAL	SMC_DIMM_1V5_ISENSE	46 50
I173		THERMAL	SMC_1V5_S3_ISENSE_R	
I174		THERMAL	SMC_DIMM_1V5_VSENSE	46 50
I170		THERMAL	SMC_GPU_ISENSE	45 50
I170		THERMAL	SMC_MXM_ISENSE_R	50
I180		THERMAL	SMC_GPU_VSENSE	45 50

SYNC_MASTER=K75F_MLB SYNC_DATE=04/14/2010

PAGE TITLE

SMC Constraints

Apple Inc.

DRAWING NUMBER 051-8600 SIZE D

REVISION A.0.0

BRANCH

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NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SWITCHNODE	SWITCHNODE	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	BGA_P1MM	BGA_P2MM
SWITCHNODE	GND	BGA_P1MM	BGA_P2MM
SWITCHNODE	*	BGA_P1MM	BGA_P2MM
SWITCHNODE	POWER	*	6:1_SPACING
SWITCHNODE	GND	*	6:1_SPACING
SWITCHNODE	*	*	SWITCHNODE

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
1128	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE1	65
1129	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE2	65
1130	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE3	65
1131	POWER	SWITCHNODE	1.5V	VR_CPU_PHASE4	66
1132	POWER	SWITCHNODE	3.3V	P3V3S5_REG_PHASE	69
1133	POWER	SWITCHNODE	5V	P5VS3_REG_PHASE	69
1134	POWER	SWITCHNODE	1.1V	VTT_REG_PHASE1	67
1135	POWER	SWITCHNODE	1.1V	VTT_REG_PHASE2	67
1136	POWER	SWITCHNODE	3.4V	P3V42G3H_SW	71
1137	POWER	SWITCHNODE	1.05V	PCHCORE_REG_PHASE	68
1138	POWER	SWITCHNODE	1.05V	P1V05_S5_REG_PHASE	71
1139	POWER	SWITCHNODE	1.5V	DDR_REG_PHASE	70
1140	POWER	SWITCHNODE	1.8V	P1V8_REG_PHASE	70
1141	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_A	28 30
1142	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFCA_B	28 31
1143	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_A	28 30
1144	POWER	POWER	1.5V	PP0V75_S3_MEM_VREFDQ_B	28 31
1681	POWER	POWER	12V	PP12V_S0_CPUVTT_FLTD	
1145	POWER	POWER	12V	PP12V_AUD_SPKRAMP_PLANE	57 58 60
1146	POWER	POWER	12V	PP12V_LCD	77
1147	POWER	POWER	12V	PP12V_LCD_CONN	77
1148	POWER	POWER	12V	PP12V_S0	6 63
1149	POWER	POWER	12V	PP12V_S0_CPU_FLTRD	64 65 66
1175	POWER	POWER	12V	PP12V_S0_FAN0_L	52 92
1176	POWER	POWER	12V	PP12V_S0_FAN1_L	52 92
1177	POWER	POWER	12V	PP12V_S0_FAN2_L	53 92
1668	POWER	POWER	12V	PP12V_G3H	6 71
1669	POWER	POWER	12V	PP12V_G3H_R	71
1178	POWER	POWER	12V	PP12V_S5	6
1150	POWER	POWER	12V	P12V_S0_FW	
1270	POWER	POWER	12V	P12V_S0_FW_CL	
1271	POWER	POWER	12V	P12V_S0_FW_D	
1268	POWER	POWER	12V	P12V_S0_FW_R	
1267	POWER	POWER	12V	FW_PORT0_VP	41
1272	POWER	POWER	12V	FW_PORT0_VP_F	41
1544	POWER	POWER	12V	PPVP_FW_PHY_CPS	40 41
1549	POWER	POWER	12V	PP12V_S3	6
1555	POWER	POWER	12V	PP12V_S3_WM_FLT	44
1259	POWER	POWER	1.1V	PPVCORE_S0_CPU	6
1258	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG1	65
1563	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG2	65
1564	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG3	65
1565	POWER	POWER	1.1V	PPVCORE_S0_CPU_REG4	66
1256	POWER	POWER	1.05V	PP1V05_SM_SOURCE	72
1174	POWER	POWER	1.05V	PP1V05_S0	6
1173	POWER	POWER	1.05V	PP1V05_S0_CK505_F	26
1182	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA	17 22
1181	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	
1180	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB	17 22
1188	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	
1187	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_EXP	22 24
1186	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_FDI	22 24
1185	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCAPLL_SATA	22 24
1184	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK	22 24
1183	POWER	POWER	1.05V	PP1V05_S0_PCH_VCCA_CLK_F	24
1609	POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP	
1599	POWER	POWER	1.05V	PP1V05_S0_CIO_VDD1P0_DP_PLL	
1614	POWER	POWER	1.05V	PP1V05_SM_PCH_LAN	6
1612	POWER	POWER	1.05V	PP1V05_S5	6
1672	POWER	POWER	1.05V	PP1V05_SM	6
1269	POWER	POWER	1.1V	PPVTT_S0	6
1555	POWER	POWER	1.1V	PPVTT_S0_CPU	6 49
1268	POWER	POWER	0.75V	PPVTT_S0_DDR	6
1611	POWER	POWER	0.75V	PP0V75_S0	6
1190	POWER	POWER	1.2V	PP1V2_S5_ENET	37
1192	POWER	POWER	1.5V	PP1V5_S0	6
1193	POWER	POWER	1.5V	PP1V5_S0_CK505_F	26
1587	POWER	POWER	1.5V	PP1V5_S0_CK505_R	26
1191	POWER	POWER	1.5V	PP1V5_S3	6
1670	POWER	POWER	1.5V	PP1V5_CPU_MEM	6 49
1208	POWER	POWER	1.5V	PP1V8R1V5_S0_PCH_VCCVRM	22 24
1410	POWER	POWER	1.5V	PP1V5_FW_VDDA	39
1203	POWER	POWER	1.5V	PP1V8_S0	6
1204	POWER	POWER	1.8V	PP1V8_S0_CPU	6 49
1206	POWER	POWER	1.96V	PP1V96_FW_PLLVDD	39
1205	POWER	POWER	1.96V	PP1V95_FW_FWPHY	39 40

POWER NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING	VOLTAGE		
1618	POWER	POWER	3.3V	PP3V3_S0	6
1619	POWER	POWER	3.3V	PP3V3_S0_CK505_F	26
1214	POWER	POWER	3.3V	PP3V3_S0_DPAUX	80
1215	POWER	POWER	3.3V	PP3V3_S0_DPFUSE	80
1216	POWER	POWER	3.3V	PP3V3_S0_DPPWR	80
1217	POWER	POWER	3.3V	PP3V3_S0_HS_F	61
1670	POWER	POWER	3.3V	PP3V3_S0M	6
1671	POWER	POWER	3.3V	PP3V3_MINI	33
1612	POWER	POWER	3.3V	PP3V3_ENET	36 37
1222	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC	17 22
1223	POWER	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	
1224	POWER	POWER	3.3V	PP3V3_S0_TSENS_R	51
1225	POWER	POWER	3.3V	PP3V3_S3	6 92
1655	POWER	POWER	3.3V	PP3V3_S3_BT_FLT	44
1238	POWER	POWER	3.3V	PP3V3_S3_SDCARD_FLT	44
1656	POWER	POWER	3.3V	PP3V3_S3_WM_FLT	44
1233	POWER	POWER	3.3V	PP3V3_S5	6
1677	POWER	POWER	3.3V	PPVTT_S3_DDR_BUF	70
1676	POWER	POWER	3.3V	PPV_S0_MXM_PWRSRC	50
1260	POWER	POWER	3.3V	PPVOUT_S0_PCH_DCPSST	22
1650	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUS	22
1660	POWER	POWER	3.3V	PPVOUT_S5_PCH_DCPSUSBYP	22
1262	POWER	POWER	3.3V	PPVOUT_G3_PCH_DCPRTC	22
1616	POWER	POWER	3.3V	PPVOUT_S0_PCH_VCCRTC_NCTF	
1662	POWER	POWER	3.3V	PPVBATT_G3_RTC	27
1663	POWER	POWER	3.3V	PPVBATT_G3_RTC_R	27
1652	POWER	POWER	3.3V	PP3V3_AUDIO_SPDIF_JACK	59
1609	POWER	POWER	3.3V	PP3V3_FW_AVDD	39
1213	POWER	POWER	3.3V	PP3V3_FW_ESD	41
1211	POWER	POWER	3.3V	PP3V3_FW_PLLVDD	39
1210	POWER	POWER	3.3V	PP3V3_FW_VDDA	39
1213	POWER	POWER	3.3V	PP3V3_G3_RTC	18 22 24 27
1214	POWER	POWER	3.3V	PP_ENET_CTRL12	37
1230	POWER	POWER	3.4V	PP3V3_G3H_SMC_AVCC	45
1231	POWER	POWER	3.3V	PP3V3_G3H_AVREF_SMC	45 46
1669	POWER	POWER	3.42V	PP3V42_G3H	6
1668	POWER	POWER	3.42V	PP3V42_G3H_R	71
1677	POWER	POWER	4.5V	4V5_REG_IN	55
1232	POWER	POWER	4.5V	PP4V5_AUDIO_ANALOG	55
1237	POWER	POWER	5V	PP5V_S0	6 92
1239	POWER	POWER	5V	PP5V_S0_CPU_VCORE_VCC	64
1238	POWER	POWER	5V	PP5V_S0_PCH_V5REF	22 24
1665	POWER	POWER	5V	PP5V_S0_SATA_FET	42
1240	POWER	POWER	5V	PP5V_S3	6
1242	POWER	POWER	5V	PP5V_S3_DDR_REG_V5FILT	70
1658	POWER	POWER	5V	PP5V_S3_CAMERA_FLT	44
1657	POWER	POWER	5V	PP5V_S3_IR_FLT	44
1604	POWER	POWER	5V	VREFMARGIN_DIMMA_P5V	28
1606	POWER	POWER	5V	VREFMARGIN_DIMMB_P5V	28
1235	POWER	POWER	5V	PP5V_S5	6
1234	POWER	POWER	5V	PP5V_S5_PCH_V5REFSUS	22 24
1608	POWER	POWER	5V	PP5V_CPUVTT_VR	67
1247	POWER	POWER	5V	PP5V_USB2_PORT0	43
1250	POWER	POWER	5V	PP5V_USB2_PORT0_F	43
1246	POWER	POWER	5V	PP5V_USB2_PORT1	43
1248	POWER	POWER	5V	PP5V_USB2_PORT1_F	43
1253	POWER	POWER	5V	PP5V_USB2_PORT2	43
1252	POWER	POWER	5V	PP5V_USB2_PORT2_F	43
1255	POWER	POWER	5V	PP5V_USB2_PORT3	43
1254	POWER	POWER	5V	PP5V_USB2_PORT3_F	43
1646	POWER	POWER		DDR_REG_PGND	70
1645	POWER	POWER		DDR_REG_CSGND	70

SENSING NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1195	SNS_DIFF	THERMAL	VR_CPU_ISNS1_P	64 65
1196	SNS_DIFF	THERMAL	VR_CPU_ISNS1_N	64 65
1197	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_P	64
1198	SNS_DIFF	THERMAL	VR_CPU_ISNS1_R_N	64
1199	SNS_DIFF	THERMAL	VR_CPU_ISNS2_P	64 65
1200	SNS_DIFF	THERMAL	VR_CPU_ISNS2_N	64 65
1201	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_P	64
1202	SNS_DIFF	THERMAL	VR_CPU_ISNS2_R_N	64
1203	SNS_DIFF	THERMAL	VR_CPU_ISNS3_P	64 65
1204	SNS_DIFF	THERMAL	VR_CPU_ISNS3_N	64 65
1205	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_P	64
1206	SNS_DIFF	THERMAL	VR_CPU_ISNS3_R_N	64
1207	SNS_DIFF	THERMAL	VR_CPU_ISNS4_P	64 66
1208	SNS_DIFF	THERMAL	VR_CPU_ISNS4_N	64 66
1209	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_P	64
1210	SNS_DIFF	THERMAL	VR_CPU_ISNS4_R_N	64
1645	SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_P	65
1667	SNS_DIFF	THERMAL	VR_CPU_ISNS1_XW_N	65
1668	SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_P	65
1666	SNS_DIFF	THERMAL	VR_CPU_ISNS2_XW_N	65
1670	SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_P	65
1671	SNS_DIFF	THERMAL	VR_CPU_ISNS3_XW_N	65
1672	SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_P	66
1673	SNS_DIFF	THERMAL	VR_CPU_ISNS4_XW_N	66
1679	SNS_DIFF		CPU_VCC_PKG_SENSE_P	13 49 64
1680	SNS_DIFF		CPU_VCC_PKG_SENSE_N	13 64
156	SNS_DIFF		CPU_VTTSENSE_P	13 49 67
157	SNS_DIFF		CPU_VTTSENSE_N	13 67
1192	SNS_DIFF		CPU_VTTSENSE_R_P	67
1193	SNS_DIFF		CPU_VTTSENSE_R_N	67
158	SNS_DIFF		VR_CPU_VSEN	64
159	SNS_DIFF		VR_CPU_RGND	64
1194	SNS_DIFF		VR_CPU_VSNS_R_N	64
1192	SNS_DIFF		VR_CPU_VSNS_R_P	64
1195	SNS_DIFF		VR_CPU_VSNS_XW_P	64
1196	SNS_DIFF		VR_CPU_VSNS_XW_N	64

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1127	VR_CTL_PHY	VR_CTL	VR_CPU_PH1_SNUB	65
1131	VR_CTL_PHY	VR_CTL	VR_CPU_PH2_SNUB	65
1133	VR_CTL_PHY	VR_CTL	VR_CPU_PH3_SNUB	65
1134	VR_CTL_PHY	VR_CTL	VR_CPU_PH4_SNUB	66
1343	VR_CTL_PHY	VR_CTL	VR_CPU_PWM1	64 65
1344	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2	64 65
1341	VR_CTL_PHY	VR_CTL	VR_CPU_PWM2_R	64
1342	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3	64 65
1345	VR_CTL_PHY	VR_CTL	VR_CPU_PWM3_R	64
1346	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4	64 66
1347	VR_CTL_PHY	VR_CTL	VR_CPU_PWM4_R	64
1348	VR_CTL_PHY	VR_CTL	VR_CPU_REF	64
1349	VR_CTL_PHY	VR_CTL	VR_CPU_SS	64
1350	VR_CTL_PHY	VR_CTL	VR_CPU_TCOMP	64
1351	VR_CTL_PHY	VR_CTL	VR_CPU_TM	64
1352	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT1_RC	65
1353	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT2_RC	65
1354	VR_CTL_PHY	VR_CTL	VR_CPU_BOOT3_RC	65
1355	VR_CTL_PHY	VR_CTL	VR_CPU_COMP	64
1356	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_R	64
1357	VR_CTL_PHY	VR_CTL	VR_CPU_COMP_RC	64
1358	VR_CTL_PHY	VR_CTL	VR_CPU_DAC	64
1359	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_BOOT	65
1360	VR_CTL_PHY	VR_CTL	VR_CPU_DRV1_GDSEL	65
1362	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_LGATE	65
1361	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV1_UGATE	65
1363	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_BOOT	65
1364	VR_CTL_PHY	VR_CTL	VR_CPU_DRV2_GDSEL	65
1366	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_LGATE	65
1365	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV2_UGATE	65
1367	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_BOOT	65
1368	VR_CTL_PHY	VR_CTL	VR_CPU_DRV3_GDSEL	65
1370	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_LGATE	65
1369	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV3_UGATE	65
1371	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_BOOT	66
1372	VR_CTL_PHY	VR_CTL	VR_CPU_DRV4_GDSEL	66
1374	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_LGATE	66
1373	VR_CTL_PHY	SWITCHNODE	VR_CPU_DRV4_UGATE	66
1375	VR_CTL_PHY	VR_CTL	VR_CPU_FAN	64
1376	VR_CTL_PHY	VR_CTL	VR_CPU_FB	64
1377	VR_CTL_PHY	VR_CTL	VR_CPU_FB_R	64
1378	VR_CTL_PHY	VR_CTL	VR_CPU_FS	64
1379	VR_CTL_PHY	VR_CTL	VR_CPU_IMON	49 64
1380	VR_CTL_PHY	VR_CTL	VR_CPU_IOUT_PD	64
1381	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_UGATE	68
1382	VR_CTL_PHY	SWITCHNODE	PCHCORE_REG_LGATE	68
1383	VR_CTL_PHY	VR_CTL	PCHCORE_REG_VFB	68
1384	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TON	68
1385	VR_CTL_PHY	VR_CTL	PCHCORE_REG_TRIP	68
1386	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT	68
1387	VR_CTL_PHY	VR_CTL	PCHCORE_REG_BOOT_R	68
1400	VR_CTL_PHY	VR_CTL	VTT_REG_BOOT1	67
1401	VR_CTL_PHY	VR_CTL	VTT_REG_BOOT2	67
1402	VR_CTL_PHY	VR_CTL	VTT_REG_COMP	67
1403	VR_CTL_PHY	VR_CTL	VTT_REG_FB	67
1404	VR_CTL_PHY	VR_CTL	VTT_REG_FS	67
1405	VR_CTL_PHY	VR_CTL	VTT_REG_ICOMP	67
1406	VR_CTL_PHY	VR_CTL	VTT_REG_IREF	67
1407	VR_CTL_PHY	VR_CTL	VTT_REG_ISUM	67
1408	VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE1	67
1409	VR_CTL_PHY	SWITCHNODE	VTT_REG_LGATE2	67
1410	VR_CTL_PHY	VR_CTL	VTT_REG_OCSET	67
1411	VR_CTL_PHY	VR_CTL	VTT_OFST	67
1412	VR_CTL_PHY	VR_CTL	VTT_REG_REF	67
1413	VR_CTL_PHY	VR_CTL	VTT_REG_RGND	67
1414	VR_CTL_PHY	VR_CTL	VTT_SEL	67
1415	VR_CTL_PHY	VR_CTL	VTT_REG_UGATE2	67
1416	VR_CTL_PHY	VR_CTL	VTT_REG_UGATE1	67
1418	VR_CTL_PHY	VR_CTL	VTT_REG_PH1_SNUB	67
1417	VR_CTL_PHY	VR_CTL	VTT_REG_PH2_SNUB	67
1419	VR_CTL_PHY	VR_CTL	VTT_REG_VSEN	67
1597	VR_CTL_PHY	VR_CTL	P1V05S5_REG_VFB	71
1607	VR_CTL_PHY	VR_CTL	P3V42G3H_BOOST	71
1608	VR_CTL_PHY	VR_CTL	P3V42G3H_FB	71

VR CTRL NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1437	VR_CTL_PHY	VR_CTL	DDR_REG_CS	70
1438	VR_CTL_PHY	VR_CTL	DDR_REG_FB	70
1439	VR_CTL_PHY	SWITCHNODE	DDR_REG_LGATE	70
1440	VR_CTL_PHY	SWITCHNODE	DDR_REG_UGATE	70
1441	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT	70
1442	VR_CTL_PHY	VR_CTL	DDR_REG_BOOT_R	70
1443	VR_CTL_PHY	VR_CTL	DDR_REG_VDDQSNS	70
1444	VR_CTL_PHY	VR_CTL	DDR_REG_VTTSNS	70
1445	VR_CTL_PHY	VR_CTL	P1V8_REG_POR	70
1446	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT	69
1447	VR_CTL_PHY	VR_CTL	P3V3S5_REG_BOOT_R	69
1452	VR_CTL_PHY	VR_CTL	P3V3S5_REG_FB	69
1453	VR_CTL_PHY	VR_CTL	P3V3S5_REG_ISEN	69
1454	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_LGATE	69
1455	VR_CTL_PHY	VR_CTL	P3V3S5_REG_OCSET	69
1456	VR_CTL_PHY	SWITCHNODE	P3V3S5_REG_UGATE	69
1457	VR_CTL_PHY	VR_CTL	P3V3S5_REG_SNUB	69
1459	VR_CTL_PHY	VR_CTL	P5VS3_REG_BOOT	69
1460	VR_CTL_PHY	VR_CTL	P5VS3_REG_FB	69
1462	VR_CTL_PHY	VR_CTL	P5VS3_REG_ISEN	69
1463	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_LGATE	69
1464	VR_CTL_PHY	VR_CTL	P5VS3_REG_OCSET	69
1466	VR_CTL_PHY	SWITCHNODE	P5VS3_REG_UGATE	69

VR VID NET PROPERTIES

NET_TYPE

	PHYSICAL	SPACING		
1649	VID_PHY	VR_CTL	CPU_VID<0>	13 16 64
1642	VID_PHY	VR_CTL	CPU_VID<1>	13 16 64
1623	VID_PHY	VR_CTL	CPU_VID<2>	13 16 64
1622	VID_PHY	VR_CTL	CPU_VID<3>	13 16 64
1621	VID_PHY	VR_CTL	CPU_VID<4>	13 16 64
1620	VID_PHY	VR_CTL	CPU_VID<5>	13 16 64
1625	VID_PHY	VR_CTL	CPU_VID<6>	13 16 64
1629	VID_PHY	VR_CTL	CPU_VID<7>	13 16 64
1555	VID_PHY	VR_CTL	CPU_PSI_L	13 16 64

PULL-UP STUB < 1-INCH
VID LENGTH SKEW < 1-INCH
VID LENGTH RANGE< 1 TO 15-INCH

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VID_PHY	*	39_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL	*	0.2MM	?

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POWER CONSTRAINTS

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PM NET PROPERTIES
(PM, RESET, EN, PGOOD)

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	2:1_SPACING
PM_VTT	PM_VTT	*	2:1_SPACING
PM_VTT	*	*	3:1_SPACING
PM_VTT	GND	*	DEFAULT
PM	GND	*	DEFAULT

	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T2		PM	PLT_RESET_L	20 27
T4		PM_VTT	PLT_RESET_LS1V1_L	11
T4		PM	PM_ACDC_PS_ON	6
T8		PM	PM_BATLOW_L	15 19 45
T5		PM	PM_CLK32K_SUSCLK	9 45 85
T7		PM	PM_CLK32K_SUSCLK_R	9 19 85
T6		PM	PM_CLKRUN_L	15 19 45 47
T10		PM	PM_EXT_TS_L<0>	11 46
T6		PM	PM_EXT_TS_L<1>	11 46
T12		PM	PM_LAN_PWRGD	15 19
T11		PM_VTT	FSB_CPURSTOUT_L	11 25
T12		PM	USB_HUB_RESET_L	34 35
T25		PM_VTT	PM_MEM_PWRGD	11 19
T24		PM	PM_ME_PWRGD	19 63
T27		PM	PM_ME_S0_EN_G	72
T26		PM	PM_ME_S0_EN_G1	72
T28		PM	PM_ME_S0_EN_R	72
T30		PM	PM_MXM_PGOOD	63 74
T29		PM	PM_PCH_PWRGD	19 63
T33		PM	PM_PGOOD_DDRREG_S3	5 62 70
T33		PM	PM_PGOOD_PVCORE_CPU	5 26 63 64
T32		PM	PM_PWRBTN_L	19 25 45
T35		PM	PM_RSMRST_L	45 62
T34		PM	PM_RSMRST_PCH_L	19 62
T36		PM	PM_SLP_M_L	5 19 62
T38		PM	PM_SLP_M_R	
T37		PM	PM_SLP_S3_L	5 19 32 33 37 46 62 63
T40		PM	PM_SLP_S3_L_AND_S0_RDY	
T42		PM	PM_SLP_S4_1_L	19 62
T41		PM	PM_SLP_S4_2_L	19 45 46
T43		PM	PM_SLP_S4_3_L	5 19
T39		PM	PM_SLP_S4_L	19 32
T44		PM	PM_SLP_S5_L	19 45
T45		PM	PM_SUS_PWR_ACK	19
T22		PM_VTT	PM_SYNC	11 19
T92		PM	SDCARD_PLT_RST_L	27 44
T46		PM	PM_SYSRST_L	19 27 45
T44		PM	PM_SYS_PWRGD	19 32 63
T48		PM_VTT	PM_THRMTRIP_L	11 21 46
T48		PM	RSMRST_PWRGD	45 63
T47		PM	RTC_RESET_L	18 91
T50		PM_VTT	CPU_PWRGD	11 21 25
T49		PM	CPU_RESET_L	11 27
T53		PM	PGOOD_1V05ME_G1	63
T51		PM	PGOOD_1V05ME_G2	63
T56		PM	PGOOD_1V8_S0_G1	63
T52		PM	PGOOD_1V8_S0_G2	63
T55		PM	PGOOD_CPU_GFX_DDR	63
T54		PM	PGOOD_P12V_S3	
T35		PM	PGOOD_P1V05_ME_S5	
T58		PM	PGOOD_P1V5_S0	72
T57		PM	PGOOD_P1V8_S0	63
T59		PM	PGOOD_P3V3_ME	72
T61		PM	PGOOD_P3V3_S0	48 63 72
T60		PM	PGOOD_P3V3_S3	34 72
T63		PM	PGOOD_P5V_S0	62 72
T62		PM	PGOOD_PCH_AND_P1V8	63
T64		PM	PGOOD_PCH_S0	63
T66		PM	PGOOD_SYSPWROK	63
T65		PM	PGOOD_SYSPWROK_R	63
T67		PM	RTC_RESET_L	18 91
T68		PM	P12V_S3_EN	62 72
T69		PM	P1V05_ME_SM_EN	62 72
T71		PM	P1V5_S0_EN	62 72
T70		PM	P3V3ME_EN	62 72
T72		PM	P3V3S0_EN	62 72
T74		PM	P3V3S3_EN	62 72
T73		PM	P5VS0_EN	62 72
T75		PM	P5VS3_EN	62 69
T77		PM	PCHCORE_REG_EN	62 68
T76		PM	PCHCORE_REG_PGOOD	5 62 63 68
T78		PM	PEG_RESET_L	9 27
T80		PM	SDCARD_RESET	21 25 44 92

	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T82		PM	4V5_REG_EN	55
T81		PM	ALL_SYS_PWRGD_R	6 25 32 63
T84		PM	ALL_SYS_PWRGD_SMC	45 63
T83		PM	CK505_27MHZ_EN	26
T85		PM	CPUVTT_REG_EN	62 67
T86		PM_VTT	CPUVTT_REG_PGOOD	11 62 63 67
T87		PM	CPU_MEM_RESET_L	11 32
T88		PM	DDRVTT_EN	32 62 70
T89		PM	DEBUG_RESET_L	27 47
T90		PM	FWPHY_RESET_L	39
T91		PM	FWXIO_SNOOP_EN	39
T92		PM	FW_RESET_L	27 39
T93		PM	GFX_VR_EN	
T94		PM	GFX_VR_PGOOD	
T95		PM	LAN_RESET_L	27 36
T97		PM	MEM_RESET_L	30 31 32
T96		PM	MINI_RESET_L	27 33
T98		PM	SMC_DELAYED_PWRGD	46 63
T100		PM	SMC_LRESET_L	27 45
T99		PM	SMC_RESET_L	45 46 47
T102		PM	T28_RESET_L	
T101		PM_VTT	XDP_CPUPWRGD	11 25
T103		PM_VTT	XDP_DBRESET_L	11 25 27
T104		PM_VTT	XDP_PWRGD	25

NET PHYSICAL FOR NC NETS
REMOVE WHEN CHECKPLUS IS FIXED

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	PCIE GRAPHICS			
T106		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_N
T106		PCIE_85D	PCIE	NC_PCIE_CLK100M_EXCARD_P
T107		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_N
T108		PCIE_85D	PCIE	NC_PCIE_EXCARD_D2R_P
T109		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_N
T110		PCIE_85D	PCIE	NC_PCIE_EXCARD_R2D_C_P
T112	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_N
T111	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXCARD_P
T113	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_N
T113	NO_TEST=TRUE	USB_90D	USB	NC_USB_EXTE_P
T116	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_N
T115	NO_TEST=TRUE	USB_90D	USB	NC_USB_TPAD_P

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PM RESETS ENABLES PGOOD CONST

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FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

J4700 USB CAMERA

	IN	PP5V_S3_CAMERA	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
85 44	IN	USB_CAMERA_L_P	FUNC_TEST=TRUE
85 44	IN	USB_CAMERA_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4700
2 Ground Testpoints near J4700

J4750 USB CARD READER

85 44	IN	USB_SDCARD_L_P	FUNC_TEST=TRUE
85 44	IN	USB_SDCARD_L_N	FUNC_TEST=TRUE
91 44 25 21	IN	SDCARD_RESET	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4750
2 Ground Testpoints near J4750

J4720 USB BLUETOOTH

85 44	IN	USB_BT_L_P	FUNC_TEST=TRUE
85 44	IN	USB_BT_L_N	FUNC_TEST=TRUE

1 PP3V3_S3 Testpoint near J4720
2 Ground Testpoints near J4720

J4780 IR BOARD

85 44	IN	USB_IR_L_P	FUNC_TEST=TRUE
85 44	IN	USB_IR_L_N	FUNC_TEST=TRUE

1 PP5V_S3_REG Testpoint near J4780
2 Ground Testpoints near J4780

J4520 SATA ODD (HIGH SPEED)

84 42	IN	SATA_ODD_R2D_P	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_R2D_N	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_D2R_C_N	FUNC_TEST=TRUE
84 42	IN	SATA_ODD_D2R_C_P	FUNC_TEST=TRUE
45 42	IN	SMC_ODD_DETECT	FUNC_TEST=TRUE

1 PP5V_S0 Testpoint near J4520
5 Ground Testpoints near J4520

J4510 SATA HDD (HIGH SPEED)

84 42	IN	SATA_HDD_R2D_P	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_R2D_N	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_D2R_C_N	FUNC_TEST=TRUE
84 42	IN	SATA_HDD_D2R_C_P	FUNC_TEST=TRUE

3 Ground Testpoints near J4510

J5520 ANALOG LCD TEMP SENSOR

88 51	IN	SNS_LCD_P	FUNC_TEST=TRUE
88 51	IN	SNS_LCD_N	FUNC_TEST=TRUE

J5521 AMBIENT TEMP SENSOR

88 51	IN	SNS_AMB_P	FUNC_TEST=TRUE
88 51	IN	SNS_AMB_N	FUNC_TEST=TRUE

J5551 ODD TEMP SENSOR

88 51	IN	SNS_ODD_P	FUNC_TEST=TRUE
88 51	IN	SNS_ODD_N	FUNC_TEST=TRUE

J5600 ODD FAN

52	IN	FAN_0_PWR_L	FUNC_TEST=TRUE
52	IN	FAN_TACH0_L	FUNC_TEST=TRUE
89 52	IN	PP12V_S0_FAN0_L	FUNC_TEST=TRUE
52	IN	FAN_0_GND	FUNC_TEST=TRUE

J5700 CPU FAN

53	IN	FAN_2_PWR_L	FUNC_TEST=TRUE
53	IN	FAN_TACH2_L	FUNC_TEST=TRUE
89 53	IN	PP12V_S0_FAN2_L	FUNC_TEST=TRUE
53	IN	FAN_2_GND	FUNC_TEST=TRUE

J5601 HD FAN

52	IN	FAN_1_PWR_L	FUNC_TEST=TRUE
52	IN	FAN_TACH1_L	FUNC_TEST=TRUE
89 52	IN	PP12V_S0_FAN1_L	FUNC_TEST=TRUE
52	IN	FAN_1_GND	FUNC_TEST=TRUE

J5550 HDD TEMP SENSOR

88 51	IN	HDD_OOB_TEMP_FILT	FUNC_TEST=TRUE

J5560 SKIN TEMP SENSOR

88 51	IN	SNS_SKIN_P	FUNC_TEST=TRUE
88 51	IN	SNS_SKIN_N	FUNC_TEST=TRUE

J6601 AUDIO MICROPHONE

59	IN	AUD_MIC_IN1_N_CONN	FUNC_TEST=TRUE
59	IN	GND_AUDIO_MIC1_CONN	FUNC_TEST=TRUE
59	IN	AUD_MIC_IN1_P_CONN	FUNC_TEST=TRUE

1 Ground Testpoint near J6601

J6602 AUDIO RIGHT SPEAKER

85 59 58	IN	AUD_SPKR_OUTLO2R_POUT	FUNC_TEST=TRUE
85 59 58	IN	AUD_SPKR_OUTLO2R_NOUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1R_POUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1R_NOUT	FUNC_TEST=TRUE

J6603 AUDIO LEFT SPEAKER

85 59 58	IN	AUD_SPKR_OUTLO2L_POUT	FUNC_TEST=TRUE
85 59 58	IN	AUD_SPKR_OUTLO2L_NOUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1L_POUT	FUNC_TEST=TRUE
85 59 57	IN	AUD_SPKR_OUTLO1L_NOUT	FUNC_TEST=TRUE

		GND	16 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=16
89 6	IN	PP3V3_S3	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=2
69 6	IN	PP5V_S3_REG	2 TP'S FUNC_TEST=TRUE MIN_ALLOWED_TPS=1
89 6	IN	PP5V_S0	FUNC_TEST=TRUE MIN_ALLOWED_TPS=1

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