

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
			2011-01-24

SCHEM, RIO, D2
 PIB2B, 03/16/2012
 820-3071-10.brd

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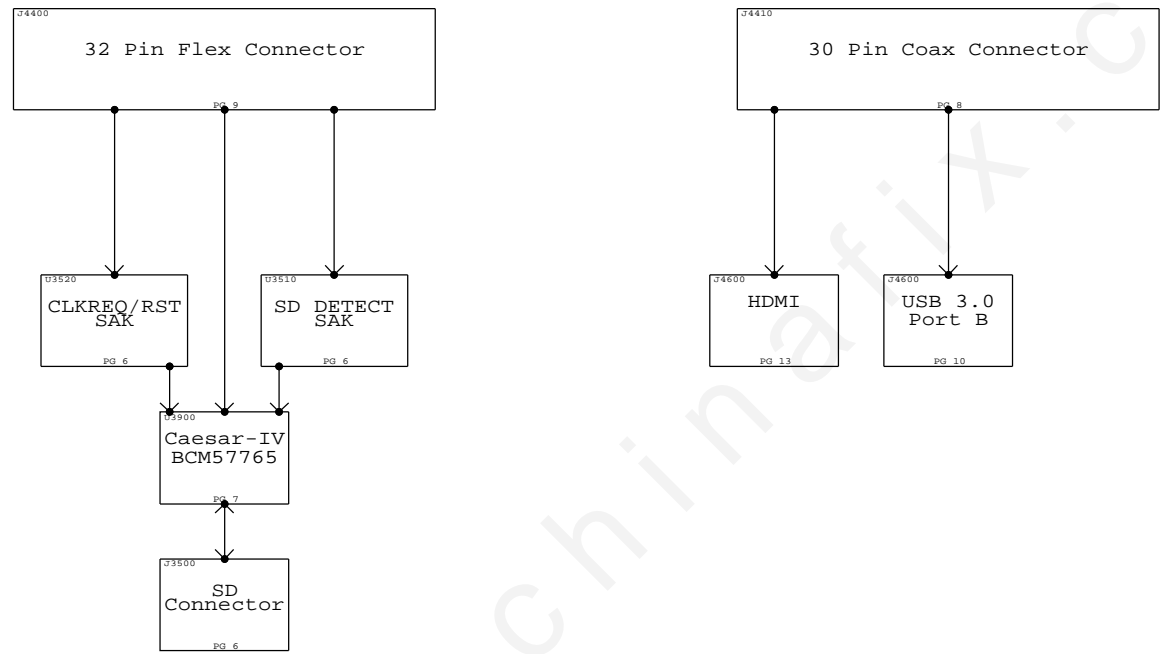
ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8974	1	SCHEM, RIO, J5	SCH	CRITICAL	
820-3071	1	PCBF, RIO, J5	PCB	CRITICAL	

DRAWING
 TITLE=TITLE
 ABBREV=DRAWING
LAST_MODIFIED=Fri Mar 16 13:44:38 2012

DRAWING TITLE		SCHEM, RIO, D2
DRAWING NUMBER		D
REVISION		
BRANCH		
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System Block Diagram			
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1907	PCBA,RIO,J5	J5_RIO_COMMON,EEEE:DL62
085-2805	PCBA,DEV RIO,J5	J5_RIO_DEVEL:ENG

J5 RIO BOM GROUPS

BOM GROUP	BOM OPTIONS
J5_RIO_COMMON	COMMON,ENETLOWPWR:NO,J5_RIO_PROGPARTS,HDMI_3V3_S0:YES,ALTERNATE
J5_RIO_PROGPARTS	
J5_RIO_DEVEL:ENG	ENET_ROM

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0311	128S0329		ALL	NEC alt to Sanyo
197S0450	197S0177		ALL	Alt EPSON Xtal
197S0451	197S0177		ALL	Alt NDK Xtal


Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
825-7753	1	TEXT, LABEL, RIO, D2	[EEEE:DL62]	CRITICAL	EEEE:DL62
825-7697	1	LBL, SERIAL NO, BOARDS, D2	TEXT_LABEL	CRITICAL	EEEE:DL62

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
-------------	-----	-------------	---------------	----------	------------

Programmables - All builds

SYNC MASTER=MASTER		SYNC DATE=MASTER	
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BOM Configuration			
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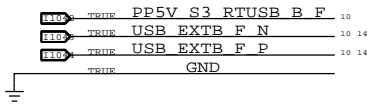
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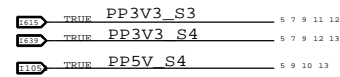
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Functional Test Points

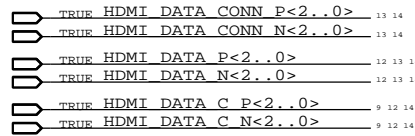
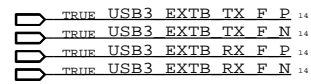
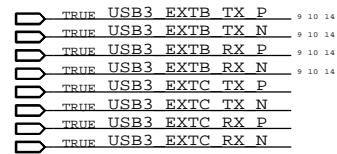
USB PORTS



POWER RAILS



NO_TEST=TRUE



www.chinafix.com

D

D

C

C

B

B

A

A

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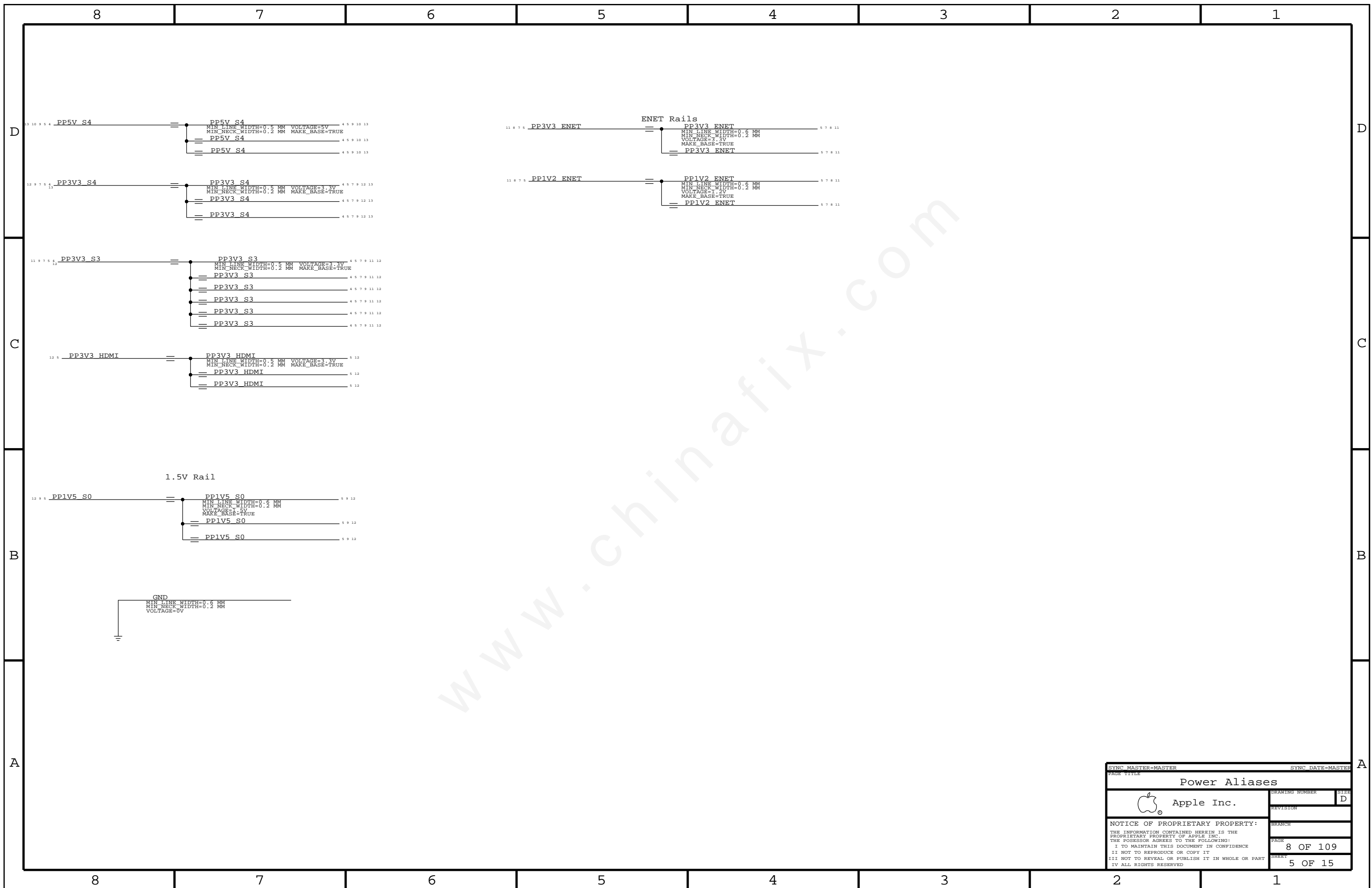
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3

2

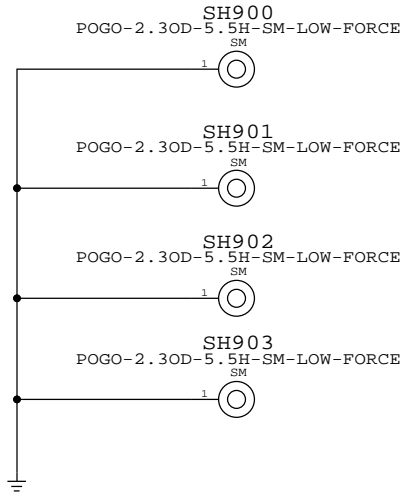
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PAGE TITLE Functional / ICT Test			
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Power Aliases			
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APN870-2451
Pogo pins



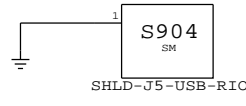
Unused ethernet signals

```

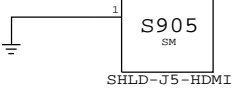
ENET MDI P<3..0> == NC ENET MDI P<3..0>
                  MAKE_BASE=TRUE NO_TEST=TRUE
ENET MDI N<3..0> == NC ENET MDI N<3..0>
                  MAKE_BASE=TRUE NO_TEST=TRUE
NC ENET WAKE L   == NC ENET WAKE L
                  MAKE_BASE=TRUE NO_TEST=TRUE
NC ENET MEDIA SENSE == NC ENET MEDIA SENSE
                  MAKE_BASE=TRUE NO_TEST=TRUE

SYSCLK_CLK25M_ENET == SYSCLK_CLK25M_ENET
                    WAKE_BASE=TRUE
    
```

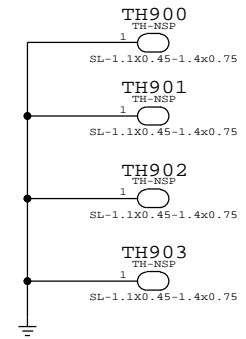
APN806-2500
can shield



APN806-2865
can shield

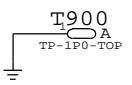


APN:998-3975



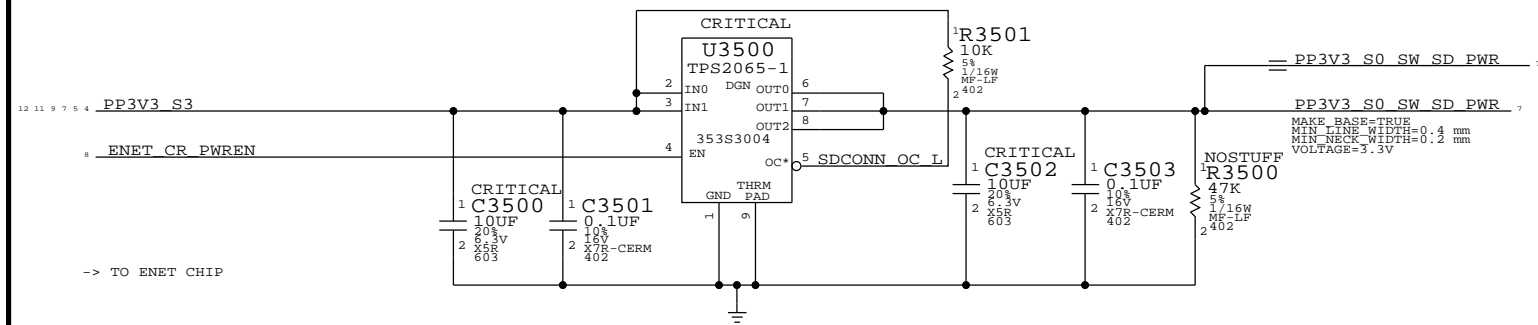
TH900/1 for USB can gnd slot
TH902/3 for HDMI can gnd slot

APN998-1457
SMT GND connuity test pin

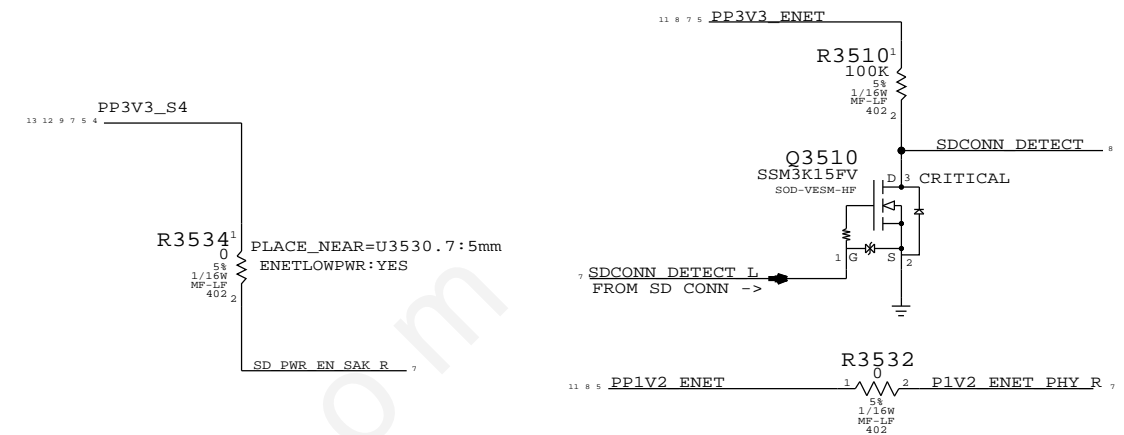


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Signal Aliases			
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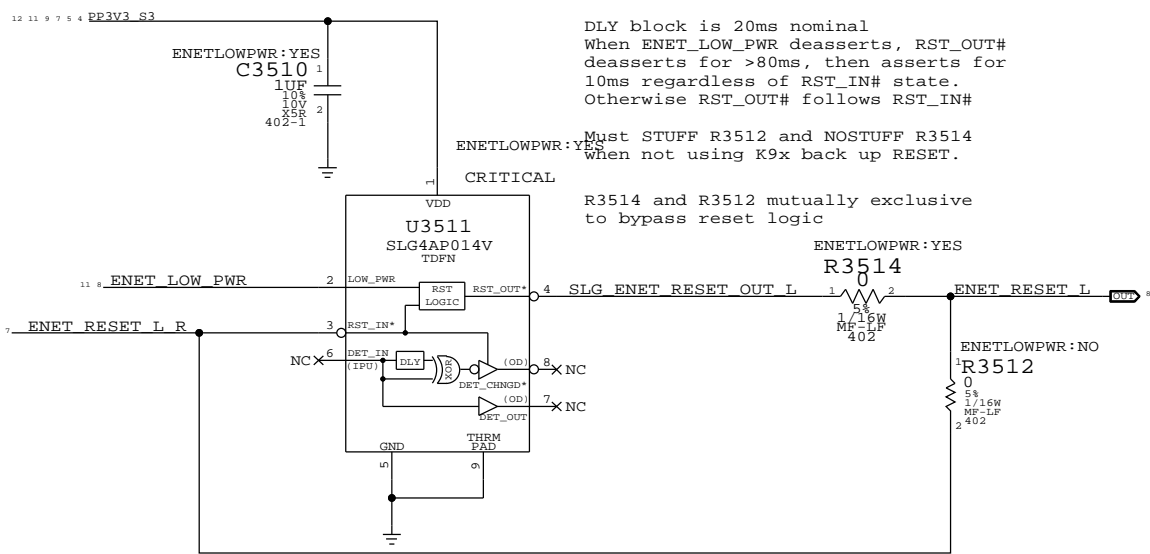
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE
TPS2065-1 (1.0A LIMIT) HAS ACTIVE LOAD DISCHARGE SO R3500 IS NOSTUFF.



DETECT ISOLATION CIRCUIT

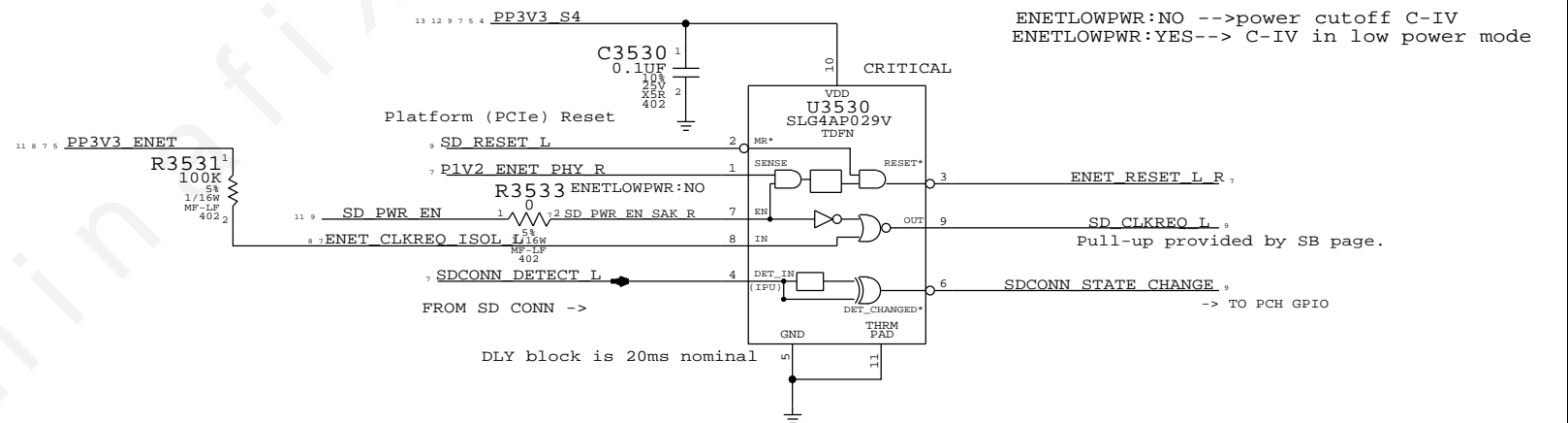


DETECT-CHANGED PCH GPIO LATCH CIRCUIT



DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT# deasserts for >80ms, then asserts for 10ms regardless of RST_IN# state. Otherwise RST_OUT# follows RST_IN#
Must STUFF R3512 and NOSTUFF R3514 when not using K9x back up RESET.
R3514 and R3512 mutually exclusive to bypass reset logic

Supervisor & CLKREQ# Isolation
SDCONN DETECT DEBOUNCE, INVERSION, AND
DETECT-CHANGED PCH GPIO LATCH CIRCUIT

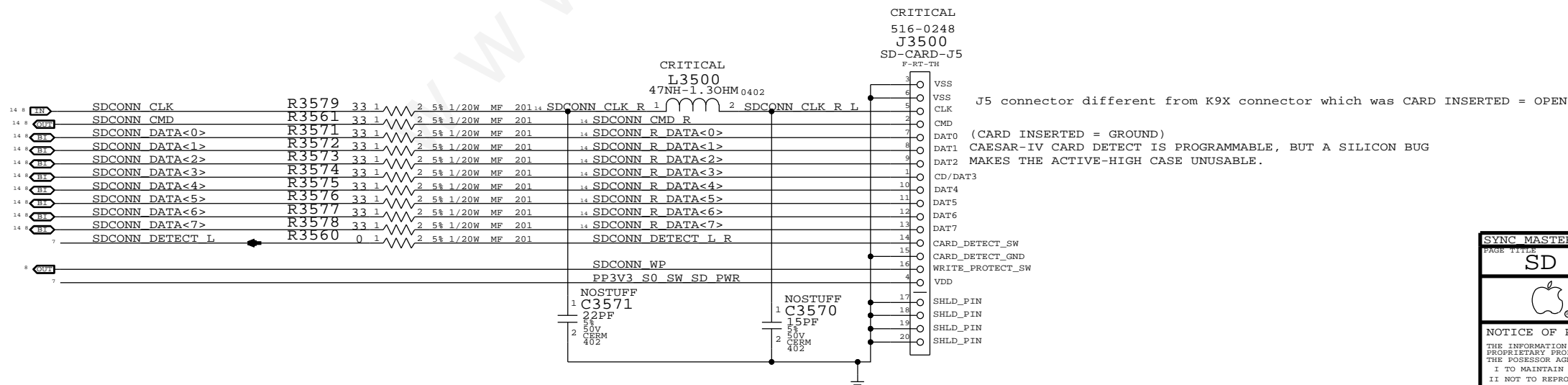


ENETLOWPWR:NO --> power cutoff C-IV
ENETLOWPWR:YES --> C-IV in low power mode

Note logic inversion of K16 connector.
Input to C-IV should remain active low

New part SLGAP029V (APN 343s0563)

SD CARD CONNECTOR



J5 connector different from K9X connector which was CARD INSERTED = OPEN

(CARD INSERTED = GROUND)
DAT1 CAESAR-IV CARD DETECT IS PROGRAMMABLE, BUT A SILICON BUG
DAT2 MAKES THE ACTIVE-HIGH CASE UNUSABLE.

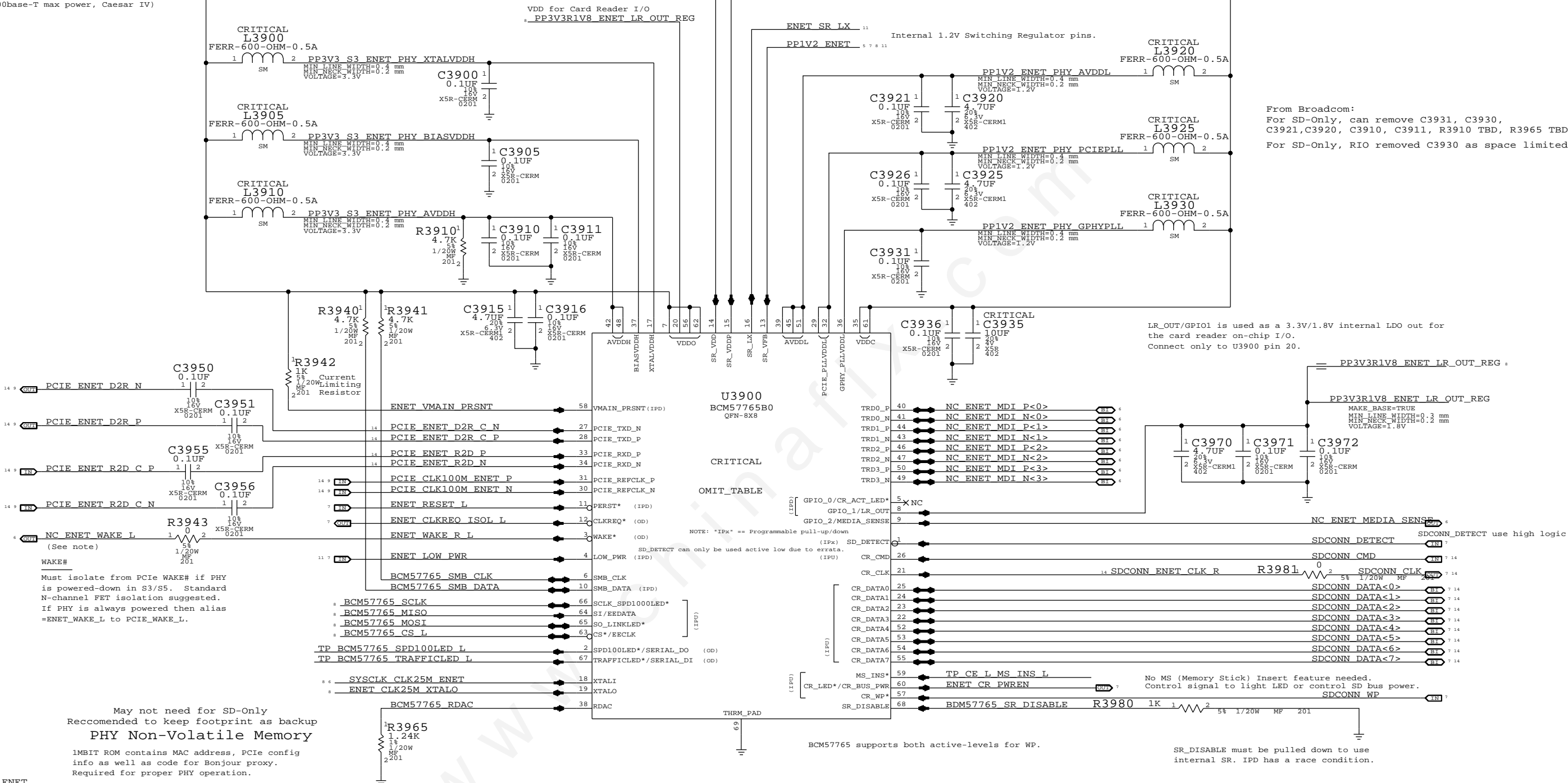
PAGE TITLE		DRAWING NUMBER	
SD READER CONNECTOR		D	
Apple Inc.		REVISION	
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0591	1	D2, S7100, SD CNTRL ONLY, B0, QFN 8x8	U3900	CRITICAL	

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
 If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
 If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
 Special Star routing needed on these pins. Decoupling on Pg 37.

11 8 7 5 PP3V3 ENET
 281mA (1000base-T max power, Caesar IV)

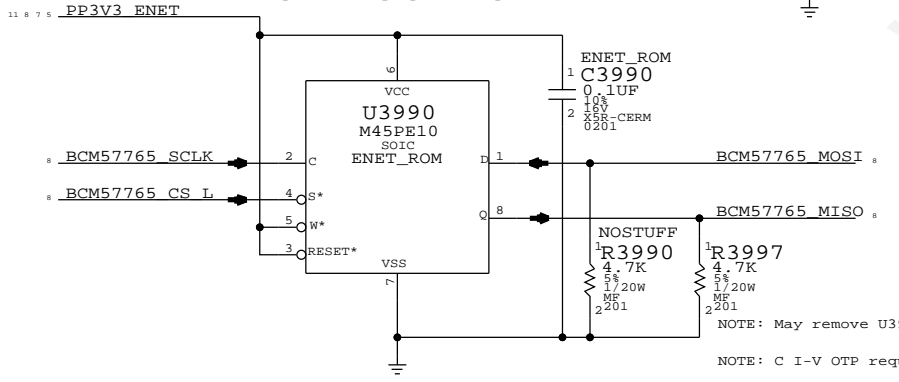
PP1V2 ENET 5 7 8 11
 ???mA (1000base-T, Caesar V)



From Broadcom:
 For SD-Only, can remove C3931, C3930, C3921, C3920, C3910, C3911, R3910 TBD, R3965 TBD
 For SD-Only, RIO removed C3930 as space limited

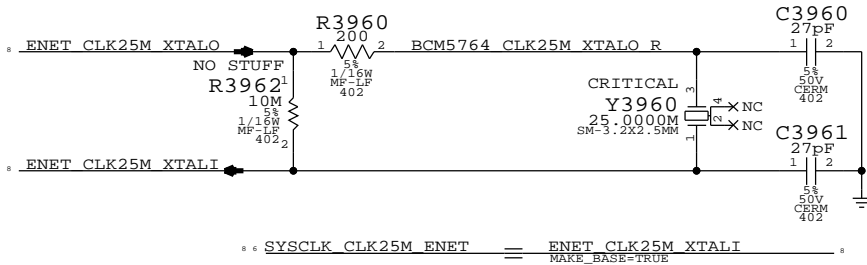
LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
 Connect only to U3900 pin 20.

May not need for SD-Only
 Recommended to keep footprint as backup
PHY Non-Volatile Memory
 1Mbit ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
 Required for proper PHY operation.



NOTE: May remove U3990 after use OTP
 NOTE: C I-V OTP requires SO pull-down instead of SI.

Caesar IV (ENET) 25MHz Crystal

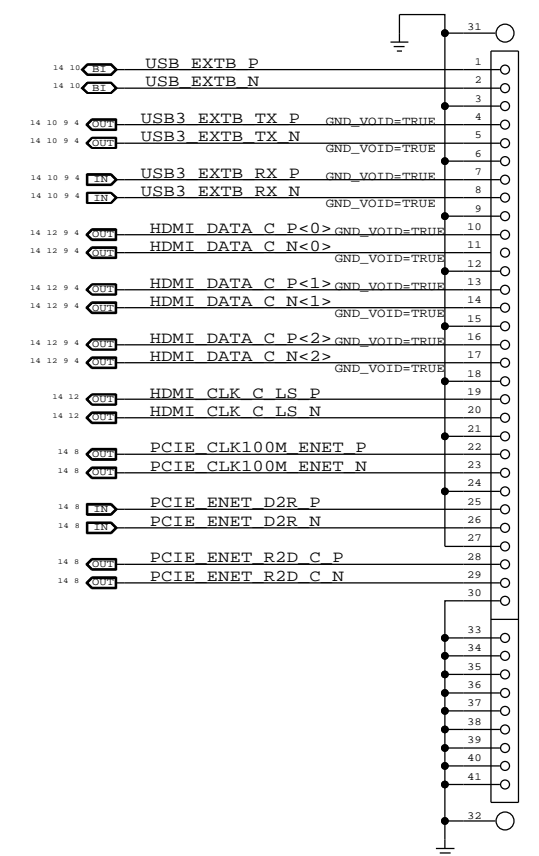
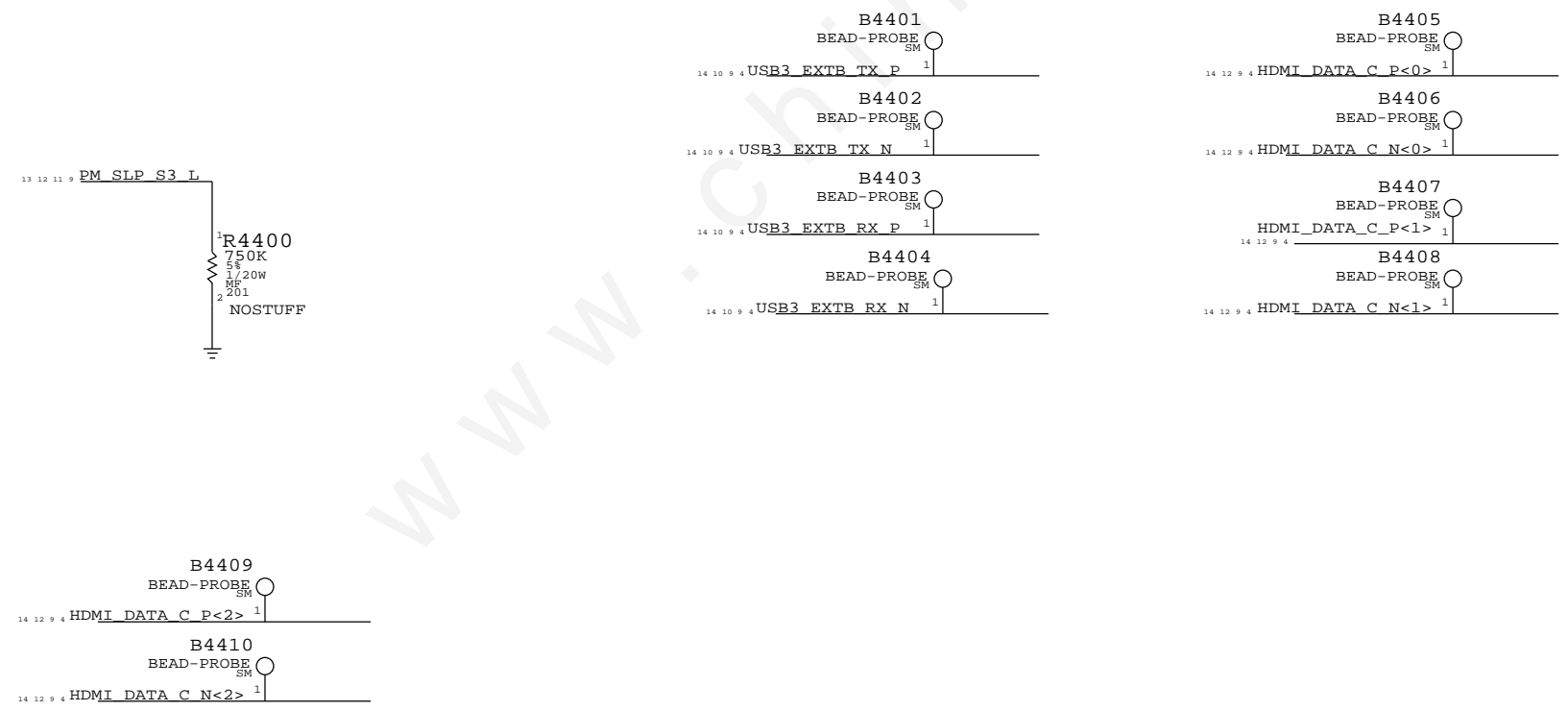
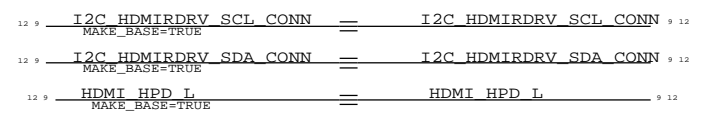
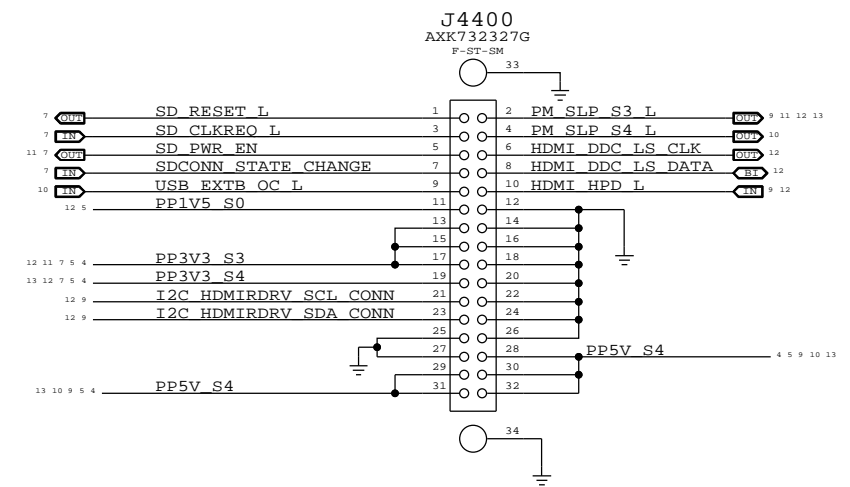


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ETHERNET PHY (CAESAR IV)			
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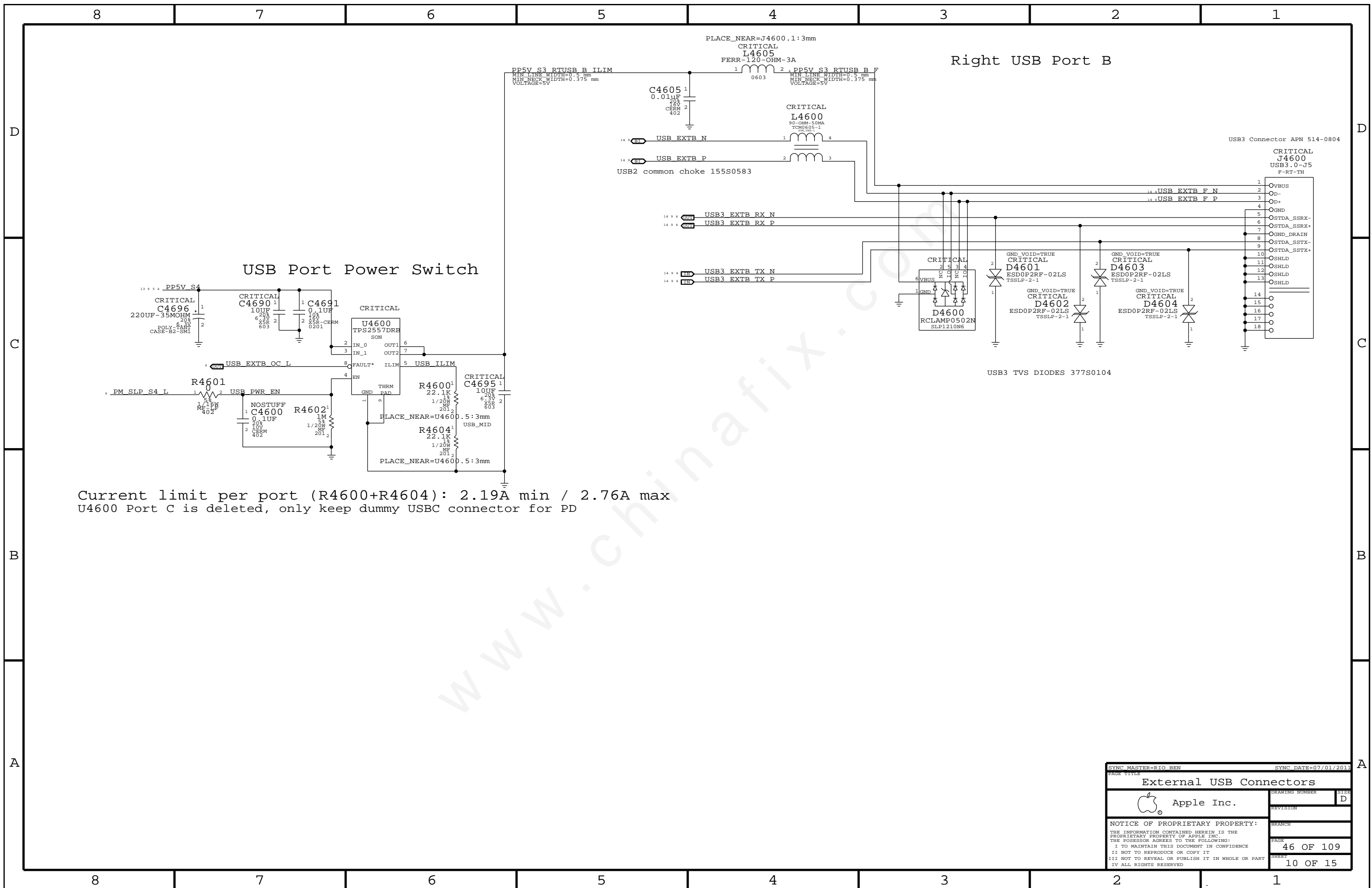
RIO cable will have pin 1 to pin 1 mapping from rev5!!!

CRITICAL TO RIO FLEX
Flex Connector
 516S0853

CRITICAL
Coax Connector
 518S0829
 J4410
 20525-130E-01
 F-RT-SM



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RIO CONNECTORS			
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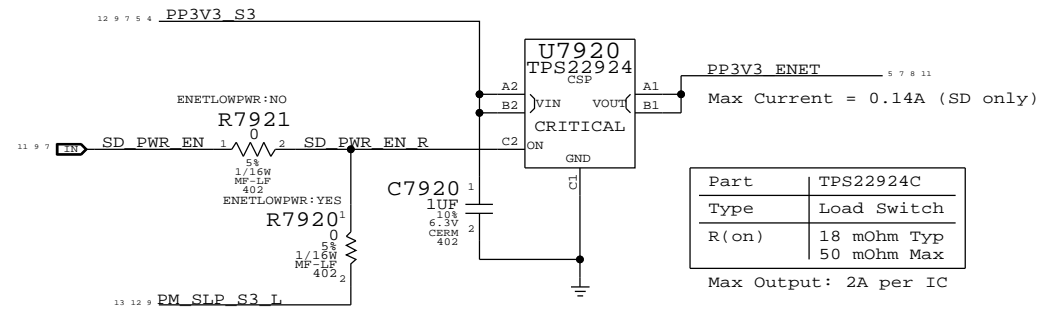


Current limit per port (R4600+R4604): 2.19A min / 2.76A max
 U4600 Port C is deleted, only keep dummy USB C connector for PD

SYNC MASTER=RIO BEN		SYNC DATE=07/01/2011	
External USB Connectors			
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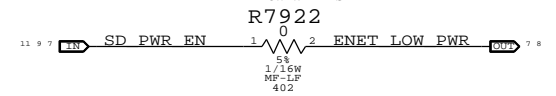
State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V ENET Switch

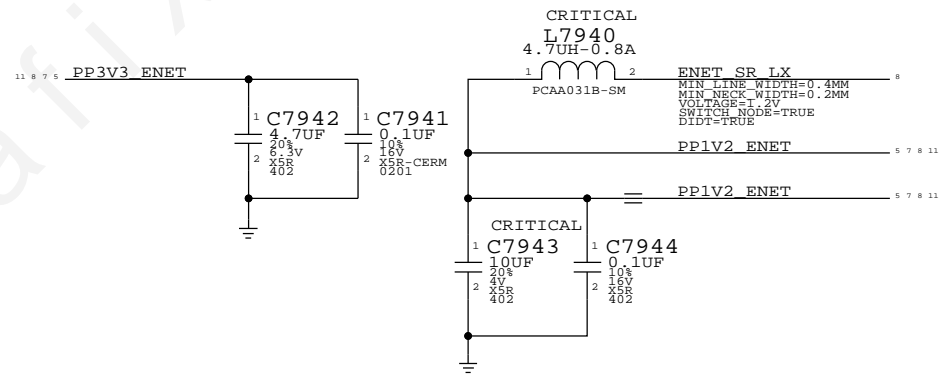


Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Stuff R7920 & R7921 force ENET switch always on and connect ENET_LOW_PWR to GPIO instead



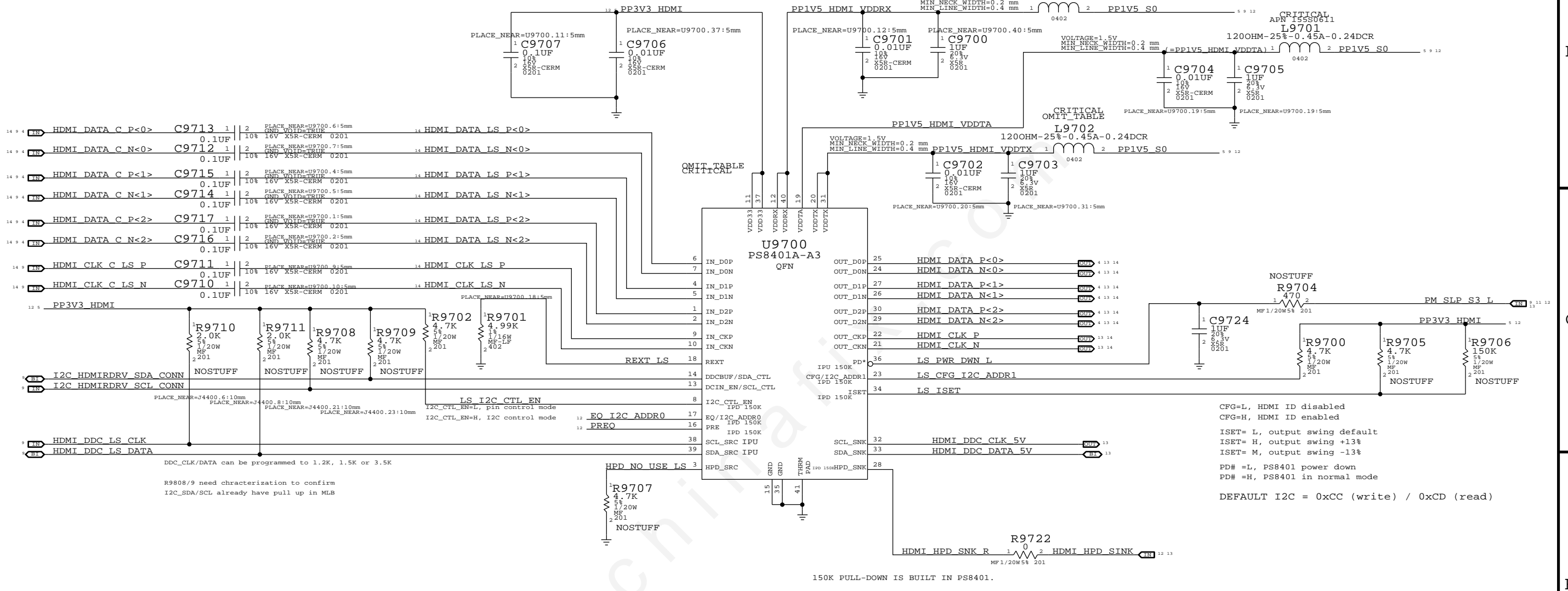
CAESAR IV 1.2V INT.VR CMPTS



SYNC MASTER=MASTER		SYNC DATE=MASTER	
Power Control 1/ENABLE			
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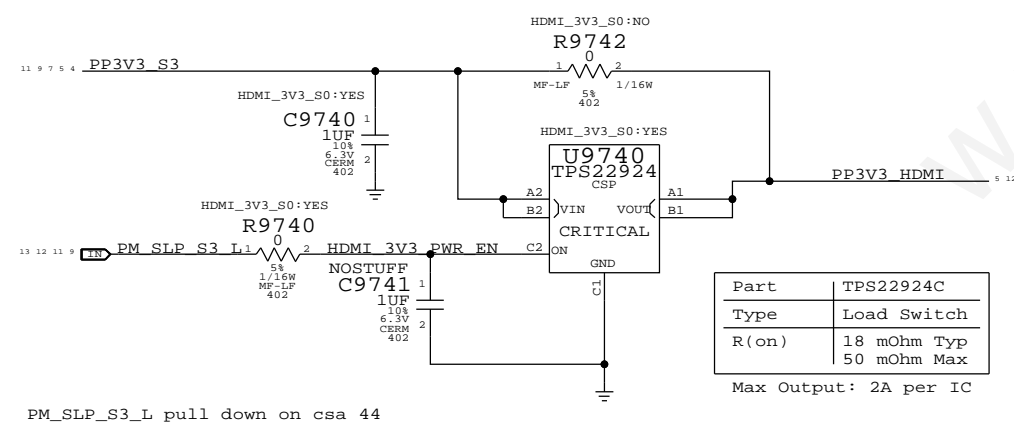
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0731	2	FERR BD,60mOHM, 0402	L9700,L9702	CRITICAL	
338S1089	1	HDMI REPEATER - A3	U9700	CRITICAL	

max 1.5V current <400mA
max 3.3V current <30mA
max 1.5V_VDDRX current <180mA
max 1.5V_VDDTX current <200mA
max 1.5V_VDDTA current <20mA



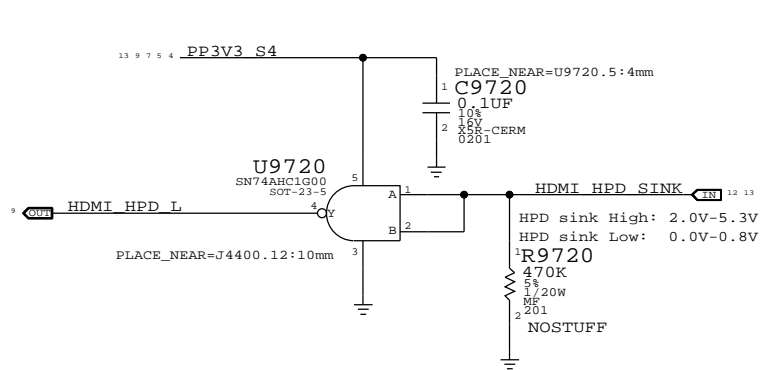
CFG=L, HDMI ID disabled
CFG=H, HDMI ID enabled
ISET= L, output swing default
ISET= H, output swing +13%
ISET= M, output swing -13%
PD# =L, PS8401 power down
PD# =H, PS8401 in normal mode
DEFAULT I2C = 0xCC (write) / 0xCD (read)

HDMI 3.3V_S0 Switch



PM_SLP_S3_L pull down on csa 44
Max Current = 30mA (HDMI 3V3_S0 only)

HDMI HPD 5.0V to 3.3V Level Shift



I2C control enabled when R9702 is stuffed

I2C_ADDR1	I2C_ADDR0	I2C ADDRESS(W/R)
L	L	0x4C/4D (default)
L	H	0x5C/5D
H	L	0xCC/CD
H	H	0xEc/ED

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HDMI SHIFTER

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HDMI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDMI_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDMI	TOP,BOTTOM	=5X_DIELECTRIC	?
HDMI	ISL3,ISL5,ISL6	=4X_DIELECTRIC	?

SOURCE: AMD/NV CONSTRAINS

PCIE Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	0.381 MM	?
PCIE	*	0.381 MM	?
CLK_PCIE	*	0.508 MM	?

SOURCE: J5 MLB

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	0.381 MM	?
USB	*	0.381 MM	?

SOURCE: Intel document 467283

USB 3.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3	TOP,BOTTOM	0.381 MM	?
USB3	ISL3,ISL5,ISL6	=4X_DIELECTRIC	?

SOURCE: Intel document 467283

CAESAR IV (SD) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_DATA	*	8 MIL	?

SOURCE: K90i

USB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFF PAIR
	PHYSICAL	SPACING	
USB_EXTR	USB_85D	USB	USB_EXTR USB_EXTB P 9 10
USB3_EXTR_TX	USB3_85D	USB3	USB_EXTR USB_EXTB N 9 10
USB3_EXTR_TX	USB3_85D	USB3	USB3_EXTB TX P 4 9 10
USB3_EXTR_TX	USB3_85D	USB3	USB3_EXTB TX N 4 9 10
USB3_EXTR_RX	USB3_85D	USB3	USB3_EXTB RX P 4 9 10
USB3_EXTR_RX	USB3_85D	USB3	USB3_EXTB RX N 4 9 10
USB_EXTR	USB_85D	USB	USB_EXTRC USB_EXTB F P 4 10
USB_EXTR	USB_85D	USB	USB_EXTRC USB_EXTB F N 4 10
USB3_EXTR_TX	USB3_85D	USB3	USB_EXTRC_TX USB3_EXTB TX F P 4
USB3_EXTR_TX	USB3_85D	USB3	USB_EXTRC_TX USB3_EXTB TX F N 4
USB3_EXTR_RX	USB3_85D	USB3	USB_EXTRC_RX USB3_EXTB RX F P 4
USB3_EXTR_RX	USB3_85D	USB3	USB_EXTRC_RX USB3_EXTB RX F N 4

PCIE Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFF PAIR
	PHYSICAL	SPACING	
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET R2D P 8
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET R2D N 8
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET R2D C P 8 9
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET R2D C N 8 9
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET D2R P 8 9
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET D2R N 8 9
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET D2R C P 8
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET D2R C N 8
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M ENET P 8 9
PCIE_CLK100M	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M ENET N 8 9

HDMI Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFF PAIR
	PHYSICAL	SPACING	
HDMI_DATA_LS	HDMI_90D	HDMI	HDMI_DATA C P<2..0> 4 9 12
HDMI_DATA_LS	HDMI_90D	HDMI	HDMI_DATA C N<2..0> 4 9 12
HDMI_CLK_LS	HDMI_90D	HDMI	HDMI_CLK C LS P 9 12
HDMI_CLK_LS	HDMI_90D	HDMI	HDMI_CLK C LS N 9 12
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA P<2..0> 4 12 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA N<2..0> 4 12 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK P 12 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK N 12 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA CONN P<2..0> 4 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA CONN N<2..0> 4 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK CONN P 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK CONN N 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA LS P<2..0> 12
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA LS N<2..0> 12
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK LS P 12
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK LS N 12
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA FLT P<2..0> 13
HDMI_DATA	HDMI_90D	HDMI	HDMI_DATA FLT N<2..0> 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK FLT P 13
HDMI_CLK	HDMI_90D	HDMI	HDMI_CLK FLT N 13

SD Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		DIFF PAIR
	PHYSICAL	SPACING	
CR_DATA	ENET_50S	SD_DATA	SDCONN_DATA<7..0> 7 8
CR_DATA	ENET_50S	SD_DATA	SDCONN_CMD 7 8
CR_CLK	ENET_50S	SD_DATA	SDCONN_CLK 7 8
CR_DATA	ENET_50S	SD_DATA	SDCONN R DATA<7..0> 7
CR_DATA	ENET_50S	SD_DATA	SDCONN_CMD R 7
CR_CLK	ENET_50S	SD_DATA	SDCONN_CLK R 7
CR_CLK	ENET_50S	SD_DATA	SDCONN ENET CLK R 8

SYNC MASTER=K92_YUN		SYNC DATE=06/25/2010	
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RIO (J5) Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS			BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, BOTTOM				NO_TYPE			MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.110 MM	0.110 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	ISL3	Y	0.085 MM	0.085 MM			
50_OHM_SE	ISL5, ISL6	Y	0.115 MM	0.115 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	TOP,BOTTOM	Y	0.112 MM	0.112 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL3	Y	0.101 MM	0.101 MM		0.140 MM	0.140 MM
85_OHM_DIFF	ISL5, ISL6	Y	0.118 MM	0.118 MM		0.130 MM	0.130 MM

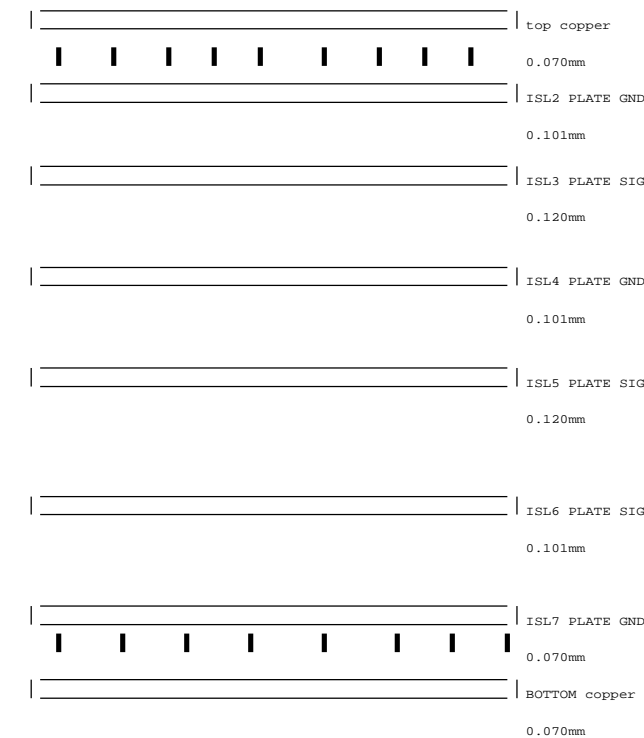
PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.130 MM	0.130 MM
90_OHM_DIFF	ISL3	Y	0.092 MM	0.092 MM		0.160 MM	0.160 MM
90_OHM_DIFF	ISL5, ISL6	Y	0.110 MM	0.110 MM		0.150 MM	0.150 MM

HDMI_keepout should be 1.016mm. However use 0.3mm per layout restriction
HDMI_spacing should be 0.635mm. However use 0.3mm per layout restriction

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1X_DIELECTRIC	TOP,BOTTOM	0.070 MM	?
1X_DIELECTRIC	ISL3	0.120 MM	?
1X_DIELECTRIC	ISL5	0.120 MM	?
1X_DIELECTRIC	ISL6	0.120 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.350 MM	?
3X_DIELECTRIC	ISL3, ISL5, ISL6	0.360 MM	?
4X_DIELECTRIC	ISL3, ISL5, ISL6	0.480 MM	?

NOTE: Based on RIO (J5) stackup 08/26/11.



SYNC MASTER=K17_MLB		SYNC DATE=05/14/2010	
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