3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
### BOM Variants

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### J30 BOM GROUPS

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### Module Parts

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### Bar Code Labels / EEEE #’s

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### Programmable Parts

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### Alternate Parts

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### Sub BOM

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The image contains a schematic diagram of a component, likely a circuit board, with various labels and reference designators. The diagram includes numbered rows and columns, possibly representing different components or connections. The specific details and components are not clearly visible due to the resolution of the image.
If HDA = S0, must also ensure that signal cannot be high in S3.

Unused clock terminations for FCIM Mode

Unused clock terminations for FCIM Mode
Systems with chip-down memory should add pull-downs on another page and set strings per software.

Revised: 2018-05-08
Sheet: 12
Page: 19
Branch: 124578

SHEET_BOMGROUP_HEAD

PCH GPIO/MISC/NCTF

Apple Inc. 081-3088-0

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PAGE TITLE

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1. Systems with chip-down memory should pull all 4 RAMCFG GPIOs high.
2. Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
3. This has internal pull up and should not pulled low.
4. Set to Vss when Low
5. Set to Vcc when High

- 1/20W
- 10K
- 5%
- 201
- MF
- 0

---
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software to S3 to S0

![Circuit Diagram]

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L

1V5 S0 "PGOOD" for CPU

MEMVTT Clamp
Ensures CKE signals are held low in S3

PM_MEM_PWRGD_L pull-up to CPU VTT rail is on CPU page

CPU Memory S3 Support
### Page Notes

Date: 02/15/2011

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---

### Ethernet Connector

- **XSMT, ISO, HALF-PORT, 1000T, 12P, SMD, HF**
- **T4000, T4001**
- **157S0084**

#### Signal Aliases Required by this Page:

- ENET_MDI_P<1>
- ENET_MDI_P<2>
- ENET_MDI_N<1>
- ENET_MDI_P<3>
- ENET_MDI_N<2>
- ENET_MDI_N<3>
- ENET_MDI_P<0>
- ENET_MDI_N<0>
- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

#### Power Aliases Required by this Page:

- ENETCONN_CTAP
- ENETCONN_P<0>
- ENETCONN_N<0>
- ENETCONN_P<1>
- ENETCONN_N<1>
- ENETCONN_P<2>
- ENETCONN_N<2>
- ENETCONN_P<3>
- ENETCONN_N<3>

#### Description:

- Place one of 0.1uf cap close to each centertap pin of transformer
  - Transformers should be mirrored on opposite sides of the board

#### BOM Options Provided by this Page:

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<thead>
<tr>
<th>Part Number</th>
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<td>C4002</td>
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<td>C4004</td>
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<td>R4000</td>
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<td>R4003</td>
<td>MF-LF 1/16W 5% 75</td>
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### Ethernet Connector

- **ENET_MDI_P<0>**
- **ENET_MDI_N<0>**
- **ENET_CTAP0**
- **ENET_CTAP1**
- **ENET_CTAP2**
- **ENET_CTAP3**

#### Physical Constraints:

- MIN_NECK_WIDTH=0.25 mm
- MIN_LINE_WIDTH=0.6 mm
USB Port Power Switch

Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux

USB Port A (Front Port)

www.qtzbwx.com
USB Port B (Back Port)

NOTE: Swapped pin 4 and 5, pin 6 and 7 for layout.
NOTE:
SMB Interrupt can be active high or low, rename out accordingly.
If SMB interrupt is not used, pull up to 3.3V exit.

NOTE:
Ground pins have "NC_Pwm" names. Unused
pins designated as outputs can be left floating,
those designated as inputs require pull-ups.
Thermal Sensor: CPU Proximity, Fin Stack, Memory Proximity, 5V/3.3V Proximity

Thermal Diode: Fin Stack
- Place (X5510) on the TOP side.
- Close to Fin Stack.

Thermal Diode: Memory Proximity
- Place (Q5520) on the BOTTOM side.
- Next to 5V and 3.3V power supplies.

Thermal Sensor: T29 Die
- Place (Q5520) on the TOP side.
- Close to Fin Stack.
- Place (Q5510) on the BOTTOM side, close to Fin Stack.

Thermal Diode: 5V/3.3V Proximity
- Place (X5520) on the TOP side.
- Close to 5V and 3.3V power supplies.

NOSTUFF
BOOSTER +18.5VDC FOR SENSORS

BOOTER DESIGN CONSIDERATION:
- DROOP LINE REGULATION
- R5812, R5813, C5818 MODIFIED
- STARTUP TIME LESS THAN 2MS

VOLTAGE=5V
MIN_NECK_WIDTH=0.20MM
MIN_LINE_WIDTH=0.50MM

To detect Keyboard backlight, SMC will:
If HIGH, keyboard backlight not present
grounded when KB BL flex connected.

Keyboard Backlight Driver & Detection

Keyboard Backlight Connector
DIGITAL MIC - Only for mock ups as of July 2011
I2C ADDRESSES: CHS uses SMBus 0 connections

CHS    U6400    WRITE   0111    0110    0x76
CHS    U6400    READ    0111    0111    0x77

VOLTAGE=3.42V
MIN_NECK_WIDTH=0.25 MM
MIN_LINE_WIDTH=0.3 MM

EXT_MIC_BIAS
EXT_MIC_N
CPU VCCIO (1.05V S0) Regulator

Vout = 1.05V

20.1A Max Output

f = 300 kHz

Vout = 0.5V * (1 + Ra / Rb)

OCP = R7641 x 8.5uA / R7640

OCP = 26.265A

Vout = 0.5V * (1 + Ra / Rb)

OCP = R7641 x 8.5uA / R7640

OCP = 26.265A
**LCD Backlight Driver**

Apple Inc. 051-9058

**PART NUMBER**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
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<th>NOM OPTION</th>
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<td>33PF 50V C0G-CERM 1/16W 5%</td>
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<td>D3</td>
<td>1</td>
<td>10UF X5R 25V</td>
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<tr>
<td>C2</td>
<td>1</td>
<td>0.1UF X5R 10%</td>
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<td>C5</td>
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**Notes:**
- Place Near: U9701.D1:3mm
- Place Near: U9701.E1:10mm
- Place Near: U9701.E2:10mm
- Place Near: U9701.E3:10mm

**Critical Components:**
- BKL:ENG
- VSYNC
- FSET
- ISET
- EN
- FILTER
- PWM

**Resistors:**
- 21 402 MF-LF 1/16W 10.2 OHM 0.1,0402,SM
- 33 402 MF-LF 1/16W 0.1,0402,SM

**(loadings:**
- **PPBUS_S0_LCDBKLT_FUSED**
- **PPBUS_S0_BKL**
- **PPVOUT_SW_LCDBKLT_FB**

**Notes:**
- CRITICAL
- LED_RETURN_1
- LED_RETURN_2
- LED_RETURN_3
- LED_RETURN_6

**Remarks:**
- *LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

**Additional Information:**
- Place Side: Bottom
- TP_BKL_FAULT

**Warning:**
- MIN LINE WIDTH = 0.5 mm
- MIN NECK WIDTH = 0.20 mm

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NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

CPU Signal Constraints

CPU Net Properties

CPU Constraints
Memory Bus Constraints

DQ to DQS matching per byte lane should be within 0.127mm.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
### USB 2.0 Interface Constraints

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<th>Layer 2 (mm)</th>
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**Notes:**
- Layer 1 and Layer 2 are unused.
- The spacing is set per layer.

### SATA Interface Constraints

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**Notes:**
- Layer 1 and Layer 2 are unused.
- The spacing is set per layer.

### USB 3.0 Interface Constraints

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**Notes:**
- Layer 1 and Layer 2 are unused.
- The spacing is set per layer.
### FireWire Interface Constraints

**SPACING_RULE_SET**

- **ENET_100D**
- **ENET_50S**
- **FW_110D**
- **ENET_3X**
- **FW_TP**

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**ELECTRICAL_CONSTRAINT_SET**

- **I165**
- **I164**
- **I163**
- **I162**
- **I161**
- **I160**
- **I159**
- **I158**

**Port 2 Not Used**

- **ENET_MDI**
- **ENET_3X**
- **ENET_50S**

**Ethernet Net Properties**

- **ENET_MDI**
- **ENET_CR_DATA**
- **ENET_CR_CLK**

**Physical Rule Set**

- **MINIMUM LINE WIDTH**
- **MAXIMUM NECK LENGTH**
- **DIFFPAIR PRIMARY GAP**
- **DIFFPAIR NECK GAP**
### DisplayPort Signal Constraints

**NOTE:** DisplayPort Physical/spacing Constraints provided by Chipset or GPO page.

#### T29 I2C Signal Constraints

<table>
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<th>Net Type</th>
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<th>Class</th>
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<th>Notes</th>
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#### T29 SPI Signal Constraints

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*Table not fully visible.*

#### T29/DP Connector Signal Constraints

- **T29_DP**
- **T29_SPI**
- **T29_I2C**

*Table not fully visible.*

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**SOURCE:** Bill Corrigan’s T29 Routing Notes

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### T29/DP Net Properties

- **Electrical Constraint Set**
- **Physical Constraint Set**

*Tables not visible.*

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### SMC SMBus Net Properties

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### SMBus Charger Net Properties

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<th>Net Set Name</th>
<th>Net Set Description</th>
<th>Type</th>
<th>&quot;Constraint&quot;</th>
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<td>CHGR_CSI_P</td>
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### SMC Constraints

- **Sync Master**: K90I_MLB
- **Sync Date**: 02/15/2011
- **Sync Master**: +STANDARD
- **Sync Master**: +STANDARD
- **Sync Master**: +STANDARD
- **Sync Master**: +STANDARD
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- **Sync Master**: +STANDARD
- **Sync Master**: +STANDARD
- **Sync Master**: +STANDARD
### Table: Board-Specific Spacing & Physical Constraints

<table>
<thead>
<tr>
<th>Impedance</th>
<th>Layer</th>
<th>Minimum Line Width</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
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<tbody>
<tr>
<td>37_OHM_SE</td>
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<tr>
<td>40_OHM_SE</td>
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<td>0.145 MM</td>
<td>0.090 MM</td>
<td>10 MM</td>
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<tr>
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<td>0.068 MM</td>
<td>0.090 MM</td>
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<tr>
<td>110_OHM_DIFF</td>
<td>TOP, BOTTOM</td>
<td>0.085 MM</td>
<td>0.1 MM</td>
<td>10 MM</td>
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<tr>
<td>110_OHM_DIFF</td>
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<td>0.080 MM</td>
<td>0.1 MM</td>
<td>10 MM</td>
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<td>100_OHM_DIFF</td>
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<tr>
<td>80_OHM_DIFF</td>
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<td>0.235 MM</td>
<td>0.190 MM</td>
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<tr>
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<tr>
<td>85_OHM_DIFF</td>
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<td>0.190 MM</td>
<td>0.190 MM</td>
<td>10 MM</td>
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*NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.*