ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
System Block diagram can be found on Kismet

PATH: Kismet > K70/72 > Block Diagrams > K70 Block Diagram
S5 Led

ALL_SYS_PWRGD Led

GPU GOOD Led

VIDEO ON Led

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=2

LED502

2N7002DW-X-G SOT-363 Q502

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=4

LED504

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=1

LED501

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=3

LED503

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=1

LED501

ALL_SYS_PWRGD Led

GPU GOOD Led

VIDEO ON Led

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=2

LED502

2N7002DW-X-G SOT-363 Q502

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=4

LED504

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=1

LED501

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=3

LED503

CRITICAL GREEN-3.6MCD 2.0X1.25MM-SM SILK_PART=1

LED501
CPU Heatsink
4mm Plated Holes (998-0850)

WIRELESS CARD MTG HOLES
998-4560 (Plated holes, 2.3mm inner diameter, 4.3mm pad)

Rear Cover
998-4559 (Plated holes, 4mm inner diameter, 8mm pad)

USB Can holes
998-3975 (Plated slot holes, 1.10mm x 0.45mm)

SSD STANDOFF
998-60-1461

Holes/PD parts

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Apple Inc.
051-8179
160.0.0
7 of 113
7 of 90
unused GPU aliases

SMC-EG pull up and pull down

CPU PCH FDI BUS

PCH DP ALIAS

Signal Aliases
VAXG DECOUPLING

INTEL RECOMMENDATION 44220P 0805, 22UF, 5% 0.12A - 0.36OHM

Place inside socket cavity.

C1704
0.12A 0.36OHM

R1720

C1705
0.12A 0.36OHM

R1730

C1740
0.12A 0.36OHM

Table 5

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1704</td>
<td>0.12A 0.36OHM</td>
<td>1</td>
<td>R1720</td>
</tr>
<tr>
<td>C1705</td>
<td>0.12A 0.36OHM</td>
<td>1</td>
<td>R1730</td>
</tr>
<tr>
<td>C1740</td>
<td>0.12A 0.36OHM</td>
<td>1</td>
<td>R1740</td>
</tr>
</tbody>
</table>

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PLACE THE RESISTOR VERY CLOSE TO COMMON POINT
SHORT THESE TWO PINS VERY NEAR THE PINS
This should stay as RTC, correct?

PCH output, for decoupling only

PLACE_NEAR=U1800.BU42:2mm

PLACE_NEAR=U1800.BA46:2mm

0.1UF

201

10%

X5R

6.3V

C2222

2

1

CERM

0.1UF

402

CERM

10V

20%

C2210

PLACE_NEAR=U1800.BU42:2mm

PCH output, for decoupling only

2

1

1UF

402

CERM

6.3V

10%

1UF

402

CERM

10V

20%

PLACE_NEAR=U1800.BU42:2mm

Need to check layout decoupling

=PP3V3_S5_PCH_VCC_DSW

=PP1V8_S0_PCH_VCC_DFTERM

=PP3V3_S0_PCH_VCC_GPIO

105mA Max, 90mA Idle

55mA Max, 5mA Idle

200 mA Max, 2mA Idle

=PP1V05_S0_PCH_VCC_SSC

=PP1V05_S0_PCH_VCC_DIFFCLK

=PP3V3_S5_PCH_VCC_SPI

20mA Max, 1mA Idle

3mA Max, 1mA Idle

Max and Idle = 1mA

40mA Max, 10mA Idle

40mA Max, 5mA Idle

PP1V05_S0_PCH_VCCADPLLB_F

TP_PPVOUT_PCH_DCPSSTYP

PP1V05_S0_PCH_VCCADPLLA_F

TP_DCPSUS_2

TP_DCPSUS_1

TP_DCPSUS_0

MIN_LINE_WIDTH=0.2 mm

VOLTAGE=3.3V

VOLTAGE=3.3VMIN_LINE_WIDTH=0.2 mm

MIN_NECK_WIDTH=0.2 mm

VCCADPLLB

VCCSPI

VCCDSW3_3

VCCDFTERM1

V_PROC_IO_NCTF

V_PROC_IO

DCPSST

V5REF_SUS

VCC3_3

VCCIO

V5REF

VCCAPLLSATA

VCCSUS3_3

VCCSUSHDA

VCCAPLL_EXP

PP1V05_S0_PCH_VCCAPLL_EXP

=PP3V3_S0_PCH_VCC

=PP3V3_S0_PCH_VCC_PCI

=PP5V_S5_PCH_V5REFSUS

=PP1V05_S0_PCH_VCCIO_USB

PP1V05_S0_PCH_VCCIO_DMI

PP1V05_S0_PCH_VCC_DMI

PP1V8_S0_PCH_VCCVRM_F

PP1V05_S0_PCH_VCCIO_PCIE

PANTHER-POINT

U1800

FCBGA

CLOCK AND MISCELLANEOUS

CPURTC

PCI/GPIO/LPC

HDA

PCI/GPIO/LPC

VCCAPLLDMI2

VCCAFDIPLL

VCCCLKDMI

VCCCORE

VCC3_3

VCCIO_DMI/CLK

VCCCORE

VCC3_3_0

VCCVRM0

VCCVRM1

VCCVRM2

VCCADAC

VCCASW

SYNC_DATE=01/19/2012

SYNC_MASTER=D7_MLB

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Apple Inc. 051-9179 16.0.0

22 OF 113

22 OF 90
Power Sequencing

1V05 S0 Rails

1V8 S0 Rails

3V3 S5 Rails

3V3 S0 Rails
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the S0-DIMMs when necessary.

**ISOLATE_CPU_MEM_L**

**MEMVTT_EN** = PM_PGOOD_FET_VDDQ_S0 * PM_SLP_S3_L

**MEM_RESET_L** = !ISOLATE_CPU_MEM_L & CPU_MEM_RESET_L

**WHEN HIGH**: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

**WHEN LOW**: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

**NOTE**: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

---

**1V5 S0 "PGOOD" for CPU**

- **MEM_RESET_L** = PP5V_S4_MEMRESET
- **MEMVTT_EN** = PP5V_S4_MEMRESET
- **MAKE_BASE** = TRUE

---

**MEMVTT Clamp**

Ensures CKE signals are held low in S3

---

**CPU Memory S3 Support**
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating.
Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC.
In the event that it is pulled up to 5V/12V inside the fan, otherwise when Q5610 is on, there would be 5V/12V power on the AG pin. Thus by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on. This resembles an open-drain if there is a pull-up going to a Hi-Z FET input. Otherwise, this is simply a pass-FET.
APPLE P/N 353S2456

4.5V POWER SUPPLY FOR CODEC
S5 Soft Enable

S4 Enables

S4 USB Enable

S3 VDDQ Enable

PM PGOOD FET_P12V_S0

PM_SLP_S3_L

NVIDIA:

Notes on sequencing requirements

1. 3V3_S0 must ramp first

2. IFPA/B_IOVDD (1.8 V) can ramp simultaneously or after 3V3_S0 (unused)

3. VDDQ must ramp after CPU_CORE

4. PEX_VDD with IFPC/D/E/F_IOVDD (1.05V) must ramp after VDDQ

5. No hard specification on platform rails

Note:
or short gate to source.

Remove Q6900 to circumvent

Rail definitions

Platform: All processor variants and non-OptiPlex (S 8, 3.3 V, 1.8 V 1.9 V, FBC Core/FG/TFM)

Sequencing Notes:

1. No hard specification on platform rails

2. PERIOD controlled in 3V3_S0 and 3V3_S5

Notes on sequencing requirements

1. 3V3_S0 must ramp first

2. CPU_CORE (1.3V) must ramp simultaneously or after 3V3_S0 (required)

3. VDDQ (3.3V/2.5V) must ramp after CPU_CORE

4. USB must ramp after 3V3_S0

5. PERIOD with SPECIFIC_VDD (1.25) must ramp after USB

6. All rails must reach their target values in more than 30 ms

C6901

CERM-X5R

C6900

0.1UF

X5R

0.1UF

X5R

2

33K

MF-LF

1/16W

100

5%

402

71

14

7

13

6 3

28 71

IN

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IN

IN

IN

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Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

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PCH Power Goods

The SMC guarantees proper assertion and de-assertion of RSMRST# for To PCH

normal operation via PM_DSW_PWRGD.

The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and
To PCH
RSMRST# signals are shorted together

Primary method:
- Asserted at least 10 ms after all suspend well power is valid
- Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V
- 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.

Secondary method:
- SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from
To PCH
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and

Note: GPU power goods are implicitly included because the power goods for VDDQ, DPVDDC, and GPU Core are wired-or together

Secondary method:
- To SMC, for 99ms delay
- To PCH

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8
CPU VccIO/PCH (1.05V) S0 Regulator

Max avg current: 7 A (design) / 14.38 A (budget)
Max peak current: 7 A (design) / 18.38 A (budget)
OC trip point: 2 A (min) / 7 A (max)
Switching freq: 500 kHz

[Diagram of circuit components and connections]
3.425V "G3Hot" Regulator

Max avg current: 7 A (design) / 0 A (budget)
Max peak current: 7 A (design) / 0.06 A (budget)
Switching freq: 7 kHz

12V S5 FET
Max avg current: 7.03 A (budget)
Max peak current: 9.49 A (budget)

---

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Max peak current: ? A (design) / 0 A (budget)
Max avg current: ? kHz
Switching freq: 7 kHz
On a H→L transition of A, Y2 follows with standard logic propagation delay. This ensures the backlight is off immediately after loss of video.

The delay applies only on a L→H transition on A. This guarantees video is valid before the backlight is enabled.

Y1 is simply an inverted version of A, with no delay.

U9000 output Y2 is a non-inverted, delayed version of input A.
Dual-Port Host DDC Crossbar
3.3V/HV Power MUX

NOTE: Polarity Swapped for Layout!

IV3P3 must be S4 to support 20%

6.3V wake from Thunderbolt devices.

8 7 6 5 4 3

C9615 X5R-CERM 4.7UF

C9610 0.1UF X7R 10%

0.22UF 1 2

TBT_B_CONFIG2_RC

201

DESCRIPTION REFERENCE DES BOM OPTION QTYPART NUMBER CRITICAL

0.22UF 1 2

TBT_B_CONFIG1_BUF

1/20W MF-LF 1/16W, 17.8K, 1,0402, SMD, LF

0.01UF 50V 1/20W MF-LF 1/20W 5%

0.1UF 50V 1/20W MF-LF 1/20W 5%

VOLTAGE=18.9V MIN LINE_WIDTH=0.38 MM

0.01UF 50V 1/20W MF-LF 1/20W 5%

0.1UF 50V 1/20W MF-LF 1/20W 5%

VOLTAGE=3.3V

GND_VOID=TRUE

NOTE: Polarity Swapped for Layout!
### General Physical Rule Definitions

<table>
<thead>
<tr>
<th>PHYSICAL_RULE_SET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP, BOTTOM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON LAYER?</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.089 MM</td>
<td></td>
<td>0.145 MM</td>
<td>0.145 MM</td>
<td>0.085 MM</td>
<td></td>
</tr>
</tbody>
</table>

### General Spacing Definitions

<table>
<thead>
<tr>
<th>PHYSICAL_RULE_SET</th>
<th>LAYER</th>
<th>MINIMUM LINE WIDTH</th>
<th>ALLOW ROUTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP, BOTTOM</td>
<td></td>
<td>0.138 MM</td>
<td></td>
</tr>
</tbody>
</table>

### Board Stack-up

- Finished board thickness: 1.58 mm
- Top signal: 0.5 mm (Cu plated)
- Bottom signal: 0.5 mm (Cu plated)

### BGA Area Constraints

<table>
<thead>
<tr>
<th>PHYSICAL_RULE_SET</th>
<th>LAYER</th>
<th>MINIMUM NECK WIDTH</th>
<th>MAXIMUM NECK LENGTH</th>
<th>DIFFPAIR PRIMARY GAP</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP, BOTTOM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ON LAYER?</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.145 MM</td>
<td></td>
<td>0.215 MM</td>
<td>0.215 MM</td>
<td>0.085 MM</td>
<td></td>
</tr>
</tbody>
</table>

---

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### DDR3

#### DDR3-specific Physical Rules

<table>
<thead>
<tr>
<th>Physical Net Type to Rule Map DDR3 Power-specific Spacing Definitions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Physical DDR3</strong></td>
</tr>
<tr>
<td><strong>DDR_DATA_ISO</strong> *</td>
</tr>
<tr>
<td><strong>DDR_CTRL_PHY</strong> * DDR_39S *</td>
</tr>
<tr>
<td>? * 900 =68_OHM_DIFFDDR_39S * STANDARD 8 7 6 5 4 3</td>
</tr>
<tr>
<td>* * =34_OHM_SE =34_OHM_SE * =34_OHM_SE * =34_OHM_SE * =34_OHM_SE</td>
</tr>
<tr>
<td>* * 8.5 6 12 4LINE-TO-LINE SPACINGLAYERSPACING_RULE_SET WEIGHT</td>
</tr>
<tr>
<td>* * 7.87 7.87 9.84 9.84 3.0 MM0.400 MMPOWER_DDR_P4MM 0.100 MM</td>
</tr>
<tr>
<td><strong>Table 3-5, Intel Doc# 473718</strong></td>
</tr>
</tbody>
</table>

#### DDR3-specific Spacing Definitions

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Notes (1)</th>
<th>Notes (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Note: DDR1 01, DDR2 01, DDR3 01</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Physical Net Type in Rule Map DDR3 Power-specific Spacing Definitions

**Area Type SPACING_RULE_SETNET_SPACING_TYPE1 NET_SPACING_TYPE2**

#### Main Segment Min Spacing Rules (initial) (Main Bypass DDR, Intel Doc 473718)

**Data: DQS[7:0], DQS#[7:0], DQ[63:0]**

* DDR_A_DQ_BYTE* DDR_A_DQS* * DDR_DATA_ISO

* DDR_B_DQ_BYTE* * * DDR_DATA_ISO

* DDR_B_DQS5 DDR_B_DQS2 DDR_B_DQS1

In order for the constraints DDR_*_DQ_BYTE* to =SAME to win coupling however). These rules are far too conservative.

To meet these rules, the spacing must be applied to the net.

Only complexity to constraints, even though it can be less. Only

---

**NOTE:**

- Deliberately set 80p to 80p spacing to 81 to avoid making component-to-component variability too constraining, even though it can be less. Only those per channel is needed by looking at the circuit space.

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Physical Net Type to Rule Map

<table>
<thead>
<tr>
<th>Physical Net Type</th>
<th>Rule</th>
<th>Notes</th>
</tr>
</thead>
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Design

* = 80 OHM_DIFF
= 90 OHM_DIFF
* = 50 OHM_SE

Physical Net Type to Rule Map

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PCIE-specific Spacing Definitions

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Spacing Constraints

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CPU PCIe Constraints

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Apple Inc.
### SPI-specific Spacing Definitions

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### Physical Rules

- **HDA**
  - SPI ROM
  - SPI
  - SPDIF

- **LPC**
  - SPI

- **PCI**
  - SPI

- **PCH**
  - SPI

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### USB-specific Physical Rules

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### Physical Net Type to Rule Map

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### USB Min Spacing Rules (mil) (Maho Bay PDG, Intel Doc# 473718)

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### USB 3.0 and USB 2.0 Tristate Mapping

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### Camera Processor-Camera Sensor Interface Physical Rules

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<td>ENET_RS</td>
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<td>ENET_MDI</td>
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<td>ENET_TRANS</td>
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### DC-DC Control

#### DC-DC Control

<table>
<thead>
<tr>
<th>Power-specific Physical Rules</th>
<th>Power and Common Constraints</th>
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<tbody>
<tr>
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<table>
<thead>
<tr>
<th>Physical Rule</th>
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<th>Options</th>
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<tr>
<td>VR_CTL_PHY</td>
<td>POWER_ISO</td>
<td>1000 = STANDARD</td>
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#### Power-specific Spacing Definitions

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<thead>
<tr>
<th>Power and Common Constraints</th>
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<tbody>
<tr>
<td>VR_SWITCH *BGA BGA_P1MM</td>
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</tbody>
</table>

**Physical Rule Set**

- **Layer**
  - Minimum: 0.150 MM
  - Maximum: 3.0 MM

- **Spacing**
  - 8:1_SPACING
  - 7:1_SPACING
  - 6:1_SPACING

**Physical Assignments**

- **Area Type**
  - NET_PHYSICAL_TYPE

- **Net Physical Type**
  - TABLE_PHYSICAL_ASSIGNMENT_HEAD
  - TABLE_PHYSICAL_ASSIGNMENT_ITEM

**Spacing Rule Set**

- **Line-to-Line Spacing**
  - TABLE_SPACING_RULE_HEAD
  - TABLE_SPACING_RULE_ITEM
  - TABLE_SPACING_RULE_ITEM

**Spacing Assignments**

- **Net Physical Rule**
  - TABLE_PHYSICAL_RULE_ITEM
  - TABLE_PHYSICAL_RULE_ITEM
  - TABLE_PHYSICAL_RULE_ITEM

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### CPU VoCIS/ PC1 1.05V S0

#### Electrical Constraints Set

<table>
<thead>
<tr>
<th>Input Bus</th>
<th>Output Spacing</th>
<th>Voltage</th>
<th>Data Rate</th>
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<tbody>
<tr>
<td>PPVCCSA_S0</td>
<td>.150 MM .300 MM 3.0 MM</td>
<td>1.05V</td>
<td>NOT Codable</td>
</tr>
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</table>

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### CPU VoCISA

#### Electrical Constraints Set

<table>
<thead>
<tr>
<th>Input Bus</th>
<th>Output Spacing</th>
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</table>
### CPU Core Phases

<table>
<thead>
<tr>
<th>Physical</th>
<th>Spacing</th>
<th>Voltage</th>
<th>DC/DC</th>
<th>AC/DC</th>
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<tbody>
<tr>
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### CPU AXG Phase and Core Controller

<table>
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<tr>
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<th>AC/DC</th>
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### CPU VReg Constraints

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### BLC Constraints

#### Backlight Controller

**BLC-specific Physical Rules**

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<thead>
<tr>
<th>Net Name</th>
<th>Line</th>
<th>Min Width</th>
<th>Max Width</th>
<th>Min Length</th>
<th>Max Length</th>
<th>Num</th>
<th>Note</th>
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<tbody>
<tr>
<td>BLC_CTL_PHY</td>
<td>Y</td>
<td>0.100</td>
<td>3.0</td>
<td>0.300</td>
<td>1.0</td>
<td>8</td>
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</tr>
<tr>
<td>BLC_P3MM</td>
<td>Y</td>
<td>0.100</td>
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<td>6</td>
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**BLC-specific Spacing Definitions**

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<tr>
<th>Net Name</th>
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<th>Note</th>
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<tbody>
<tr>
<td>BLC_CTL_COPY</td>
<td>Y</td>
<td>0.100</td>
<td>3.0</td>
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<td>BLC_P3MM_COPY</td>
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**Backlight Controller**

**BLC Control**

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**BLC High Voltage Output**

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<th>Line</th>
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<th>Num</th>
<th>Note</th>
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<tbody>
<tr>
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<td>BLC_P3MM ISO</td>
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**BLC Phase**

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**Cell Miscellaneous**

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<thead>
<tr>
<th>Physical Layer</th>
<th>Spacing</th>
<th>Volume</th>
<th>COST</th>
<th>BLK/REV</th>
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<td>Secondary Layer</td>
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<td>0.100</td>
<td>0.05</td>
<td>0.00</td>
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</tbody>
</table>

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Is it chel'oh or sel'oh?