### J11 MLB PIB SCHEMATIC

**2.6.0**

**02/23/12**

<table>
<thead>
<tr>
<th>Page</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>J13_MLB</td>
</tr>
<tr>
<td>2</td>
<td>K21_MLB</td>
</tr>
<tr>
<td>3</td>
<td>J30_MLB</td>
</tr>
<tr>
<td>4</td>
<td>J13_MLB</td>
</tr>
<tr>
<td>5</td>
<td>K21_MLB</td>
</tr>
<tr>
<td>6</td>
<td>J13_MLB</td>
</tr>
<tr>
<td>7</td>
<td>J13_MLB</td>
</tr>
<tr>
<td>8</td>
<td>J13_MLB</td>
</tr>
<tr>
<td>9</td>
<td>J13_MLB</td>
</tr>
<tr>
<td>10</td>
<td>J13_MLB</td>
</tr>
<tr>
<td>11</td>
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<td>12</td>
<td>J13_MLB</td>
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**Product Safety Requirements:**

PCB, UL Recognized, MIL-120-C Temp. Rating and V-0 Flame Rating per UL 746a & UL 94.

**PCB to be PC/12-12%**

**PCB P/N:**

**PCB Material Designation:**

**In 110-2 Temp. Rating and V-0 Flame Rating.**

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<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
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**Bar Code Labels / EEEE #'s**

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<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
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<tbody>
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<td>2.7.0</td>
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<td></td>
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<td></td>
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**ROM Variants**

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<th>ROM NUMBER</th>
<th>ROM DSOR</th>
<th>ROM OPTIONS</th>
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</tbody>
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**Sub-BOMs**

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<th>QTY</th>
<th>DESCRIPTION</th>
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<th>BOM OPTION</th>
</tr>
</thead>
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**K78 ROM Variants**

Apple Inc. 051-9276 2.7.0

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### Alternate Parts

<table>
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<th>PART NUMBER</th>
<th>QTY</th>
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<th>CRITICAL</th>
<th>ROM OPTION</th>
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### Programmable Parts

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### DRAM CFG CHART

```
A1
A2
A3
A4
A5
A6
A7
A8
```

### Module Parts

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<th>QTY</th>
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### PD Module Parts

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### DDR3

- SAMSUNG_4GB
- HYNIX_4GB

### J11_DEBUG

- PVT
- ENG

### Reference Descriptions

- ALTERNATE
- BKLT:ENG
- XDP_CONN
- XDP_PCH
- DDRVREF_DAC
- VREFDQ:M1_M3
- VREFCA:LDO_DAC
- S0PGOOD_ISL
- S3_S0_LED
- VCCIOISNS_ENG
- AIRPORTISNS_ENG
- HDDISNS_ENG
- LCDBKLTISNS_ENG

### Notes

- Murata alt to Samsung
- Fairchild alt to Siliconix
- Toko alt to NEC inductor
- Diodes alt to Toshiba
- Rohm alt to Toshiba

### Other

- IC,SMC,PIB,J11
- CRITICAL
- BOOTROM_BLANK
- TBTROM:BLANK
- TBTROM:PROG
- SMC_BLANK
- ELPIDA_8GB
- ELPIDA_4GB
- PCH_C1TDP
- PCH_C1
- PCH_C0
- IVB,QC9C,QS,L1,1.9,17W,2+2,1.15,4M,ULVBG
- IVB,QC9E,QS,L1,1.7,17W,2+2,1.05,3M,ULVBG
- IVB,QC9B,QS,L1,2.0,17W,2+2,1.15,4M,ULVBG
- IVB,QBP8,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB
If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard.

Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation. Therefore, an inverting level shifter is required on the motherboard.

CFG [4]: eDP ENABLE/DISABLE 1 = DISABLED 0 = ENABLED

These can be placed close to J2500 and only for debug access.
Redundant to pull-down on audio page

---

NO STUFF

---

5%

---

1/20W

---

BLC_I2C_MUX_SEL

---

TP_PCH_STRP_ESI_L

---

PCH_GPIO54

---

BLC_GPIO

---

AUD_I2C_INT_L

---

TBT_PWR_REQ_L

---

JTAG_GMUX_TMS

---

PCH_CLK33M_PCIOUT

---

TP_PCH_STRP_BBS1

---

TP_PCI_CLK33M_OUT3

---

PLT_RESET_L

---

USB3_EXTA_TX_P

---

USB3_EXTC_TX_N

---

USB3_EXTA_TX_N

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USB3_EXTD_RX_P

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USB3_EXTA_RX_P

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USB3_EXTB_RX_N

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USB3_EXTA_RX_N

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BJ27

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BF26

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BL27

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BF30

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BB28

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BF26

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AD10

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AR42

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AR40

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AN42

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AN40

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BH16

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BK16

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BH20

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BK24

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F40

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F45

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C41

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A47

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D44

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F46

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G46

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C45

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C47

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C48

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F46

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G46

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C45

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C47

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C48

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A47

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D44

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F45

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C41

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F40

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K30

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W40

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D24

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B24

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AT4

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D20

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E3

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E49

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H48

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J43

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H48

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J43

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G45

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F45

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F40

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F46

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G46

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C45

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C47

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C48

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A47

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D44

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F45

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C41

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F40

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K30

---

W40

---

D24

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B24

---

AT4

---

D20
Systems with no chip-down memory should pull all 4 RAMCFG GPIO high.

Systems with chip-down memory should pull all 4 RAMCFG GPIO high and pull-opens on another page and set straps per software.

NOTE: TCK from PCH is Push-Pull CMOS
NOTE: TDO from CR is Push-Pull CMOS

JTAG Isolation due to glitch in and out of sleep

TBT_PWR_EN goes high for JTAG Programming

This has internal pull up and should not pulled low.

THE SIGNAL IS INTENDED FOR FIRMWARE HUB AND WE ARE NOT USING IT.
must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

When HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.
A16/A15 FOR 2G/8G MODE ONLY
C01 IS FOR 2G DQIP BANK CONTROL
Right USB Port A

USB Port Power Switch

Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux

APN: 514-0819

External A USB3 Connector

SYNC_MASTER=J13_MLB
SYNC_DATE=10/06/2011
LIO CONNECTOR
998-4617 (HIROSE 3.0mm RCPT)

---

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**LIO CONNECTORS**

Apple Inc.

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Page 12 of 109

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---
CPU Proximity Sensor

Read Address: 0x99
Write Address: 0x98

Placement note:
To connect Die Sensor, stuff R5550 & R5551, no stuff R5540 & R5541
To connect Proximity Sensor, stuff R5540 & R5541, no stuff R5550, R5551

Detect TBT Die Temperature

Placement note:
Place U5510 under CPU

Replacing caps with 100K PD on ISENSE SMC inputs

TBT Die

Sync Date: 08/30/2011
Sync Master: J13_MLB

Thermal Sensors

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Page Title
Sheet
Version
Drawing Number
Revision
Branch
Size

4 5 6 7 8

1 2 3 4

5 6 7 8

1 2 3 4

5 6 7 8

1 2 3 4

5 6 7 8

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FAN CONNECTOR

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**Component List:**

- **R5661**: 100k Ω 1/20W
- **R5660**: 4.7k Ω 1/20W
- **Q5660**: SSM3K15FV SOD-VESM-HF
- **5% 1/20W MF201**: 47k
- **5% 1/20W MF201**: 100k

---

**Other Elements:**

- **SYNC_DATE=12/13/2010**
- **SYNC_MASTER=K21_MLB**
- **051-9276 2.7.0 56 OF 109**
- **47 OF 12**
To detect Keyboard backlight, do not close I2C_SCL, I2C_SDA.
If LOW, keyboard backlight present.
If HIGH, keyboard backlight not present.
SMC always working. KBDLED only grounded when KB BL flex connected.
If LOW, keyboard backlight present.
If HIGH, keyboard backlight not present.
These parts 1 to 4 are grounded on keyboard backlight fuse.

SYNC_MASTER=K21_MLB
SYNC_DATE=12/13/2010
PAGE BRANCH REVISION DRAWING NUMBER
IPD / KBD Backlight
Apple Inc.

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PAGE 57 OF 109
SIZE D
57 OF 72

PAGE 48 OF 72
SIZE D
2.7.0
If LVDDR3_HM10 is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SSW is turned ON.
CPU=IV Bridge ULV, AXG=GT2

PHASE 1

AXG PHASE
CPU VCCIO (1.05V S0) Regulator

CPU VCCIO (1.05V S0) Power Supply

Apple Inc.

OCP = 25.6A

Vout = 0.5V * (1 + Ra / Rb)

OCP = R7641 x 8.5uA / R7640

Vout = 1.05V

21A Max Output

f = 300 kHz

2.7.0

SYNC_DATE=09/01/2011

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PAGE BRANCH

REV.

DRAWING NUMBER

SHEET

D  A  C  B  D  A  C
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.

1.05V SUS LDO

Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups.  Alternative is strong voltage dividers (200/100) to 3.3V, which burns 100mW in all S-states.

Max Current = 0.020A
Vout = 1.05V
Freq = 1 MHz

1.5V S0 LDO

Max Current = 0.35A
Vout = 1.5V

1.8V S0 Regulator

Vout = 0.8V * (1 + Ra / Rb)
Vout = 1.794V
Max Current = 1.8A

1.05V S0 LDO

Vout = 1.05V
Max Current = 0.02A

Misc Power Supplies

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### CPU Signal Constraints

| Area_Type | Net_Name     | Min_Shift | Max_Shift | Spacing_Mode | Corner_1 | Corner_2 | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE
|------------|--------------|-----------|-----------|---------------|----------|----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| PCIE_CPU_TX | CPU_27P4S    | 8         | 7         | 6            | 5        | 4        | 3                      | 2                      | 1                      | 0                      |                        |                        |                        |                        |                        |                        | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE

### Parity Interface Constraints

| Area_Type | Net_Name     | Min_Shift | Max_Shift | Spacing_Mode | Corner_1 | Corner_2 | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE
|------------|--------------|-----------|-----------|---------------|----------|----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| PCIE_CPU_TX | CPU_27P4S    | 8         | 7         | 6            | 5        | 4        | 3                      | 2                      | 1                      | 0                      |                        |                        |                        |                        |                        |                        | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE

### PCI-Express Interface Constraints

| Area_Type | Net_Name     | Min_Shift | Max_Shift | Spacing_Mode | Corner_1 | Corner_2 | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE
|------------|--------------|-----------|-----------|---------------|----------|----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| PCIE_CPU_TX | CPU_27P4S    | 8         | 7         | 6            | 5        | 4        | 3                      | 2                      | 1                      | 0                      |                        |                        |                        |                        |                        |                        | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE

### CPU Net Properties

| Area_Type | Net_Name     | Min_Shift | Max_Shift | Spacing_Mode | Corner_1 | Corner_2 | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE
|------------|--------------|-----------|-----------|---------------|----------|----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| PCIE_CPU_TX | CPU_27P4S    | 8         | 7         | 6            | 5        | 4        | 3                      | 2                      | 1                      | 0                      |                        |                        |                        |                        |                        |                        | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE

### CPU Constraints

| Area_Type | Net_Name     | Min_Shift | Max_Shift | Spacing_Mode | Corner_1 | Corner_2 | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Referenced_Dielectric | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE
|------------|--------------|-----------|-----------|---------------|----------|----------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|------------------------|
| PCIE_CPU_TX | CPU_27P4S    | 8         | 7         | 6            | 5        | 4        | 3                      | 2                      | 1                      | 0                      |                        |                        |                        |                        |                        |                        | Note: CPU_CLK and CPU_TX can be connected back to TABLE_SPACING_RULE

Note: DisplayPort tables are on Page 103
### SATA Interface Constraints

<table>
<thead>
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<tr>
<td>SATA_MUX_SSD_D2R</td>
<td>Source: <em>Source: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8</em>, NET_SPACING_TYPE1 NET_SPACING_TYPE2 SATA3_PCH_RX SATA3_PCH_TX _RX SATA3_PCH_TX _TX SATA3_PCH_TX</td>
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<tr>
<td></td>
<td>Source: <em>Source: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8</em>, NET_SPACING_TYPE1 NET_SPACING_TYPE2 SATA3_PCH_RX SATA3_PCH_TX _RX SATA3_PCH_TX _TX SATA3_PCH_TX</td>
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### USB 2.0 Interface Constraints

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<td>USB3_PCH_TX</td>
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<tr>
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### USB 3.0 Interface Constraints

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### UART Interface Constraints

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<td>Source: <em>Source: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8</em>, NET_SPACING_TYPE1 NET_SPACING_TYPE2 SATA3_PCH_RX SATA3_PCH_TX _RX SATA3_PCH_TX _TX SATA3_PCH_TX</td>
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### PCH Net Properties

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<tr>
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### PCH Constraints 1

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### System Clock Signal Constraints

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<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Diff Primary Gap</th>
<th>Diff Neck Gap</th>
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<tbody>
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<th>Ymax</th>
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<th>Min Neck Length</th>
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### LPC Bus Constraints

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<th>Ymax</th>
<th>Spacing</th>
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<th>Min Neck Length</th>
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<th>Ymax</th>
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### Chipset Net Properties

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<th>Min Neck Length</th>
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<td>HDA_SYNC_R</td>
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### Clock Net Properties

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<th>Ymin</th>
<th>Ymax</th>
<th>Spacing</th>
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<th>Min Neck Width</th>
<th>Min Neck Length</th>
<th>Diff Primary Gap</th>
<th>Diff Neck Gap</th>
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<tbody>
<tr>
<td>CLK_25M_45S</td>
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<td>80_OHM</td>
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### Thunderbolt/DP Connector Signal Constraints

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<th>NET SPACING TYPE 2</th>
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<td>TBT_DP_TX</td>
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<tr>
<td>TBT_DP_RX</td>
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**TBT_SPI**

<table>
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<th>LAYER</th>
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<tr>
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<td>TBT_DP_TX</td>
<td>TBT_DP_TX</td>
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**LINE-TO-LINE SPACING**

- **ALLOW ROUTE**
- **MAXIMUM NECK LENGTH**
- **MINIMUM NECK WIDTH**
- **DIFFPAIR PRIMARY GAP**
- **DIFFPAIR NECK GAP**

**PHYSICAL RULE SET**

- **=80_OHM_DIFF**
- **=80_OHM_SE**
- **=45_OHM_SE**
- **=4x_DIELECTRIC**
- **=6x_DIELECTRIC**

### Thunderbolt/DP Net Properties

<table>
<thead>
<tr>
<th>Thunderbolt/DP Net Properties</th>
<th>Position</th>
<th>Distance</th>
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### Thunderbolt IC Net Properties

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Only used on dual-port hosts.
### Single-ended Physical Constraints

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<td>ISL3, ISL10</td>
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### Differential Pair Physical Constraints

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### Spacing Constraints

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<td>TOP, ISL2, ISL11</td>
<td>TOP</td>
<td>ISL4, ISL9</td>
<td>TOP, BOTTOM</td>
<td>45_OHM_SE</td>
<td>45_OHM_SE</td>
</tr>
<tr>
<td>TOP, ISL2, ISL11</td>
<td>TOP</td>
<td>ISL4, ISL9</td>
<td>TOP, BOTTOM</td>
<td>45_OHM_SE</td>
<td>45_OHM_SE</td>
</tr>
</tbody>
</table>

### PCB Rule Definitions

Apple Inc. 851-282

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SHEET: 119 OF 119

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