1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

D8 MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0001607307	ENGINEERING RELEASED	2012-08-28

LAST_MODIFIED=Mon Aug 27 13:24:34 2012

DRAWING
TITLE=K22
ABBREV=DRAWING
LAST_MODIFIED=Mon Aug 27 13:24:34 2012

DRAWING TITLE: SCH,D8,MLB

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D
REVISION: 7.0.0
BRANCH: prefsb
PAGE: 1 OF 143
SHEET: 1 OF 117

System Block diagram can be found on Kismet

PATH: Kismet > K70/72 > Block Diagrams > K70 Block Diagram

D8_MLB

01/05/2012

PAGE TITLE
System Block Diagram

Apple Inc.

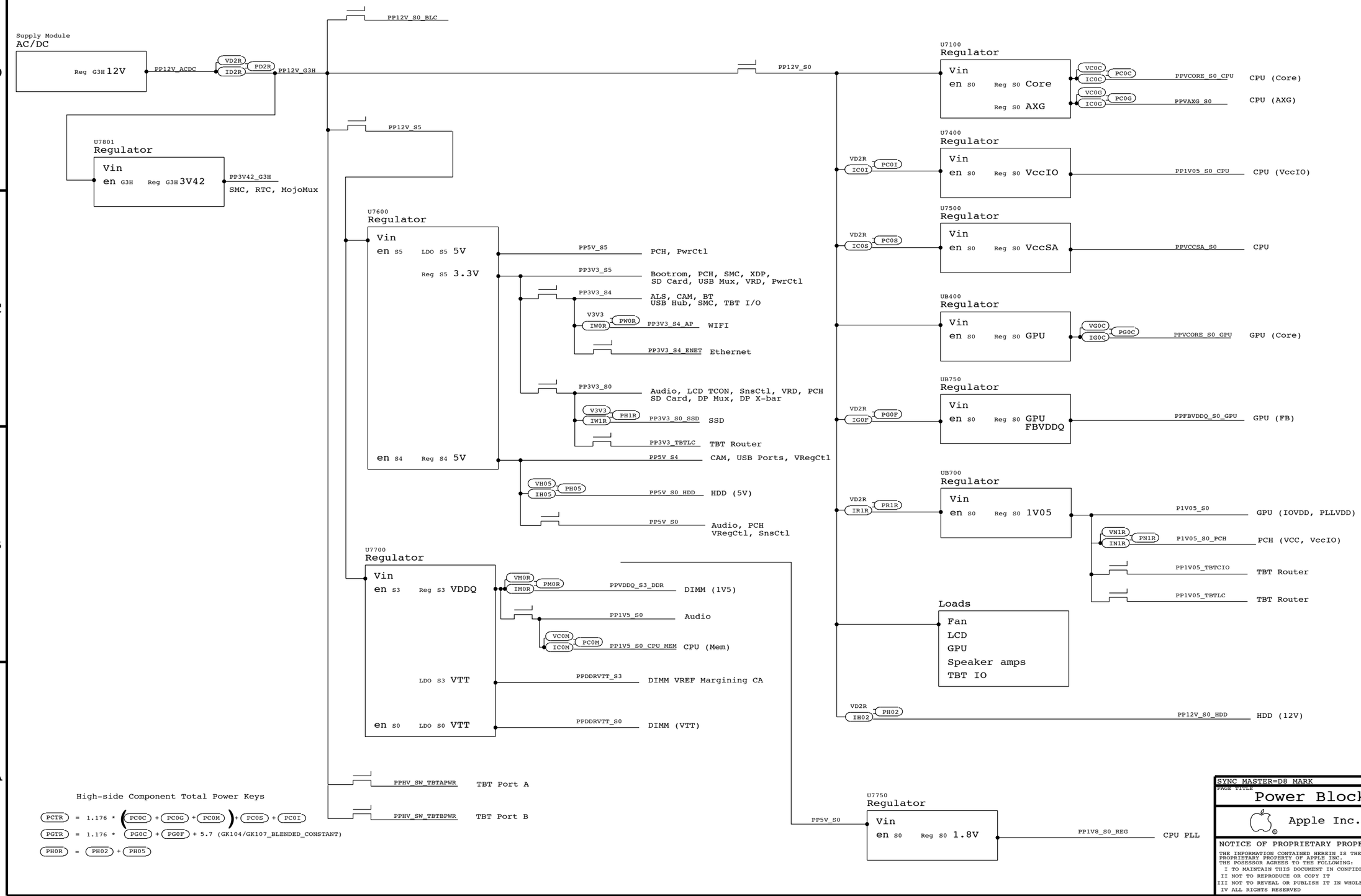
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 2 OF 143

SHEET 2 OF 117



SYNC MASTER=D8 MARK SYNC DATE=04/23/2012

PAGE TITLE
Power Block Diagram

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 3 OF 143
SHEET 3 OF 117

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-3816	PCBA,MLB,2.9G,4C,GK107,SAM,D8	D8_COMMON,D8,CPU:4C_2P9GHZ,GPU:107EGE,FB:BOTH_SAMSUNG,EEEE:F2FR
639-3952	PCBA,MLB,3.1G,4C,GK107,SAM,D8	D8_COMMON,D8,CPU:4C_3P1GHZ,GPU:107EGE,FB:BOTH_SAMSUNG,EEEE:F49T
639-4092	PCBA,MLB,2.9G,4C,GK107,HYN.D8	D8_COMMON,D8,CPU:4C_2P9GHZ,GPU:107EGE,FB:BOTH_HYNIX,EEEE:F653
639-4093	PCBA,MLB,3.1G,4C,GK107,HYN.D8	D8_COMMON,D8,CPU:4C_3P1GHZ,GPU:107EGE,FB:BOTH_HYNIX,EEEE:F654
085-4433	PCBA,MLB,DEV,D8	DEVELOPMENT,D8_DEVEL

Bar Code Labels / EEEE #'s

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7896	1	LABEL,MLB,2D	EEEE_DHNM	CRITICAL	EEEE:DHNM
825-7896	1	LABEL,MLB,2D	EEEE_F2FR	CRITICAL	EEEE:F2FR
825-7896	1	LABEL,MLB,2D	EEEE_F49V	CRITICAL	EEEE:F49V
825-7896	1	LABEL,MLB,2D	EEEE_F49T	CRITICAL	EEEE:F49T
825-7896	1	LABEL,MLB,2D	EEEE_F653	CRITICAL	EEEE:F653
825-7896	1	LABEL,MLB,2D	EEEE_F654	CRITICAL	EEEE:F654

BOM Groups

BOM GROUP	BOM OPTIONS
D8_COMMON	COMMON,ALTERNATE,D8_COMMON1,D8_PROGPARTS,D8_PRODUCTION
D8_COMMON1	XDP,RSMRST:GATE,SPEAKERID,VREF:CPU,TBTHV:P12V,FBA,FBB
D8_PROGPARTS	SMC:PROG,BOOTROM:PROG,TBTROM:PROG,CIVROM:PROG,CAMROM:PROG,BLCMCU:PROG
D8_DEVEL	XDP_CONN,LPCPLUS,VREFMRGN:EXT,DEVEL_AUDIO,TEMPSNSDEV
D8_PRODUCTION	VREFMRGN:N,PRODUCTION

CPUs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4355	1	IVB,SR0TA,PRQ,N1,2.9,65W,4+1,1.1,6M,LGA	CPU	CRITICAL	CPU:4C_2P9GHZ
337S4372	1	IVB,SR0T9,PRQ,N0,3.1,65W,4+1,1.1,6M,LGA	CPU	CRITICAL	CPU:4C_3P1GHZ

ASICs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S4277	1	IC,PANTHER POINT,C1,SLJC7,PRQ,BD82Z77	U1800	CRITICAL	
338S1113	1	IC,TBT,CR-4C,B1,PRQ,288 FCBGA,12X12MM	U3600	CRITICAL	
337S4280	1	IC, GPU, NV GK107-GE-PS-A2	U8000	CRITICAL	GPU:107EGE
343S0616	1	IC,BCM57766A1,ENET&SD,8X8	U3900	CRITICAL	

Programmable Parts

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
341S3672	1	IC,EEPROM,CR,V14.1 (B1),D8	U3690	CRITICAL	TBTROM:PROG	
335S0865	1	IC,EEPROM,SERIAL,8KB,MLP8	U3690	CRITICAL	TBTROM:BLANK	
341S3673	1	IC,PROGRMD,EFI ROM,V00FC,D7/D8	U5110	CRITICAL	BOOTROM:PROG	ALTERNATE:335S0812
335S0807	1	IC,64 MBIT SPI SERIAL FLASH	U5110	CRITICAL	BOOTROM:BLANK	
341S3394	1	IC,PROGRMD,SMC,A3,V2.2A32,D8	U4900	CRITICAL	SMC:PROG	
338S1098	1	IC,SMC,LX4FS1AH5BBCIGA3	U4900	CRITICAL	SMC:BLANK	
341S3675	1	IC,CAMERA FLASH,V7228,D7/D8	U4202	CRITICAL	CAMROM:PROG	
335S0852	1	IC,FLASH,SPI,1MBIT,3V3	U4202	CRITICAL	CAMROM:BLANK	
341S3645	1	IC,ENET 1MBIT, SPI,ROM, V1.13 D8	U3990	CRITICAL	CIVROM:PROG	ALTERNATE:335S0854
335S0862	1	IC,SERIAL FLASH,2MBIT, 2.7V, REF F	U3990	CRITICAL	CIVROM:BLANK	
341S3674	1	IC,BLC,MCU, PRPOGRAMMED, V0204, D8	U9700	CRITICAL	BLCMCU:PROG	
337S3978	1	IC,BLC MCU LPC2132FBD64/01, LQFP64	U9700	CRITICAL	BLCMCU:BLANK	

CPU SOCKET

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0073	1	SOCKET,MOLEX,LGA1155,CPU-LF	U1000	CRITICAL	

CPU SOCKET ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
511S0071	511S0073		ALL	TYCO SOCKET
511S0072	511S0073		ALL	FOXCONN SOCKET

D8 SCHEMATIC / PCB #'S

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9504	1	SCH,MLB,D8	SCH1	CRITICAL	D8
820-3298	1	PCBF,MLB,D8	PCB1	CRITICAL	D8

D8 ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0147	377S0126		ALL	USB diodes
157S0084	157S0058		ALL	Enet Magnetics
341S3644	341S3645		U3990	CIVROM
376S0975	376S1081		ALL	P/NCH DUAL FET
128S0365	128S0368		ALL	150UF CAPS BLK
138S0803	138S0804		ALL	2.2UF CAPS SOFT
102S0880	102S0879		ALL	0.010 OHM,1%,1206

VRAM MODULE PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0619	4	IC,SGRAM,GDDR5,32MX32,1.5GHz,G-DIE,HF	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_SAMSUNG
333S0620	4	IC,GDDR5,32MX32,1.5GHZ,VEGA 44NM,H-DIE	U8400,U8450,U8500,U8550	CRITICAL	FB:BOTH_HYNIX

SYNC MASTER=D8 MLB SYNC DATE=12/19/2011

PAGE TITLE
BOM Configuration

Apple Inc.

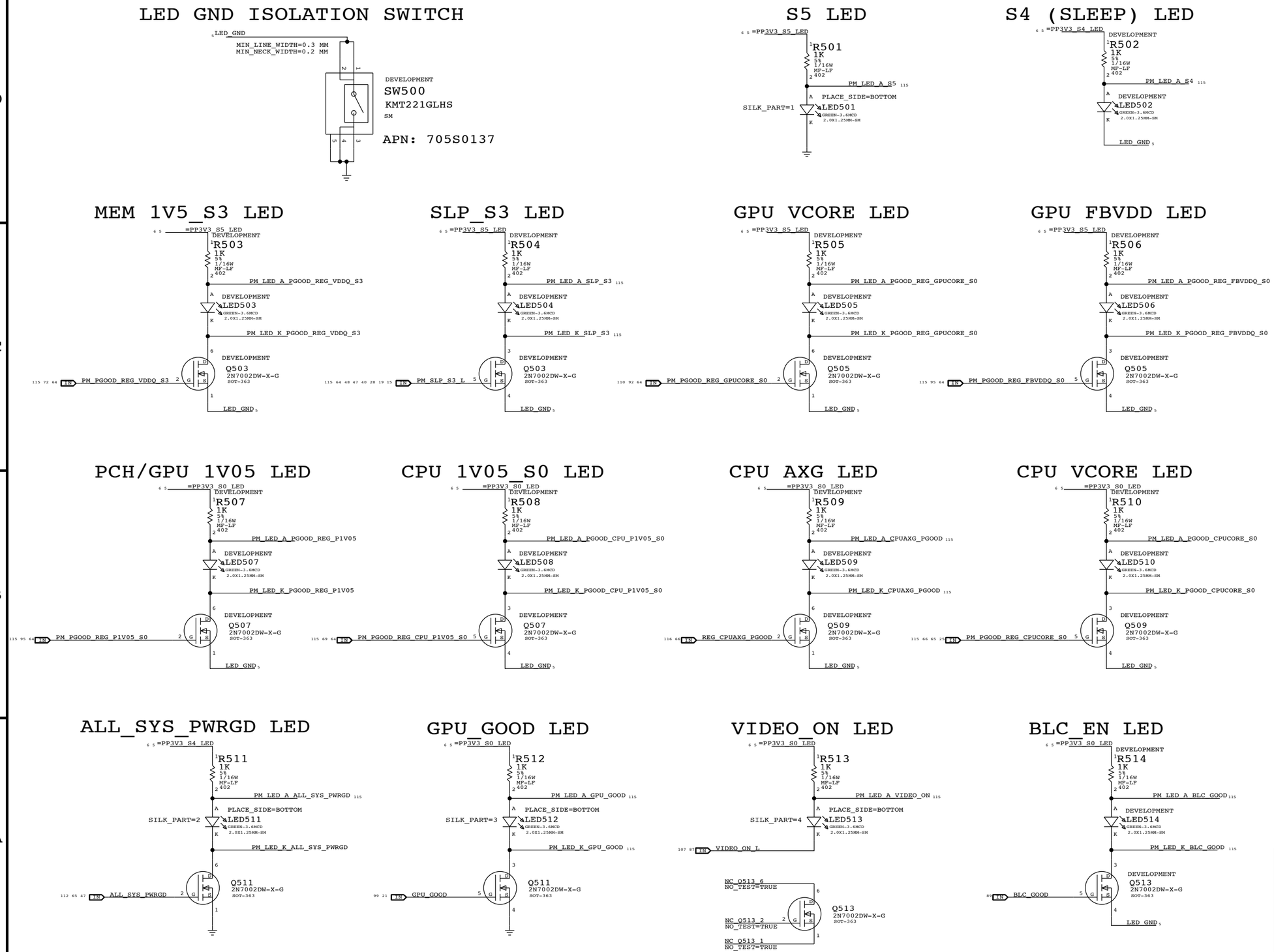
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 4 OF 143

SHEET 4 OF 117



MLB to AC-DC Supplemental Signal Connector

SILK_PART=PWRSIG
J601
504050-0791
M-RT-SM
518S0863

116 48 OUT PWR_BTN — PLACE_NEAR=R606.1:3MM
R606 1K 5% 1/16W MF-LF 402 — PLACE_NEAR=J601.1:3MM
116 PWR_BTN_R — PLACE_NEAR=J601.1:3MM
C600 0.1UF 10% 16V X7R-CERM 0402
D600 6.8V-100PF 402
116 6 SMC_ACDC_ID_R
117 53 OUT TSNS_ACDC_N
117 53 OUT TSNS_ACDC_P
PLACE_NEAR=J601.7:3MM
R600 1K 5% 1/16W MF-LF 402 — BURSTMODE_EN_R_L
C605 0.1UF 10% 16V X7R-CERM 0402 — PLACE_NEAR=R600.1:3MM
D602 6.8V-100PF 402 — PLACE_NEAR=J601.7:3MM
71 48 112 IN BURSTMODE_EN_L

FILTER ADDED TO BURSTMODE_EN_L TO PASS SURGE RDAR://11059712

95 92 72 70 69 66 6 =PP3V3_S0_VRD
R603 10K 5% 1/16W MF-LF 402 — PLACE_NEAR=J601.3:30MM
116 6 SMC_ACDC_ID_R
R604 1K 5% 1/16W MF-LF 402 — PLACE_NEAR=J601.3:3MM
SMC_ACDC_ID 48 116
D601 6.8V-100PF 402 — PLACE_NEAR=J601.1:4MM
C604 0.01UF 20% 16V X7R-CERM 0402 — PLACE_NEAR=R604.2:3MM

CRITICAL
J600
43045-1201
M-RT-TH-1
518-0389

MLB to AC-DC Connector

6 PP12V_G3H_ACDC
J600.4:10MM C601 10UF 10% 25V X5R 805
EMC J600.5:10MM C602 1000PF 5% 25V NP0-C0G 402
EMC J600.5:10MM C603 1000PF 5% 25V NP0-C0G 402
PP12V_G3H_ACDC 6

G3 Rails

Always on: Keeps the PCH RTC alive

106 PP3V3_G3 — MAKE_BASE=TRUE
- PP3V3_G3_RTC 26 115
- =PP3V3_G3_PCH_RTC 22
- =PP3V3_G3_PCH 18 19

G3H Rails

On with AC/DC plugged in

106 PP12V_ACDC — MAKE_BASE=TRUE
- PP12V_G3H_ACDC 6
- =PP12V_G3H_PWR 51

106 PP12V_G3H — MAKE_BASE=TRUE
- PP12V_G3H_SNS 51
- =PP12V_G3H_P3V42 73
- =PP12V_G3H_FET_P12V_S0 74
- =PP12V_G3H_FET_P12V_S5 74

106 PP3V42_G3H — MAKE_BASE=TRUE
- PP3V42_G3H_REG 73
- =PP3V3_G3H_BT 35
- =PP3V3_G3H_RTC_D 26
- =PP3V3_G3H_SMC 47 48 50
- =PP3V3_G3H_SMC_USBMUX 45
- =PPVIN_G3H_SMCVREF 48
- =PP3V3_G3H_LPCPLUS 49

S5 Rails

On when in S5

106 PP12V_S5 — MAKE_BASE=TRUE
- PP12V_S5_FET 74
- =PP12V_S5_REG_P3V3P5V_S5 71
- =PP12V_S5_REG_VDDQ_S3 72
- =PP12V_S5_PWRCTL 64 65 74
- =PPHV_SW_TBTAPWRSW 86
- =PPHV_SW_TBTBPWRSW 88
- =PP12V_S5_SNS 51

106 PP5V_S5 — MAKE_BASE=TRUE
- PP5V_S5_LDO 71
- =PP5V_S5_PWRCTL 71
- =PP5V_S5_PCH 24

106 PP3V3_S5 — MAKE_BASE=TRUE
- PP3V3_S5_REG 71
- =PP3V3_S5_FET_P3V3_S0 74
- =PP3V3_S5_FET_P3V3_S4 74
- =PP3V3_S5_SMC 48
- =PP3V3_S5_LED 5
- =PP3V3_S5_PCH 19 24 26
- =PP3V3_S5_PCH_STRAPS 15
- =PP3V3_S5_PCH_VCCSUS_HDA 22 24
- =PP3V3_S5_PCH_VCCSUS_USB 22 24
- =PP3V3_S5_PCH_VCC_DSW 22 24
- =PP3V3_S5_PCH_VCC_SPI 22 24
- =PP3V3_S5_PWRCTL 64 65
- =PP3V3_S5_ROM 49
- =PP3V3_S5_VRD 71
- =PP3V3_S5_XDP 25
- =PP3V3_S5_SMC_USBMUX 45 46
- =PP3V3_S5_SENSE 51
- =PP3V3_S5_SDCARD 41

S4 Rails

Enabled when system has AC and is in run or sleep

106 PP5V_S4 — MAKE_BASE=TRUE
- PP5V_S4_REG 71
- =PP5V_S4_REG_VDDQ_S3 72
- =PP5V_S4_FET_P5V_S0 74
- =PP5V_S4_MEMRESET 28
- =PP5V_S4_USB 45 46
- =PP5V_S4_CAMERA 42

106 PP3V3_S4 — MAKE_BASE=TRUE
- PP3V3_S4_FET 74
- =PP3V3_S4_ALS 42
- =PP3V3_S4_AP_PWR 55
- =PP3V3_S4_CAMERA 42 43
- =PP3V3_S4_ENET 40
- =PP3V3_S4_LED 5
- =PP3V3_S4_MEMRESET 28
- =PP3V3_S4_PM 28
- =PP3V3_S4_PWRCTL 65 72 74
- =PP3V3_S4_SENSE 51
- =PP3V3_S4_SMBUS 50
- =PP3V3_S4_SMBUS_SMC 50
- =PP3V3_S4_SMC 48
- =PP3V3_S4_TBT 36 37 38 86 88
- =PP3V3_S4_TBTAPWRSW 48 86
- =PP3V3_S4_TBTBPWRSW 48 88
- =PP3V3_S4_USB_HUB 27
- =PP3V3_S4_VREFMRGN 34
- =PP3V3_S4_AUDIO_DIG 60

106 PP3V3_S4_AP — MAKE_BASE=TRUE
- PP3V3_S4_AP_SNS 55
- =PP3V3_S4_AP 15 35

106 PP3V3_S4_ENET — MAKE_BASE=TRUE
- PP3V3_S4_ENET_FET 40
- =PP3V3_S4_ENET_FET 39 40
- =PP3V3_S4_ENET_SYSCLK 26
- =PP3V3_S4_ENET_CLK 26

S3 Rails

Enabled when system is in run or sleep

106 PPVDDQ_S3 — MAKE_BASE=TRUE
- PPVDDQ_S3_REG 72
- =PPVDDQ_S3_DDR_PWR 51
- =PPVDDQ_S3_FET_VDDQ_S0 74
- =PPVDDQ_S3_LDO_DDRVTT 72

THIS IS 1.5V RAIL

106 PPVDDQ_S3_DDR — MAKE_BASE=TRUE
- PPVDDQ_S3_DDR_SNS 51
- =PPVDDQ_S3_DDR_VREF 34
- =PPVDDQ_S3_MEM_A 29 30
- =PPVDDQ_S3_MEM_B 31 32
- =PPVDDQ_S3_MEMRESET 28

THIS IS 1.5V RAIL

106 PPDDRVTT_S3 — MAKE_BASE=TRUE
- PPDDRVTT_S3_LDO 72
- =PPDDRVTT_S3_VREFCA 34

THIS IS 1.5V RAIL

S0 Rails

Enabled when system is in run

106 PP12V_S0 — MAKE_BASE=TRUE
- PP12V_S0_FET 74
- =PP12V_S0_AUDIO_SPKRAMP 58 59
- =PP12V_S0_FAN 54
- =PP12V_S0_FBVDDQ_PWR 51
- =PP12V_S0_REG_GPUCORE 92
- =PP12V_S0_HDD_PWR 51
- =PP12V_S0_LCD 87
- =PP12V_S0_REG_CPUCORE 67
- =PP12V_S0_REG_CPU_P1V05_PWR 55
- =PP12V_S0_REG_CPU_VCCSA_PWR 55
- =PP12V_S0_REG_P1V05_PWR 55
- =PP12V_S0_PWRCTL 65

106 PP12V_S0_HDD — MAKE_BASE=TRUE
- PP12V_S0_HDD_SNS 51
- =PP12V_S0_HDD 52

106 PP12V_S0_BLC — MAKE_BASE=TRUE
- PP12V_S0_BLC_FET 74
- =PP12V_S0_BLC 91

106 PP12V_S0_FBVDDQ — MAKE_BASE=TRUE
- PP12V_S0_FBVDDQ_SNS 51
- =PP12V_S0_REG_FBVDDQ 95

106 PP12V_S0_CPU_P1V05 — MAKE_BASE=TRUE
- PP12V_S0_REG_CPU_P1V05_SNS 55
- =PP12V_S0_REG_CPU_P1V05 69

106 PP12V_S0_VCCSA — MAKE_BASE=TRUE
- PP12V_S0_REG_CPU_VCCSA_SNS 55
- =PP12V_S0_REG_VCCSA 70

106 PP12V_S0_P1V05 — MAKE_BASE=TRUE
- PP12V_S0_REG_P1V05_SNS 55
- =PP12V_S0_REG_P1V05 95

106 PP5V_S0 — MAKE_BASE=TRUE
- PP5V_S0_FET 74
- =PP5V_S0_AUDIO 56 63
- =PP5V_S0_BLC 91
- =PP5V_S0_HDD_PWR 51
- =PP5V_S0_ISENSE 51
- =PP5V_S0_LPCPLUS 49
- =PP5V_S0_PCH 24
- =PP5V_S0_REG_CPUCORE 66
- =PP5V_S0_REG_CPU_P1V05 69
- =PP5V_S0_REG_FBVDDQ 95
- =PP5V_S0_REG_P1V05 95
- =PP5V_S0_REG_P1V8 72
- =PP5V_S0_REG_VCCSA 70
- =PP5V_S0_VRD 72 92

106 PP5V_S0_HDD — MAKE_BASE=TRUE
- PP5V_S0_HDD_SNS 51
- =PP5V_S0_HDD 52

104 PP3V3_S0 — MAKE_BASE=TRUE
- PP3V3_S0_FET 74
- =PP3V3_S0_GPU_IFPX_PLLVDD 78
- =PP3V3_S0_GPU_MISC 78
- =PP3V3_S0_GPU_VDD33 78
- =PP3V3_S0_AUDIO 42 56 58 59 62
- =PP3V3_S0_AUDIO_DIG 60
- =PP3V3_S0_BLC 89
- =PP3V3_S0_DP 85 87
- =PP3V3_S0_ENET 39
- =PP3V3_S0_FAN 54
- =PP3V3_S0_GPU 78 92
- =PP3V3_S0_INTDPMUX 84
- =PP3V3_S0_LED 5
- =PP3V3_S0_LED_SATA 15 44
- =PP3V3_S0_MEM_A_SPD 29 30
- =PP3V3_S0_MEM_B_SPD 31 32
- =PP3V3_S0_P3V3TBTFET 38
- =PP3V3_S0_PCH 18 21 24
- =PP3V3_S0_PCH_GPIO 15 19 20 38
- =PP3V3_S0_PCH_PM 26
- =PP3V3_S0_PCH_STRAPS 15
- =PP3V3_S0_PCH_VCC 22 24
- =PP3V3_S0_PCH_VCC_ADAC 17
- =PP3V3_S0_PCH_VCC_GPIO 22 24
- =PP3V3_S0_PCH_VCC_HVCMOS 22 24
- =PP3V3_S0_PCH_VCC_PCI 22 24
- =PP3V3_S0_PWRCTL 28 74
- =PP3V3_S0_RSTBUF 26
- =PP3V3_S0_SDCARD 41
- =PP3V3_S0_SENSE 51 52 53 55
- =PP3V3_S0_SMBUS 50
- =PP3V3_S0_SMBUS_SMC 50
- =PP3V3_S0_SMBUS_TCON 50
- =PP3V3_S0_SMC 48 51 82
- =PP3V3_S0_TBTPWRCTL 38
- =PP3V3_S0_VRD 6 66 69 70 72 92 95
- =PP3V3_S0_SSD_PWR 51

104 PP3V3_S0_SSD — MAKE_BASE=TRUE
- PP3V3_S0_SSD_SNS 51
- =PP3V3_S0_SSD 44

106 PP1V8_S0 — MAKE_BASE=TRUE
- PP1V8_S0_REG 72
- =PP1V8_S0_CPU_PLL 13 16
- =PP1V8_S0_PCH 19
- =PP1V8_S0_PCH_VCC_DFTERM 22 24
- =PP1V8_S0_PCH_VCC_VRM 24
- =PP1V8_S0_PCH_CLK 26

106 PP1V5_S0 — MAKE_BASE=TRUE
- PP1V5_S0_FET 74
- =PP1V5_S0_AUD_DIG 56
- =PP1V5_S0_CPU_MEM_PWR 51
- =PP1V5_S0_DP 84

106 PP1V5_S0_CPU_MEM — MAKE_BASE=TRUE
- PP1V5_S0_CPU_MEM_SNS 51
- =PP1V5_S0_CPU_MEM 11 13 16

106 PPDDRVTT_S0 — MAKE_BASE=TRUE
- PPDDRVTT_S0_LDO 72
- =PPDDRVTT_S0_CLAMP 28
- =PPDDRVTT_S0_MEM_A 29 30
- =PPDDRVTT_S0_MEM_B 31 32

106 PPDDRVREF_DQ_MEM_A_S3 — MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_A 34
- =PPDDRVREF_DQ_MEM_A 29 30

106 PPDDRVREF_CA_MEM_A_S3 — MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_A 34
- =PPDDRVREF_CA_MEM_A 29 30

106 PPDDRVREF_DQ_MEM_B_S3 — MAKE_BASE=TRUE
- PPDDRVREF_DQ_MEM_B 34
- =PPDDRVREF_DQ_MEM_B 31 32

106 PPDDRVREF_CA_MEM_B_S3 — MAKE_BASE=TRUE
- PPDDRVREF_CA_MEM_B 34
- =PPDDRVREF_CA_MEM_B 31 32

104 PP1V05_S0_CPU — MAKE_BASE=TRUE
- PP1V05_S0_CPU_REG 69
- =PPVCCIO_S0_CPU 10 11 13 16 28 66
- =PPVCCIO_S0_SMC 48
- =PPVCCIO_S0_XDP 25

104 PP1V05_S0 — MAKE_BASE=TRUE
- PP1V05_S0_REG 95
- =PP1V05_S0_PCH_PWR 51
- =PP1V05_S0_P1V05TBTFET 38
- =PP1V05_S0_GPU_IFPCD_IOVDD 78
- =PP1V05_S0_GPU_IFPEF_IOVDD 78
- =PP1V05_S0_GPU_PEX_PLLVDD 78
- =PP1V05_S0_GPU_PEX_IOVDD 78

105 PPVCORE_S0_CPU — MAKE_BASE=TRUE
- PPCPUCORE_S0_REG 67 68
- =PPVCORE_S0_CPU 13 16 51 66

105 PPVAXG_S0 — MAKE_BASE=TRUE
- PPCPUAXG_S0_REG 17 68
- =PPVAXG_S0_CPU 13 17 51 66

104 PPVCCSA_S0 — MAKE_BASE=TRUE
- PPVCCSA_S0_REG 70
- =PPVCCSA_S0_CPU 13 16

Thunderbolt Rails (S0)

Enabled when Thunderbolt cable is plugged in

106 PP3V3_TBTLC — MAKE_BASE=TRUE
- =PP3V3_TBTLC_FET 38
- =PP3V3_TBT_PCH_GPIO 15
- =PP3V3_TBTLC_RTR 15 36 37 38 50
- =PP3V3_TBT_CLK 26

104 38 PP1V05_TBTLC — MAKE_BASE=TRUE
- =PP1V05_TBTLC_FET 38
- =PP1V05_TBTLC_RTR 37

104 PP1V05_TBTCIO — MAKE_BASE=TRUE
- =PP1V05_TBTCIO_FET 38
- =PP1V05_TBTCIO_RTR 37

Ground/Common

GND — MAKE_BASE=TRUE

GPU Rails (S0)

Enabled when system is in run

110 PPVCORE_S0_GPU — MAKE_BASE=TRUE
- PPGPUCORE_S0_REG 93 94
- =PPVCORE_S0_GPU 51 78

106 PPFBVDDQ_S0_GPU — MAKE_BASE=TRUE
- PP1V5R1V35_S0_GPU_REG 95 110
- =PP1V35_S0_GPU_FBVDDQ 78

104 PP1V05_S0_PCH — MAKE_BASE=TRUE
- PP1V05_S0_PCH_SNS 51
- =PP1V05_S0_PCH 18
- =PP1V05_S0_PCH_VCCCLKDMI 22 24
- =PP1V05_S0_PCH_VCCIO_DMI 22 24
- =PP1V05_S0_PCH_VCCIO_PCIE 18 19 22 24
- =PP1V05_S0_PCH_VCCIO_SATA 18 22 24
- =PP1V05_S0_PCH_VCCIO_USB 22 24
- =PP1V05_S0_PCH_VCC_ADPLL 17
- =PP1V05_S0_PCH_VCC_ASW 22 24
- =PP1V05_S0_PCH_VCC_CORE 22 24
- =PP1V05_S0_PCH_VCC_DIFFCLK 22 24
- =PP1V05_S0_PCH_VCC_DMI 22 24
- =PP1V05_S0_PCH_VCC_SSC 22 24
- =PP1V05_S0_PCH_V_PROC_IO 22 24

SYNC MASTER=D8 DOUG SYNC DATE=06/20/2012

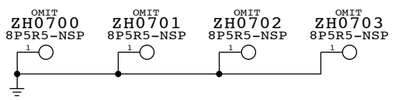
PAGE TITLE
Power Connectors/Aliases

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 6 OF 143
SHEET 6 OF 117

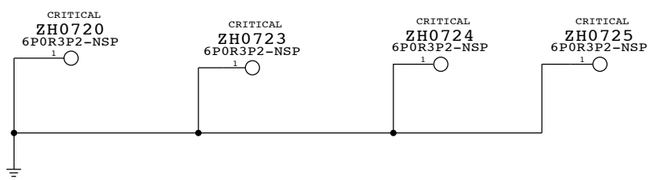
CPU Heatsink

4MM PLATED HOLES (998-4158)



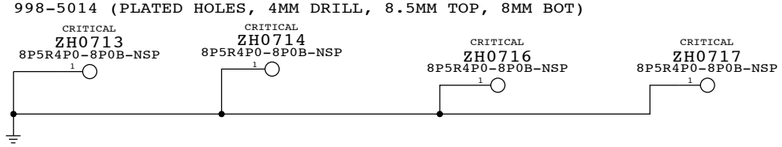
GPU HEATSINK MOUNTING FEATURES

(998-5013. PLATED HOLE, 3.2MM DIA, 6MM PAD TOP/BOT)



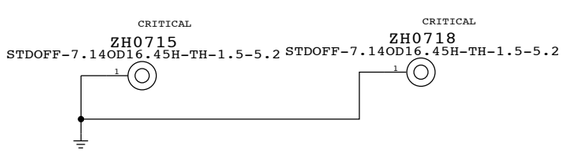
Rear Cover

998-5014 (PLATED HOLES, 4MM DRILL, 8.5MM TOP, 8MM BOT)



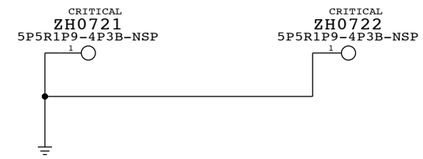
Rear Cover

860-1487 (PCB STANDOFF)



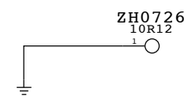
WIRELESS CARD MTG HOLES

998-4938 (PLATED HOLES, 1.9MM INNER DIAMETER, 4.3MM PAD)



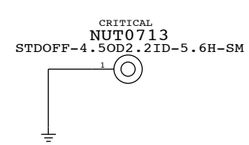
HEATPIPE MTG HOLES

998-4640 (PLATED HOLES, 10MM DIA, 12MM PAD)



SSD STANDOFF

APN: 860-1461



SYNC MASTER=D8 MLB SYNC DATE=03/25/2012

PAGE TITLE: Holes/PD parts

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

PAGE: 7 OF 143

SHEET: 7 OF 117

CPU Reserved

10	TP_CPU_RSVD<16..1>	NC_CPU_RSVD<16..1>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_RSVD<46..19>	NC_CPU_RSVD<46..19>	MAKE_BASE=TRUE NO_TEST=TRUE
10	CPU_CFG<15..12>	TP_CPU_CFG<15..12>	MAKE_BASE=TRUE

CPU Memory

12	TP_MEM_A_DQ_CB<7..0>	NC_MEM_A_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_N<8>	NC_MEM_A_DQSNX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_A_DQS_P<8>	NC_MEM_A_DQSPX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQ_CB<7..0>	NC_MEM_B_DQ_CB<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_N<8>	NC_MEM_B_DQSNX<8>	MAKE_BASE=TRUE NO_TEST=TRUE
12	TP_MEM_B_DQS_P<8>	NC_MEM_B_DQSPX<8>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCIe

18	TP_PCIE1_D2RN	NC_PCIE1_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_D2RP	NC_PCIE1_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_R2D_CN	NC_PCIE1_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE1_R2D_CP	NC_PCIE1_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_D2RN	NC_PCIE2_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_D2RP	NC_PCIE2_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_R2D_CN	NC_PCIE2_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE2_R2D_CP	NC_PCIE2_R2D_PNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_N	NC_DMI_MIDBUS_CLK100NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	DMI_MIDBUS_CLK100M_P	NC_DMI_MIDBUS_CLK100PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE0N	NC_PCIE_CLK100M_PE0NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE0P	NC_PCIE_CLK100M_PE0PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4N	NC_PCIE_CLK100M_PE4NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE4P	NC_PCIE_CLK100M_PE4PX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5N	NC_PCIE_CLK100M_PE5NX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCIE_CLK100M_PE5P	NC_PCIE_CLK100M_PE5PX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6N	NC_PCIE_CLK100M_PE6NX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE6P	NC_PCIE_CLK100M_PE6PX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7N	NC_PCIE_CLK100M_PE7NX	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCIE_CLK100M_PE7P	NC_PCIE_CLK100M_PE7PX	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_N<3..0>	NC_PE_TNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_TX_P<3..0>	NC_PE_TPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_N<3..0>	NC_PE_RNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_PE_RX_P<3..0>	NC_PE_RPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE

PCH USB

20	USB_PCH_4_N	NC_USB_PCH_4NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_4_P	NC_USB_PCH_4PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_N	NC_USB_PCH_5NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_5_P	NC_USB_PCH_5PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_N	NC_USB_PCH_6NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_6_P	NC_USB_PCH_6PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_N	NC_USB_PCH_11NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_11_P	NC_USB_PCH_11PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_N	NC_USB_PCH_12NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_12_P	NC_USB_PCH_12PX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_N	NC_USB_PCH_13NX	MAKE_BASE=TRUE NO_TEST=TRUE
20	USB_PCH_13_P	NC_USB_PCH_13PX	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Clocks

18	TP_PCH_CLKOUT_DPN	NC_PCH_CLKOUT_DPNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CLKOUT_DPP	NC_PCH_CLKOUT_DPPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	PCH_CLK25M_XTALOUT	NC_PCH_CLK25M_XTALOUT	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO64_CLKOUTFLEX0	NC_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO65_CLKOUTFLEX1	NC_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO66_CLKOUTFLEX2	NC_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_GPIO67_CLKOUTFLEX3	NC_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Unused Display

19	TP_CRT_IG_RED	NC_CRT_IG_RED	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_GREEN	NC_CRT_IG_GREEN	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_BLUE	NC_CRT_IG_BLUE	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_HSYNC	NC_CRT_IG_HSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_VSYNC	NC_CRT_IG_VSYNC	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_CLK	NC_CRT_IG_DDC_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_CRT_IG_DDC_DATA	NC_CRT_IG_DDC_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLN<3..0>	NC_DP_IG_B_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_MLP<3..0>	NC_DP_IG_B_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_N	NC_DP_IG_B_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_AUX_P	NC_DP_IG_B_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_HPD	NC_DP_IG_B_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_CLK	NC_DP_IG_B_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_B_DDC_DATA	NC_DP_IG_B_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLN<3..0>	NC_DP_IG_C_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_MLP<3..0>	NC_DP_IG_C_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_N	NC_DP_IG_C_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_AUX_P	NC_DP_IG_C_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_HPD	NC_DP_IG_C_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_CLK	NC_DP_IG_C_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_C_CTRL_DATA	NC_DP_IG_C_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLN<3..0>	NC_DP_IG_D_MLNX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_MLP<3..0>	NC_DP_IG_D_MLPX<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXN	NC_DP_IG_D_AUXNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_AUXP	NC_DP_IG_D_AUXPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_HPD	NC_DP_IG_D_HPD	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_CLK	NC_DP_IG_D_CTRL_CLK	MAKE_BASE=TRUE NO_TEST=TRUE
19	DP_IG_D_CTRL_DATA	NC_DP_IG_D_CTRL_DATA	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINN	NC_SDVO_TVCLKINNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_TVCLKINP	NC_SDVO_TVCLKINPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLN	NC_SDVO_STALLNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_STALLP	NC_SDVO_STALLPX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTN	NC_SDVO_INTNX	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_SDVO_INTP	NC_SDVO_INTPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTCTL	NC_PCH_L_BKLTCTL	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_BKLTEN	NC_PCH_L_BKLTEN	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_L_VDD_EN	NC_PCH_L_VDD_EN	MAKE_BASE=TRUE NO_TEST=TRUE

PCH SATA

18	TP_SATA_C_R2D_CN	NC_SATA_C_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_R2D_CP	NC_SATA_C_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RN	NC_SATA_C_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_C_D2RP	NC_SATA_C_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CN	NC_SATA_D_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_R2D_CP	NC_SATA_D_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RN	NC_SATA_D_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_D_D2RP	NC_SATA_D_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CN	NC_SATA_E_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_R2D_CP	NC_SATA_E_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RN	NC_SATA_E_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_E_D2RP	NC_SATA_E_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CN	NC_SATA_F_R2D_CNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_R2D_CP	NC_SATA_F_R2D_CPX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RN	NC_SATA_F_D2RNX	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_SATA_F_D2RP	NC_SATA_F_D2RPX	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Reserved

19	TP_PCH_RESERVE_0	NC_PCH_RESERVE_0	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_1	NC_PCH_RESERVE_1	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_2	NC_PCH_RESERVE_2	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_3	NC_PCH_RESERVE_3	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_4	NC_PCH_RESERVE_4	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_5	NC_PCH_RESERVE_5	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_6	NC_PCH_RESERVE_6	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_7	NC_PCH_RESERVE_7	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_8	NC_PCH_RESERVE_8	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_9	NC_PCH_RESERVE_9	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_10	NC_PCH_RESERVE_10	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_11	NC_PCH_RESERVE_11	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_12	NC_PCH_RESERVE_12	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_13	NC_PCH_RESERVE_13	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_14	NC_PCH_RESERVE_14	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_15	NC_PCH_RESERVE_15	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_16	NC_PCH_RESERVE_16	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_17	NC_PCH_RESERVE_17	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_18	NC_PCH_RESERVE_18	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_19	NC_PCH_RESERVE_19	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_20	NC_PCH_RESERVE_20	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_21	NC_PCH_RESERVE_21	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_22	NC_PCH_RESERVE_22	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_23	NC_PCH_RESERVE_23	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_24	NC_PCH_RESERVE_24	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_25	NC_PCH_RESERVE_25	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_26	NC_PCH_RESERVE_26	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_27	NC_PCH_RESERVE_27	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_RESERVE_28	NC_PCH_RESERVE_28	MAKE_BASE=TRUE NO_TEST=TRUE

PCH and CPU FDI

10	TP_CPU_FDI_TX_N<7..0>	NC_CPU_FDI_TNX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_TX_P<7..0>	NC_CPU_FDI_TPX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_N<7..0>	NC_PCH_FDI_RNX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_RX_P<7..0>	NC_PCH_FDI_RPX<7..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_FSYNC<1..0>	NC_CPU_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_LSYNC<1..0>	NC_CPU_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
10	TP_CPU_FDI_INT	NC_CPU_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_FSYNC<1..0>	NC_PCH_FDI_FSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_LSYNC<1..0>	NC_PCH_FDI_LSYNC<1..0>	MAKE_BASE=TRUE NO_TEST=TRUE
19	PCH_FDI_INT	NC_PCH_FDI_INT	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Test Points

21	TP_PCH_TP1	NC_PCH_TP1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP2	NC_PCH_TP2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP3	NC_PCH_TP3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP4	NC_PCH_TP4	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP5	NC_PCH_TP5	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP6	NC_PCH_TP6	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP7	NC_PCH_TP7	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP8	NC_PCH_TP8	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP9	NC_PCH_TP9	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP10	NC_PCH_TP10	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP11	NC_PCH_TP11	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP12	NC_PCH_TP12	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP13	NC_PCH_TP13	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP14	NC_PCH_TP14	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP15	NC_PCH_TP15	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP16	NC_PCH_TP16	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP17	NC_PCH_TP17	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP18	NC_PCH_TP18	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP19	NC_PCH_TP19	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_TP20	NC_PCH_TP20	MAKE_BASE=TRUE NO_TEST=TRUE

PCH PCI

20	TP_PCI_AD<31..0>	NC_PCI_AD<31..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_C_BE_L<3..0>	NC_PCI_C_BE_L<3..0>	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_PAR	NC_PCI_PAR	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_RESET_L	NC_PCI_RESET_L	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCH_PCI_GNT0_L	NC_PCI_GNT0_L	MAKE_BASE=TRUE NO_TEST=TRUE
19	TP_PCH_INIT3V3_L	NC_PCH_INIT3V3_L	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_LPC_DREQ0_L	NC_LPC_DREQ0_L	MAKE_BASE=TRUE NO_TEST=TRUE

PCH Miscellaneous

18	TP_HDA_SDIN1	NC_HDA_SDIN1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN2	NC_HDA_SDIN2	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_HDA_SDIN3	NC_HDA_SDIN3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM0	NC_PCH_PWM0	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM1	NC_PCH_PWM1	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM2	NC_PCH_PWM2	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_PWM3	NC_PCH_PWM3	MAKE_BASE=TRUE NO_TEST=TRUE
21	TP_PCH_SST	NC_PCH_SST	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_CLK1	NC_PCH_CL_CLK1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_DATA1	NC_PCH_CL_DATA1	MAKE_BASE=TRUE NO_TEST=TRUE
18	TP_PCH_CL_RST1	NC_PCH_CL_RST1	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT2	NC_PCI_CLK33M_OUT2	MAKE_BASE=TRUE NO_TEST=TRUE
20	TP_PCI_CLK33M_OUT3	NC_PCI_CLK33M_OUT3	MAKE_BASE=TRUE NO_TEST=TRUE

SYNC MASTER=D8 MLB ULTIMATE SYNC DATE=04/02/2012

PAGE TITLE
Unused Signal Aliases

Apple Inc.

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REVISION 7.0.0

BRANCH prefsb

PAGE 8 OF 143

SHEET 8 OF 117

ALIASES (BLANK)

SYNC MASTER=K70 MLB SYNC DATE=08/23/2011

PAGE TITLE
Signal Aliases

Apple Inc.

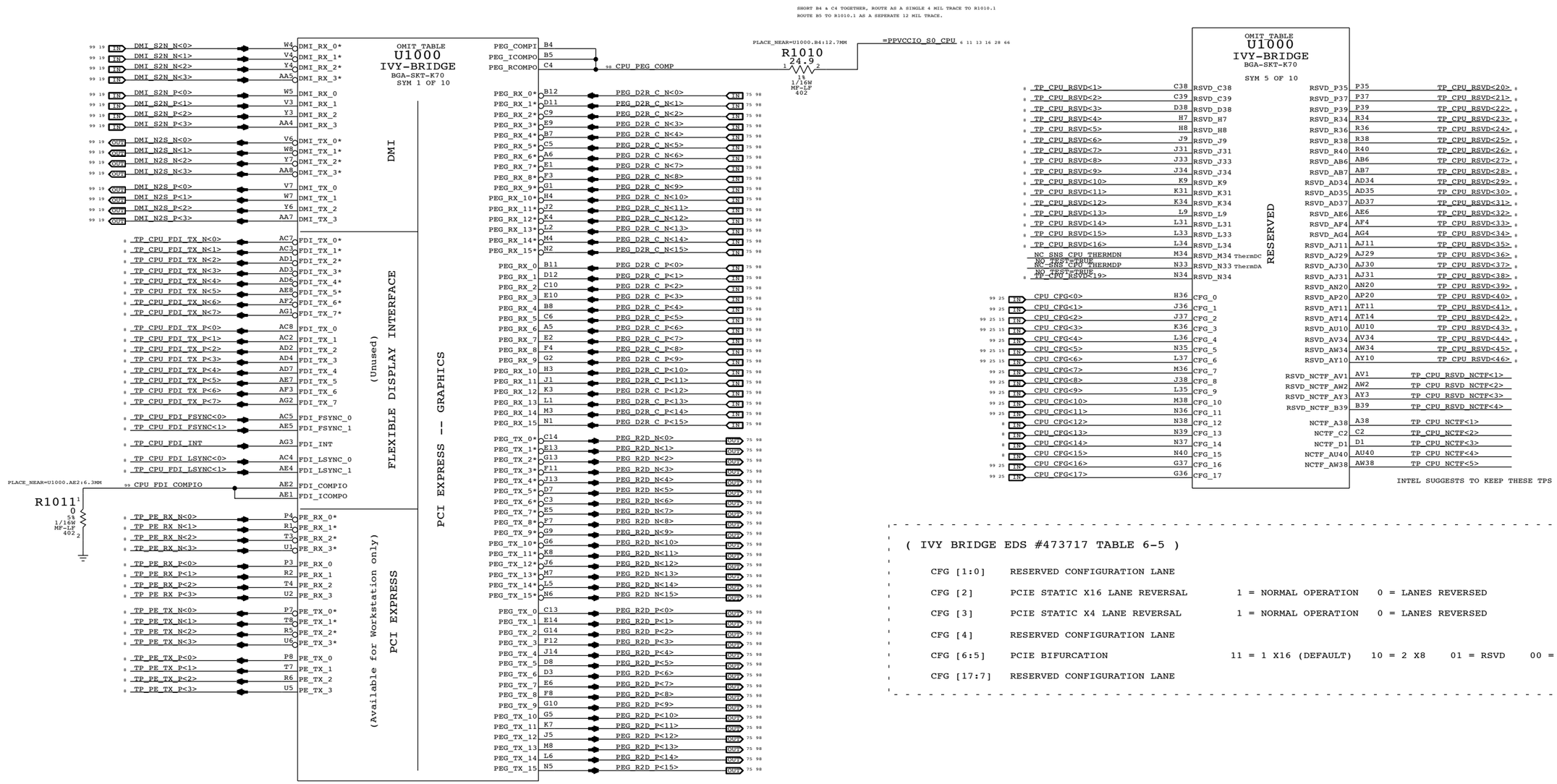
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 9 OF 143

SHEET 9 OF 117



(IVY BRIDGE EDS #473717 TABLE 6-5)

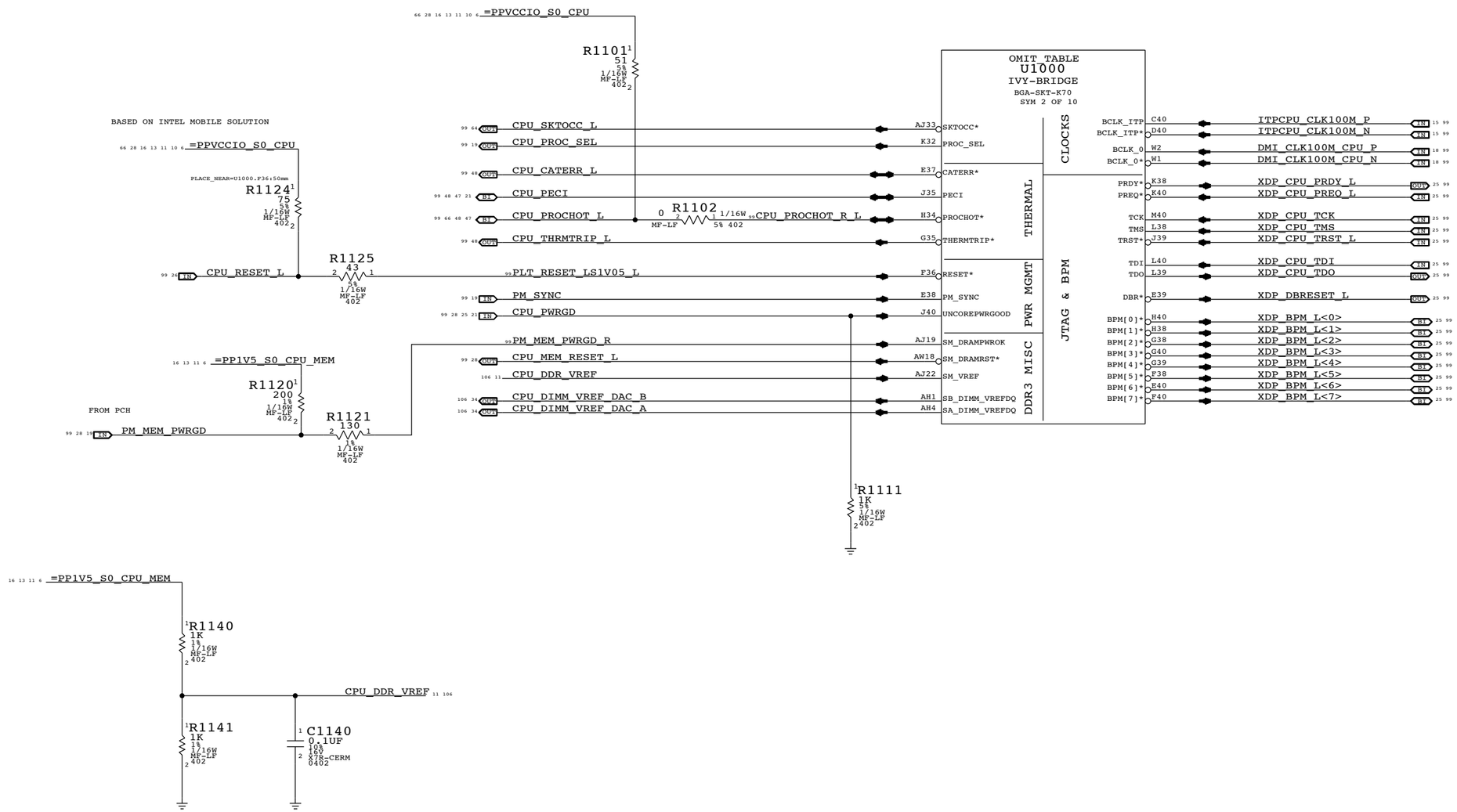
CFG [1:0]	RESERVED CONFIGURATION LANE			
CFG [2]	PCIE STATIC X16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED	
CFG [3]	PCIE STATIC X4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED	
CFG [4]	RESERVED CONFIGURATION LANE			
CFG [6:5]	PCIE BIFURCATION	11 = 1 X16 (DEFAULT)	10 = 2 X8	01 = RSVD 00 = 1 X8, 2 X4
CFG [17:7]	RESERVED CONFIGURATION LANE			

SYNC MASTER=D8 ROSITA SYNC DATE=03/23/2012

PAGE TITLE
CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 10 OF 143
SHEET 10 OF 117



SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE

CPU CLOCK/MISC/JTAG

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

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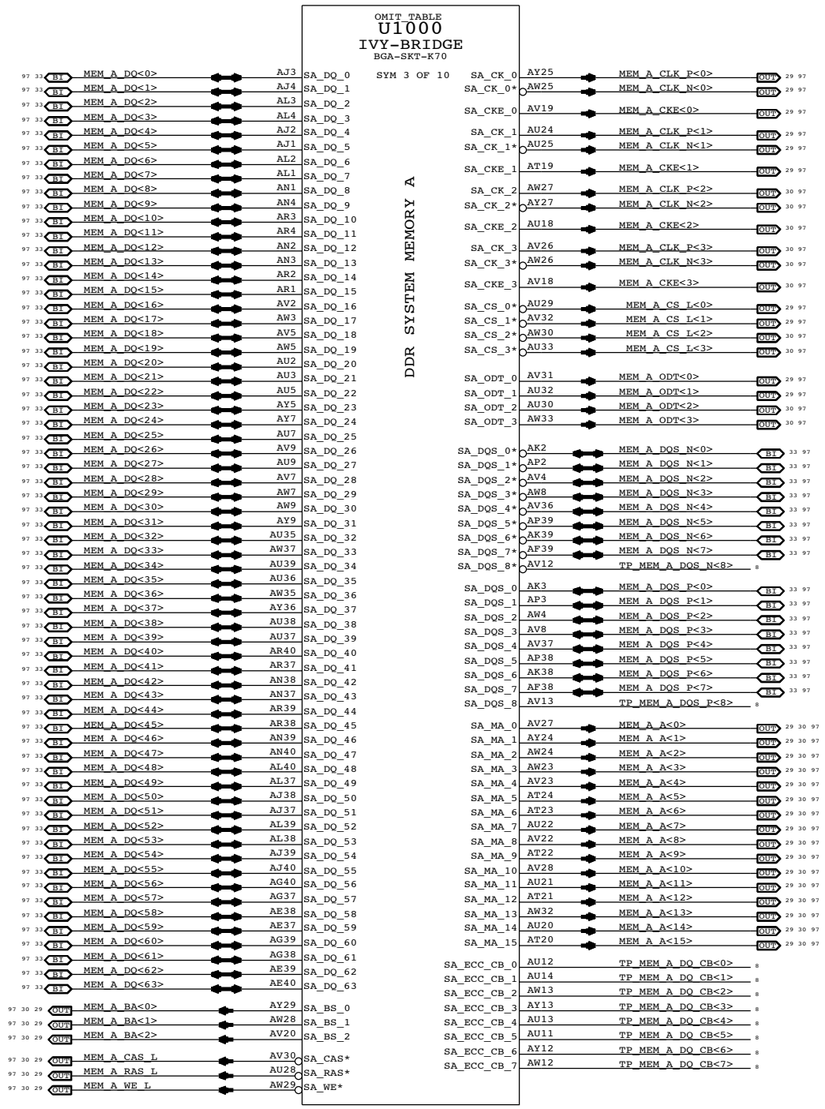
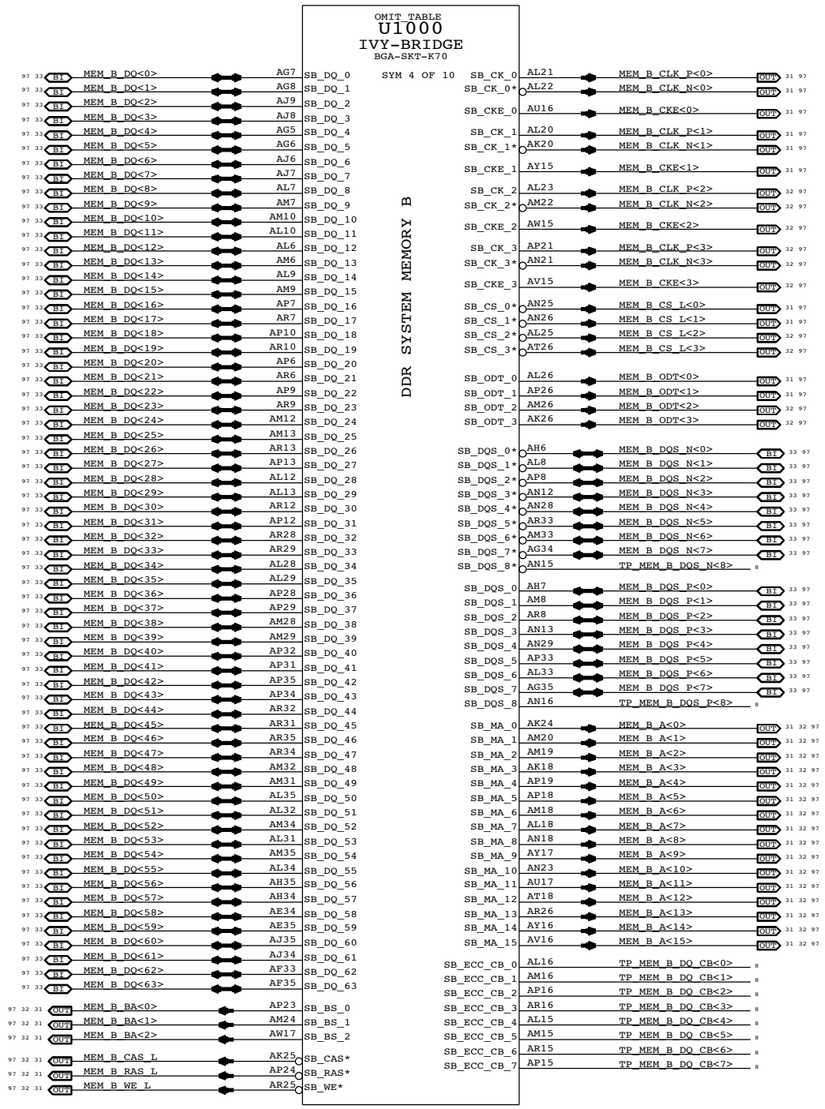
PAGE 11 OF 143

SHEET 11 OF 117





SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

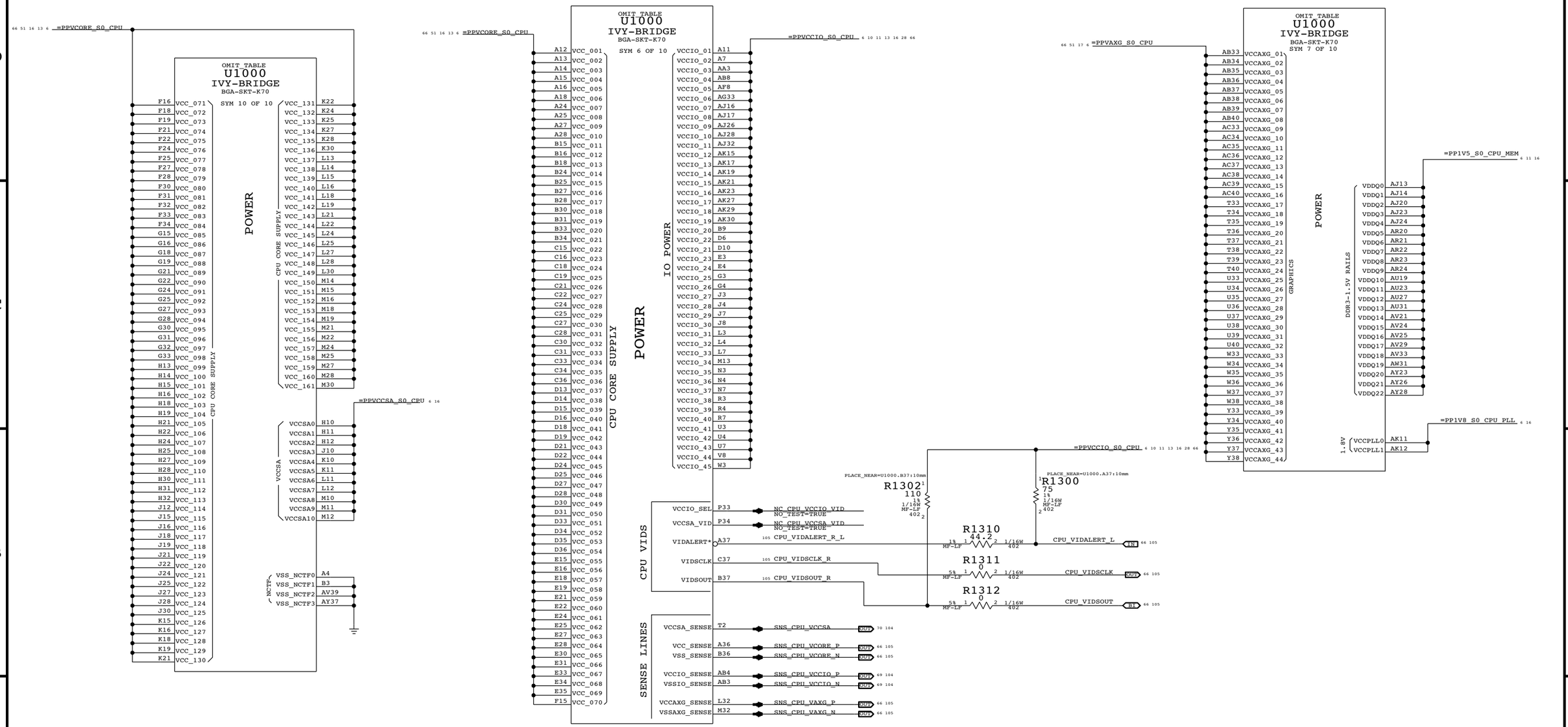
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 12 OF 143

SHEET 12 OF 117



SYNC MASTER=D7_MLB SYNC DATE=03/15/2012

PAGE TITLE

CPU POWER

Apple Inc.

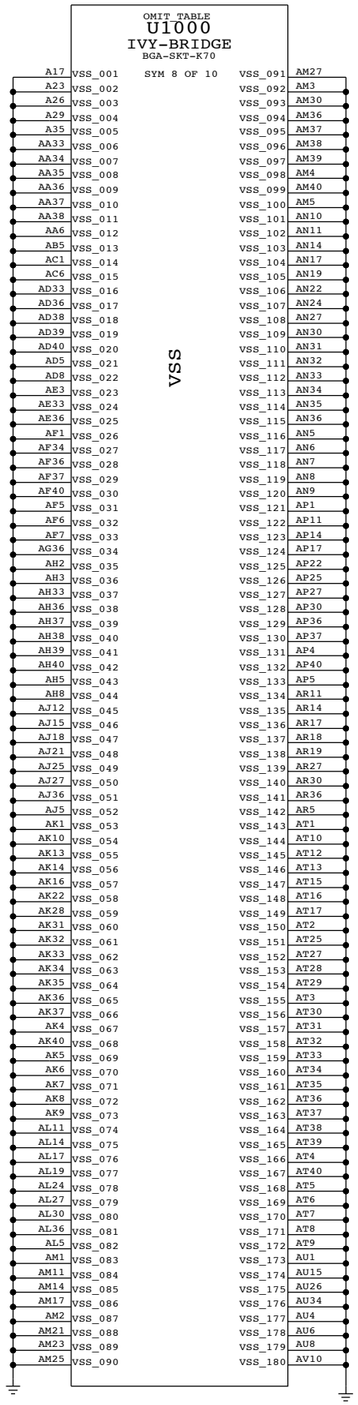
DRAWING NUMBER 051-9504 SIZE D

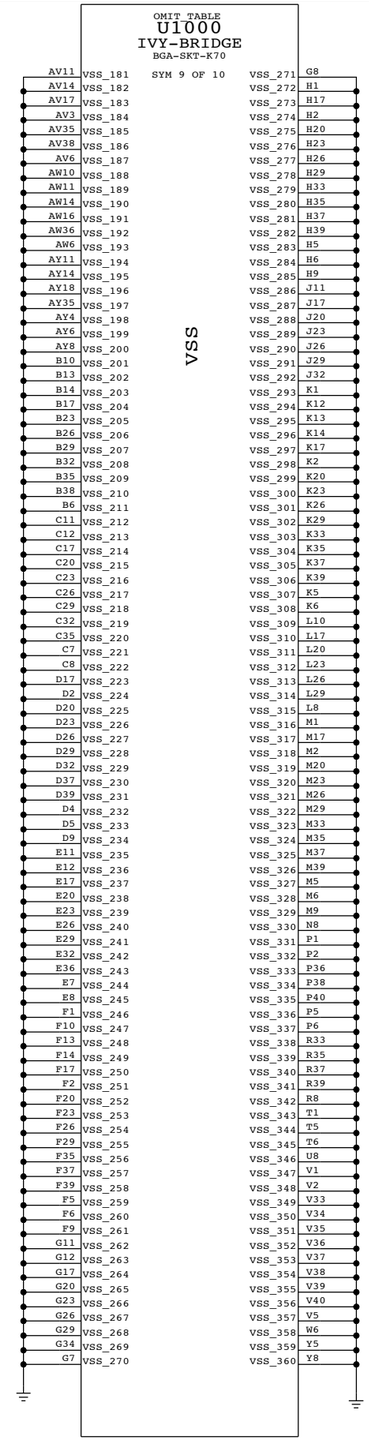
REVISION 7.0.0

BRANCH prefsb

PAGE 13 OF 143

SHEET 13 OF 117





SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE

CPU GROUNDS

Apple Inc.

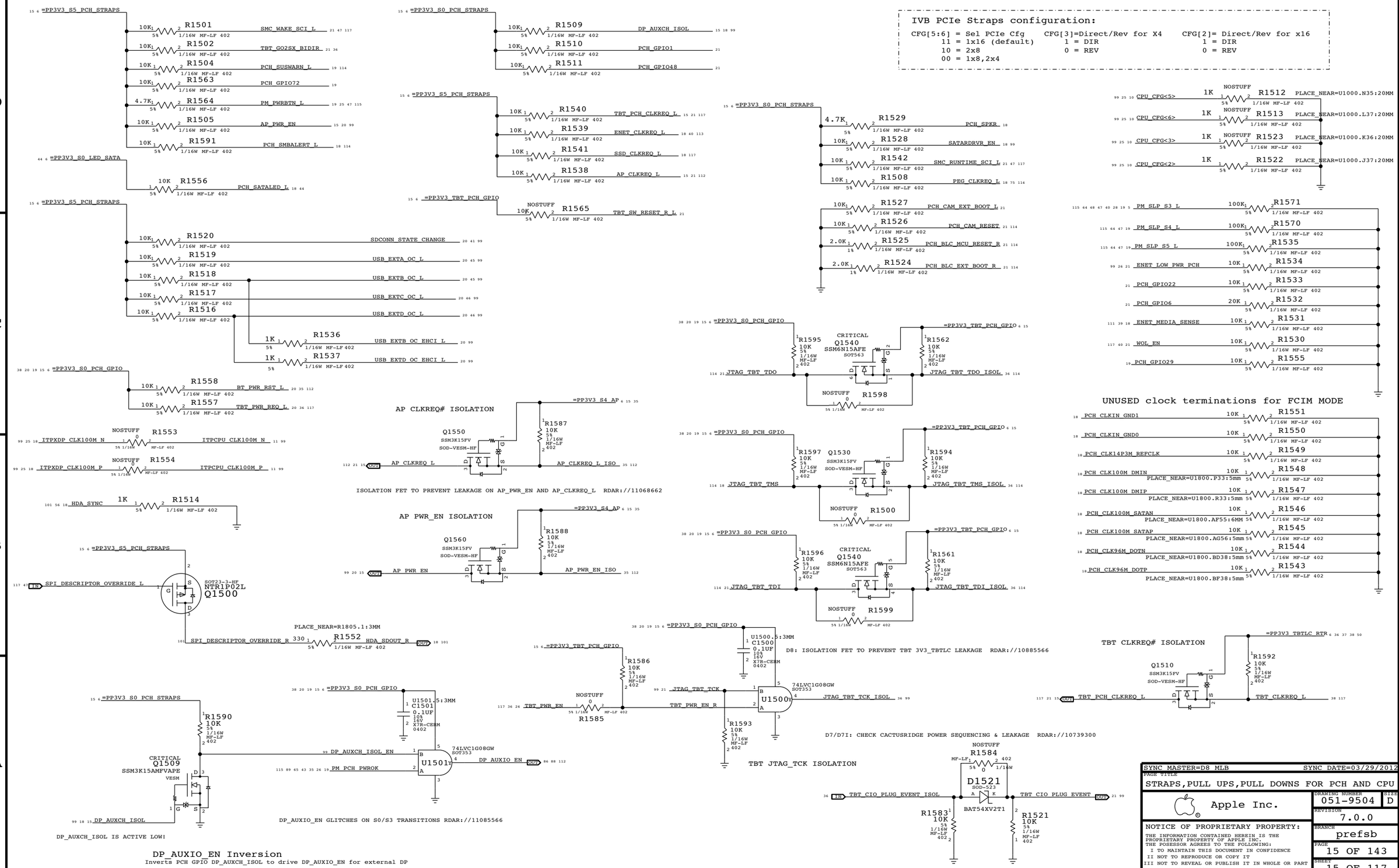
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 14 OF 143

SHEET 14 OF 117



CPU VCORE DECOUPLING

14x 22UF,0805 INTEL RECOMMENDATION 18X 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT_NOTE (C1600-C1613):

REPLACED WITH 603 PER RDAR://10700439

16 13 6 66 51 =PPVCORE_S0_CPU

C1600 22UF 20% 6.3V X5R-CERM2 0603
C1601 22UF 20% 6.3V X5R-CERM2 0603
C1602 22UF 20% 6.3V X5R-CERM2 0603
C1603 22UF 20% 6.3V X5R-CERM2 0603
C1604 22UF 20% 6.3V X5R-CERM2 0603
C1605 22UF 20% 6.3V X5R-CERM2 0603
C1606 22UF 20% 6.3V X5R-CERM2 0603
C1607 22UF 20% 6.3V X5R-CERM2 0603
C1608 22UF 20% 6.3V X5R-CERM2 0603
C1609 22UF 20% 6.3V X5R-CERM2 0603

C1610 22UF 20% 6.3V X5R-CERM2 0603
C1611 22UF 20% 6.3V X5R-CERM2 0603
C1612 22UF 20% 6.3V X5R-CERM2 0603
C1613 22UF 20% 6.3V X5R-CERM2 0603

BULK CAPS ON CPU VREG PAGE 72

10x 10UF and 10x 1UF CAPACITORS

66 51 16 13 6 =PPVCORE_S0_CPU

Place inside socket cavity

C1620 10UF 20% 6.3V X5R 603
C1621 10UF 20% 6.3V X5R 603
C1622 10UF 20% 6.3V X5R 603
C1623 10UF 20% 6.3V X5R 603
C1624 10UF 20% 6.3V X5R 603
C1625 10UF 20% 6.3V X5R 603
C1626 10UF 20% 6.3V X5R 603
C1627 10UF 20% 6.3V X5R 603
C1628 10UF 20% 6.3V X5R 603
C1629 10UF 20% 6.3V X5R 603

C1630 1UF 10% 16V X5R 402
C1631 1UF 10% 16V X5R 402
C1632 1UF 10% 16V X5R 402
C1633 1UF 10% 16V X5R 402
C1634 1UF 10% 16V X5R 402
C1635 1UF 10% 16V X5R 402
C1636 1UF 10% 16V X5R 402
C1637 1UF 10% 16V X5R 402
C1638 1UF 10% 16V X5R 402
C1639 1UF 10% 16V X5R 402

CPU VCCIO DECOUPLING

8X 22UF 0805, 6X 10UF 0805 INTEL RECOMMENDATION 9X22UF 0805,16X 0805 placeholders

PLACEMENT_NOTE (C1650-C1657):

13 11 10 6 66 28 =PPVCCIO_S0_CPU

C1650 22UF 20% 6.3V X5R-CERM2 0603
C1651 22UF 20% 6.3V X5R-CERM2 0603
C1652 22UF 20% 6.3V X5R-CERM2 0603
C1653 22UF 20% 6.3V X5R-CERM2 0603
C1654 22UF 20% 6.3V X5R-CERM2 0603
C1655 22UF 20% 6.3V X5R-CERM2 0603
C1656 22UF 20% 6.3V X5R-CERM2 0603
C1657 22UF 20% 6.3V X5R-CERM2 0603

PLACEMENT_NOTE (C1660-C1665):

Place at edge of socket.

C1660 10uF 20% 6.3V X5R 603
C1661 10uF 20% 6.3V X5R 603
C1662 10uF 20% 6.3V X5R 603
C1663 10uF 20% 6.3V X5R 603
C1664 10uF 20% 6.3V X5R 603
C1665 10uF 20% 6.3V X5R 603

BULK CAPS ON CPU VREG PAGE 74

CRITICAL
C1670 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

CPU VCCSA DECOUPLING

2x 10uF 0603. INTEL RECOMMENDATION 2X 10uF 0805

13 6 =PPVCCSA_S0_CPU

C1666 10uF 20% 6.3V X5R 603
C1667 10uF 20% 6.3V X5R 603

Bulk decoupling is on VCCSA reg page 75

Memory (CPU VCCDDR) DECOUPLING

13 11 6 =PP1V5_S0_CPU_MEM

C1676 22UF 20% 6.3V X5R-CERM2 0603
C1677 22UF 20% 6.3V X5R-CERM2 0603
C1678 22UF 20% 6.3V X5R-CERM2 0603
C1679 22UF 20% 6.3V X5R-CERM2 0603
C1680 22UF 20% 6.3V X5R-CERM2 0603
C1681 22UF 20% 6.3V X5R-CERM2 0603
C1682 1UF 20% 6.3V X5R 0201
C1683 1UF 20% 6.3V X5R 0201
C1684 1UF 20% 6.3V X5R 0201
C1685 1UF 20% 6.3V X5R 0201
C1686 1UF 20% 6.3V X5R 0201

CRITICAL
NOSTUFF
C1687 330UF-0.0045OHM 20% 2V POLY CASE-D2-SM

PLL (CPU VCCSFR) DECOUPLING

2x 47uF, 1x 22uF 0805, 1x 10uF 0603, 1x 4.7uF 0603, 1x 2.2uF 0402, 2x 1uF 0402. INTEL RECOMMENDATION 1x 10uF 0805

13 6 =PP1V8_S0_CPU_PLL

C1693 1UF 10% 16V X5R 402
C1694 1UF 10% 16V X5R 402
C1692 2.2UF 10% 6.3V X5R 402
C1691 4.7UF 10% 6.3V X5R-CERM 603
C1695 10UF 20% 6.3V X5R 603
C1690 22UF 20% 6.3V X5R-CERM2 0603
C1696 47UF 20% 6.3V X5R 0805
C1697 47UF 20% 6.3V X5R 0805

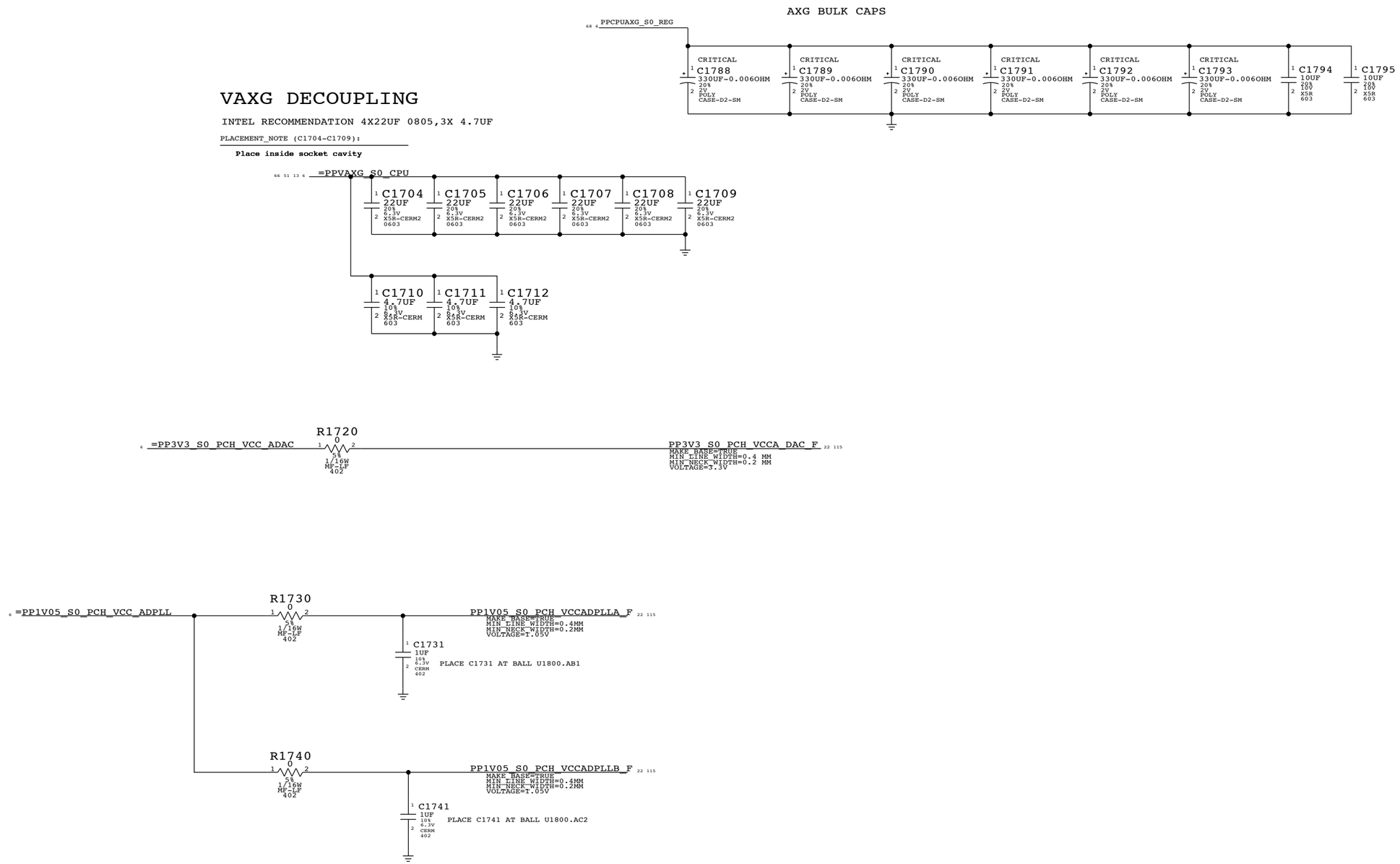
BULK CAPS ON VTT REG PAGE 77

SYNC MASTER=D7 MLB SYNC DATE=12/20/2011

PAGE TITLE
CPU NON-GFX DECOUPLING

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 16 OF 143
SHEET 16 OF 117



SYNC MASTER=D8 KOSECOFF SYNC DATE=01/26/2012

PAGE TITLE
GFX DECOUPLING & PCH PWR ALIAS

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

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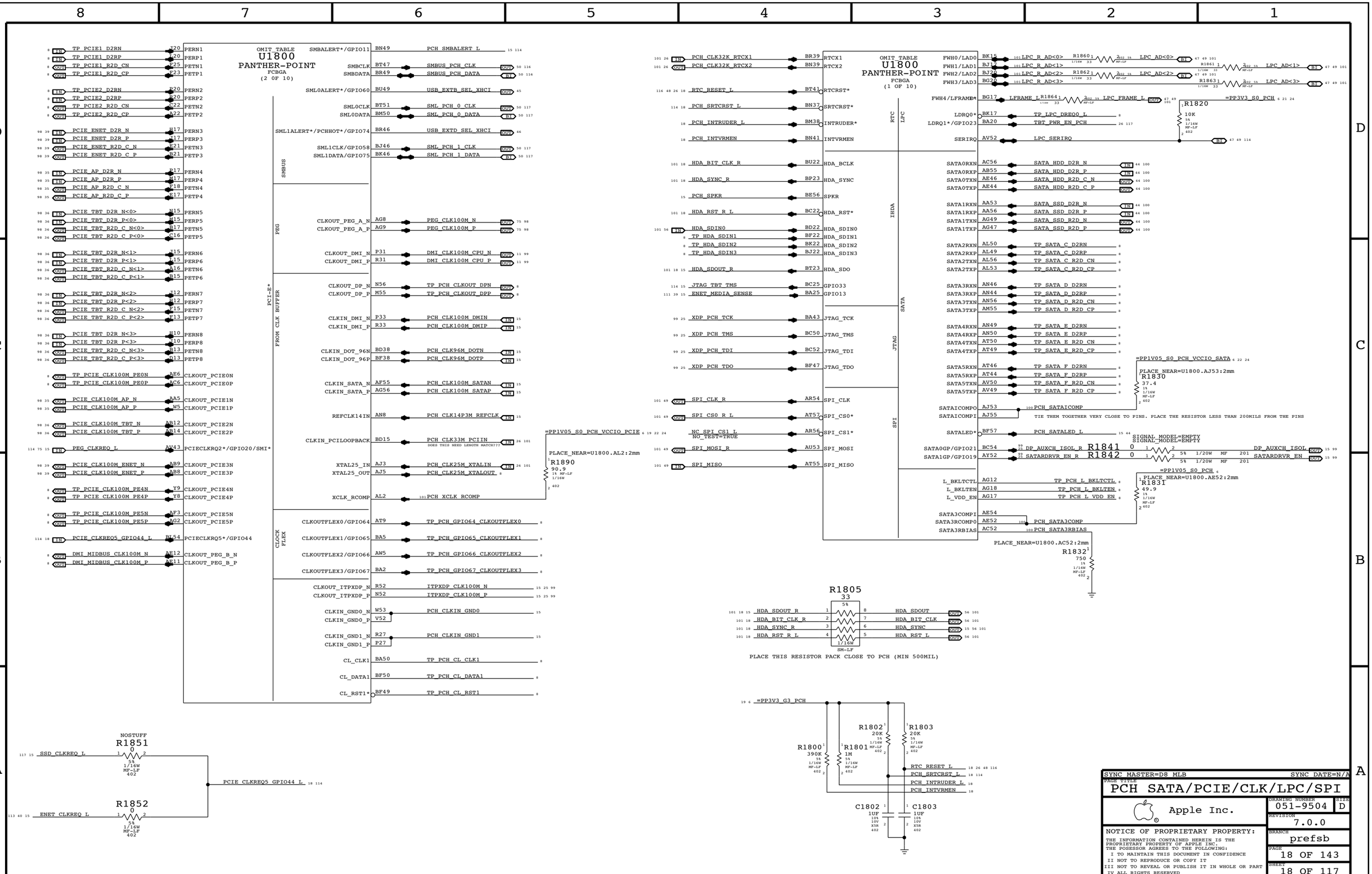
PAGE 17 OF 143

SHEET 17 OF 117

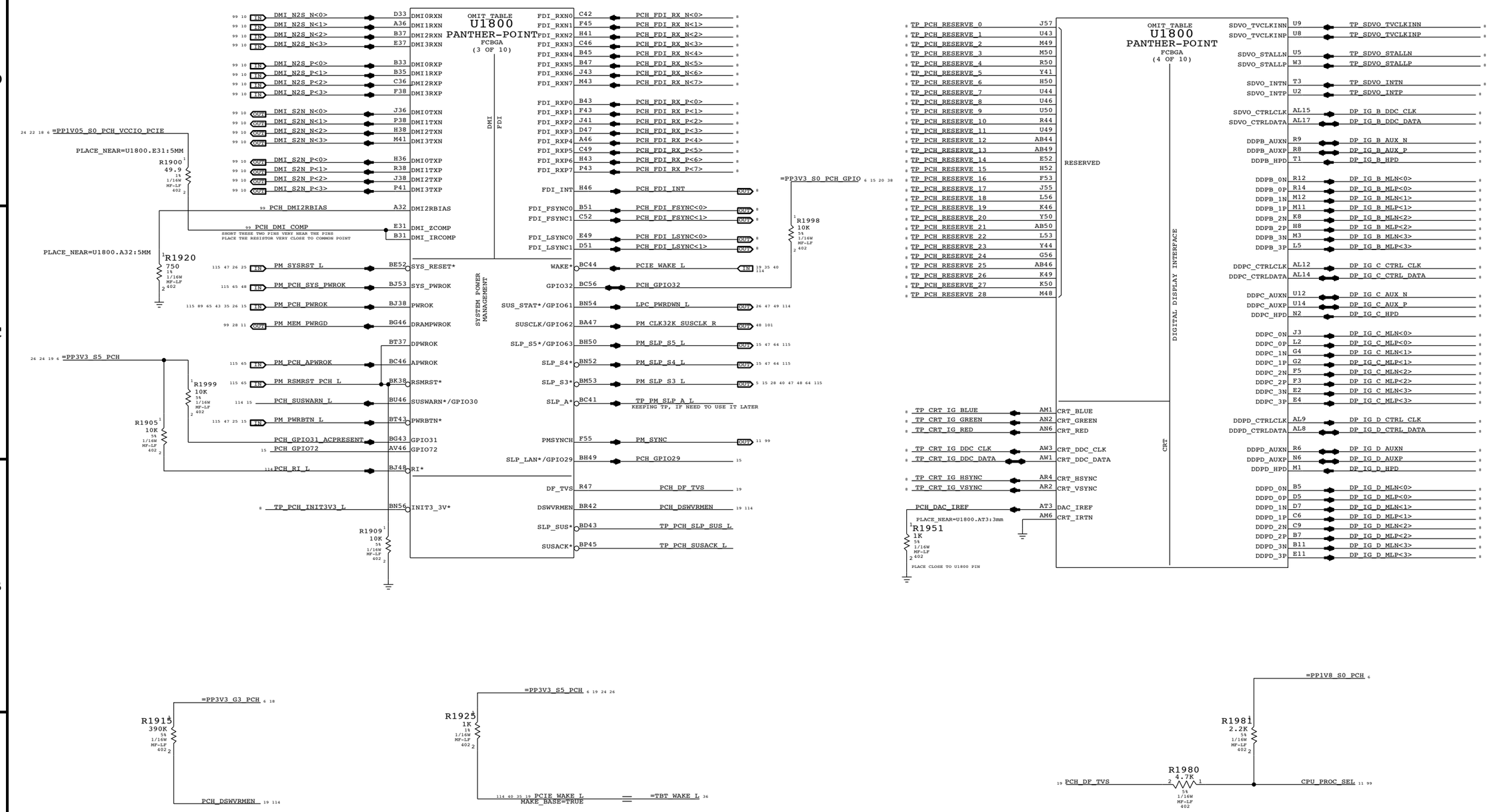


SYNC MASTER=D8 MLB SYNC DATE=N/A

PAGE TITLE
PCH SATA/PCIE/CLK/LPC/SPI

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 18 OF 143
SHEET 18 OF 117



SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE

PCH DMI/FDI/GRAPHICS

Apple Inc.

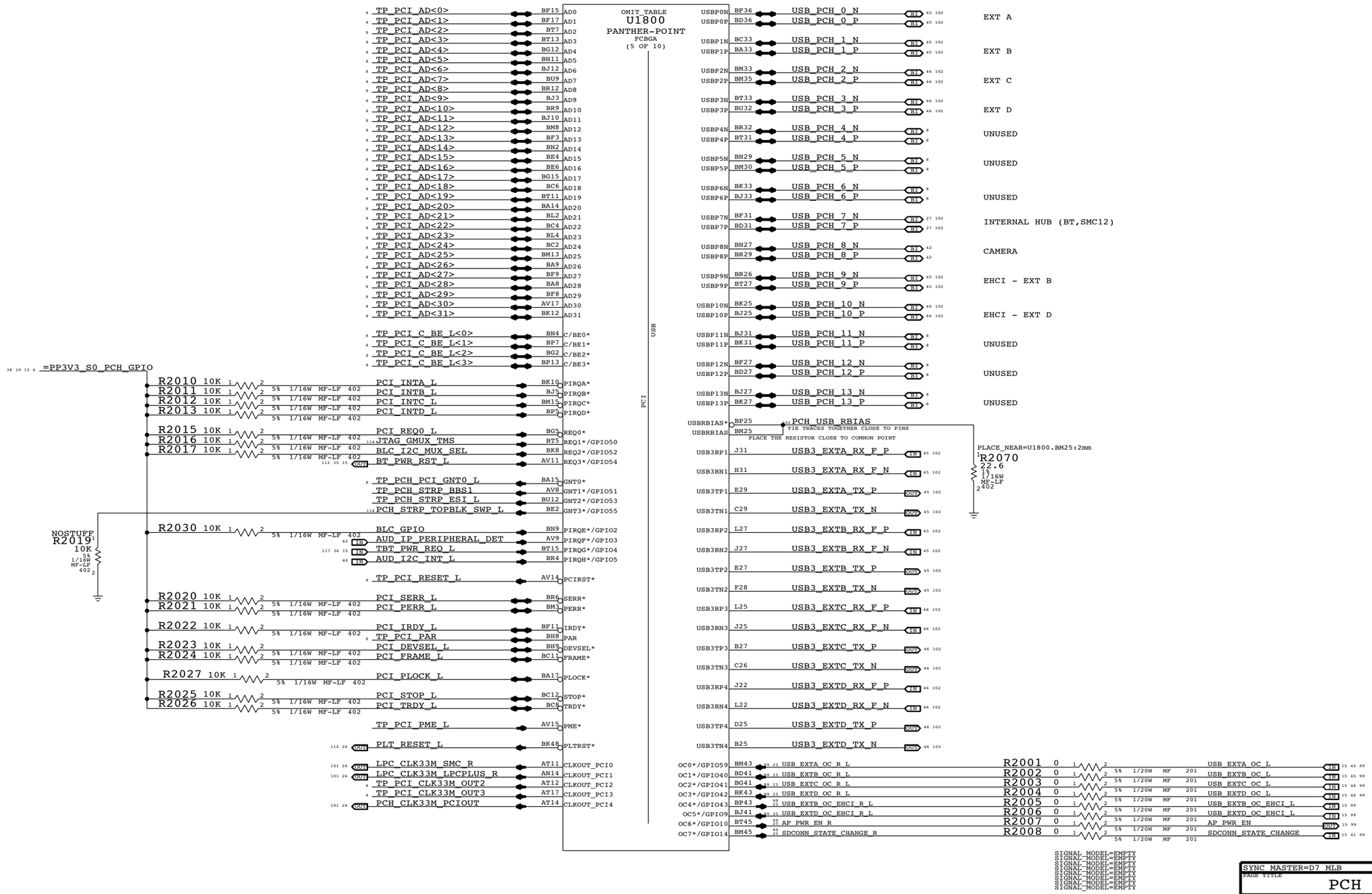
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 19 OF 143

SHEET 19 OF 117



SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE
PCH PCI/USB

Apple Inc.

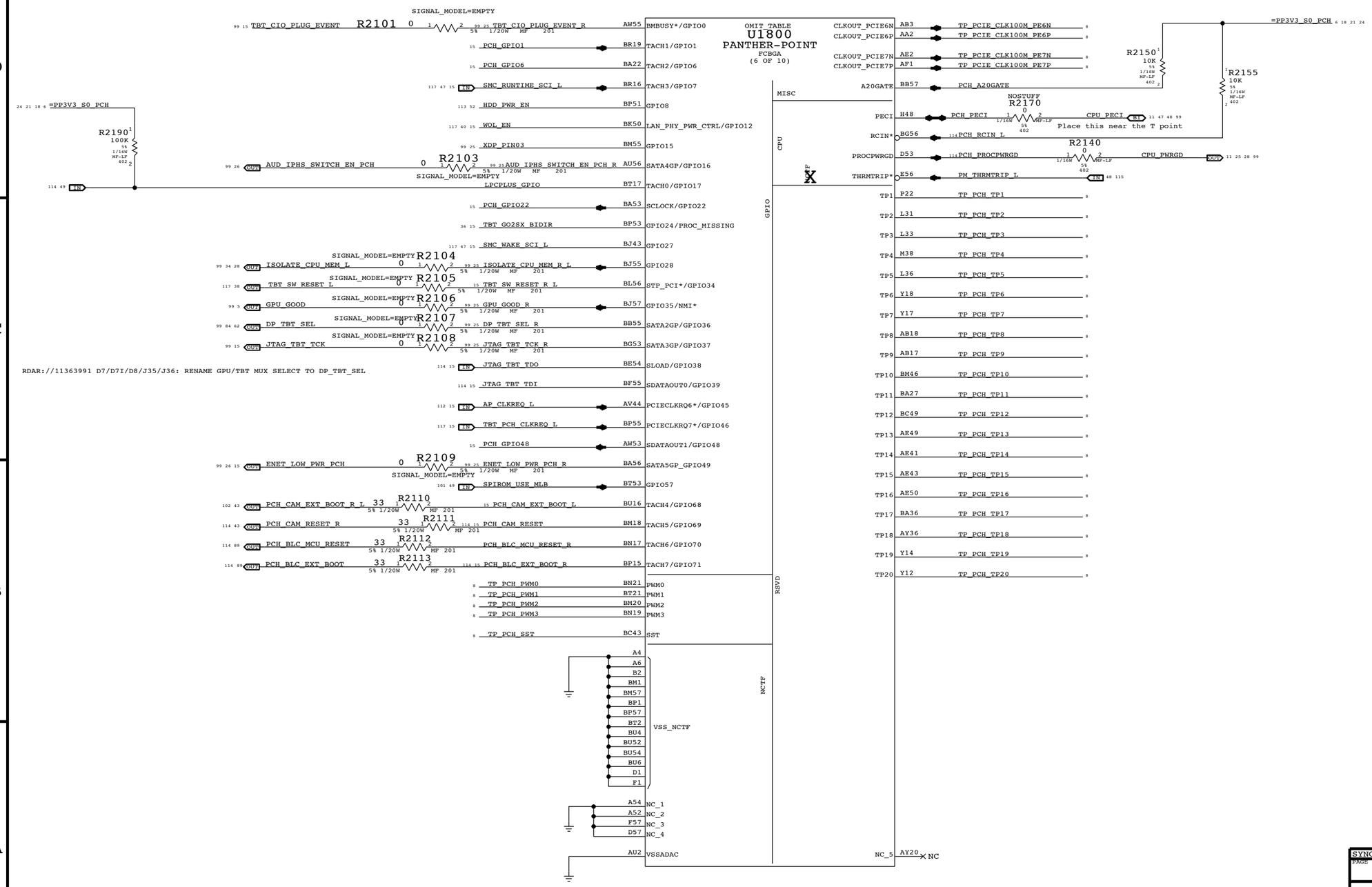
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 20 OF 143

SHEET 20 OF 117



RDAR://11363991 D7/D7I/D8/J35/J36: RENAME GPU/TBT MUX SELECT TO DP_TBT_SEL

SYNC MASTER=D8 MLB SYNC DATE=N/A

PAGE TITLE

PCH MISC

Apple Inc.

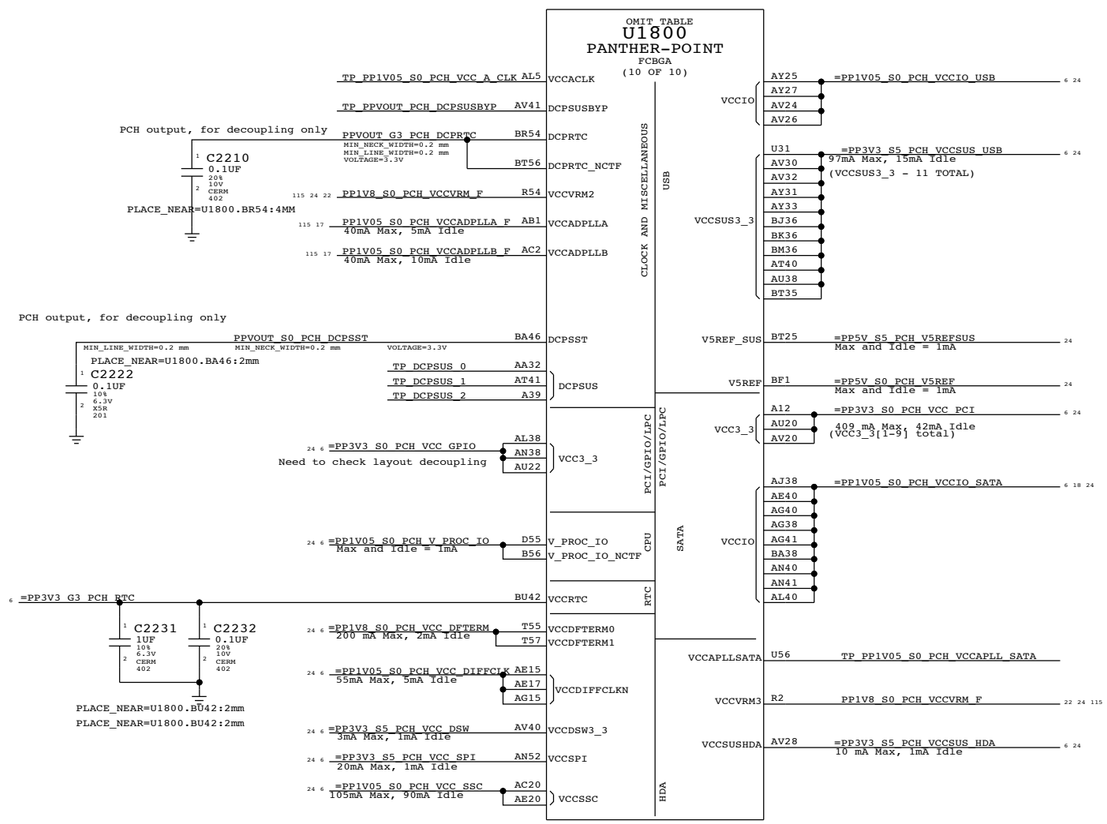
DRAWING NUMBER 051-9504 SIZE D

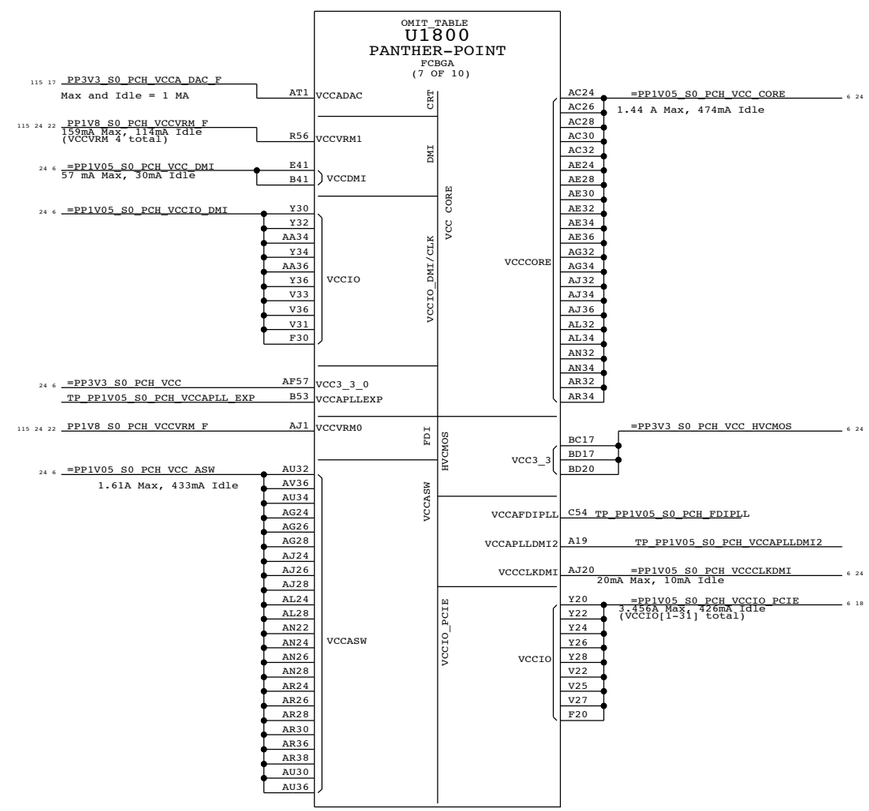
REVISION 7.0.0

BRANCH prefsb

PAGE 21 OF 143

SHEET 21 OF 117





SYNC MASTER=D8_MLB SYNC DATE=N/A

PAGE TITLE
PCH POWER

Apple Inc.

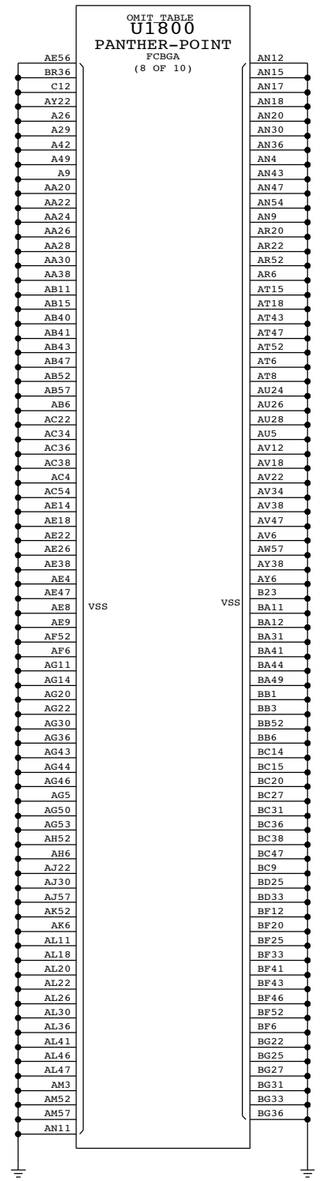
DRAWING NUMBER 051-9504 SIZE D

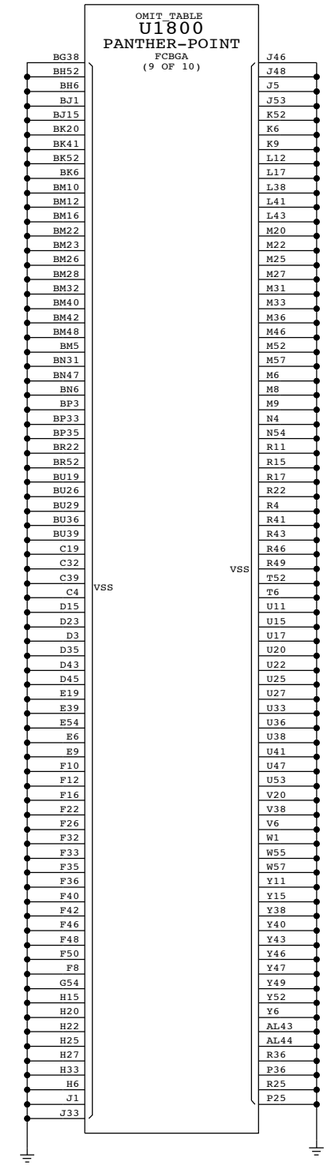
REVISION 7.0.0

BRANCH prefsb

PAGE 22 OF 143

SHEET 22 OF 117





SYNC MASTER=D7 MLB SYNC DATE=03/15/2012

PAGE TITLE
PCH GROUNDS

Apple Inc.

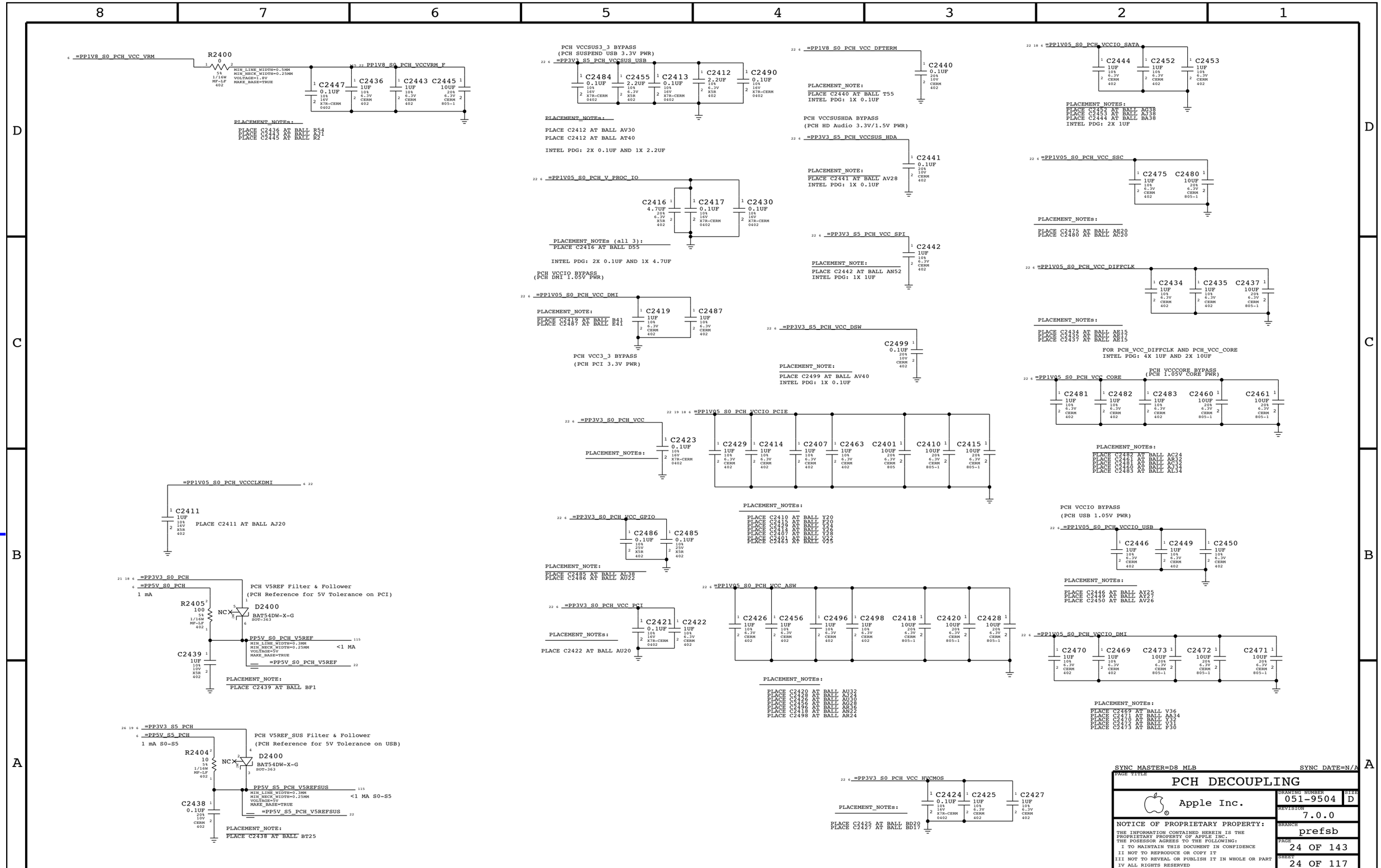
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

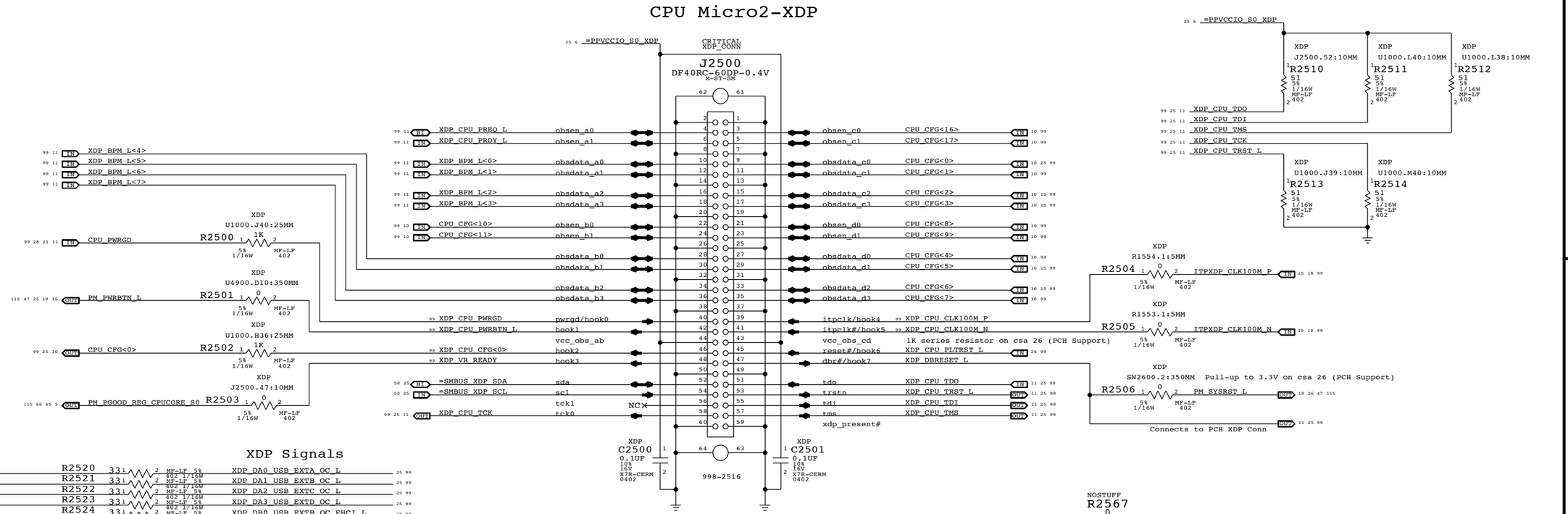
BRANCH prefsb

PAGE 23 OF 143

SHEET 23 OF 117



CPU Micro2-XDP

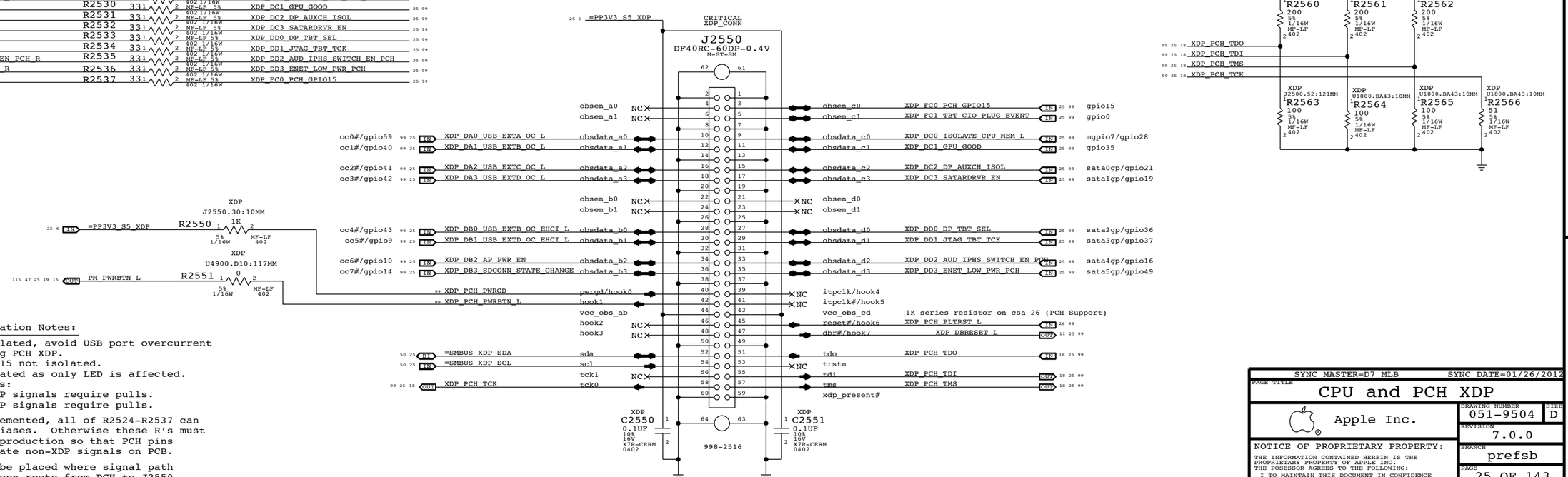


PCH Signals

USB_EXTA_OC_R_L	R2520	33	XDP_DA0_USB_EXTA_OC_L
USB_EXTB_OC_R_L	R2521	33	XDP_DA1_USB_EXTB_OC_L
USB_EXTC_OC_R_L	R2522	33	XDP_DA2_USB_EXTC_OC_L
USB_EXTD_OC_R_L	R2523	33	XDP_DA3_USB_EXTD_OC_L
USB_EXTB_OC_EHCI_R_L	R2524	33	XDP_DB0_USB_EXTB_OC_EHCI_L
USB_EXTD_OC_EHCI_R_L	R2525	33	XDP_DB1_USB_EXTD_OC_EHCI_L
AP_PWR_EN_R	R2526	33	XDP_DB2_AP_PWR_EN
SDCONN_STATE_CHANGE_R	R2527	33	XDP_DB3_SDCONN_STATE_CHANGE
TBT_CIO_PLUG_EVENT_R	R2528	33	XDP_FC1_TBT_CIO_PLUG_EVENT
ISOLATE_CPU_MEM_R_L	R2529	33	XDP_DC0_ISOLATE_CPU_MEM_L
GPU_GOOD_R	R2530	33	XDP_DC1_GPU_GOOD
DP_AUXCH_ISOL_R	R2531	33	XDP_DC2_DP_AUXCH_ISOL
SATARDRVR_EN_R	R2532	33	XDP_DC3_SATARDRVR_EN
DP_TBT_SEL_R	R2533	33	XDP_DD0_DP_TBT_SEL
JTAG_TBT_TCK_R	R2534	33	XDP_DD1_JTAG_TBT_TCK
AUD_IPHS_SWITCH_EN_PCH_R	R2535	33	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH_R	R2536	33	XDP_DD3_ENET_LOW_PWR_PCH
XDP_PIN03	R2537	33	XDP_FC0_PCH_GPIO15

XDP Signals

PCH Micro2-XDP



PCH/XDP Signal Isolation Notes:

- USB OC#'s not isolated, avoid USB port overcurrent events while using PCH XDP.
- Unused GPIOs 0 & 15 not isolated.
- MXM_GOOD not isolated as only LED is affected.
- For isolated GPIOs:
  - 'Output' non-XDP signals require pulls.
  - 'Output' PCH/XDP signals require pulls.

If PCH XDP not implemented, all of R2524-R2537 can be replaced with aliases. Otherwise these R's must be stuffed even in production so that PCH pins connect to appropriate non-XDP signals on PCB.

R2524-R2537 should be placed where signal path needs to split between route from PCH to J2550 and path to non-XDP signal destination.

SYNC MASTER=D7 MLB SYNC DATE=01/26/2012

PAGE TITLE: CPU and PCH XDP

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DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

PAGE: 25 OF 143

SHEET: 25 OF 117

System 25MHz Clock Generator

VDD must be powered if any VDDIO is.
ENET > S0 > TBT, so ENET is used here.

GreenClk 25MHz Power — =PP3V3_S4_ENET_SYSCLK
Ethernet XTAL Power — =PP3V3_S4_ENET_CLK
SB XTAL Power — =PP1V8_S0_PCH_CLK
TBT XTAL Power — =PP3V3_TBT_CLK

C2624 0.1UF 20% 10V CERM 402
C2622 0.1UF 20% 10V CERM 402
C2620 0.1UF 20% 10V CERM 402
C2602 1UF 10% 6.3V CERM 402

U2600 SLG3NB146V TDFN CRITICAL
VDD, VDDIO_A, VDDIO_B, VDDIO_C, XOUT, XIN, GND, THRM PAD
25MHZ_A — SYSCLK_CLK25M_SB
25MHZ_B — SYSCLK_CLK25M_ENET_R
25MHZ_C — SYSCLK_CLK25M_TBT

C2605 12PF 5% 50V C0G-CERM 0402
C2606 12PF 5% 50V C0G-CERM 0402
Y2605 CRITICAL 25.000MHZ-20PPM-12PF-85C 3.2X2.5MM-SM
R2605 0 5% 1/16W MF-LF 402
R2606 1M 5% 1/16W MF-LF 402 NO STUFF
SYSCLK_CLK25M_X2 — SYSCLK_CLK25M_X2_R — SYSCLK_CLK25M_X1
NOTE: 30 PPM crystal required

RTC Power Sources

Coin-Cell Holder
J2600 BB10201-C1403-7H SM 511-0054
PPVBATT_G3_RTC — MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
R2602 1K 5% 1/16W MF-LF 402
=PP3V3_G3H_RTC_D — PPVBATT_G3_RTC_R — MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.2 mm VOLTAGE=3.3V
D2600 BAT54DW-X-G SOT-363
PP3V3_G3_RTC — MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=3.3V
TP2600 1.97X2.02MM-NSP SMT-PAD OMIT
TP2601 1.97X2.02MM-NSP SMT-PAD OMIT

RDAR://11218892 TESTPOINT TO RESET RTC FOR APPLE CARE

TP2602 1.4-SQ-NSP SM-PAD OMIT — RTC_RESET_L
TP2603 1.4-SQ-NSP SM-PAD OMIT

PCH RTC Crystal

PCH_CLK32K_RTCX2 — R2610 0 5% 1/16W MF-LF 402 — PCH_CLK32K_RTCX2_R
R2611 10M 5% 1/16W MF-LF 402
Y2610 CRITICAL 32.768K-12.5PF SM-HF
C2610 12PF 5% 50V C0G-CERM 0402 PLACE_NEAR=Y2610.3:7MM
C2611 12PF 5% 50V C0G-CERM 0402 PLACE_NEAR=Y2610.1:2MM
PCH_CLK32K_RTCX1

Clock series termination

LPC_CLK33M_SMC_R — PLACE_NEAR=U1800.AT11:10mm — R2625 33 5% 1/16W MF-LF 402 — LPC_CLK33M_SMC
LPC_CLK33M_LPCPLUS_R — PLACE_NEAR=U1800.AN14:10mm — R2626 33 5% 1/16W MF-LF 402 — LPC_CLK33M_LPCPLUS
PCH_CLK33M_PCIOUT — PLACE_NEAR=U1800.AT14:10mm — R2627 33 5% 1/16W MF-LF 402 — PCH_CLK33M_PCIIN
SYSCLK_CLK25M_ENET_R — PLACE_NEAR=U2600.4:10MM — R2628 33 5% 1/16W MF-LF 402 — SYSCLK_CLK25M_ENET

PCH 25MHZ CLOCK

SYSCLK_CLK25M_SB From GreenClk @ 1.8V — R2671 40.2 1% 1/16W MF-LF 402 — PCH_CLK25M_XTALIN to PCH @ 1.1V
R2672 140 1% 1/16W MF-LF 402

GPIO Isolation to prevent glitches on critical core well GPIOs

=PP3V3_S5_PCH — C2650 0.1UF 20% 10V CERM 402 PLACE_NEAR=U2650.8:2MM
U2650 74LVC2G08GT SOT833 CRITICAL
TBT_PWR_EN_PCH, LPC_PWRDWN_L — TBT_PWR_EN
=PP3V3_S5_PCH — ENET_LOW_PWR_PCH, PM_PCH_PWROK — ENET_LOW_PWR
=PP3V3_S5_PCH — C2660 0.1UF 20% 10V CERM 402 PLACE_NEAR=U2660.5:2MM
U2660 MC74VHC1G08 SOT23-5-HF — AUD_IPHS_SWITCH_EN_PCH, PM_PCH_PWROK — AUD_IPHS_SWITCH_EN

Platform Reset Connections

PLT_RESET_L MAKE_BASE=TRUE

Unbuffered:
R2681 33 5% 1/16W MF-LF 402 — DEBUG_RESET_L
R2655 33 5% 1/16W MF-LF 402 — SMC_LRESET_L MAKE_BASE=TRUE
XDP R2699 1K 5% 1/16W MF-LF 402 — XDP_PCH_PLTRST_L

Buffered:
XDP R2698 1K 5% 1/16W MF-LF 402 — XDP_CPU_PLTRST_L
MAY NEED TO MOVE LONGER TRACE ONES TO BUFFERED
R2694 VREFMRGN:EXT 33 5% 1/16W MF-LF 402 — PCA9557D_RESET_L

=PP3V3_S0_RSTBUF — U2680 MC74VHC1G08 SOT23-5-HF — PLT_RST_BUF_L
C2680 0.1UF 20% 10V CERM 402
R2680 100K 5% 1/16W MF-LF 402
R2690 33 5% 1/16W MF-LF 402 — GPU_RESET_L
R2691 33 5% 1/16W MF-LF 402 — TBT_PLT_RST_L MAKE_BASE=TRUE — =TBT_RESET_L
R2688 33 5% 1/16W MF-LF 402 — AP_RESET_L
R2692 33 5% 1/16W MF-LF 402 — ENET_SD_RESET_L

=PP3V3_S0_RSTBUF — OPEN-DRAIN BUFFER
U2690 74LVC1G07 SC70 — CPU_RESET_L
VTT VOLTAGE DIVIDER AND PU ON CPU PAGE
C2690 0.1UF 20% 10V CERM 402

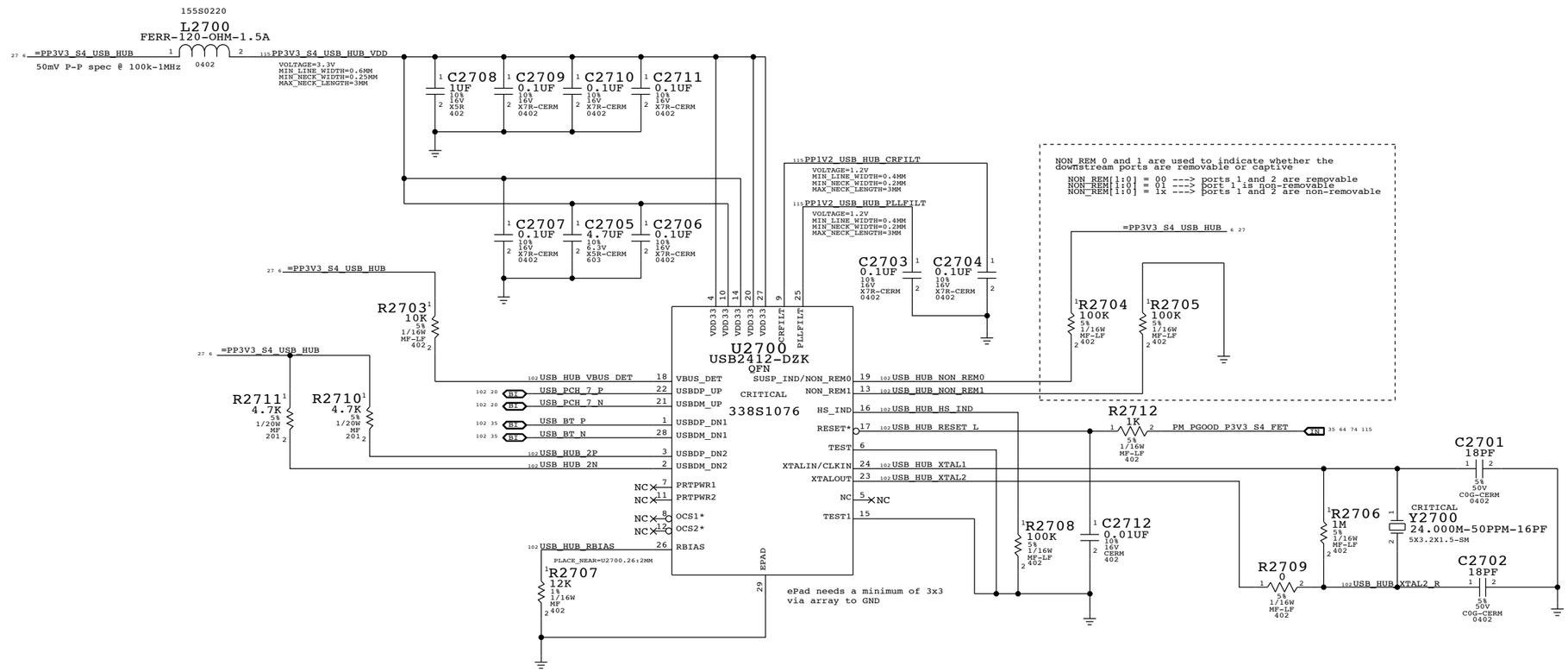
Reset Button

=PP3V3_S0_PCH_PM — R2697 4.7K 5% 1/16W MF-LF 402
DEVELOPMENT SW2600 NTC020AA1JB260T SM
SILK_PART=SYS RESET
PM_SYSRST_L
NOSTUFF R2696 0 5% 1/16W MF-LF 402 SILK_PART=SYS RESET

SYNC MASTER=D8 MLB — SYNC DATE=N/A
PAGE TITLE: CHIPSET SUPPORT

Apple Inc.

DRAWING NUMBER	051-9504
SIZE	D
REVISION	7.0.0
BRANCH	prefsb
PAGE	26 OF 143
SHEET	26 OF 117



SYNC MASTER=D8 ROSITA SYNC DATE=03/23/2012

PAGE TITLE
USB 2.0 HUB (BT/SMC)

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

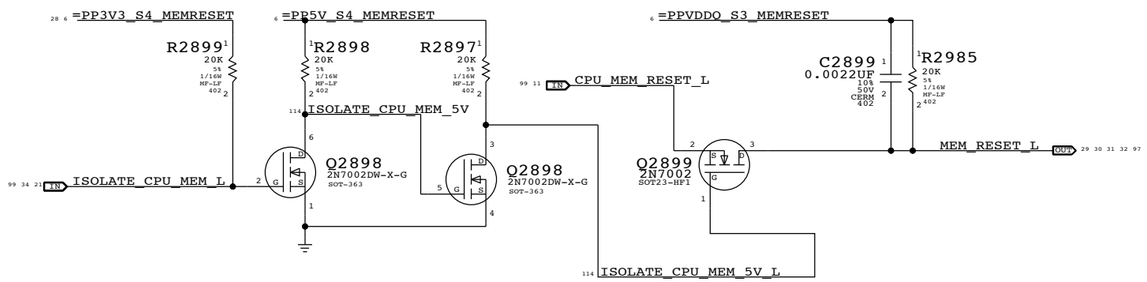
PAGE 27 OF 143

SHEET 27 OF 117

MEM_RESET_L Generator

The circuits below handle MEMVTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

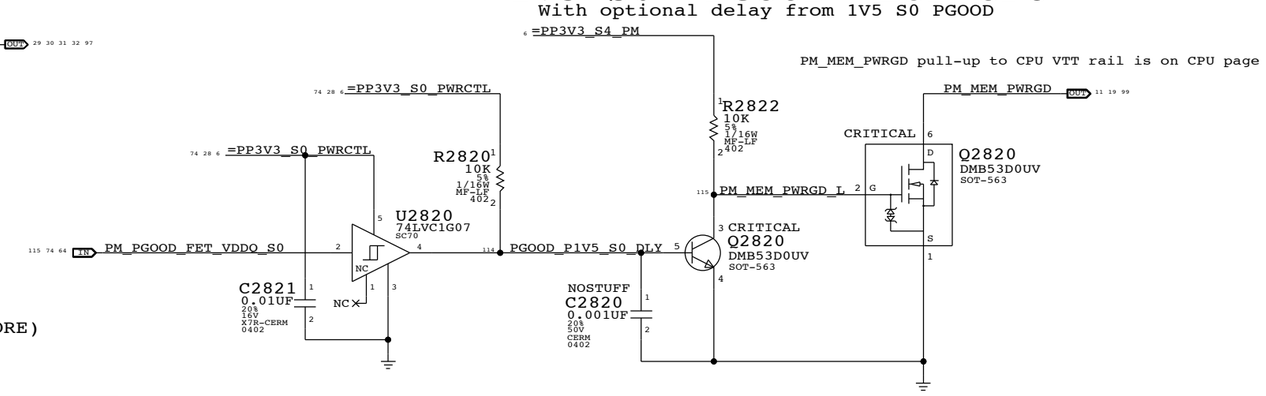
ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behaviour of signals.
WHEN HIGH: MEM_RESET_L NOT ISOLATED.
WHEN LOW: MEM_RESET_L IS ISOLATED.
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L (Block CPU from driving MEM_RESET_L in S3)



1V5 S0 "PGOOD" for CPU

With optional delay from 1V5 S0 PGOOD

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page

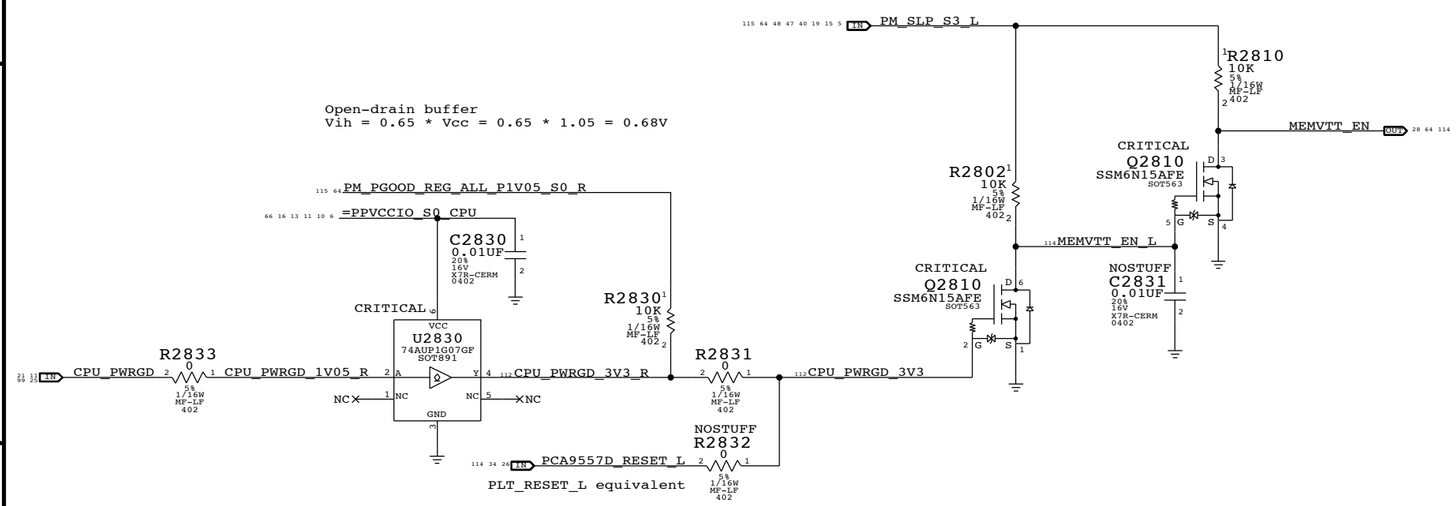


MEMVTT_EN Generator

rdar://11117167 Enables MEMVTT when PCH drives CPU PWRGD.

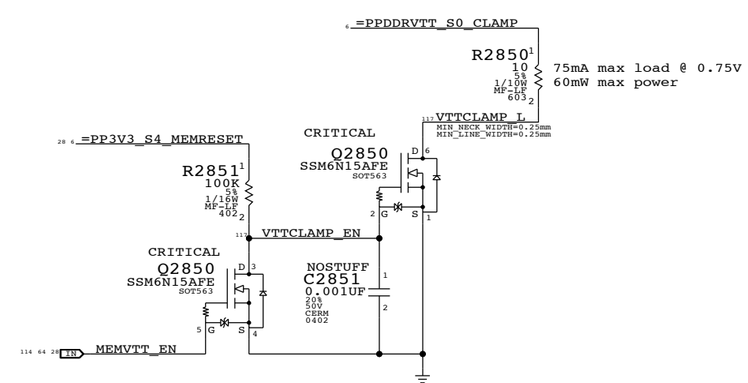
CPU does not drive MEM_CKE until VCCORE activated but CPU 1V5 (VDDQ) leaks into it.
Clamping MEMVTT will keep the MEM_CKE low until CPU actively controls it.
MEMVTT Clamp actively holds MEMVTT rail low until MEMVTT is enabled.
MEMVTT_EN = CPU_PWRGD * PM_SLP_S3_L (VTT is enabled when PCH tells CPU to enable VCCORE)

Open-drain buffer
Vih = 0.65 * Vcc = 0.65 * 1.05 = 0.68V



MEMVTT Clamp

Ensures CKE signals are held low in S3 and in S0 before CPU PWRGD



	Step	ISOLATE_CPU_MEM_L	PM_SLP_S3_L	CPU_PWRGD	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN
S0	0	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1
S3	2	0	1	1	1	1	1
	3	0	0	0	X	1	0
	4	0	0	0	X	1	0
to	5	0	1	1	0 (*)	1	1
	6	0	1	1	1	1	1
S0	7	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: On a S5->S0 transition, ISOLATE_CPU_MEM_L will default low.
Rails will power-up as if from S3, but MEM_RESET_L now needs to be asserted in S0. Software must de-assert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=D8 MARK SYNC DATE=04/23/2012

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

PAGE: 28 OF 143

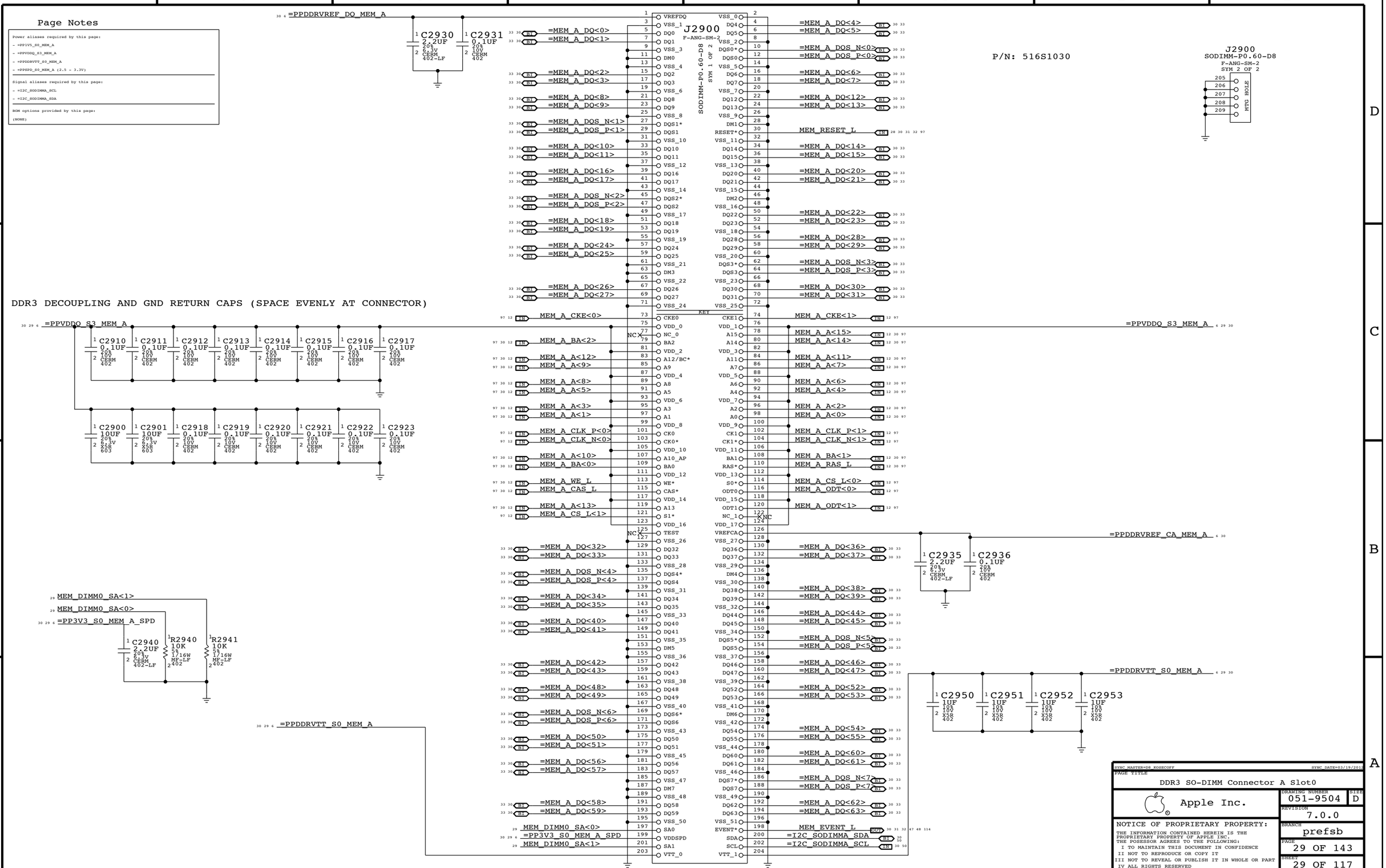
SHEET: 28 OF 117

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PPVDDQ_S3_MEM_A
- =PPDDRVTT_S0_MEM_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)



SYNC_MASTER=D8_KOSECOFF SYNC_DATE=03/19/2012

PAGE TITLE

DDR3 SO-DIMM Connector A Slot0

Apple Inc.

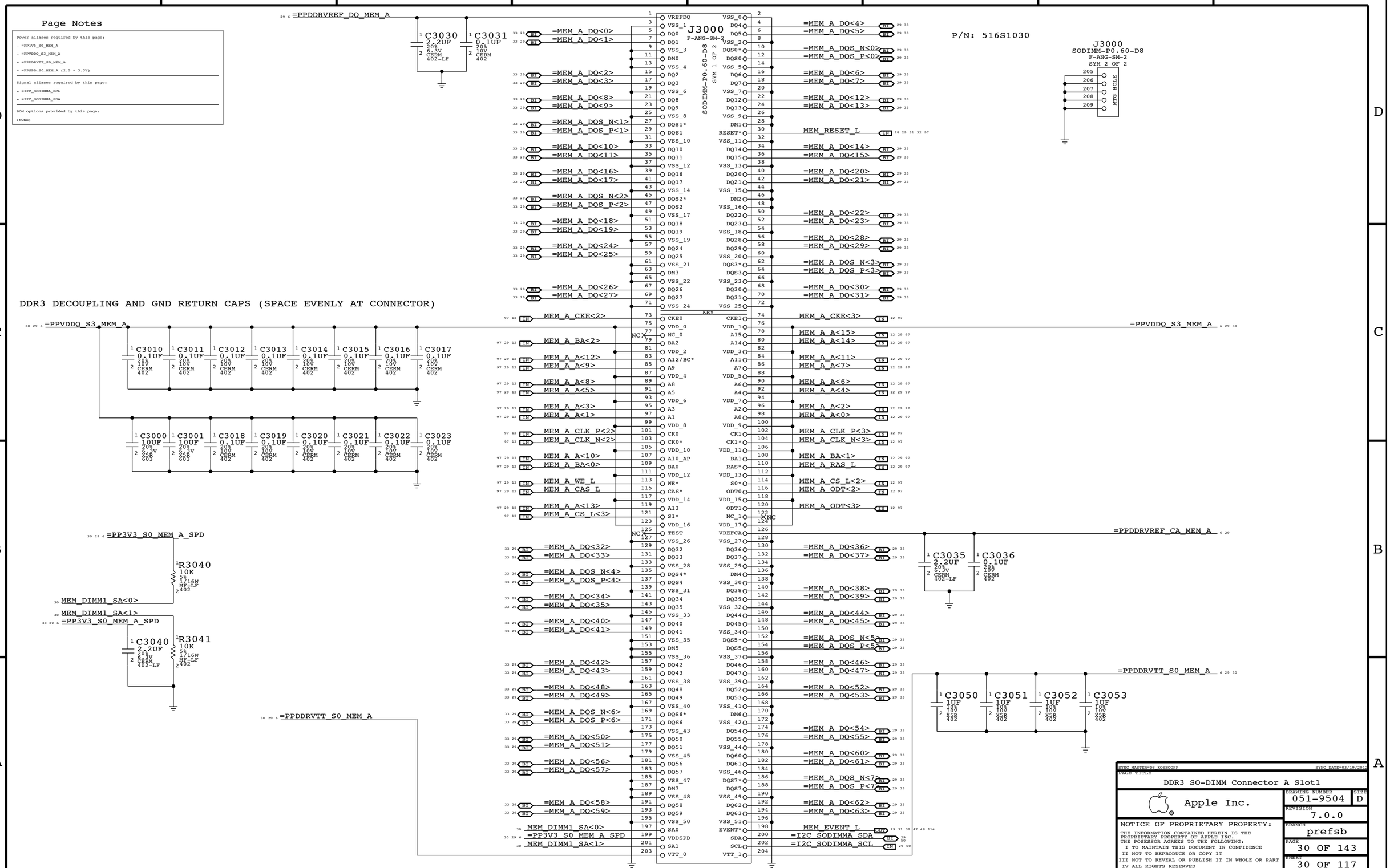
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 29 OF 143

SHEET 29 OF 117



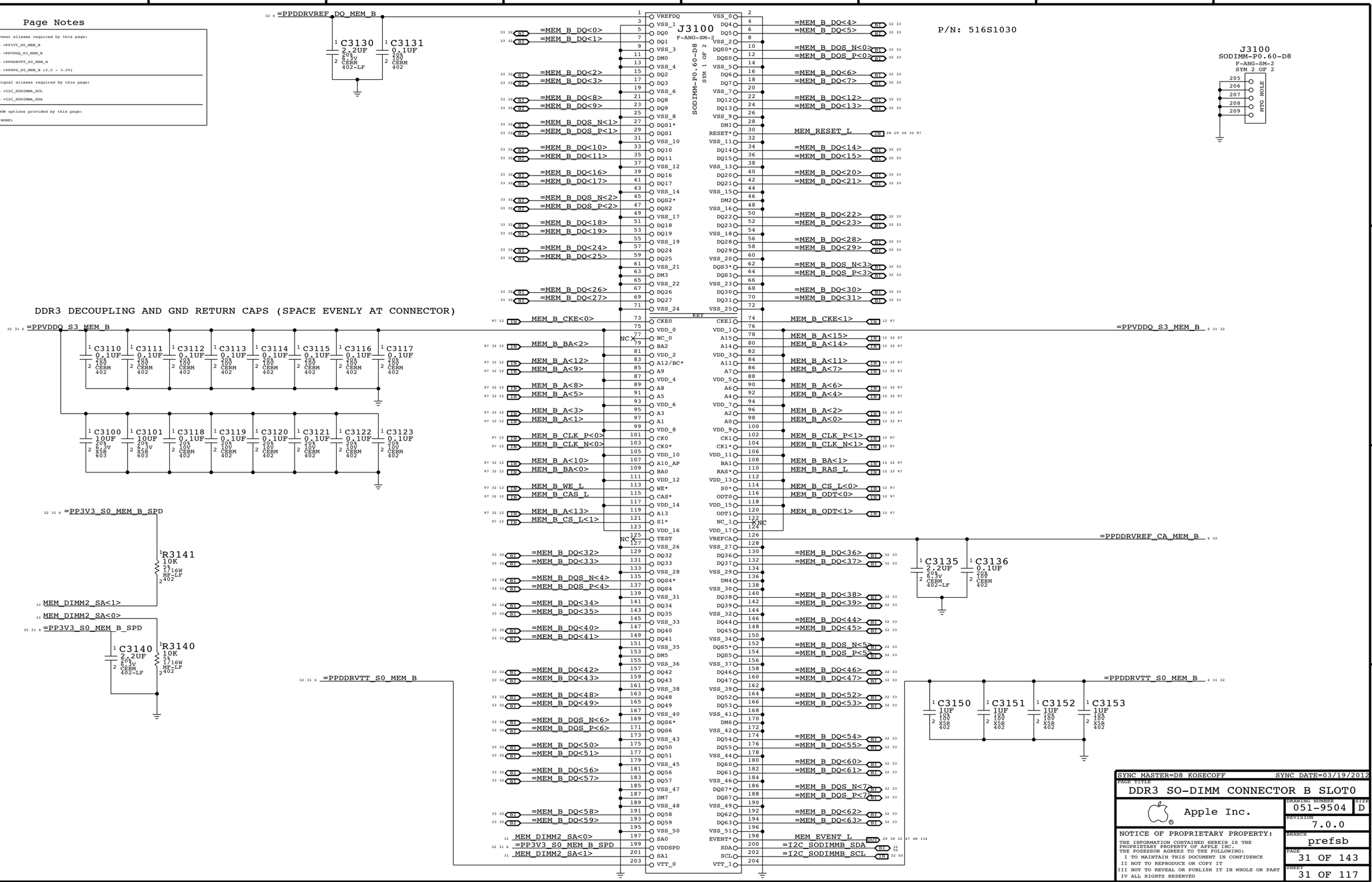
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030



SYNC MASTER=D8 KOSECOFF SYNC DATE=03/19/2012

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B SLOT0

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 31 OF 143
SHEET 31 OF 117

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PPVDDQ_S3_MEM_B
- =PPDDRVTT_S0_MEM_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

P/N: 516S1030

=PPDDRVREF_DQ_MEM_B

C3230 2.2UF 20% 6.3V CERM 402-LF
C3231 0.1UF 20% 10V CERM 402

J3200
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 1 OF 2

Pin	Signal	Pin	Signal
1	VREFDQ	2	VSS_0
3	VSS_1	4	DQ4
5	DQ0	6	DQ5
7	DQ1	8	VSS_2
9	VSS_3	10	DQS0*
11	DM0	12	DQS0
13	VSS_4	14	VSS_5
15	DQ2	16	DQ6
17	DQ3	18	DQ7
19	VSS_6	20	VSS_7
21	DQ8	22	DQ12
23	DQ9	24	DQ13
25	VSS_8	26	VSS_9
27	DQS1*	28	DM1
29	DQS1	30	RESET*
31	VSS_10	32	VSS_11
33	DQ10	34	DQ14
35	DQ11	36	DQ15
37	VSS_12	38	VSS_13
39	DQ16	40	DQ20
41	DQ17	42	DQ21
43	VSS_14	44	VSS_15
45	DQS2*	46	DM2
47	DQS2	48	VSS_16
49	VSS_17	50	DQ22
51	DQ18	52	DQ23
53	DQ19	54	VSS_18
55	VSS_19	56	DQ28
57	DQ24	58	DQ29
59	DQ25	60	VSS_20
61	VSS_21	62	DQS3*
63	DM3	64	DQS3
65	VSS_22	66	VSS_23
67	DQ26	68	DQ30
69	DQ27	70	DQ31
71	VSS_24	72	VSS_25
73	CKE0	74	CKE1
75	VDD_0	76	VDD_1
77	NC_0	78	A15
79	BA2	80	A14
81	VDD_2	82	VDD_3
83	A12/BC*	84	A11
85	A9	86	A7
87	VDD_4	88	VDD_5
89	A8	90	A6
91	A5	92	A4
93	VDD_6	94	VDD_7
95	A3	96	A2
97	A1	98	A0
99	VDD_8	100	VDD_9
101	CK0	102	CK1
103	CK0*	104	CK1*
105	VDD_10	106	VDD_11
107	A10_AP	108	BA1
109	BA0	110	RAS*
111	VDD_12	112	VDD_13
113	WE*	114	S0*
115	CAS*	116	ODT0
117	VDD_14	118	VDD_15
119	A13	120	ODT1
121	S1*	122	NC_1
123	VDD_16	124	VDD_17
125	TEST	126	VREFCA
127	VSS_26	128	VSS_27
129	DQ32	130	DQ36
131	DQ33	132	DQ37
133	VSS_28	134	VSS_29
135	DQS4*	136	DM4
137	DQS4	138	VSS_30
139	VSS_31	140	DQ38
141	DQ34	142	DQ39
143	DQ35	144	VSS_32
145	VSS_33	146	DQ44
147	DQ40	148	DQ45
149	DQ41	150	VSS_34
151	VSS_35	152	DQS5*
153	DM5	154	DQS5
155	VSS_36	156	VSS_37
157	DQ42	158	DQ46
159	DQ43	160	DQ47
161	VSS_38	162	VSS_39
163	DQ48	164	DQ52
165	DQ49	166	DQ53
167	VSS_40	168	VSS_41
169	DQS6*	170	DM6
171	DQS6	172	VSS_42
173	VSS_43	174	DQ54
175	DQ50	176	DQ55
177	DQ51	178	VSS_44
179	VSS_45	180	DQ60
181	DQ56	182	DQ61
183	DQ57	184	VSS_46
185	VSS_47	186	DQS7*
187	DM7	188	DQS7
189	VSS_48	190	VSS_49
191	DQ58	192	DQ62
193	DQ59	194	DQ63
195	VSS_50	196	VSS_51
197	SA0	198	EVENT*
199	VDDSPD	200	SDA
201	SA1	202	SCL
203	VTT_0	204	VTT_1

SODIMM-P0.60-D8 SYM 1 OF 2

Signal	Pin
=MEM_B_DQ<0>	5
=MEM_B_DQ<1>	7
=MEM_B_DQ<2>	15
=MEM_B_DQ<3>	17
=MEM_B_DQ<8>	21
=MEM_B_DQ<9>	23
=MEM_B_DQS_N<1>	27
=MEM_B_DQS_P<1>	29
=MEM_B_DQ<10>	33
=MEM_B_DQ<11>	35
=MEM_B_DQ<16>	39
=MEM_B_DQ<17>	41
=MEM_B_DQS_N<2>	45
=MEM_B_DQS_P<2>	47
=MEM_B_DQ<18>	51
=MEM_B_DQ<19>	53
=MEM_B_DQ<24>	57
=MEM_B_DQ<25>	59
=MEM_B_DQ<26>	67
=MEM_B_DQ<27>	69
MEM_B_CKE<2>	73
MEM_B_BA<2>	79
MEM_B_A<12>	83
MEM_B_A<9>	85
MEM_B_A<8>	89
MEM_B_A<5>	91
MEM_B_A<3>	95
MEM_B_A<1>	97
MEM_B_CLK_P<2>	101
MEM_B_CLK_N<2>	103
MEM_B_A<10>	107
MEM_B_BA<0>	109
MEM_B_WE_L	113
MEM_B_CAS_L	115
MEM_B_A<13>	119
MEM_B_CS_L<3>	121
=MEM_B_DQ<32>	129
=MEM_B_DQ<33>	131
=MEM_B_DQS_N<4>	135
=MEM_B_DQS_P<4>	137
=MEM_B_DQ<34>	141
=MEM_B_DQ<35>	143
=MEM_B_DQ<40>	147
=MEM_B_DQ<41>	149
=MEM_B_DQ<42>	157
=MEM_B_DQ<43>	159
=MEM_B_DQ<48>	163
=MEM_B_DQ<49>	165
=MEM_B_DQS_N<6>	169
=MEM_B_DQS_P<6>	171
=MEM_B_DQ<50>	175
=MEM_B_DQ<51>	177
=MEM_B_DQ<56>	181
=MEM_B_DQ<57>	183
=MEM_B_DQ<58>	191
=MEM_B_DQ<59>	193
MEM_DIMM3_SA<0>	197
=PP3V3_S0_MEM_B_SPD	199
MEM_DIMM3_SA<1>	201

SODIMM-P0.60-D8 SYM 1 OF 2

Signal	Pin
=MEM_B_DQ<4>	6
=MEM_B_DQ<5>	8
=MEM_B_DQS_N<0>	10
=MEM_B_DQS_P<0>	12
=MEM_B_DQ<6>	16
=MEM_B_DQ<7>	18
=MEM_B_DQ<12>	22
=MEM_B_DQ<13>	24
MEM_RESET_L	30
=MEM_B_DQ<14>	34
=MEM_B_DQ<15>	36
=MEM_B_DQ<20>	40
=MEM_B_DQ<21>	42
=MEM_B_DQ<22>	50
=MEM_B_DQ<23>	52
=MEM_B_DQ<28>	56
=MEM_B_DQ<29>	58
=MEM_B_DQS_N<3>	62
=MEM_B_DQS_P<3>	64
=MEM_B_DQ<30>	68
=MEM_B_DQ<31>	70
MEM_B_CKE<3>	74
MEM_B_A<15>	78
MEM_B_A<14>	80
MEM_B_A<11>	84
MEM_B_A<7>	86
MEM_B_A<6>	90
MEM_B_A<4>	92
MEM_B_A<2>	96
MEM_B_A<0>	98
MEM_B_CLK_P<3>	102
MEM_B_CLK_N<3>	104
MEM_B_BA<1>	108
MEM_B_RAS_L	110
MEM_B_CS_L<2>	114
MEM_B_ODT<2>	116
MEM_B_ODT<3>	120
=PPDDRVREF_CA_MEM_B	126
=MEM_B_DQ<36>	130
=MEM_B_DQ<37>	132
=MEM_B_DQ<38>	140
=MEM_B_DQ<39>	142
=MEM_B_DQ<44>	146
=MEM_B_DQ<45>	148
=MEM_B_DQS_N<5>	152
=MEM_B_DQS_P<5>	154
=MEM_B_DQ<46>	158
=MEM_B_DQ<47>	160
=MEM_B_DQ<52>	164
=MEM_B_DQ<53>	166
=MEM_B_DQ<54>	174
=MEM_B_DQ<55>	176
=MEM_B_DQ<60>	180
=MEM_B_DQ<61>	182
=MEM_B_DQS_N<7>	186
=MEM_B_DQS_P<7>	188
=MEM_B_DQ<62>	192
=MEM_B_DQ<63>	194
MEM_EVENT_L	198
=I2C_SODIMMB_SDA	200
=I2C_SODIMMB_SCL	202

J3200
SODIMM-P0.60-D8
F-ANG-SM-2
SYM 2 OF 2

Pin	Signal
205	MTG HOLE
206	
207	
208	
209	

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

=PPVDDQ_S3_MEM_B

C3210 0.1UF 20% 10V CERM 402
C3211 0.1UF 20% 10V CERM 402
C3212 0.1UF 20% 10V CERM 402
C3213 0.1UF 20% 10V CERM 402
C3214 0.1UF 20% 10V CERM 402
C3215 0.1UF 20% 10V CERM 402
C3216 0.1UF 20% 10V CERM 402
C3217 0.1UF 20% 10V CERM 402

C3200 10UF 20% 6.3V X5R 603
C3201 10UF 20% 6.3V X5R 603
C3218 0.1UF 20% 10V CERM 402
C3219 0.1UF 20% 10V CERM 402
C3220 0.1UF 20% 10V CERM 402
C3221 0.1UF 20% 10V CERM 402
C3222 0.1UF 20% 10V CERM 402
C3223 0.1UF 20% 10V CERM 402

=PP3V3_S0_MEM_B_SPD

R3241 10K 5% 1/16W MF-LF 402
R3240 10K 5% 1/16W MF-LF 402

MEM_DIMM3_SA<1>
MEM_DIMM3_SA<0>
=PP3V3_S0_MEM_B_SPD

C3240 2.2UF 20% 6.3V CERM 402-LF

=PPDDRVTT_S0_MEM_B

C3235 2.2UF 20% 6.3V CERM 402-LF
C3236 0.1UF 20% 10V CERM 402

=PPDDRVTT_S0_MEM_B

C3250 1UF 10% 10V X5R 402
C3251 1UF 10% 10V X5R 402
C3252 1UF 10% 10V X5R 402
C3253 1UF 10% 10V X5R 402

SYNC MASTER=D8 KOSECOFF SYNC DATE=03/19/2012

PAGE TITLE
DDR3 SO-DIMM CONNECTOR B SLOT1

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DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 32 OF 143
SHEET 32 OF 117

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>		MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>		MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	
MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<7>		MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	
MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>		MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	
MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<4>		MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	
MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<1>		MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	
MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<3>		MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	
MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<2>		MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	
MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<5>		MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	
MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<0>		MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	
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MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>		MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	
MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<15>		MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	
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MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<33>		MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	
MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<36>		MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	
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MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<46>		MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	
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SYNC MASTER=D8 KOSECOFF SYNC DATE=03/19/2012

PAGE TITLE
DDR3 ALIASES AND BITSWAPS

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

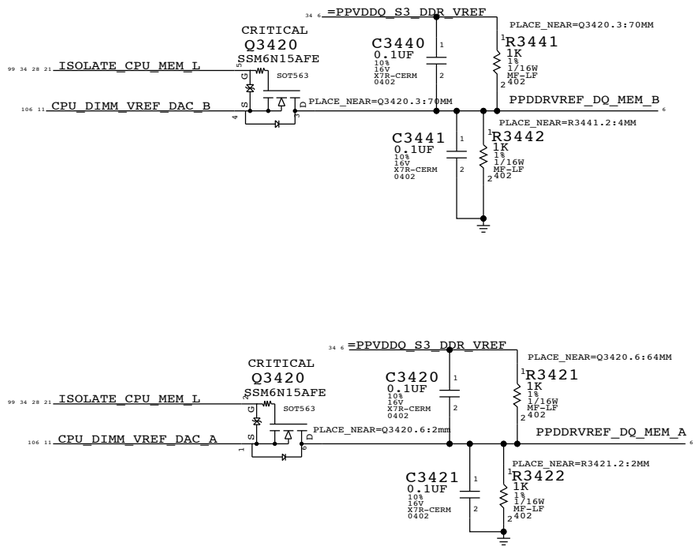
PAGE 33 OF 143

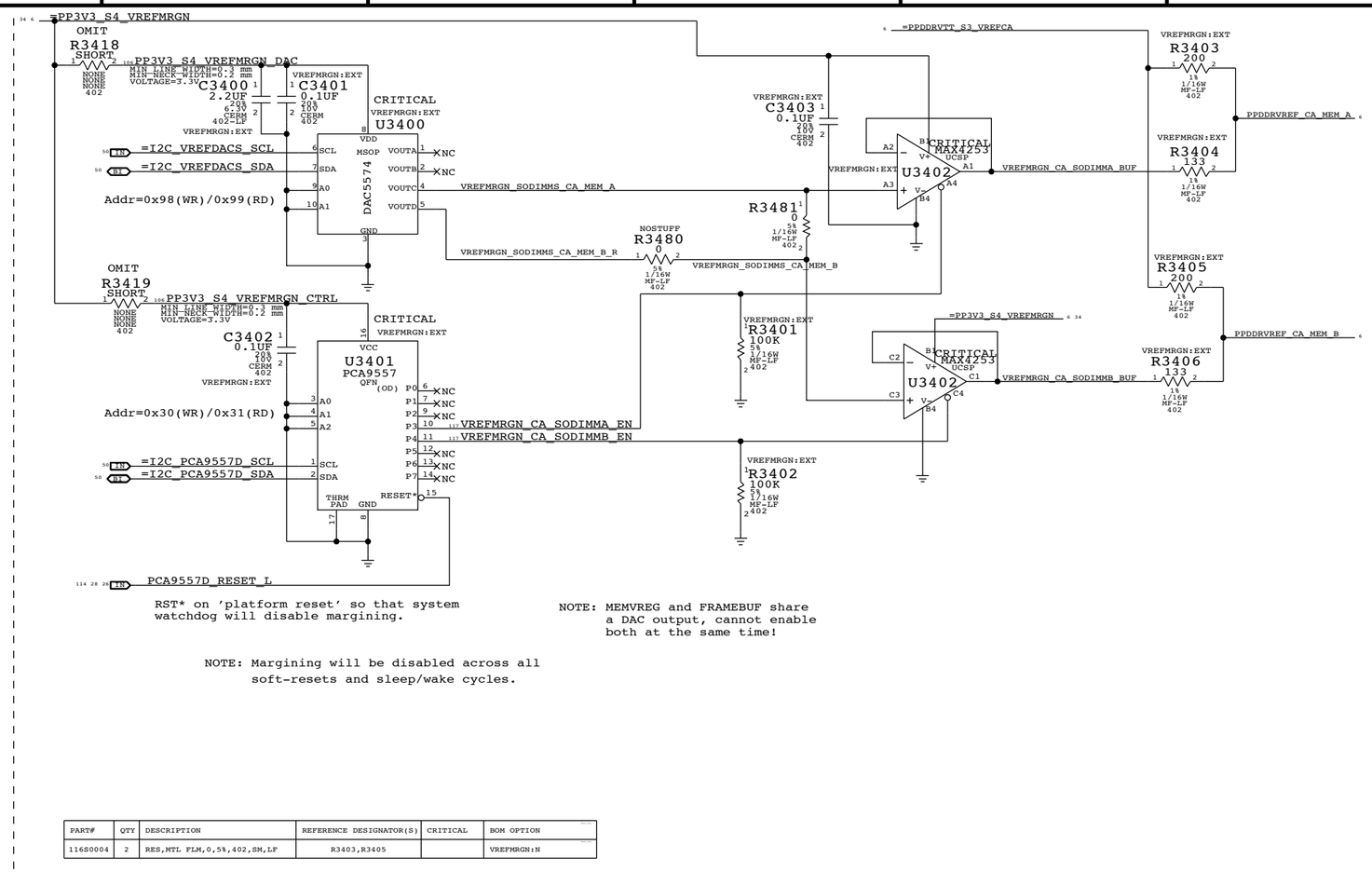
SHEET 33 OF 117

VRef DQ

Driven by CPU

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step





RST* on 'platform reset' so that system watchdog will disable margining.

NOTE: MEMVREG and FRAMEBUF share a DAC output, cannot enable both at the same time!

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11680004	2	RES,MTL FLM,0,5%,402,SM,LF	R3403,R3405		VREFMRGN:N

	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	C	C	D	D
PCA9557D Pin:	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)		1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)		1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)		0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)		+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output		8.59mV / step @ output	1.51mV / step @ output

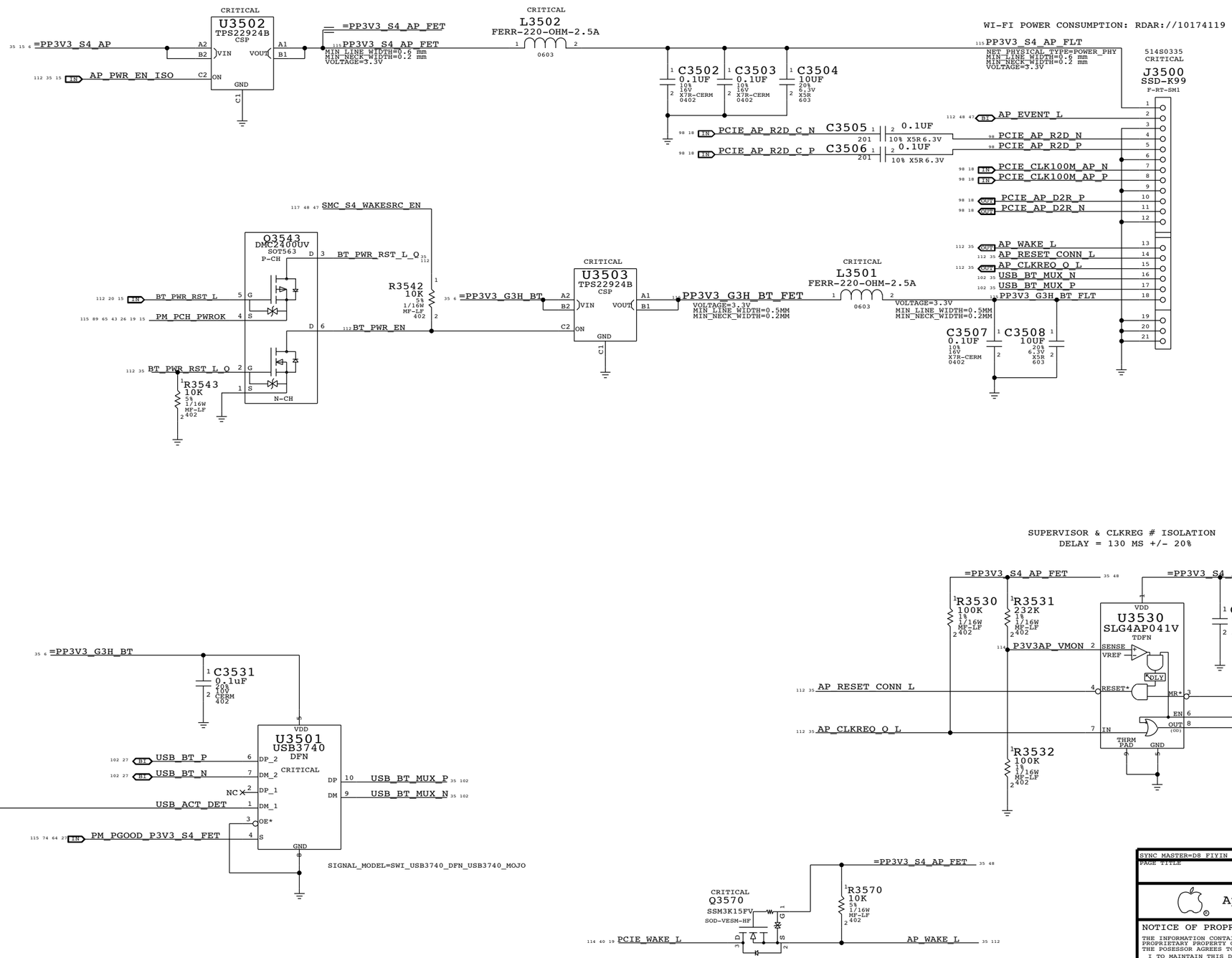
SYNC MASTER=D8 KOSECOFF SYNC DATE=03/19/2012

PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 34 OF 143
SHEET 34 OF 117

AIRPORT BLUETOOTH



SYNC MASTER=D8_FIYIN SYNC DATE=07/02/2012

PAGE TITLE: AIRPORT/BT

Apple Inc.

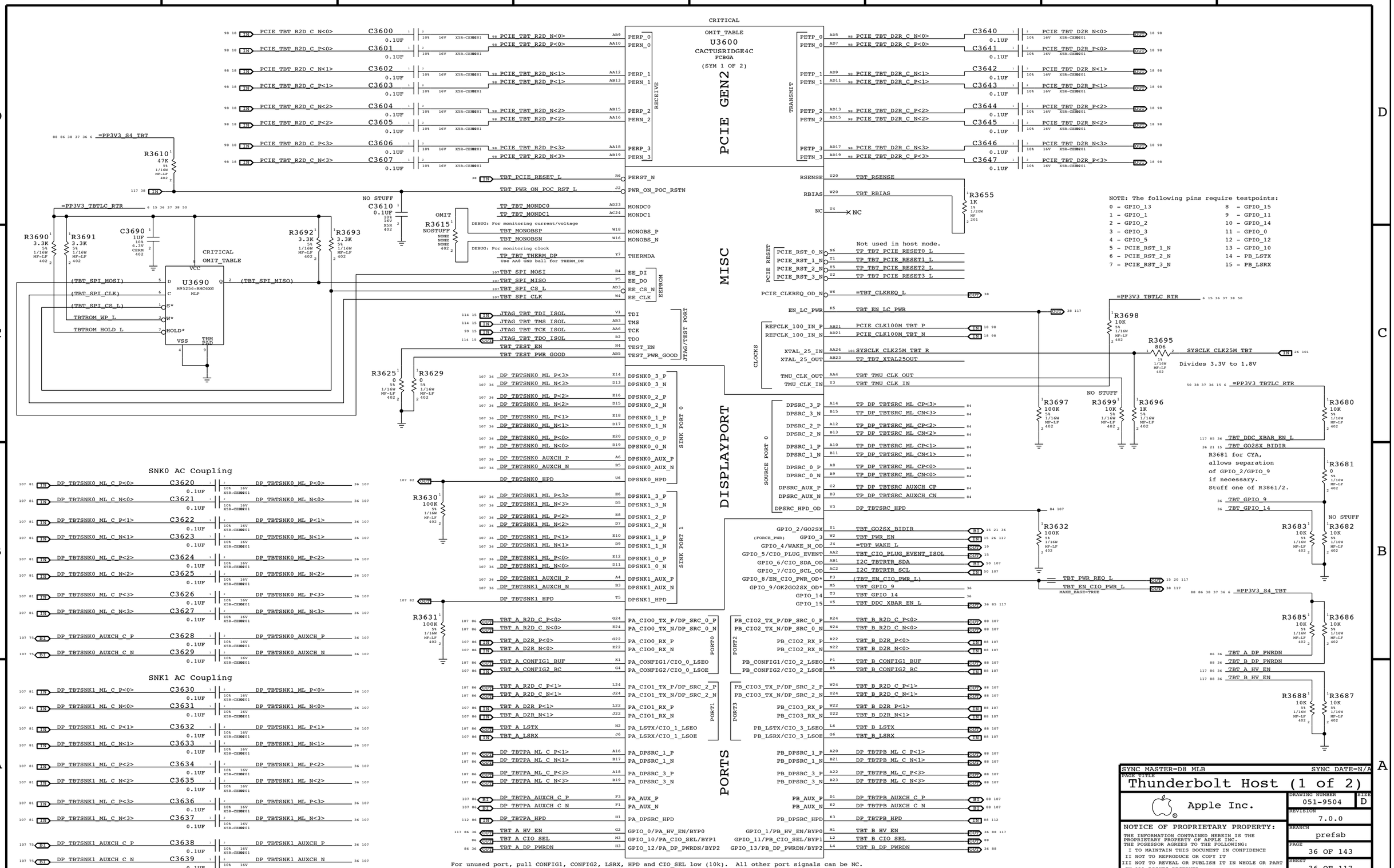
DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

PAGE: 35 OF 143

SHEET: 35 OF 117

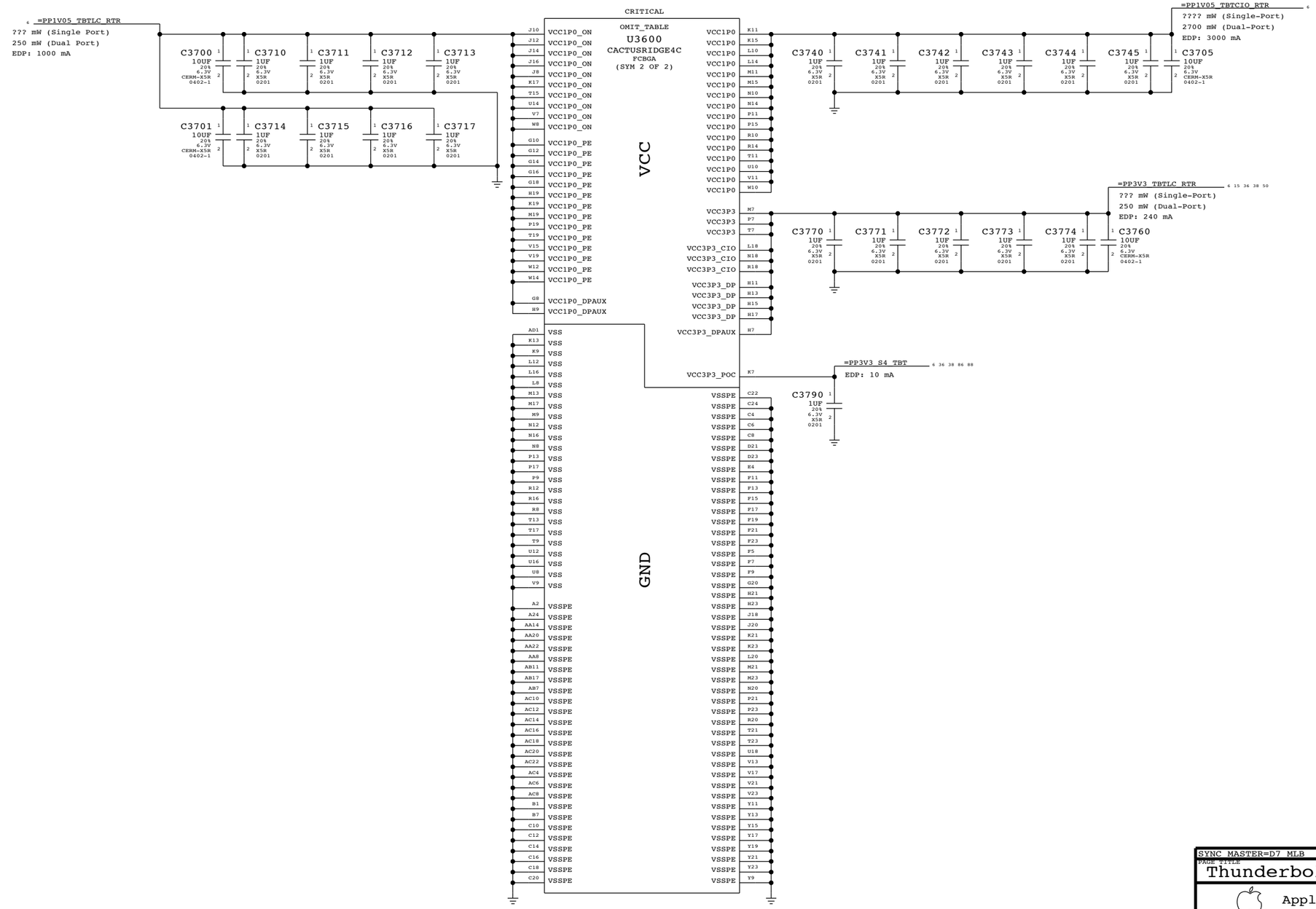


SYNC MASTER=D8 MLB SYNC DATE=N/A

PAGE TITLE
Thunderbolt Host (1 of 2)

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 36 OF 143
SHEET 36 OF 117



EDP current / power consumption figures from CR DG v0.57, IBL doc #472455.

SYNC MASTER=D7_MLB SYNC DATE=03/15/2012

PAGE TITLE
Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 37 OF 143

SHEET 37 OF 117

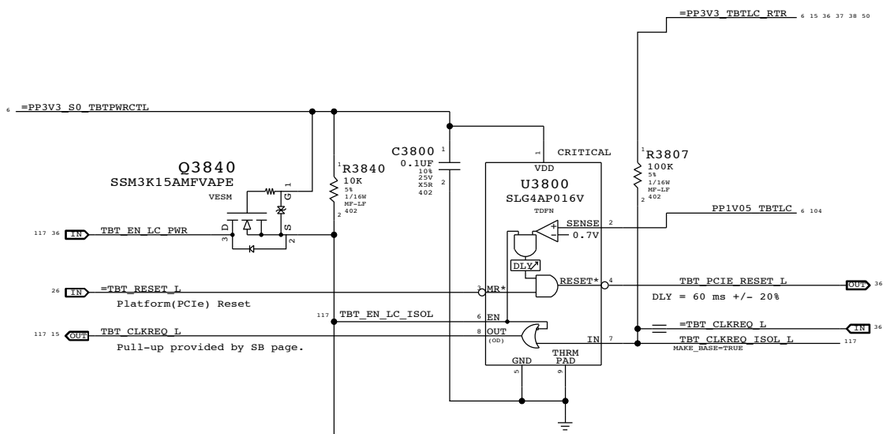
Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)
- =PP3V3_TBT_P3V3TBTFET (3.3V FET Input)
- =PP3V3_TBT_FET (3.3V FET Output)
- =PP3V3_S0_TBTPWRCTL
- =PP1V05_TBT_P1V05TBTFET (1.05V FET Input)
- =PP1V05_TBT_FET (1.05V FET Output)

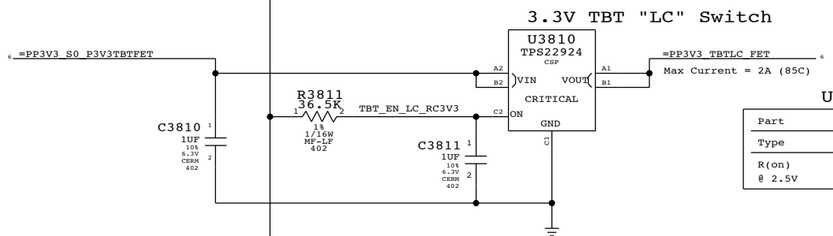
Signal aliases required by this page:
- =TBT_CLKREQ_L
- =TBT_RESET_L

BOM options provided by this page:
TBTBST:Y - Stuffs 15V boost circuitry.

Supervisor & CLKREQ# Isolation



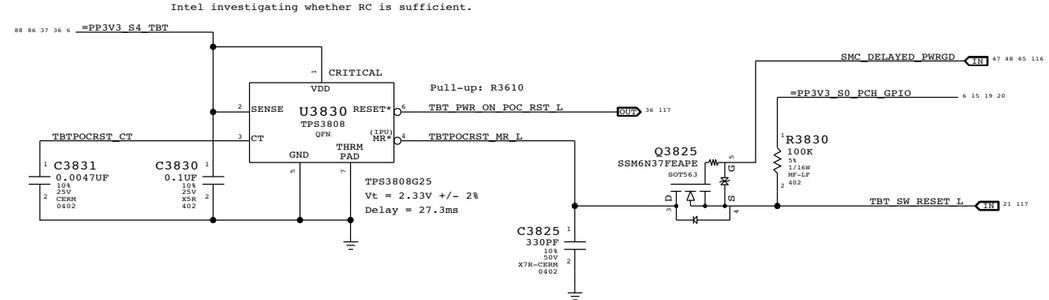
3.3V TBT "LC" Switch



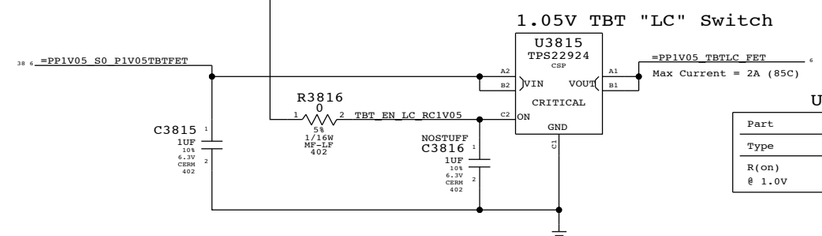
U3810	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

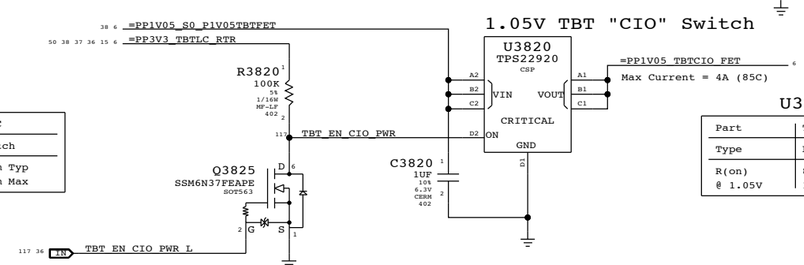


1.05V TBT "LC" Switch



U3815	
Part	TPS22924C
Type	Load Switch
R(on) @ 1.0V	20.3 mOhm Typ 28.6 mOhm Max

1.05V TBT "CIO" Switch



U3820	
Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC MASTER=D7_MLB SYNC DATE=03/15/2012

PAGE TITLE
Thunderbolt Power Support

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 38 OF 143
SHEET 38 OF 117

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

=PP3V3_S4_ENET_FET
281mA (1000base-T max power, Caesar IV)

R3901 0 5% 1/16W MF-LF 402
PP3V3_S4_ENET_FET_SRVDD — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V
C3979 4.7UF 20% 6.3V X5R-CERM1 402
C3996 0.1UF 10% 16V X5R-CERM 0201
C3997 0.1UF 10% 16V X5R-CERM 0201
=PP3V3R1V8_CR_IOPWR_OUT — VDD for Card Reader I/O

CRITICAL L3900 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_S4_ENET_FET_XTALVDDH — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V
C3900 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3905 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_S4_ENET_FET_BIASVDDH — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V
C3905 0.1UF 10% 16V X5R-CERM 0201

CRITICAL L3910 FERR-600-OHM-300MA-0.85OHM 0402
PP3V3_S4_ENET_FET_AVDDH — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X5R-CERM 0201
C3911 0.1UF 10% 16V X5R-CERM 0201
C3912 1.0UF 10% 6.3V X5R-CERM 0201

C3915 4.7UF 20% 6.3V X5R-CERM1 402
C3999 0.1UF 10% 16V X5R-CERM 0201
C3998 0.1UF 10% 16V X5R-CERM 0201
C3916 0.1UF 10% 16V X5R-CERM 0201

=PP3V3_S0_ENET
R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

ENET_SR_LX
ENET_SR_VFB
Internal 1.2V Switching Regulator pins.

=PP1V2_S4_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL L3920 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_S4_ENET_PHY_AVDDL — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=1.2V
C3921 0.1UF 10% 16V X5R-CERM 0201
C3920 4.7UF 20% 6.3V X5R-CERM1 402
C3913 1.0UF 10% 6.3V X5R-CERM 0201

CRITICAL L3925 FERR-600-OHM-0.5A SM
PP1V2_S4_ENET_PHY_PCIEPLL — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=1.2V
C3926 0.1UF 10% 16V X5R-CERM 0201
C3925 4.7UF 20% 6.3V X5R-CERM1 402

CRITICAL L3930 FERR-600-OHM-300MA-0.85OHM 0402
PP1V2_S4_ENET_PHY_GPHYPLL — MIN LINE WIDTH=0.4 mm, MIN NECK WIDTH=0.2 MM, VOLTAGE=1.2V
C3931 0.1UF 10% 16V X5R-CERM 0201
C3930 4.7UF 20% 6.3V X5R-CERM1 402

C3936 0.1UF 10% 16V X5R-CERM 0201
C3935 10UF 20% 6.3V X5R 603

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

OMIT_TABLE
U3900
BCM57765
QFN-8X8

Signal	Pin	Note
AVDDH	42, 48	
BIASVDDH	37	
XTALVDDH	17	
VDDO	7, 20, 56, 62	
SR_VDD	14	
SR_VDDP	15	
SR_LX	16	
SR_VFB	13	
AVDDL	39, 45, 51	
PCIE_PLLVDDL	29, 32	
GPHY_PLLVDDL	36	
VDDC	35, 61	
VMAIN_PRSNT	58	(IPD-ENET)
PCIE_TXD_N	27	
PCIE_TXD_P	28	
PCIE_RXD_P	33	
PCIE_RXD_N	34	
PCIE_REFCLK_P	31	
PCIE_REFCLK_N	30	
PERST*	11	(IPD)
CLKREQ*	12	(OD)
WAKE*	3	(OD)
LOW_PWR	4	(IPD)
SMB_CLK	6	
SMD_DATA	10	(IPD-ENETM)
SCLK	66	
SI/LINKLED*	64	
SO	65	
CS*	63	
SPD100LED*/SERIAL_DO	2	(OD)
TRAFFICLED*/SERIAL_DI	67	(OD)
XTALI	18	
XTALO	19	NC
RDAC	38	
THRM_PAD	69	
TRD0_P	40	
TRD0_N	41	
TRD1_P	44	
TRD1_N	43	
TRD2_P	46	
TRD2_N	47	
TRD3_P	50	
TRD3_N	49	
GPIO_0	5	(IPD)
GPIO_1/CR_BUS_PWR	8	
RE*/GPIO_2	9	
SD_DETECT/WE*	1	(IPx-ENETM)
CR_CMD/CLE	26	(IPU-ENET)
CR_CLK/RY_BY*	21	
CR_DATA0	25	(IPU-ENET)
CR_DATA1	24	
CR_DATA2	23	
CR_DATA3	22	
CR_DATA4	52	
CR_DATA5	53	
CR_DATA6	54	
CR_DATA7	55	
CE*/MS_INS*	59	(IPU-ENET)
CR_LED/ALE	60	(IPU-ENET)
CR_WP*/XD_WP*	57	(IPU-ENET)
XD_DETECT	68	(NO IPU OR IPD-ENET)

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

PCIE_ENET_D2R_N — C3950 0.1UF 10% 16V X5R-CERM 0201
PCIE_ENET_D2R_P — C3951 0.1UF 10% 16V X5R-CERM 0201
PCIE_ENET_R2D_C_P — C3955 0.1UF 10% 16V X5R-CERM 0201
PCIE_ENET_R2D_C_N — C3956 0.1UF 10% 16V X5R-CERM 0201
=ENET_WAKE_L (See note)

WAKE#
Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT
PCIE_ENET_D2R_C_N
PCIE_ENET_D2R_C_P
PCIE_ENET_R2D_P
PCIE_ENET_R2D_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
ENET_RESET_L
ENET_CLKREQ_L_O
ENET_LOW_PWR
SMB_ENET_SCL
SMB_ENET_SDA
ENET_SCLK
ENET_MISO
ENET_MOSI
ENET_CS_L
TP_ENET_CR_3V3_EN_L
ENET_TRAFFICLED_L
SYSCLK_CLK25M_ENET
ENET_RDAC — R3965 1.24K 1% 1/16W MF-LF 402

ENETCONN_MDI_P<0>
ENETCONN_MDI_N<0>
ENETCONN_MDI_P<1>
ENETCONN_MDI_N<1>
ENETCONN_MDI_P<2>
ENETCONN_MDI_N<2>
ENETCONN_MDI_P<3>
ENETCONN_MDI_N<3>

TP_ENET_CR_1V8_EN
PP3V3R1V8_ENET_LR_OUT_REG — MIN LINE WIDTH=0.3 mm, MIN NECK WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE — =PP3V3R1V8_CR_IOPWR_OUT
ENET_MEDIA_SENSE
ENET_SD_DETECT_L

ENET_SD_CMD — R3961 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.26:5MM — SDCONN_CMD
ENET_SD_CLK — R3979 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.21:5MM — SDCONN_CLK
ENET_CR_DATA<0> — R3971 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.25:5MM — SDCONN_DATA<0>
ENET_CR_DATA<1> — R3972 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.24:5MM — SDCONN_DATA<1>
ENET_CR_DATA<2> — R3973 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.23:5MM — SDCONN_DATA<2>
ENET_CR_DATA<3> — R3974 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.22:5MM — SDCONN_DATA<3>
ENET_CR_DATA<4> — R3975 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.52:5MM — SDCONN_DATA<4>
ENET_CR_DATA<5> — R3976 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.53:5MM — SDCONN_DATA<5>
ENET_CR_DATA<6> — R3977 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.54:5MM — SDCONN_DATA<6>
ENET_CR_DATA<7> — R3978 33 5% 1/20W MF 201 — 2PLACE NEAR=U3900.55:5MM — SDCONN_DATA<7>
NC_ENET_CE_L_MS_INS_L — NO_TEST=TRUE
ENET_CR_PWREN
ENET_SR_DISABLE — R3981 1K 5% 1/16W MF-LF 402
SDCONN_WP

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET_CR Signals
BCM requests SD CR[0:7], CMD, CLK termination.

ENET_SR_DISABLE
IF ENET SWITCHING REGULATOR IS USED, THIS PIN SHOULD HAVE A 1K PD TO GND

ENET supports both active-levels for WP.

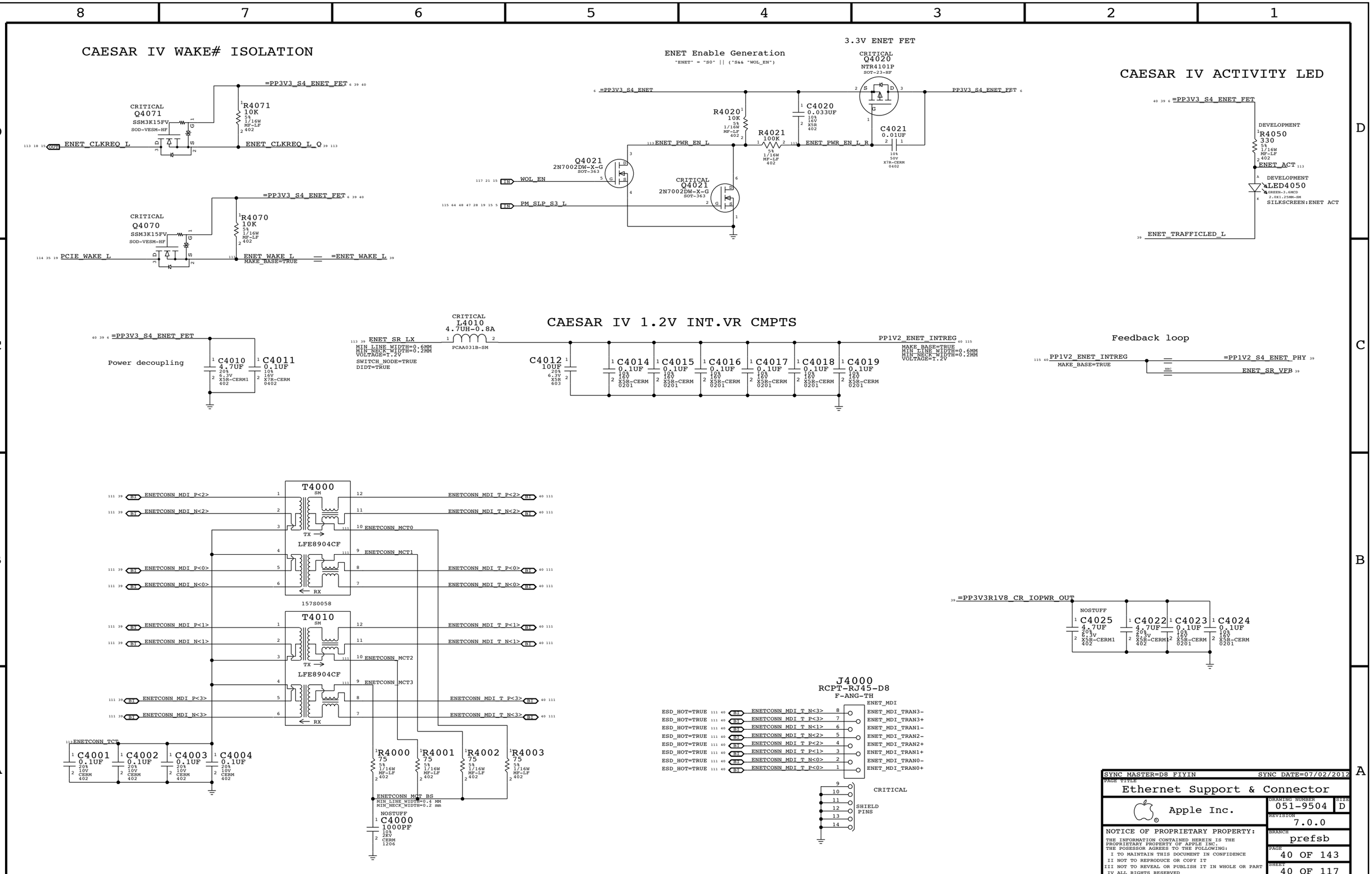
PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

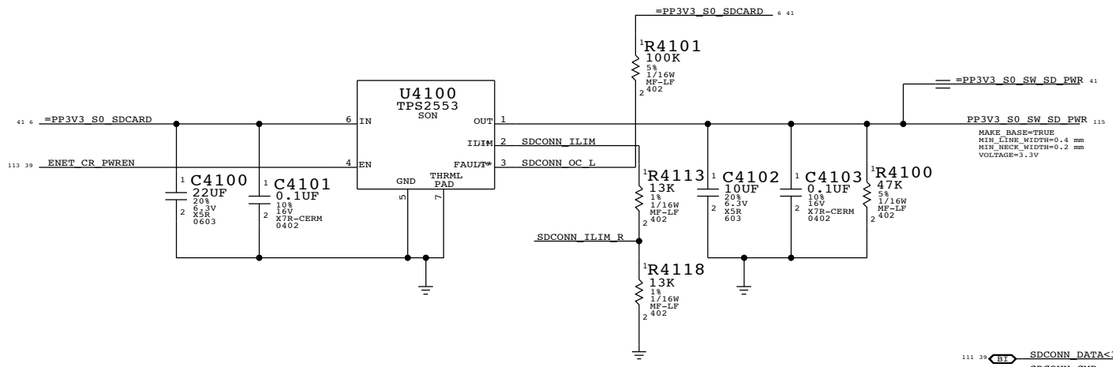
=PP3V3_S4_ENET_FET
C3990 0.1UF 10% 16V X5R-CERM 0201
U3990 AT45DB011D SOIC-8S1 OMIT_TABLE
VCC, SCK, CS*, WP*, RESET*, SI, SO, GND
ENET_SCLK
ENET_CS_L
ENET_MOSI
ENET_MISO
NOSTUFF R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

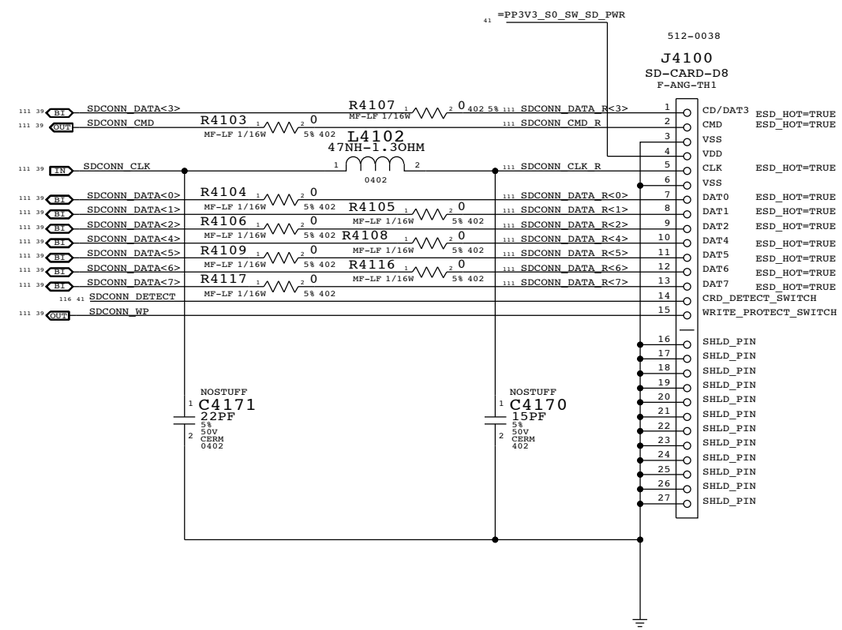
NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC MASTER=D8 FIYIN — SYNC DATE=07/02/2012
PAGE TITLE: ETHERNET PHY (CAESAR IV+)
Apple Inc.
DRAWING NUMBER 051-9504 — SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 39 OF 143
SHEET 39 OF 117

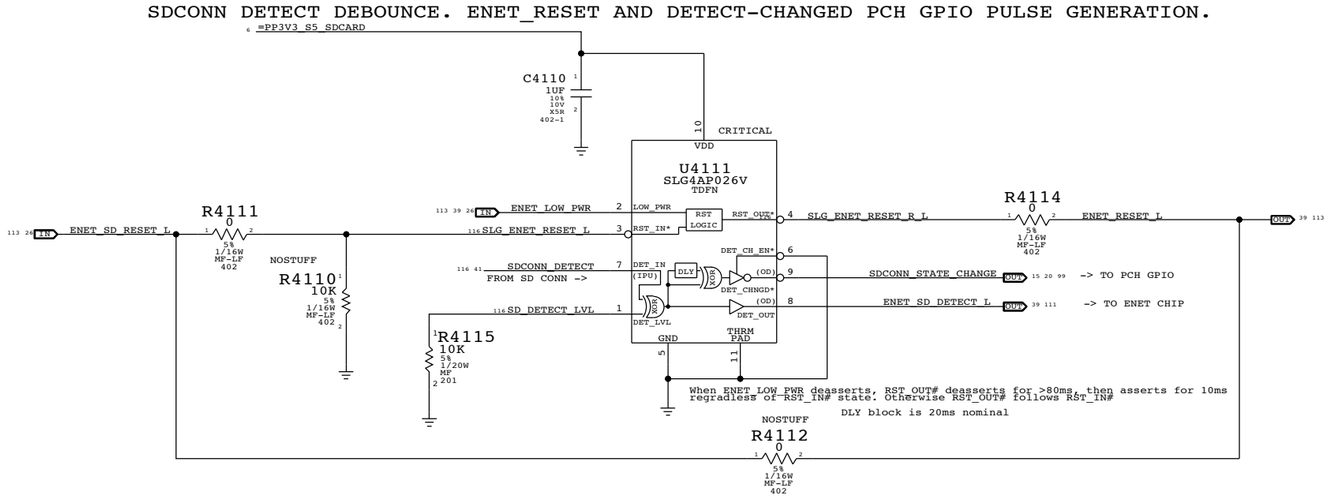


SD CARD 3.3V OVERCURRENT PROTECTION





SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SYNC MASTER=D8 FIYIN SYNC DATE=07/02/2012

PAGE TITLE
SD READER CONNECTOR

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

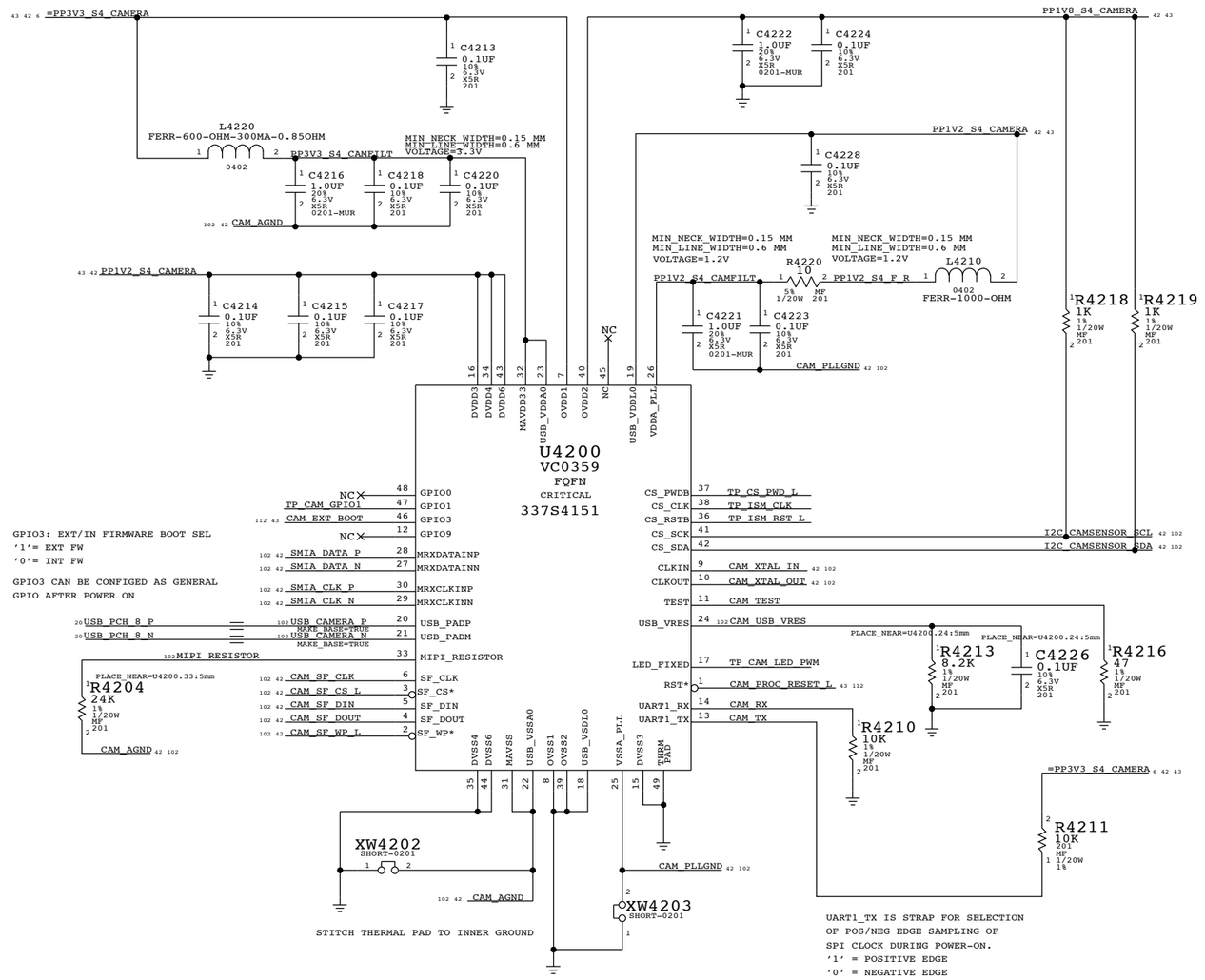
REVISION 7.0.0

BRANCH prefsb

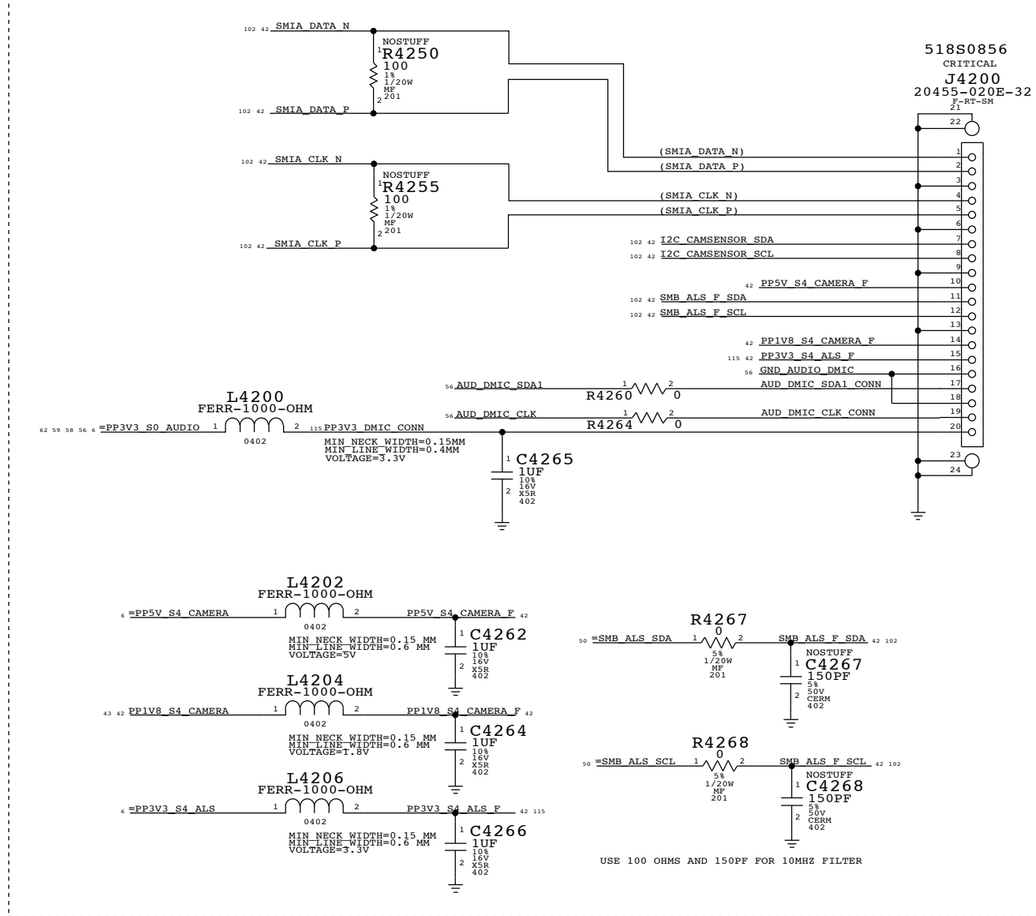
PAGE 41 OF 143

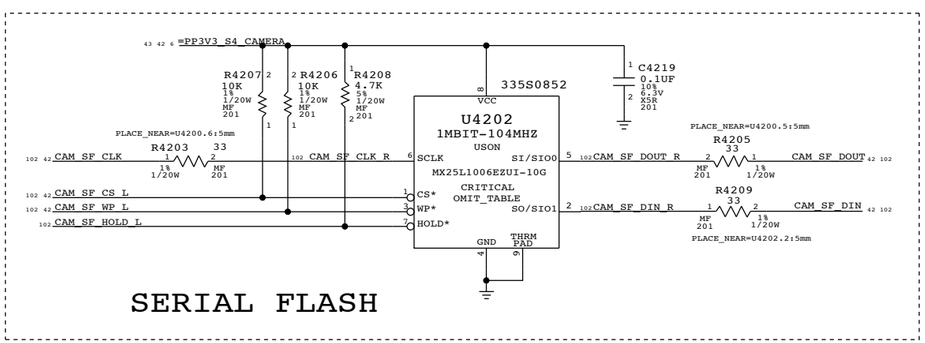
SHEET 41 OF 117

USB CAMERA CONTROLLER

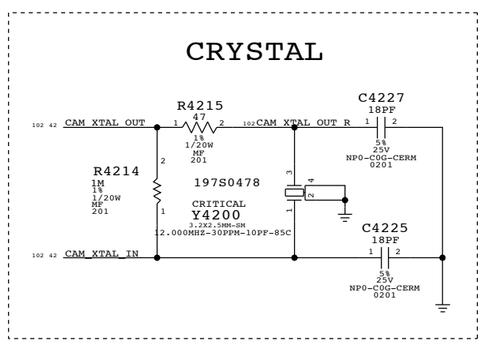


CAMERA/ALS/DMIC CONNECTOR





SERIAL FLASH



SYNC MASTER=D8 ROSITA SYNC DATE=03/23/2012

PAGE TITLE: Camera Controller

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

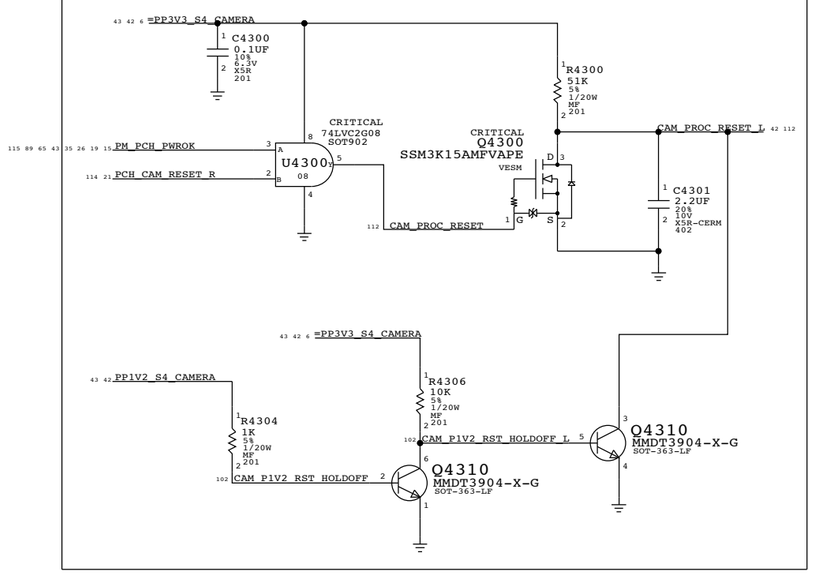
REVISION: 7.0.0

BRANCH: prefsb

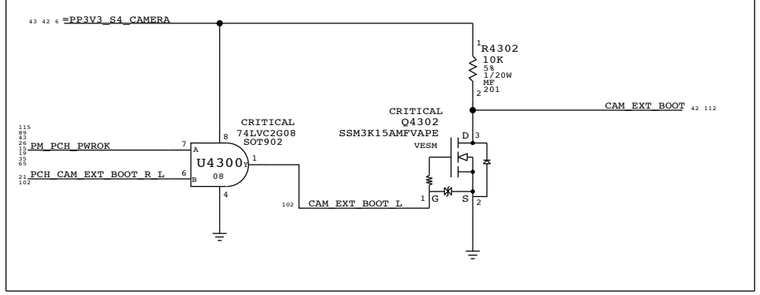
PAGE: 42 OF 143

SHEET: 42 OF 117

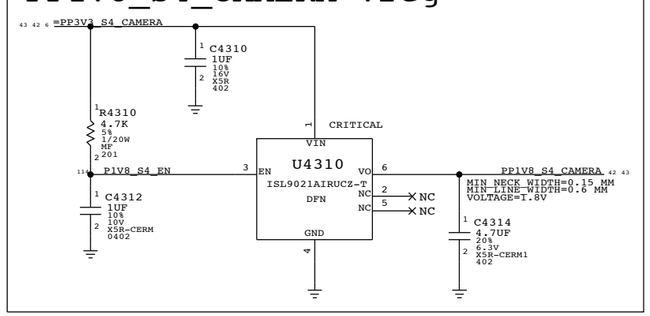
Camera Processor Reset



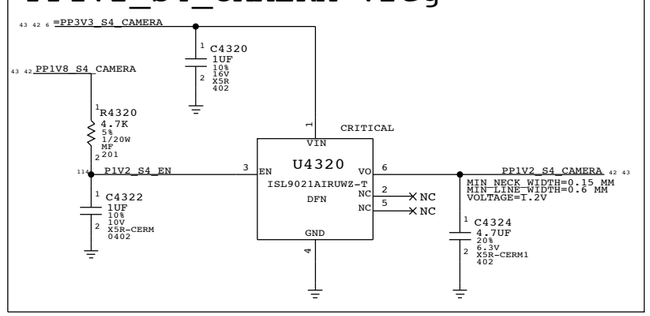
Camera Processor ExtBoot Cntl



PP1V8_S4_CAMERA Vreg



PP1V2_S4_CAMERA Vreg

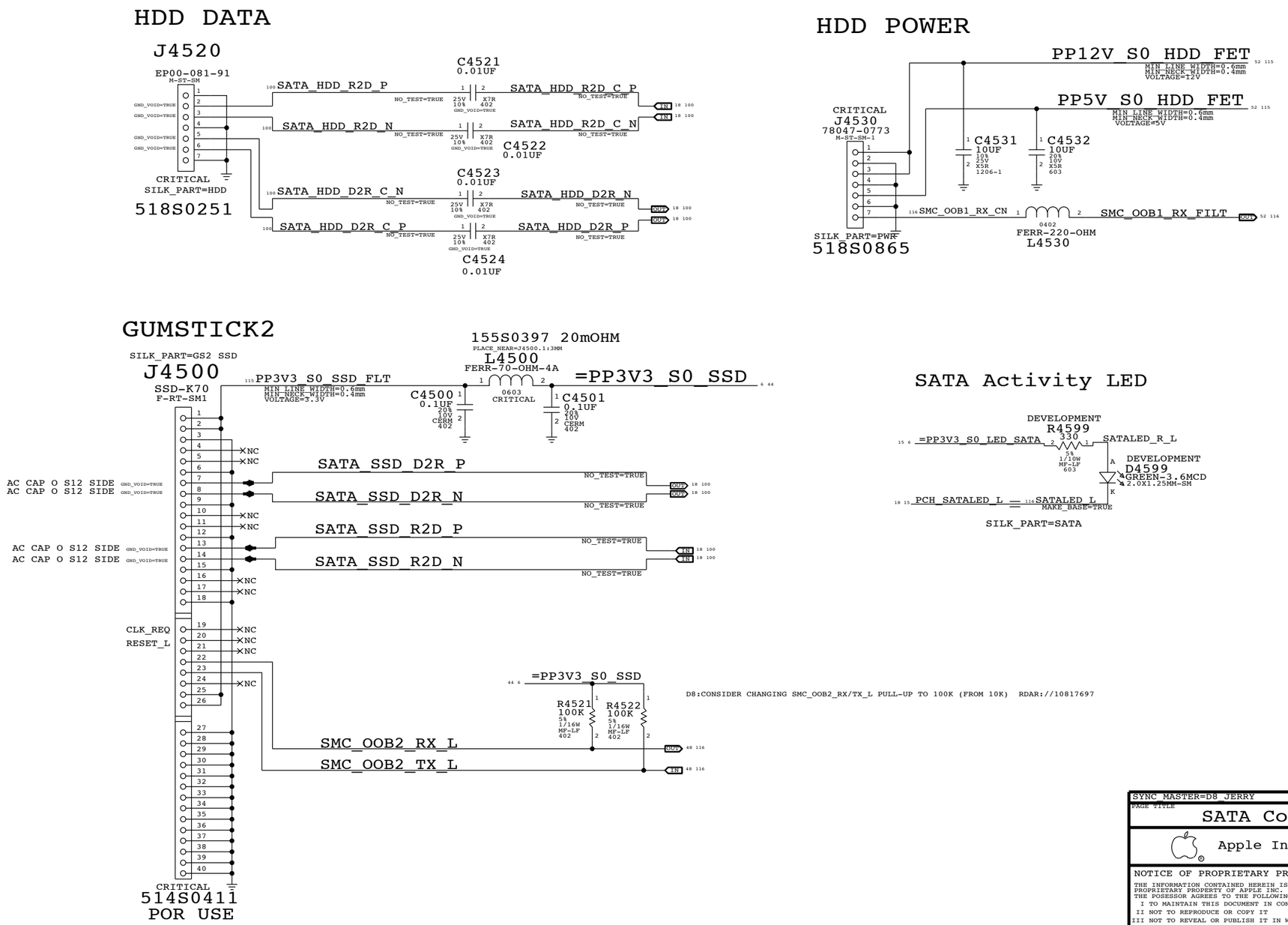


SYNC MASTER=D7_MLB SYNC DATE=03/15/2012

PAGE TITLE
Camera Controller Support

Apple Inc.

DRAWING NUMBER	051-9504
SIZE	D
REVISION	7.0.0
BRANCH	prefsb
PAGE	43 OF 143
SHEET	43 OF 117



SYNC MASTER=D8_JERRY SYNC DATE=01/31/2012

PAGE TITLE
SATA Connectors

Apple Inc.

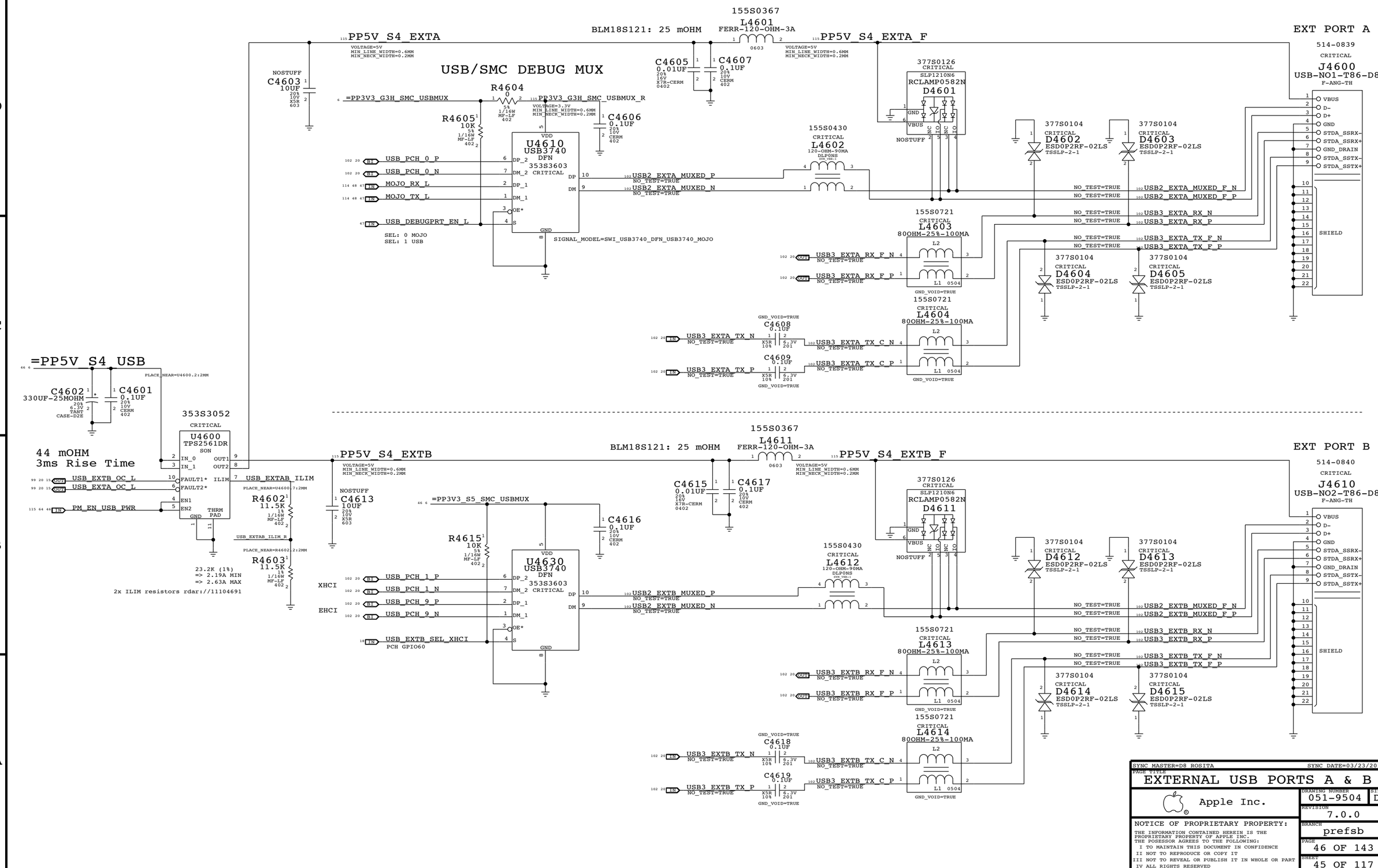
DRAWING NUMBER 051-9504 SIZE D

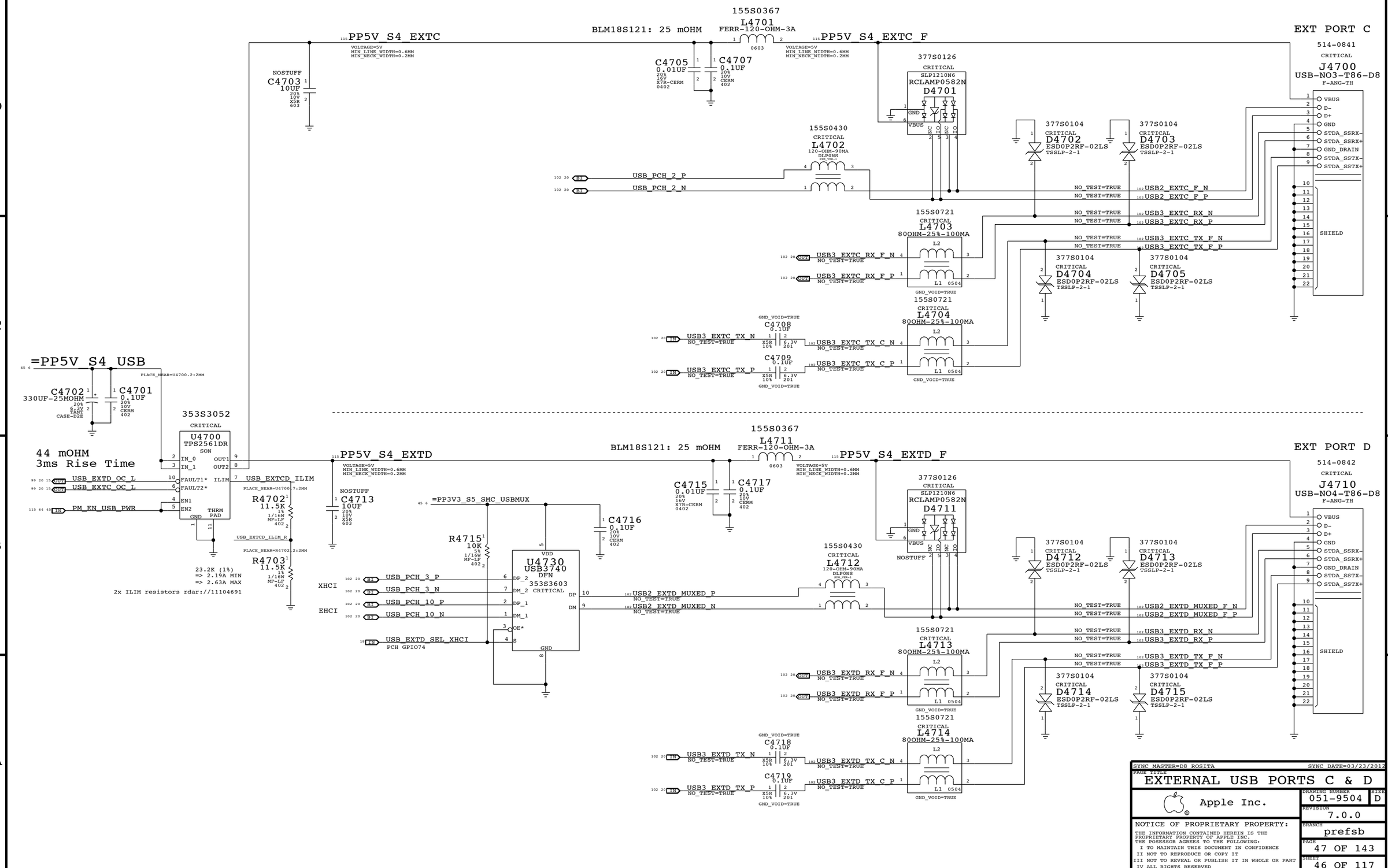
REVISION 7.0.0

BRANCH prefsb

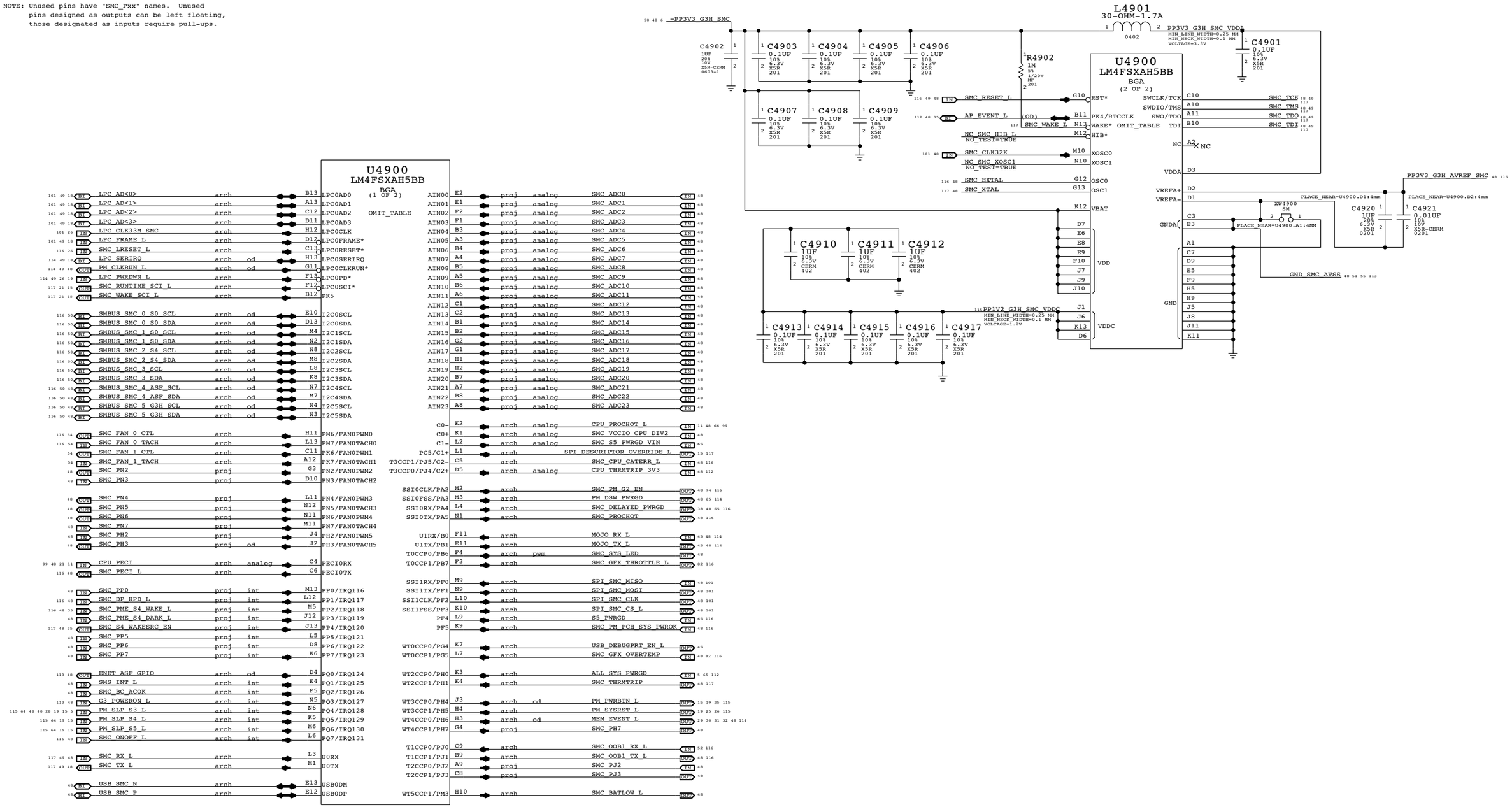
PAGE 45 OF 143

SHEET 44 OF 117





NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



SYNC MASTER=D8 MARK SYNC DATE=03/22/2012

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

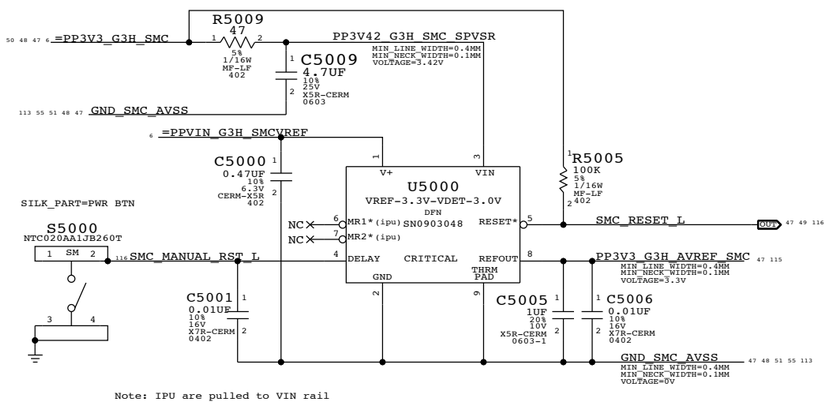
BRANCH: prefsb

PAGE: 49 OF 143

SHEET: 47 OF 117

SMC Supervisor and AVREF Supply

rdar://11180279 SMC_RESET_L workaround



Note: IPU are pulled to VIN rail

ADC Channel Aliases

SMC_ADC0	SMCVSNS_P12VG3H	MAKE_BASE=TRUE	
SMC_ADC1	SMCVSNS_P12VG3H	MAKE_BASE=TRUE	
SMC_ADC2	SMCVSNS_GPUCORE	MAKE_BASE=TRUE	
SMC_ADC3	SMCISNS_GPUCORE	MAKE_BASE=TRUE	
SMC_ADC4	SMCVSNS_P1V5S0_CPU_MEM	MAKE_BASE=TRUE	
SMC_ADC5	SMCISNS_P1V5S0_CPU_MEM	MAKE_BASE=TRUE	
SMC_ADC6	SMCVSNS_PVDDQS3_DDR	MAKE_BASE=TRUE	
SMC_ADC7	SMCISNS_PVDDQS3_DDR	MAKE_BASE=TRUE	
SMC_ADC8	SMCISNS_P12VS0_P1V05	MAKE_BASE=TRUE	
SMC_ADC9	SMCISNS_P12VS0_FBVDDQ	MAKE_BASE=TRUE	
SMC_ADC10	SMCVSNS_CPUCORE	MAKE_BASE=TRUE	
SMC_ADC11	SMCISNS_CPUCORE	MAKE_BASE=TRUE	
SMC_ADC12	SMCVSNS_CPUAXG	MAKE_BASE=TRUE	
SMC_ADC13	SMCISNS_CPUAXG	MAKE_BASE=TRUE	
SMC_ADC14	SMCVSNS_P5VS0_HDD	MAKE_BASE=TRUE	
SMC_ADC15	SMCISNS_P5VS0_HDD	MAKE_BASE=TRUE	
SMC_ADC16	SMCVSNS_P1V05S0_PCH	MAKE_BASE=TRUE	
SMC_ADC17	SMCISNS_P1V05S0_PCH	MAKE_BASE=TRUE	
SMC_ADC18	SMCISNS_P12VS0_HDD	MAKE_BASE=TRUE	
SMC_ADC19	SMCISNS_P3V3S4_AP	MAKE_BASE=TRUE	
SMC_ADC20	SMCVSNS_P3V3S0	MAKE_BASE=TRUE	
SMC_ADC21	SMCISNS_P3V3S0_SSD	MAKE_BASE=TRUE	
SMC_ADC22	SMCISNS_P12VS0_CPU_VCCSA	MAKE_BASE=TRUE	
SMC_ADC23	SMCISNS_P12VS0_CPU_P1V05	MAKE_BASE=TRUE	

Project-specific Aliases

SMC_PH3	BDV_BKL_PWM	MAKE_BASE=TRUE	
SMC_PN5	ACDC_BURST_EN_L	MAKE_BASE=TRUE	
SMC_PJ3	SMC_OOB2_TX_L	MAKE_BASE=TRUE	
SMC_PJ2	SMC_OOB2_RX_L	MAKE_BASE=TRUE	
SMC_PP0	SMC_ACDC_ID	MAKE_BASE=TRUE	
SMC_PH2	SMC_ASSERT_RTCRST	MAKE_BASE=TRUE	
SMC_PN4	SMC_BLC_FAULT	MAKE_BASE=TRUE	

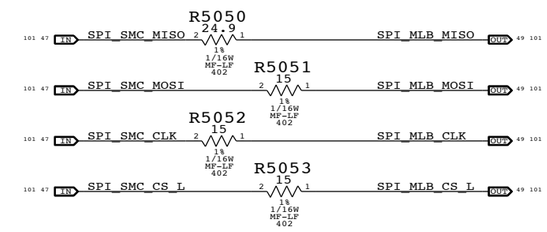
Unused Project-specific

radar://11033060 Remove USB hookup from SMC (not needed)

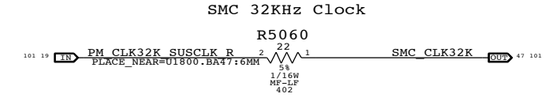
USB_SMC_P	NC_USB_SMC_P	MAKE_BASE=TRUE	NO_TEST=TRUE
USB_SMC_N	NC_USB_SMC_N	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN2	NC_SMC_PN2	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN3	NC_SMC_PN3	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN6	NC_SMC_PN6	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PN7	NC_SMC_PN7	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP5	NC_SMC_PP5	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP6	NC_SMC_PP6	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PP7	NC_SMC_PP7	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PME_S4_DARK_L	NC_SMC_PME_S4_DARK_L	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_PH7	TP_SMC_PH7	MAKE_BASE=TRUE	
TP for access if ZPB re-instated			
SMBUS_SMC_4_ASF_SCL	NC_SMBUS_SMC_4_ASF_SCL	MAKE_BASE=TRUE	NO_TEST=TRUE
SMBUS_SMC_4_ASF_SDA	NC_SMBUS_SMC_4_ASF_SDA	MAKE_BASE=TRUE	NO_TEST=TRUE
SMBUS_SMC_5_G3H_SCL	NC_SMBUS_SMC_5_G3H_SCL	MAKE_BASE=TRUE	NO_TEST=TRUE
SMBUS_SMC_5_G3H_SDA	NC_SMBUS_SMC_5_G3H_SDA	MAKE_BASE=TRUE	NO_TEST=TRUE
SMC_OOB1_TX_L	NC_SMB_OOB1_TX_L	MAKE_BASE=TRUE	NO_TEST=TRUE

SMC SPI Support

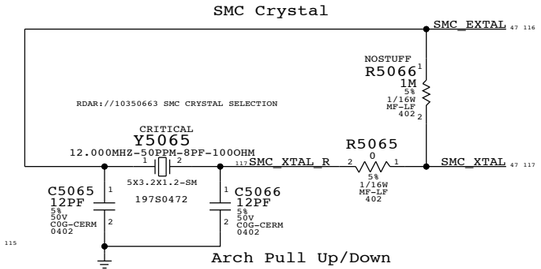
RDAR://11158919 D8:DETERMINE VALUE AND STUFF SERIES R FOR SPI BUS



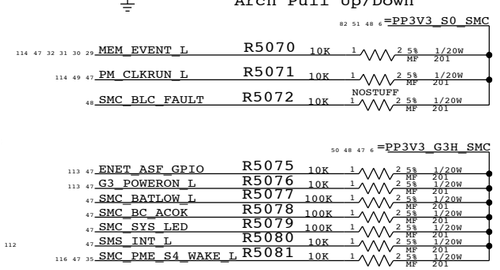
SMC 32KHz Clock



SMC Crystal

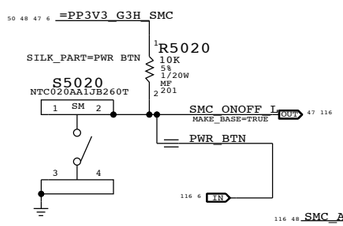


Arch Pull Up/Down

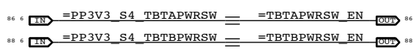


Note:
Pull-down needed for SMC SSI signals

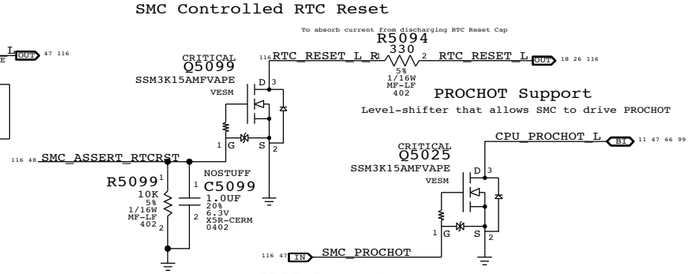
Power Button



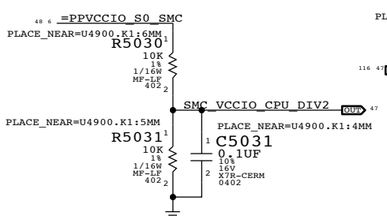
Enable S4 Wake Sources



SMC Controlled RTC Reset



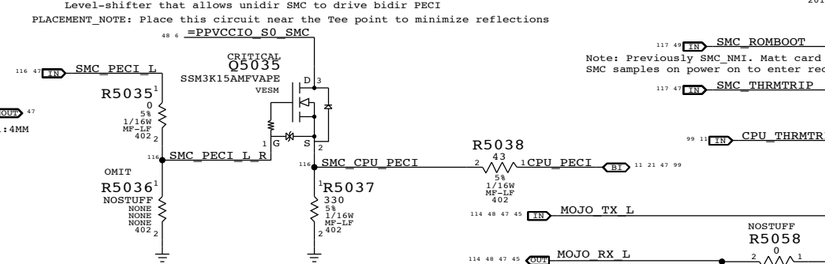
Comparator VCCIO Reference



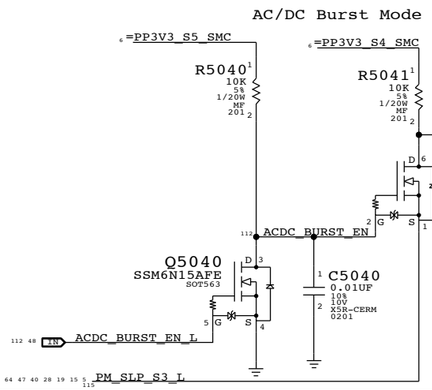
PECI Support

Level-shifter that allows unidir SMC to drive bidir PECI

PLACEMENT_NOTE: Place this circuit near the Tee point to minimize reflections



AC/DC Burst Mode Enable



Note:
Open-drain stage on S4 to account case when SMC is initializing in S5, and chip is not yet configured. and ACDC_BURST_EN_L could be floating.

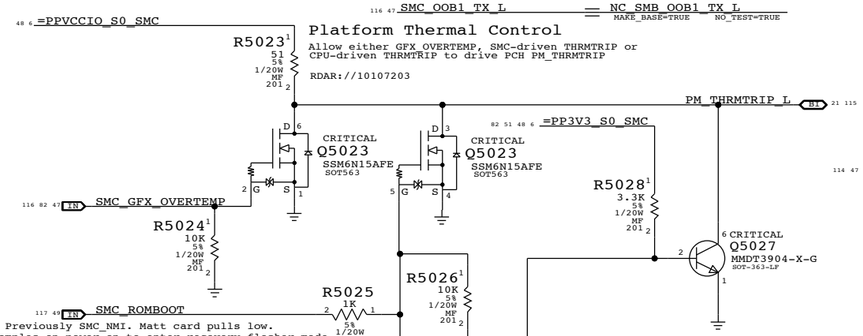
SMC to monitor 12V G3H power in S3 If power high (i.e. charging iPad) enable BURSTMODE to avoid the AC/DC from oscillating in and out.

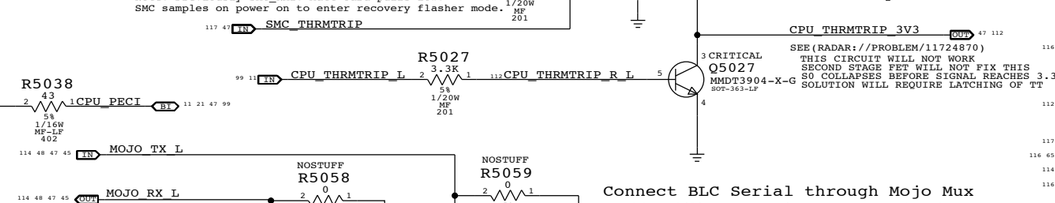
rdar://10506970
rdar://10196882

Platform Thermal Control

Allow either GFX_OVERTEMP, SMC-driven THRMTRIP or CPU-driven THRMTRIP to drive PCH PM_THRMTRIP

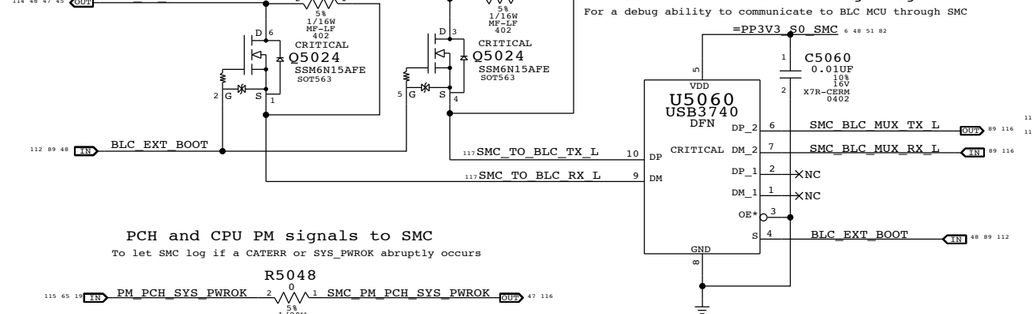
RDAR://10107203





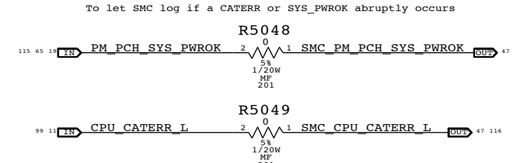
Connect BLC Serial through Mojo Mux

For a debug ability to communicate to BLC MCU through SMC



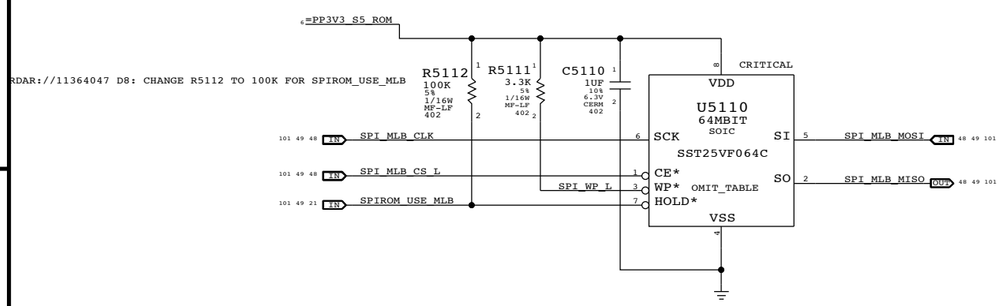
PCH and CPU PM signals to SMC

To let SMC log if a CATERR or SYS_PWROK abruptly occurs

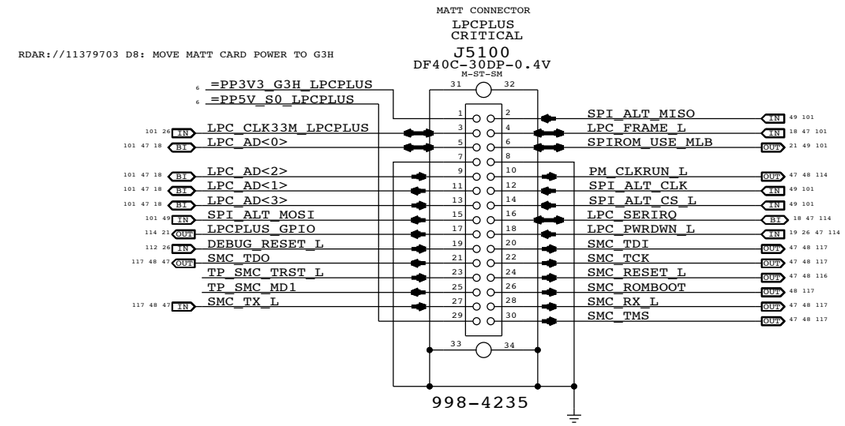


SYNC MASTER=D8 DOUG	SYNC DATE=07/19/2012
PAGE TITLE	SMC Support
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
	PAGE 50 OF 143
	SHEET 48 OF 117

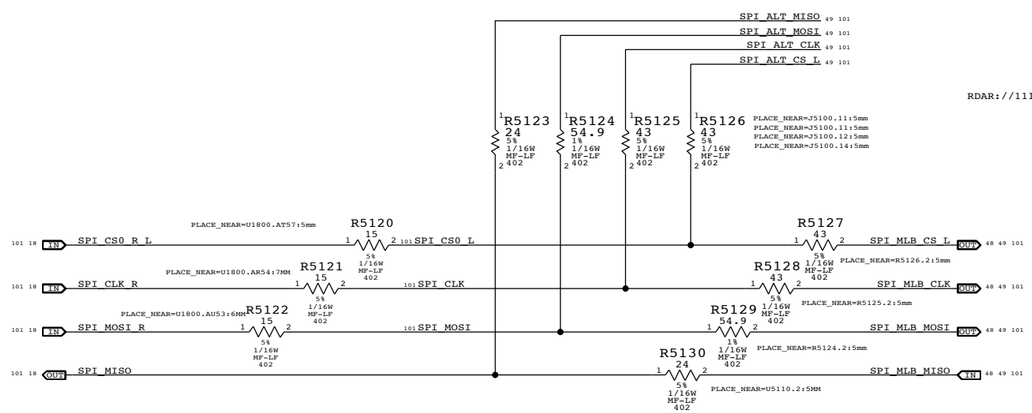
SPI BootROM



LPC+SPI Connector



SPI Series Termination



SYNC MASTER=D8 MLB SYNC DATE=N/A

PAGE TITLE
SPI and Debug Connector

Apple Inc.

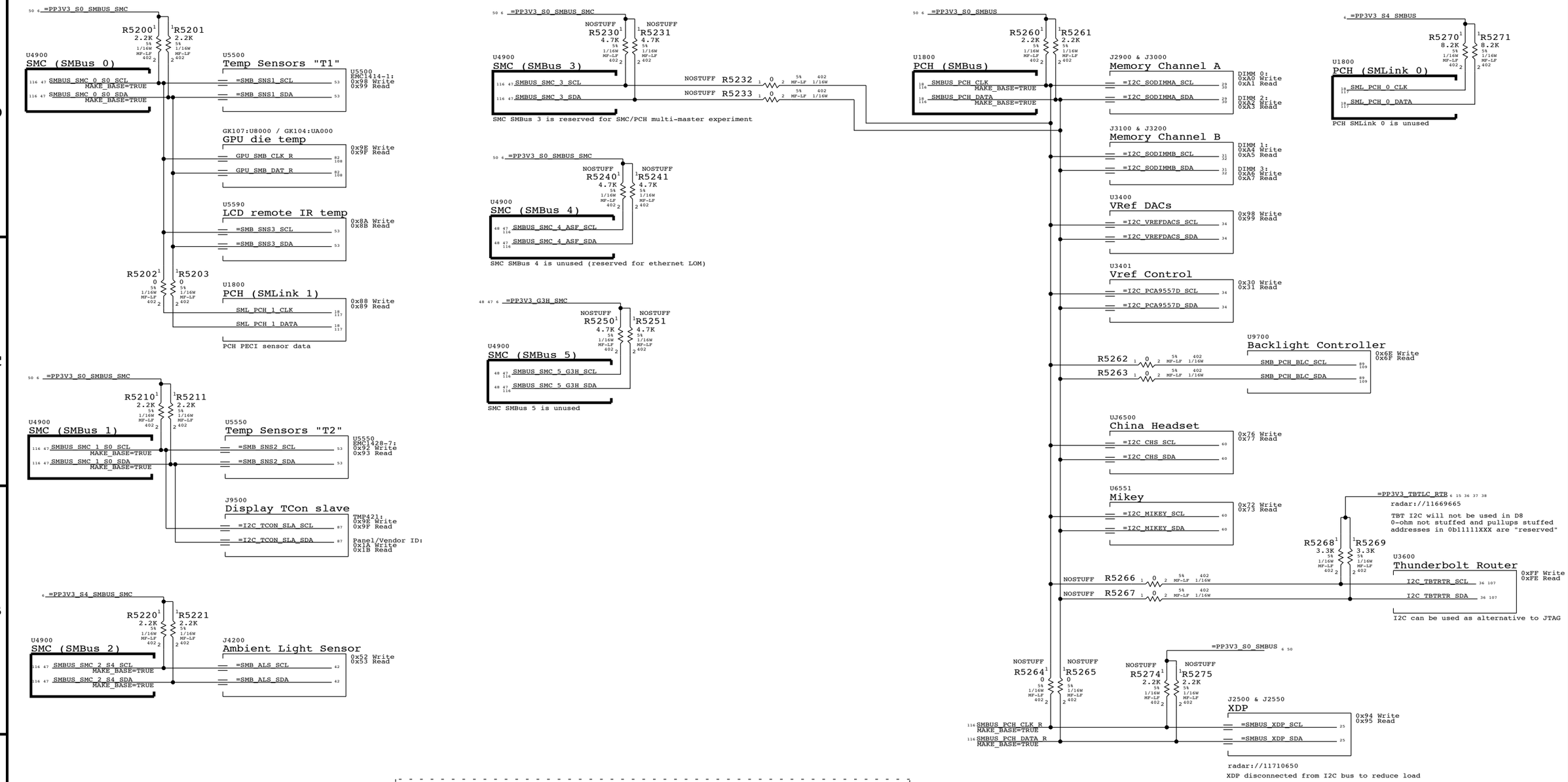
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 51 OF 143

SHEET 49 OF 117



SYNC MASTER=D8 TAVYS SYNC DATE=06/22/2012

PAGE TITLE

SMBus Connections

Apple Inc.

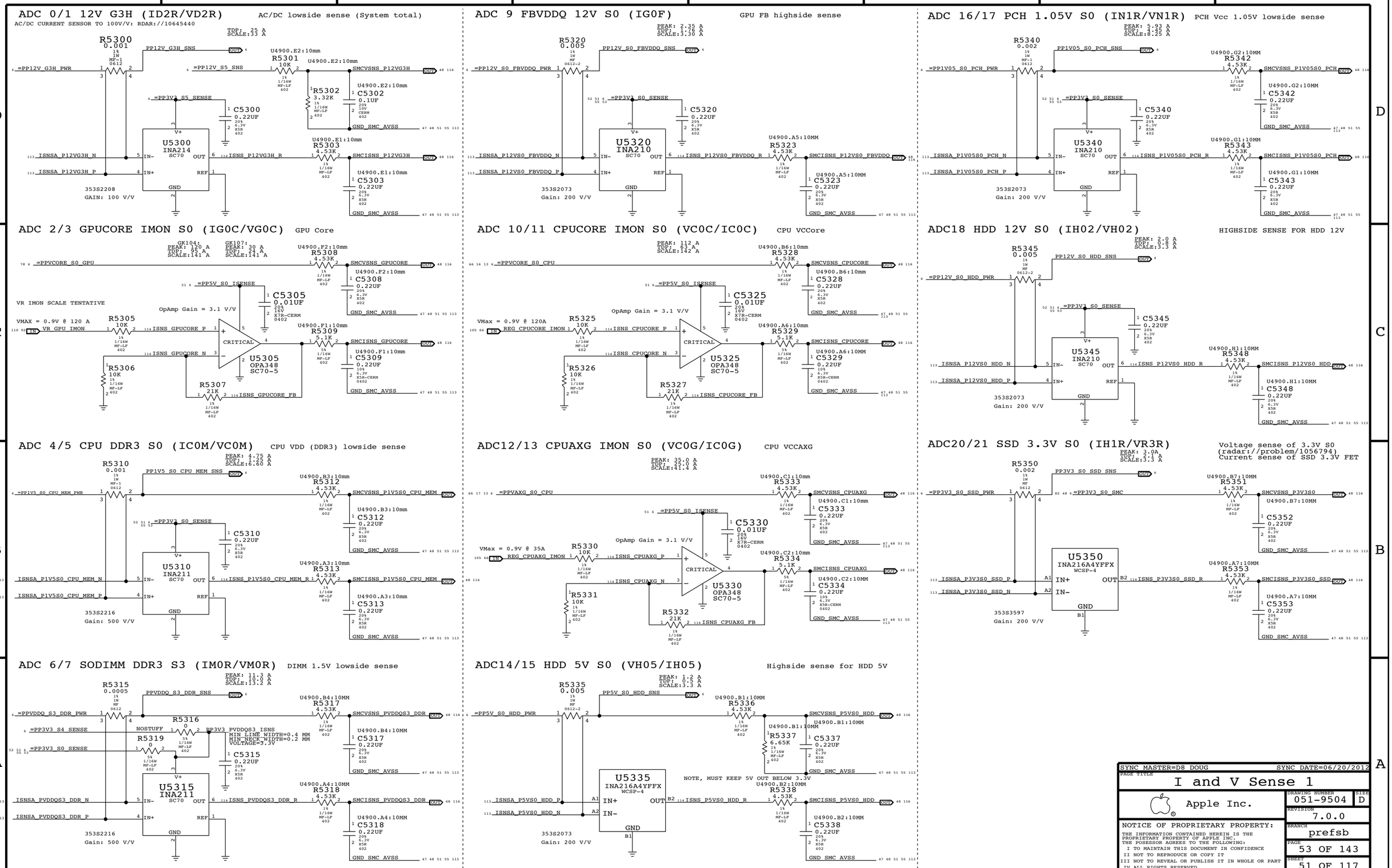
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

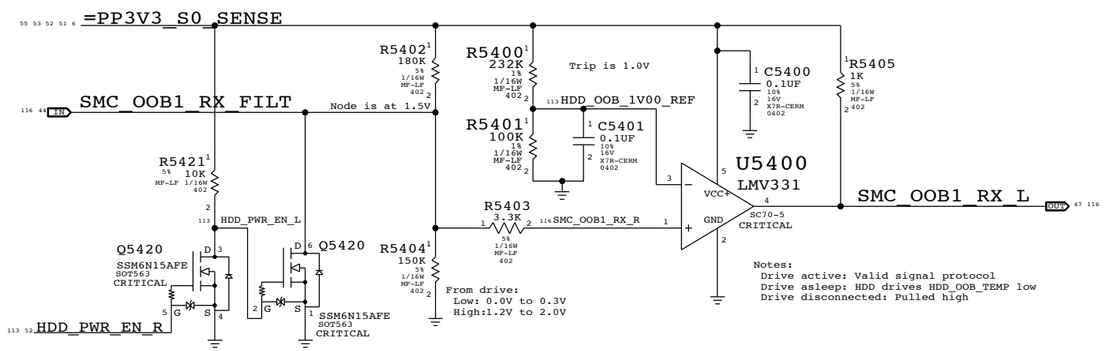
PAGE 52 OF 143

SHEET 50 OF 117

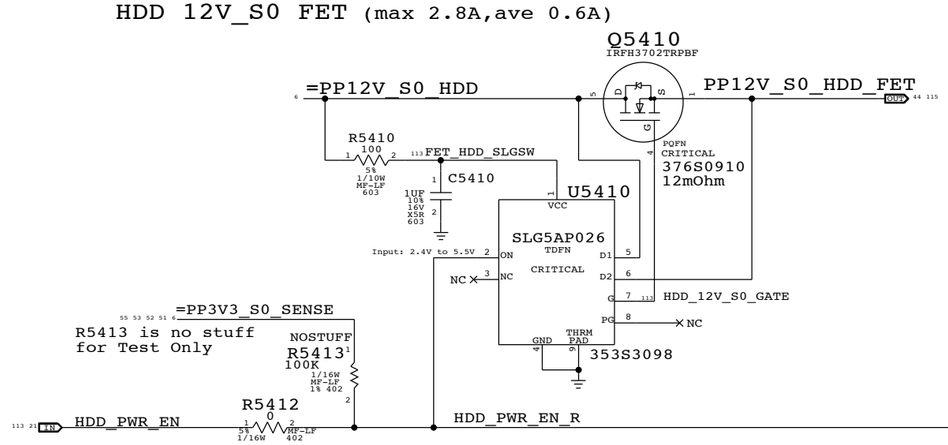


HDD Out-of-Band Temp Sensing

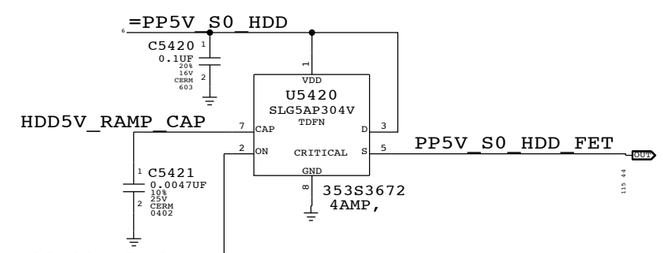
Temperature read from SATA power connecter pin 11



HDD 12V_S0 FET (max 2.8A,ave 0.6A)



HDD 5V_S0 FET (max 0.7A,ave 0.3A)



REMOVE R5413 AND SHORT R5412 AFTER HDD_PWR_EN WORKS

SYNC-MASTER=D8-JERRY- - - - - - - SYNC-DATE=02/25/2012

PAGE TITLE: HDD/SSD Temp Sense

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

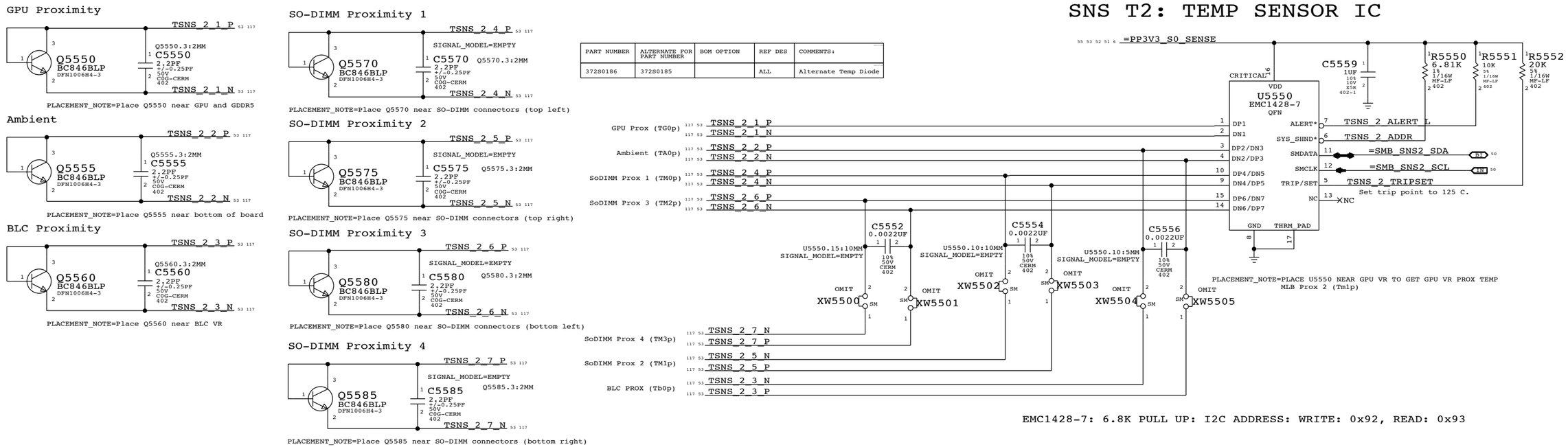
REVISION: 7.0.0

BRANCH: prefsb

PAGE: 54 OF 143

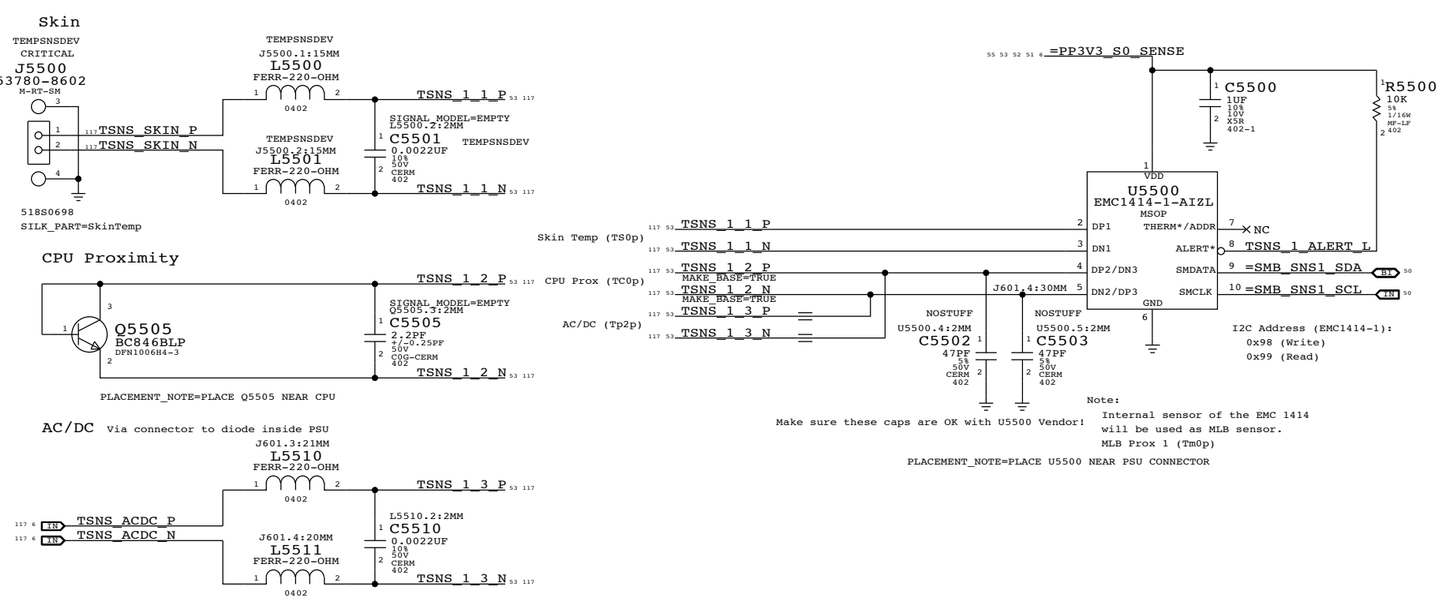
SHEET: 52 OF 117

Temperature Sensor T2 EMC1428: Near GPU VR

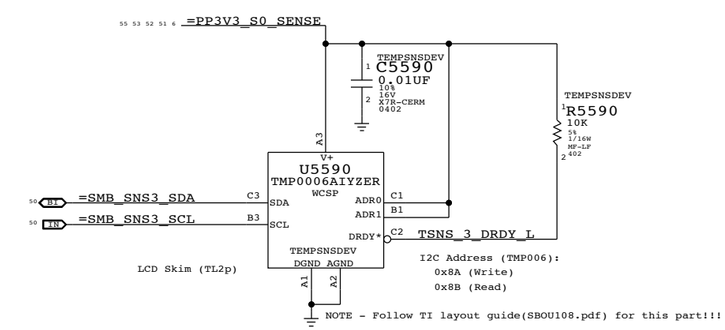


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
372S0186	372S0185		ALL	Alternate Temp Diode

Temperature Sensor T1 EMC1414: Near PSU Conn



Temperature Sensor T3: LCD Remote Sensor(Dev4Now)



SYNC MASTER=D8 DOUG SYNC DATE=06/07/2012

PAGE TITLE
Temperature Sensors

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 55 OF 143

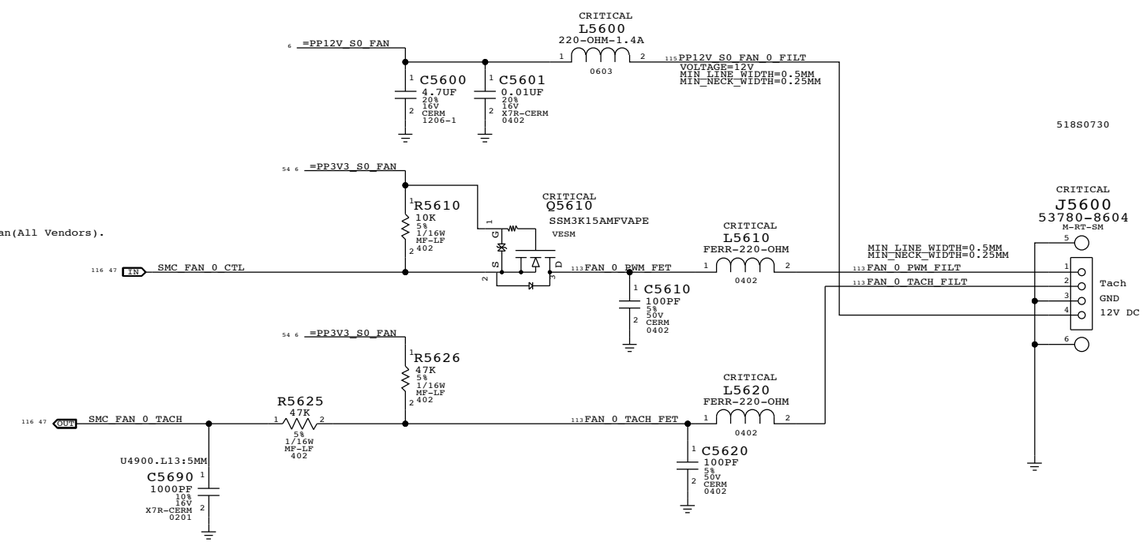
SHEET 53 OF 117

SMC Fan 0 (System)

Note:
The circuit for the PWM input to the fan acts as a non-inverting level-shifter to protect the SMC. It is assumed there is a pull-up to 5V/12V inside the fan, otherwise when the SMC PWM goes low and Q5610 turns on, there would be 5V/12V present on the SMC pin! Then by definition, the drain of Q5610 is at common and the SMC sinks current when Q5610 is on.

This resembles an open-drain if there is a pull-up, going to a Hi-Z FET input.

Otherwise, this is simply a pass-FET.
See RADAR: 10565825- D7: Need scematic and PCB file of fan(All Vendors).



SMC Fan 1 (Unused)

SYNC MASTER=D8 DOUG SYNC DATE=07/19/2012

PAGE TITLE
System Fan

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

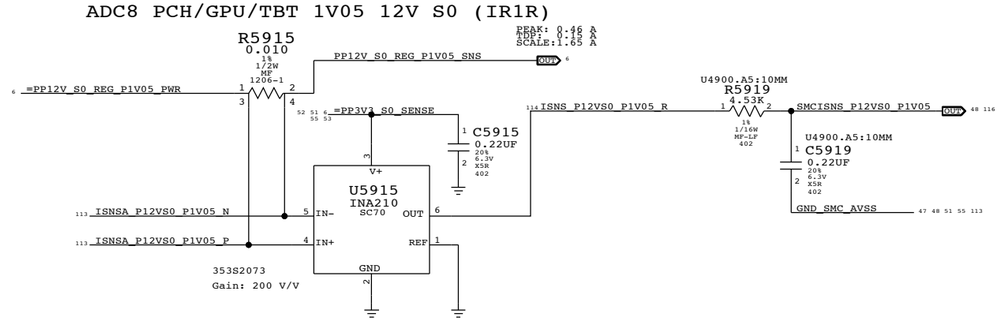
REVISION 7.0.0

BRANCH prefsb

PAGE 56 OF 143

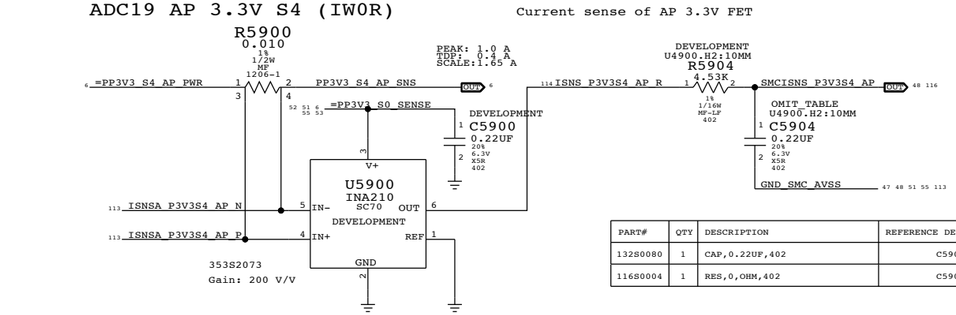
SHEET 54 OF 117

ADC8 PCH/GPU/TBT 1V05 12V S0 (IR1R)



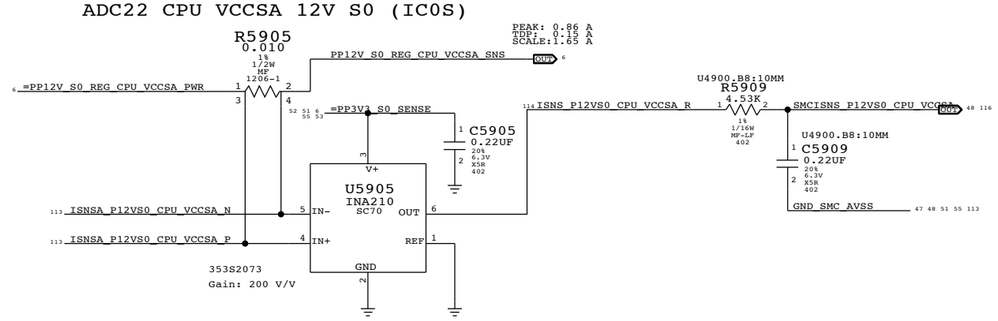
ADC19 AP 3.3V S4 (IW0R)

Current sense of AP 3.3V FET

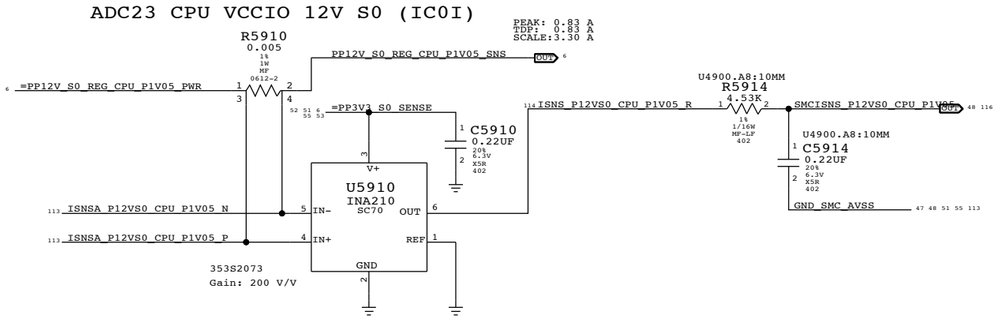


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0080	1	CAP,0.22UF,402	C5904	DEVELOPMENT
116S0004	1	RES,0,OHM,402	C5904	PRODUCTION

ADC22 CPU VCCSA 12V S0 (IC0S)



ADC23 CPU VCCIO 12V S0 (IC0I)



SYNC MASTER=D8 MARK SYNC DATE=04/23/2012

PAGE TITLE
I and V Sense 2

Apple Inc.

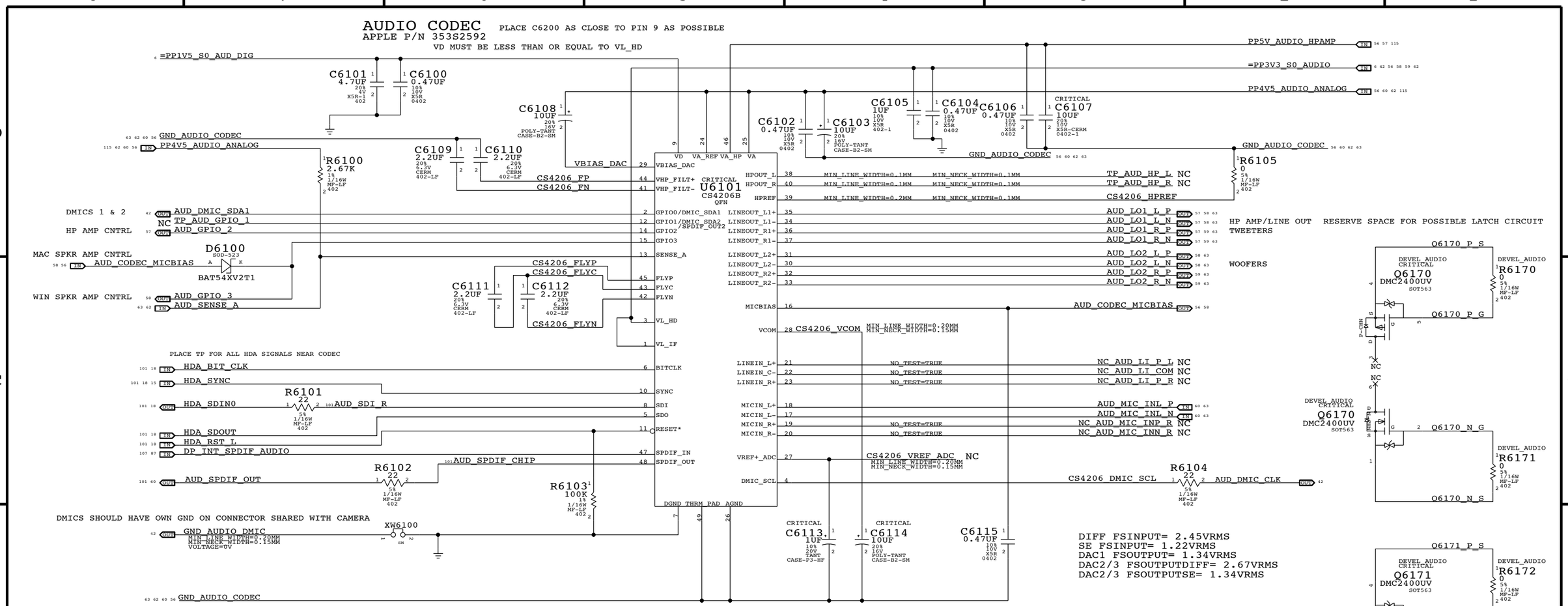
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 59 OF 143

SHEET 55 OF 117



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0134	127S0111		C6113	THAILAND ALTERNATE

SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE
AUDIO: CODEC/REGULATORS

Apple Inc.

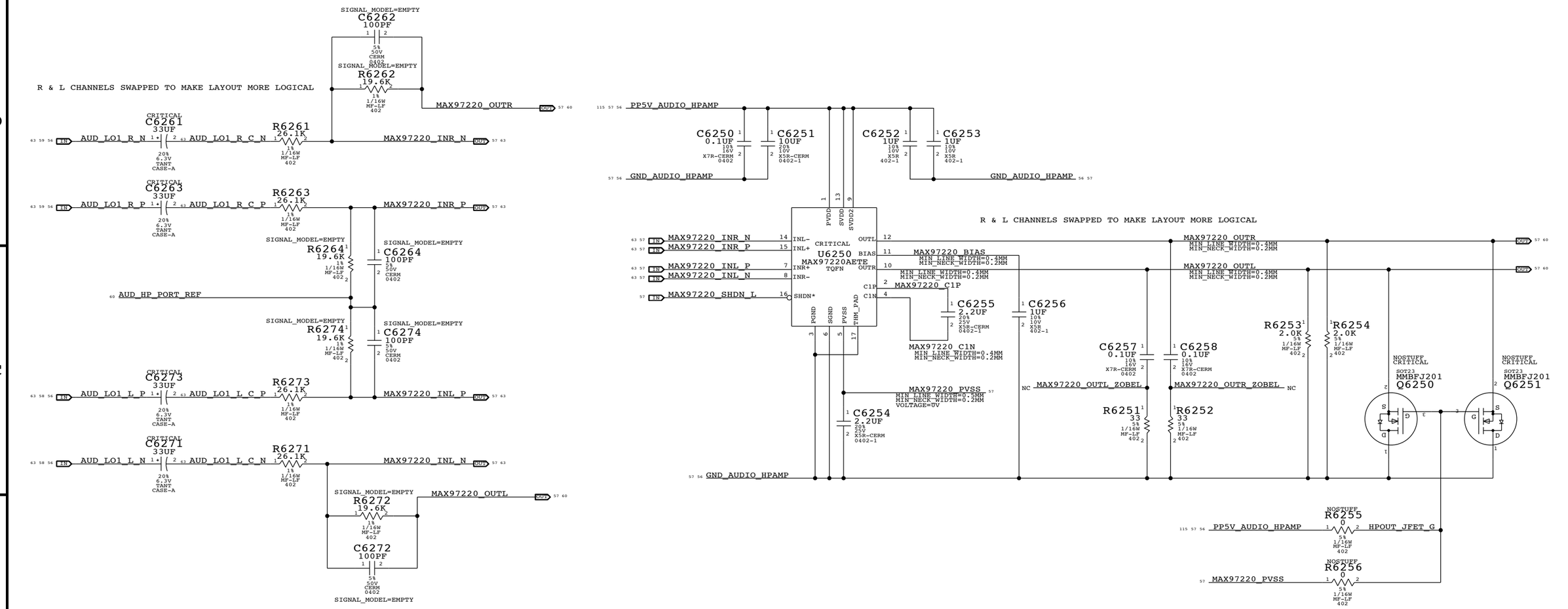
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 61 OF 143

SHEET 56 OF 117



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
127S0135	127S0120		C6261	THAILAND ALTERNATE
127S0135	127S0120		C6263	THAILAND ALTERNATE
127S0135	127S0120		C6271	THAILAND ALTERNATE
127S0135	127S0120		C6273	THAILAND ALTERNATE

SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE
AUDIO: HEADPHONE AMP

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

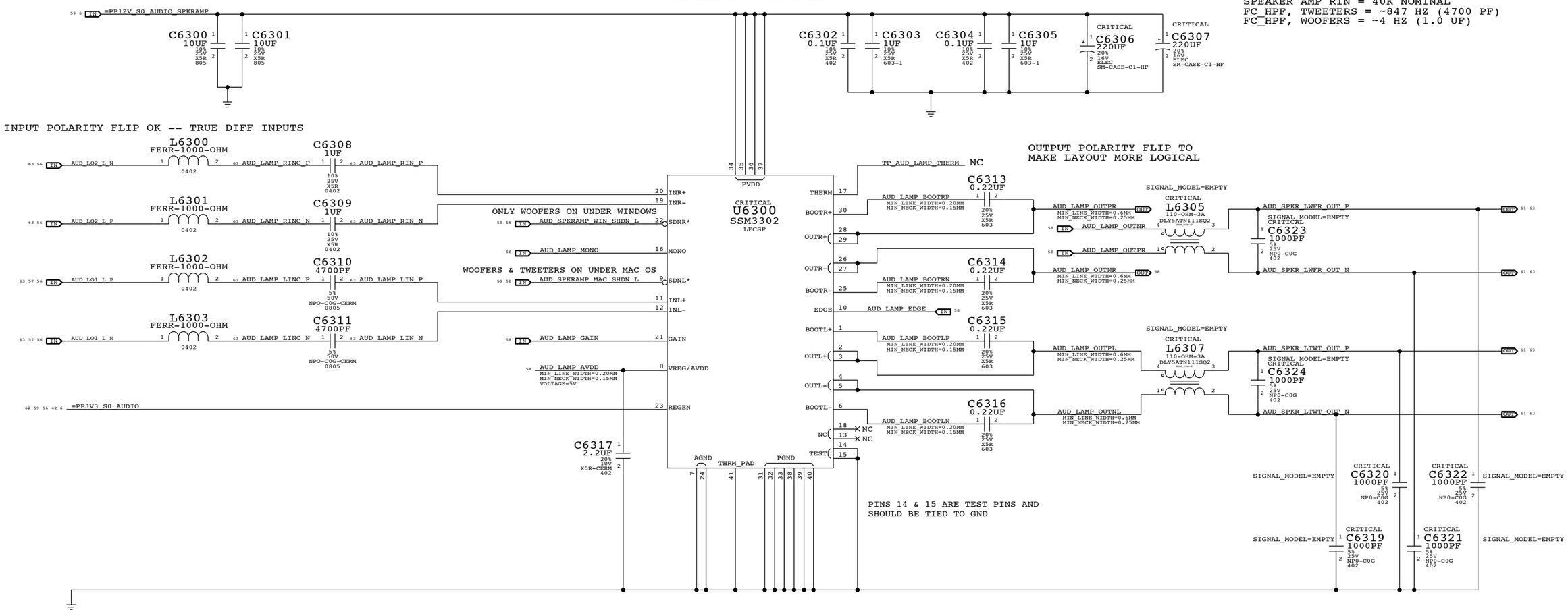
BRANCH prefsb

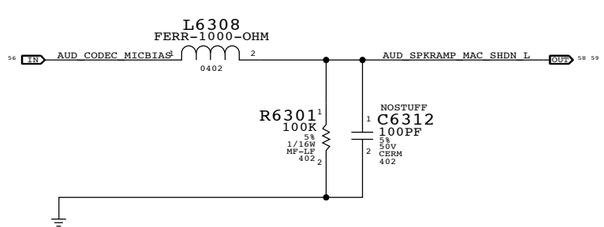
PAGE 62 OF 143

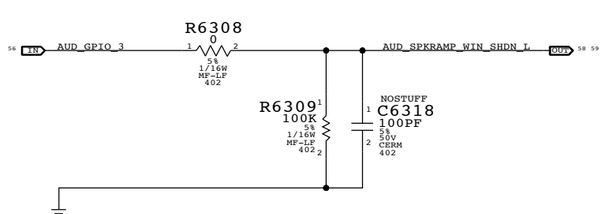
SHEET 57 OF 117

LEFT CH SPEAKER AMP
APPLE P/N 353S3163

SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)



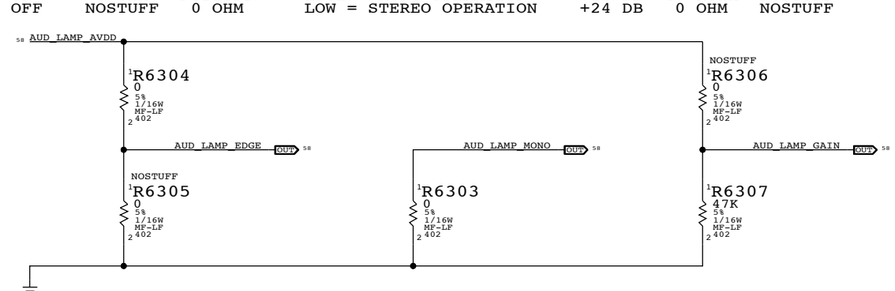




EDGE RATE CONTROL	R6304	R6305
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6306	R6307
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF



SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

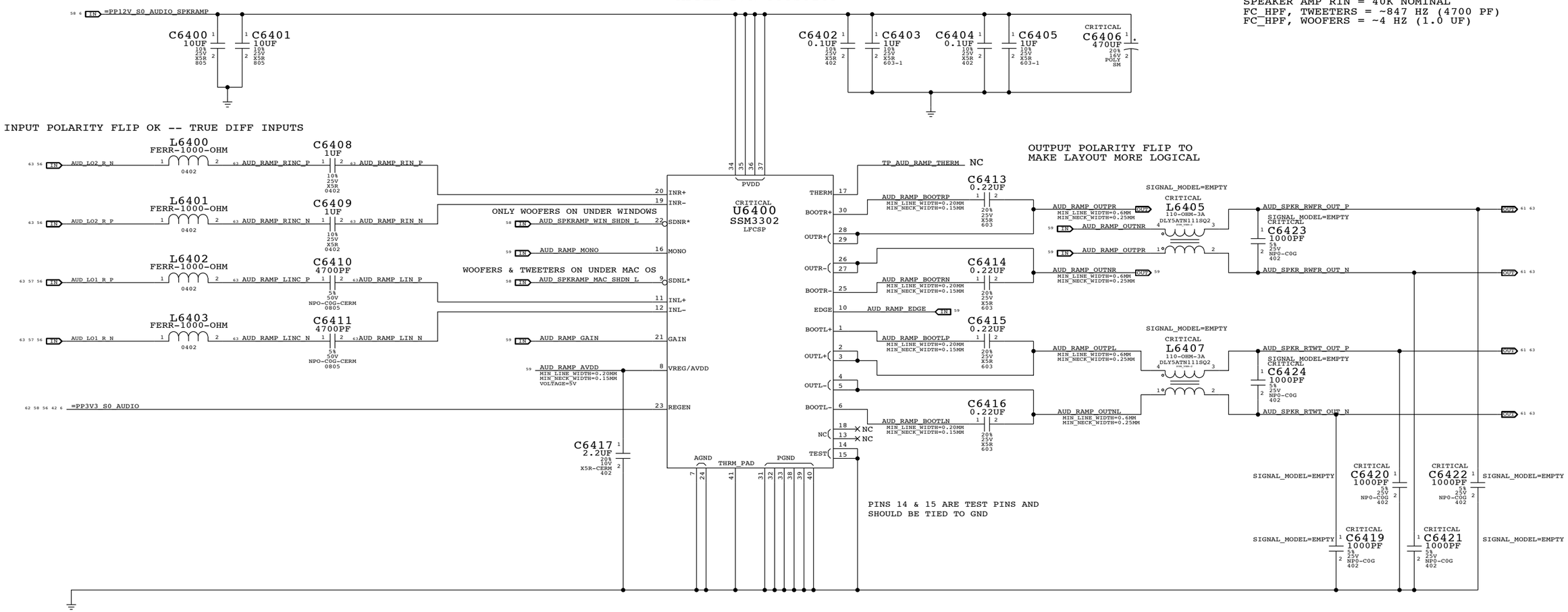
PAGE TITLE
AUDIO: LEFT SPKR AMP

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 63 OF 143
SHEET 58 OF 117

RIGHT CH SPEAKER AMP
APPLE P/N 353S3163

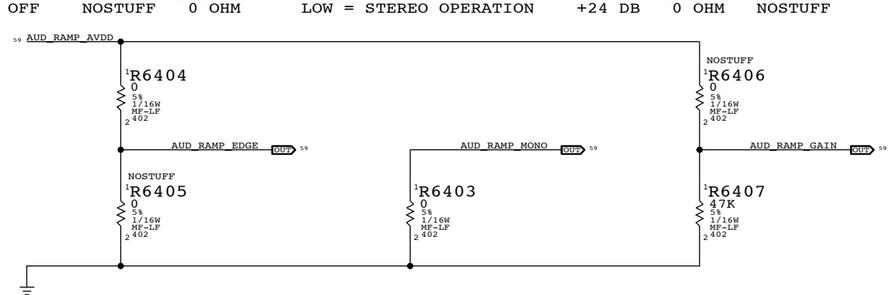
SPEAKER AMP GAIN = +9 DB
SPEAKER AMP RIN = 40K NOMINAL
FC_HPF, TWEETERS = ~847 HZ (4700 PF)
FC_HPF, WOOFERS = ~4 HZ (1.0 UF)



EDGE RATE CONTROL	R6404	R6405
ON	0 OHM	NOSTUFF
OFF	NOSTUFF	0 OHM

AUD_RAMP_MONO NET:
HIGH = MONO OPERATION
LOW = STEREO OPERATION

GAIN	R6406	R6407
+9 DB	NOSTUFF	0 OHM
+12 DB	NOSTUFF	47 KOHM
+15 DB	NOSTUFF	NOSTUFF
+18 DB	47 KOHM	NOSTUFF
+24 DB	0 OHM	NOSTUFF



SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE
AUDIO: RIGHT SPKR AMP

Apple Inc.

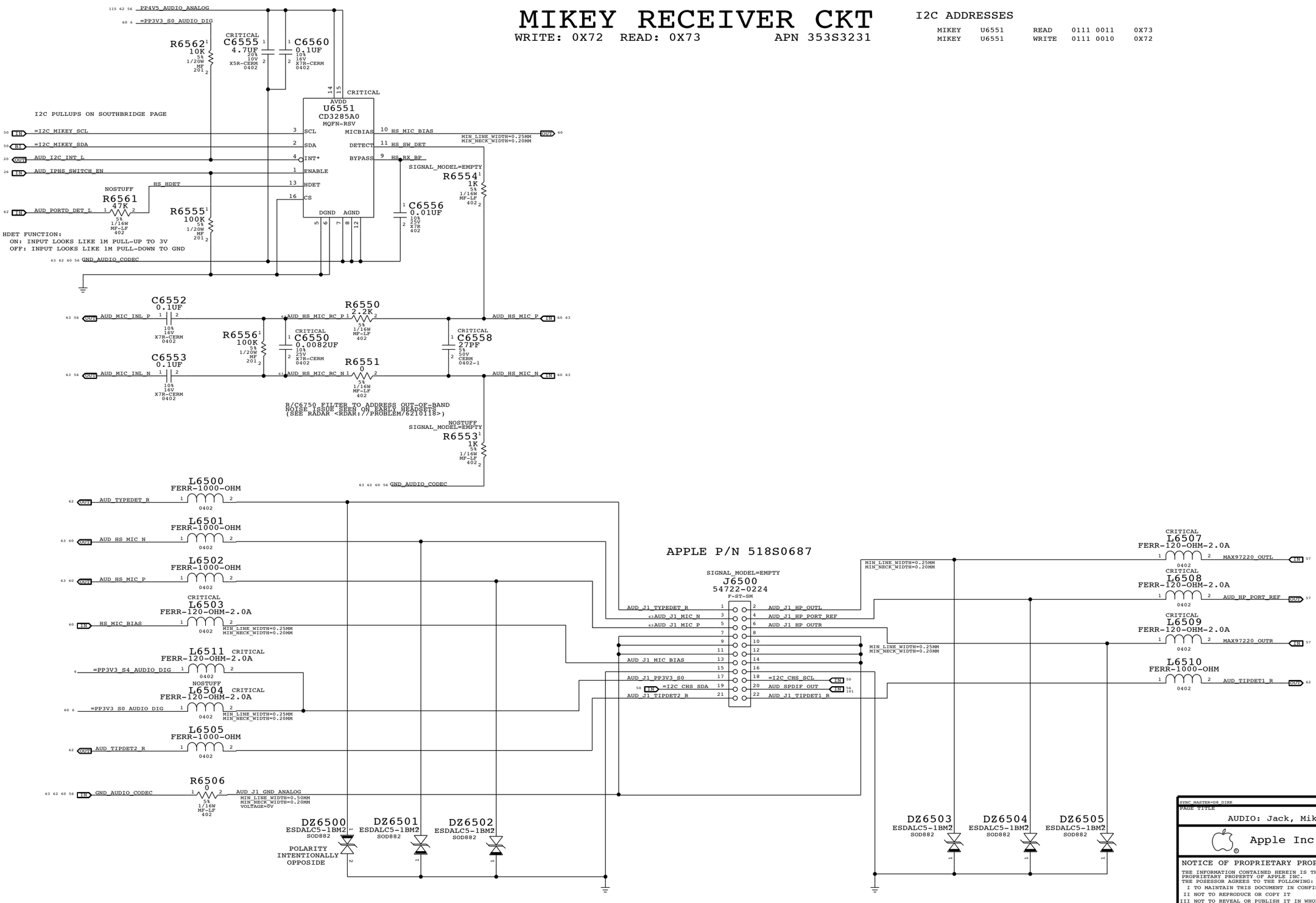
DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 64 OF 143
SHEET 59 OF 117

MIKEY RECEIVER CKT

WRITE: 0X72 READ: 0X73 APN 353S3231

I2C ADDRESSES

MIKEY	U6551	READ	0111 0011	0X73
MIKEY	U6551	WRITE	0111 0010	0X72



SYNC_MASTER=D8_DIRK SYNC_DATE=06/29/2012

PAGE TITLE

AUDIO: Jack, Mikey, CHS Switch

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

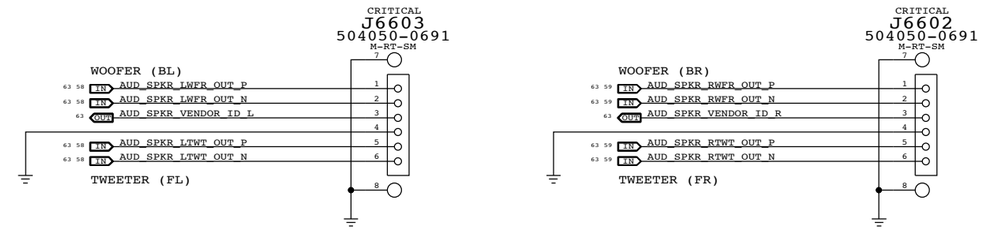
BRANCH prefsb

PAGE 65 OF 143

SHEET 60 OF 117

SPEAKER CABLE CONNECTORS

APPLE P/N 518S0862



SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE
Audio: Spkr/Mic Conn.

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

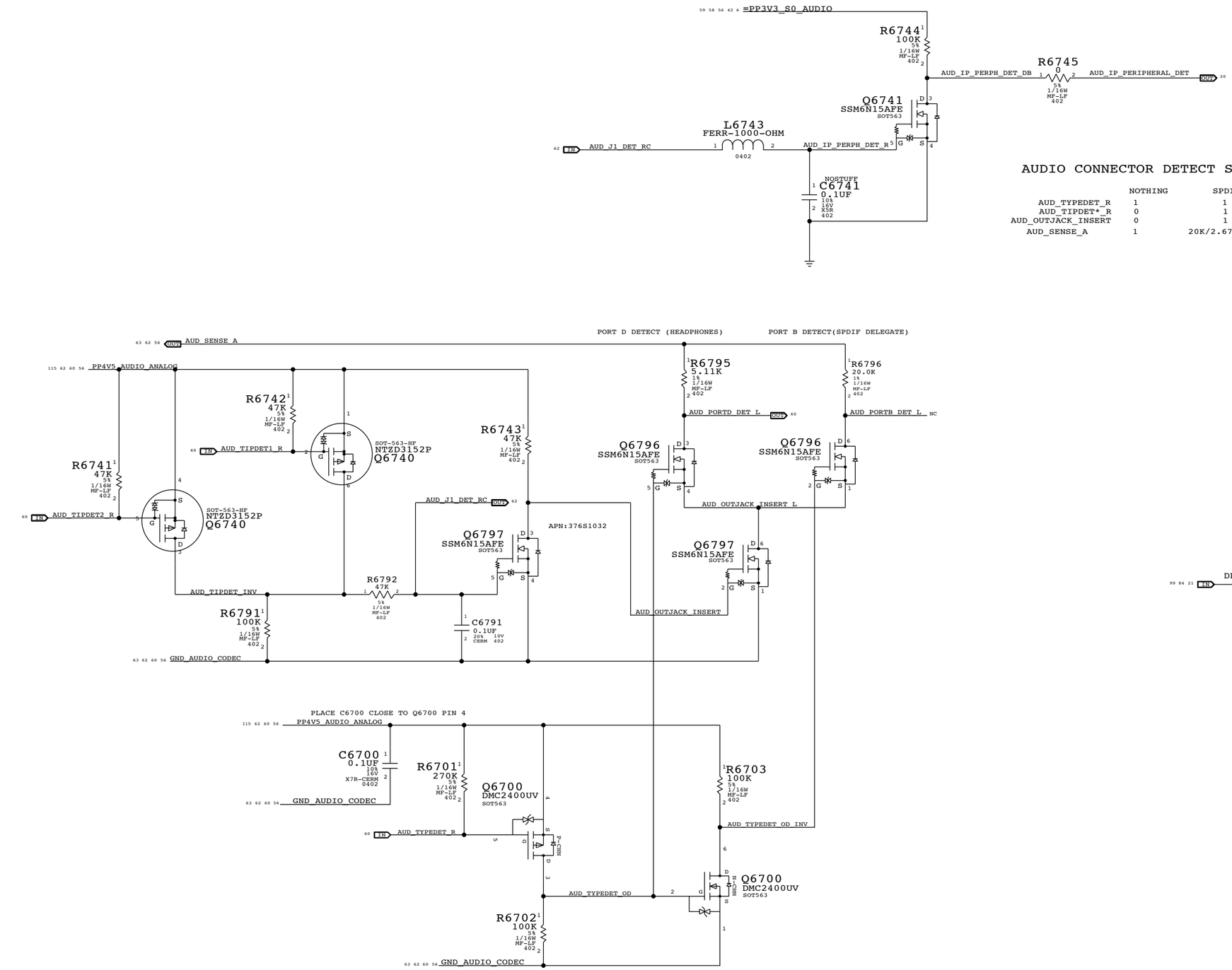
REVISION 7.0.0

BRANCH prefsb

PAGE 66 OF 143

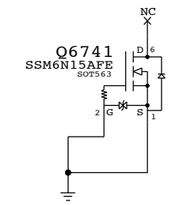
SHEET 61 OF 117

IPHS HS Detect Debounce CKT

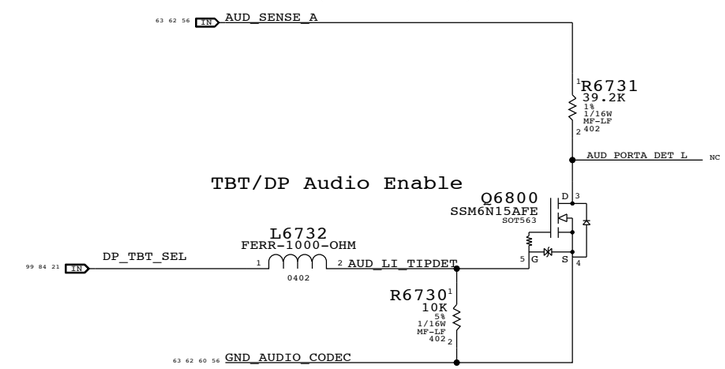


AUDIO CONNECTOR DETECT STATES

	NOTHING	SPDIF	HEADPHONE
AUD_TYPEDET_R	1	1	0
AUD_TIPDET*_R	0	1	1
AUD_OUTJACK_INSERT	0	1	1
AUD_SENSE_A	1	20K/2.67K RDIV	5.11K/2.67K RDIV



LI Insert Detect (DETECT A)



SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE
AUDIO: Detects/Grounding

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 67 OF 143

SHEET 62 OF 117

CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME/MUTE	CONVERTER	PIN COMPLEX	MAC SHDN	WIN SHDN	DET ASSIGNMENT
HP/LINE OUT	0X03 (3)	0X03 (3)	0X0A (10,D)	GPIO_2	GPIO_2	0X0A (DET D)
PRIMARY SPKRS (WFR)	0X04 (4)	0X04 (4)	0X0B (11)	MICBIAS	GPIO_3	N/A
SECONDARY SPKRS (TWT)	0X03 (3)	0X03 (3)	0X0A (10,V24)	MICBIAS	N/A	N/A
SPDIF OUT	N/A	0X08 (8)	0x10 (16)	N/A	N/A	0X0D (DET B)

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
SPDIF IN	0X07 (7)	0x0F (15)	N/A	0X09 (DET A)
INTERNAL MIC ARRAY	0X06 (6) 0X05 (5)	0X0E (14,LEFT & RIGHT) 0X12 (18,LEFT)	N/A	N/A
EXTERNAL MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	PANTHER POINT GPIO 16	PANTHER POINT GPIO 5 (RCVR INT) PANTHER POINT GPIO 3 (PERIPH DET)

OTHER DETECT

FUNCTION	CONVERTER	PIN COMPLEX	ENABLE/CONTROL	DET ASSIGNMENT
MULTIPLE SPKR VENDORS	N/A	N/A	N/A	0X0C (DET C)

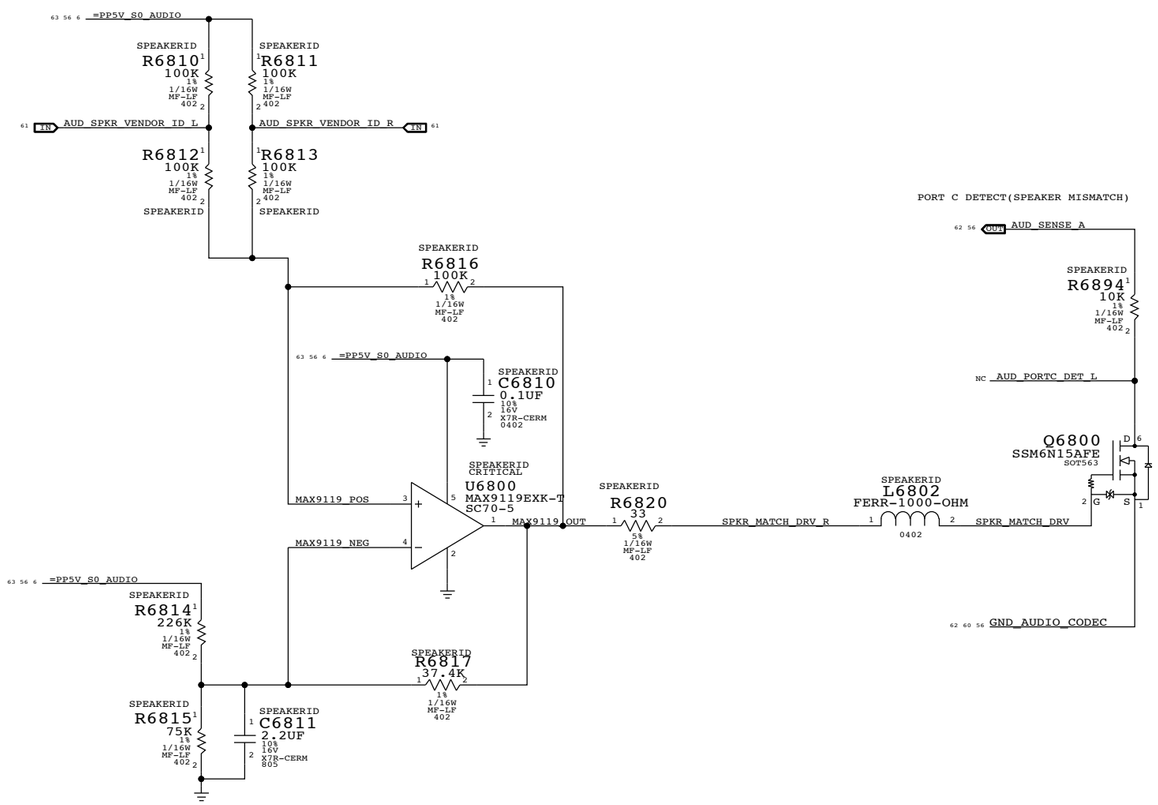
SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.1 MM	?
SPKROUT	*	0.2 MM	?

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIODIFF	*	AUDIODIFF
SPKROUTDIFF	*	SPKROUTDIFF

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
SPKROUTDIFF	*	Y	0.6 MM	0.25 MM	10 MM	0.2 MM	0.2 MM

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
P15 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_P	56 57 58
P16 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_N	56 57 58
P17 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_P	57
P18 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_L_C_N	57
P19 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_P	56 57 59
P20 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_N	56 57 59
P21 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_P	57
P22 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO1_R_C_N	57
P23 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P	56 58
P24 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N	56 58
P25 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P	56 59
P26 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N	56 59
P27 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_P	59
P28 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LINC_N	59
P29 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_P	59
P30 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RINC_N	59
P31 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_P	59
P32 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_LIN_N	59
P33 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_P	59
P34 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_RAMP_RIN_N	59
P35 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_P	58
P36 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LINC_N	58
P37 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_P	58
P38 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RINC_N	58
P39 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_P	58
P40 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_LIN_N	58
P41 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_P	58
P42 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LAMP_RIN_N	58
P43 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_P	57
P44 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INL_N	57
P45 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_P	57
P46 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	MAX97220_INR_N	57
P47 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_P	59 61
P48 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RWFR_OUT_N	59 61
P49 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_P	59 61
P50 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_RTWT_OUT_N	59 61
P51 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_P	58 61
P52 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LWFR_OUT_N	58 61
P53 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_P	58 61
P54 SPKROUT_DIFFPAIR	SPKROUTDIFF	SPKROUT	AUD_SPKR_LTWT_OUT_N	58 61
P55 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_P	56 60
P56 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_MIC_INL_N	56 60
P57 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_P	60
P58 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_RC_N	60
P59 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_P	60
P60 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_HS_MIC_N	60
P61 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_P	60
P62 AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_J1_MIC_N	60

CIRCUIT THEORY OF OPERATION AVAILABLE IN <RDAR://PROBLEM/9776522>



PORT C DETECT(SPEAKER MISMATCH)

SYNC MASTER=D8 DAVID SYNC DATE=06/13/2012

PAGE TITLE

AUDIO: Speaker ID

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

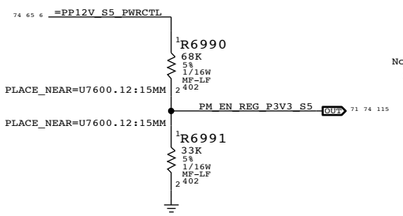
REVISION 7.0.0

BRANCH prefsb

PAGE 68 OF 143

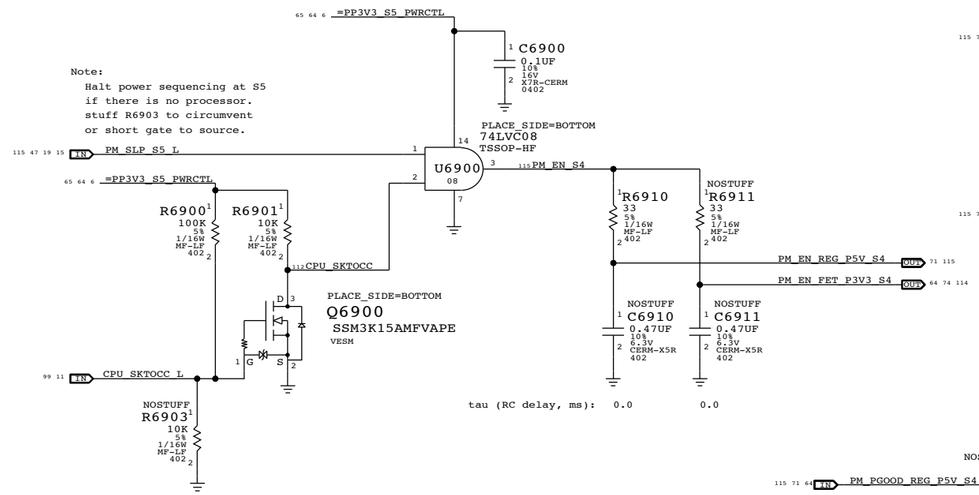
SHEET 63 OF 117

S5 3V3 Soft Enable



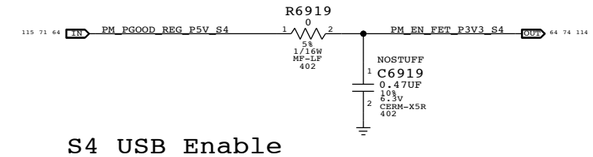
Note:
Expected 3.9V +/- 0.4V EN signal

S4 5V Enable

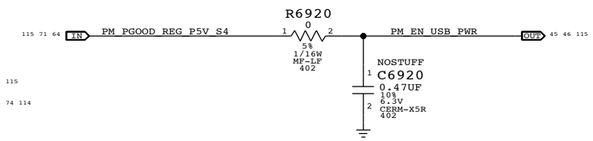


Note:
Halt power sequencing at S5
if there is no processor.
stuff R6903 to circumvent
or short gate to source.

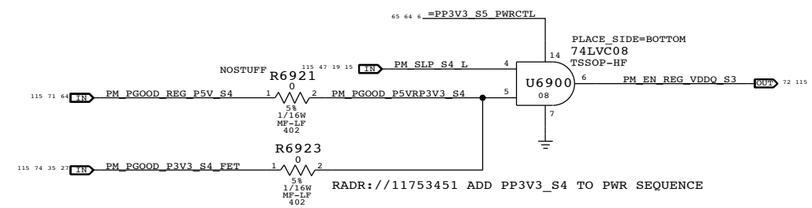
S4 3V3 Enable



S4 USB Enable

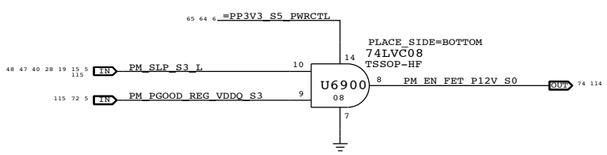


S3 1V5 Reg (S0/S3) Enable

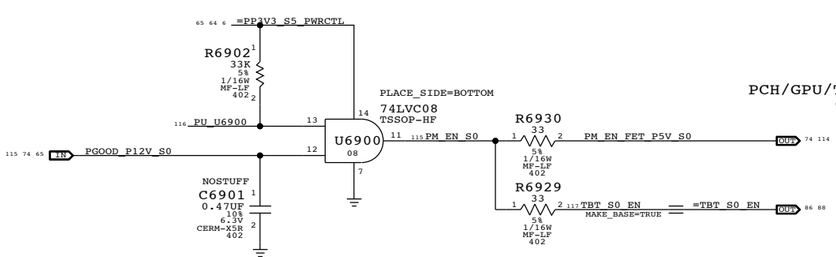


RADR://11753451 ADD PP3V3_S4 TO PWR SEQUENCE

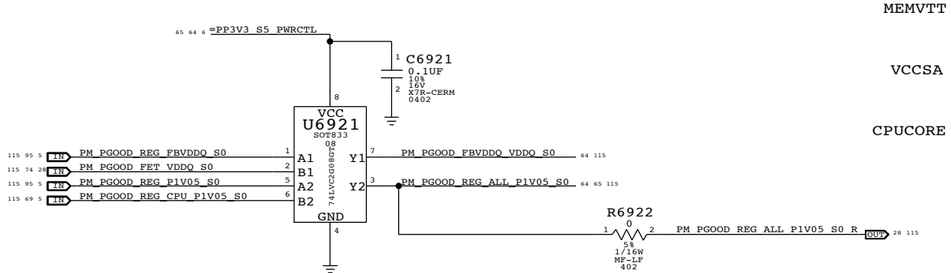
S0 12V Enable



S0 5V and TBT Enable

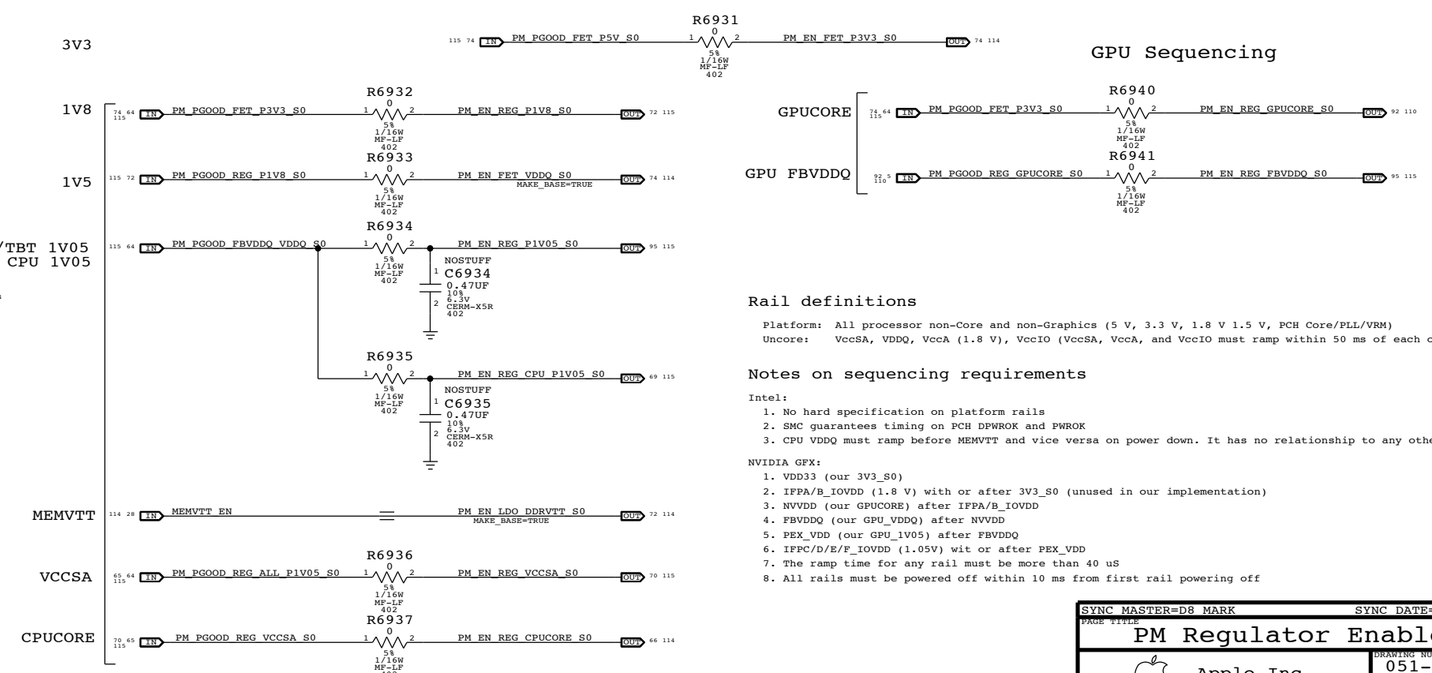


Parallel Enable PGOOD combinator



S0 Platform Parallel Sequence Enable

CPU/PCH Sequencing



GPU Sequencing

Rail definitions

Platform: All processor non-Core and non-Graphics (5 V, 3.3 V, 1.8 V 1.5 V, PCH Core/PLL/VRM)
Uncore: VccSA, VDDQ, VccA (1.8 V), VccIO (VccSA, VccA, and VccIO must ramp within 50 ms of each other)

Notes on sequencing requirements

Intel:
1. No hard specification on platform rails
2. SMC guarantees timing on PCH DPWROK and PWROK
3. CPU VDDQ must ramp before MEMVTT and vice versa on power down. It has no relationship to any other rails.

NVIDIA GFX:
1. VDD33 (our 3V3_S0)
2. IFPA/B_IOVDD (1.8 V) with or after 3V3_S0 (unused in our implementation)
3. NVVDD (our GPUCORE) after IFPA/B_IOVDD
4. FBVDDQ (our GPU_VDDQ) after NVVDD
5. PEX_VDD (our GPU_1V05) after FBVDDQ
6. IFPC/D/E/F_IOVDD (1.05V) wit or after PEX_VDD
7. The ramp time for any rail must be more than 40 uS
8. All rails must be powered off within 10 ms from first rail powering off

SYNC MASTER=D8 MARK	SYNC DATE=04/23/2012
PAGE TITLE: PM Regulator Enables	
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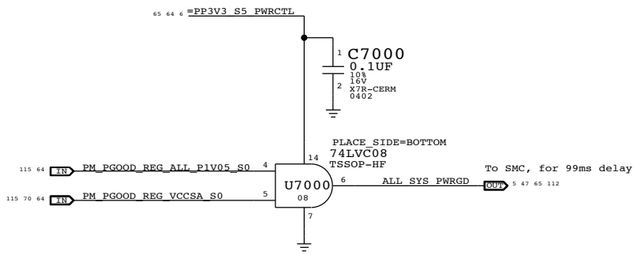
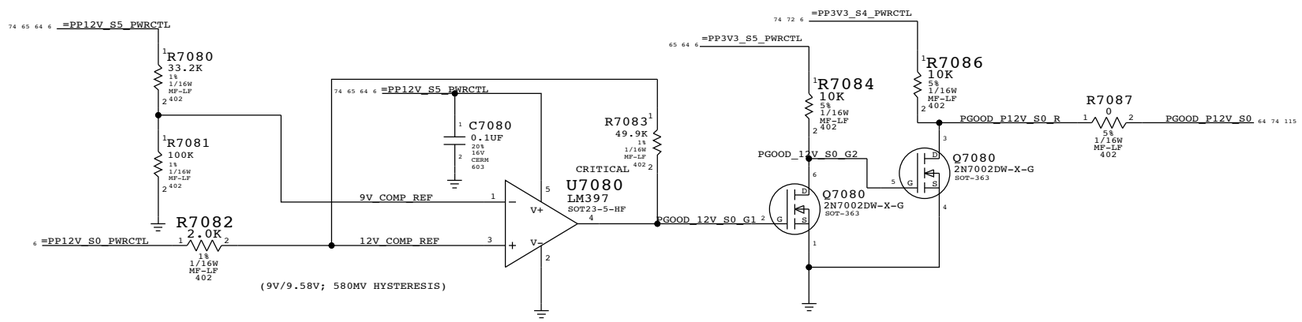
	PAGE: 69 OF 143
	SHEET: 64 OF 117

Platform Power Good Derive SMC ALL_SYS_PWRGD

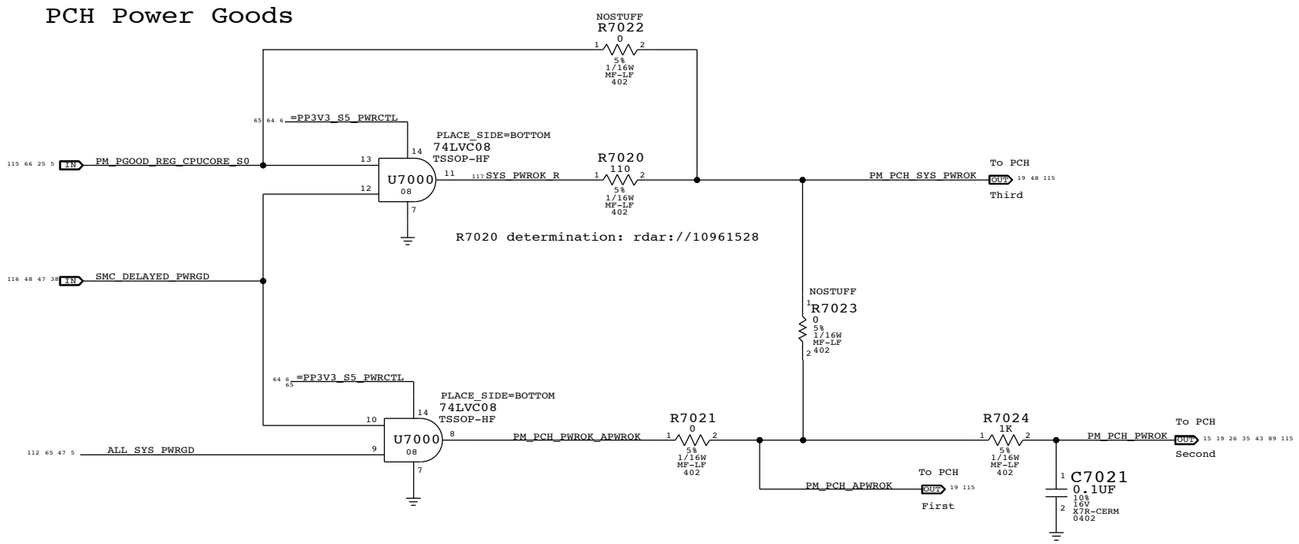
The end of the power sequence for S0 rails except CPU CORE.



PGOOD COMPARATORS FOR PP12V_S0



PCH Power Goods



radar://11043352 Need AND Gate to deassert PM_PCH_PWROK to PCH when unexpected power loss happens

Resume Reset

Intel Doc# 29517 Maho Bay PDG, Section 22.13
Intel Doc# 29562 Panther Point EDS, Section 8.7 and 8.8

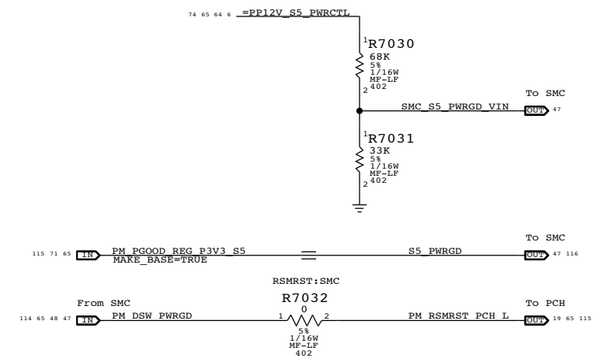
Note:
The iMac K70K72 designs does not support Deep Sx modes so both DPWROK and RSMRST# signals are shorted together

Requirements:
Power on:
Asserted at least 10 ms after all suspend well power is valid
Power off or loss of AC:
Transition to 0.8V or less before VccSUS3_3 drops to 2.90 V to allow PCH to switch suspend well to battery without excessive loading

Primary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation.

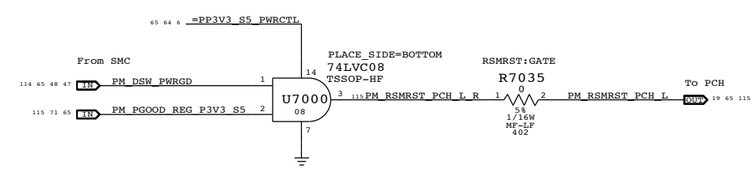
SMC de-asserts RSMRST# (PM_DSW_PWRGD) when S5_PWRGD input is asserted and SMC_S5_PWRGD_VIN input is above comparator input level of 1.5 V.

SMC asserts RSMRST# (PM_DSW_PWRGD) when SMC_S5_PWRGD_VIN input drops from 1.8 V to 1.5 V (as implemented) when 12 V S5 rail drops to 10 V.



Secondary method:
The SMC guarantees proper assertion and de-assertion of RSMRST# for normal operation via PM_DSW_PWRGD.

RSMRST# is asserted when power good from regulator is de-asserted in the event AC is lost. Power good de-assertion should happen quickly enough to meet Intel spec.

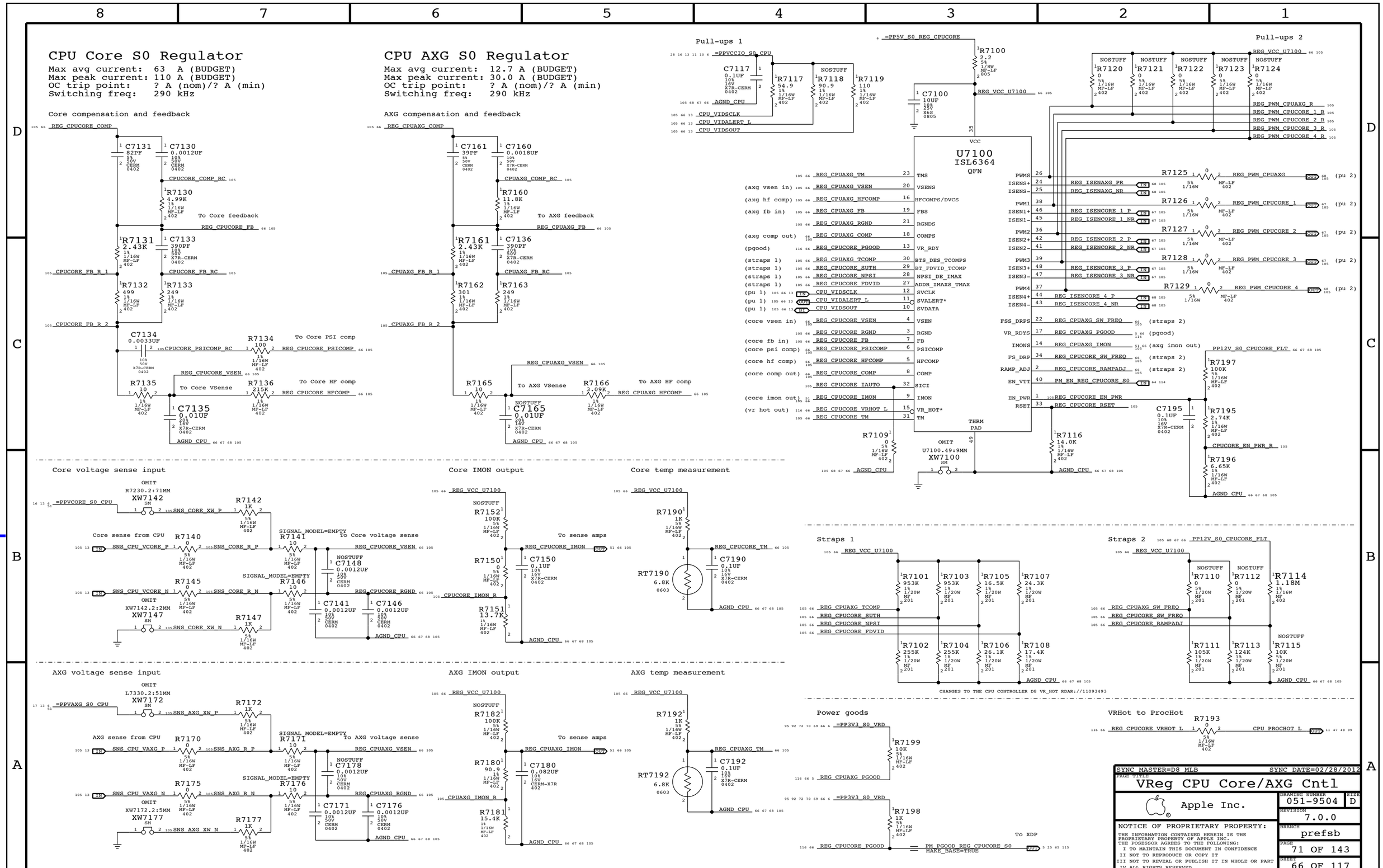


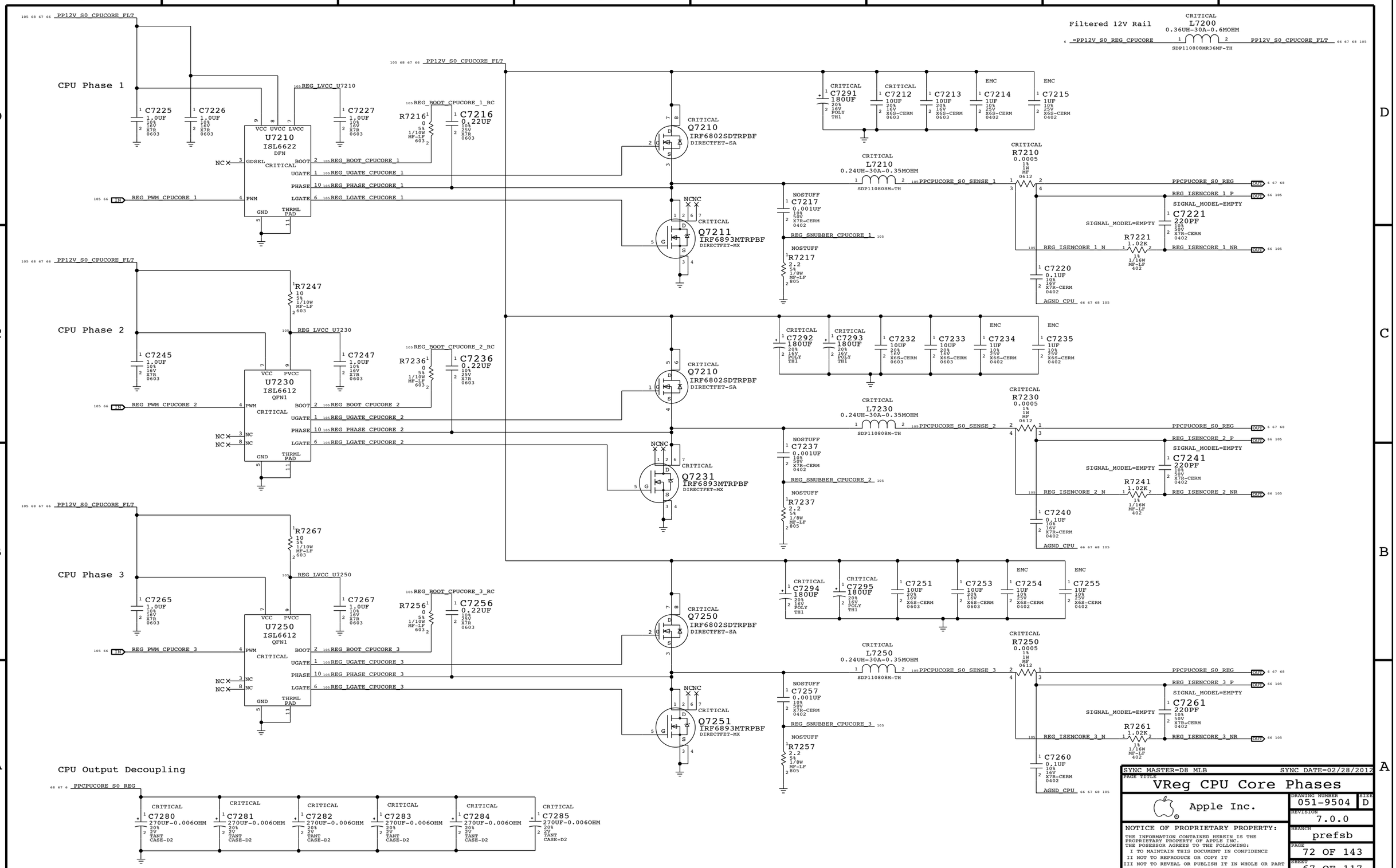
SYNC MASTER=D8 MARK SYNC DATE=04/23/2012

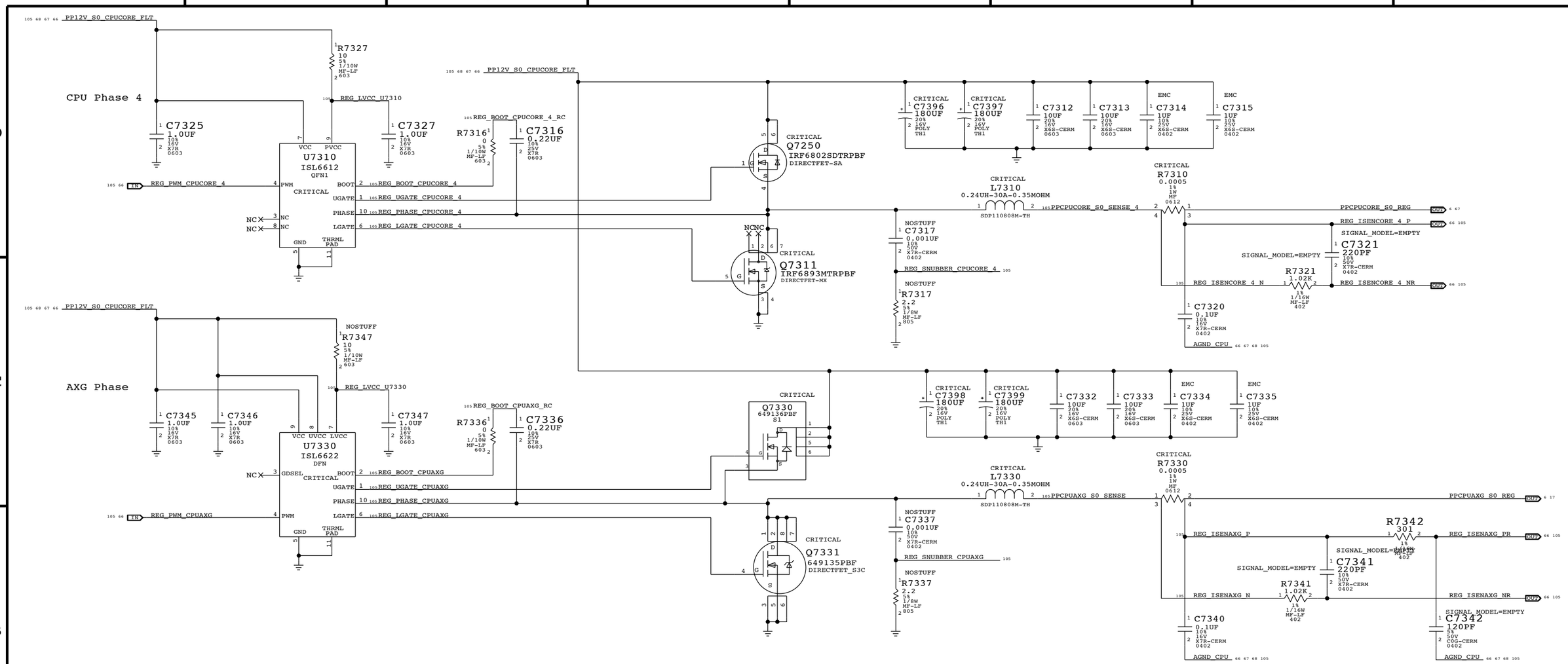
PAGE TITLE
PM Power Good

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 70 OF 143
SHEET 65 OF 117







SYNC MASTER=D8 MLB SYNC DATE=02/28/2012

PAGE TITLE

VReg CPU AXG Phases

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

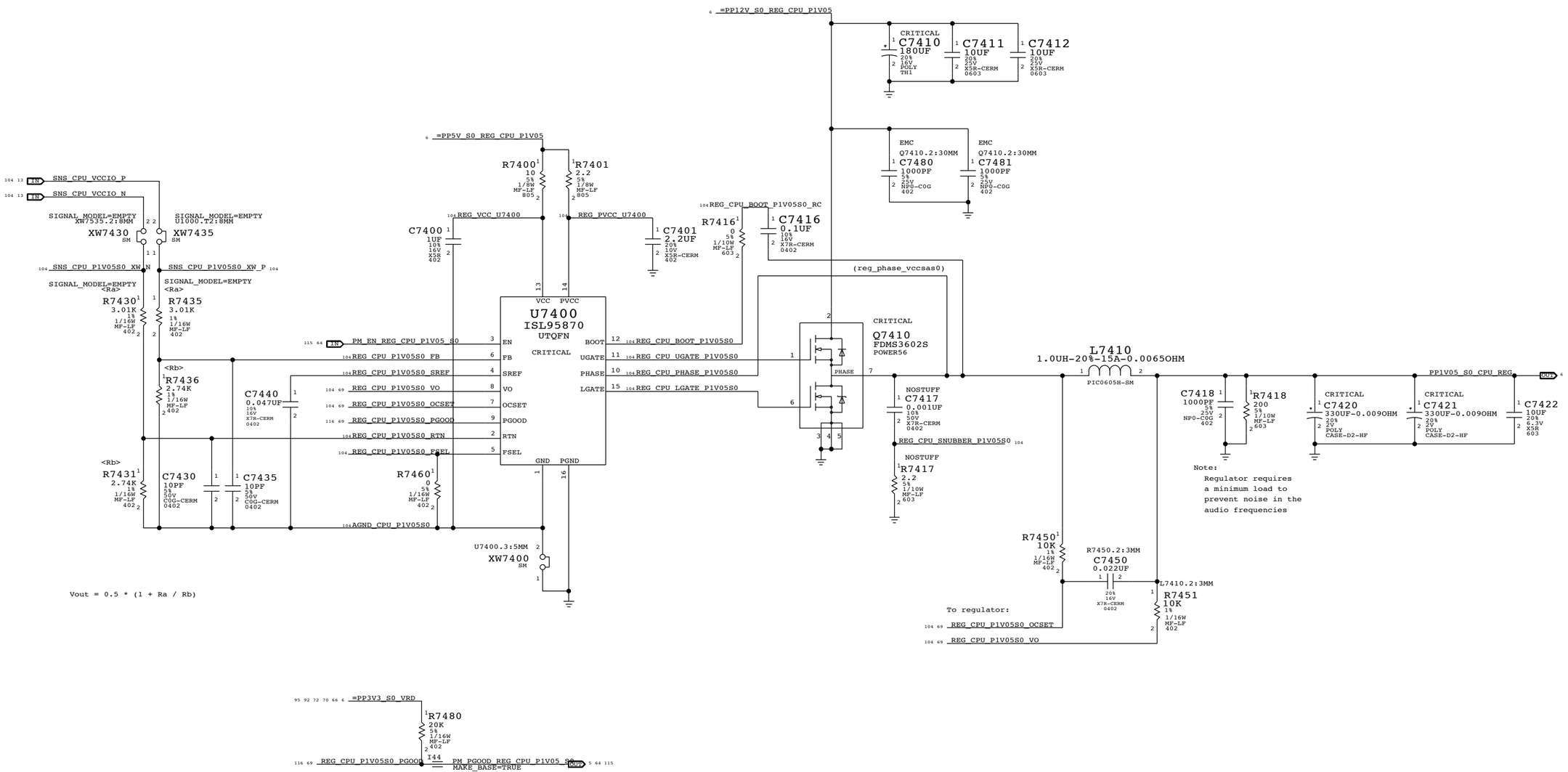
BRANCH prefsb

PAGE 73 OF 143

SHEET 68 OF 117

CPU VccIO (1.05V) S0 Regulator

Max avg current: 8.10 A (BUDGET)
Max peak current: 8.50 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



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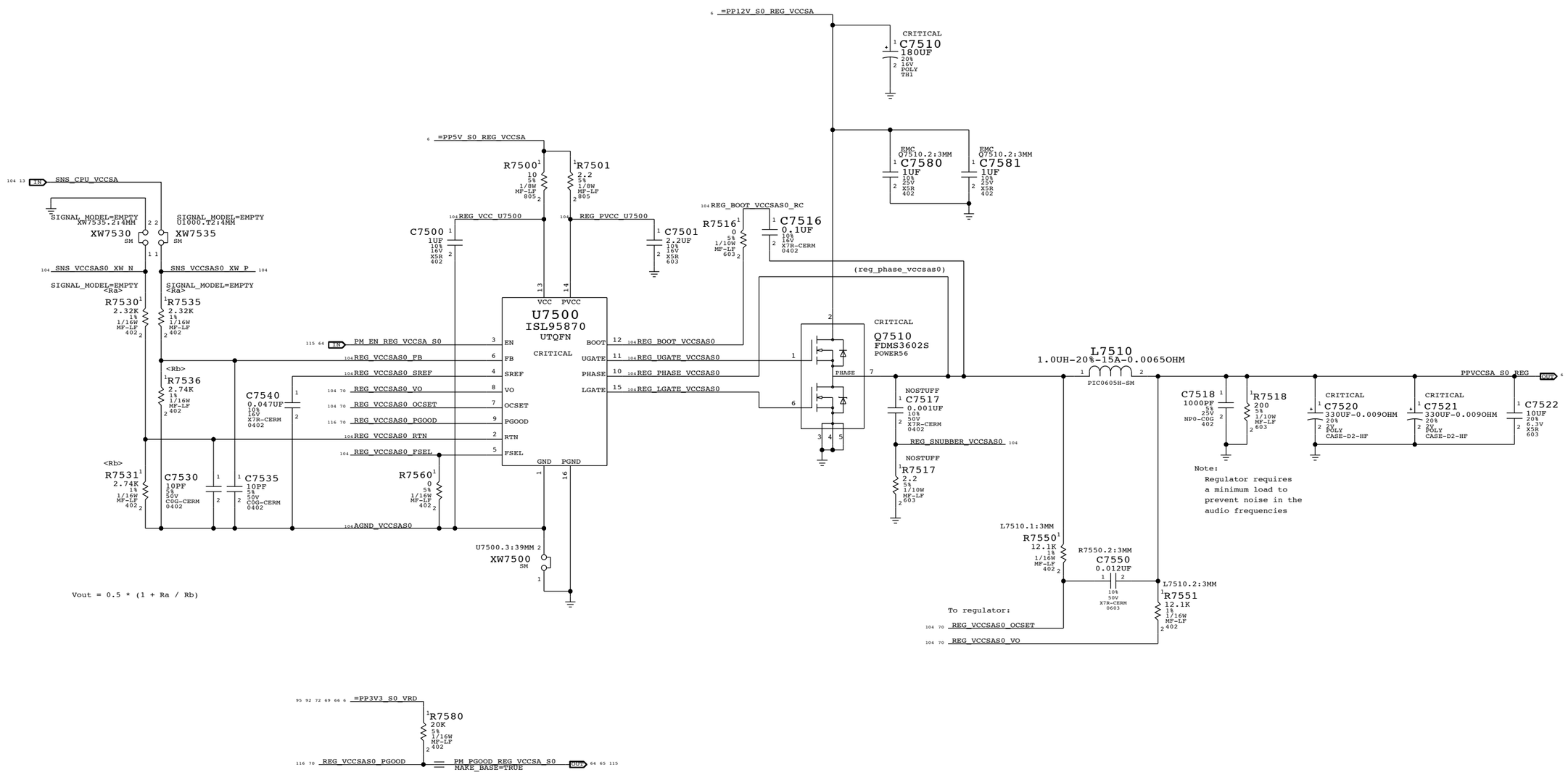
PAGE TITLE: VReg CPU 1.05V S0	
Apple Inc.	DRAWING NUMBER 051-9504 / SIZE D
	REVISION 7.0.0
	BRANCH prefsb
	PAGE 74 OF 143
	SHEET 69 OF 117

CPU VccSA (0.925V) S0 Regulator

Max avg current: 12.07 A (BUDGET)
Max peak current: 30 A (BUDGET)
OC trip point: ? A (min)/? A (max)
Switching freq: 500 kHz



SYNC MASTER=D8 KOSECOFF	SYNC DATE=02/25/2012
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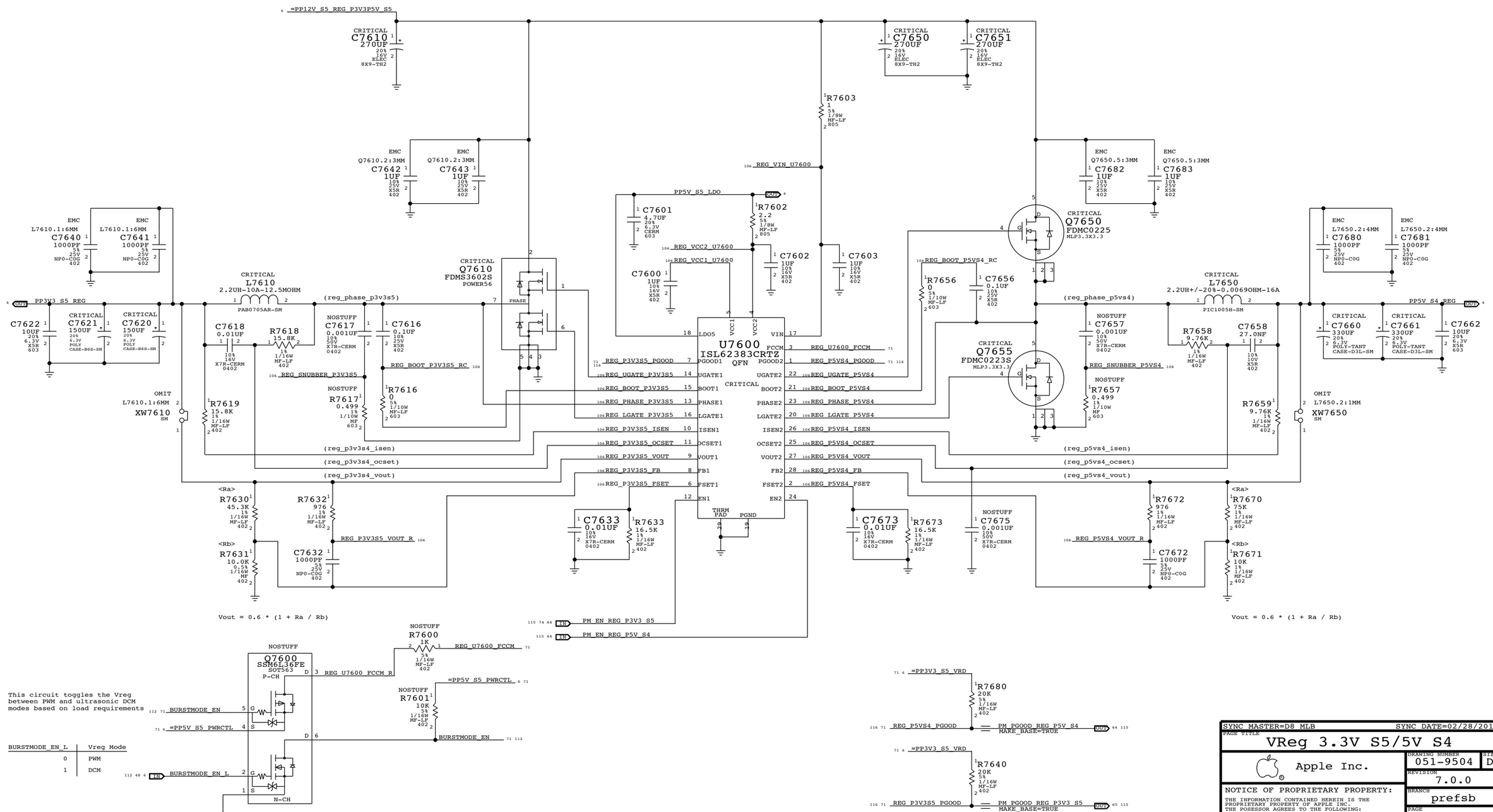
	PAGE: 75 OF 143
	SHEET: 70 OF 117

3.3V S5 Regulator

Max avg current: 6 A (design)/ 4.85 A (budget)
Max peak current: ? A (design)/ 6.6 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz

5V S4 Regulator

Max avg current: 10 A (design)/ 6.08 A (budget)
Max peak current: ? A (design)/ 6.9 A (budget)
OC trip point: ? A (nom)/? A (min)
Switching freq: 350 kHz



SYNC MASTER=D8 MLB SYNC DATE=02/28/2012

PAGE TITLE: VReg 3.3V S5/5V S4

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DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

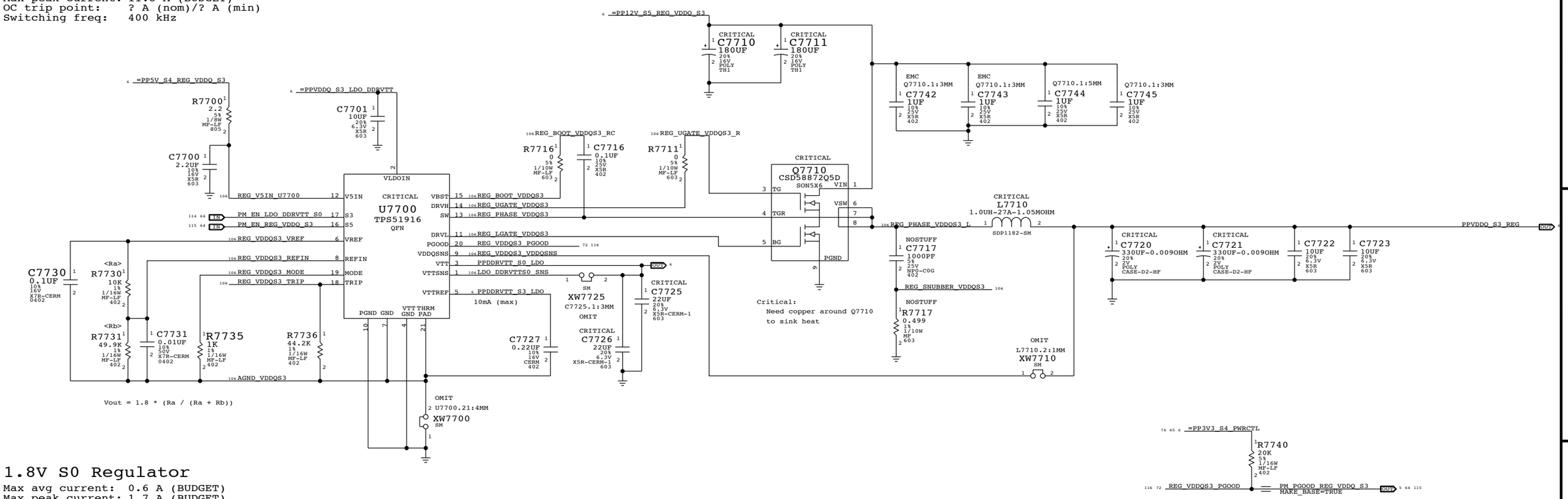
BRANCH: prefsb

PAGE: 76 OF 143

SHEET: 71 OF 117

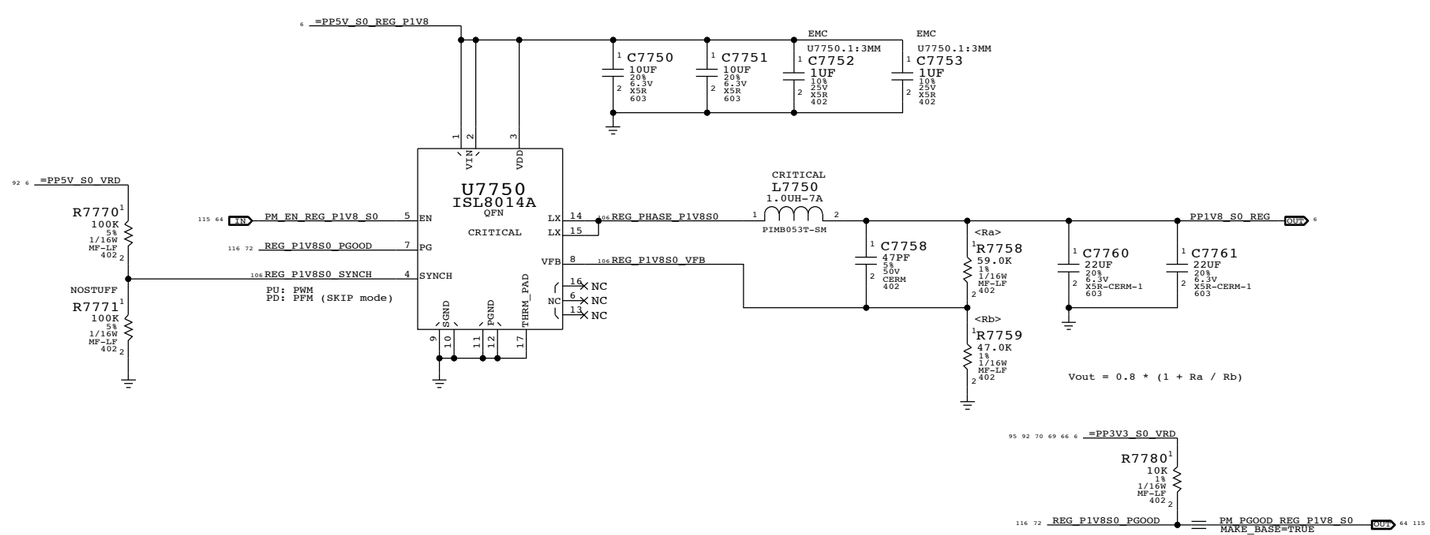
VDDQ (1.5V) S3 Regulator

Max avg current: 9.0 A (BUDGET)
Max peak current: 11.3 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: 400 kHz



1.8V S0 Regulator

Max avg current: 0.6 A (BUDGET)
Max peak current: 1.7 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



SYNC MASTER=D8 KOSECOFF SYNC DATE=02/25/2012

PAGE TITLE: VReg VDDQ and 1.8V S0

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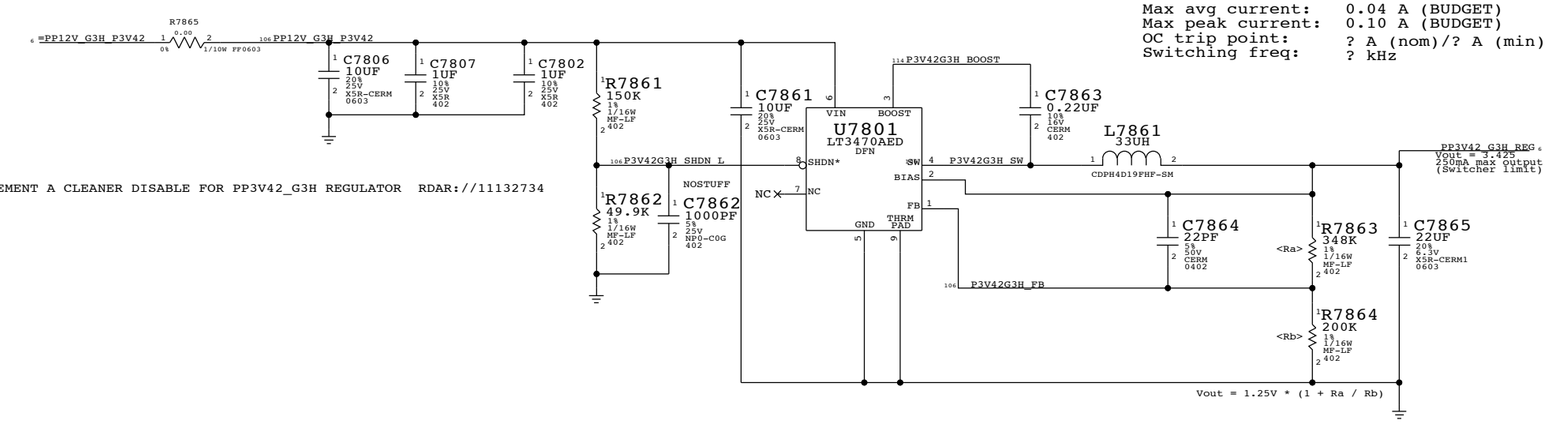
DRAWING NUMBER: 051-9504 SIZE: D
REVISION: 7.0.0
BRANCH: prefsb
PAGE: 77 OF 143
SHEET: 72 OF 117

D8:CONTROLLER CHANGE FOR 3.42V SMC SUPPLY RDAR://11003901

D7/D7I: IMPLEMENT A CLEANER DISABLE FOR PP3V42_G3H REGULATOR RDAR://11132734

3.425V "G3Hot" Regulator

Max avg current: 0.04 A (BUDGET)
Max peak current: 0.10 A (BUDGET)
OC trip point: ? A (nom)/? A (min)
Switching freq: ? kHz



SYNC MASTER=D8 MLB SYNC DATE=04/11/2012

PAGE TITLE
VREG 3.42V G3HOT

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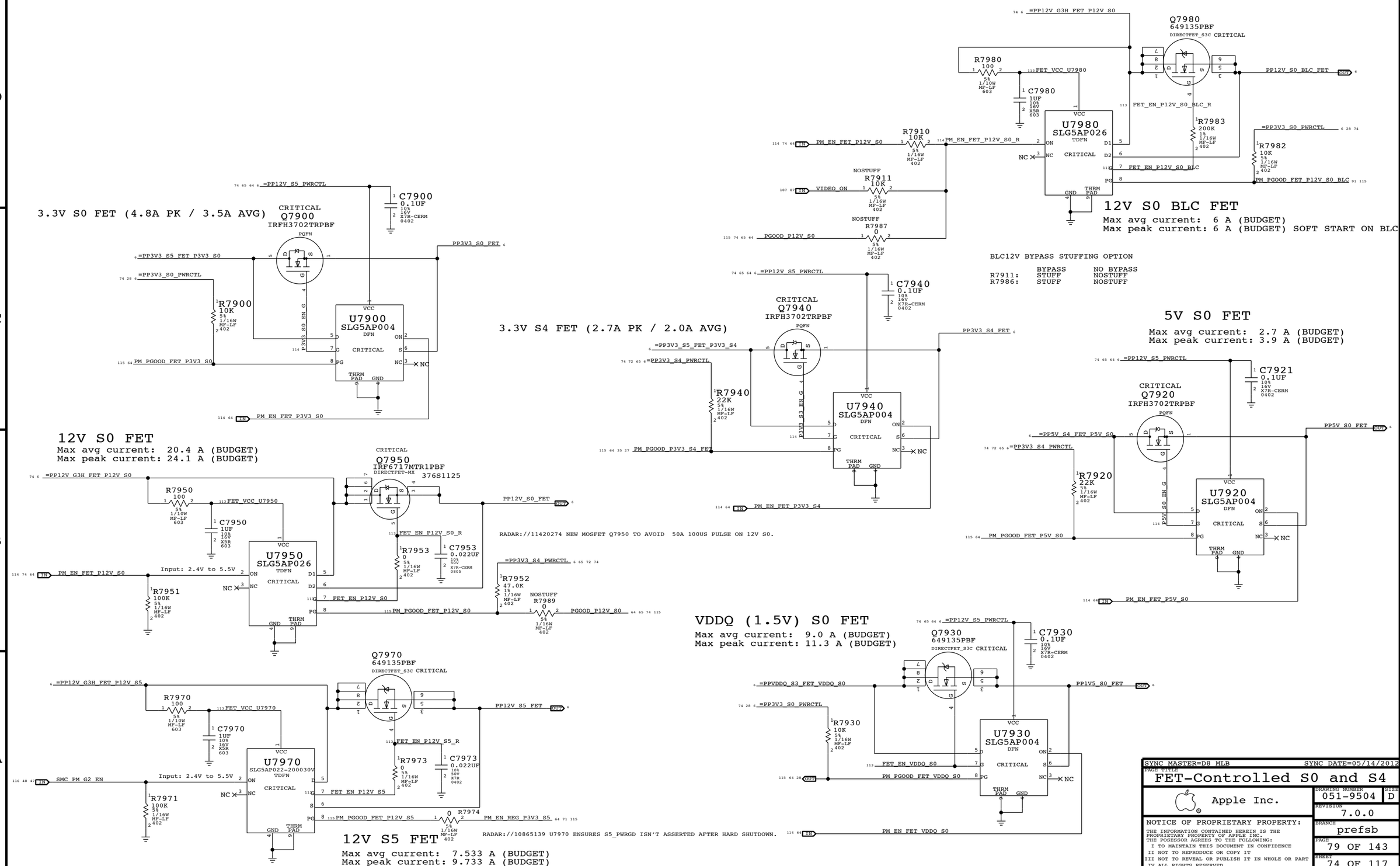
DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 78 OF 143
SHEET 73 OF 117



Page Notes

Power aliases required by this page:

- =PPVX1_GPU_VDDII

Signal aliases required by this page:

(NONE)

ROM options provided by this page:

(NONE)

ALL LANES ARE REVERSED AND LANES 10,8,7,6,5,3,2,1 ARE POLARITY SWAPPED

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PEG_D2R_N<13>	CA059	PEG_D2R_C_P<2>	PEG_D2R_N<5>	CA075	PEG_D2R_C_P<10>
PEG_D2R_P<13>	CA060	PEG_D2R_C_N<2>	PEG_D2R_P<5>	CA076	PEG_D2R_C_N<10>
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PEG_D2R_P<10>	CA065	PEG_D2R_C_P<5>	PEG_D2R_P<2>	CA081	PEG_D2R_C_P<13>
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PEG_D2R_P<8>	CA070	PEG_D2R_C_N<7>	PEG_D2R_P<0>	CA086	PEG_D2R_C_N<15>

DP_TBTSNK0_EG_AUXCH_P	DP_TBTSNK0_AUXCH_C_P	MAKE_BASE=TRUE
DP_TBTSNK0_EG_AUXCH_N	DP_TBTSNK0_AUXCH_C_N	MAKE_BASE=TRUE
DP_TBTSNK1_EG_AUXCH_P	DP_TBTSNK1_AUXCH_C_P	MAKE_BASE=TRUE
DP_TBTSNK1_EG_AUXCH_N	DP_TBTSNK1_AUXCH_C_N	MAKE_BASE=TRUE

OMIT_TABLE

U8000
NV-GK107
BGA
(1 OF 10)

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PEG_R2D_C_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_N<1>
PEG_R2D_C_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_P<2>
PEG_R2D_C_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_N<2>
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PEG_R2D_C_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_P<5>
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PEG_R2D_C_N<8>	AP21	PEX_RX8*	PEX_TX8*	AJ20	PEG_D2R_N<8>
PEG_R2D_C_P<9>	AN21	PEX_RX9	PEX_TX9	AH20	PEG_D2R_P<9>
PEG_R2D_C_N<9>	AM21	PEX_RX9*	PEX_TX9*	AG20	PEG_D2R_N<9>
PEG_R2D_C_P<10>	AN23	PEX_RX10	PEX_TX10	AK21	PEG_D2R_P<10>
PEG_R2D_C_N<10>	AM23	PEX_RX10*	PEX_TX10*	AJ21	PEG_D2R_N<10>
PEG_R2D_C_P<11>	AP23	PEX_RX11	PEX_TX11	AL22	PEG_D2R_P<11>
PEG_R2D_C_N<11>	AP24	PEX_RX11*	PEX_TX11*	AK22	PEG_D2R_N<11>
PEG_R2D_C_P<12>	AN24	PEX_RX12	PEX_TX12	AK23	PEG_D2R_P<12>
PEG_R2D_C_N<12>	AM24	PEX_RX12*	PEX_TX12*	AJ23	PEG_D2R_N<12>
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PEG_R2D_C_N<13>	AM26	PEX_RX13*	PEX_TX13*	AG23	PEG_D2R_N<13>
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PEG_R2D_C_N<15>	AM27	PEX_RX15*	PEX_TX15*	AK25	PEG_D2R_N<15>
PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK_O_PL
PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	PEX_TSTCLK_O_NG
GPU_RESET_L	AJ12	PEX_RST*	PEX_TERMP	AP29	GPU_PEX_TERMP
PEG_CLKREQ_L	AK12	PEX_CLKREQ*			
NC	AJ11	PEX_WAKE*	PEX_SVDD_3V3	AG12	=PP3V3_GPU_VDDJ3

R8000: GPU_RESET_L – 0 – GPU_RESET_R_L, MF 5% 1/20W 201

R8002: 200, 1% MF 1/20W 201, MOSTUFF

R8005: 2.49K, 1% 1/20W MF 201

SYNC MASTER=D8 AARON SYNC DATE=03/13/2012

PAGE TITLE

KEPLER PCI-E

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

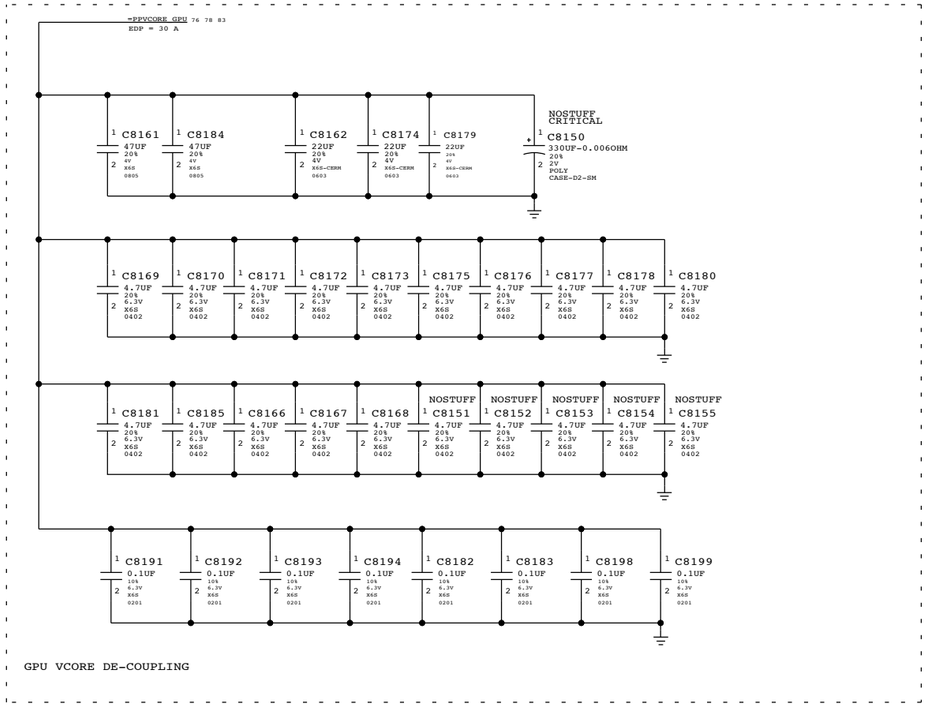
REVISION 7.0.0

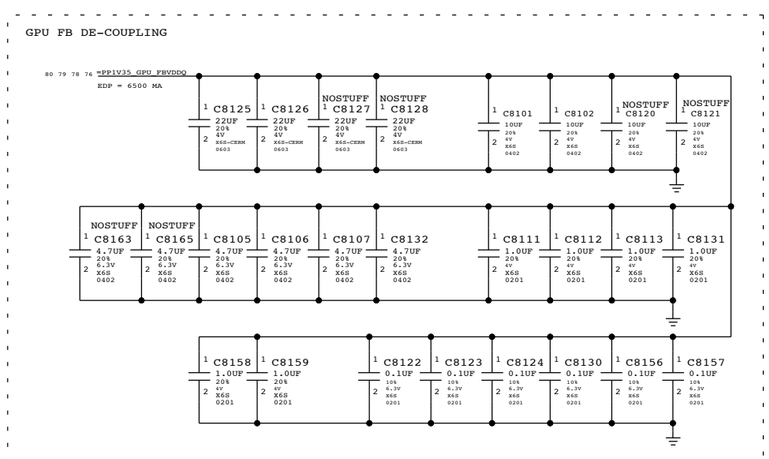
BRANCH prefsb

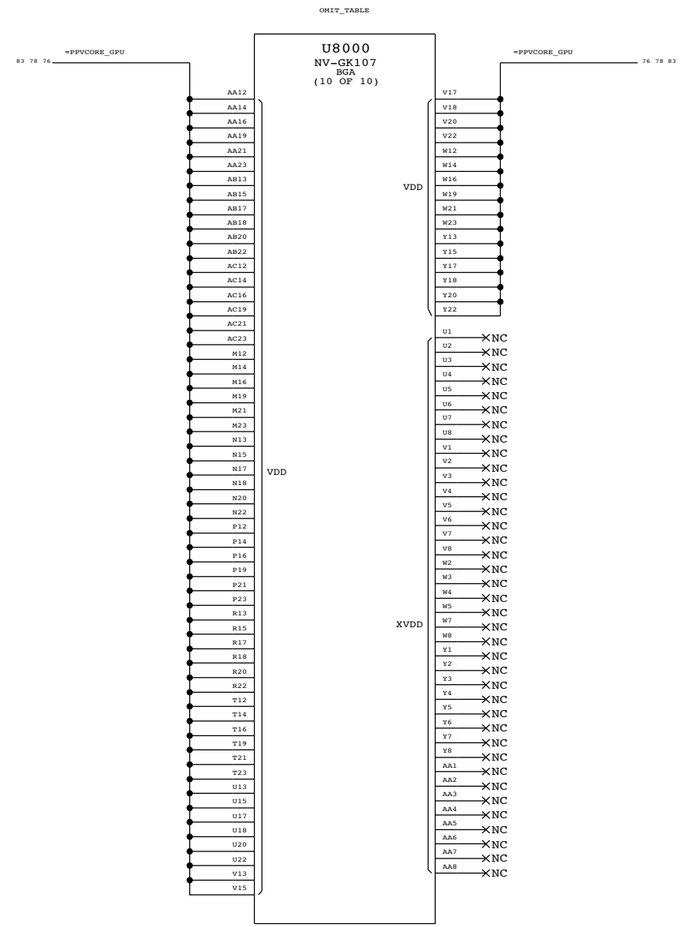
PAGE 80 OF 143

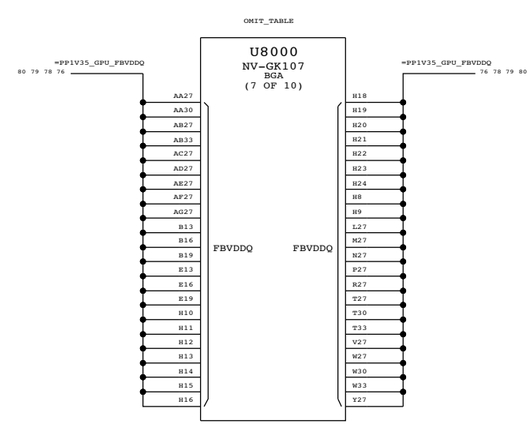
SHEET 75 OF 117

DE-COUPLING IS BASED ON NV DESIGN GUIDELINE DG-05587-001









Page Notes

Power aliases required by this page:

- =PPVPCORE_GPU
- =PPV1V5_GPU_FBVDDQ

Signal aliases required by this page.

(NONE;

BOM options provided by this page.

(NONE;

SYNC MASTER=D8 YAN SYNC DATE=04/09/2012

PAGE TITLE
KEPLER CORE/FB POWER

Apple Inc.

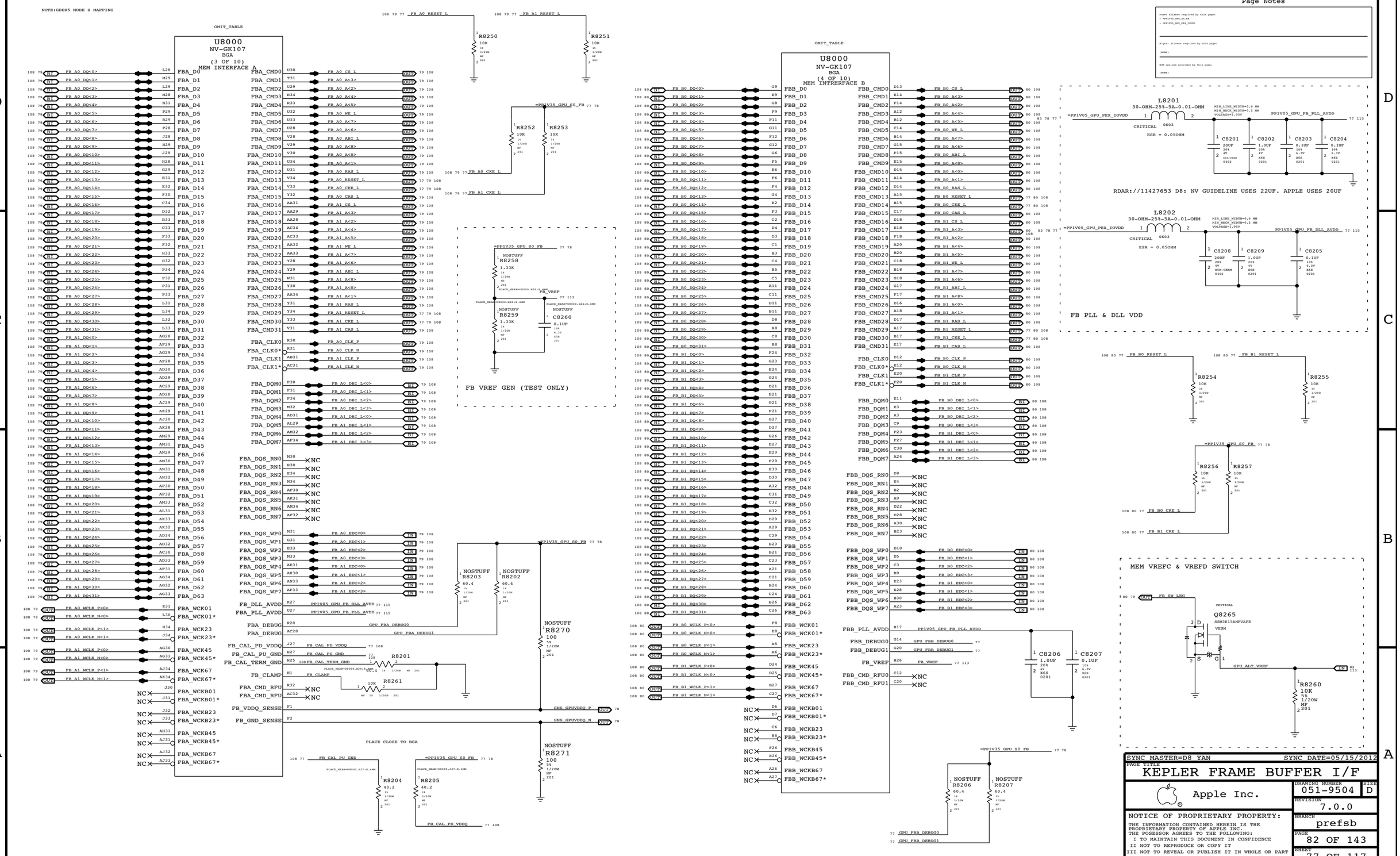
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 81 OF 143

SHEET 76 OF 117



GPU POWER ALIAS

80 79 76	=PP1V35_GPU_FBVDDQ	=PP1V35_S0_GPU_FBVDDQ	6
77	=PP1V35_GPU_S0_FB		
83 76	=PPVCORE_GPU	=PPVCORE_S0_GPU	6 51
83 77	=PP1V05_GPU_PEX_IOVDD	=PP1V05_S0_GPU_PEX_IOVDD	6
83 82 81 75	=PP3V3_GPU_VDD33	=PP3V3_S0_GPU_VDD33	6
81	=PP3V3_GPU_MISC	=PP3V3_S0_GPU_MISC	6
83 81	=PP1V05_GPU_PEX_PLLVDD	=PP1V05_S0_GPU_PEX_PLLVDD	6
81	=PP1V05_GPU_IFPCD_IOVDD	=PP1V05_S0_GPU_IFPCD_IOVDD	6
81	=PP1V05_GPU_IFPEF_IOVDD	=PP1V05_S0_GPU_IFPEF_IOVDD	6
81	=PP3V3_GPU_IFPX_PLLVDD	=PP3V3_S0_GPU_IFPX_PLLVDD	6

GPU SIGNAL & SENSE ALIAS

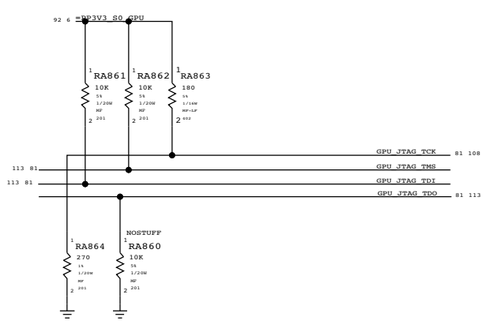
83	GPU_VDD_SENSE	VSNS_GPU_VDD MAKE_BASE=TRUE	92 110
83	GPU_GND_SENSE	VSNS_GPU_VSS MAKE_BASE=TRUE	92 110
77	SNS_GPUVDDQ_P	VSNS_FBVDDQ_P MAKE_BASE=TRUE	95 110
77	SNS_GPUVDDQ_N	VSNS_FBVDDQ_N MAKE_BASE=TRUE	95 110
81	GPU_TDIODE_P	NC_GPU_TDIODEP MAKE_BASE=TRUE NO_TEST=TRUE	
81	GPU_TDIODE_N	NC_GPU_TDIODEN MAKE_BASE=TRUE NO_TEST=TRUE	

GPU VIDS ALIAS (VR VID0 IS TIED LOW)

110 82	GPU_VCORE_VID0	RA850 0 5% 1/20W MF 201	REG_GPUCORE_VID1 92 110
110 82	GPU_VCORE_VID1	RA851 0 5% 1/20W MF 201	REG_GPUCORE_VID2 92 110
110 82	GPU_VCORE_VID2	RA852 0 5% 1/20W MF 201	REG_GPUCORE_VID3 92 110
110 82	GPU_VCORE_VID3	RA853 0 5% 1/20W MF 201	REG_GPUCORE_VID4 92 110
110 82	GPU_VCORE_VID4	RA854 0 5% 1/20W MF 201	REG_GPUCORE_VID5 92 110
110 82	GPU_VCORE_VID5	RA855 0 5% 1/20W MF 201	REG_GPUCORE_VID6 92 110

THESE POWER ALIASES ARE CRAETED TO MATCH D8 GK104

PU/PD IS BASED ON RECOMMENDATION FROM NV FOR NVDIA GPU JTAG DEBUGGER



SYNC MASTER=D8 YAN SYNC DATE=04/09/2012

PAGE TITLE
GPU SIGNAL & POWER ALIASES

Apple Inc.

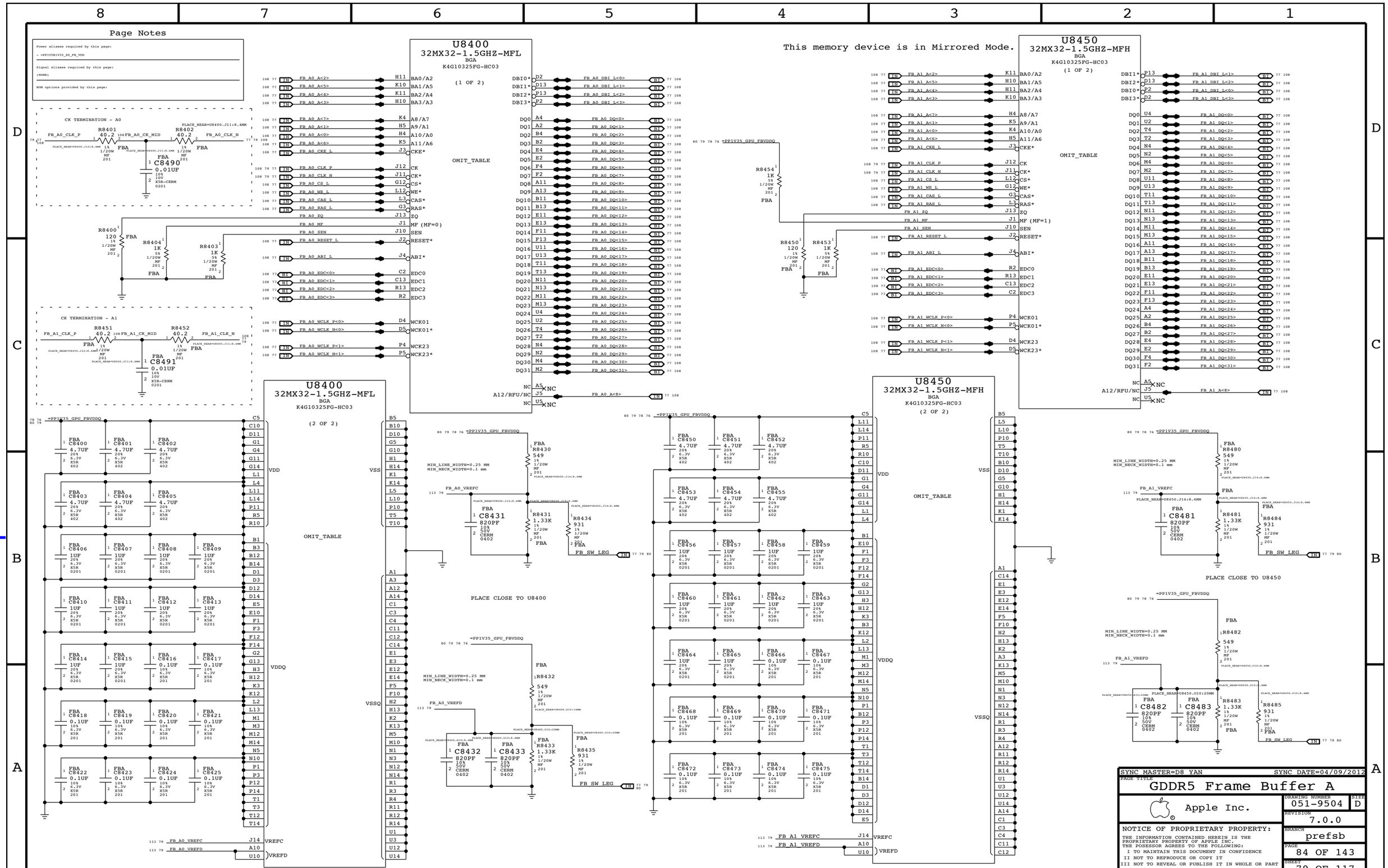
DRAWING NUMBER 051-9504 SIZE D

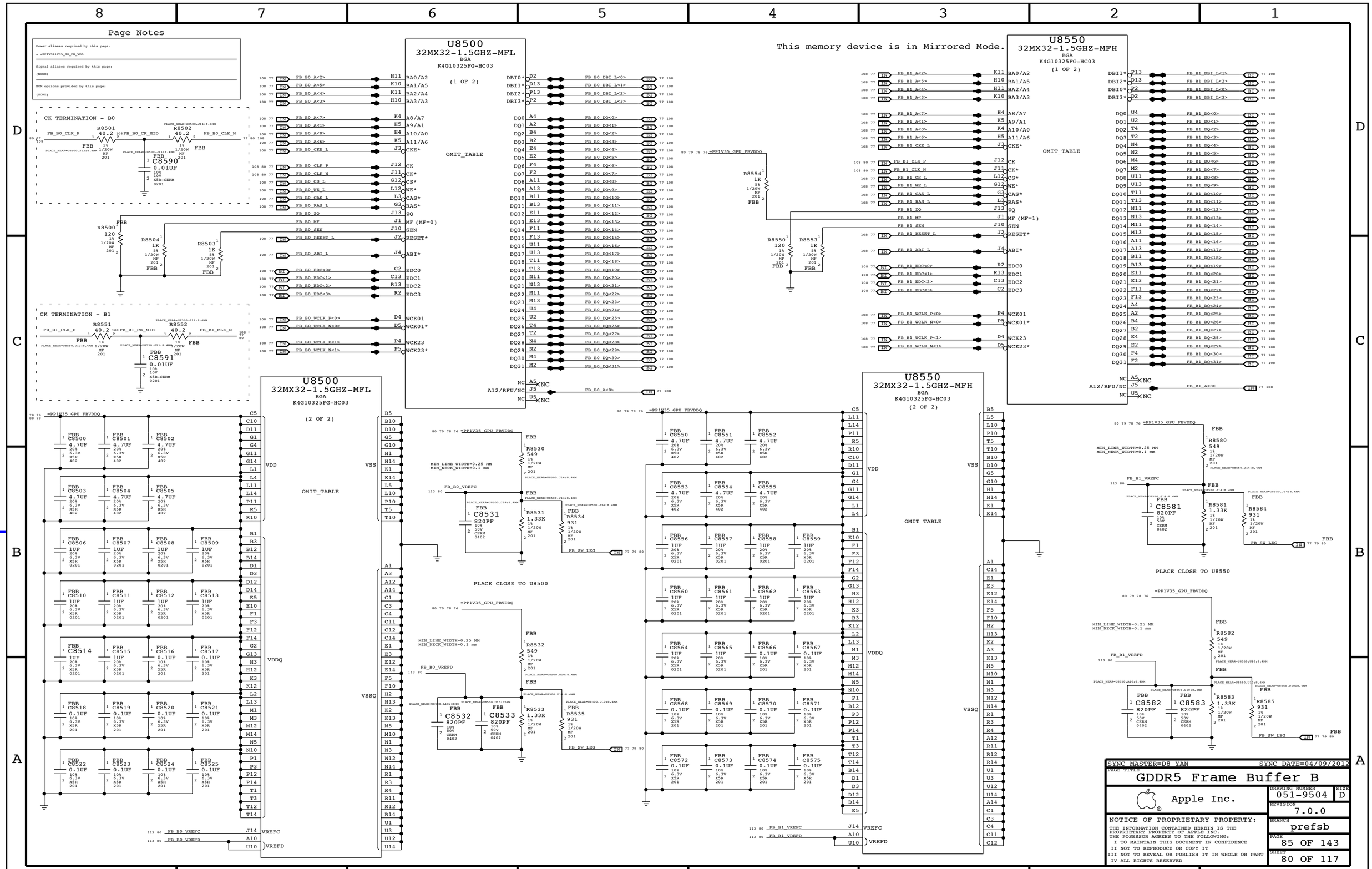
REVISION 7.0.0

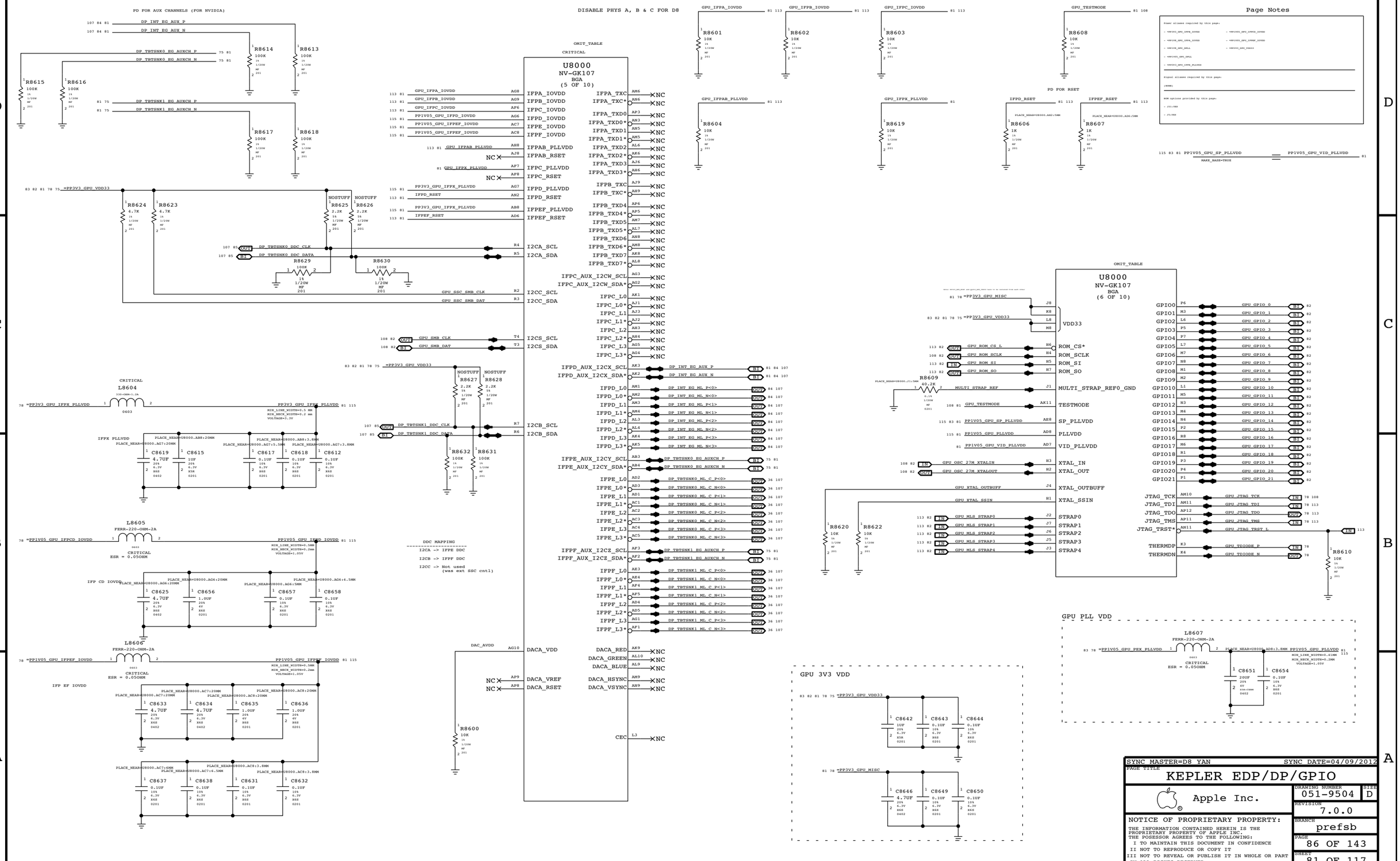
BRANCH prefsb

PAGE 83 OF 143

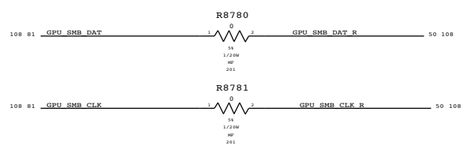
SHEET 78 OF 117



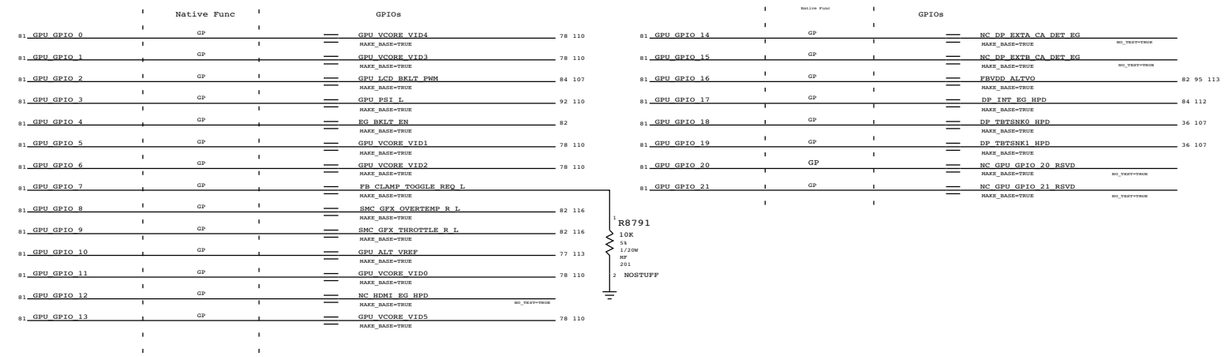




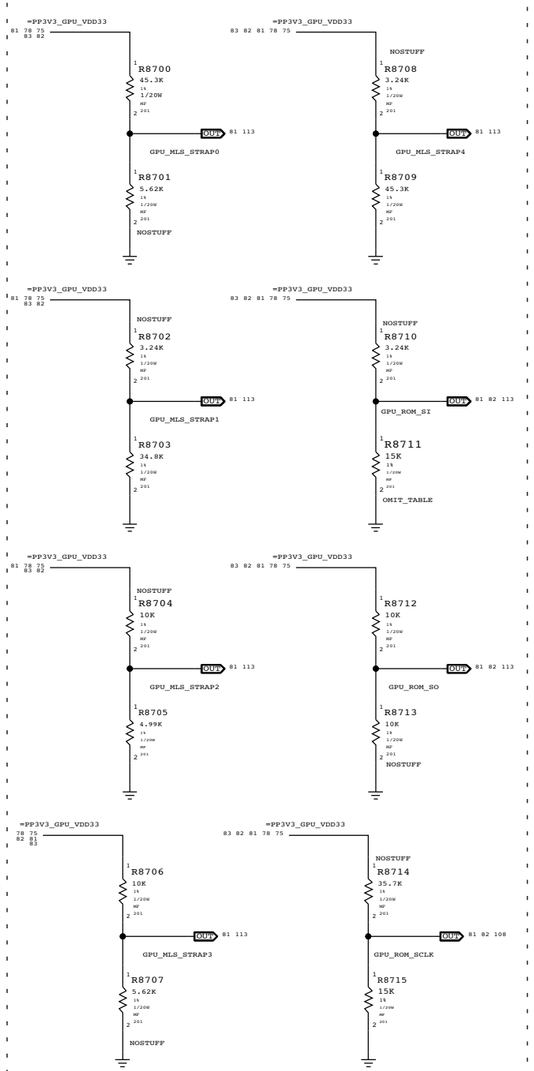
ISOLATION R's for GPU Int Temp Sense



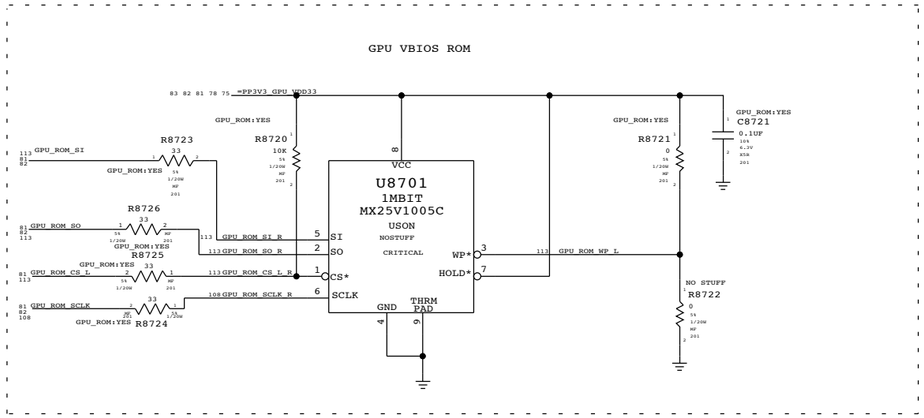
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0175	1	RES,MF,20.0k ,1,1/20W,0201	R8711		FB:BOTH_SAMSUNG
118S0105	1	RES,MF,15.0k ,1,1/20W,0201	R8711		FB:BOTH_HYNIX



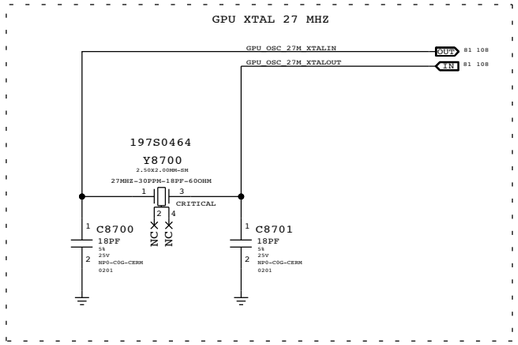
CONFIG STRAPS - MLPS USE 1% FOR ACCURACY



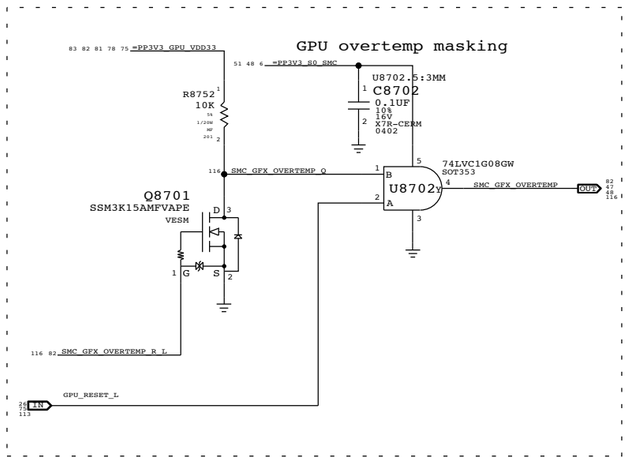
GPU VBIOS ROM

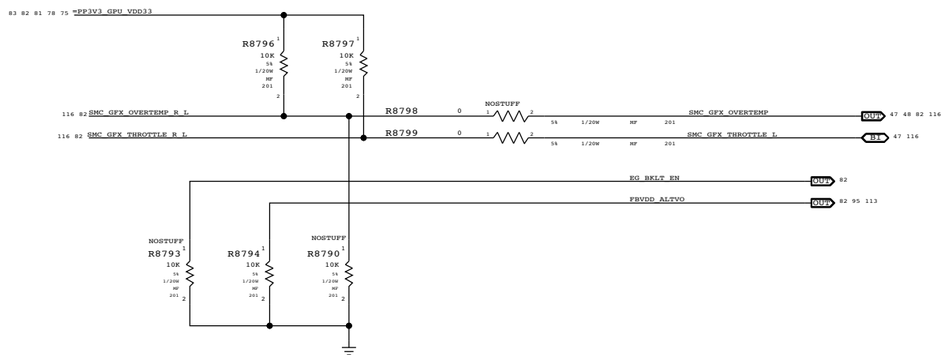


GPU XTAL 27 MHZ

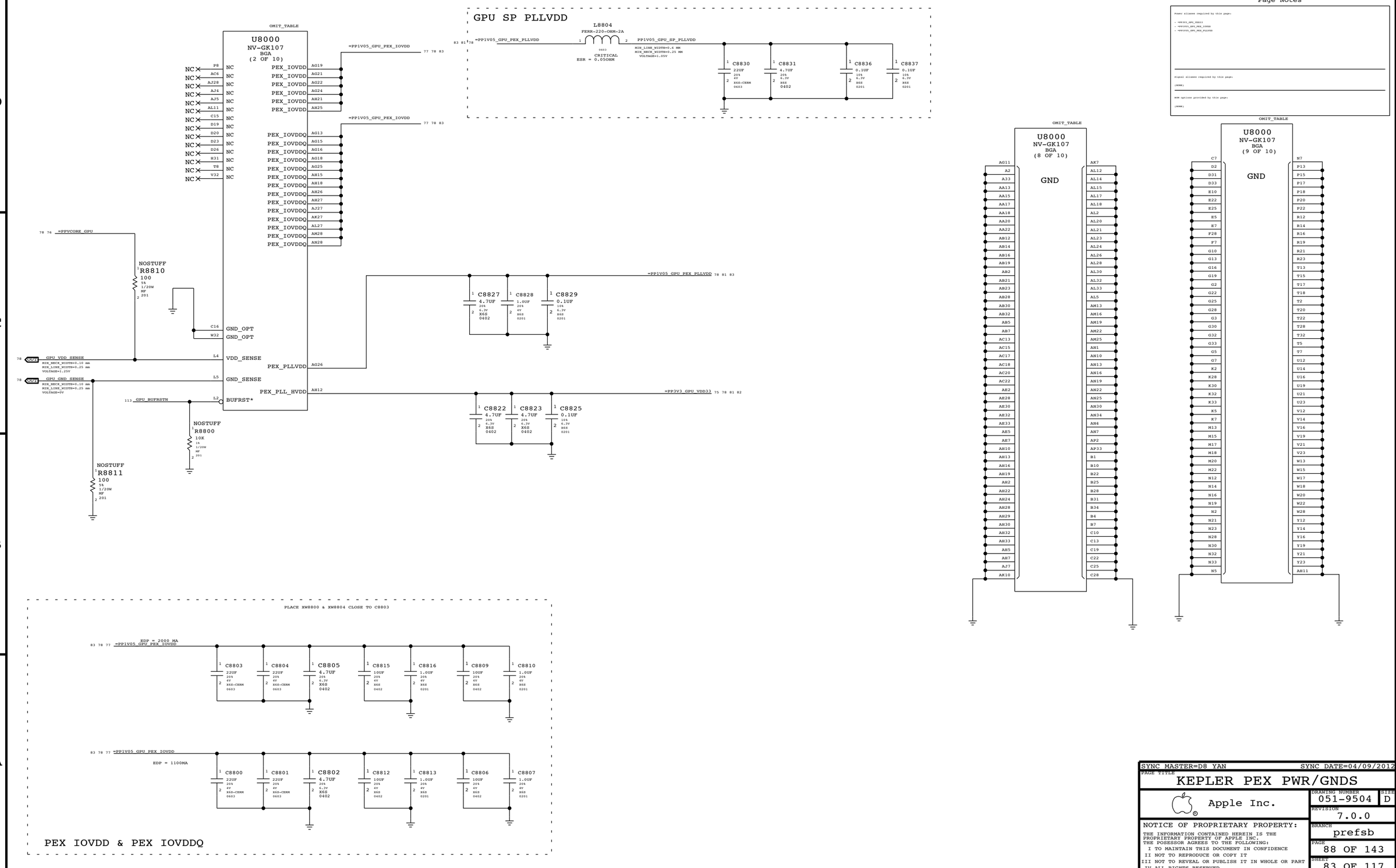


GPU overtemp masking





SYNC MASTER=D8 YAN	SYNC DATE=07/27/2012
PAGE TITLE: KEPLER GPIOS,CLK & STRAPS	
Apple Inc.	DRAWING NUMBER: 051-9504 SIZE: D
	REVISION: 7.0.0
	BRANCH: prefsb
	PAGE: 87 OF 143
	SHEET: 82 OF 117



SYNC MASTER=D8 YAN SYNC DATE=04/09/2012

PAGE TITLE

KEPLER PEX PWR/GNDS

Apple Inc.

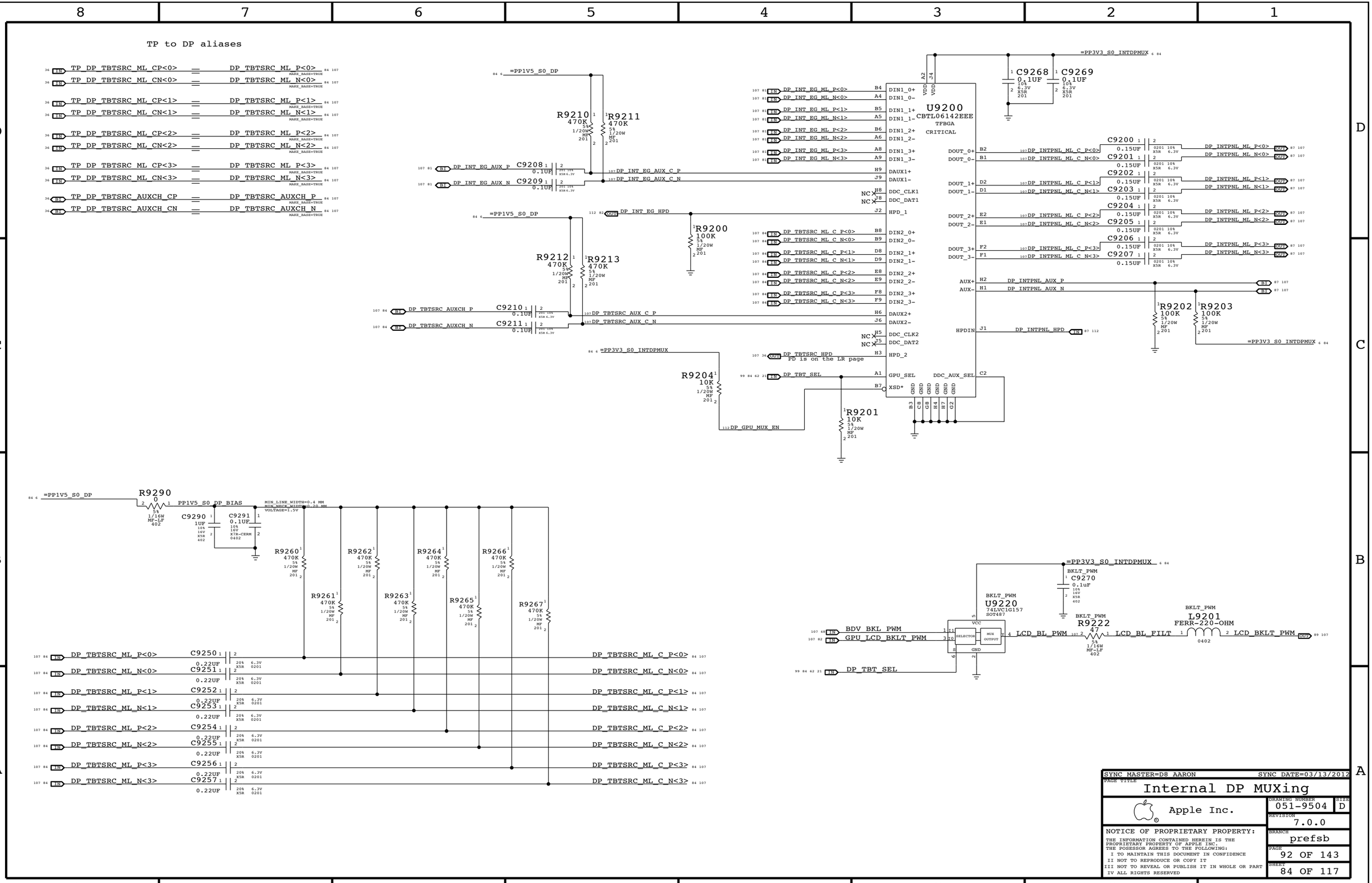
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

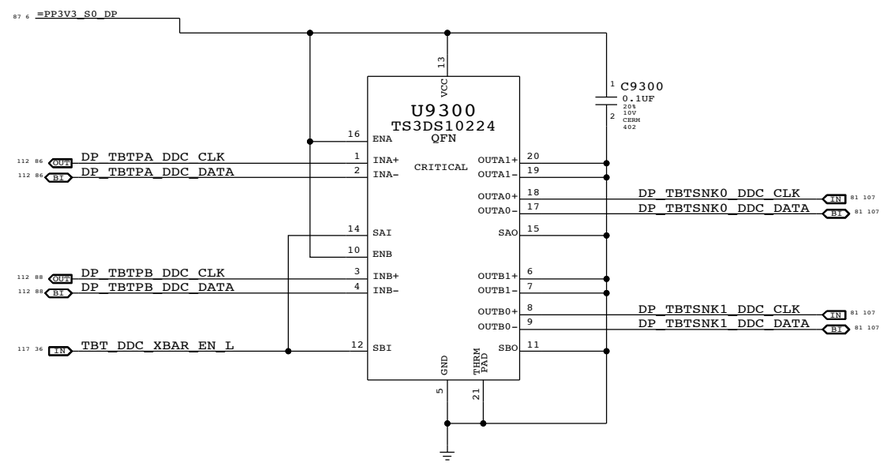
BRANCH prefsb

PAGE 88 OF 143

SHEET 83 OF 117



Dual-Port Host DDC Crossbar



SYNC MASTER=D7_MLB SYNC DATE=03/15/2012

PAGE TITLE

TBT DDC Crossbar

Apple Inc.

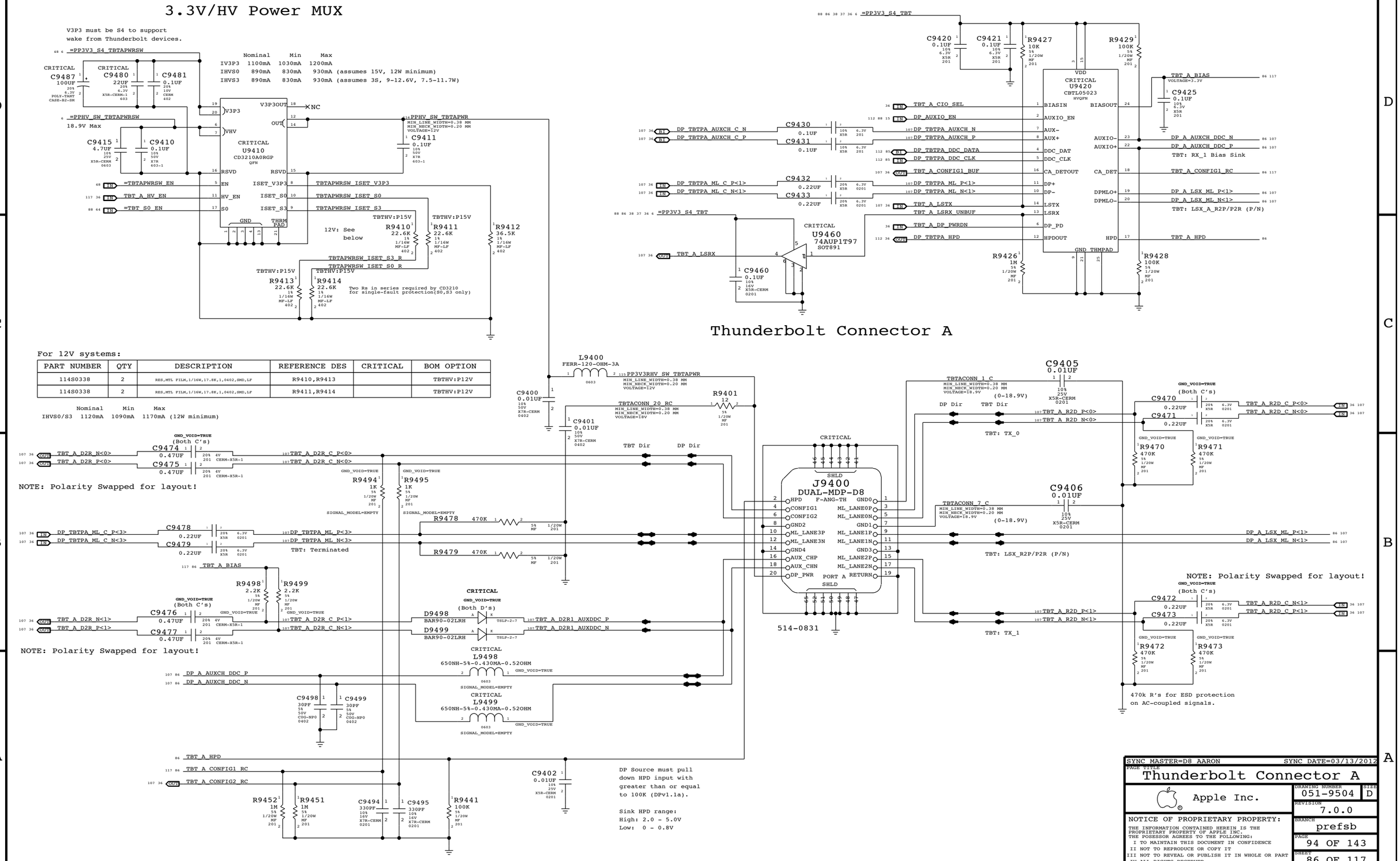
DRAWING NUMBER 051-9504 SIZE D

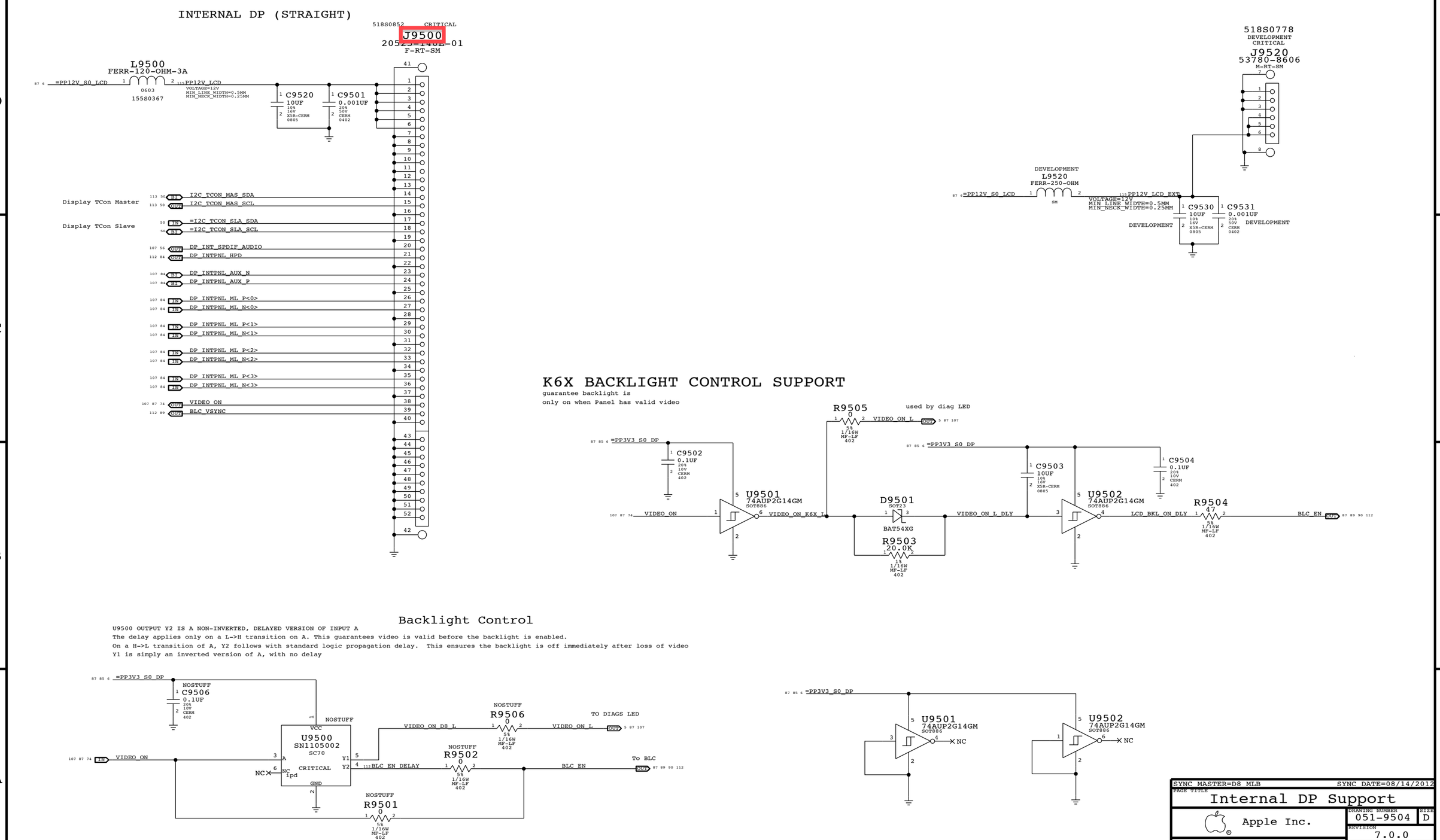
REVISION 7.0.0

BRANCH prefsb

PAGE 93 OF 143

SHEET 85 OF 117





SYNC MASTER=D8 MLB SYNC DATE=08/14/2012

PAGE TITLE
Internal DP Support

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

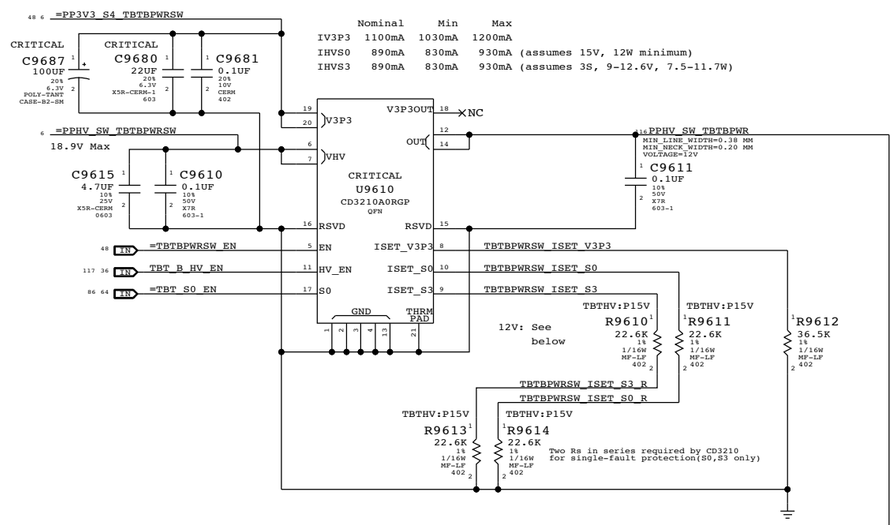
PAGE 95 OF 143

SHEET 87 OF 117

3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max
IV3P3	1100mA	1030mA	1200mA
IHVS0	890mA	830mA	930mA (assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA (assumes 3S, 9-12.6V, 7.5-11.7W)

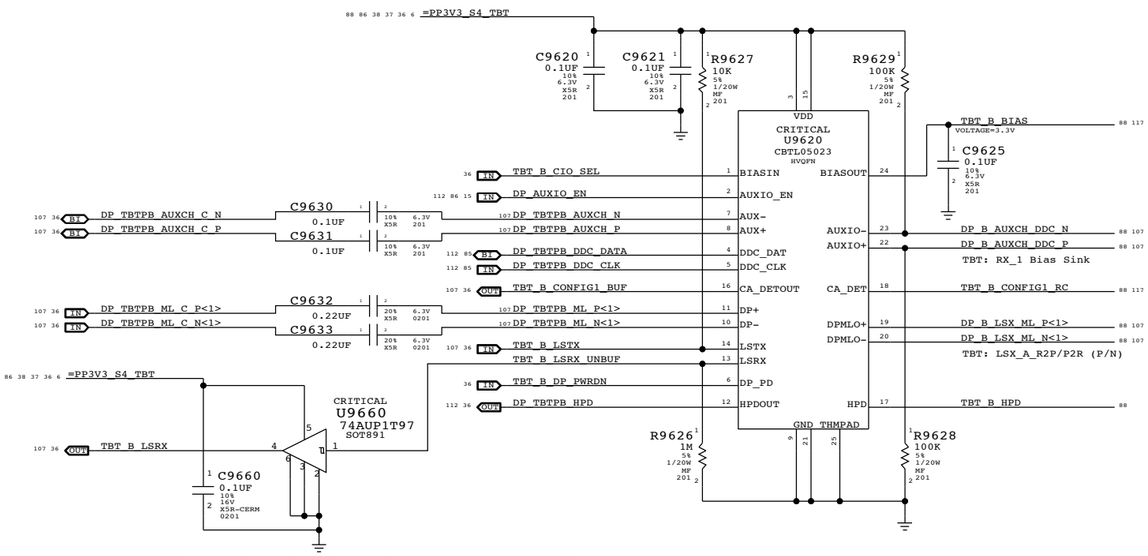


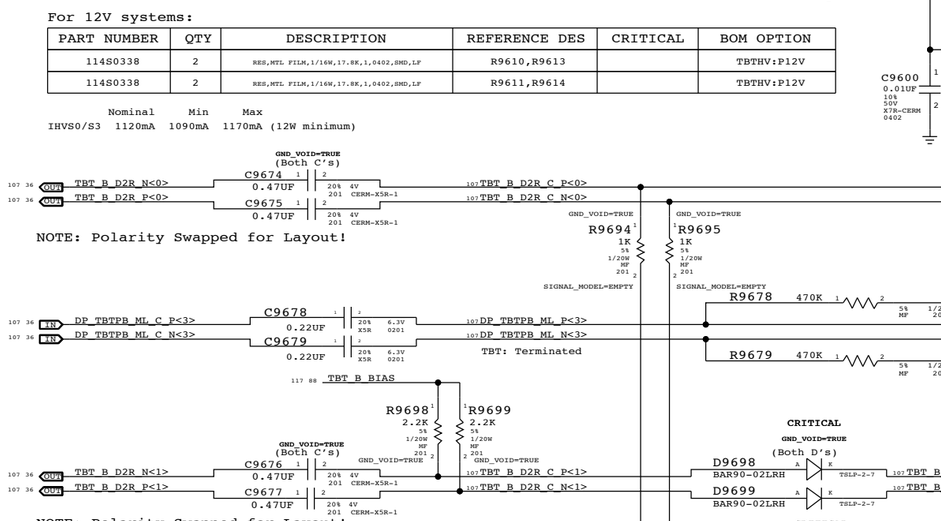
For 12V systems:

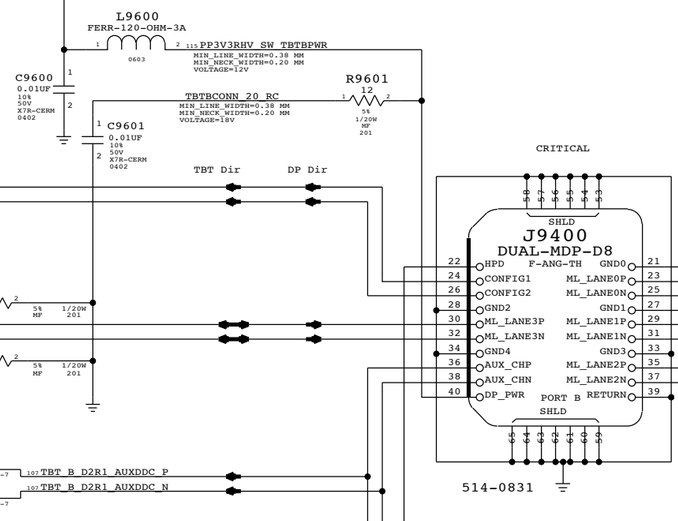
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9610,R9613		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9611,R9614		TBTHV:P12V

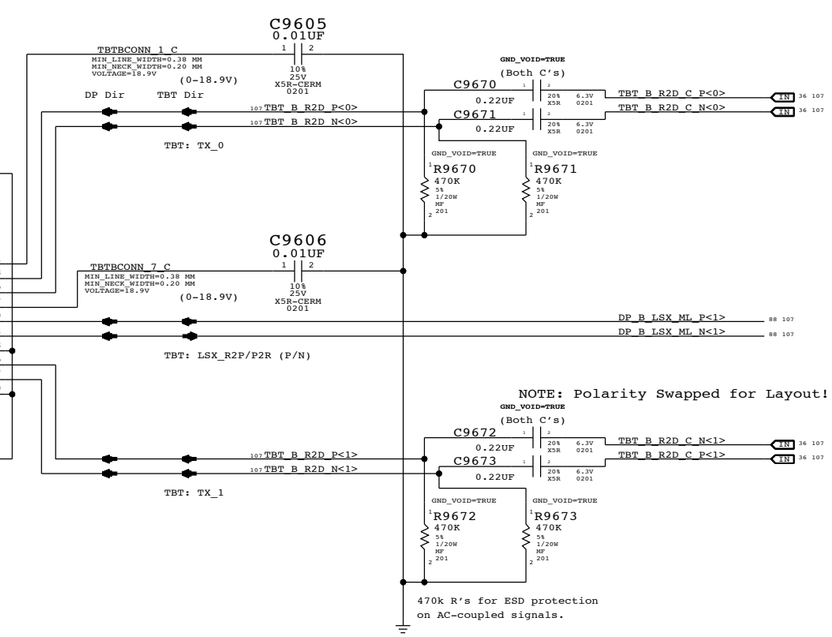
	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector B









DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

SYNC MASTER=D8 AARON SYNC DATE=03/13/2012

PAGE TITLE: Thunderbolt Connector B

Apple Inc.

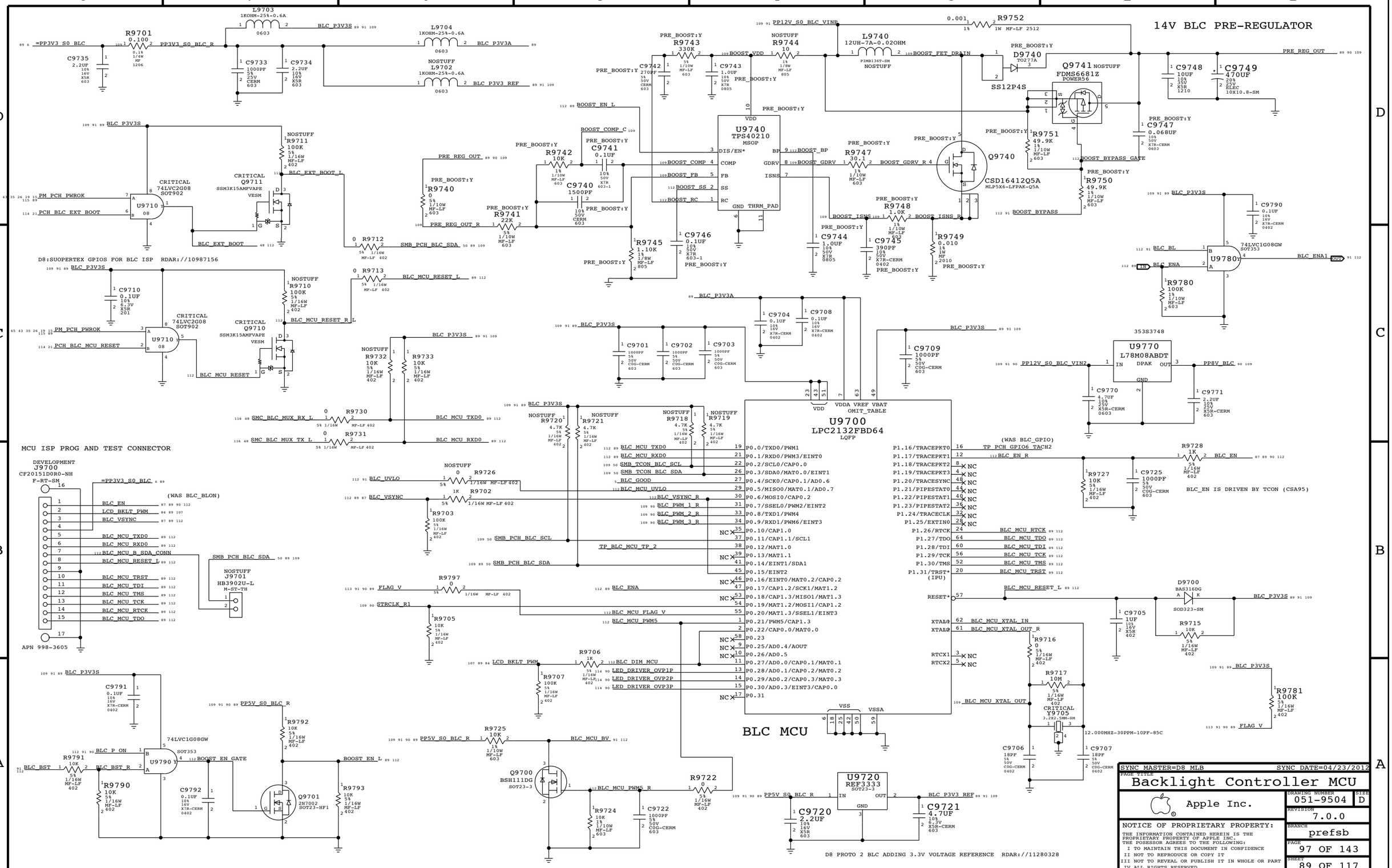
DRAWING NUMBER: 051-9504 SIZE: D

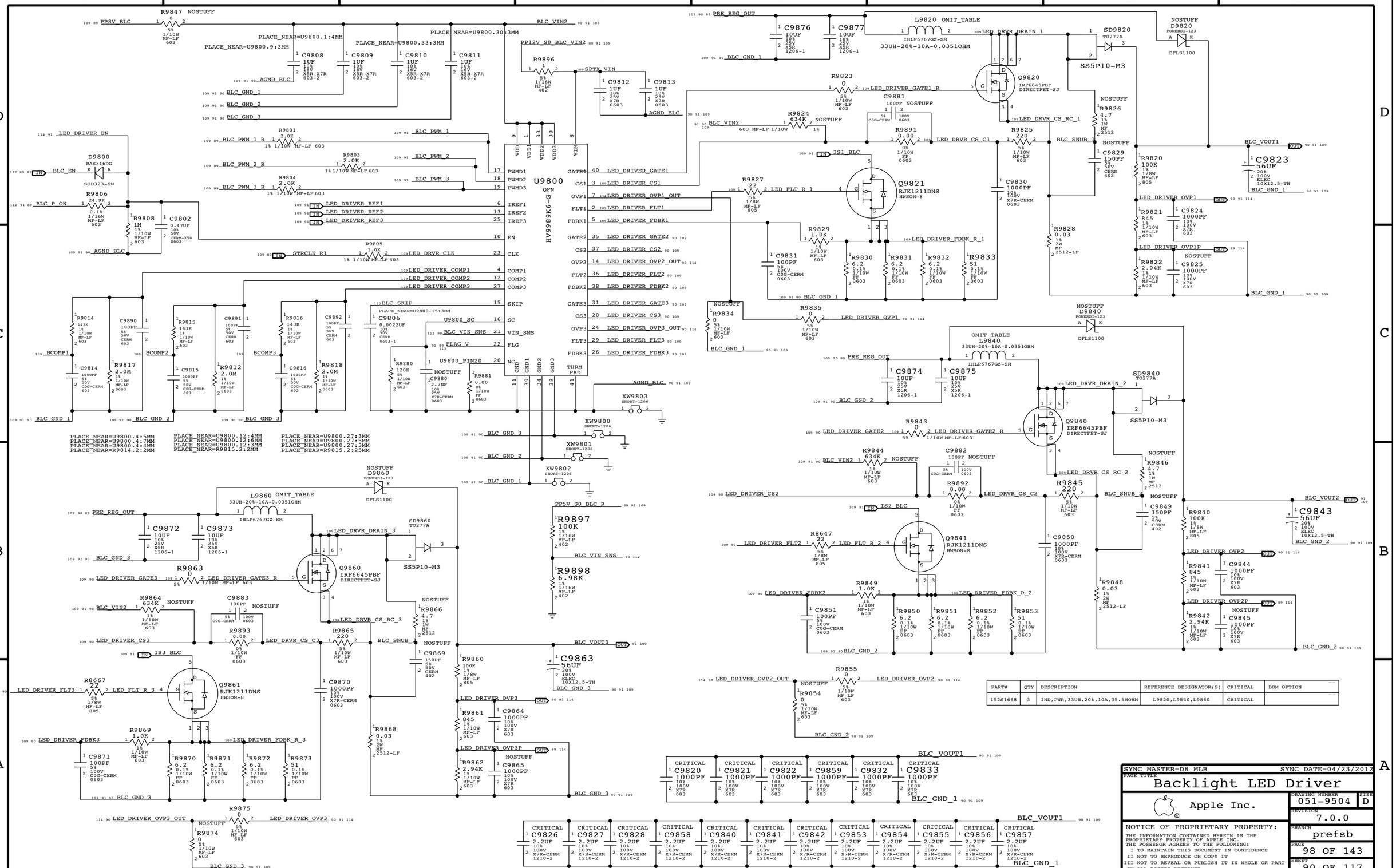
REVISION: 7.0.0

BRANCH: prefsb

PAGE: 96 OF 143

SHEET: 88 OF 117





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1668	3	IND,PWR,33UH,20%,10A,35.5MOHM	L9820,L9840,L9860	CRITICAL	

SYNC MASTER=D8 MLB SYNC DATE=04/23/2012

PAGE TITLE
Backlight LED Driver

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

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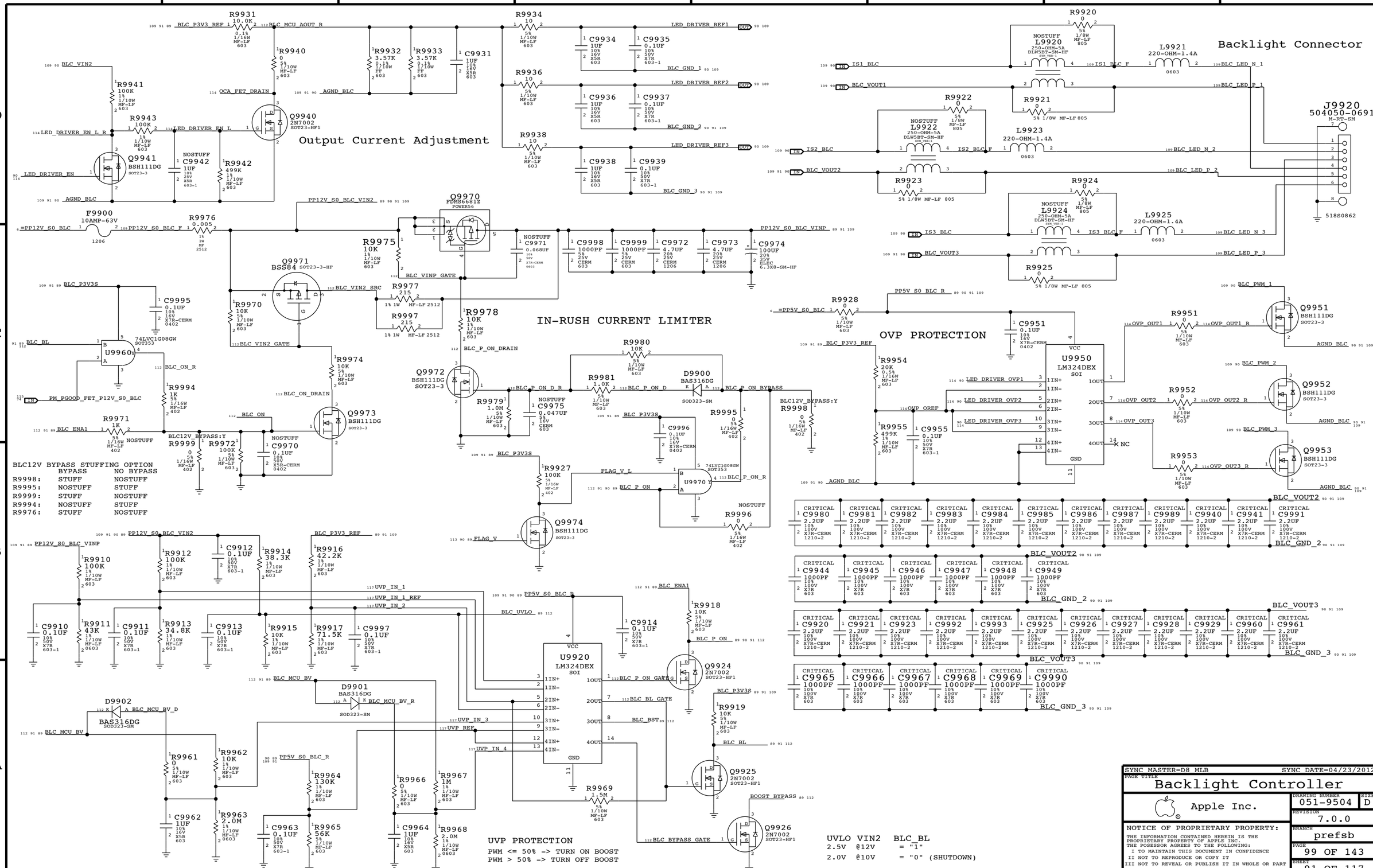
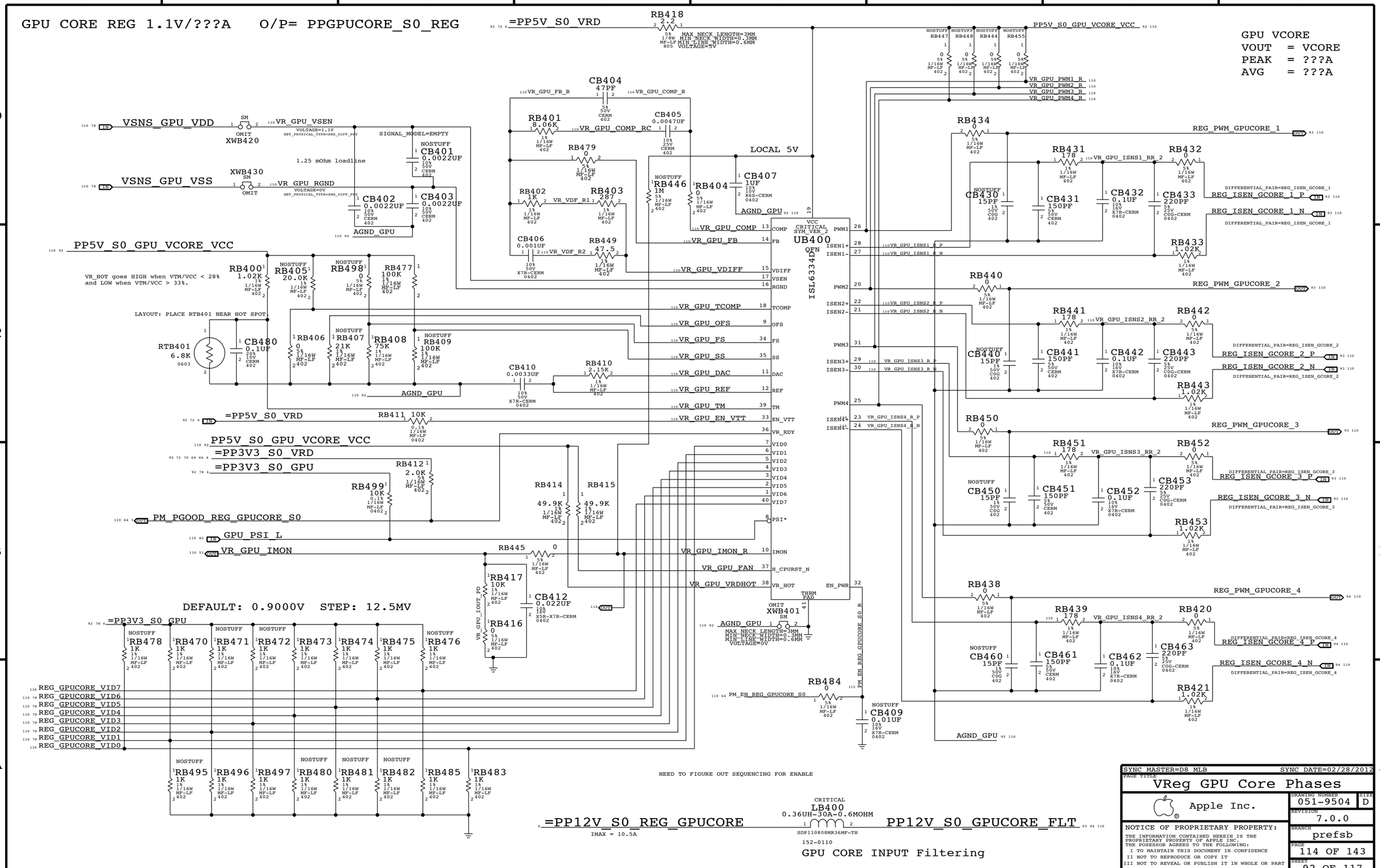
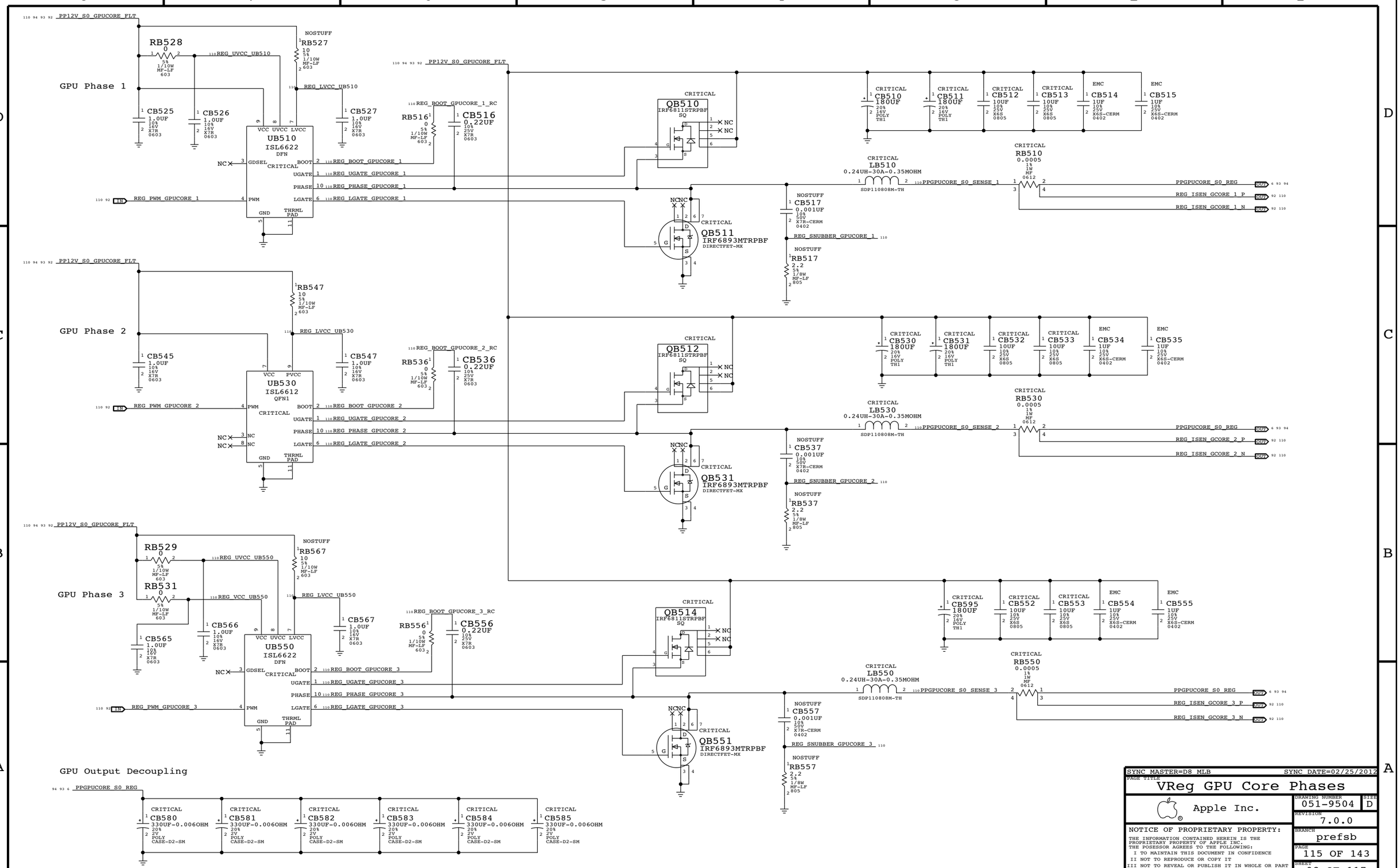
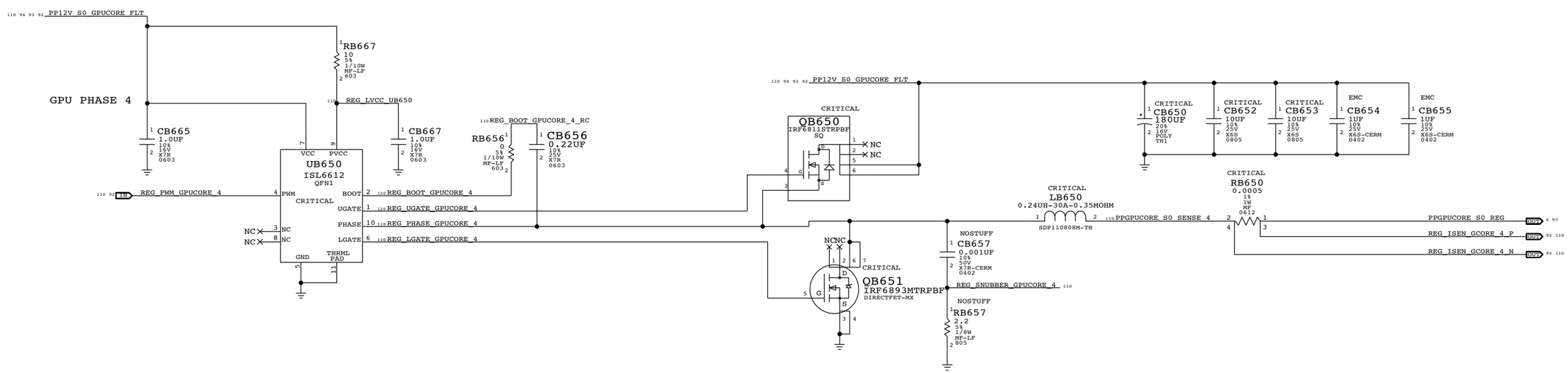
PAGE 98 OF 143

SHEET 90 OF 117









SYNC MASTER=D8 MLB SYNC DATE=02/06/2012

PAGE TITLE

VREG GPU CORE PHASE 4

Apple Inc.

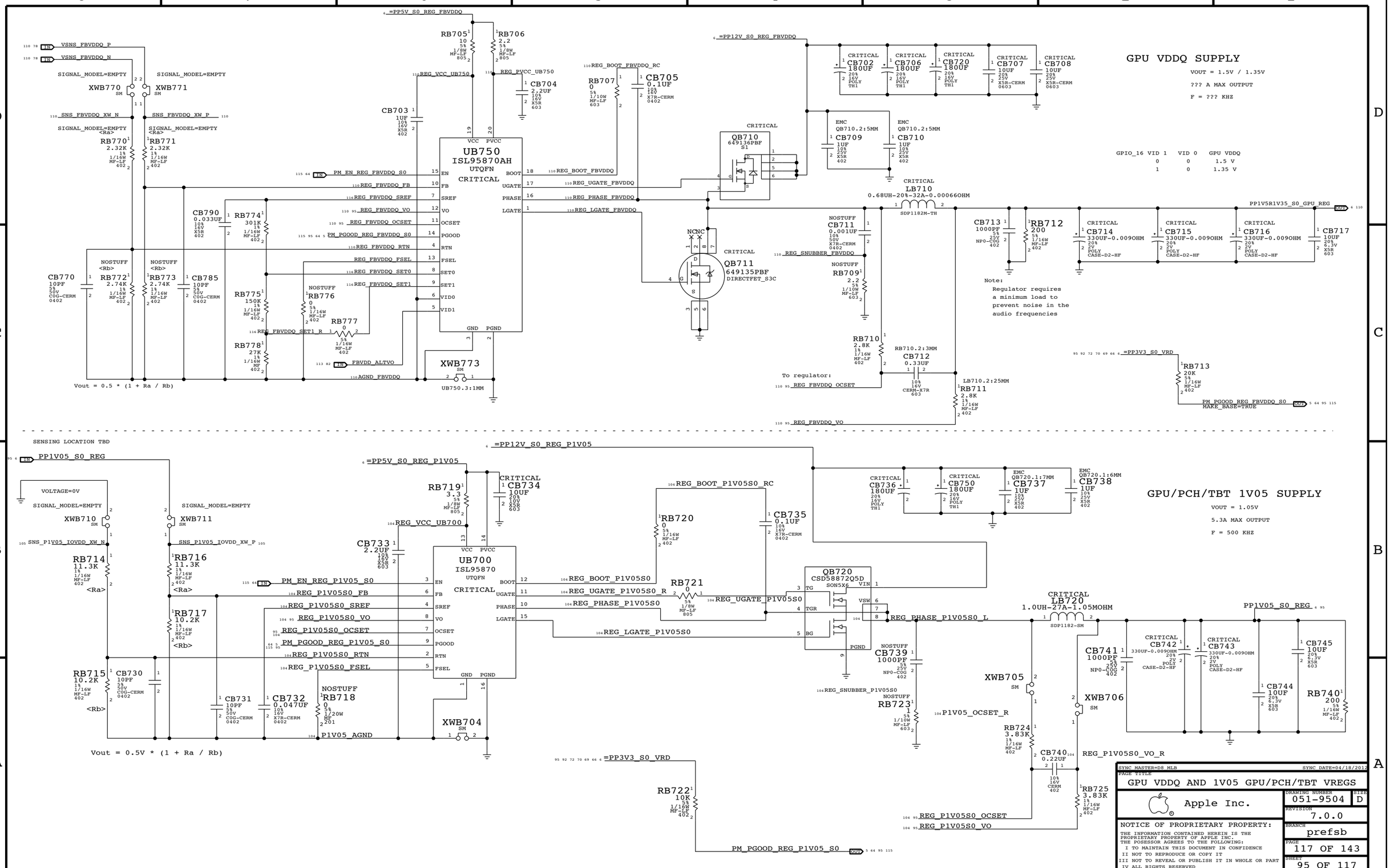
DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 116 OF 143

SHEET 94 OF 117



D8 BOARD SPECIFIC PHYSICAL AND SPACING CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,BGA_TBT	MM	16.2

General Physical Rule Definitions

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	0.1 MM	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
34_OHM_SE	*	Y	0.185 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	ISL5,ISL8	Y	0.205 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
34_OHM_SE	TOP,BOTTOM	Y	0.220 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
39_OHM_SE	*	Y	0.150 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	ISL5,ISL8	Y	0.165 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
39_OHM_SE	TOP,BOTTOM	Y	0.175 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
42_OHM_SE	*	Y	0.130 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	ISL5,ISL8	Y	0.145 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
42_OHM_SE	TOP,BOTTOM	Y	0.155 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	*	Y	0.115 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	ISL5,ISL8	Y	0.126 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	*	Y	0.090 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	ISL5,ISL8	Y	0.100 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD
50_OHM_SE	TOP,BOTTOM	Y	0.105 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.075 MM	0.075 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	ISL5,ISL8	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
68_OHM_DIFF	*	Y	0.171 MM	0.085 MM	=STANDARD	0.130 MM	0.1 MM
68_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.085 MM	=STANDARD	0.150 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.136 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.141 MM	0.085 MM	=STANDARD	0.185 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.121 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.085 MM	=STANDARD	0.190 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.109 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.086 MM	0.085 MM	=STANDARD	0.200 MM	0.1 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.090 MM	0.085 MM	=STANDARD	0.230 MM	0.1 MM

Compensation Physical Rule Definition

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
COMP_SE	*	Y	0.305 MM	0.105 MM	3 MM	=STANDARD	=STANDARD

NOTE: line width based on 12 mil recommendation
NOTE: neck width based on 4 mil recommendation

BGA

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BGA_P1MM	*	=STANDARD	?

Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_ISO	*	=STANDARD	8000
GND_P2MM	*	=2:1_SPACING	1000
PWR_P2MM	*	=2:1_SPACING	1100

GENERIC

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GENERIC_ISO	*	=1:1_SPACING	?
PM_ISO	*	=1:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PM	*	*	PM_ISO
PM	GND	*	DEFAULT

BGA Area Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM

General Spacing Definitions

Default

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

Fixed and Dielectric

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
1X_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1X_DIELECTRIC	ISL3,ISL10	0.101 MM	?
1X_DIELECTRIC	*	0.076 MM	?

Board Stack-up

FINISHED BOARD THICKNESS: 1.94 MM

	Top	Signal	0.5 oz (Cu plated)
		Prepreg	0.071 MM
	2	Plane	1 oz
		Core	0.101 MM
	3	Signal	0.5 oz
		Prepreg	0.115 MM
	4	Plane	1 oz
		Core	0.076 MM
	5	Signal	0.5 oz
		Prepreg	0.380 MM
	6	Plane	1 oz
		Core	0.076 MM
	7	Plane	1 oz
		Prepreg	0.380 MM
	8	Signal	0.5 oz
		Core	0.076 MM
	9	Plane	1 oz
		Prepreg	0.115 MM
	10	Signal	0.5 oz
		Core	0.101 MM
	11	Plane	1 oz
		Prepreg	0.071 MM
	Btm	Signal	0.5 oz (Cu plated)

SYNC MASTER=D8 KOSECOFF SYNC DATE=03/19/2012

PAGE TITLE
D8 RULE DEFINITIONS

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DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 120 OF 143
SHEET 96 OF 117

DDR3

DDR3-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_34S	*	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	=STANDARD	=STANDARD
DDR_34S	BOTTOM	=34_OHM_SE	=34_OHM_SE	=34_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_39S	*	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=39_OHM_SE	=STANDARD	=STANDARD
DDR_42S	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=STANDARD	=STANDARD
DDR_42S	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	=STANDARD	=STANDARD
DDR_42S_D	*	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	=42_OHM_SE	0.1016 MM	0.1016 MM
DDR_42S_D	BOTTOM	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_42S_D	ISL5,ISL8	=42_OHM_SE	=55_OHM_SE	=55_OHM_SE	2.0 MM	0.1016 MM	0.1016 MM
DDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
DDR_68D	*	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF	=68_OHM_DIFF

Minimum diff spacing is 4 mil
Table 3-5, Intel Doc# 473718

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
POWER_DDR_P4MM	*	Y	0.400 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_DDR_PHY	*	POWER_DDR_P4MM
DDR_CLK_PHY	*	DDR_68D
DDR_CTRL_PHY	*	DDR_39S
DDR_CMD_PHY	*	DDR_34S
DDR_DQ_PHY	*	DDR_42S
DDR_DQS_PHY	*	DDR_42S_D

DDR3-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DDR_CLK_ISO	TOP,BOTTOM	=5.5X_DIELECTRIC	?
DDR_CLK_ISO	ISL3,ISL10	=4.9X_DIELECTRIC	?
DDR_CLK_ISO	*	=6.5X_DIELECTRIC	?
DDR_CTRL_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CTRL_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CTRL_ISO	*	=5.3X_DIELECTRIC	?
DDR_CTRL2CTRL	TOP,BOTTOM	=3.0X_DIELECTRIC	?
DDR_CTRL2CTRL	ISL3,ISL10	=2.6X_DIELECTRIC	?
DDR_CTRL2CTRL	*	=3.5X_DIELECTRIC	?
DDR_CMD_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_CMD_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_CMD_ISO	*	=5.3X_DIELECTRIC	?
DDR_CMD2CMD	TOP,BOTTOM	=2.3X_DIELECTRIC	?
DDR_CMD2CMD	ISL3,ISL10	=2.0X_DIELECTRIC	?
DDR_CMD2CMD	*	=2.7X_DIELECTRIC	?
DDR_DATA_ISO	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_DATA_ISO	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_DATA_ISO	*	=5.3X_DIELECTRIC	?
DDR_DQ2DQ	TOP,BOTTOM	=3.2X_DIELECTRIC	900
DDR_DQ2DQ	ISL3,ISL10	=2.8X_DIELECTRIC	900
DDR_DQ2DQ	*	=3.8X_DIELECTRIC	900
DDR_DQ2DQS	TOP,BOTTOM	=3.7X_DIELECTRIC	?
DDR_DQ2DQS	ISL3,ISL10	=3.3X_DIELECTRIC	?
DDR_DQ2DQS	*	=4.4X_DIELECTRIC	?
DDR_BL2BL	TOP,BOTTOM	=4.5X_DIELECTRIC	?
DDR_BL2BL	ISL3,ISL10	=4.0X_DIELECTRIC	?
DDR_BL2BL	*	=5.3X_DIELECTRIC	?
DDR_CH2CH	TOP,BOTTOM	=9.1X_DIELECTRIC	?
DDR_CH2CH	ISL3,ISL10	=8.2X_DIELECTRIC	?
DDR_CH2CH	*	=10.9X_DIELECTRIC	?
CMD2DATA_ISO	TOP,BOTTOM	=7X_DIELECTRIC	?
CMD2DATA_ISO	ISL3,ISL10	=5X_DIELECTRIC	?
CMD2DATA_ISO	*	=5X_DIELECTRIC	?

DDR3 Power-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_DDR_ISO	*	=4.3X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER_DDR	*	*	POWER_DDR_ISO

Constraints

Clocks: CK[3:0], CK#[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CLK	*	*	DDR_CLK_ISO

Control: CS#[3:0], CKE[3:0], ODT[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CTRL	*	*	DDR_CTRL_ISO
DDR_CTRL	DDR_CTRL	*	DDR_CTRL2CTRL

Command: MA[15:0], RAS#, CAS#, WE# BS[2:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR_CMD	*	*	DDR_CMD_ISO
DDR_CMD	DDR_CMD	*	DDR_CMD2CMD
DDR_CMD	DDR_A_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_A_DQS*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQ_BYTE*	*	CMD2DATA_ISO
DDR_CMD	DDR_B_DQS*	*	CMD2DATA_ISO

Data: DQS[7:0], DQS#[7:0], DQ[63:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
DDR_A_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_A_DQS*	*	*	DDR_DATA_ISO	
DDR_B_DQ_BYTE*	*	*	DDR_DATA_ISO	
DDR_B_DQS*	*	*	DDR_DATA_ISO	
DDR_*_DQ_BYTE*	=SAME	*	DDR_DQ2DQ	See Note (3)
DDR_A_DQ_BYTE*	DDR_A_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_A_DQ_BYTE*	DDR_A_DQ_BYTE*	*	DDR_BL2BL	See Note (3)
DDR_B_DQ_BYTE*	DDR_B_DQS*	*	DDR_DQ2DQS	See Note (1)
DDR_B_DQ_BYTE*	DDR_B_DQ_BYTE*	*	DDR_BL2BL	
DDR_A_*	DDR_B_*	*	DDR_CH2CH	See Note (2)

Note (1):
Deliberately set DQ to DQS spacing to 3:1 to avoid adding complexity to contraints, even though it can be less. Only one rule per channel is needed by trading off a little space.

Note (2):
Intel suggests 25 mil (0.65 mm) spacing for via to channel, and via to pad to two different channels. DDR3 draws about 20 mA per trace with edge rates in the 100s of ps. The main coupling mechanism is capacitive. A 0.65 mm spacing is used for power nets, which draw far more current (inductive coupling however). These rules are far too conservative. To meet these rules, the spacing must be applied to the net.

Note (3):
In order for the constraints DDR_*_DQ_BYTE* to =SAME so win out over DDR_{A,B}_DQ_BYTE* to DDR_{A,B}_DQ_BYTE* so that the small intra-bytelane spacing is used, the spacing rule DDR_DQ2DQ must have a weight greater than DDR_BL2BL.

DDR3

Electrical Contraint Set		Physical	Spacing		
Channel A					
117	DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<1..0>	12 29
117	DDR_A_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<1..0>	12 29
125	DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_P<3..2>	12 30
125	DDR_A_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_A_CLK_N<3..2>	12 30
118	DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<1..0>	12 29
118	DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<1..0>	12 29
118	DDR_A_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<1..0>	12 29
124	DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CKE<3..2>	12 30
124	DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_CS_L<3..2>	12 30
124	DDR_A_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_A_ODT<3..2>	12 30
118	DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_A<15..0>	12 29 30
118	DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_BA<2..0>	12 29 30
118	DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_RAS_L	12 29 30
118	DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_CAS_L	12 29 30
118	DDR_A_CMD	DDR_CMD_PHY	DDR_CMD	MEM_A_WE_L	12 29 30
119	DDR_A_DQ_BYTE0	DDR_DQ_PHY	DDR_A_DQ_BYTE0	MEM_A_DQ<7..0>	12 33
119	DDR_A_DQ_BYTE1	DDR_DQ_PHY	DDR_A_DQ_BYTE1	MEM_A_DQ<15..8>	12 33
119	DDR_A_DQ_BYTE2	DDR_DQ_PHY	DDR_A_DQ_BYTE2	MEM_A_DQ<23..16>	12 33
119	DDR_A_DQ_BYTE3	DDR_DQ_PHY	DDR_A_DQ_BYTE3	MEM_A_DQ<31..24>	12 33
119	DDR_A_DQ_BYTE4	DDR_DQ_PHY	DDR_A_DQ_BYTE4	MEM_A_DQ<39..32>	12 33
119	DDR_A_DQ_BYTE5	DDR_DQ_PHY	DDR_A_DQ_BYTE5	MEM_A_DQ<47..40>	12 33
119	DDR_A_DQ_BYTE6	DDR_DQ_PHY	DDR_A_DQ_BYTE6	MEM_A_DQ<55..48>	12 33
119	DDR_A_DQ_BYTE7	DDR_DQ_PHY	DDR_A_DQ_BYTE7	MEM_A_DQ<63..56>	12 33
119	DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_P<0>	12 33
119	DDR_A_DQS0	DDR_DQS_PHY	DDR_A_DQS0	MEM_A_DQS_N<0>	12 33
119	DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_P<1>	12 33
119	DDR_A_DQS1	DDR_DQS_PHY	DDR_A_DQS1	MEM_A_DQS_N<1>	12 33
120	DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_P<2>	12 33
120	DDR_A_DQS2	DDR_DQS_PHY	DDR_A_DQS2	MEM_A_DQS_N<2>	12 33
120	DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_P<3>	12 33
120	DDR_A_DQS3	DDR_DQS_PHY	DDR_A_DQS3	MEM_A_DQS_N<3>	12 33
120	DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_P<4>	12 33
120	DDR_A_DQS4	DDR_DQS_PHY	DDR_A_DQS4	MEM_A_DQS_N<4>	12 33
120	DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_P<5>	12 33
120	DDR_A_DQS5	DDR_DQS_PHY	DDR_A_DQS5	MEM_A_DQS_N<5>	12 33
120	DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_P<6>	12 33
120	DDR_A_DQS6	DDR_DQS_PHY	DDR_A_DQS6	MEM_A_DQS_N<6>	12 33
121	DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_P<7>	12 33
121	DDR_A_DQS7	DDR_DQS_PHY	DDR_A_DQS7	MEM_A_DQS_N<7>	12 33
Channel B					
121	DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<1..0>	12 31
121	DDR_B_CLK0	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<1..0>	12 31
125	DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_P<3..2>	12 32
125	DDR_B_CLK1	DDR_CLK_PHY	DDR_CLK	MEM_B_CLK_N<3..2>	12 32
121	DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<1..0>	12 31
121	DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<1..0>	12 31
121	DDR_B_CTRL0	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<1..0>	12 31
125	DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CKE<3..2>	12 32
125	DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_CS_L<3..2>	12 32
125	DDR_B_CTRL1	DDR_CTRL_PHY	DDR_CTRL	MEM_B_ODT<3..2>	12 32
121	DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_A<15..0>	12 31 32
121	DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_BA<2..0>	12 31 32
121	DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_RAS_L	12 31 32
122	DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_CAS_L	12 31 32
122	DDR_B_CMD	DDR_CMD_PHY	DDR_CMD	MEM_B_WE_L	12 31 32
122	DDR_B_DQ_BYTE0	DDR_DQ_PHY	DDR_B_DQ_BYTE0	MEM_B_DQ<7..0>	12 33
122	DDR_B_DQ_BYTE1	DDR_DQ_PHY	DDR_B_DQ_BYTE1	MEM_B_DQ<15..8>	12 33
122	DDR_B_DQ_BYTE2	DDR_DQ_PHY	DDR_B_DQ_BYTE2	MEM_B_DQ<23..16>	12 33
122	DDR_B_DQ_BYTE3	DDR_DQ_PHY	DDR_B_DQ_BYTE3	MEM_B_DQ<31..24>	12 33
122	DDR_B_DQ_BYTE4	DDR_DQ_PHY	DDR_B_DQ_BYTE4	MEM_B_DQ<39..32>	12 33
122	DDR_B_DQ_BYTE5	DDR_DQ_PHY	DDR_B_DQ_BYTE5	MEM_B_DQ<47..40>	12 33
122	DDR_B_DQ_BYTE6	DDR_DQ_PHY	DDR_B_DQ_BYTE6	MEM_B_DQ<55..48>	12 33
122	DDR_B_DQ_BYTE7	DDR_DQ_PHY	DDR_B_DQ_BYTE7	MEM_B_DQ<63..56>	12 33
123	DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_P<0>	12 33
123	DDR_B_DQS0	DDR_DQS_PHY	DDR_B_DQS0	MEM_B_DQS_N<0>	12 33
123	DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_P<1>	12 33
123	DDR_B_DQS1	DDR_DQS_PHY	DDR_B_DQS1	MEM_B_DQS_N<1>	12 33
123	DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_P<2>	12 33
123	DDR_B_DQS2	DDR_DQS_PHY	DDR_B_DQS2	MEM_B_DQS_N<2>	12 33
123	DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_P<3>	12 33
123	DDR_B_DQS3	DDR_DQS_PHY	DDR_B_DQS3	MEM_B_DQS_N<3>	12 33
123	DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_P<4>	12 33
123	DDR_B_DQS4	DDR_DQS_PHY	DDR_B_DQS4	MEM_B_DQS_N<4>	12 33
124	DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_P<5>	12 33
124	DDR_B_DQS5	DDR_DQS_PHY	DDR_B_DQS5	MEM_B_DQS_N<5>	12 33
124	DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_P<6>	12 33
124	DDR_B_DQS6	DDR_DQS_PHY	DDR_B_DQS6	MEM_B_DQS_N<6>	12 33
124	DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_P<7>	12 33
124	DDR_B_DQS7	DDR_DQS_PHY	DDR_B_DQS7	MEM_B_DQS_N<7>	12 33
Reset					
124		DDR_50S	CPU	MEM_RESET_L	28 29 30 31 32

SYNC MASTER=D8 KOSECOFF SYNC DATE=03/19/2012

PAGE TITLE
DDR3 Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 121 OF 143
SHEET 97 OF 117

PCI EXPRESS

PCIe-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_PHY	*	PCIE_80D
CLK_PCIE_PHY	*	PCIE_90D
COMP_PCIE_PHY	*	COMP_SE

PCIe-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_ISO	*	=4X_DIELECTRIC	?
CLK_PCIE_ISO	*	=5:1_SPACING	?
COMP_PCIE_ISO	*	=4:1_SPACING	?

PCIe Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
4.2.1	80	85	16	15.75	PCIe Gen2, PCIe Gen3, DMI

PCIe and DMI Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
4-5	50	50	15	15.75	PCIe. Impedance inferred from Table 4-7.
4-7	50	50	8	15.75	DMI. Numbers based on Intel stack-up.

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	PCIE_ISO
CLK_PCIE	*	*	CLK_PCIE_ISO
COMP_PCIE	*	*	COMP_PCIE_ISO

PCIe (PCH)

Electrical Contraint Set	Physical	Spacing			
x1 AirPort					
T59 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_P	NO_TEST=TRUE	35
T60 PCIE_GEN2_R2D_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_R2D_N	NO_TEST=TRUE	35
T61	PCIE_PHY	PCIE	PCIE_AP_R2D_C_P	NO_TEST=TRUE	18 35
T62	PCIE_PHY	PCIE	PCIE_AP_R2D_C_N	NO_TEST=TRUE	18 35
T63 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_P	NO_TEST=TRUE	18 35
T64 PCIE_GEN2_D2R_CONN_AP	PCIE_PHY	PCIE	PCIE_AP_D2R_N	NO_TEST=TRUE	18 35
T65 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_P		18 35
T66 PCIE_REF_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_AP_N		18 35
x1 Caesar IV					
T67 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_P	NO_TEST=TRUE	39
T68 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_ENET_R2D_N	NO_TEST=TRUE	39
T69	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_P	NO_TEST=TRUE	18 39
T70	PCIE_PHY	PCIE	PCIE_ENET_R2D_C_N	NO_TEST=TRUE	18 39
T71 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_P	NO_TEST=TRUE	18 39
T72 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_ENET_D2R_N	NO_TEST=TRUE	18 39
T73	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_P	NO_TEST=TRUE	39
T74	PCIE_PHY	PCIE	PCIE_ENET_D2R_C_N	NO_TEST=TRUE	39
T75 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_P		18 39
T76 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_ENET_N		18 39

PCIE (PCH - TBT)

Electrical Contraint Set	Physical	Spacing			
x4 Thunderbolt					
T577 PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<2..0>	NO_TEST=TRUE	36
T578 PCIE_GEN2_R2D_PINV	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<2..0>	NO_TEST=TRUE	36
T620 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_P<3>	NO_TEST=TRUE	36
T619 PCIE_GEN2_R2D	PCIE_PHY	PCIE	PCIE_TBT_R2D_N<3>	NO_TEST=TRUE	36
T579	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_P<3..0>	NO_TEST=TRUE	18 36
T580	PCIE_PHY	PCIE	PCIE_TBT_R2D_C_N<3..0>	NO_TEST=TRUE	18 36
T581	PCIE_PHY	PCIE	PCIE_TBT_D2R_P<3..0>	NO_TEST=TRUE	18 36
T582	PCIE_PHY	PCIE	PCIE_TBT_D2R_N<3..0>	NO_TEST=TRUE	18 36
T583 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<1..0>	NO_TEST=TRUE	36
T584 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<1..0>	NO_TEST=TRUE	36
T621 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<2>	NO_TEST=TRUE	36
T622 PCIE_GEN2_D2R	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<2>	NO_TEST=TRUE	36
T623 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_P<3>	NO_TEST=TRUE	36
T624 PCIE_GEN2_D2R_PINV	PCIE_PHY	PCIE	PCIE_TBT_D2R_C_N<3>	NO_TEST=TRUE	36
T585 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_P		18 36
T586 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PCIE_CLK100M_TBT_N		18 36

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing			
x16 Graphics					
T446 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<15>	NO_TEST=TRUE	10 75
T447 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<15>	NO_TEST=TRUE	10 75
T448	PCIE_PHY	PCIE	PEG_R2D_C_P<15>	NO_TEST=TRUE	75
T449	PCIE_PHY	PCIE	PEG_R2D_C_N<15>	NO_TEST=TRUE	75
T450 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<15>	NO_TEST=TRUE	75
T451 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<15>	NO_TEST=TRUE	75
T452	PCIE_PHY	PCIE	PEG_D2R_C_P<15>	NO_TEST=TRUE	10 75
T453	PCIE_PHY	PCIE	PEG_D2R_C_N<15>	NO_TEST=TRUE	10 75
T454 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<14>	NO_TEST=TRUE	10 75
T455 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<14>	NO_TEST=TRUE	10 75
T456	PCIE_PHY	PCIE	PEG_R2D_C_P<14>	NO_TEST=TRUE	75
T457	PCIE_PHY	PCIE	PEG_R2D_C_N<14>	NO_TEST=TRUE	75
T458 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<14>	NO_TEST=TRUE	75
T459 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<14>	NO_TEST=TRUE	75
T460	PCIE_PHY	PCIE	PEG_D2R_C_P<14>	NO_TEST=TRUE	10 75
T461	PCIE_PHY	PCIE	PEG_D2R_C_N<14>	NO_TEST=TRUE	10 75
T462 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<13>	NO_TEST=TRUE	10 75
T463 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<13>	NO_TEST=TRUE	10 75
T464	PCIE_PHY	PCIE	PEG_R2D_C_P<13>	NO_TEST=TRUE	75
T465	PCIE_PHY	PCIE	PEG_R2D_C_N<13>	NO_TEST=TRUE	75
T466 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<13>	NO_TEST=TRUE	75
T467 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<13>	NO_TEST=TRUE	75
T468	PCIE_PHY	PCIE	PEG_D2R_C_P<13>	NO_TEST=TRUE	10 75
T469	PCIE_PHY	PCIE	PEG_D2R_C_N<13>	NO_TEST=TRUE	10 75
T470 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<12>	NO_TEST=TRUE	10 75
T471 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<12>	NO_TEST=TRUE	10 75
T472	PCIE_PHY	PCIE	PEG_R2D_C_P<12>	NO_TEST=TRUE	75
T473	PCIE_PHY	PCIE	PEG_R2D_C_N<12>	NO_TEST=TRUE	75
T474 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<12>	NO_TEST=TRUE	75
T475 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<12>	NO_TEST=TRUE	75
T476	PCIE_PHY	PCIE	PEG_D2R_C_P<12>	NO_TEST=TRUE	10 75
T477	PCIE_PHY	PCIE	PEG_D2R_C_N<12>	NO_TEST=TRUE	10 75
T478 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<11>	NO_TEST=TRUE	10 75
T479 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<11>	NO_TEST=TRUE	10 75
T480	PCIE_PHY	PCIE	PEG_R2D_C_P<11>	NO_TEST=TRUE	75
T481	PCIE_PHY	PCIE	PEG_R2D_C_N<11>	NO_TEST=TRUE	75
T482 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<11>	NO_TEST=TRUE	75
T483 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<11>	NO_TEST=TRUE	75
T484	PCIE_PHY	PCIE	PEG_D2R_C_P<11>	NO_TEST=TRUE	10 75
T485	PCIE_PHY	PCIE	PEG_D2R_C_N<11>	NO_TEST=TRUE	10 75
T486 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<10>	NO_TEST=TRUE	10 75
T487 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<10>	NO_TEST=TRUE	10 75
T488	PCIE_PHY	PCIE	PEG_R2D_C_P<10>	NO_TEST=TRUE	75
T489	PCIE_PHY	PCIE	PEG_R2D_C_N<10>	NO_TEST=TRUE	75
T490 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<10>	NO_TEST=TRUE	75
T491 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<10>	NO_TEST=TRUE	75
T492	PCIE_PHY	PCIE	PEG_D2R_C_P<10>	NO_TEST=TRUE	10 75
T493	PCIE_PHY	PCIE	PEG_D2R_C_N<10>	NO_TEST=TRUE	10 75
T494 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<9>	NO_TEST=TRUE	10 75
T495 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<9>	NO_TEST=TRUE	10 75
T496	PCIE_PHY	PCIE	PEG_R2D_C_P<9>	NO_TEST=TRUE	75
T497	PCIE_PHY	PCIE	PEG_R2D_C_N<9>	NO_TEST=TRUE	75
T498 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<9>	NO_TEST=TRUE	75
T499 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<9>	NO_TEST=TRUE	75
T500	PCIE_PHY	PCIE	PEG_D2R_C_P<9>	NO_TEST=TRUE	10 75
T501	PCIE_PHY	PCIE	PEG_D2R_C_N<9>	NO_TEST=TRUE	10 75
T502 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<8>	NO_TEST=TRUE	10 75
T503 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<8>	NO_TEST=TRUE	10 75
T504	PCIE_PHY	PCIE	PEG_R2D_C_P<8>	NO_TEST=TRUE	75
T505	PCIE_PHY	PCIE	PEG_R2D_C_N<8>	NO_TEST=TRUE	75
T506 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<8>	NO_TEST=TRUE	75
T507 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<8>	NO_TEST=TRUE	75
T508	PCIE_PHY	PCIE	PEG_D2R_C_P<8>	NO_TEST=TRUE	10 75
T509	PCIE_PHY	PCIE	PEG_D2R_C_N<8>	NO_TEST=TRUE	10 75

PCIe (CPU)

Electrical Contraint Set	Physical	Spacing			
x16 Graphics					
T509 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<7>	NO_TEST=TRUE	10 75
T508 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<7>	NO_TEST=TRUE	10 75
T507	PCIE_PHY	PCIE	PEG_R2D_C_P<7>	NO_TEST=TRUE	75
T506	PCIE_PHY	PCIE	PEG_R2D_C_N<7>	NO_TEST=TRUE	75
T505 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<7>	NO_TEST=TRUE	75
T504 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<7>	NO_TEST=TRUE	75
T511	PCIE_PHY	PCIE	PEG_D2R_C_P<7>	NO_TEST=TRUE	10 75
T510	PCIE_PHY	PCIE	PEG_D2R_C_N<7>	NO_TEST=TRUE	10 75
T513 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<6>	NO_TEST=TRUE	10 75
T512 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<6>	NO_TEST=TRUE	10 75
T515	PCIE_PHY	PCIE	PEG_R2D_C_P<6>	NO_TEST=TRUE	75
T514	PCIE_PHY	PCIE	PEG_R2D_C_N<6>	NO_TEST=TRUE	75
T503 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<6>	NO_TEST=TRUE	75
T501 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<6>	NO_TEST=TRUE	75
T517	PCIE_PHY	PCIE	PEG_D2R_C_P<6>	NO_TEST=TRUE	10 75
T516	PCIE_PHY	PCIE	PEG_D2R_C_N<6>	NO_TEST=TRUE	10 75
T527 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<5>	NO_TEST=TRUE	10 75
T526 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<5>	NO_TEST=TRUE	10 75
T529	PCIE_PHY	PCIE	PEG_R2D_C_P<5>	NO_TEST=TRUE	75
T528	PCIE_PHY	PCIE	PEG_R2D_C_N<5>	NO_TEST=TRUE	75
T524 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<5>	NO_TEST=TRUE	75
T525 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<5>	NO_TEST=TRUE	75
T532	PCIE_PHY	PCIE	PEG_D2R_C_P<5>	NO_TEST=TRUE	10 75
T531	PCIE_PHY	PCIE	PEG_D2R_C_N<5>	NO_TEST=TRUE	10 75
T530 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<4>	NO_TEST=TRUE	10 75
T529 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<4>	NO_TEST=TRUE	10 75
T536	PCIE_PHY	PCIE	PEG_R2D_C_P<4>	NO_TEST=TRUE	75
T535	PCIE_PHY	PCIE	PEG_R2D_C_N<4>	NO_TEST=TRUE	75
T534 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<4>	NO_TEST=TRUE	75
T533 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<4>	NO_TEST=TRUE	75
T538	PCIE_PHY	PCIE	PEG_D2R_C_P<4>	NO_TEST=TRUE	10 75
T537	PCIE_PHY	PCIE	PEG_D2R_C_N<4>	NO_TEST=TRUE	10 75
T543 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<3>	NO_TEST=TRUE	10 75
T542 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<3>	NO_TEST=TRUE	10 75
T541	PCIE_PHY	PCIE	PEG_R2D_C_P<3>	NO_TEST=TRUE	75
T540	PCIE_PHY	PCIE	PEG_R2D_C_N<3>	NO_TEST=TRUE	75
T547 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<3>	NO_TEST=TRUE	75
T546 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<3>	NO_TEST=TRUE	75
T549	PCIE_PHY	PCIE	PEG_D2R_C_P<3>	NO_TEST=TRUE	10 75
T548	PCIE_PHY	PCIE	PEG_D2R_C_N<3>	NO_TEST=TRUE	10 75
T545 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<2>	NO_TEST=TRUE	10 75
T544 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<2>	NO_TEST=TRUE	10 75
T553	PCIE_PHY	PCIE	PEG_R2D_C_P<2>	NO_TEST=TRUE	75
T552	PCIE_PHY	PCIE	PEG_R2D_C_N<2>	NO_TEST=TRUE	75
T551 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<2>	NO_TEST=TRUE	75
T550 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<2>	NO_TEST=TRUE	75
T557	PCIE_PHY	PCIE	PEG_D2R_C_P<2>	NO_TEST=TRUE	10 75
T556	PCIE_PHY	PCIE	PEG_D2R_C_N<2>	NO_TEST=TRUE	10 75
T555 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_P<1>	NO_TEST=TRUE	10 75
T554 PCIE_GEN3_R2D_PINV	PCIE_PHY	PCIE	PEG_R2D_N<1>	NO_TEST=TRUE	10 75
T559	PCIE_PHY	PCIE	PEG_R2D_C_P<1>	NO_TEST=TRUE	75
T558	PCIE_PHY	PCIE	PEG_R2D_C_N<1>	NO_TEST=TRUE	75
T563 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_P<1>	NO_TEST=TRUE	75
T562 PCIE_GEN3_D2R	PCIE_PHY	PCIE	PEG_D2R_N<1>	NO_TEST=TRUE	75
T561	PCIE_PHY	PCIE	PEG_D2R_C_P<1>	NO_TEST=TRUE	10 75
T560	PCIE_PHY	PCIE	PEG_D2R_C_N<1>	NO_TEST=TRUE	10 75
T566 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_P<0>	NO_TEST=TRUE	10 75
T565 PCIE_GEN3_R2D	PCIE_PHY	PCIE	PEG_R2D_N<0>	NO_TEST=TRUE	10 75
T568	PCIE_PHY	PCIE	PEG_R2D_C_P<0>	NO_TEST=TRUE	75
T567	PCIE_PHY	PCIE	PEG_R2D_C_N<0>	NO_TEST=TRUE	75
T564 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_P<0>	NO_TEST=TRUE	75
T563 PCIE_GEN3_D2R_PINV	PCIE_PHY	PCIE	PEG_D2R_N<0>	NO_TEST=TRUE	75
T570	PCIE_PHY	PCIE	PEG_D2R_C_P<0>	NO_TEST=TRUE	10 75
T569	PCIE_PHY	PCIE	PEG_D2R_C_N<0>	NO_TEST=TRUE	10 75
CPU PCIe Clocks					
T555 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_P	NO_TEST=TRUE	18 75
T556 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	PEG_CLK100M_N	NO_TEST=TRUE	18 75
CPU PCIe Compensation					
T570	COMP_PCIE_PHY	COMP_PCIE	CPU_PEG_COMP		10

SYNC MASTER=D8 AARON SYNC DATE=03/13/2012

PAGE TITLE

CPU PCIe Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 122 OF 143

SHEET 98 OF 117

DMI

DMI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DMI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DMI_PHY	*	DMI_85D

CPU Misc / FDI

CPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
COMP_FDI_SE	*	Y	0.3 MM	0.25 MM	3 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_PHY	*	CPU_50S
COMP_FDI_PHY	*	COMP_FDI_SE

CPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_ISO	*	=3:1_SPACING	?
COMP_FDI_ISO	*	=4:1_SPACING	?

FDI Compensation Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Table	Trace	Design	Iso	Design	Comments
6-4	10	11.81	-	15.75	Using PCIe guidelines

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU	*	*	CPU_ISO
COMP_FDI	*	*	COMP_FDI_ISO

XDP

XDP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
XDP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
XDP_PHY	*	XDP_50S

XDP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XDP_ISO	*	=2:1_SPACING	?
XDP_CLK_ISO	*	=4:1_SPACING	?

Desktop Debug Design Guide (Intel Doc# 430883)

Section	Imp	Design	Iso	Design	Comments
1.5	45-65	50	-	15.75	Isolation is for JTAG clocks. All signals default are 50 Ohm SE.

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XDP	*	*	XDP_ISO
CLK_JTAG	*	*	XDP_CLK_ISO
OBS_STROBE	*	*	XDP_CLK_ISO

DMI

Electrical Contraint Set	Physical	Spacing		
DMI				
B160 DMI_N2S	DMI_PHY	PCIE	DMI_N2S_P<3..0> NO_TEST=TRUE	10 19
B161 DMI_N2S	DMI_PHY	PCIE	DMI_N2S_N<3..0> NO_TEST=TRUE	10 19
B162 DMI_S2N	DMI_PHY	PCIE	DMI_S2N_P<3..0> NO_TEST=TRUE	10 19
B163 DMI_S2N	DMI_PHY	PCIE	DMI_S2N_N<3..0> NO_TEST=TRUE	10 19
B283 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_P	11 18
B284 PCIE_REF_CLK	CLK_PCIE_PHY	CLK_PCIE	DMI_CLK100M_CPU_N	11 18
DMI Compensation				
B171	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI_COMP	19
B272	COMP_PCIE_PHY	COMP_PCIE	PCH_DMI2RBIAS	19

CPU Misc.

Electrical Contraint Set	Physical	Spacing		
CPU Misc.				
B245	CPU_PHY	CPU	CPU_SKTOCC_L	11 64
B246	CPU_PHY	CPU	CPU_PROC_SEL	11 19
B236	CPU_PHY	CPU	CPU_CATERR_L	11 48
B255	CPU_PHY	CPU	CPU_PECI	11 21 47 48
B256	CPU_PHY	CPU	CPU_PROCHOT_L	11 47 48 66
B267	CPU_PHY	CPU	CPU_PROCHOT_R_L	11
B245	CPU_PHY	CPU	CPU_THRMTRIP_L	11 48
B240	CPU_PHY	CPU	CPU_RESET_L	11 26
B247	CPU_PHY	CPU	PLT_RESET_LS1V05_L	11
B232	CPU_PHY	CPU	PM_SYNC	11 19
B235	CPU_PHY	CPU	CPU_PWRGD	11 21 25 28
B260	CPU_PHY	CPU	PM_MEM_PWRGD	11 19 28
B254	CPU_PHY	CPU	PM_MEM_PWRGD_R	11
B251	CPU_PHY	CPU	CPU_MEM_RESET_L	11 28

FDI

Electrical Contraint Set	Physical	Spacing		
FDI Compensation				
B261	COMP_FDI_PHY	COMP_FDI	CPU_FDI_COMPIO	10

XDP

Electrical Contraint Set	Physical	Spacing		
XDP MISC.				
B172 XDP_BPM_L	XDP_PHY	XDP	XDP_BPM_L<7..0>	11 25
B173	XDP_PHY	XDP	CPU_CFG<17..16>	10 25
B257	XDP_PHY	XDP	CPU_CFG<11..0>	10 15 25
B260	XDP_PHY	XDP	XDP_DBRESET_L	11 25
B265	XDP_PHY	XDP	XDP_CPU_PWRGD	25
B264	XDP_PHY	XDP	XDP_CPU_PWRBTN_L	25
B262	XDP_PHY	XDP	XDP_CPU_CFG<0>	25
B263	XDP_PHY	XDP	XDP_VR_READY	25
B270	XDP_PHY	XDP	XDP_CPU_PLTRST_L	25 26
B269	XDP_PHY	XDP	XDP_PCH_PWRGD	25
B268	XDP_PHY	XDP	XDP_PCH_PWRBTN_L	25
B271	XDP_PHY	XDP	XDP_PCH_PLTRST_L	25 26
B176	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_P	11 15
B177	CLK_PCIE_PHY	CLK_PCIE	ITPCPU_CLK100M_N	11 15
B178 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_P	15 18 25
B180 ITP_CLK_CONN	CLK_PCIE_PHY	CLK_PCIE	ITPXDP_CLK100M_N	15 18 25
B179	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_P	25
B181	CLK_PCIE_PHY	CLK_PCIE	XDP_CPU_CLK100M_N	25
CPU JTAG				
B182	XDP_PHY	CLK_JTAG	XDP_CPU_TCK	11 25
B183	XDP_PHY	XDP	XDP_CPU_TMS	11 25
B184	XDP_PHY	XDP	XDP_CPU_TDI	11 25
B185	XDP_PHY	XDP	XDP_CPU_TDO	11 25
B190	XDP_PHY	XDP	XDP_CPU_TRST_L	11 25
B258	XDP_PHY	XDP	XDP_CPU_PRDY_L	11 25
B259	XDP_PHY	XDP	XDP_CPU_PREQ_L	11 25
PCH JTAG				
B186	XDP_PHY	CLK_JTAG	XDP_PCH_TCK	18 25
B187	XDP_PHY	XDP	XDP_PCH_TMS	18 25
B188	XDP_PHY	XDP	XDP_PCH_TDI	18 25
B189	XDP_PHY	XDP	XDP_PCH_TDO	18 25

Chipset Test Interface

Electrical Contraint Set	Physical	Spacing		
OBS PCH Side				
B191 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTA_OC_R_L	20 25
B192 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_R_L	20 25
B203 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTC_OC_R_L	20 25
B208 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_R_L	20 25
B205 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTB_OC_EHCI_R_L	20 25
B206 XDP_PCH_OBS	XDP_PHY	XDP	USB_EXTD_OC_EHCI_R_L	20 25
B209 XDP_PCH_OBS	XDP_PHY	XDP	AP_PWR_EN_R	20 25
B202 XDP_PCH_OBS	XDP_PHY	XDP	SDCONN_STATE_CHANGE_R	20 25
B201 XDP_PCH_OBS	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT_R	21 25
B200 XDP_PCH_OBS	XDP_PHY	XDP	ISOLATE_CPU_MEM_R_L	21 25
B199 XDP_PCH_OBS	XDP_PHY	XDP	GPU_GOOD_R	21 25
B198 XDP_PCH_OBS	XDP_PHY	XDP	DP_AUXCH_ISOL_R	18 25
B197 XDP_PCH_OBS	XDP_PHY	XDP	SATARDRVR_EN_R	18 25
B194 XDP_PCH_OBS	XDP_PHY	XDP	DP_TBT_SEL_R	21 25
B193 XDP_PCH_OBS	XDP_PHY	XDP	JTAG_TBT_TCK_R	21 25
B196 XDP_PCH_OBS	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH_R	21 25
B195 XDP_PCH_OBS	XDP_PHY	XDP	ENET_LOW_PWR_PCH_R	21 25
B240 XDP_PCH_OBS_UNUSED	XDP_PHY	OBS_STROBE	XDP_PIN03	21 25
OBS XDP Side				
B200	XDP_PHY	XDP	XDP_DA0_USB_EXTA_OC_L	25
B210	XDP_PHY	XDP	XDP_DA1_USB_EXTB_OC_L	25
B211	XDP_PHY	XDP	XDP_DA2_USB_EXTC_OC_L	25
B212	XDP_PHY	XDP	XDP_DA3_USB_EXTD_OC_L	25
B213	XDP_PHY	XDP	XDP_DB0_USB_EXTB_OC_EHCI_L	25
B214	XDP_PHY	XDP	XDP_DB1_USB_EXTD_OC_EHCI_L	25
B215	XDP_PHY	XDP	XDP_DB2_AP_PWR_EN	25
B216	XDP_PHY	XDP	XDP_DB3_SDCONN_STATE_CHANGE	25
B219	XDP_PHY	OBS_STROBE	XDP_FC1_TBT_CIO_PLUG_EVENT	25
B218	XDP_PHY	XDP	XDP_DC0_ISOLATE_CPU_MEM_L	25
B219	XDP_PHY	XDP	XDP_DC1_GPU_GOOD	25
B220	XDP_PHY	XDP	XDP_DC2_DP_AUXCH_ISOL	25
B223	XDP_PHY	XDP	XDP_DC3_SATARDRVR_EN	25
B222	XDP_PHY	XDP	XDP_DD0_DP_TBT_SEL	25
B222	XDP_PHY	XDP	XDP_DD1_JTAG_TBT_TCK	25
B226	XDP_PHY	XDP	XDP_DD2_AUD_IPHS_SWITCH_EN_PCH	25
B225	XDP_PHY	XDP	XDP_DD3_ENET_LOW_PWR_PCH	25
B224	XDP_PHY	OBS_STROBE	XDP_FC0_PCH_GPIO15	25
Standard usage branch off from OBS				
B229	XDP_PHY	XDP	USB_EXTA_OC_L	15 20 45
B228	XDP_PHY	XDP	USB_EXTB_OC_L	15 20 45
B230	XDP_PHY	XDP	USB_EXTC_OC_L	15 20 46
B229	XDP_PHY	XDP	USB_EXTD_OC_L	15 20 46
B232	XDP_PHY	XDP	USB_EXTB_OC_EHCI_L	15 20
B231	XDP_PHY	XDP	USB_EXTD_OC_EHCI_L	15 20
B243	XDP_PHY	XDP	AP_PWR_EN	15 20
B235	XDP_PHY	XDP	SDCONN_STATE_CHANGE	15 20 41
B239	XDP_PHY	OBS_STROBE	TBT_CIO_PLUG_EVENT	15 21
B240	XDP_PHY	XDP	ISOLATE_CPU_MEM_L	21 28 34
B243	XDP_PHY	XDP	GPU_GOOD	5 21
B238	XDP_PHY	XDP	DP_AUXCH_ISOL	15 18
B240	XDP_PHY	XDP	SATARDRVR_EN	15 18
B236	XDP_PHY	XDP	DP_TBT_SEL	21 62 84
B241	XDP_PHY	XDP	JTAG_TBT_TCK	15 21
B237	XDP_PHY	XDP	JTAG_TBT_TCK_ISOL	15 36
B244	XDP_PHY	XDP	AUD_IPHS_SWITCH_EN_PCH	21 26
B242	XDP_PHY	XDP	ENET_LOW_PWR_PCH	15 21 26
B272	XDP_PHY	XDP	DP_AUXCH_ISOL_EN	15

SYNC MASTER=D8 ROSITA SYNC DATE=03/23/2012

PAGE TITLE
CPU MISC/DMI/FDI/XDP Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 123 OF 143
SHEET 99 OF 117

SATA

SATA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SATA_PHY	*	SATA_90D
COMP_SATA_PHY	*	SATA_50S

SATA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_ISO	*	=7.2X_DIELECTRIC	?
COMP_SATA_ISO	*	=5.4X_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA	*	*	SATA_ISO
COMP_SATA	*	*	COMP_SATA_ISO

SATA Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Design	Comments
15.2.1	90	95	20	23.62	SATA Gen2, SATA Gen3

SATA Compensation Rules (mils)

Table	Imp	Design	Iso	Design	Comments
15-3	50	50	15	15.75	SATA Gen2, SATA Gen3

SATA

Electrical Contraint Set	Physical	Spacing		
PCH SATA Port 0 (HDD)				
B90 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_P	44
B92 SATA_R2D	SATA_PHY	SATA	SATA_HDD_R2D_N	44
B88	SATA_PHY	SATA	SATA_HDD_R2D_C_P	18 44
B89	SATA_PHY	SATA	SATA_HDD_R2D_C_N	18 44
B94 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_P	18 44
B95 SATA_D2R	SATA_PHY	SATA	SATA_HDD_D2R_N	18 44
B91	SATA_PHY	SATA	SATA_HDD_D2R_C_P	44
B93	SATA_PHY	SATA	SATA_HDD_D2R_C_N	44
PCH SATA Port 1 (SSD)				
B97 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_P	18 44
B99 SATA_R2D_MUX_SSD	SATA_PHY	SATA	SATA_SSD_R2D_N	18 44
B100 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_P	18 44
B102 SATA_D2R_MUX_SSD	SATA_PHY	SATA	SATA_SSD_D2R_N	18 44
PCH SATA Compensation				
B106	COMP_SATA_PHY	COMP_SATA	PCH_SATA1COMP	18
B108	COMP_SATA_PHY	COMP_SATA	PCH_SATA3COMP	18
B105	COMP_SATA_PHY	COMP_SATA	PCH_SATA3RBIAS	18

Unused

Electrical Contraint Set	Physical	Spacing

PAGE TITLE
SATA/FDI/XDP Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 124 OF 143
SHEET 100 OF 117

PCH

PCH-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCH_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCH-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCH_ISO	*	=6.5X_DIELECTRIC	?
COMP_PCH_ISO	*	=2:1_SPACING	?
PCH_ISO	*	=3:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCH	*	*	CLK_PCH_ISO
COMP_PCH	*	*	COMP_PCH_ISO
PCH	*	*	PCH_ISO

PCI

PCI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

PCI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCI_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCI	*	*	CLK_PCI_ISO

LPC

LPC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

LPC-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC_ISO	*	=1.5:1_SPACING	?
CLK_LPC_ISO	*	=3.6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LPC	*	*	LPC_ISO
CLK_LPC	*	*	CLK_LPC_ISO

HDA

HDA-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

HDA-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	HDA_ISO

Crystal

Crystal-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_XTAL	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

Crystal-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
XTAL_ISO	*	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
XTAL	*	*	XTAL_ISO

SPI

SPI-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPI-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI_ISO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	SPI_ISO

PCI

Electrical Contraint Set	Physical	Spacing		
PCI Clock				
B33	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIIN	18 26
B32	CLK_PCI_50S	CLK_PCI	PCH_CLK33M_PCIOUT	20 26

LPC

Electrical Contraint Set	Physical	Spacing		
LPC				
B32	LPC_50S	LPC	LPC_AD<3..0>	18 47 49
B33	LPC_50S	LPC	LPC_R_AD<3..0>	18
B33	LPC_50S	LPC	LPC_FRAME_L	18 47 49
B37	LPC_50S	LPC	LFRAME_L	18
LPC Clocks				
B33	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	26 49
B34	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	20 26
B34	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	26 47
B32	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	20 26

PCH Clocks

Electrical Contraint Set	Physical	Spacing		
PCH Reference Clock				
B18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_SB	26
B20	CLK_PCH_50S	CLK_PCH	PCH_CLK25M_XTALIN	18 26
PCH Ref Clock Comp				
B10	PCH_50S	COMP_PCH	PCH_XCLK_RCOMP	18
PCH RTC 32K				
B18	CLK_XTAL	XTAL	PCH_CLK32K_RTCX1	18 26
B18	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2	18 26
B32	CLK_XTAL	XTAL	PCH_CLK32K_RTCX2_R	26
SMC 32K				
B20	CLK_PCH_50S	CLK_PCH	PM_CLK32K_SUSCLK_R	19 48
B50	CLK_PCH_50S	CLK_PCH	SMC_CLK32K	47 48

25 MHz Reference Clocks

Electrical Contraint Set	Physical	Spacing		
25M Reference Crystal				
B20	CLK_XTAL	XTAL	SYSCLK_CLK25M_X1	26
B18	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2	26
B18	CLK_XTAL	XTAL	SYSCLK_CLK25M_X2_R	26
25M Reference Clocks				
B18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET	26 39
B18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_ENET_R	26
B18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT	26 36
B18	CLK_PCH_50S	CLK_PCH	SYSCLK_CLK25M_TBT_R	36

HDA

Electrical Contraint Set	Physical	Spacing		
HDA				
B35	HDA_50S	HDA	HDA_BIT_CLK	18 56
B36	HDA_50S	HDA	HDA_BIT_CLK_R	18
B36	HDA_50S	HDA	HDA_RST_L	18 56
B36	HDA_50S	HDA	HDA_RST_R_L	18
B36	HDA_50S	HDA	HDA_SDOUT	18 56
B36	HDA_50S	HDA	HDA_SDOUT_R	15 18
B36	HDA_50S	HDA	HDA_SYNC	15 18 56
B36	HDA_50S	HDA	HDA_SYNC_R	18
B36	HDA_50S	HDA	HDA_SDIN0	18 56
B36	HDA_50S	HDA	AUD_SDI_R	56
B16	HDA_50S	HDA	SPI_DESCRIPTOR_OVERRIDE_R	15
SPDIF				
B30		HDA	AUD_SPDIF_CHIP	56
B37		HDA	AUD_SPDIF_OUT	56 60

SPI Bootrom

Electrical Contraint Set	Physical	Spacing		
SPI ROM				
B31	SPI_50S	SPI	SPI_CLK_R	18 49
B32	SPI_50S	SPI	SPI_CLK	49
B32	SPI_50S	SPI	SPI_ALT_CLK	49
B40	SPI_50S	SPI	SPI_SMC_CLK	47 48
B40	SPI_50S	SPI	SPI_MLB_CLK	48 49
B34	SPI_50S	SPI	SPI_CS0_R_L	18 49
B35	SPI_50S	SPI	SPI_CS0_L	49
B35	SPI_50S	SPI	SPI_ALT_CS_L	49
B40	SPI_50S	SPI	SPI_SMC_CS_L	47 48
B37	SPI_50S	SPI	SPI_MLB_CS_L	48 49
B39	SPI_50S	SPI	SPI_MOSI_R	18 49
B40	SPI_50S	SPI	SPI_MOSI	49
B40	SPI_50S	SPI	SPI_ALT_MOSI	49
B40	SPI_50S	SPI	SPI_SMC_MOSI	47 48
B41	SPI_50S	SPI	SPI_MLB_MOSI	48 49
B40	SPI_50S	SPI	SPI_MISO	18 49
B40	SPI_50S	SPI	SPI_ALT_MISO	49
B40	SPI_50S	SPI	SPI_SMC_MISO	47 48
B41	SPI_50S	SPI	SPI_MLB_MISO	48 49
B60	SPI_50S	SPI	SPIROM_USE_MLB	21 49

SYNC MASTER=D8 MARK SYNC DATE=02/10/2012

PAGE TITLE
PCH and BR Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 125 OF 143

SHEET 101 OF 117

USB

USB-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
USB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB2_PHY	*	USB_90D
USB3_PHY	*	USB_85D
USB_HUB_PHY	*	USB_50S

USB Min Spacing Rules (mils) (Maho Bay PDG, Intel Doc# 473718)

Section	Imp	Design	Iso	Comments
12.2.1	90	90	12/2.8 mils = 4.29:1	USB 2.0
13.3.1	85	85	20/2.8 mils = 7.14:1	USB 3.0
			50/2.8 mils = 17.9:1	USB 2.0/3.0

SMSC Hub Application Note 15.17
Single-ended impedance range from 45-80 ohm is acceptable

USB 2.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2_ISO	*	=4.4X_DIELECTRIC	?
USB2_ISO	TOP,BOTTOM	=4.4X_DIELECTRIC	?
USB2_CLK_ISO	*	=18X_DIELECTRIC	?
USB2_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB_HUB_ISO	*	=2:1_SPACING	?

USB 3.0 Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_CLK_ISO	*	=18X_DIELECTRIC	?
USB3_CLK_ISO	TOP,BOTTOM	=18X_DIELECTRIC	?
USB3_USB3_ISO	*	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	TOP,BOTTOM	=7.3X_DIELECTRIC	?
USB3_USB3_ISO	ISL10	=5X_DIELECTRIC	?

USB 2.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB2	*	*	USB2_ISO
USB2	*CLK*	*	USB2_CLK_ISO
USB2	DISPLAYPORT	*	USB2_CLK_ISO
USB2	*TBT*	*	USB2_CLK_ISO
USB2	*ENET*	*	USB2_CLK_ISO
USB2	*SD*	*	USB2_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB_HUB	*	*	USB_HUB_ISO

USB 3.0 Spacing Rules

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3	*	*	USB3_ISO
USB3	*CLK*	*	USB3_CLK_ISO
USB3	DISPLAYPORT	*	USB3_CLK_ISO
USB3	*TBT*	*	USB3_CLK_ISO
USB3	*ENET*	*	USB3_CLK_ISO
USB3	*SD*	*	USB3_CLK_ISO
USB3	PCIE	*	USB3_CLK_ISO
USB3	SATA	*	USB3_CLK_ISO
USB3	USB3	*	USB3_USB3_ISO

CAMERA CONTROLLER

Camera Controller's SMIA Interface & MISC. Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMIA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CAM_SE	*	Y	0.2 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMIA_DIFF_PHY	*	SMIA_100D
CAM_PHY	*	CAM_SE

Camera Controller's SMIA Interface & MISC. Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMIA_DIFF_ISO	*	=6:1_SPACING	?
SMIA_DIFF2DIFF	*	=3:1_SPACING	?
CAM_ISO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMIA_DIFF	*	*	SMIA_DIFF_ISO
SMIA_DIFF	SMIA_DIFF	*	SMIA_DIFF2DIFF
CAM	*	*	CAM_ISO

USB 3.0 and USB 2.0 Trixies Muxing

Electrical Contraint Set	Physical	Spacing		
External Port A (J4600)				
E370 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_P	45
E371 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTA_RX_N	45
E372	USB3_PHY	USB3	USB3_EXTA_RX_F_P	20 45
E373	USB3_PHY	USB3	USB3_EXTA_RX_F_N	20 45
E374 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_P	20 45
E375 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTA_TX_N	20 45
E376	USB3_PHY	USB3	USB3_EXTA_TX_F_P	45
E377	USB3_PHY	USB3	USB3_EXTA_TX_F_N	45
E378	USB3_PHY	USB3	USB3_EXTA_TX_C_P	45
E379	USB3_PHY	USB3	USB3_EXTA_TX_C_N	45
E380 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_P	20 45
E381 USB2_MUXED_MOJO_CONN	USB2_PHY	USB2	USB_PCH_0_N	20 45
E382	USB2_PHY	USB2	USB2_EXTA_MUXED_P	45
E383	USB2_PHY	USB2	USB2_EXTA_MUXED_N	45
E384	USB2_PHY	USB2	USB2_EXTA_MUXED_F_P	45
E385	USB2_PHY	USB2	USB2_EXTA_MUXED_F_N	45
External Port B (J4610)				
E386 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_P	45
E387 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTB_RX_N	45
E388	USB3_PHY	USB3	USB3_EXTB_RX_F_P	20 45
E389	USB3_PHY	USB3	USB3_EXTB_RX_F_N	20 45
E390 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_P	20 45
E391 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTB_TX_N	20 45
E392	USB3_PHY	USB3	USB3_EXTB_TX_F_P	45
E393	USB3_PHY	USB3	USB3_EXTB_TX_F_N	45
E394	USB3_PHY	USB3	USB3_EXTB_TX_C_P	45
E395	USB3_PHY	USB3	USB3_EXTB_TX_C_N	45
E396 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_P	20 45
E397 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_1_N	20 45
E398	USB2_PHY	USB2	USB_PCH_9_P	20 45
E399	USB2_PHY	USB2	USB_PCH_9_N	20 45
E400	USB2_PHY	USB2	USB2_EXTB_MUXED_P	45
E401	USB2_PHY	USB2	USB2_EXTB_MUXED_N	45
E402	USB2_PHY	USB2	USB2_EXTB_MUXED_F_P	45
E403	USB2_PHY	USB2	USB2_EXTB_MUXED_F_N	45
External Port C (J4700)				
E404 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_P	46
E405 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTC_RX_N	46
E406	USB3_PHY	USB3	USB3_EXTC_RX_F_P	20 46
E407	USB3_PHY	USB3	USB3_EXTC_RX_F_N	20 46
E408 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_P	20 46
E409 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTC_TX_N	20 46
E410	USB3_PHY	USB3	USB3_EXTC_TX_F_P	46
E411	USB3_PHY	USB3	USB3_EXTC_TX_F_N	46
E412	USB3_PHY	USB3	USB3_EXTC_TX_C_P	46
E413	USB3_PHY	USB3	USB3_EXTC_TX_C_N	46
E414 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_P	20 46
E415 USB2_CONN	USB2_PHY	USB2	USB_PCH_2_N	20 46
E416	USB2_PHY	USB2	USB2_EXTC_F_P	46
E417	USB2_PHY	USB2	USB2_EXTC_F_N	46
External Port D (J4710)				
E418 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_P	46
E419 USB3_RX_CONN	USB3_PHY	USB3	USB3_EXTD_RX_N	46
E420	USB3_PHY	USB3	USB3_EXTD_RX_F_P	20 46
E421	USB3_PHY	USB3	USB3_EXTD_RX_F_N	20 46
E422 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_P	20 46
E423 USB3_TX_CONN	USB3_PHY	USB3	USB3_EXTD_TX_N	20 46
E424	USB3_PHY	USB3	USB3_EXTD_TX_F_P	46
E425	USB3_PHY	USB3	USB3_EXTD_TX_F_N	46
E426	USB3_PHY	USB3	USB3_EXTD_TX_C_P	46
E427	USB3_PHY	USB3	USB3_EXTD_TX_C_N	46
E428 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_P	20 46
E429 USB2_MUXED_CONN	USB2_PHY	USB2	USB_PCH_3_N	20 46
E430	USB2_PHY	USB2	USB_PCH_10_P	20 46
E431	USB2_PHY	USB2	USB_PCH_10_N	20 46
E432	USB2_PHY	USB2	USB2_EXTD_MUXED_P	46
E433	USB2_PHY	USB2	USB2_EXTD_MUXED_N	46
E434	USB2_PHY	USB2	USB2_EXTD_MUXED_F_P	46
E435	USB2_PHY	USB2	USB2_EXTD_MUXED_F_N	46
Camera (U4200)				
E436 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_P	42
E437 USB2_CONN_INT	USB2_PHY	USB2	USB_CAMERA_N	42
PCH USB Compensation				
E438	PCH_50S	COMP_PCH	PCH_USB_RBIAS	20

Electrical Contraint Set	Physical	Spacing	Voltage		
Camera Controller Local Ground					
E439	GND_PHY	GND	0V	CAM_AGND	42
E440	GND_PHY	GND	0V	CAM_PLLGND	42

USB Hub

Electrical Contraint Set	Physical	Spacing		
USB 2.0 Hub				
E441 USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_P	20 27
E442 USB2_HUB_PCH	USB2_PHY	USB2	USB_PCH_7_N	20 27
E443 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_P	27 35
E444 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_N	27 35
E445 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_P	35
E446 USB2_HUB_BT	USB2_PHY	USB2	USB_BT_MUX_N	35
E447	USB_HUB_PHY	USB_HUB	USB_HUB_2P	27
E448	USB_HUB_PHY	USB_HUB	USB_HUB_2N	27
USB 2.0 Hub Misc.				
E449	USB_HUB_PHY	USB_HUB	USB_HUB_RESET_L	27
E450	USB_HUB_PHY	USB_HUB	USB_HUB_VBUS_DET	27
E451	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM0	27
E452	USB_HUB_PHY	USB_HUB	USB_HUB_NON_REM1	27
E453	USB_HUB_PHY	USB_HUB	USB_HUB_HS_IND	27
USB 2.0 Hub Compensation				
E454	PCH_50S	COMP_PCH	USB_HUB_RBIAS	27
USB 2.0 Hub Crystal				
E455	CLK_XTAL	XTAL	USB_HUB_XTAL1	27
E456	CLK_XTAL	XTAL	USB_HUB_XTAL2	27
E457	CLK_XTAL	XTAL	USB_HUB_XTAL2_R	27

Camera Controller

Electrical Contraint Set	Physical	Spacing		
SMIA				
E458 SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_P	42
E459 SMIA_DATA	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_DATA_N	42
E460 SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_P	42
E461 SMIA_CLK	SMIA_DIFF_PHY	SMIA_DIFF	SMIA_CLK_N	42
MISC				
E462	SPI_50S	SPI	CAM_SF_CLK	42
E463	SPI_50S	SPI	CAM_SF_CLK_R	42
E464	SPI_50S	SPI	CAM_SF_DIN	42
E465	SPI_50S	SPI	CAM_SF_DIN_R	42
E466	SPI_50S	SPI	CAM_SF_CS_L	42
E467	SPI_50S	SPI	CAM_SF_WP_L	42
E468	SPI_50S	SPI	CAM_SF_DOUT	42
E469	SPI_50S	SPI	CAM_SF_DOUT_R	42
E470	SPI_50S	SPI	CAM_SF_HOLD_L	42
E471	CAM_PHY	CAM	CAM_USB_VRES	42
E472	CAM_PHY	CAM	MIPI_RESISTOR	42
E473		PM	CAM_EXT_BOOT_L	43
E474		PM	PCH_CAM_EXT_BOOT_R_L	21 43
E475		PM	CAM_P1V2_RST_HOLDOFF	43
E476		PM	CAM_P1V2_RST_HOLDOFF_L	43
I2C				
E477	SMB_PHY	SMB	I2C_CAMSENSOR_SDA	42
E478	SMB_PHY	SMB	I2C_CAMSENSOR_SCL	42
E479	SMB_PHY	SMB	SMB_ALS_F_SDA	42
E480	SMB_PHY	SMB	SMB_ALS_F_SCL	42
Camera Controller Crystal				
E481	CLK_XTAL	XTAL	CAM_XTAL_IN	42
E482	CLK_XTAL	XTAL	CAM_XTAL_OUT	42
E483	CLK_XTAL	XTAL	CAM_XTAL_OUT_R	42

SYNC MASTER=D8 KOSECOFF SYNC DATE=06/22/2012

PAGE TITLE
USB/Camera Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 126 OF 143
SHEET 102 OF 117

SMBus

SMBus-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_PHY	*	SMB_55S

SMBus-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB_ISO	*	=2x_DIELECTRIC	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SMB_ISO

Sensor

Sensor-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.085 MM
SNS_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SNS_DIFF_PHY	*	1:1_DIFFPAIR
SNS_PHY	*	SNS_50S

Sensor-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE_ISO	*	=4:1_SPACING	?

Constraints

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SENSE	*	*	SENSE_ISO
SENSE	POWER	*	PWR_P2MM
SENSE	GND	*	GND_P2MM

SYNC MASTER=D8 MARK SYNC DATE=04/23/2012

PAGE TITLE
SMBus/Sensor Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 127 OF 143
SHEET 103 OF 117

DC-DC

Power-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GND_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
GND_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
POWER_P3MM	*	Y	0.300 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P6MM	*	Y	0.600 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD
POWER_P5MM	*	Y	0.500 MM	0.200 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VR_CTL_PHY	*	POWER_P5MM
VR_CTL_PHY	BGA	STANDARD
VR_VID_PHY	*	POWER_50S
POWER_PHY	*	POWER_P6MM
GND_PHY	*	GND_P5MM

Constraints
Power and Common

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
POWER	*	*	POWER_ISO
GND	*	*	GND_ISO

Power-specific Spacing Definitions
Power and Common

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
POWER_ISO	*	=STANDARD	?

DC-DC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_SWITCH	*	*	SWNODE_ISO
VR_SWITCH	*	BGA	BGA_P1MM
VR_SWITCH	VR_SWITCH	*	SWNODE_SW2SW
VR_SWITCH	POWER	*	SWNODE_SW2PWR
VR_SWITCH	GND	*	SWNODE_SW2GND
VR_LGATE	*	*	SWNODE_ISO
VR_LGATE	VR_SWITCH	*	SWNODE_LG2SW

DC-DC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SWNODE_ISO	*	=8:1_SPACING	1000
SWNODE_SW2SW	*	=1:1_SPACING	?
SWNODE_SW2PWR	*	=2:1_SPACING	?
SWNODE_SW2GND	*	=2:1_SPACING	?
SWNODE_LG2SW	*	=3:1_SPACING	?

DC-DC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VR_CTL	*	*	VR_CTL_ISO
VR_VID	*	*	VR_VID_ISO

DC-DC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
VR_CTL_ISO	*	=3:1_SPACING	?
VR_VID_ISO	*	=4X_DIELECTRIC	?

CPU VccSA

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B24	POWER_PHY	POWER	5V			REG_VCC_U7500	70
B25	POWER_PHY	POWER	5V			REG_PVCC_U7500	70
Local Ground							
B26	GND_PHY	GND	0V			AGND_VCCSAS0	70
VCCIO							
B27	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VCCSAS0	70
B28	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VCCSAS0	70
B29	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VCCSAS0_RC	70
B31	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VCCSAS0	70
B30	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VCCSAS0	70
B33	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_VCCSAS0	70
B32	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_OCSET	70
B35	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_VO	70
B34		SENSE				SNS_CPU_VCCSA	13 70
B37 VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_P	70
B36 VSNS_CPU_VCCSA	SNS_DIFF_PHY	SENSE				SNS_VCCSAS0_XW_N	70
B38		SENSE				REG_VCCSAS0_FB	70
B39		SENSE				REG_VCCSAS0_RTN	70
B40	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_SREF	70
B41	VR_CTL_PHY	VR_CTL				REG_VCCSAS0_FSEL	70
Output Bus							
B42	POWER_PHY	POWER	0.925V			PPVCCSA_S0	6

CPU VccIO PCH 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
F1	POWER_PHY	POWER	5V			REG_VCC_U7400	69
F2	POWER_PHY	POWER	5V			REG_PVCC_U7400	69
Local Ground							
F3	GND_PHY	GND	0V			AGND_CPU_P1V05S0	69
1.05V S0							
F5	POWER_PHY	VR_SWITCH	12V	TRUE		REG_CPU_PHASE_P1V05S0	69
F7	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_BOOT_P1V05S0	69
F6	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_BOOT_P1V05S0_RC	69
F8	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0	69
F9	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_CPU_UGATE_P1V05S0_R	
F10	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_CPU_LGATE_P1V05S0	69
F12	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_CPU_SNUBBER_P1V05S0	69
F11	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_OCSET	69
F14	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_VO	69
F13 VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_P	13 69
F15 VSNS_CPU_VCCIO	SNS_DIFF_PHY	SENSE				SNS_CPU_VCCIO_N	13 69
F16	SNS_DIFF_PHY	SENSE				SNS_CPU_P1V05S0_XW_P	69
F17	SNS_DIFF_PHY	SENSE				SNS_CPU_P1V05S0_XW_N	69
F19		SENSE				REG_CPU_P1V05S0_FB	69
F18		SENSE				REG_CPU_P1V05S0_RTN	69
F21	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_SREF	69
F20	VR_CTL_PHY	VR_CTL				REG_CPU_P1V05S0_FSEL	69
Output Bus							
F22	POWER_PHY	POWER	1.05V			PP1V05_S0_CPU	6

PCH/GPU/TBT 1.05V S0

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
E44	POWER_PHY	POWER	5V			REG_VCC_UB700	95
Local Ground							
E46	GND_PHY	GND	0V			P1V05_AGND	95
1.05V S0							
E47	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0	95
E48	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P1V05S0_L	95
E49	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P1V05S0	95
E50	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P1V05S0_RC	95
E51	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0	95
E52	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P1V05S0_R	95
E53	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P1V05S0	95
E55	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_P1V05S0	95
E56	VR_CTL_PHY	VR_CTL				REG_P1V05S0_OCSET	95
E54	VR_CTL_PHY	VR_CTL				REG_P1V05S0_VO	95
E72	POWER_PHY	VR_SWITCH	12V			REG_P1V05S0_VO_R	95
E73	POWER_PHY	VR_SWITCH	12V			P1V05_OCSET_R	95
E61		SENSE				REG_P1V05S0_FB	95
E62		SENSE				REG_P1V05S0_RTN	95
E63	VR_CTL_PHY	VR_CTL				REG_P1V05S0_SREF	95
E64	VR_CTL_PHY	VR_CTL				REG_P1V05S0_FSEL	95
Output Bus							
E65	POWER_PHY	POWER	1.05V			PP1V05_S0_PCH	6
E66	POWER_PHY	POWER	1.05V			PP1V05_S0	6
FET Switched							
E67	POWER_PHY	POWER	1.05V			PP1V05_TBTLC	6 38
E68	POWER_PHY	POWER	1.05V			PP1V05_TBTCIO	6

SYNC MASTER=D8 MARK SYNC DATE=02/10/2012

PAGE TITLE
VReg Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 128 OF 143

SHEET 104 OF 117

CPU Core Phases

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B1A0	POWER_PHY	POWER	12V			PP12V_S0_CPUCORE_FLT	66 67 68
B1A1	POWER_PHY	POWER	5V			REG_VCC_U7100	66
Local Ground							
B1A2	GND_PHY	GND	0V			AGND_CPU	66 67 68
Phase 1							
B1B0	POWER_PHY	POWER	12V			REG_LVCC_U7210	67
B1B1	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1	66 67
B1B2	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_1_R	66
B1B3	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_1	67
B1B4	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_1	67
B1B5	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_1_RC	67
B1B6	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_1	67
B1B7	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_1	67
B1B8	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_1	67
B1B9	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_1	67
B1BA ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_P	66 67
B1BB ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_1_N	67
B1BC		SENSE				REG_ISENCORE_1_NR	66 67
Phase 2							
B1C0	POWER_PHY	POWER	12V			REG_LVCC_U7230	67
B1C1	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2	66 67
B1C2	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_2_R	66
B1C3	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_2	67
B1C4	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_2	67
B1C5	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_2_RC	67
B1C6	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_2	67
B1C7	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_2	67
B1C8	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_2	67
B1C9	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_2	67
B1CA ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_P	66 67
B1CB ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_2_N	67
B1CC		SENSE				REG_ISENCORE_2_NR	66 67
Phase 3							
B1D0	POWER_PHY	POWER	12V			REG_LVCC_U7250	67
B1D1	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3	66 67
B1D2	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_3_R	66
B1D3	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_3	67
B1D4	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_3	67
B1D5	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_3_RC	67
B1D6	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_3	67
B1D7	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_3	67
B1D8	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_3	67
B1D9	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_3	67
B1DA ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_P	66 67
B1DB ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_3_N	67
B1DC		SENSE				REG_ISENCORE_3_NR	66 67
Phase 4							
B1E0	POWER_PHY	POWER	12V			REG_LVCC_U7310	68
B1E1	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4	66 68
B1E2	VR_CTL_PHY	VR_CTL				REG_PWM_CPUCORE_4_R	66
B1E3	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUCORE_4	68
B1E4	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUCORE_4	68
B1E5	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUCORE_4_RC	68
B1E6	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUCORE_4	68
B1E7	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUCORE_4	68
B1E8	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUCORE_4	68
B1E9	POWER_PHY	POWER	1.1V			PPCPUCORE_S0_SENSE_4	68
B1EA ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_4_P	66 68
B1EB ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISENCORE_4_N	68
B1EC		SENSE				REG_ISENCORE_4_NR	66 68
B1F0 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_XW_P	66
B1F1 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_XW_N	66
B1F2 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_R_P	66
B1F3 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CORE_R_N	66
B1F4 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_P	13 66
B1F5 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VAXG_N	13 66
B1F6 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_P	13 66
B1F7 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_CPU_VCORE_N	13 66
B1F8 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_P1V05_IOVDD_XW_P	95
B1F9 ISNS_CPU_CORE	SNS_DIFF_PHY	SENSE				SNS_P1V05_IOVDD_XW_N	95

CPU AXG Phase and Core Controller

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
AXG							
B1G0	POWER_PHY	POWER	12V			REG_LVCC_U7330	68
B1G1	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG	66 68
B1G2	VR_CTL_PHY	VR_CTL				REG_PWM_CPUAXG_R	66
B1G3	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_CPUAXG	68
B1G4	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_CPUAXG	68
B1G5	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_CPUAXG_RC	68
B1G6	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_CPUAXG	68
B1G7	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_CPUAXG	68
B1G8	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_CPUAXG	68
B1G9	POWER_PHY	POWER	1.1V			PPCPUAXG_S0_SENSE	68
B1GA ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_P	68
B1GB ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				REG_ISENAXG_N	68
B1GC		SENSE				REG_ISENAXG_PR	66 68
B1GD		SENSE				REG_ISENAXG_NR	66 68
B1H2 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_R_P	66
B1H3 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_R_N	66
B1H4 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_XW_P	66
B1H5 ISNS_CPU_AXG	SNS_DIFF_PHY	SENSE				SNS_AXG_XW_N	66
ISL6364							
B1H0	VR_CTL_PHY	VR_CTL				REG_CPUCORE_COMP	66
B1H1	VR_CTL_PHY	VR_CTL				CPUCORE_COMP_RC	66
B1H2	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FB	66
B1H3	VR_CTL_PHY	VR_CTL				CPUCORE_FB_RC	66
B1H4	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_1	66
B1H5	VR_CTL_PHY	VR_CTL				CPUCORE_FB_R_2	66
B1H6	VR_CTL_PHY	VR_CTL				CPUCORE_PSICOMP_RC	66
B1H7	VR_CTL_PHY	VR_CTL				REG_CPUCORE_PSICOMP	66
B1H8	VR_CTL_PHY	VR_CTL				REG_CPUCORE_HFCOMP	66
B1H9		SENSE				REG_CPUCORE_VSEN	66
B1HA		SENSE				REG_CPUCORE_RGND	66
B1HB	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IMON	51 66
B1HC	VR_CTL_PHY	VR_CTL				CPUCORE_IMON_R	66
B1HD	VR_CTL_PHY	VR_CTL				REG_CPUCORE_TM	66
B1HE	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SUTH	66
B1HF	VR_CTL_PHY	VR_CTL				REG_CPUCORE_NPSI	66
B1HG	VR_CTL_PHY	VR_CTL				REG_CPUCORE_FDVID	66
B1HH	VR_CTL_PHY	VR_CTL				REG_CPUCORE_IAUTO	66
B1HJ	VR_CTL_PHY	VR_CTL				REG_CPUCORE_SW_FREQ	66
B1HK	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RAMPADJ	66
B1HL	VR_CTL_PHY	VR_CTL				REG_CPUCORE_EN_PWR	66
B1HM	VR_CTL_PHY	VR_CTL				CPUCORE_EN_PWR_R	66
B1HN	VR_CTL_PHY	VR_CTL				REG_CPUCORE_RSET	66
B1HP	VR_CTL_PHY	VR_CTL				REG_CPUAXG_COMP	66
B1HQ	VR_CTL_PHY	VR_CTL				CPUAXG_COMP_RC	66
B1HR	VR_CTL_PHY	VR_CTL				REG_CPUAXG_FB	66
B1HS	VR_CTL_PHY	VR_CTL				CPUAXG_FB_RC	66
B1HT	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_1	66
B1HU	VR_CTL_PHY	VR_CTL				CPUAXG_FB_R_2	66
B1HV	VR_CTL_PHY	VR_CTL				REG_CPUAXG_HFCOMP	66
B1HW		SENSE				REG_CPUAXG_VSEN	66
B1HX		SENSE				REG_CPUAXG_RGND	66
B1HY	VR_CTL_PHY	VR_CTL				REG_CPUAXG_IMON	51 66
B1HZ	VR_CTL_PHY	VR_CTL				CPUAXG_IMON_R	66
B1J0	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TM	66
B1J1	VR_CTL_PHY	VR_CTL				REG_CPUAXG_TCOMP	66
B1J2	VR_CTL_PHY	VR_CTL				REG_CPUAXG_SW_FREQ	66
B1J3	VR_VID_PHY	VR_VID				CPU_VIDSCLK	13 66
B1J4	VR_VID_PHY	VR_VID				CPU_VIDSCLK_R	13
B1J5	VR_VID_PHY	VR_VID				CPU_VIDALERT_L	13 66
B1J6	VR_VID_PHY	VR_VID				CPU_VIDALERT_R_L	13
B1J7	VR_VID_PHY	VR_VID				CPU_VIDSOUT	13 66
B1J8	VR_VID_PHY	VR_VID				CPU_VIDSOUT_R	13
Output Bus							
B1J9	POWER_PHY	POWER	1.1V			PPVCORE_S0_CPU	6
B1JA	POWER_PHY	POWER	1.1V			PPVAXG_S0	6

SYNC MASTER=D8 MARK SYNC DATE=02/10/2012

PAGE TITLE
CPU VReg Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 129 OF 143

SHEET 105 OF 117

3.3V S5/5V S4

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B115	POWER_PHY	POWER	12V			REG_VIN_U7600	71
B115	POWER_PHY	POWER	5V			REG_VCC1_U7600	71
B115	POWER_PHY	POWER	5V			REG_VCC2_U7600	71
3.3V S5							
B116	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P3V3S5	71
B116	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P3V3S5	71
B116	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P3V3S5_RC	71
B116	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P3V3S5	71
B116	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P3V3S5	71
B116	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P3V3S5	71
B116	VR_CTL_PHY	VR_CTL				REG_P3V3S5_ISEN	71
B116	VR_CTL_PHY	VR_CTL				REG_P3V3S5_OCSET	71
B116	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FSET	71
B116	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT	71
B116	VR_CTL_PHY	VR_CTL				REG_P3V3S5_VOUT_R	71
B116	VR_CTL_PHY	VR_CTL				REG_P3V3S5_FB	71
5V S3							
B115	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_P5VS4	71
B115	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_P5VS4	71
B115	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_P5VS4_RC	71
B115	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_P5VS4	71
B115	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_P5VS4	71
B115	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_P5VS4	71
B115	VR_CTL_PHY	VR_CTL				REG_P5VS4_ISEN	71
B115	VR_CTL_PHY	VR_CTL				REG_P5VS4_OCSET	71
B115	VR_CTL_PHY	VR_CTL				REG_P5VS4_FSET	71
B115	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT	71
B115	VR_CTL_PHY	VR_CTL				REG_P5VS4_VOUT_R	71
B115	VR_CTL_PHY	VR_CTL				REG_P5VS4_FB	71
Output Bus							
B116	POWER_PHY	POWER	5V			PP5V_S5	6
B116	POWER_PHY	POWER	5V			PP5V_S4	6
B116	POWER_PHY	POWER	3.3V			PP3V3_S5	6
FET Switched							
B123	POWER_PHY	POWER	5V			PP5V_S0	6
B123	POWER_PHY	POWER	3.3V			PP3V3_S4	6
B123	POWER_PHY	POWER	3.3V			PP3V3_S0	6
B123	POWER_PHY	POWER	3.3V			PP3V3_S4_ENET	6
B123	POWER_PHY	POWER	3.3V			PP3V3_TBTLC	6
B123	POWER_PHY	POWER	3.3V			PP3V3_S4_AP	6
B123	POWER_PHY	POWER	3.3V			PP3V3_S0_SSD	6

VDDQ S3 (1.5V)/VTT S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B123	POWER_PHY	POWER	5V			REG_V5IN_U7700	72
Local Ground							
B132	GND_PHY	GND	0V			AGND_VDDQS3	72
VDDQ S3							
B126	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3	72
B126	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_VDDQS3_L	72
B126	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_VDDQS3	72
B126	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_VDDQS3_RC	72
B126	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3	72
B126	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_VDDQS3_R	72
B126	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_VDDQS3	72
B126	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_SNUBBER_VDDQS3	72
B118	POWER_PHY	POWER	1.5V			PPVDDQ_S3_SENSE	
B126	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VDDQSNS	72
B126	VR_CTL_PHY	VR_CTL				REG_VDDQS3_VREF	72
B126	VR_CTL_PHY	VR_CTL				REG_VDDQS3_REFIN	72
B126	VR_CTL_PHY	VR_CTL				REG_VDDQS3_MODE	72
B126	VR_CTL_PHY	VR_CTL				REG_VDDQS3_TRIP	72
B121	VR_CTL_PHY	VR_CTL				LDO_DDRVTTS0_SNS	72
Output Bus							
B121	POWER_PHY	POWER	1.5V			PPVDDQ_S3	6
B121	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S0	6
FET Switched							
B118	POWER_PHY	POWER	1.5V			PP1V5_S0	6
Sensed							
B118	POWER_PHY	POWER	1.5V			PPVDDQ_S3_DDR	6
B118	POWER_PHY	POWER	1.5V			PP1V5_S0_CPU_MEM	6
B118	POWER_PHY	POWER	1.5V			PPFBVDDQ_S0_GPU	6

DDR3 Vref

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Memory Vref							
B135	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_DAC	34
B135	POWER_PHY	POWER	3.3V			PP3V3_S4_VREFMRGN_CTRL	34
B135	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_A_S3	6
B135	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_DQ_MEM_B_S3	6
B143	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_A	11 34
B143	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DIMM_VREF_DAC_B	11 34
B135	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_A_S3	6
B135	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVREF_CA_MEM_B_S3	6
B130	POWER_DDR_PHY	POWER_DDR	0.75V			CPU_DDR_VREF	11
B140	POWER_DDR_PHY	POWER_DDR	0.75V			PPDDRVTT_S3	6

1.8V S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
1.8V S0							
B115	POWER_PHY	VR_SWITCH	5V	TRUE		REG_PHASE_P1V8S0	72
B116	VR_CTL_PHY	VR_CTL				REG_P1V8S0_VFB	72
B116	VR_CTL_PHY	VR_CTL				REG_P1V8S0_SYNCH	72
Output Bus							
B118	POWER_PHY	POWER	1.8V			PP1V8_S0	6

HDD S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
HDD S0							
B139	POWER_PHY	POWER	5V			PP5V_S0_HDD	6

12V S5

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B139	POWER_PHY	POWER	12V			PP12V_ACDC	6
FET Switched							
B139	POWER_PHY	POWER	12V			PP12V_S0	6
Sensed							
B139	POWER_PHY	POWER	12V			PP12V_S5	6
B139	POWER_PHY	POWER	12V			PP12V_G3H	6
B141	POWER_PHY	POWER	12V			PP12V_G3H_P3V42	73
B140	POWER_PHY	POWER	12V			PP12V_S0_FBVDDQ	6
B140	POWER_PHY	POWER	12V			PP12V_S0_CPU_P1V05	6
B140	POWER_PHY	POWER	12V			PP12V_S0_VCCSA	6
B140	POWER_PHY	POWER	12V			PP12V_S0_P1V05	6
B139	POWER_PHY	POWER	12V			PP12V_S0_HDD	6
B140	POWER_PHY	POWER	12V			PP12V_S0_BLC	6

Ground/Common

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Common							
B132	GND_PHY	GND	0V			GND	

3V42 S0

	Physical	Spacing	Voltage	DIDT	NO_TEST		
3V42 S0							
B133	POWER_PHY	VR_SWITCH	5V	TRUE		P3V42G3H_SW	73
B133	VR_CTL_PHY	VR_CTL				P3V42G3H_FB	73
B133	VR_CTL_PHY	VR_CTL				P3V42G3H_SHDN_L	73
B133	POWER_PHY	POWER	3.3V			PP3V3_G3	6
B133	POWER_PHY	POWER	3.3V			PP3V42_G3H	6

SYNC MASTER=D8 MARK SYNC DATE=02/10/2012

PAGE TITLE
Platform VReg Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 130 OF 143

SHEET 106 OF 117

Thunderbolt

Thunderbolt-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBT_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
TBTDP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	0.075MM
TBT_GEN_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

Thunderbolt-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_I2C_ISO	*	=2x_DIELECTRIC	?
TBT_SPI_ISO	*	=2x_DIELECTRIC	?
TBTDP_ISO	*	=5x_DIELECTRIC	?
TBTDP_ISO	TOP,BOTTOM	=7x_DIELECTRIC	?
TBT_GEN_ISO	*	=2X_DIELECTRIC	?
BGA_TBT_AREA	*	0.075MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_TBT	BGA_TBT_AREA
TBT_I2C	*	*	TBT_I2C_ISO
TBT_SPI	*	*	TBT_SPI_ISO
TBTDP	*	*	TBTDP_ISO
TBT_GEN	*	*	TBT_GEN_ISO

SOURCE: Bill Cornelius's T29 Routing Notes

DisplayPort

DP-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	0.08MM	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

DP-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_ISO	*	=6.7X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	*	*	DP_ISO

MAX LENGTH OF DISPLAYPORT TRACES: 6 INCHES

DISPLAYPORT INTRA-PAIR MATCHING SHOULD BE 1 PS. INTER-PAIR MATCHING SHOULD BE WITHIN 150 PS.
DISPLAYPORT AUX CHANNEL INTRA-PAIR MATCHING SHOULD BE 5 PS.

TBT IC Net Properties

Electrical Contraint Set	Physical	Spacing			
1611	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	NO_TEST=TRUE	36 81
1612	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	NO_TEST=TRUE	36 81
1613 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	NO_TEST=TRUE	36
1614 DP_TBTSNK0_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	NO_TEST=TRUE	36
1615	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P		36 75
1616	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N		36 75
1617 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P		36
1618 DP_TBTSNK0_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N		36
1619	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	NO_TEST=TRUE	36 81
1620	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	NO_TEST=TRUE	36 81
1621 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	NO_TEST=TRUE	36
1622 DP_TBTSNK1_ML	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	NO_TEST=TRUE	36
1623	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P		36 75
1624	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N		36 75
1625 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P		36
1626 DP_TBTSNK1_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N		36
1660 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_P<3..0>	NO_TEST=TRUE	84
1662 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_N<3..0>	NO_TEST=TRUE	84
1664 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	NO_TEST=TRUE	84
1667 DP_INTPNL_TBT_ML_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	NO_TEST=TRUE	84
1672 DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_P		84
1673 DP_INTPNL_TBT_AUX_MUX	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_N		84
1660	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_P		84
1662	DP_85D	DISPLAYPORT	DP_TBTSRC_AUX_C_N		84
1631	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SCL		36 50
1632	TBT_I2C_55S	TBT_I2C	I2C_TBTRTR_SDA		36 50
1633 TBT_SPI_CLK	TBT_I2C_55S	TBT_SPI	TBT_SPI_CLK		36
1632 TBT_SPI_MOSI	TBT_I2C_55S	TBT_SPI	TBT_SPI_MOSI		36
1631 TBT_SPI_MISO	TBT_I2C_55S	TBT_SPI	TBT_SPI_MISO		36
1633 TBT_SPI_CS_L	TBT_I2C_55S	TBT_SPI	TBT_SPI_CS_L		36
1688	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG1_BUF		36 86
1689	TBT_GEN_55S	TBT_GEN	TBT_A_CONFIG2_RC		36 86
1691	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG1_BUF		36 88
1690	TBT_GEN_55S	TBT_GEN	TBT_B_CONFIG2_RC		36 88
1693	TBT_GEN_55S	TBT_GEN	TBT_A_LSTX		36 86
1692	TBT_GEN_55S	TBT_GEN	TBT_A_LSRX		36 86
1695	TBT_GEN_55S	TBT_GEN	TBT_B_LSTX		36 88
1694	TBT_GEN_55S	TBT_GEN	TBT_B_LSRX		36 88
1697	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_HPD		36 82
1696	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_HPD		36 82
1698	TBT_GEN_55S	TBT_GEN	DP_TBTSRC_HPD		36 84
1699	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_CLK		81 85
1701	TBT_GEN_55S	TBT_GEN	DP_TBTSNK0_DDC_DATA		81 85
1700	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_CLK		81 85
1702	TBT_GEN_55S	TBT_GEN	DP_TBTSNK1_DDC_DATA		81 85
1703	TBT_GEN_55S	TBT_GEN	VIDEO_ON		74 87
1704	TBT_GEN_55S	TBT_GEN	VIDEO_ON_L		5 87
1705	TBT_GEN_55S	TBT_GEN	BDV_BKL_PWM		48 84
1706	TBT_GEN_55S	TBT_GEN	GPU_LCD_BKLT_PWM	NO_TEST=TRUE	82 84
1707	TBT_GEN_55S	TBT_GEN	LCD_BL_PWM		84
1708	TBT_GEN_55S	TBT_GEN	LCD_BL_FILT		84
1709	TBT_GEN_55S	TBT_GEN	LCD_BKLT_PWM		84 89

*: Only used on hosts supporting T29 video-in

TBT/DP Net Properties

Electrical Contraint Set	Physical	Spacing			
Port A					
1631 TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<0>	NO_TEST=TRUE	36 86
1632 TBT_A_R2D	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<0>	NO_TEST=TRUE	36 86
1633 TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_N<1>	NO_TEST=TRUE	36 86
1634 TBT_A_R2D_PINV	TBTDP_90D	TBTDP	TBT_A_R2D_C_P<1>	NO_TEST=TRUE	36 86
1635	TBTDP_90D	TBTDP	TBT_A_R2D_P<1..0>	NO_TEST=TRUE	86
1636	TBTDP_90D	TBTDP	TBT_A_R2D_N<1..0>	NO_TEST=TRUE	86
1638 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	NO_TEST=TRUE	36 86
1639 DP_TBTPA_ML1	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	NO_TEST=TRUE	36 86
1680 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	NO_TEST=TRUE	36 86
1681 DP_TBTPA_ML3	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	NO_TEST=TRUE	36 86
1546	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	NO_TEST=TRUE	86
1547	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	NO_TEST=TRUE	86
1670	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	NO_TEST=TRUE	86
1671	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	NO_TEST=TRUE	86
1536	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>		86
1538	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>		86
1549	TBTDP_90D	TBTDP	TBT_A_D2R_C_P<1..0>	NO_TEST=TRUE	86
1550	TBTDP_90D	TBTDP	TBT_A_D2R_C_N<1..0>	NO_TEST=TRUE	86
1554 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_P<1>	NO_TEST=TRUE	36 86
1555 TBT_A_D2R1	TBTDP_90D	TBTDP	TBT_A_D2R_N<1>	NO_TEST=TRUE	36 86
1646 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_P<0>	NO_TEST=TRUE	36 86
1647 TBT_A_D2R0	TBTDP_90D	TBTDP	TBT_A_D2R_N<0>	NO_TEST=TRUE	36 86
1639 DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_P		36 86
1640 DP_TBT_A_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_C_N		36 86
1555	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_P		86
1556	DP_85D	DISPLAYPORT	DP_TBTPA_AUXCH_N		86
1641	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_P		86
1642	DP_85D	DISPLAYPORT	DP_A_AUXCH_DDC_N		86
1650	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_P	NO_TEST=TRUE	86
1651	TBTDP_90D	TBTDP	TBT_A_D2R1_AUXDDC_N	NO_TEST=TRUE	86
Port B					
1652 TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_P<1..0>	NO_TEST=TRUE	36 88
1653 TBT_B_R2D	TBTDP_90D	TBTDP	TBT_B_R2D_C_N<1..0>	NO_TEST=TRUE	36 88
1655	TBTDP_90D	TBTDP	TBT_B_R2D_P<1..0>	NO_TEST=TRUE	88
1654	TBTDP_90D	TBTDP	TBT_B_R2D_N<1..0>	NO_TEST=TRUE	88
1657 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	NO_TEST=TRUE	36 88
1658 DP_TBTPB_ML1	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	NO_TEST=TRUE	36 88
1685 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	NO_TEST=TRUE	36 88
1684 DP_TBTPB_ML3	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	NO_TEST=TRUE	36 88
1663	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	NO_TEST=TRUE	88
1665	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	NO_TEST=TRUE	88
1668	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	NO_TEST=TRUE	88
1669	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	NO_TEST=TRUE	88
1529	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	NO_TEST=TRUE	88
1532	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	NO_TEST=TRUE	88
1543	TBTDP_90D	TBTDP	TBT_B_D2R_C_P<1..0>	NO_TEST=TRUE	88
1544	TBTDP_90D	TBTDP	TBT_B_D2R_C_N<1..0>	NO_TEST=TRUE	88
1560 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_P<1>	NO_TEST=TRUE	36 88
1561 TBT_B_D2R1	TBTDP_90D	TBTDP	TBT_B_D2R_N<1>	NO_TEST=TRUE	36 88
1677 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_P<0>	NO_TEST=TRUE	36 88
1678 TBT_B_D2R0	TBTDP_90D	TBTDP	TBT_B_D2R_N<0>	NO_TEST=TRUE	36 88
1643 DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_P		36 88
1644 DP_TBT_B_AUXCH	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_C_N		36 88
1645	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_P		88
1646	DP_85D	DISPLAYPORT	DP_TBTPB_AUXCH_N		88
1648	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_P		88
1649	DP_85D	DISPLAYPORT	DP_B_AUXCH_DDC_N		88
1671	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_P	NO_TEST=TRUE	88
1672	TBTDP_90D	TBTDP	TBT_B_D2R1_AUXDDC_N	NO_TEST=TRUE	88

DisplayPort

Electrical Contraint Set	Physical	Spacing			
Graphics Source					
1640 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>	NO_TEST=TRUE	81 84
1642 DP_INTPNL_EG_ML_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>	NO_TEST=TRUE	81 84
1644 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P	NO_TEST=TRUE	81 84
1645 DP_INTPNL_EG_AUX_MUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N	NO_TEST=TRUE	81 84
1640	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_P		84
1642	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_C_N		84
Internal Panel					
1600	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_P<3..0>	NO_TEST=TRUE	84
1602	DP_85D	DISPLAYPORT	DP_INTPNL_ML_C_N<3..0>	NO_TEST=TRUE	84
1603 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_P<3..0>	NO_TEST=TRUE	84 87
1605 DP_INTPNL_ML_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_ML_N<3..0>	NO_TEST=TRUE	84 87
1608 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_P		84 87
1610 DP_INTPNL_AUX_CONN	DP_85D	DISPLAYPORT	DP_INTPNL_AUX_N		84 87
Internal DP SPDIF					
1611		HDA	DP_INT_SPDIF_AUDIO		56 87

SYNC_MASTER=D8 AARON SYNC_DATE=03/13/2012

PAGE TITLE
TBT/DP Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 131 OF 143
SHEET 107 OF 117

GDDR5

GDDR5-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
GDDR_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12 MM	=STANDARD	=STANDARD
GDDR_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GDDR_MA_PHY	*	GDDR_45S
GDDR_ADBI_PHY	*	GDDR_45S
GDDR_CTRL_PHY	*	GDDR_45S
GDDR_CLK_PHY	*	GDDR_80D
GDDR_DQ_PHY	*	GDDR_45S
GDDR_EDC_PHY	*	GDDR_45S
GDDR_DBI_PHY	*	GDDR_45S
GDDR_WCK_PHY	*	GDDR_80D

Main Segment Min Spacing Rules for 4.5 Gbps or Less (AMD Doc# 49919)

	Trace-to-Trace				Isolation				
Table	Micro	Design	Strip	Design	Micro	Design	Strip	Design	Comments
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Memory address (MA). Implented 4.5 Gbps or less rules for K70.
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Address dynamic bus inversion (ADBI)
5-6/5-7	2:1	2:1	2:1	2:1	5:1	5:1	5:1	5:1	Control (CTRL)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Clock (CLK)
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data (DQ)
5-6/5-7	7:1	7:1	7:1	7:1	7:1	7:1	7:1	7:1	Error detection pins (EDC). Using larger isolation rules,
5-6/5-7	3:1	3:1	3:1	3:1	5:1	5:1	5:1	5:1	Data dynamic bus inversion (DBI)
5-6/5-7	5:1	5:1	5:1	5:1	5:1	5:1	5:1	5:1	Forwarded clock (WCK)

GDDR5-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_ISO	*	=3X_DIELECTRIC	?
GDDR_ISO	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR_MA2MA	*	=2x_DIELECTRIC	?
GDDR_MA2MA	TOP,BOTTOM	=3X_DIELECTRIC	?
GDDR_ADBI2ADBI	*	=2x_DIELECTRIC	?
GDDR_ADBI2ADBI	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	*	=2x_DIELECTRIC	?
GDDR_CTRL2CTRL	TOP,BOTTOM	=2x_DIELECTRIC	?
GDDR_CLK2CLK	*	=3X_DIELECTRIC	?
GDDR_CLK2CLK	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR_DQ2DQ	*	=3x_DIELECTRIC	?
GDDR_DQ2DQ	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_EDC_ISO	*	=3X_DIELECTRIC	?
GDDR_EDC_ISO	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_EDC2EDC	*	=3X_DIELECTRIC	?
GDDR_EDC2EDC	TOP,BOTTOM	=5X_DIELECTRIC	?
GDDR_DBI2DBI	*	=3x_DIELECTRIC	?
GDDR_DBI2DBI	TOP,BOTTOM	=3x_DIELECTRIC	?
GDDR_WCK2WCK	*	=3X_DIELECTRIC	?
GDDR_WCK2WCK	TOP,BOTTOM	=5x_DIELECTRIC	?

Constraints (x in {A, B}, y in {0, 1})

Memory Address: MAxy[8:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_MA	*	*	GDDR_ISO
GDDR_*_*_MA	=SAME	*	GDDR_MA2MA

Data: DQxy[31:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DQ	*	*	GDDR_ISO
GDDR_*_*_DQ	=SAME	*	GDDR_DQ2DQ

Address Dynamic Bus Inversion: ADBIxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_ADBI	*	*	GDDR_ISO
GDDR_*_*_ADBI	=SAME	*	GDDR_ADBI2ADBI

Error Detection: EDCxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_EDC	*	*	GDDR_EDC_ISO
GDDR_*_*_EDC	=SAME	*	GDDR_EDC2EDC

Control: Reset, CKExy, CSxy, WExy, RASxy, CASxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	*	*	GDDR_ISO
GDDR_*_*_CTRL	=SAME	*	GDDR_CTRL2CTRL

Data Dynamic Bus Inversion: DDBIxy[3:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_DBI	*	*	GDDR_ISO
GDDR_*_*_DBI	=SAME	*	GDDR_DBI2DBI

Clock: CKxy

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_CLK	*	*	GDDR_ISO
GDDR_*_*_CLK	=SAME	*	GDDR_CLK2CLK

Forwarded Clock: WCKxy[1:0]

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GDDR_*_*_WCK	*	*	GDDR_ISO
GDDR_*_*_WCK	=SAME	*	GDDR_WCK2WCK

GPU

GPU-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_GPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

GPU-specific Spacing Definitions

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_GPU_ISO	*	=4:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_GPU	*	*	CLK_GPU_ISO

GDDR5 Frame Buffer A

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1642 GDDR_A0_MA	GDDR_MA_PHY	GDDR_A_0_MA	FB_A0_A<8..0>	NO_TEST=TRUE	?? 79
1643 GDDR_A1_MA	GDDR_MA_PHY	GDDR_A_1_MA	FB_A1_A<8..0>	NO_TEST=TRUE	?? 79
Address Dynamic Bus Inv					
1644 GDDR_A0_ADBI	GDDR_ADBI_PHY	GDDR_A_0_ADBI	FB_A0_ABI_L	NO_TEST=TRUE	?? 79
1645 GDDR_A1_ADBI	GDDR_ADBI_PHY	GDDR_A_1_ADBI	FB_A1_ABI_L	NO_TEST=TRUE	?? 79
Control					
1646 GDDR_A0_CKE	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CKE_L	NO_TEST=TRUE	?? 79
1648 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CS_L	NO_TEST=TRUE	?? 79
1649 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_WE_L	NO_TEST=TRUE	?? 79
1650 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_CAS_L	NO_TEST=TRUE	?? 79
1651 GDDR_A0_CTRL	GDDR_CTRL_PHY	GDDR_A_0_CTRL	FB_A0_RAS_L	NO_TEST=TRUE	?? 79
1652 GDDR_A1_CKE	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CKE_L	NO_TEST=TRUE	?? 79
1654 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CS_L	NO_TEST=TRUE	?? 79
1653 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_WE_L	NO_TEST=TRUE	?? 79
1655 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_CAS_L	NO_TEST=TRUE	?? 79
1656 GDDR_A1_CTRL	GDDR_CTRL_PHY	GDDR_A_1_CTRL	FB_A1_RAS_L	NO_TEST=TRUE	?? 79
Clock					
1657 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_P	NO_TEST=TRUE	?? 79
1658 GDDR_A0_CLK	GDDR_CLK_PHY	GDDR_A_0_CLK	FB_A0_CLK_N	NO_TEST=TRUE	?? 79
1660 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_P	NO_TEST=TRUE	?? 79
1659 GDDR_A1_CLK	GDDR_CLK_PHY	GDDR_A_1_CLK	FB_A1_CLK_N	NO_TEST=TRUE	?? 79
Data					
1661 GDDR_A0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<7..0>	NO_TEST=TRUE	?? 79
1662 GDDR_A0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<15..8>	NO_TEST=TRUE	?? 79
1663 GDDR_A0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<23..16>	NO_TEST=TRUE	?? 79
1664 GDDR_A0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_0_DQ	FB_A0_DQ<31..24>	NO_TEST=TRUE	?? 79
1666 GDDR_A1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<7..0>	NO_TEST=TRUE	?? 79
1665 GDDR_A1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<15..8>	NO_TEST=TRUE	?? 79
1667 GDDR_A1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<23..16>	NO_TEST=TRUE	?? 79
1668 GDDR_A1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_A_1_DQ	FB_A1_DQ<31..24>	NO_TEST=TRUE	?? 79
Error Detection					
1670 GDDR_A0_EDC0	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<0>	NO_TEST=TRUE	?? 79
1669 GDDR_A0_EDC1	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<1>	NO_TEST=TRUE	?? 79
1671 GDDR_A0_EDC2	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<2>	NO_TEST=TRUE	?? 79
1672 GDDR_A0_EDC3	GDDR_EDC_PHY	GDDR_A_0_EDC	FB_A0_EDC<3>	NO_TEST=TRUE	?? 79
1673 GDDR_A1_EDC0	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<0>	NO_TEST=TRUE	?? 79
1674 GDDR_A1_EDC1	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<1>	NO_TEST=TRUE	?? 79
1676 GDDR_A1_EDC2	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<2>	NO_TEST=TRUE	?? 79
1675 GDDR_A1_EDC3	GDDR_EDC_PHY	GDDR_A_1_EDC	FB_A1_EDC<3>	NO_TEST=TRUE	?? 79
Data Dynamic Bus Inv					
1677 GDDR_A0_DBI0	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<0>	NO_TEST=TRUE	?? 79
1678 GDDR_A0_DBI1	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<1>	NO_TEST=TRUE	?? 79
1680 GDDR_A0_DBI2	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<2>	NO_TEST=TRUE	?? 79
1679 GDDR_A0_DBI3	GDDR_DBI_PHY	GDDR_A_0_DBI	FB_A0_DBI_L<3>	NO_TEST=TRUE	?? 79
1682 GDDR_A1_DBI0	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<0>	NO_TEST=TRUE	?? 79
1683 GDDR_A1_DBI1	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<1>	NO_TEST=TRUE	?? 79
1685 GDDR_A1_DBI2	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<2>	NO_TEST=TRUE	?? 79
1684 GDDR_A1_DBI3	GDDR_DBI_PHY	GDDR_A_1_DBI	FB_A1_DBI_L<3>	NO_TEST=TRUE	?? 79
Forwarded Clock					
1688 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<0>	NO_TEST=TRUE	?? 79
1689 GDDR_A0_WCK0	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<0>	NO_TEST=TRUE	?? 79
1686 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_P<1>	NO_TEST=TRUE	?? 79
1687 GDDR_A0_WCK1	GDDR_WCK_PHY	GDDR_A_0_WCK	FB_A0_WCLK_N<1>	NO_TEST=TRUE	?? 79
1690 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<0>	NO_TEST=TRUE	?? 79
1691 GDDR_A1_WCK0	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<0>	NO_TEST=TRUE	?? 79
1692 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_P<1>	NO_TEST=TRUE	?? 79
1693 GDDR_A1_WCK1	GDDR_WCK_PHY	GDDR_A_1_WCK	FB_A1_WCLK_N<1>	NO_TEST=TRUE	?? 79

GDDR5 Frame Buffer B

Electrical Contraint Set	Physical	Spacing			
Memory Address					
1695 GDDR_B0_MA	GDDR_MA_PHY	GDDR_B_0_MA	FB_B0_A<8..0>	NO_TEST=TRUE	?? 80
1694 GDDR_B1_MA	GDDR_MA_PHY	GDDR_B_1_MA	FB_B1_A<8..0>	NO_TEST=TRUE	?? 80
Address Dynamic Bus Inv					
1696 GDDR_B0_ADBI	GDDR_ADBI_PHY	GDDR_B_0_ADBI	FB_B0_ABI_L	NO_TEST=TRUE	?? 80
1697 GDDR_B1_ADBI	GDDR_ADBI_PHY	GDDR_B_1_ADBI	FB_B1_ABI_L	NO_TEST=TRUE	?? 80
Control					
1698 GDDR_B0_CKE	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CKE_L	NO_TEST=TRUE	?? 80
1700 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CS_L	NO_TEST=TRUE	?? 80
1701 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_WE_L	NO_TEST=TRUE	?? 80
1702 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_CAS_L	NO_TEST=TRUE	?? 80
1703 GDDR_B0_CTRL	GDDR_CTRL_PHY	GDDR_B_0_CTRL	FB_B0_RAS_L	NO_TEST=TRUE	?? 80
1706 GDDR_B1_CKE	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CKE_L	NO_TEST=TRUE	?? 80
1705 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CS_L	NO_TEST=TRUE	?? 80
1704 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_WE_L	NO_TEST=TRUE	?? 80
1708 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_CAS_L	NO_TEST=TRUE	?? 80
1707 GDDR_B1_CTRL	GDDR_CTRL_PHY	GDDR_B_1_CTRL	FB_B1_RAS_L	NO_TEST=TRUE	?? 80
Clock					
1709 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_P	NO_TEST=TRUE	?? 80
1710 GDDR_B0_CLK	GDDR_CLK_PHY	GDDR_B_0_CLK	FB_B0_CLK_N	NO_TEST=TRUE	?? 80
1712 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_P	NO_TEST=TRUE	?? 80
1711 GDDR_B1_CLK	GDDR_CLK_PHY	GDDR_B_1_CLK	FB_B1_CLK_N	NO_TEST=TRUE	?? 80
Data					
1713 GDDR_B0_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<7..0>	NO_TEST=TRUE	?? 80
1714 GDDR_B0_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<15..8>	NO_TEST=TRUE	?? 80
1716 GDDR_B0_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<23..16>	NO_TEST=TRUE	?? 80
1715 GDDR_B0_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_0_DQ	FB_B0_DQ<31..24>	NO_TEST=TRUE	?? 80
1719 GDDR_B1_DQ_BYTE0	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<7..0>	NO_TEST=TRUE	?? 80
1718 GDDR_B1_DQ_BYTE1	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<15..8>	NO_TEST=TRUE	?? 80
1717 GDDR_B1_DQ_BYTE2	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<23..16>	NO_TEST=TRUE	?? 80
1720 GDDR_B1_DQ_BYTE3	GDDR_DQ_PHY	GDDR_B_1_DQ	FB_B1_DQ<31..24>	NO_TEST=TRUE	?? 80
Error Detection					
1720 GDDR_B0_EDC0	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<0>	NO_TEST=TRUE	?? 80
1721 GDDR_B0_EDC1	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<1>	NO_TEST=TRUE	?? 80
1723 GDDR_B0_EDC2	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<2>	NO_TEST=TRUE	?? 80
1722 GDDR_B0_EDC3	GDDR_EDC_PHY	GDDR_B_0_EDC	FB_B0_EDC<3>	NO_TEST=TRUE	?? 80
1725 GDDR_B1_EDC0	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<0>	NO_TEST=TRUE	?? 80
1724 GDDR_B1_EDC1	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<1>	NO_TEST=TRUE	?? 80
1726 GDDR_B1_EDC2	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<2>	NO_TEST=TRUE	?? 80
1727 GDDR_B1_EDC3	GDDR_EDC_PHY	GDDR_B_1_EDC	FB_B1_EDC<3>	NO_TEST=TRUE	?? 80
Data Dynamic Bus Inv					
1729 GDDR_B0_DBI0	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<0>	NO_TEST=TRUE	?? 80
1728 GDDR_B0_DBI1	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<1>	NO_TEST=TRUE	?? 80
1730 GDDR_B0_DBI2	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<2>	NO_TEST=TRUE	?? 80
1731 GDDR_B0_DBI3	GDDR_DBI_PHY	GDDR_B_0_DBI	FB_B0_DBI_L<3>	NO_TEST=TRUE	?? 80
1732 GDDR_B1_DBI0	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<0>	NO_TEST=TRUE	?? 80
1733 GDDR_B1_DBI1	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<1>	NO_TEST=TRUE	?? 80
1734 GDDR_B1_DBI2	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<2>	NO_TEST=TRUE	?? 80
1735 GDDR_B1_DBI3	GDDR_DBI_PHY	GDDR_B_1_DBI	FB_B1_DBI_L<3>	NO_TEST=TRUE	?? 80
Forwarded Clock					
1736 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<0>	NO_TEST=TRUE	?? 80
1737 GDDR_B0_WCK0	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<0>	NO_TEST=TRUE	?? 80
1739 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_P<1>	NO_TEST=TRUE	?? 80
1738 GDDR_B0_WCK1	GDDR_WCK_PHY	GDDR_B_0_WCK	FB_B0_WCLK_N<1>	NO_TEST=TRUE	?? 80
1740 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<0>	NO_TEST=TRUE	?? 80
1741 GDDR_B1_WCK0	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<0>	NO_TEST=TRUE	?? 80
1743 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_P<1>	NO_TEST=TRUE	?? 80
1742 GDDR_B1_WCK1	GDDR_WCK_PHY	GDDR_B_1_WCK	FB_B1_WCLK_N<1>	NO_TEST=TRUE	?? 80

GPU

Electrical Contraint Set	Physical	Spacing			
Clocks					
1744	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_PL		75
1745	CLK_GPU_55S	CLK_GPU	PEX_TSTCLK_O_NG		75
1749	CLK_PCIE_PHY	CLK_PCIE	GPU_TESTMODE		81
1750	CLK_PCIE_PHY	CLK_PCIE	GPU_PEX_TERMP		75
1756	CLK_GPU_55S	CLK_GPU	FB_A0_CK_MID	NO_TEST=TRUE	79
1754	CLK_GPU_55S	CLK_GPU	FB_A1_CK_MID	NO_TEST=TRUE	79
1755	CLK_GPU_55S	CLK_GPU	FB_B0_CK_MID	NO_TEST=TRUE	80
1764	CLK_GPU_55S	CLK_GPU	FB_B1_CK_MID	NO_TEST=TRUE	80
1765	CLK_GPU_55S	CLK_GPU	FB_C0_CK_MID	NO_TEST=TRUE	
1766	CLK_GPU_55S	CLK_GPU	FB_C1_CK_MID	NO_TEST=TRUE	ULTIMATE
1767	CLK_GPU_55S	CLK_GPU	FB_D0_CK_MID	NO_TEST=TRUE	ONLY
1770	CLK_GPU_55S	CLK_GPU	FB_D1_CK_MID	NO_TEST=TRUE	
1771	CLK_GPU_55S	CLK_GPU	GPU_JTAG_TCK		78 81
1772	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK		81 82
1773	CLK_GPU_55S	CLK_GPU	GPU_ROM_SCLK_R		82
1775	CLK_GPU_55S	CLK_GPU	GPU_XTALOUT		
1774	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALOUT		81 82
1776	CLK_GPU_55S	CLK_GPU	GPU_OSC_27M_XTALIN		81 82
SMB					
1754	SMB_PHY	SMB	GPU_SMB_CLK		81 82
1753	SMB_PHY	SMB	GPU_SMB_DAT		81 82
1751	SMB_PHY	SMB	GPU_SMB_CLK_R		50 82
1752	SMB_PHY	SMB	GPU_SMB_DAT_R		50 82
PCIe Compensation					
1752	PCIE_50S	COMP_PCIE	FB_CAL_PD_VDDQ		??
1760	PCIE_50S	COMP_PCIE	FB_CAL_PU_GND		??
1762	PCIE_50S	COMP_PCIE	FB_CAL_TERM_GND		??

Frame Buffer Reset

Electrical Contraint Set	Physical	Spacing		
Reset				
1744 GDDR_A0_RESET	GDDR_50S	GDDR_CTRL	FB_A0_RESET_L	?? 79
1745 GDDR_A1_RESET	GDDR_50S	GDDR_CTRL	FB_A1_RESET_L	?? 79
1750 GDDR_B0_RESET	GDDR_50S	GDDR_CTRL	FB_B0_RESET_L	?? 80
1749 GDDR_B1_RESET	GDDR_50S	GDDR_CTRL	FB_B1_RESET_L	?? 80
1765 GDDR_C0_RESET	GDDR_50S	GDDR_CTRL	FB_C0_RESET_L	
1755 GDDR_C1_RESET	GDDR_50S	GDDR_CTRL	FB_C1_RESET_L	ULTIMATE
1760 GDDR_D0_RESET	GDDR_50S	GDDR_CTRL	FB_D0_RESET_L	ONLY
1767 GDDR_D1_RESET	GDDR_50S	GDDR_CTRL	FB_D1_RESET_L	

SYNC MASTER=D8 AARON SYNC DATE=03/13/2012

PAGE TITLE
GDDR5/GPU Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 132 OF 143

SHEET 108 OF 117

Backlight Controller

BLC-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BLC_P6MM	*	Y	0.600 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD
BLC_P3MM	*	Y	0.300 MM	0.100 MM	3.0 MM	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
POWER_BLC	*	BLC_P6MM
POWER_BLC_RET	*	BLC_P3MM
BLC_CTL_PHY	*	BLC_P3MM

BLC-specific Spacing Definitions

BLC High Voltage Output

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_HV_ISO	*	1.00MM	1000

Constraints

BLC High Voltage Output

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_HV	BLC_HV	*	BLC_CTL_ISO
BLC_HV	*	*	BLC_HV_ISO

BLC Baddies

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PHASE_ISO	*	=8:1_SPACING	2000
PHASE_SW2SW	*	=1:1_SPACING	?
PHASE_SW2PWR	*	=2:1_SPACING	?
PHASE_SW2GND	*	=2:1_SPACING	?

BLC Baddies

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_PHASE	*	*	PHASE_ISO
BLC_PHASE	BLC_PHASE	*	PHASE_SW2SW
BLC_PHASE	POWER	*	PHASE_SW2PWR
BLC_PHASE	GND	*	PHASE_SW2GND

BLC Control

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
BLC_CTL_ISO	*	=3:1_SPACING	?

BLC Control

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BLC_CTL	*	*	BLC_CTL_ISO

BKLT MISCELLANEOUS

Electrical Contraint Set	Physical	Spacing		
SPI				
B56	SMB_PHY	SMB	SMB_PCH_BLC_SCL	50 89
B56	SMB_PHY	SMB	SMB_PCH_BLC_SDA	50 89
B81	SMB_PHY	SMB	SMB_TCON_BLC_SCL	50 89
B81	SMB_PHY	SMB	SMB_TCON_BLC_SDA	50 89
12M REFERENCE CRYSTAL				
B84	CLK_XTAL	XTAL	BLC_MCU_XTAL_IN	89
B84	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT	89
B84	CLK_XTAL	XTAL	BLC_MCU_XTAL_OUT_R	89
250K REFERENCE CLOCKS				
B85	CLK_PCH_50S	CLK_PCH	STRCLK_R1	89 90
B86	CLK_PCH_50S	CLK_PCH	LED_DRVR_CLK	90

	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
B900	POWER_PHY	POWER	12V			PP12V_S0_BLC_VIN2	89 90 91
B902	POWER_PHY	POWER	12V			PP12V_S0_BLC_VINP	89 91
B906	POWER_PHY	POWER	14V			PRE_REG_OUT	89 90
B907	POWER_PHY	POWER	3.3V			BLC_P3V3S	89 91
B908	POWER_PHY	POWER	3.3V			BLC_P3V3_REF	89 91
B909	POWER_PHY	POWER	3.3V			BLC_P3V3	
B910	POWER_PHY	POWER	3.3V			PP3V3_S0_BLC_R	89
B911	POWER_PHY	POWER	8V			SPTX_VIN	90
B913	POWER_PHY	POWER	8V			PP8V_BLC	89 90
B914	POWER_PHY	POWER	8V			BLC_VIN2	90 91
B922	POWER_PHY	POWER	14V			BOOST_FET_DRAIN	89
B923	POWER_PHY	POWER	12V			BOOST_VDD	89
B925	POWER_PHY	POWER	5V			PP5V_S0_BLC_R	89 90 91
B926	POWER_PHY	POWER	12V			PP12V_S0_BLC_F	91
Local Ground							
B901	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_1	90 91
B904	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_2	90 91
B905	BLC_CTL_PHY	BLC_PHASE	0V			BLC_GND_3	90 91
B918	GND_PHY	GND	0V			AGND_BLC	90 91
Backlight							
B955	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1	90
B956	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE1_R	90
B976	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2	90
B977	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE2_R	90
B978	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3	90
B979	BLC_CTL_PHY	BLC_PHASE				LED_DRIVER_GATE3_R	90
B975	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_1	90
B974	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_2	90
B976	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_RC_3	90
B957	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS1	90
B958	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS2	90
B959	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_CS3	90
B973	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C1	90
B972	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C2	90
B971	BLC_CTL_PHY	BLC_CTL				LED_DRVR_CS_C3	90
B933	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_1	90
B932	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_2	90
B931	BLC_CTL_PHY	BLC_HV	80V			LED_DRIVER_FDBK_R_3	90
B930	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK1	90
B929	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK2	90
B928	BLC_CTL_PHY	BLC_CTL	80V			LED_DRIVER_FDBK3	90
B943	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1_R	89 90
B946	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2_R	89 90
B947	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3_R	89 90
B940	BLC_CTL_PHY	BLC_CTL				BLC_PWM_1	90 91
B939	BLC_CTL_PHY	BLC_CTL				BLC_PWM_2	90 91
B938	BLC_CTL_PHY	BLC_CTL				BLC_PWM_3	90 91
B960	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF1	90 91
B963	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF2	90 91
B962	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_REF3	90 91
B950	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP1	90
B949	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP2	90
B948	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_COMP3	90
B952	BLC_CTL_PHY	BLC_CTL				BCOMP1	90
B953	BLC_CTL_PHY	BLC_CTL				BCOMP2	90
B954	BLC_CTL_PHY	BLC_CTL				BCOMP3	90
B945	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT1	90
B944	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT2	90
B942	BLC_CTL_PHY	BLC_CTL				LED_DRIVER_FLT3	90
B935	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_1	90
B934	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_2	90
B936	BLC_CTL_PHY	BLC_CTL				LED_FLT_R_3	90
B966	BLC_CTL_PHY	BLC_CTL				PRE_REG_OUT_R	89
B965	BLC_CTL_PHY	BLC_CTL				BOOST_FB	89
B964	BLC_CTL_PHY	BLC_CTL				BOOST_COMP	89
B967	BLC_CTL_PHY	BLC_CTL				BOOST_COMP_C	89
B968	BLC_CTL_PHY	BLC_CTL		TRUE		BOOST_GDRV	89
B969	BLC_CTL_PHY	BLC_CTL		TRUE		BOOST_GDRV_R	89
B970	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS	89
B980	BLC_CTL_PHY	BLC_CTL				BOOST_ISNS_R	89
B750	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_1	90
B751	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_2	90
B752	BLC_CTL_PHY	BLC_HV	80V			LED_DRVR_DRAIN_3	90
OUTPUT BUS							
B780	POWER_BLC_RET	BLC_HV	80V			IS1_BLC_F	91
B781	POWER_BLC_RET	BLC_HV	80V			IS2_BLC_F	91
B782	POWER_BLC_RET	BLC_HV	80V			IS3_BLC_F	91
B791	POWER_BLC_RET	BLC_HV	80V			IS1_BLC	90 91
B792	POWER_BLC_RET	BLC_HV	80V			IS2_BLC	90 91
B793	POWER_BLC_RET	BLC_HV	80V			IS3_BLC	90 91
B783	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_1	91
B784	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_1	91
B785	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_2	91
B786	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_2	91
B787	POWER_BLC_RET	BLC_HV	80V			BLC_LED_P_3	91
B788	POWER_BLC_RET	BLC_HV	80V			BLC_LED_N_3	91
B825	POWER_BLC	BLC_HV	80V			BLC_VOUT1	90 91
B824	POWER_BLC	BLC_HV	80V			BLC_VOUT2	90 91
B823	POWER_BLC	BLC_HV	80V			BLC_VOUT3	90 91

SYNC MASTER=D8 MLB SYNC DATE=12/19/2011

PAGE TITLE

BLC Constraints

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 134 OF 143

SHEET 109 OF 117

GPU CORE PHASES

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
8186	POWER_PHY	POWER	12V			PP12V_S0_GPUCORE_FLT	92 93 94
8186	POWER_PHY	POWER	5V			PP5V_S0_GPU_VCORE_VCC	92
Local Ground							
8186	GND_PHY	GND	0V			AGND_GPU	92
Phase 1							
8186	POWER_PHY	POWER	12V			REG_LVCC_UB510	93
8186	POWER_PHY	POWER	12V			REG_UVCC_UB510	93
8186	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_1	92 93
8186	VR_CTL_PHY	VR_CTL				VR_GPU_PWM1_R	92
8186	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_1	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_1	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_1_RC	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_1	93
8186	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_1	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_1	93
8186	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_1	93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_P	92 93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_1_N	92 93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_P	92
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS1_R_N	92
8186 ISNS_GPU_CORE		SENSE				VR_GPU_ISNS1_RR_2	92
Phase 2							
8186	POWER_PHY	POWER	12V			REG_LVCC_UB530	93
8186	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_2	92 93
8186	VR_CTL_PHY	VR_CTL				VR_GPU_PWM2_R	92
8186	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_2	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_2	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_2_RC	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_2	93
8186	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_2	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_2	93
8186	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_2	93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_P	92 93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_2_N	92 93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_P	92
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS2_R_N	92
8186 ISNS_GPU_CORE		SENSE				VR_GPU_ISNS2_RR_2	92
Phase 3							
8186	POWER_PHY	POWER	12V			REG_VCC_UB550	93
8186	POWER_PHY	POWER	12V			REG_UVCC_UB550	93
8186	POWER_PHY	POWER	12V			REG_LVCC_UB550	93
8186	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_3	92 93
8186	VR_CTL_PHY	VR_CTL				VR_GPU_PWM3_R	92
8186	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_3	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_3	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_3_RC	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_3	93
8186	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_3	93
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_3	93
8186	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_3	93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_P	92 93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_3_N	92 93
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_P	92
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS3_R_N	92
8186 ISNS_GPU_CORE		SENSE				VR_GPU_ISNS3_RR_2	92
Phase 4							
8186	POWER_PHY	POWER	12V			REG_LVCC_UB650	94
8186	VR_CTL_PHY	VR_CTL				REG_PWM_GPUCORE_4	92 94
8186	VR_CTL_PHY	VR_CTL				VR_GPU_PWM4_R	92
8186	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_GPUCORE_4	94
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_GPUCORE_4	94
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_GPUCORE_4_RC	94
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_GPUCORE_4	94
8186	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_GPUCORE_4	94
8186	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_GPUCORE_4	94
8186	POWER_PHY	POWER	0.9V			PPGPUCORE_S0_SENSE_4	94
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_P	92 94
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				REG_ISEN_GCORE_4_N	92 94
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_P	92
8186 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VR_GPU_ISNS4_R_N	92
8186 ISNS_GPU_CORE		SENSE				VR_GPU_ISNS4_RR_2	92

GPU CORE CONTROLLER

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
ISL6334							
8142	VR_CTL_PHY	VR_CTL				VR_GPU_COMP	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_R	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_COMP_RC	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_FB	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_FB_R	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_VDIFF	92
8142	VR_CTL_PHY	VR_CTL				VR_VDF_R1	92
8142	VR_CTL_PHY	VR_CTL				VR_VDF_R2	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_TCOMP	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_OFS	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_FS	92
8142		VR_CTL				VR_GPU_EN_VTT	92
8142		VR_CTL				PM_EN_REG_GPUCORE_S0	64 92
8142		VR_CTL				PM_PGOOD_REG_GPUCORE_S0	5 64 92
8142		VR_CTL				GPU_PSI_L	82 92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_IOUT	
8142	VR_CTL_PHY	VR_CTL				VR_GPU_IMON	51 92 110
8142	VR_CTL_PHY	VR_CTL				VR_GPU_FAN	92 110
8142		VR_CTL				VR_GPU_VRDHOT	92
8142		VR_CTL				VR_GPU_EN_PWR	
8142	VR_CTL_PHY	VR_CTL				VR_GPU_SS	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_DAC	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_REF	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_TM	92
8142	VR_CTL_PHY	VR_CTL				VR_GPU_IMON	51 92 110
8142	VR_CTL_PHY	VR_CTL				VR_GPU_FAN	92 110
8142	VR_CTL_PHY	VR_CTL				VR_GPU_VRHOT	
8142		VR_CTL				GPU_PSI_R	
8142		VR_CTL				GPU_PSI_L_R	
8142	VR_CTL_PHY	VR_CTL				VR_GPU_IMON_R	92
8137 VSNS_GPU_VDD	SNS_DIFF_PHY	SENSE				VSNS_GPU_VDD	78 92
8137 VSNS_GPU_VSS	SNS_DIFF_PHY	SENSE				VSNS_GPU_VSS	78 92
8137	SNS_DIFF_PHY	SENSE				VR_GPU_VSEN	92
8137	SNS_DIFF_PHY	SENSE				VR_GPU_RGND	92
GPU VIDS							
8142		VR_VID				REG_GPUCORE_VID7	92
8142		VR_VID				REG_GPUCORE_VID6	78 92
8142		VR_VID				REG_GPUCORE_VID5	78 92
8142		VR_VID				REG_GPUCORE_VID4	78 92
8142		VR_VID				REG_GPUCORE_VID3	78 92
8142		VR_VID				REG_GPUCORE_VID2	78 92
8142		VR_VID				REG_GPUCORE_VID1	78 92
8142		VR_VID				REG_GPUCORE_VID0	92
8142		VR_VID				GPU_VCORE_VID6	
8142		VR_VID				GPU_VCORE_VID5	78 82
8142		VR_VID				GPU_VCORE_VID4	78 82
8142		VR_VID				GPU_VCORE_VID3	78 82
8142		VR_VID				GPU_VCORE_VID2	78 82
8142		VR_VID				GPU_VCORE_VID1	78 82
8142		VR_VID				GPU_VCORE_VID0	78 82
Output Bus							
8142	POWER_PHY	POWER	0.9V			PPVCORE_S0_GPU	6

GPU FBVDDQ

Electrical Contraint Set	Physical	Spacing	Voltage	DIDT	NO_TEST		
Input Bus							
8145	POWER_PHY	POWER	5V			REG_VCC_UB750	95
8145	POWER_PHY	POWER	5V			REG_PVCC_UB750	95
Local Ground							
8145	GND_PHY	GND	0V			AGND_FBVDDQ	95
FBVDDQ							
8145	POWER_PHY	VR_SWITCH	12V	TRUE		REG_PHASE_FBVDDQ	95
8145	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_BOOT_FBVDDQ	95
8145	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_BOOT_FBVDDQ_RC	95
8145	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ	95
8145	VR_CTL_PHY	VR_SWITCH	12V	TRUE		REG_UGATE_FBVDDQ_R	
8145	VR_CTL_PHY	VR_LGATE	12V	TRUE		REG_LGATE_FBVDDQ	95
8145	VR_CTL_PHY	VR_SWITCH	12V	TRUE	TRUE	REG_SNUBBER_FBVDDQ	95
8145		SENSE				VSNS_FBVDDQ	
8145 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_P	78 95
8145 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				VSNS_FBVDDQ_N	78 95
8145 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_P	95
8145 ISNS_GPU_CORE	SNS_DIFF_PHY	SENSE				SNS_FBVDDQ_XW_N	95
8145		SENSE				FBVDDQ_SENSE_R	
8145	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_OCSET	
8145	VR_CTL_PHY	VR_CTL				REG_FBVDDQ_VO	95
8145		SENSE				REG_FBVDDQ_FB	95
8145		SENSE				REG_FBVDDQ_RTN	95
Output Bus							
8145	POWER_PHY	POWER	1.5V			PP1V5R1V35_S0_GPU_REG	6 95

SYNC MASTER=D8 MARK SYNC DATE=02/10/2012

PAGE TITLE
GPU VREG CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D

REVISION 7.0.0

BRANCH prefsb

PAGE 135 OF 143

SHEET 110 OF 117

Caesar IV (Ethernet/SD)

CIV-specific Physical Rules

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
SD_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

Physical Net Type to Rule Map

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_COMP_PHY	*	ENET_50S
ENET_DIFF_PHY	*	ENET_100D
SD_PHY	*	SD_50S

CIV-specific Spacing Definitions
Ethernet

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_DIFF_ISO	*	=6:1_SPACING	?
ENET_DIFF2DIFF	*	=3:1_SPACING	?
ENET_TRANS_ISO	*	1.27 MM	?
COMP_ENET_ISO	*	=4:1_SPACING	?

SD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SD_ISO	*	=3:1_SPACING	?

Constraints
Ethernet

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
ENET_DIFF	*	*	ENET_DIFF_ISO	
ENET_DIFF	ENET_DIFF	*	ENET_DIFF2DIFF	
ENET_TRANS	*	*	ENET_TRANS_ISO	2 kV isolation
COMP_ENET	*	*	COMP_ENET_ISO	
ENET_TRANS	ENET_TRANS	*	ENET_DIFF2DIFF	

SD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SD	*	*	SD_ISO

VENI, VIDI, VICI!

Electrical Contraint Set		Physical	Spacing			
Ethernet						
147G	ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_P<3..0>		39 40
147G	ENET_MDI_NORM	ENET_DIFF_PHY	ENET_DIFF	ENETCONN_MDI_N<3..0>		39 40
147G		ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_P<3..0>		40
147G		ENET_DIFF_PHY	ENET_TRANS	ENETCONN_MDI_T_N<3..0>		40
150G			ENET_TRANS	ENETCONN_MCT3		40
150G			ENET_TRANS	ENETCONN_MCT2		40
150G			ENET_TRANS	ENETCONN_MCT1		40
150G			ENET_TRANS	ENETCONN_MCT0		40
147G		ENET_COMP_PHY	COMP_ENET	ENET_RDAC		39
SD						
147G	SD_DATA	SD_PHY	SD	ENET_CR_DATA<7..0>	NO_TEST=TRUE	39
148G		SD_PHY	SD	SDCONN_DATA<7..0>		39 41
149G		SD_PHY	SD	SDCONN_DATA_R<7..0>	NO_TEST=TRUE	41
148G	SD_CMD	SD_PHY	SD	ENET_SD_CMD	NO_TEST=TRUE	39
148G		SD_PHY	SD	SDCONN_CMD	NO_TEST=TRUE	39 41
150G		SD_PHY	SD	SDCONN_CMD_R	NO_TEST=TRUE	41
148G	SD_CLK	SD_PHY	SD	ENET_SD_CLK	NO_TEST=TRUE	39
148G		SD_PHY	SD	SDCONN_CLK	NO_TEST=TRUE	39 41
148G		SD_PHY	SD	SDCONN_CLK_R	NO_TEST=TRUE	41
148G		SD_PHY	SD	ENET_MEDIA_SENSE		15 18 39
148G		SD_PHY	SD	ENET_SD_DETECT_L		39 41
148G		SD_PHY	SD	SDCONN_WP		39 41
CIV SPI						
149G		SPI_50S	SPI	ENET_SCLK		39
149G		SPI_50S	SPI	ENET_MISO		39
149G		SPI_50S	SPI	ENET_MOSI		39
149G		SPI_50S	SPI	ENET_CS_L		39

SYNC MASTER=D8 FIYIN SYNC DATE=07/02/2012

PAGE TITLE
ETHERNET/SD CONSTRAINTS

Apple Inc.

DRAWING NUMBER 051-9504 SIZE D
REVISION 7.0.0
BRANCH prefsb
PAGE 136 OF 143
SHEET 111 OF 117

AUTO-CONSTRAINTS PG 1

4V5_*

	Physical	Spacing	Netname	
H1		PM	4V5_REG_EN	56
H2	POWER_PHY	POWER	4V5_REG_IN	56

ACDC_*

	Spacing	Netname	
H3	PM	ACDC_BURST_EN	48
H4	PM	ACDC_BURST_EN_L	48

ALL_*

	Spacing	Netname	
H5	PM	ALL_SYS_PWRGD	5 47 65

AP_*

	Spacing	Netname	
H6	GENERIC_ISO	AP_CLKREQ_L	15 21
H7	GENERIC_ISO	AP_CLKREQ_L_ISO	15 35
H8	GENERIC_ISO	AP_CLKREQ_Q_L	35
H9	GENERIC_ISO	AP_EVENT_L	35 47 48
H10	GENERIC_ISO	AP_PWR_EN_ISO	15 35
H11	PM	AP_RESET_CONN_L	35
H12	PM	AP_RESET_L	26 35
H13	PM	AP_WAKE_L	35

BLC12V_*

	Spacing	Netname
H14	PM	BLC12V_FAULT
H15	PM	BLC12V_FAULT_L
H16	PM	BLC12V_UVLO
H17	PM	BLC12V_UVLO_OUT
H18	PM	BLC12V_UVLO_REF

BLC_*

	Physical	Spacing	Voltage	Netname	
H19		GENERIC_ISO		BLC_BL	89 91
H20		GENERIC_ISO		BLC_BL_GATE	91
H21		GENERIC_ISO		BLC_BST	89 91
H22		GENERIC_ISO		BLC_BST_R	89
H23		GENERIC_ISO		BLC_BYPASS_GATE	91
H24		GENERIC_ISO		BLC_DIM_MCU	89
H25		PM		BLC_EN	87 89 90
H26		GENERIC_ISO		BLC_ENA	89
H27		GENERIC_ISO		BLC_ENA1	89 91
H28		PM		BLC_EN_DELAY	87
H29		PM		BLC_EN_R	89

BLC_*

	Physical	Spacing	Voltage	Netname	
H30		PM		BLC_EXT_BOOT	48 89
H31		PM		BLC_EXT_BOOT_L	89
H32	BLC_CTL_PHY	BLC_CTL	5V	BLC_MCU_AOUT_R	91
H33		GENERIC_ISO		BLC_MCU_BV	89 91
H34		GENERIC_ISO		BLC_MCU_BV_D	91
H35		GENERIC_ISO		BLC_MCU_BV_R	91
H36	SMB_PHY	SMB		BLC_MCU_B_SDA_CONN	89
H37		GENERIC_ISO		BLC_MCU_FLAG_V	89
H38		GENERIC_ISO		BLC_MCU_PWM5	89
H39		GENERIC_ISO		BLC_MCU_PWM5_R	89
H40		PM		BLC_MCU_RESET	89
H41		PM		BLC_MCU_RESET_L	89
H42		PM		BLC_MCU_RESET_R_L	89
H43	XDP_PHY	CLK_JTAG		BLC_MCU_RTCK	89
H44		GENERIC_ISO		BLC_MCU_RXD0	89
H45	XDP_PHY	XDP		BLC_MCU_TCK	89
H46	XDP_PHY	XDP		BLC_MCU_TDI	89
H47	XDP_PHY	XDP		BLC_MCU_TDO	89
H48	XDP_PHY	XDP		BLC_MCU_TMS	89
H49	XDP_PHY	XDP		BLC_MCU_TRST	89
H50	XDP_PHY	XDP		BLC_MCU_TXD0	89
H51		GENERIC_ISO		BLC_MCU_UVLO	89
H52		GENERIC_ISO		BLC_ON	91
H53		GENERIC_ISO		BLC_ON_DRAIN	91
H54		GENERIC_ISO		BLC_ON_R	91
H55		GENERIC_ISO		BLC_P_ON	89 90 91
H56		GENERIC_ISO		BLC_P_ON_BYPASS	91
H57		GENERIC_ISO		BLC_P_ON_D	91
H58		GENERIC_ISO		BLC_P_ON_DRAIN	91
H59		GENERIC_ISO		BLC_P_ON_D_R	91
H60		GENERIC_ISO		BLC_P_ON_GATE	91
H61		GENERIC_ISO		BLC_P_ON_R	91
H62		GENERIC_ISO		BLC_SKIP	90
H63		GENERIC_ISO		BLC_SNUB_1	90
H64		GENERIC_ISO		BLC_SNUB_2	90
H65		GENERIC_ISO		BLC_SNUB_3	90
H66		GENERIC_ISO		BLC_UVLO	89 91
H67		GENERIC_ISO		BLC_VIN2_GATE	91
H68		GENERIC_ISO		BLC_VIN2_SRC	91
H69		GENERIC_ISO		BLC_VINP_GATE	91
H70		GENERIC_ISO		BLC_VIN_SNS	90
H71		GENERIC_ISO		BLC_VSYNC	87 89
H72		GENERIC_ISO		BLC_VSYNC_R	89

BOOST_*

	Spacing	Netname	
H73	GENERIC_ISO	BOOST_BP	89
H74	GENERIC_ISO	BOOST_BYPASS	89 91
H75	GENERIC_ISO	BOOST_BYPASS_GATE	89
H76	PM	BOOST_EN_GATE	89
H77	PM	BOOST_EN_L	89
H78	GENERIC_ISO	BOOST_RC	89
H79	GENERIC_ISO	BOOST_SS	89

BT_*

	Spacing	Netname	
H80	PM	BT_PWR_EN	35
H81	PM	BT_PWR_RST_L	15 20 35
H82	PM	BT_PWR_RST_L_O	35

BURSTMODE_*

	Spacing	Netname	
H83	PM	BURSTMODE_EN	71
H84	PM	BURSTMODE_EN_L	6 48 71

CAM_*

	Spacing	Netname	
H85	PM	CAM_EXT_BOOT	42 43
H86	PM	CAM_PROC_RESET	43
H87	PM	CAM_PROC_RESET_L	42 43

CPU_*

	Physical	Spacing	Netname	
H88		PM	CPU_PWRGD_1V05_R	28
H89		PM	CPU_PWRGD_3V3	28
H90		PM	CPU_PWRGD_3V3_R	28
H91		GENERIC_ISO	CPU_SKTOCC	64
H92	CPU_PHY	CPU	CPU_THRMTRIP_3V3	47 48
H93	CPU_PHY	CPU	CPU_THRMTRIP_R_L	48

DEBUG_*

	Spacing	Netname	
H94	PM	DEBUG_RESET_L	26 49

DP_*

	Physical	Spacing	Netname	
H95		PM	DP_AUXIO_EN	15 86 88
H96		PM	DP_GPU_MUX_EN	84
H97		GENERIC_ISO	DP_INTPNL_HPD	84 87
H98		GENERIC_ISO	DP_INT_EG_HPD	82 84
H99	TBT_GEN_55S	TBT_GEN	DP_TBTPA_DDC_CLK	85 86
H100	TBT_GEN_55S	TBT_GEN	DP_TBTPA_DDC_DATA	85 86
H101		GENERIC_ISO	DP_TBTPA_HPD	36 86
H102	TBT_GEN_55S	TBT_GEN	DP_TBTPB_DDC_CLK	85 88
H103	TBT_GEN_55S	TBT_GEN	DP_TBTPB_DDC_DATA	85 88
H104		GENERIC_ISO	DP_TBTPB_HPD	36 88

AUTO-CONSTRAINTS GENERATED Fri 04/06/12 07:24:10 PM

PAGE TITLE: AUTO-CONSTRAINTS 1

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

PAGE: 138 OF 143

SHEET: 112 OF 117

AUTO-CONSTRAINTS PG 2

ENETCONN_*

	Spacing	Netname	
E1	GENERIC_ISO	ENETCONN_TCT	40

ENET_*

	Physical	Spacing	Netname	
E2		GENERIC_ISO	ENET_ACT	40
E3		GENERIC_ISO	ENET_ASF_GPIO	47 48
E4		GENERIC_ISO	ENET_CLKREQ_L	15 18 40
E5		PM	ENET_CLKREQ_L_Q	39 40
E6		PM	ENET_CR_1V8_EN	
E7		PM	ENET_CR_1V8_EN_R	
E8		PM	ENET_CR_3V3_EN_L	
E9		PM	ENET_CR_3V3_EN_L_R	
E10		PM	ENET_CR_PWREN	39 41
E11	XDP_PHY	XDP	ENET_LOW_PWR	26 39 41
E12		PM	ENET_PWR_EN_L	40
E13		PM	ENET_PWR_EN_L_R	40
E14		PM	ENET_RESET_L	39 41
E15		PM	ENET_SD_RESET_L	26 41
E16		GENERIC_ISO	ENET_SR_DISABLE	39
E17		GENERIC_ISO	ENET_SR_LX	39 40
E18		PM	ENET_WAKE_L	40

FAN_*

	Spacing	Netname	
E19	GENERIC_ISO	FAN_0_PWM_FET	54
E20	GENERIC_ISO	FAN_0_PWM_FILT	54
E21	GENERIC_ISO	FAN_0_TACH_FET	54
E22	GENERIC_ISO	FAN_0_TACH_FILT	54

FBVDD_*

	Spacing	Netname	
E23	GENERIC_ISO	FBVDD_ALTVO	82 95

FB_*

	Spacing	Netname	
E24	GENERIC_ISO	FB_A0_VREFC	79
E25	GENERIC_ISO	FB_A0_VREFD	79
E26	GENERIC_ISO	FB_A1_VREFC	79
E27	GENERIC_ISO	FB_A1_VREFD	79
E28	GENERIC_ISO	FB_B0_VREFC	80
E29	GENERIC_ISO	FB_B0_VREFD	80
E30	GENERIC_ISO	FB_B1_VREFC	80
E31	GENERIC_ISO	FB_B1_VREFD	80
E32	GENERIC_ISO	FB_VREF	77

FET_*

	Physical	Spacing	Voltage	Netname	
E33		GENERIC_ISO		FET_EN_P12V_S0	74
E34		GENERIC_ISO		FET_EN_P12V_S0_BLC	74
E35		GENERIC_ISO		FET_EN_P12V_S0_BLC_R	74
E36		GENERIC_ISO		FET_EN_P12V_S0_R	74
E37		GENERIC_ISO		FET_EN_P12V_S5	74
E38		GENERIC_ISO		FET_EN_P12V_S5_R	74
E39		GENERIC_ISO		FET_EN_VDDQ_S0	74
E40		GENERIC_ISO		FET_HDD_SLGSW	52
E41	POWER_PHY	POWER	12V	FET_VCC_U7950	74
E42	POWER_PHY	POWER	12V	FET_VCC_U7970	74
E43	POWER_PHY	POWER	12V	FET_VCC_U7980	74

FLAG_*

	Spacing	Netname	
E44	GENERIC_ISO	FLAG_V	89 90 91

G3_*

	Spacing	Netname	
E45	GENERIC_ISO	G3_POWERON_L	47 48

GND_*

	Spacing	Netname	
E46	SENSE	GND_SMC_AVSS	47 48 51 55

GPU_*

	Physical	Spacing	Netname	
E47		GENERIC_ISO	GPU_ALT_VREF	77 82
E48		GENERIC_ISO	GPU_BUFRSTN	83
E49		GENERIC_ISO	GPU_IFPAB_PLLVDD	81
E50		GENERIC_ISO	GPU_IFPA_IOVDD	81
E51		GENERIC_ISO	GPU_IFPB_IOVDD	81
E52		GENERIC_ISO	GPU_IFPC_IOVDD	81
E53	XDP_PHY	XDP	GPU_JTAG_TDI	78 81
E54	XDP_PHY	XDP	GPU_JTAG_TDO	78 81
E55	XDP_PHY	XDP	GPU_JTAG_TMS	78 81
E56	XDP_PHY	XDP	GPU_JTAG_TRST_L	81
E57		GENERIC_ISO	GPU_MLS_STRAP0	81 82
E58		GENERIC_ISO	GPU_MLS_STRAP1	81 82
E59		GENERIC_ISO	GPU_MLS_STRAP2	81 82
E60		GENERIC_ISO	GPU_MLS_STRAP3	81 82
E61		GENERIC_ISO	GPU_MLS_STRAP4	81 82
E62		GENERIC_ISO	GPU_RESET_L	26 75 82
E63	SPI_50S	SPI	GPU_ROM_CS_L	81 82
E64	SPI_50S	SPI	GPU_ROM_CS_L_R	82
E65	SPI_50S	SPI	GPU_ROM_SI	81 82
E66	SPI_50S	SPI	GPU_ROM_SI_R	82
E67	SPI_50S	SPI	GPU_ROM_SO	81 82
E68	SPI_50S	SPI	GPU_ROM_SO_R	82
E69	SPI_50S	SPI	GPU_ROM_WP_L	82

HDD_*

	Spacing	Netname	
E70	GENERIC_ISO	HDD_12V_S0_GATE	52
E71	GENERIC_ISO	HDD_OOB_1V00_REF	52
E72	PM	HDD_PWR_EN	21 52
E73	GENERIC_ISO	HDD_PWR_EN_L	52
E74	GENERIC_ISO	HDD_PWR_EN_R	52

I2C_*

	Physical	Spacing	Netname	
E75	SMB_PHY	SMB	I2C_TCON_MAS_SCL	50 87
E76	SMB_PHY	SMB	I2C_TCON_MAS_SDA	50 87

IFPD_*

	Spacing	Netname	
E77	GENERIC_ISO	IFPD_RSET	81

IFPEF_*

	Spacing	Netname	
E78	GENERIC_ISO	IFPEF_RSET	81

ISNSA_*

	Electrical	Physical	Spacing	Netname	
E79	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_N	51
E80	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VG3H_P	51
E81	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_N	55
E82	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_P1V05_P	55
E83	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_N	55
E84	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_CPU_VCCSA_P	55
E85	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_N	51
E86	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_FBVDDQ_P	51
E87	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_N	51
E88	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_HDD_P	51
E89	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_N	55
E90	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P12VS0_P1V05_P	55
E91	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_N	51
E92	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V05S0_PCH_P	51
E93	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_N	51
E94	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P1V5S0_CPU_MEM_P	51
E95	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_N	51
E96	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S0_SSD_P	51
E97	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_N	55
E98	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P3V3S4_AP_P	55
E99	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_N	51
E100	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_P5VS0_HDD_P	51
E101	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_N	51
E102	SNS_CURRENT	SNS_DIFF_PHY	SENSE	ISNSA_PVDDQS3_DDR_P	51

AUTO-CONSTRAINTS GENERATED Fri 04/06/12 07:24:10 PM

PAGE TITLE: AUTO-CONSTRAINTS 2

Apple Inc.

DRAWING NUMBER: 051-9504 SIZE: D

REVISION: 7.0.0

BRANCH: prefsb

PAGE: 139 OF 143

SHEET: 113 OF 117

AUTO-CONSTRAINTS PG 3

ISNS_*

	Physical	Spacing	Netname	
E1	SNS_PHY	SENSE	ISNS_CPUAXG_FB	51
E2	SNS_PHY	SENSE	ISNS_CPUAXG_N	51
E3	SNS_PHY	SENSE	ISNS_CPUAXG_P	51
E4	SNS_PHY	SENSE	ISNS_CPUCORE_FB	51
E5	SNS_PHY	SENSE	ISNS_CPUCORE_N	51
E6	SNS_PHY	SENSE	ISNS_CPUCORE_P	51
E7	SNS_PHY	SENSE	ISNS_GPUCORE_FB	51
E8	SNS_PHY	SENSE	ISNS_GPUCORE_N	51
E9	SNS_PHY	SENSE	ISNS_GPUCORE_P	51
E10	SNS_PHY	SENSE	ISNS_P12VG3H_R	51
E11	SNS_PHY	SENSE	ISNS_P12VS0_CPU_P1V05_R	55
E12	SNS_PHY	SENSE	ISNS_P12VS0_CPU_VCCSA_R	55
E13	SNS_PHY	SENSE	ISNS_P12VS0_FBVDDQ_R	51
E14	SNS_PHY	SENSE	ISNS_P12VS0_HDD_R	51
E15	SNS_PHY	SENSE	ISNS_P12VS0_P1V05_R	55
E16	SNS_PHY	SENSE	ISNS_P1V05S0_PCH_R	51
E17	SNS_PHY	SENSE	ISNS_P1V5S0_CPU_MEM_R	51
E18	SNS_PHY	SENSE	ISNS_P3V3S0_SSD_R	51
E19	SNS_PHY	SENSE	ISNS_P3V3S4_AP_R	55
E20	SNS_PHY	SENSE	ISNS_P5VS0_HDD_R	51
E21	SNS_PHY	SENSE	ISNS_PVDDQS3_DDR_R	51

ISOLATE_*

	Spacing	Netname	
E22	PM	ISOLATE_CPU_MEM_5V	28
E23	PM	ISOLATE_CPU_MEM_5V_L	28

JTAG_*

	Physical	Spacing	Netname	
E24	XDP_PHY	XDP	JTAG_GMUX_TMS	20
E25	XDP_PHY	XDP	JTAG_TBT_TDI	15 21
E26	XDP_PHY	XDP	JTAG_TBT_TDI_ISOL	15 36
E27	XDP_PHY	XDP	JTAG_TBT_TDO	15 21
E28	XDP_PHY	XDP	JTAG_TBT_TDO_ISOL	15 36
E29	XDP_PHY	XDP	JTAG_TBT_TMS	15 18
E30	XDP_PHY	XDP	JTAG_TBT_TMS_ISOL	15 36

LED_*

	Spacing	Netname	
E31	PM	LED_DRIVER_EN	90 91
E32	PM	LED_DRIVER_EN_L	91
E33	PM	LED_DRIVER_EN_L_R	91
E34	GENERIC_ISO	LED_DRIVER_OVP1	90 91
E35	GENERIC_ISO	LED_DRIVER_OVP1P	89 90
E36	GENERIC_ISO	LED_DRIVER_OVP1_OUT	90
E37	GENERIC_ISO	LED_DRIVER_OVP2	90 91
E38	GENERIC_ISO	LED_DRIVER_OVP2P	89 90
E39	GENERIC_ISO	LED_DRIVER_OVP2_OUT	90
E40	GENERIC_ISO	LED_DRIVER_OVP3	90 91
E41	GENERIC_ISO	LED_DRIVER_OVP3P	89 90
E42	GENERIC_ISO	LED_DRIVER_OVP3_OUT	90

LPCPLUS_*

	Spacing	Netname	
E43	GENERIC_ISO	LPCPLUS_GPIO	21 49

LPC_*

	Spacing	Netname	
E44	GENERIC_ISO	LPC_PWRDWN_L	19 26 47 49
E45	GENERIC_ISO	LPC_SERIRQ	18 47 49

MEMVTT_*

	Spacing	Netname	
E46	PM	MEMVTT_EN	28 64
E47	PM	MEMVTT_EN_L	28

MEM_*

	Spacing	Netname	
E48	GENERIC_ISO	MEM_EVENT_L	29 30 31 32 47 48

MOJO_*

	Physical	Spacing	Netname	
E49	XDP_PHY	XDP	MOJO_RX_L	45 47 48
E50	XDP_PHY	XDP	MOJO_TX_L	45 47 48

OCA_*

	Spacing	Netname	
E51	GENERIC_ISO	OCA_FET_DRAIN	91

OVP_*

	Spacing	Netname	
E52	GENERIC_ISO	OVP_OREF	91
E53	GENERIC_ISO	OVP_OUT1	91
E54	GENERIC_ISO	OVP_OUT1_R	91
E55	GENERIC_ISO	OVP_OUT2	91
E56	GENERIC_ISO	OVP_OUT2_R	91
E57	GENERIC_ISO	OVP_OUT3	91
E58	GENERIC_ISO	OVP_OUT3_R	91

P1V2_*

	Spacing	Netname	
E59	PM	P1V2_S4_EN	43

P1V8_*

	Spacing	Netname	
E60	PM	P1V8_S4_EN	43

P3V3AP_*

	Spacing	Netname	
E61	GENERIC_ISO	P3V3AP_VMON	35

P3V3_*

	Spacing	Netname	
E62	GENERIC_ISO	P3V3_S0_EN_G	74
E63	GENERIC_ISO	P3V3_S3_EN_G	74

P3V42G3H_*

	Spacing	Netname	
E64	GENERIC_ISO	P3V42G3H_BOOST	73

P5V_*

	Spacing	Netname	
E65	GENERIC_ISO	P5V_S0_EN_G	74

PCA9557D_*

	Spacing	Netname	
E66	GENERIC_ISO	PCA9557D_RESET_L	26 28 34

PCH_*

	Physical	Spacing	Netname	
E67		PM	PCH_BLC_EXT_BOOT	21 89
E68		PM	PCH_BLC_EXT_BOOT_R	15 21
E69		PM	PCH_BLC_MCU_RESET	21 89
E70		PM	PCH_BLC_MCU_RESET_R	15 21
E71		PM	PCH_CAM_RESET	15 21
E72		PM	PCH_CAM_RESET_R	21 43
E73		GENERIC_ISO	PCH_DSWVRMEN	19
E74	CPU_PHY	CPU	PCH_PECI	21
E75	CPU_PHY	CPU	PCH_PROCPWRGD	21
E76		GENERIC_ISO	PCH_RCIN_L	21
E77		GENERIC_ISO	PCH_RI_L	19
E78		GENERIC_ISO	PCH_SMBALERT_L	15 18
E79		GENERIC_ISO	PCH_SRTCRST_L	18
E80		GENERIC_ISO	PCH_STRP_TOPBLK_SWP_L	20
E81		GENERIC_ISO	PCH_SUSWARN_L	15 19

PCIE_*

	Spacing	Netname	
E82	GENERIC_ISO	PCIE_CLKREQ5_GPIO44_L	18
E83	PM	PCIE_WAKE_L	19 35 40

PEG_*

	Spacing	Netname	
E84	GENERIC_ISO	PEG_CLKREQ_L	15 18 75

PGOOD_*

	Spacing	Netname	
E85	PM	PGOOD_P1V5_S0_DLY	28

PLT_*

	Spacing	Netname	
E86	PCH	PLT_RESET_L	20 26
E87	PCH	PLT_RST_BUF_L	26

PM_*

	Spacing	Netname	
E88	PM	PM_CLKRUN_L	47 48 49
E89	PM	PM_DSW_PWRGD	47 48 65
E90	PM	PM_EN_FET_P12V_S0	64 74
E91	PM	PM_EN_FET_P12V_S0_R	74
E92	PM	PM_EN_FET_P3V3_S0	64 74
E93	PM	PM_EN_FET_P3V3_S4	64 74
E94	PM	PM_EN_FET_P5V_S0	64 74
E95	PM	PM_EN_FET_VDDQ_S0	64 74
E96	PM	PM_EN_LDO_DDRVTT_S0	64 72
E97	PM	PM_EN_REG_CPUCORE_S0	64 66

AUTO-CONSTRAINTS GENERATED Fri 04/06/12 07:24:10 PM

PAGE TITLE	AUTO-CONSTRAINTS 3
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
	PAGE 140 OF 143
	SHEET 114 OF 117

AUTO-CONSTRAINTS PG 4

PM_*

	Spacing	Netname	
B4	PM	PM_EN_REG_CPU_P1V05_S0	64 49
B5	PM	PM_EN_REG_FBVDDQ_S0	64 95
B6	PM	PM_EN_REG_GPUCORE_S0_R	92
B7	PM	PM_EN_REG_P1V05_S0	64 95
B8	PM	PM_EN_REG_P1V8_S0	64 72
B9	PM	PM_EN_REG_P3V3_S5	64 71 74
B10	PM	PM_EN_REG_P5V_S4	64 71
B11	PM	PM_EN_REG_VCCSA_S0	64 70
B12	PM	PM_EN_REG_VDDQ_S3	64 72
B13	PM	PM_EN_S0	64
B14	PM	PM_EN_S4	64
B15	PM	PM_EN_USB_PWR	45 46 64
B16	PM	PM_LED_A_ALL_SYS_PWRGD	5
B17	PM	PM_LED_A_BLC_GOOD	5
B18	PM	PM_LED_A_CPUAXG_PGOOD	5
B19	PM	PM_LED_A_GPU_GOOD	5
B20	PM	PM_LED_A_PGOOD_CPUCORE_S0	5
B21	PM	PM_LED_A_PGOOD_CPU_P1V05_S0	5
B22	PM	PM_LED_A_PGOOD_REG_FBVDDQ_S0	5
B23	PM	PM_LED_A_PGOOD_REG_GPUCORE_S0	5
B24	PM	PM_LED_A_PGOOD_REG_P1V05	5
B25	PM	PM_LED_A_PGOOD_REG_VDDQ_S3	5
B26	PM	PM_LED_A_S4	5
B27	PM	PM_LED_A_S5	5
B28	PM	PM_LED_A_SLP_S3	5
B29	PM	PM_LED_A_VIDEO_ON	5
B30	PM	PM_LED_K_ALL_SYS_PWRGD	5
B31	PM	PM_LED_K_BLC_GOOD	5
B32	PM	PM_LED_K_CPUAXG_PGOOD	5
B33	PM	PM_LED_K_GPU_GOOD	5
B34	PM	PM_LED_K_PGOOD_CPUCORE_S0	5
B35	PM	PM_LED_K_PGOOD_CPU_P1V05_S0	5
B36	PM	PM_LED_K_PGOOD_REG_FBVDDQ_S0	5
B37	PM	PM_LED_K_PGOOD_REG_GPUCORE_S0	5
B38	PM	PM_LED_K_PGOOD_REG_P1V05	5
B39	PM	PM_LED_K_PGOOD_REG_VDDQ_S3	5
B40	PM	PM_LED_K_SLP_S3	5
B41	PM	PM_MEM_PWRGD_L	28
B42	PM	PM_PCH_APWROK	19 65
B43	PM	PM_PCH_PWROK	15 19 26 35 43 65 89
B44	PM	PM_PCH_PWROK_APWROK	65
B45	PM	PM_PCH_SYS_PWROK	19 48 65
B46	PM	PM_PGOOD_FBVDDQ_VDDQ_S0	64
B47	PM	PM_PGOOD_FET_P12V_S0	74
B48	PM	PM_PGOOD_FET_P12V_S0_BLC	74 91
B49	PM	PM_PGOOD_FET_P12V_S5	74
B50	PM	PM_PGOOD_FET_P3V3_S0	64 74
B51	PM	PM_PGOOD_FET_P5V_S0	64 74
B52	PM	PM_PGOOD_FET_VDDQ_S0	28 64 74
B53	PM	PM_PGOOD_P3V3_S4_FET	27 35 64 74
B54	PM	PM_PGOOD_REG_ALL_P1V05_S0	64 65
B55	PM	PM_PGOOD_REG_ALL_P1V05_S0_R	28 64
B56	PM	PM_PGOOD_REG_CPUCORE_S0	5 25 65 66
B57	PM	PM_PGOOD_REG_CPU_P1V05_S0	5 64 69
B58	PM	PM_PGOOD_REG_FBVDDQ_S0	5 64 95
B59	PM	PM_PGOOD_REG_P1V05_S0	5 64 95
B60	PM	PM_PGOOD_REG_P1V8_S0	64 72
B61	PM	PM_PGOOD_REG_P3V3_S5	65 71
B62	PM	PM_PGOOD_REG_P5V_S4	64 71
B63	PM	PM_PGOOD_REG_VCCSA_S0	64 65 70
B64	PM	PM_PGOOD_REG_VDDQ_S3	5 64 72
B65	PM	PM_PWRBTN_L	15 19 25 47
B66	PM	PM_RSMRST_PCH_L	19 65
B67	PM	PM_RSMRST_PCH_L_R	65
B68	PM	PM_SLP_S3_L	5 15 19 28 40 47 48 64
B69	PM	PM_SLP_S4_L	15 19 47 64
B70	PM	PM_SLP_S5_L	15 19 47 64
B71	PCH	PM_SYSRST_L	19 25 26 47
B72	PCH	PM_THRMTRIP_L	21 48
B73	PM	PGOOD_P12V_S0_R	65
B74	PM	PGOOD_P12V_S0	64 65 74

PP12V_*

	Physical	Spacing	Voltage	Netname	
B70	POWER_PHY	POWER	12V	PP12V_LCD	87
B71	POWER_PHY	POWER	12V	PP12V_LCD_EXT	87
B72	POWER_PHY	POWER	12V	PP12V_S0_FAN_0_FILT	54
B73	POWER_PHY	POWER	12V	PP12V_S0_HDD_FET	44 52

PP1V05_*

	Physical	Spacing	Voltage	Netname	
B74	POWER_PHY	POWER	1.05V	PP1V05_GPU_FB_DLL_AVDD	77
B75	POWER_PHY	POWER	1.05V	PP1V05_GPU_FB_PLL_AVDD	77
B76	POWER_PHY	POWER	1.05V	PP1V05_GPU_IFPD_IOVDD	81
B77	POWER_PHY	POWER	1.05V	PP1V05_GPU_IFPEF_IOVDD	81
B78	POWER_PHY	POWER	1.05V	PP1V05_GPU_PLLVDD	81
B79	POWER_PHY	POWER	1.05V	PP1V05_GPU_SP_PLLVDD	81 83
B80	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLA_F	17 22
B81	POWER_PHY	POWER	1.05V	PP1V05_S0_PCH_VCCADPLLB_F	17 22

PP1V2_*

	Physical	Spacing	Voltage	Netname	
B82	POWER_PHY	POWER	1.2V	PP1V2_ENET_INTREG	40
B83	POWER_PHY	POWER	1.2V	PP1V2_G3H_SMC_VDDC	47
B84	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_AVDDL	39
B85	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_GPHYPLL	39
B86	POWER_PHY	POWER	1.2V	PP1V2_S4_ENET_PHY_PCIEPLL	39
B87	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_CRFILT	27
B88	POWER_PHY	POWER	1.2V	PP1V2_USB_HUB_PLLFILT	27

PP1V5_*

	Physical	Spacing	Voltage	Netname	
B89	POWER_PHY	POWER	1.5V	PP1V5_S0_DP_BIAS	84

PP1V8_*

	Physical	Spacing	Voltage	Netname	
B90	POWER_PHY	POWER	1.8V	PP1V8_S0_PCH_VCCVRM_F	22 24

PP3V3R1V8_*

	Physical	Spacing	Netname	
B92	POWER_PHY	POWER	PP3V3R1V8_ENET_LR_OUT_REG	39

PP3V3RHV_*

	Physical	Spacing	Voltage	Netname	
B93	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTAPWR	86
B94	POWER_PHY	POWER	12V	PP3V3RHV_SW_TBTBPWR	88

PP3V3_*

	Physical	Spacing	Voltage	Netname	
B95	POWER_PHY	POWER	3.3V	PP3V3_DMIC_CONN	42
B96	POWER_PHY	POWER	3.3V	PP3V3_G3H_AVREF_SMC	47 48
B97	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FET	35
B98	POWER_PHY	POWER	3.3V	PP3V3_G3H_BT_FLT	35
B99	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_USBMUX_R	45
B100	POWER_PHY	POWER	3.3V	PP3V3_G3H_SMC_VDDA	47
B101	POWER_PHY	POWER	3.3V	PP3V3_G3_RTC	6 26
B102	POWER_PHY	POWER	3.3V	PP3V3_GPU_IFPX_PLLVDD	81
B103	POWER_PHY	POWER	3.3V	PP3V3_PVDDQS3_ISNS	51
B104	POWER_PHY	POWER	3.3V	PP3V3_S0_PCH_VCCA_DAC_F	17 22
B105	POWER_PHY	POWER	3.3V	PP3V3_S0_SSD_FLT	44
B106	POWER_PHY	POWER	3.3V	PP3V3_S0_SW_SD_PWR	41
B107	POWER_PHY	POWER	3.3V	PP3V3_S4_ALS_F	42
B108	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FET	35
B109	POWER_PHY	POWER	3.3V	PP3V3_S4_AP_FLT	35
B110	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_AVDDH	39
B111	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_BIASVDDH	39
B112	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_SRVDD	39
B113	POWER_PHY	POWER	3.3V	PP3V3_S4_ENET_FET_XTALVDDH	39
B114	POWER_PHY	POWER	3.3V	PP3V3_S4_USB_HUB_VDD	27
B115	POWER_PHY	POWER	3.3V	PP3V3_S5_XDP_R	25

PP4V5_*

	Physical	Spacing	Voltage	Netname	
B116	POWER_PHY	POWER	4.5V	PP4V5_AUDIO_ANALOG	56 60 62

PP5V_*

	Physical	Spacing	Voltage	Netname	
B117	POWER_PHY	POWER	5V	PP5V_AUDIO_HPAMP	56 57
B118	POWER_PHY	POWER	5V	PP5V_S0_HDD_FET	44 52
B119	POWER_PHY	POWER	5V	PP5V_S0_PCH_V5REF	24
B120	POWER_PHY	POWER	5V	PP5V_S4_EXTA	45
B121	POWER_PHY	POWER	5V	PP5V_S4_EXTA_F	45
B122	POWER_PHY	POWER	5V	PP5V_S4_EXTB	45
B123	POWER_PHY	POWER	5V	PP5V_S4_EXTB_F	45
B124	POWER_PHY	POWER	5V	PP5V_S4_EXTC	46
B125	POWER_PHY	POWER	5V	PP5V_S4_EXTC_F	46
B126	POWER_PHY	POWER	5V	PP5V_S4_EXTD	46
B127	POWER_PHY	POWER	5V	PP5V_S4_EXTD_F	46
B128	POWER_PHY	POWER	5V	PP5V_S5_PCH_V5REFSUS	24

AUTO-CONSTRAINTS GENERATED Fri 04/06/12 07:24:10 PM

PAGE TITLE	AUTO-CONSTRAINTS 4
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
	PAGE 141 OF 143
	SHEET 115 OF 117

AUTO-CONSTRAINTS PG 5

PPHV_*

	Physical	Spacing	Voltage	Netname	
H6	POWER_PHY	POWER	12V	PPHV_SW_TBTAPWR	86
H7	POWER_PHY	POWER	12V	PPHV_SW_TBTBPWR	88

PPVBATT_*

	Physical	Spacing	Voltage	Netname	
H4	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC	26
H5	POWER_PHY	POWER	3.3V	PPVBATT_G3_RTC_R	26

PU_*

	Spacing	Netname	
H8	GENERIC_ISO	PU_U6900	44

PWR_*

	Spacing	Netname	
H6	PM	PWR_BTN	6 48
H7	PM	PWR_BTN_R	6

REG_*

	Physical	Spacing	Netname	
H8		PM	REG_CPUAXG_PGOOD	5 46
H9		PM	REG_CPUCORE_PGOOD	66
H10	CPU_PHY	CPU	REG_CPUCORE_VRHOT_L	66
H11		PM	REG_CPU_P1V05S0_PGOOD	69
H12	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET0	95
H13	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1	95
H14	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SET1_R	95
H15	VR_CTL_PHY	VR_CTL	REG_FBVDDQ_SREF	95
H16		PM	REG_P1V8S0_PGOOD	72
H17		PM	REG_P3V3S5_PGOOD	71
H18		PM	REG_P5VS4_PGOOD	71
H19		PM	REG_VCCSAS0_PGOOD	70
H20		PM	REG_VDDQS3_PGOOD	72

RTC_*

	Spacing	Netname	
H21	PM	RTC_RESET_L	18 26 48
H22	PM	RTC_RESET_L_R	48

S5_*

	Spacing	Netname	
F23	PM	S5_PWRGD	47 65

SATALED_*

	Spacing	Netname	
F24	GENERIC_ISO	SATALED_L	44

SDCONN_*

	Spacing	Netname	
F25	GENERIC_ISO	SDCONN_DETECT	41
F26	GENERIC_ISO	SDCONN_ILLIM	41
F27	GENERIC_ISO	SDCONN_OC_L	41

SD_*

	Spacing	Netname	
F28	GENERIC_ISO	SD_DETECT_LVL	41

SLG_*

	Spacing	Netname	
F29	PM	SLG_ENET_RESET_L	41
F30	PM	SLG_ENET_RESET_R_L	41

SMBUS_*

	Physical	Spacing	Netname	
F31	SMB_PHY	SMB	SMBUS_PCH_CLK	18 50
F32	SMB_PHY	SMB	SMBUS_PCH_CLK_R	50
F33	SMB_PHY	SMB	SMBUS_PCH_DATA	18 50
F34	SMB_PHY	SMB	SMBUS_PCH_DATA_R	50
F35	SMB_PHY	SMB	SMBUS_SMC_0_S0_SCL	47 50
F36	SMB_PHY	SMB	SMBUS_SMC_0_S0_SDA	47 50
F37	SMB_PHY	SMB	SMBUS_SMC_1_S0_SCL	47 50
F38	SMB_PHY	SMB	SMBUS_SMC_1_S0_SDA	47 50
F39	SMB_PHY	SMB	SMBUS_SMC_2_S4_SCL	47 50
F40	SMB_PHY	SMB	SMBUS_SMC_2_S4_SDA	47 50
F41	SMB_PHY	SMB	SMBUS_SMC_3_SCL	47 50
F42	SMB_PHY	SMB	SMBUS_SMC_3_SDA	47 50
F43	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SCL	47 48 50
F44	SMB_PHY	SMB	SMBUS_SMC_4_ASF_SDA	47 48 50
F45	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SCL	47 48 50
F46	SMB_PHY	SMB	SMBUS_SMC_5_G3H_SDA	47 48 50

SMCISNS_*

	Physical	Spacing	Netname	
H47	SNS_PHY	SENSE	SMCISNS_CPUAXG	48 51
H48	SNS_PHY	SENSE	SMCISNS_CPUCORE	48 51
H49	SNS_PHY	SENSE	SMCISNS_GPUCORE	48 51
H50	SNS_PHY	SENSE	SMCISNS_P12VG3H	48 51
H51	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_P1V05	48 55
H52	SNS_PHY	SENSE	SMCISNS_P12VS0_CPU_VCCSA	48 55
H53	SNS_PHY	SENSE	SMCISNS_P12VS0_FBVDDQ	48 51
H54	SNS_PHY	SENSE	SMCISNS_P12VS0_HDD	48 51
H55	SNS_PHY	SENSE	SMCISNS_P12VS0_P1V05	48 55
H56	SNS_PHY	SENSE	SMCISNS_P1V05S0_PCH	48 51
H57	SNS_PHY	SENSE	SMCISNS_P1V5S0_CPU_MEM	48 51
H58	SNS_PHY	SENSE	SMCISNS_P3V3S0_SSD	48 51
H59	SNS_PHY	SENSE	SMCISNS_P3V3S4_AP	48 55
H60	SNS_PHY	SENSE	SMCISNS_P5VS0_HDD	48 51
H61	SNS_PHY	SENSE	SMCISNS_PVDDQS3_DDR	48 51

SMCVSNS_*

	Physical	Spacing	Netname	
H62	SNS_PHY	SENSE	SMCVSNS_CPUAXG	48 51
H63	SNS_PHY	SENSE	SMCVSNS_CPUCORE	48 51
H64	SNS_PHY	SENSE	SMCVSNS_GPUCORE	48 51
H65	SNS_PHY	SENSE	SMCVSNS_P12VG3H	48 51
H66	SNS_PHY	SENSE	SMCVSNS_P1V05S0_PCH	48 51
H67	SNS_PHY	SENSE	SMCVSNS_P1V5S0_CPU_MEM	48 51
H68	SNS_PHY	SENSE	SMCVSNS_P3V3S0	48 51
H69	SNS_PHY	SENSE	SMCVSNS_P5VS0_HDD	48 51
H70	SNS_PHY	SENSE	SMCVSNS_PVDDQS3_DDR	48 51

SMC_*

	Physical	Spacing	Netname	
H71		GENERIC_ISO	SMC_ACDC_ID	6 48
H72		GENERIC_ISO	SMC_ACDC_ID_R	6
H73		PM	SMC_ASSERT_RTCRST	48
H74		GENERIC_ISO	SMC_BLC_MUX_RX_L	48 89
H75		GENERIC_ISO	SMC_BLC_MUX_TX_L	48 89
H76		GENERIC_ISO	SMC_CPU_CATERR_L	47 48
H77	CPU_PHY	CPU	SMC_CPU_PECI	48
H78		PM	SMC_DELAYED_PWRGD	38 47 48 65
H79		GENERIC_ISO	SMC_DP_HPD_L	47 48
H80	CLK_XTAL	XTAL	SMC_EXTAL	47 48
H81		GENERIC_ISO	SMC_FAN_0_CTL	47 54
H82		GENERIC_ISO	SMC_FAN_0_TACH	47 54
H83		GENERIC_ISO	SMC_GFX_OVERTEMP	47 48 82
H84		GENERIC_ISO	SMC_GFX_OVERTEMP_Q	82
H85		GENERIC_ISO	SMC_GFX_OVERTEMP_R_L	82
H86		PM	SMC_GFX_THROTTLE_L	47 82
H87		PM	SMC_GFX_THROTTLE_R_L	82
H88		PM	SMC_LRESET_L	26 47
H89		PM	SMC_MANUAL_RST_L	48
H90		PM	SMC_ONOFF_L	47 48
H91		SENSE	SMC_OOB1_RX_CN	44
H92		SENSE	SMC_OOB1_RX_FILT	44 52
H93		SENSE	SMC_OOB1_RX_L	47 52
H94		SENSE	SMC_OOB1_RX_R	52
H95		SENSE	SMC_OOB1_TX_L	47 48
H96		SENSE	SMC_OOB2_RX_L	44 48
H97		SENSE	SMC_OOB2_TX_L	44 48
H98	CPU_PHY	CPU	SMC_PECI_L	47 48
H99	CPU_PHY	CPU	SMC_PECI_L_R	48
H100		PM	SMC_PME_S4_WAKE_L	35 47 48
H101		GENERIC_ISO	SMC_PM_G2_EN	47 48 74
H102		PM	SMC_PM_PCH_SYS_PWROK	47 48
H103		CPU	SMC_PROCHOT	47 48
H104		PM	SMC_RESET_L	47 48 49

AUTO-CONSTRAINTS GENERATED Fri 04/06/12 07:24:10 PM

PAGE TITLE	AUTO-CONSTRAINTS 5
Apple Inc.	DRAWING NUMBER 051-9504 SIZE D
	REVISION 7.0.0
	BRANCH prefsb
	PAGE 142 OF 143
	SHEET 116 OF 117

AUTO-CONSTRAINTS PG 6

SMC_*

	Physical	Spacing	Netname	
B4		GENERIC_ISO	SMC_ROMBOOT	48 49
B5		GENERIC_ISO	SMC_RUNTIME_SCI_L	15 21 47
B6		GENERIC_ISO	SMC_RX_L	47 48 49
B7		PM	SMC_S4_WAKESRC_EN	35 47 48
B8		GENERIC_ISO	SMC_TCK	47 48 49
B9		GENERIC_ISO	SMC_TDI	47 48 49
B10		GENERIC_ISO	SMC_TDO	47 48 49
B11		PM	SMC_THRMTRIP	47 48
B12		GENERIC_ISO	SMC_TMS	47 48 49
B13		GENERIC_ISO	SMC_TO_BLC_RX_L	48
B14		GENERIC_ISO	SMC_TO_BLC_TX_L	48
B15		GENERIC_ISO	SMC_TX_L	47 48 49
B16		PM	SMC_WAKE_L	47
B17		GENERIC_ISO	SMC_WAKE_SCI_L	15 21 47
B18	CLK_XTAL	XTAL	SMC_XTAL	47 48
B19	CLK_XTAL	XTAL	SMC_XTAL_R	48

SML_*

	Physical	Spacing	Netname	
B17	SMB_PHY	SMB	SML_PCH_0_CLK	18 50
B18	SMB_PHY	SMB	SML_PCH_0_DATA	18 50
B19	SMB_PHY	SMB	SML_PCH_1_CLK	18 50
B20	SMB_PHY	SMB	SML_PCH_1_DATA	18 50

SPI_*

	Spacing	Netname	
B21	GENERIC_ISO	SPI_DESCRIPTOR_OVERRIDE_L	15 47

SSD_*

	Spacing	Netname	
B22	GENERIC_ISO	SSD_CLKREQ_L	15 18

SYS_*

	Spacing	Netname	
B23	PM	SYS_PWROK_R	65

TBT_*

	Physical	Spacing	Voltage	Netname	
B24		GENERIC_ISO	3.3V	TBT_A_BIAS	86
B25	TBT_GEN_55S	TBT_GEN		TBT_A_CONFIG1_RC	86
B26		PM		TBT_A_HV_EN	36 86
B27		GENERIC_ISO	3.3V	TBT_B_BIAS	88
B28	TBT_GEN_55S	TBT_GEN		TBT_B_CONFIG1_RC	88
B29		PM		TBT_B_HV_EN	36 88
B30		GENERIC_ISO		TBT_CLKREQ_ISOL_L	38
B31		GENERIC_ISO		TBT_CLKREQ_L	15 38
B32		GENERIC_ISO		TBT_DDC_XBAR_EN_L	36 85
B33		GENERIC_ISO		TBT_EN_CIO_PWR	38
B34		PM		TBT_EN_CIO_PWR_L	36 38
B35		GENERIC_ISO		TBT_EN_LC_ISOL	38
B36		GENERIC_ISO		TBT_EN_LC_PWR	36 38
B37		GENERIC_ISO		TBT_PCH_CLKREQ_L	15 21
B38		PM		TBT_PWR_EN	15 26 36
B39		PM		TBT_PWR_EN_PCH	18 26
B40		PM		TBT_PWR_ON_POC_RST_L	36 38
B41		PM		TBT_PWR_REQ_L	15 20 36
B42		PM		TBT_S0_EN	64
B43		PM		TBT_SW_RESET_L	21 38

TSNS_*

	Electrical	Physical	Spacing	Netname	
B44	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_N	53
B45	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_1_P	53
B46	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_N	53
B47	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_2_P	53
B48	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_N	53
B49	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_1_3_P	53
B50	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_N	53
B51	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_1_P	53
B52	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_N	53
B53	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_2_P	53
B54	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_N	53
B55	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_3_P	53
B56	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_N	53
B57	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_4_P	53
B58	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_N	53
B59	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_5_P	53
B60	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_N	53
B61	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_6_P	53
B62	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_N	53
B63	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_2_7_P	53
B64	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_N	4 53
B65	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_ACDC_P	4 53
B66	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_N	53
B67	SNS_TEMP	SNS_DIFF_PHY	SENSE	TSNS_SKIN_P	53

UVP_*

	Spacing	Netname	
B68	PM	UVP_IN_1	91
B69	PM	UVP_IN_1_REF	91
B70	PM	UVP_IN_2	91
B71	PM	UVP_IN_3	91
B72	PM	UVP_IN_4	91
B73	PM	UVP_REF	91

VREFMRGN_*

	Spacing	Netname	
B74	GENERIC_ISO	VREFMRGN_CA_SODIMMA_EN	34
B75	GENERIC_ISO	VREFMRGN_CA_SODIMMB_EN	34

VTTCLAMP_*

	Spacing	Netname	
B76	GENERIC_ISO	VTTCLAMP_EN	28
B77	GENERIC_ISO	VTTCLAMP_L	28

WOL_*

	Spacing	Netname	
B78	GENERIC_ISO	WOL_EN	15 21 40

AUTO-CONSTRAINTS GENERATED Fri 04/06/12 07:24:10 PM

PAGE TITLE: AUTO-CONSTRAINTS 6

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PAGE: 143 OF 143

SHEET: 117 OF 117