1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB,M59

09/19/2006

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
A		463525	PRODUCTION RELEASE	9/19/2006	9/19/2006

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7150	1	SCHEM,MLB,M59	SCH	CRITICAL	
820-2054	1	PCBF,MLB,M59	PCB	CRITICAL	

DRAWING
TITLE=M59_MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Sep 25 10:45:58 2006

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

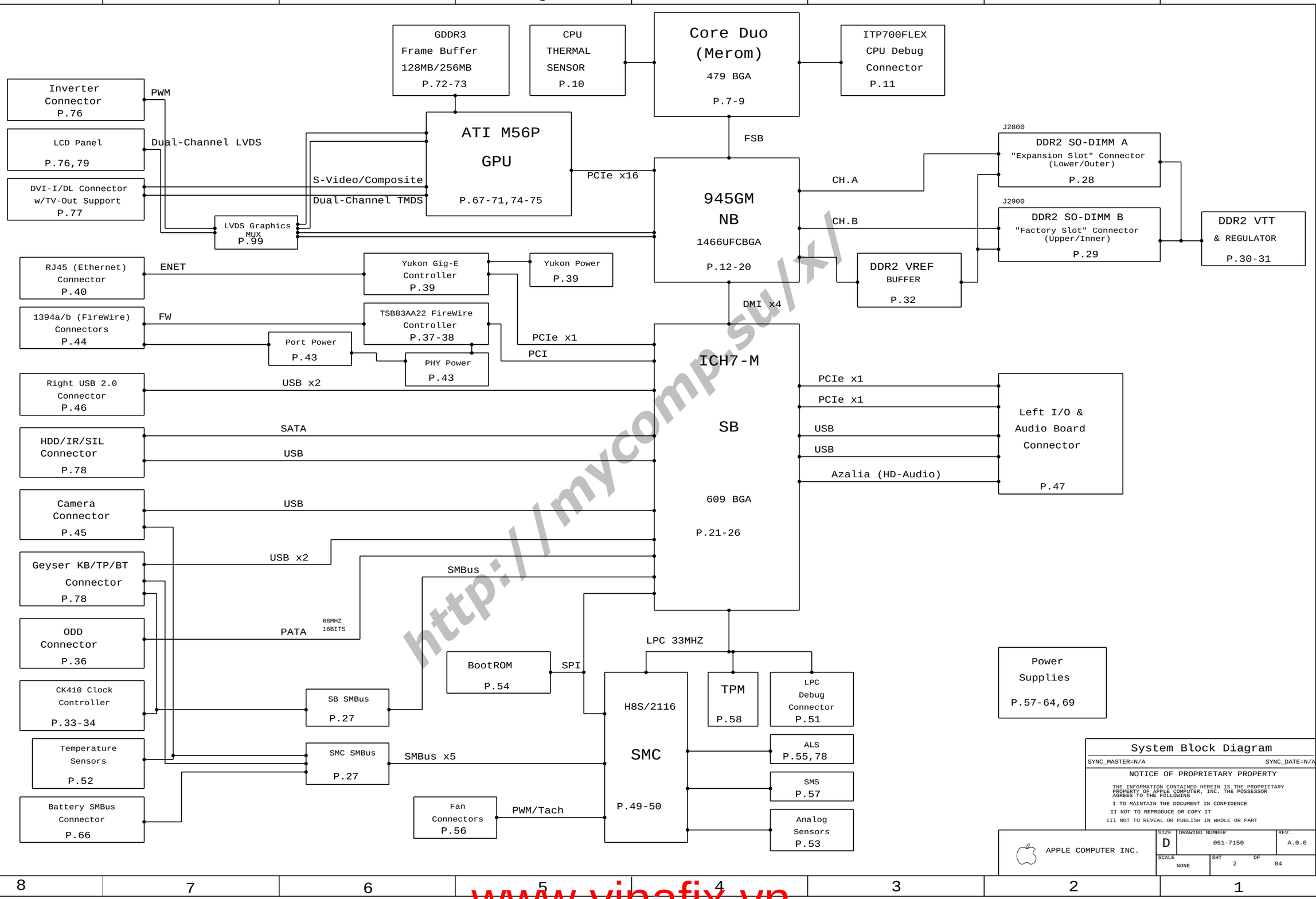
MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

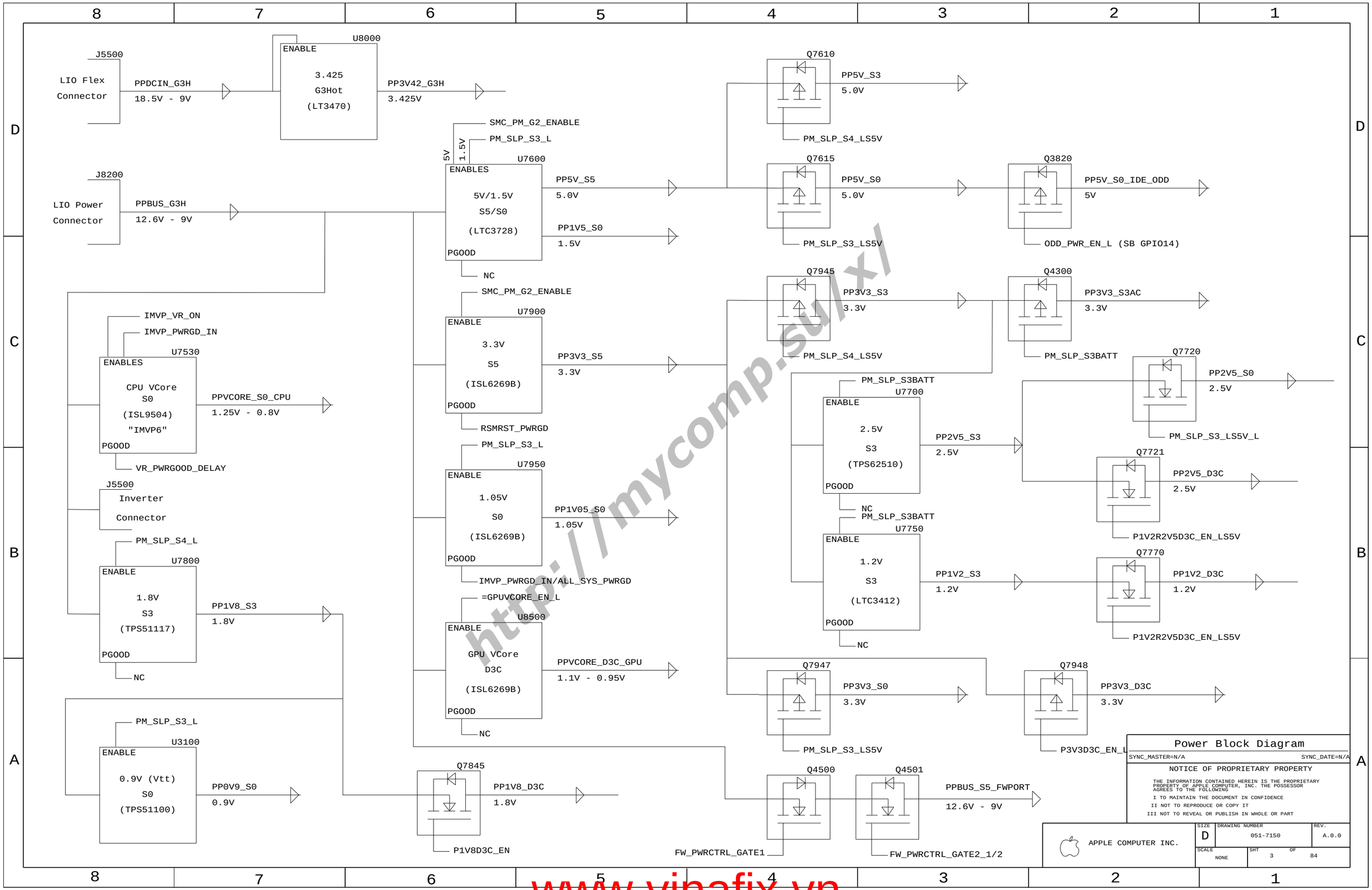
Apple Computer Inc.

TITLE
SCHEM,MLB,M59

DRAWING NUMBER 051-7150 | REV. A.0.0

SHT 1 OF 84





2.16Ghz BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7849	PCBA,2.16GHZ,128VRAM,M59,MBP15	EEE_WTE,M59_COMMON,CPU_2_16GHZ,VRAM_SAM128

2.33Ghz BOMs

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7851	PCBA,2.33GHZ,256VRAM,M59,MBP15	EEE_WTG,M59_COMMON,CPU_2_33GHZ,VRAM_SAM256

Bar Code Label / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WTE]	CRITICAL	EEE_WTE
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:WTG]	CRITICAL	EEE_WTG

BOMOPTION Groups

BOM GROUP	BOM OPTIONS
M59_COMMON	ALTERNATE,COMMON,M59_COMMON1,M59_COMMON2,M59_COMMON3
M59_COMMON1	BOOTROM_FINAL,ENET_LOWPWR_EN,ENETPWR_S3AC,GPU_BB_CTL,D3CPGOOD_3V3
M59_COMMON2	ITP,KBDLED_HAS,LPCPLUS,LVDS_PD,MEMVREF_S3
M59_COMMON3	MEMVTT_EN_PU,RTUSB_ESD,SMC_PRGRM,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
VRAM_INF128	GPU_MEM_NOT_SAM,VRAM_128_INFINEON
VRAM_SAM128	VRAM_128_SAMSUNG
VRAM_INF256	GPU_MEM_256M,GPU_MEM_NOT_SAM,VRAM_256_INFINEON
VRAM_SAM256	GPU_MEM_256M,VRAM_256_SAMSUNG
M59_TPM	TPM

extra TPM options:
SMC_TPM_GPIO2
SMC_TPM_GPIO1
SMC_TPM_PP

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_SAMSUNG
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_SAMSUNG
333S0358	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_HYNIX
333S0351	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_HYNIX
333S0376	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128_INFINEON
333S0377	4	IC,SGRAM,GDDR3,16MX32,600MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256_INFINEON
337S3391	1	IC,MDC,B2,PRQ,2.16G,34W,667M,4M,479BGA	U0700	CRITICAL	CPU_2_16GHZ
337S3393	1	IC,MDC,B2,PRQ,2.33G,34W,667M,4M,479BGA	U0700	CRITICAL	CPU_2_33GHZ
341S1922	1	IC,EFI,BOOTROM DEVELOPMENT (UNLOCKED),M59	U6301	CRITICAL	BOOTROM_DEVEL
341S1923	1	IC,EFI,BOOTROM FINAL (LOCKED),M59	U6301	CRITICAL	BOOTROM_FINAL
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	SMC_BLANK
341S1929	1	IC,PRGRM,SMC (NEW),M59	U5800	CRITICAL	SMC_PRGRM
338S0269	1	IC,945GM,NORTHBRIDGE	U1200	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	
338S0368	1	IC,ATI,M56L-LLP,GRPHXCRTL,LF 880BGA	U8400	CRITICAL	
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	TPM
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	
343S0385	1	IC,ICH7M,BGA	U2100	CRITICAL	
353S1461	1	IC,ISL9504,SYNC REG CTRL,QFN48	U7530	CRITICAL	
359S0109	1	LOW POWER CLOCK SYNTHESIZER, 68PIN	U3301	CRITICAL	

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0094	128S0060		ALL	330uF,2V,9MOHM,D2
128S0095	128S0060		ALL	330uF,2V,6MOHM,D2
128S0081	128S0061		ALL	150uF,6.3V,25MOHM,C2
376S0448	376S0445		ALL	Si7806ADN for FDM6296
353S1465	353S1461		ALL	Screened ISL6262 for ISL9504
152S0287	152S0435		ALL	Alternates for Coilcraft MSS1132
128S0093	128S0092		ALL	33uF,16V,D2

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	4	84

Functional Test Points

Power Supply NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		IMVP6_RBIAS	59C7
TRUE		IMVP6_COMP	59B7
TRUE		P5VS5_RUNSS	60C5 64A6
TRUE		P1V5S0_RUNSS	5B7 60C4 64C6
TRUE		P1V2S3_RT	61B6
TRUE		P1V2S3_RUNSS	41C4 61B7
TRUE		P3V3S5_COMP	5B7 63C6
TRUE		P3V3S5_FSET	5B7 63D6
TRUE		P1V05S0_COMP	5C7 63A7
TRUE		P1V05S0_FSET	5B7 63B7
TRUE		P3V42G3H_FB	64C3
TRUE		GPUVCORE_COMP	68C7
TRUE		GPUVCORE_FSET	68C7
TRUE		GPUBBP_ADJ	68B7
TRUE		GPUBBN_FB	68A3
TRUE		GPUVCORE_FB	68C7
TRUE		GPUVCORE_FB_RC	68C3
TRUE		GPUVCORE_ISEN	68C5
TRUE		GPUVCORE_LG	68C5
TRUE		GPUVCORE_PHASE	68C5
TRUE		GPUVCORE_UG	68D5
TRUE		IMVP6_COMP_RC	59B8
TRUE		IMVP6_DFB	59B6
TRUE		IMVP6_FB	59B7
TRUE		IMVP6_OCSET	59C6
TRUE		IMVP6_VDIFF	59C7
TRUE		IMVP6_VDIFF_RC	59B8
TRUE		P1V05S0_BOOT	63B5
TRUE		P1V05S0_BOOT_R	63B5
TRUE		P1V05S0_COMP	5D7 63A7
TRUE		P1V05S0_COMP_R	63A7
TRUE		P1V05S0_FB	63A7
TRUE		P1V05S0_FB_RC	63A3
TRUE		P1V05S0_FSET	5D7 63B7
TRUE		P1V05S0_ISEN	63A5
TRUE		P1V05S0_LG	63A5
TRUE		P1V05S0_PHASE	63B5
TRUE		P1V05S0_UG	63B5
TRUE		P1V5S0_RUNSS	5D7 60C4 64C6
TRUE		P3V3S5_BOOT	63D4
TRUE		P3V3S5_BOOT_R	63D4
TRUE		P3V3S5_COMP	5D7 63C6
TRUE		P3V3S5_COMP_R	63C6
TRUE		P3V3S5_FB	63C6
TRUE		P3V3S5_FB_RC	63C2
TRUE		P3V3S5_FSET	5D7 63D6
TRUE		P3V3S5_ISEN	63C4
TRUE		P3V3S5_LG	63C4
TRUE		P3V3S5_UG	63D4
TRUE		CK410_XTAL_IN	33C6

CPU FSB NO_TESTs

NO_TEST	EXPOSED_VIA		
TRUE		FSB_A_L<31..3>	7C8 7D8 12C4 12D4 84D6
TRUE		FSB_ADS_L	7D6 12C4 84D6
TRUE	TRUE	FSB_ADSTB_L<1..0>	7C8 7D8 12C4 84C6
TRUE		FSB_BNR_L	7D6 12C4 84D6
TRUE		FSB_BREQ0_L	7D6 12C4 84D6
TRUE		FSB_D_L<63..0>	7B3 7B4 7C3 7C4 12B6 12C6 12D6 84D6
TRUE		FSB_DBSY_L	7D6 12B4 84D6
TRUE	TRUE	FSB_DINV_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE		FSB_DRDY_L	7D6 12B4 84D6
TRUE	TRUE	FSB_DSTBN_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE	TRUE	FSB_DSTBP_L<3..0>	7B3 7B4 7C3 7C4 12B4 84D6
TRUE		FSB_HIT_L	7D6 12B4 84D6
TRUE		FSB_HITM_L	7D6 12B4 84D6
TRUE		FSB_LOCK_L	7D6 12B4 84D6
TRUE		FSB_REQ_L<4..0>	7D8 12A4 12B4 84D6

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	56C7 65A1
TRUE	FAN_LT_PWM	56B6
TRUE	FAN_LT_TACH	56B6
TRUE	FAN_RT_PWM	56B3
TRUE	FAN_RT_TACH	56B3

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	51C4 65D3
TRUE	=PP5V_S0_LPCPLUS	51C4 65A1
TRUE	LPC_AD<0>	21D4 49D7 51C4 58C6
TRUE	LPC_AD<1>	21D4 49D7 51C4 58C6
TRUE	LPC_FRAME_L	21C5 49C7 51C4 58C6
TRUE	PM_CLKRUN_L	23C8 49C5 51C4 58C6
TRUE	BOOT_LPC_SPI_L	22B3 49C7 51B4
TRUE	SMC_TMS	49B5 50B2 51B4
TRUE	DEBUG_RST_L	26B1 51B4
TRUE	SMC_TRST_L	49C1 51B4
TRUE	SMC_TDO	49B5 50B2 51B4
TRUE	SMC_MD1	49C1 51B4
TRUE	SMC_TX_L	46B5 49C7 50B2 50B3 51B4
TRUE	FWH_INIT_L	21C4 50D3 51C5
TRUE	PCI_CLK_PORT80_LPC	34D6 51C5
TRUE	LPC_AD<2>	21D4 49C7 51C5 58C6
TRUE	LPC_AD<3>	21D4 49C7 51C5 58C6
TRUE	INT_SERIRQ	23C8 49C7 51C5 58C6
TRUE	PM_SUS_STAT_L	23C5 49C5 50A2 51B5 58C6
TRUE	SMC_TDI	49B5 50B2 51B5
TRUE	SMC_TCK	49C5 50B2 51B5
TRUE	SMC_RST_L	49C3 50D6 51B5
TRUE	SMC_NMI	49C1 51B5
TRUE	SMC_RX_L	46B5 49C7 50B2 50B3 51B5
TRUE	SV_SET_UP	23B6 23C3 51B5

Left ALS Connector

FUNC_TEST

TRUE	=PP3V3_S3_LTALS	65C3 78C5
TRUE	ALS_GAIN	6D5 49B5 78C6
TRUE	LTALS_OUT	55C7 78C6
TRUE	GND	

Thermal Diode Connectors

FUNC_TEST

TRUE	HSTHMSNS_DX_P	52C5
TRUE	HSTHMSNS_DX_N	52C5
TRUE	RSFSTHMSNS_D_P	52D5
TRUE	RSFSTHMSNS_D_N	52C5

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	53A4 63A2 65D8
TRUE	PM_SYSRST_L	23C5 26C5 49B7
TRUE	SMC_ONOFF_L	49C5 50B2 50C6 78C2

Current Sense Calibration

FUNC_TEST

TRUE	ISENSE_CAL_EN	49B7 53A8
TRUE	=PP5V_S0_ISENSECAL	53A8 65A1
TRUE	=PP1V8_S3_REG	62C1 65B8
TRUE	=PP1V5_S0_REG	60C1 65C8
TRUE	PPVCORE_S0_GPU	
TRUE	PPVCORE_S0_CPU	65D1
TRUE	GND	

2 TPs per

8 TPs, 2 with each of above TP pairs

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	49C5 50B2 66B5
TRUE	=SMBUS_BATT_SCL	27C1 66B5
TRUE	=SMBUS_BATT_SDA	27C1 66B5
TRUE	GND_BATT	66B5

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	47D6 65C6
TRUE	=PPDCIN_G3H_LIO	47C6 65A8
TRUE	=PP5V_S5_LIO	47C6 65B1
TRUE	=PP3V42_G3H_LIO	47D6 65D3
TRUE	PP5V_S0_AUDIO_PWR	47D4
TRUE	PP5V_S0_AUDIO	47C4
TRUE	GND_AUDIO_PWR	47A4
TRUE	GND_AUDIO	47A4
TRUE	ACZ_SDATAIN<0>	21C7 47B6 84B4
TRUE	ACZ_SDATAOUT	21C7 47B6 84B4
TRUE	ACZ_BITCLK	21C7 47B6 84B4
TRUE	ACZ_RST_L	21C7 47B3 84B4
TRUE	EXCARD_OC_L	6C3 47C6 50B3
TRUE	LTUSB_OC_L	6D3 47C6
TRUE	LIO_BATT_ISENSE	47C6 53C3
TRUE	SMC_SYS_ISET	47C6 49B5
TRUE	SMC_BATT_ISET	47B6 49B5
TRUE	SMC_BATT_CHG_EN	47C6 49D7 50A2
TRUE	SMC_BC_ACOK	47B6 49C5 50A2
TRUE	SMC_ADAPTER_EN	43B7 47C6 49D5 50A2
TRUE	LIO_P3V3S0_EN_L	47B6 64C6
TRUE	LIO_DCIN_ISENSE	47B6 53C5
TRUE	LIO_P3V3S3_EN	47B6 64A6
TRUE	SMC_BATT_TRICKLE_EN_L	47B6 49D7 50A2
TRUE	SYS_ONEWIRE	47C6 49B7 50B2
TRUE	MINI_CLKREQ_L	34A3 47C6
TRUE	SMC_EXCARD_CP	47B6 49B7 50A2
TRUE	EXCARD_CLKREQ_L	34A3 47C6
TRUE	SMC_EXCARD_PWR_EN	47B6 49B7
TRUE	LIO_PLT_RESET_L	26C1 47C6
TRUE	ACZ_SYNC	21C7 47B6 84B4
TRUE	=USB2_LT_N	6D3 47C3
TRUE	=USB2_LT_P	6D3 47C3
TRUE	=USB2_EXCARD_N	6C3 47C3
TRUE	=USB2_EXCARD_P	6C3 47C3
TRUE	=PCIE_EXCARD_R2D_N	47B3 48C6
TRUE	=PCIE_EXCARD_R2D_P	47B3 48C6
TRUE	=PCIE_EXCARD_D2R_N	47B3 48B6
TRUE	=PCIE_EXCARD_D2R_P	47B3 48C6
TRUE	PCIE_CLK100M_EXCARD_P	34C3 47B3
TRUE	PCIE_CLK100M_EXCARD_N	34B3 47B3
TRUE	=PCIE_MINI_R2D_N	47B3 48C6
TRUE	=PCIE_MINI_R2D_P	47B3 48C6
TRUE	=PCIE_MINI_D2R_N	47C3 48C6
TRUE	=PCIE_MINI_D2R_P	47C3 48C6
TRUE	PCIE_CLK100M_MINI_P	34D4 47C3
TRUE	PCIE_CLK100M_MINI_N	34D4 47C3
TRUE	=SMBUS_LIO_SMC_SCL	27D1 47C3
TRUE	=SMBUS_LIO_SMC_SDA	27D1 47C3
TRUE	=SMBUS_LIO_SB_SCL	27B6 47C3
TRUE	=SMBUS_LIO_SB_SDA	27B6 47C3
TRUE	PCIE_WAKE_L	23C8 39C6 47C3

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	65C3 66C4
TRUE	GND	

Request for at least 10 GND test points

NOTE: 10 additional GND test points are called out separately in these notes.

EXPOSED_VIA property indicates that the net should have a via with 10-mil soldermask opening for use as engineering probe point.

Misc EXPOSED_VIA Nets

EXPOSED_VIA		
TRUE	DMI_N2S_P<1..0>	14B4 22D2
TRUE	DMI_N2S_N<1..0>	14B4 22D2
TRUE	SB_CLK100M_SATA_P	21B6 34C3
TRUE	SB_CLK100M_SATA_N	21B6 34C3

Camera Connector

FUNC_TEST

TRUE	=PP5V_S3_CAMERA	45C3 65B1
	=USB2_CAMERA_N	6C3 45C3
	=USB2_CAMERA_P	6D3 45B3

Inverter Connector

FUNC_TEST

TRUE	GND_CHASSIS_INVERTER	6A8
TRUE	PPBUS_S0_INVERTER	76B5
TRUE	GND_INVERTER	76A5
TRUE	INVERTER_PWM	76A5
TRUE	PP5V_INVERTER_SW	76B5

RTC Battery Connector

FUNC_TEST

TRUE	PPVBATT_G3C_RTC	26D6
TRUE	GND	

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 5 OF 84	

NC_CPU_A32_L — TP_CPU_A32_L (7C8)
NC_CPU_A33_L — TP_CPU_A33_L (7B8)
NC_CPU_A34_L — TP_CPU_A34_L (7B8)
NC_CPU_A35_L — TP_CPU_A35_L (7B8)
NC_CPU_A36_L — TP_CPU_A36_L (7B8)
NC_CPU_A37_L — TP_CPU_A37_L (7B8)
NC_CPU_A38_L — TP_CPU_A38_L (7B8)
NC_CPU_A39_L — TP_CPU_A39_L (7B8)
NC_CPU_APM0_L — TP_CPU_APM0_L (7B8)
NC_CPU_APM1_L — TP_CPU_APM1_L (7B8)
NC_CPU_EXTBREF — TP_CPU_EXTBREF (7B6)
NC_CPU_HFPLL — TP_CPU_HFPLL (7B8)
NC_CPU_SPARE0 — TP_CPU_SPARE0 (7B6)
NC_CPU_SPARE1 — TP_CPU_SPARE1 (7B6)
NC_CPU_SPARE2 — TP_CPU_SPARE2 (7B6)
NC_CPU_SPARE4 — TP_CPU_SPARE4 (7B6)

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28C3)
NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29C3)
TP_NB_CFG<4..3> — NB_CFG<4..3> (14C6)
TP_NB_CFG<6> — NB_CFG<6> (14C6)
TP_NB_CFG<8> — NB_CFG<8> (14C6)
TP_NB_CFG<11..10> — NB_CFG<11..10> (14C6)
TP_NB_CFG<15..14> — NB_CFG<15..14> (14C6)
TP_NB_CFG<17> — NB_CFG<17> (14C6)

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14C6)

TP_SB_SUS_CLK — SUS_CLK_SB (23C3)

NC_SB_XOR_T5 — TP_SB_XOR_T5 (21C6)
NC_SB_XOR_U5 — TP_SB_XOR_U5 (21C6)
NC_SB_XOR_V3 — TP_SB_XOR_V3 (21C6)
NC_SB_XOR_V4 — TP_SB_XOR_V4 (21C6)
NC_SB_XOR_W3 — TP_SB_XOR_W3 (21C6)

FireWire Aliases

=PP3V3_FWPHY_REG (42C4) — PP3V3_FWPHY (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE)
  =PP3V3_FWPHY (38D7 44B8)
  =PP3V3_FWPHY_CORE (42C4)
  =PP3V3_FWLATEVG (44A8)
  =PP3V3_FWLATEVG_ACTIVE (43A7)

=PP1V95_FWPHY_CORE_LDO (42C1) — PP1V95_FWPHY (VOLTAGE=1.95V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm, MAKE_BASE=TRUE)
  =PP1V95_FWPHY (38D5)
  =PP1V8_FWPHY_OSC (38B2)

SMC_RSTGATE_L (49D7 6D4) — MAKE_BASE=TRUE
  =SMC_FWRSTGATE_L (37A8)

PCI_AD<19> (37C6 22A7) — MAKE_BASE=TRUE
  =FW_PCI_IDSEL (37B7)

PCI_GNT3_L (22B6) — MAKE_BASE=TRUE
  =FW_PCI_GNT_L (37D3)

PCI_REQ3_L (26D2 22B6) — MAKE_BASE=TRUE
  =FW_PCI_REQ_L (37D3)

Chassis GNDs

GND_CHASSIS_RTUSB (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
  =GND_CHASSIS_RTUSB (46B2)
  =GND_CHASSIS_FW_PORT2L (44A1)
  =GND_CHASSIS_FW_EMI_R (44A3)

GND_CHASSIS_DVI_TOP (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
  C0600 0.01UF 10% 50V X7R 402
  =GND_CHASSIS_DVI2 (77A5)
  =GND_CHASSIS_DVI4 (77A3)

GND_CHASSIS_DVI_BOT (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
  R0601 0 5% 1/16W MF-LF 402
  =GND_CHASSIS_DVI1 (77B5)
  =GND_CHASSIS_DVI3 (77A2)
  =GND_CHASSIS_DVI5 (77A2)

GND_CHASSIS_ENET (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
  =GND_CHASSIS_ENET (40B2)
  =GND_CHASSIS_FW_PORT1 (44C1)
  =GND_CHASSIS_FW_PORT2U (44A1)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602 HOLE-VIA-P5RP25
C0602 0.01UF 10% 50V X7R 402

GND_CHASSIS_LVDS (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
  =GND_CHASSIS_LCD1 (76D2)
  =GND_CHASSIS_LCD2 (76D3)
  =GND_CHASSIS_LCD3 (76C3)
  =GND_CHASSIS_LCD4 (76B2)

SH0600 OG-503040 SHLD-SM-LF

GND_CHASSIS_INVERTER (5A4) (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE)
  =GND_CHASSIS_INVERTER (76A6)
  =GND_CHASSIS_CAMERA (45B5 45C5)

TP_SMC_RSTGATE_L (MAKE_BASE=TRUE) — SMC_RSTGATE_L (6B7 49D7)
ALS_GAIN (78C6 49B5 5B2) (MAKE_BASE=TRUE) — =RTALS_GAIN (55C4)

NC_ENET_CTRL12 (MAKE_BASE=TRUE, NO_TEST=TRUE) — ENET_CTRL12 (39C8)
NC_ENET_CTRL25 (MAKE_BASE=TRUE, NO_TEST=TRUE) — ENET_CTRL25 (39C8)

Ethernet Power Management Support

ENET_LOWPWR_EN
R0600 0 5% 1/16W MF-LF 402
22D8 22C4 SB_GPIO30 (IN) — ENET_LOWPWR_EN (39B8) (OUT)

NOTE: BOM options "USB_G_OC_PU" and "ENET_LOWPWR_EN" are mutually-exclusive.

Inverter PWM Reset Alias

26C1 MS9_INVERTER_PLT_RST_L — =INVERTER_PWM_PLT_RST_L (76A8)

Thermal Module Holes

Add 2 blind vias per hole per side to GND

Top CPU TM Hole
Top GPU Right TM Hole
Left CPU TM Hole
Right CPU TM Hole
Bottom Left GPU TM Hole

RAM door (Torx) holes

ZT0630 HOLE-VIA-P5RP25 — GND_CHASSIS_RAMDOOR_HOLE_0 (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
C0630 0.01UF 10% 50V X7R 402

ZT0631 HOLE-VIA-P5RP25 — GND_CHASSIS_RAMDOOR_HOLE_1 (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
C0631 0.01UF 10% 50V X7R 402

Frame holes

ZT0615 HOLE-VIA-P5RP25 — GND_CHASSIS_RIGHT_FAN_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0614 HOLE-VIA-P5RP25 — GND_CHASSIS_RIGHT_FAN_NOTCH (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0613 HOLE-VIA-P5RP25 — GND_CHASSIS_DIMM_NOTCH (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0612 HOLE-VIA-P5RP25 — GND_CHASSIS_LIOFLEX_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0611 HOLE-VIA-P5RP25 — GND_CHASSIS_BATTCONN_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)
ZT0610 HOLE-VIA-P5RP25 — GND_CHASSIS_LNDACARD_HOLE (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V)

C0610 0.01UF 10% 50V X7R 402
C0611 0.01UF 10% 50V X7R 402
C0612 0.01UF 10% 50V X7R 402
C0613 0.01UF 10% 50V X7R 402
C0614 0.01UF 10% 50V X7R 402
C0615 0.01UF 10% 50V X7R 402

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P (46B5) — USB2_RT_P (MAKE_BASE=TRUE) — USB_A_P (22C2)
=USB2_RT_N (46B5) — USB2_RT_N (MAKE_BASE=TRUE) — USB_A_N (22C2)
=RTUSB_OC_L (46C5) — RTUSB_OC_L (MAKE_BASE=TRUE) — USB_A_OC_L (22C4 22D8)

USB Port "B" = Trackpad (Geyser)

=USB_TRACKPAD_P (78C3) — USB_TRACKPAD_P (MAKE_BASE=TRUE) — USB_B_P (22C2)
=USB_TRACKPAD_N (78C3) — USB_TRACKPAD_N (MAKE_BASE=TRUE) — USB_B_N (22C2)
UNUSED_USB_B_OC_L (MAKE_BASE=TRUE) — USB_B_OC_L (22C4 22D8)

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P (47C3 5B1) — USB2_LT_P (MAKE_BASE=TRUE) — USB_C_P (22C2)
=USB2_LT_N (47C3 5B1) — USB2_LT_N (MAKE_BASE=TRUE) — USB_C_N (22C2)
LTUSB_OC_L (47C6 5C1) (MAKE_BASE=TRUE) — USB_C_OC_L (22C4 22D8)

USB Port "D" = Camera

=USB2_CAMERA_P (45B3 5A4) — USB2_CAMERA_P (MAKE_BASE=TRUE) — USB_D_P (22C2)
=USB2_CAMERA_N (45C3 5A4) — USB2_CAMERA_N (MAKE_BASE=TRUE) — USB_D_N (22C2)
UNUSED_USB_D_OC_L (MAKE_BASE=TRUE) — USB_D_OC_L (22C4 22D8)

USB Port "E" = ExpressCard

=USB2_EXCARD_P (47C3 5B1) — USB2_EXCARD_P (MAKE_BASE=TRUE) — USB_E_P (22C2)
=USB2_EXCARD_N (47C3 5B1) — USB2_EXCARD_N (MAKE_BASE=TRUE) — USB_E_N (22C2)
EXCARD_OC_L (50B3 47C6 5C1) (MAKE_BASE=TRUE) — USB_E_OC_L (22C4 22D8)

USB Port "F" = IR Receiver

=USB_IR_P (78B4) — USB_IR_P (MAKE_BASE=TRUE) — USB_F_P (22C2)
=USB_IR_N (78B4) — USB_IR_N (MAKE_BASE=TRUE) — USB_F_N (22C2)

USB Port "G" = Bluetooth (M13L)

=USB_BT_P (78C2) — USB_BT_P (MAKE_BASE=TRUE) — USB_G_P (22C2)
=USB_BT_N (78C2) — USB_BT_N (MAKE_BASE=TRUE) — USB_G_N (22C2)

USB Port "H" = Reserved

TP_USB_H_P (22C2 6C1) (MAKE_BASE=TRUE) — TP_USB_H_P (6C2 22C2)
TP_USB_H_N (22C2 6C1) (MAKE_BASE=TRUE) — TP_USB_H_N (6C2 22C2)

LVDS pulldown aliases

=LVDS_PD_U_CLK_N (79B8) — LVDS_U_CLK_CONN_N (MAKE_BASE=TRUE) (76B2 76D7 79C1)
=LVDS_PD_U_CLK_P (79B8) — LVDS_U_CLK_CONN_P (MAKE_BASE=TRUE) (76B2 76D7 79C1)
=LVDS_PD_U_DATA_P<0> (79C8) — LVDS_U_DATA_CONN_P<0> (MAKE_BASE=TRUE) (76C2 76D7 79D1)
=LVDS_PD_U_DATA_N<0> (79C8) — LVDS_U_DATA_CONN_N<0> (MAKE_BASE=TRUE) (76C2 76D7 79D1)
=LVDS_PD_U_DATA_P<1> (79B8) — LVDS_U_DATA_CONN_P<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_U_DATA_N<1> (79B8) — LVDS_U_DATA_CONN_N<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_U_DATA_P<2> (79B8) — LVDS_U_DATA_CONN_P<2> (MAKE_BASE=TRUE) (76B2 76D7 79C1)
=LVDS_PD_U_DATA_N<2> (79B8) — LVDS_U_DATA_CONN_N<2> (MAKE_BASE=TRUE) (76C2 76D7 79D1)
=LVDS_PD_L_CLK_N (79C8) — LVDS_L_CLK_CONN_N (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_L_CLK_P (79C8) — LVDS_L_CLK_CONN_P (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_L_DATA_P<0> (79D8) — LVDS_L_DATA_CONN_P<0> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_L_DATA_N<0> (79D8) — LVDS_L_DATA_CONN_N<0> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_L_DATA_P<1> (79D8) — LVDS_L_DATA_CONN_P<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_L_DATA_N<1> (79C8) — LVDS_L_DATA_CONN_N<1> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_L_DATA_P<2> (79C8) — LVDS_L_DATA_CONN_P<2> (MAKE_BASE=TRUE) (76C2 76D7 79C1)
=LVDS_PD_L_DATA_N<2> (79C8) — LVDS_L_DATA_CONN_N<2> (MAKE_BASE=TRUE) (76C2 76D7 79C1)

Signal Aliases/Misc Comps

SYNC_MASTER=N/A — SYNC_DATE=N/A

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-7150 | REV. A.0.0
SCALE NONE | SHT 6 OF 84

OMIT

U0700
YONAH
CPU
BGA
(1 OF 4)

ADDR GROUP0

FSB_A_L<3> J4 A3*
FSB_A_L<4> L4 A4*
FSB_A_L<5> M3 A5*
FSB_A_L<6> K5 A6*
FSB_A_L<7> M1 A7*
FSB_A_L<8> N2 A8*
FSB_A_L<9> J1 A9*
FSB_A_L<10> N3 A10*
FSB_A_L<11> P5 A11*
FSB_A_L<12> P2 A12*
FSB_A_L<13> L1 A13*
FSB_A_L<14> P4 A14*
FSB_A_L<15> P1 A15*
FSB_A_L<16> R1 A16*
FSB_ADSTB_L<0> L2 ADSTB0*

ADDR GROUP1

FSB_A_L<17> Y2 A17*
FSB_A_L<18> U5 A18*
FSB_A_L<19> R3 A19*
FSB_A_L<20> W6 A20*
FSB_A_L<21> U4 A21*
FSB_A_L<22> Y5 A22*
FSB_A_L<23> U2 A23*
FSB_A_L<24> R4 A24*
FSB_A_L<25> T5 A25*
FSB_A_L<26> T3 A26*
FSB_A_L<27> W3 A27*
FSB_A_L<28> W5 A28*
FSB_A_L<29> Y4 A29*
FSB_A_L<30> W2 A30*
FSB_A_L<31> Y1 A31*
FSB_ADSTB_L<1> V4 ADSTB1*

CPU_A20M_L A6 A20M*
CPU_FERR_L A5 FERR*
CPU_IGNNE_L C4 IGNNE*
CPU_STPCLK_L D5 STPCLK*
CPU_INTR C6 LINT0
CPU_NMI B4 LINT1
CPU_SMI_L A3 SMI*

RESERVED

TP_CPU_A32_L AA1 RSVD1
TP_CPU_A33_L AA4 RSVD2
TP_CPU_A34_L AB2 RSVD3
TP_CPU_A35_L AA3 RSVD4
TP_CPU_A36_L M4 RSVD5
TP_CPU_A37_L N5 RSVD6
TP_CPU_A38_L T2 RSVD7
TP_CPU_A39_L V3 RSVD8
TP_CPU_APM0_L B2 RSVD9
TP_CPU_APM1_L C3 RSVD10
TP_CPU_HFPLL B25 RSVD11

CONTROL

ADS* H1 FSB_ADS_L
BNR* E2 FSB_BNR_L
BPRI* G5 FSB_BPRI_L
DEFER* H5 FSB_DEFER_L
DRDY* F21 FSB_DRDY_L
DBSY* E1 FSB_DBSY_L
BR0* F1 FSB_BREQ0_L
IERR* D20 FSB_IERR_L
INIT* B3 CPU_INIT_L
LOCK* H4 FSB_LOCK_L
RESET* B1 FSB_CPURST_L
RS0* F3 FSB_RS_L<0>
RS1* F4 FSB_RS_L<1>
RS2* G3 FSB_RS_L<2>
TRDY* G2 FSB_TRDY_L
HIT* G6 FSB_HIT_L
HITM* E4 FSB_HITM_L

REQ0* K3 FSB_REQ_L<0>
REQ1* H2 FSB_REQ_L<1>
REQ2* K2 FSB_REQ_L<2>
REQ3* J3 FSB_REQ_L<3>
REQ4* L5 FSB_REQ_L<4>

XDP/ITP SIGNALS

BPM0* AD4 XDP_BPM_L<0>
BPM1* AD3 XDP_BPM_L<1>
BPM2* AD1 XDP_BPM_L<2>
BPM3* AC4 XDP_BPM_L<3>
PRDY* AC2 XDP_BPM_L<4>
PREQ* AC1 XDP_BPM_L<5>
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST* AB6 XDP_TRST_L
DBR* C20 XDP_DBRESET_L

THERM

PROCHOT* D21 CPU_PROCHOT_L
THERMDA A24 CPU_THERMD_P
THERMDC A25 CPU_THERMD_N
THERMTRIP* C7 PM_THRMTRIP_L

HCLK

BCLK0 A22 FSB_CLK_CPU_P
BCLK1 A21 FSB_CLK_CPU_N

RSVD12 T22 TP_CPU_EXTBREF
RSVD13 D2 TP_CPU_SPARE0
RSVD14 F6 TP_CPU_SPARE1
RSVD15 D3 TP_CPU_SPARE2
RSVD16 C1 TP_CPU_SPARE3
RSVD17 AF1 TP_CPU_SPARE4
RSVD18 D22 TP_CPU_SPARE5
RSVD19 C23 TP_CPU_SPARE6
RSVD20 C24 TP_CPU_SPARE7

SPARE[7-0],HFPLL:
ROUTE TO TP VIA AND
PLACE GND VIA W/IN 1000 MILS

=PP1V05_S0_CPU

R0702 54.9 1% 1/16W MF-LF 402
R0703 54.9 1% 1/16W MF-LF 402
R0704 68 5% 1/16W MF-LF 402

PLACE TESTPOINT ON
FSB_IERR_L WITH A GND
0.1" AWAY

CPU_PROCHOT_L TO SMC
AND CPU VR TO INFORM
CPU IS HOT

PM_THRMTRIP#
SHOULD CONNECT TO
ICH7-M AND GMCH
WITHOUT T-ING (NO
STUB)

R0720 54.9 1% 402 XDP_TMS
R0721 54.9 1% 402 XDP_TDI
R0722 54.9 1% 402 XDP_TCK

R0705 1K 1% 1/16W MF-LF 402
R0706 2.0K 1% 1/16W MF-LF 402
LAYOUT NOTE: 0.5" MAX LENGTH

CPU_GTLREF
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>

NOSTUFF R0730 0 402
R0712 51 5% 1/16W MF-LF 402
NOSTUFF R0707 1K 5% 1/16W MF-LF 402

OMIT

U0700
YONAH
CPU
BGA
(2 OF 4)

DATA GRP0

FSB_D_L<0> E22 D0*
FSB_D_L<1> F24 D1*
FSB_D_L<2> E26 D2*
FSB_D_L<3> H22 D3*
FSB_D_L<4> F23 D4*
FSB_D_L<5> G25 D5*
FSB_D_L<6> E25 D6*
FSB_D_L<7> E23 D7*
FSB_D_L<8> K24 D8*
FSB_D_L<9> G24 D9*
FSB_D_L<10> J24 D10*
FSB_D_L<11> J23 D11*
FSB_D_L<12> H26 D12*
FSB_D_L<13> F26 D13*
FSB_D_L<14> K22 D14*
FSB_D_L<15> H25 D15*
FSB_DSTBN_L<0> H23 DSTBN0*
FSB_DSTBP_L<0> G22 DSTBP0*
FSB_DINV_L<0> J26 DINV0*

DATA GRP1

FSB_D_L<16> N22 D16*
FSB_D_L<17> K25 D17*
FSB_D_L<18> P26 D18*
FSB_D_L<19> R23 D19*
FSB_D_L<20> L25 D20*
FSB_D_L<21> L22 D21*
FSB_D_L<22> L23 D22*
FSB_D_L<23> M23 D23*
FSB_D_L<24> P25 D24*
FSB_D_L<25> P22 D25*
FSB_D_L<26> P23 D26*
FSB_D_L<27> T24 D27*
FSB_D_L<28> R24 D28*
FSB_D_L<29> L26 D29*
FSB_D_L<30> T25 D30*
FSB_D_L<31> N24 D31*
FSB_DSTBN_L<1> M24 DSTBN1*
FSB_DSTBP_L<1> N25 DSTBP1*
FSB_DINV_L<1> M26 DINV1*

MISC

GTLREF AD26
NC A2
TEST1 C26
TEST2 D25
BSEL0 B22
BSEL1 B23
BSEL2 C21

DATA GRP2

D32* AA23 FSB_D_L<32>
D33* AB24 FSB_D_L<33>
D34* V24 FSB_D_L<34>
D35* V26 FSB_D_L<35>
D36* W25 FSB_D_L<36>
D37* U23 FSB_D_L<37>
D38* U25 FSB_D_L<38>
D39* U22 FSB_D_L<39>
D40* AB25 FSB_D_L<40>
D41* W22 FSB_D_L<41>
D42* Y23 FSB_D_L<42>
D43* AA26 FSB_D_L<43>
D44* Y26 FSB_D_L<44>
D45* Y22 FSB_D_L<45>
D46* AC26 FSB_D_L<46>
D47* AA24 FSB_D_L<47>
DSTBN2* W24 FSB_DSTBN_L<2>
DSTBP2* Y25 FSB_DSTBP_L<2>
DINV2* V23 FSB_DINV_L<2>

DATA GRP3

D48* AC22 FSB_D_L<48>
D49* AC23 FSB_D_L<49>
D50* AB22 FSB_D_L<50>
D51* AA21 FSB_D_L<51>
D52* AB21 FSB_D_L<52>
D53* AC25 FSB_D_L<53>
D54* AD20 FSB_D_L<54>
D55* AE22 FSB_D_L<55>
D56* AF23 FSB_D_L<56>
D57* AD24 FSB_D_L<57>
D58* AE21 FSB_D_L<58>
D59* AD21 FSB_D_L<59>
D60* AE25 FSB_D_L<60>
D61* AF25 FSB_D_L<61>
D62* AF22 FSB_D_L<62>
D63* AF26 FSB_D_L<63>
DSTBN3* AD23 FSB_DSTBN_L<3>
DSTBP3* AE24 FSB_DSTBP_L<3>
DINV3* AC20 FSB_DINV_L<3>

MISC

COMP0 R26 CPU_COMP<0>
COMP1 U26 CPU_COMP<1>
COMP2 U1 CPU_COMP<2>
COMP3 V1 CPU_COMP<3>
DPRSTP* E5 CPU_DPRSTP_L
DPSLP* B5 CPU_DPSLP_L
DPWR* D24 FSB_DPWR_L
PWRGOOD D6 CPU_PWRGD
SLP* D7 FSB_SLPCPU_L
PSI* AE6 CPU_PSI_L

LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM, MAKE
TRACE LENGTH SHORTER THAN 0.5".

R0716 27.4 1% 402
R0717 54.9 1% 402
R0718 27.4 1% 402
R0719 54.9 1% 402

CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9

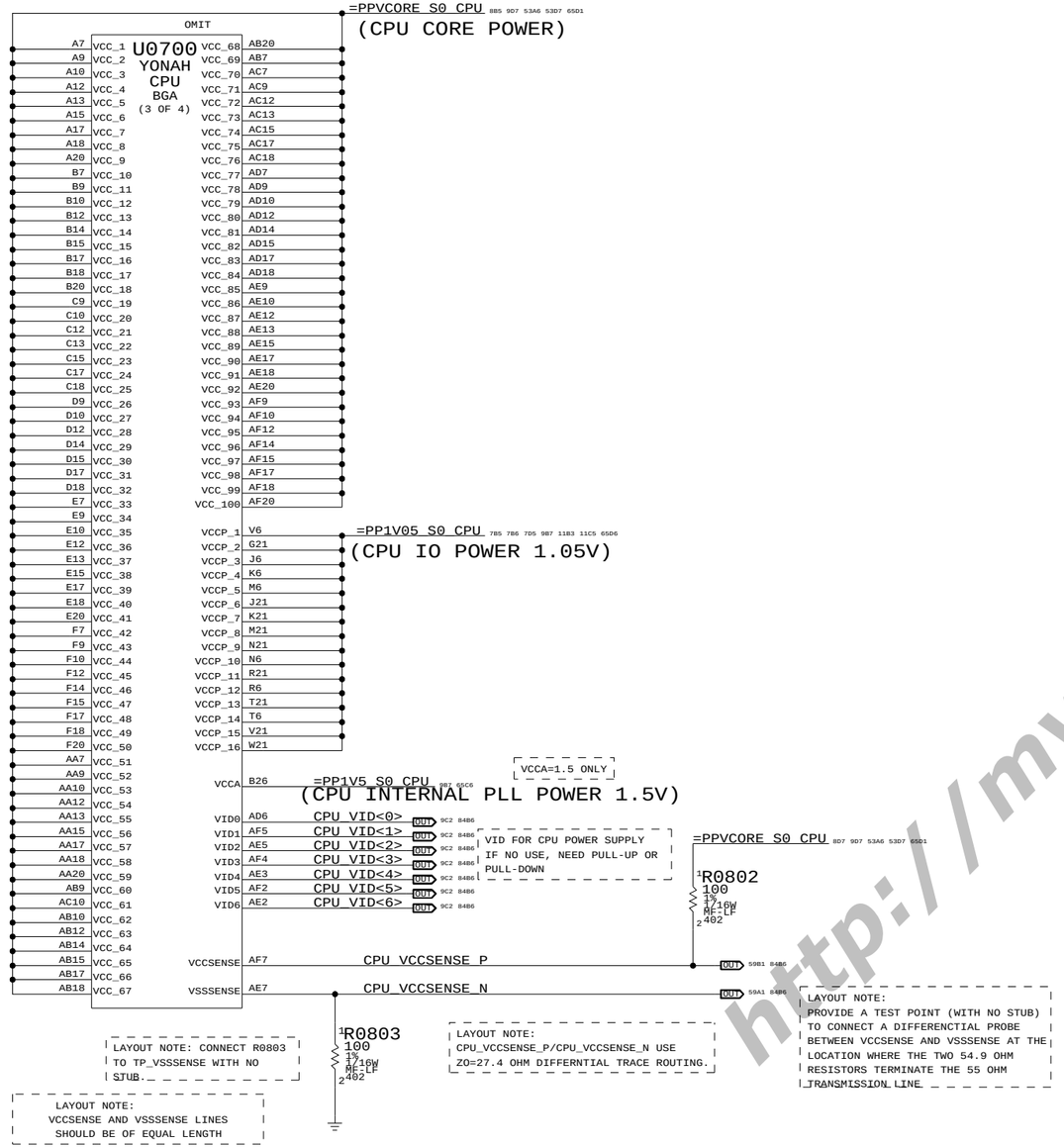
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)

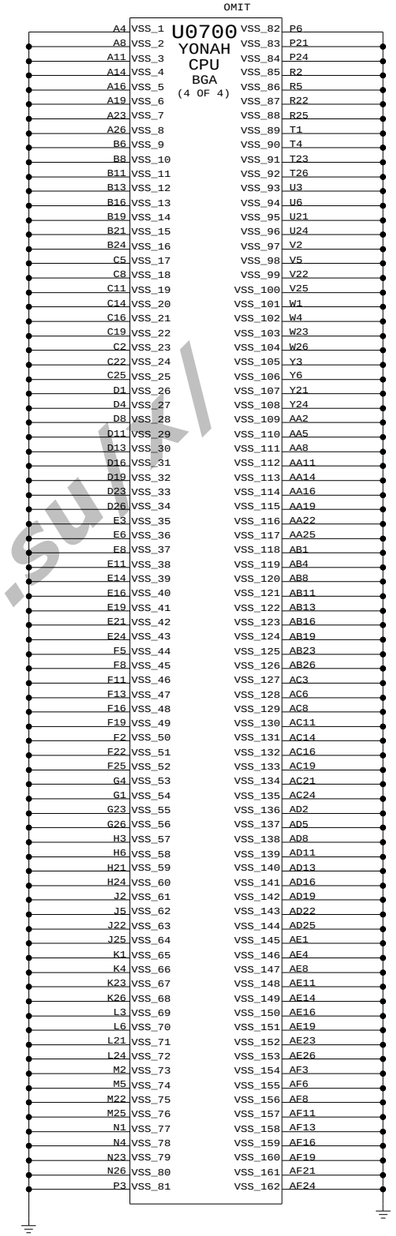
CPU 1 OF 2-FSB

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 7 OF 84	





CPU 2 OF 2-PWR/GND

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 8 OF 84

CPU VCORE HF AND BULK DECOUPLING

65D1 53D7 53A6 8D7 8B5 =PPVCORE_S0_CPU

4x 330uF. 20x 22uF 0805

C0900 C0901 C0902 C0903 C0904 C0905 C0906 C0907 C0908 C0909
22UF 20% 6.3V CERM 805

C0910 C0911 C0912 C0913 C0914 C0915 C0916 C0917 C0918 C0919
22UF 20% 6.3V CERM 805

CRITICAL C0950 330UF 20% 2.5V POLY D2T
CRITICAL C0952 330UF 20% 2.5V POLY D2T
CRITICAL C0953 330UF 20% 2.5V POLY D2T
CRITICAL C0954 330UF 20% 2.5V POLY D2T

VCCA (CPU AVdd) Decoupling

65C6 8B7 =PP1V5_S0_CPU

1x 10uF, 1x 0.01uF

C0980 10uF 20% 6.3V X5R 603
C0981 0.01UF 20% 16V CERM 402

VCCP (CPU I/O) Decoupling

65D6 11C5 11B3 8C7 7D5 7B6 7B5 =PP1V05_S0_CPU

1x 470uF, 6x 0.1uF 0402

C0935 470uF 20% 2.5V TANT D2T CRITICAL
C0936 C0937 C0938 C0939 C0940 C0941
0.1UF 20% 10V CERM 402

NOTE: This cap is shared between CPU and NB

CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production

RP0990
0
5%
8486 8B7 CPU_VID<0> 1 — 8 IMVP6_VID<0> 59C7
8486 8B7 CPU_VID<1> 2 — 7 IMVP6_VID<1> 59C7
8486 8B7 CPU_VID<2> 3 — 6 IMVP6_VID<2> 59C7
8486 8B7 CPU_VID<3> 4 — 5 IMVP6_VID<3> 59C7
1/16W
SM-LF

RP0991
0
5%
8486 8B7 CPU_VID<4> 1 — 8 IMVP6_VID<4> 59C7
8486 8B7 CPU_VID<5> 2 — 7 IMVP6_VID<5> 59C7
8486 8B7 CPU_VID<6> 3 — 6 IMVP6_VID<6> 59C7
NC 4 — 5 NC
1/16W
SM-LF

CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 9 OF 84	

CPU ZONE THERMAL SENSOR

LAYOUT NOTE:
ADD GND GUARD TRACE
FOR CPU_THERMD_P AND
CPU_THERMD_N

LAYOUT NOTE:
ROUTE CPU_THERMD_P AND
CPU_THERMD_N ON SAME
LAYER.
10 MIL TRACE
10 MIL SPACING

(TO CPU INTERNAL THERMAL DIODE)
(TC0D)

OUT 7C6 CPU_THERMD_P
IN 7C6 CPU_THERMD_N

R1001 499 1% 1/16W MF-LF 402
R1002 499 1% 1/16W MF-LF 402
C1001 0.001UF 10% 50V CERM 402

THRM_CPU_DX_P
THRM_CPU_DX_N

65B3 =PP3V3_S0_THRM_SNR
C1002 0.1UF 10% 16V X5R 402
R1006 10K 5% 1/16W MF-LF 402
R1005 10K 5% 1/16W MF-LF 402

U1001 TMP401 MSOP CRITICAL

1	VDD		
2	D+		
3	D-		
4	THM*	THRM_ALERT	
5	GND		
6	ALERT*/THM2*	THRM_ALERT_L	
7	SDATA	27D1 SMB_THRM_DATA	TO
8	SCLK	27D1 SMB_THRM_CLK	TO

PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

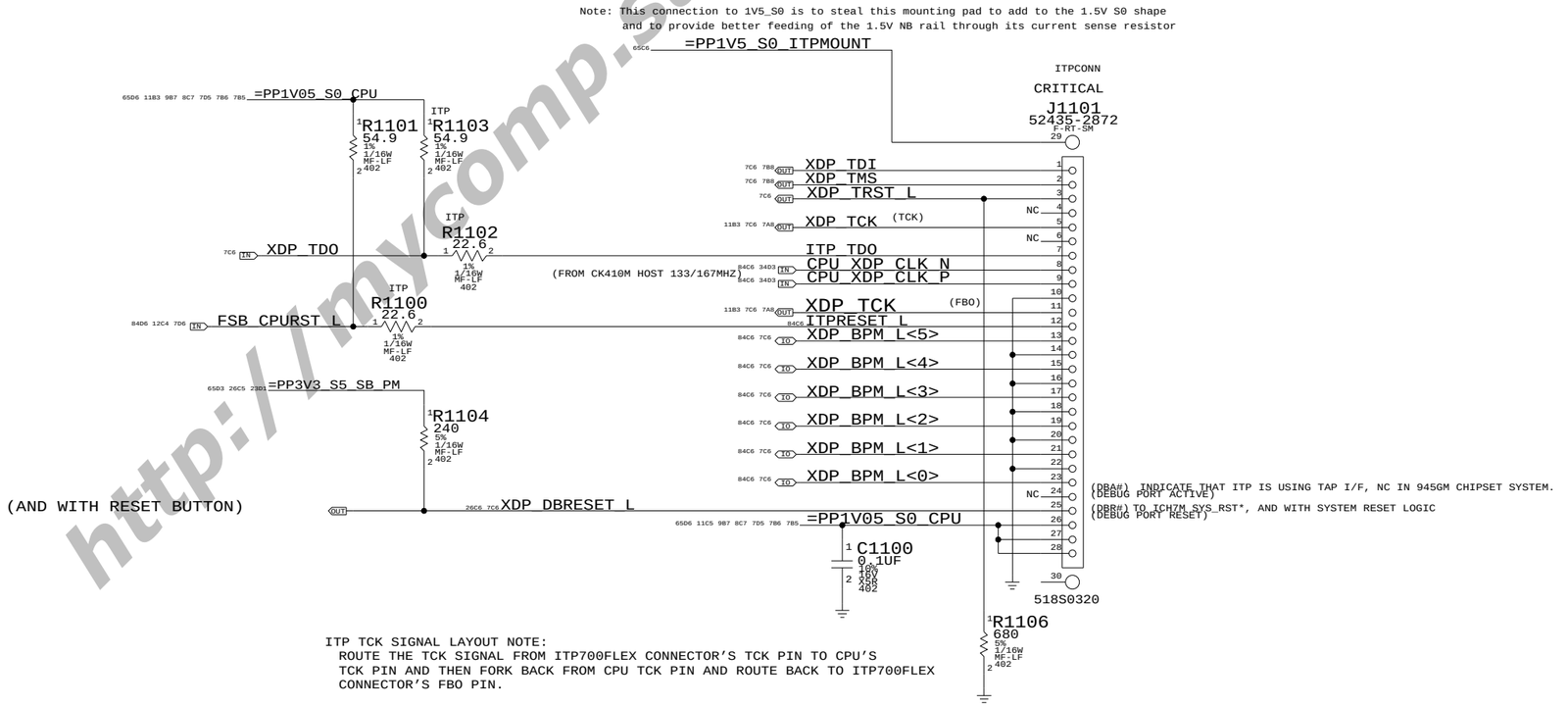
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	10	84

CPU ITP700FLEX DEBUG SUPPORT



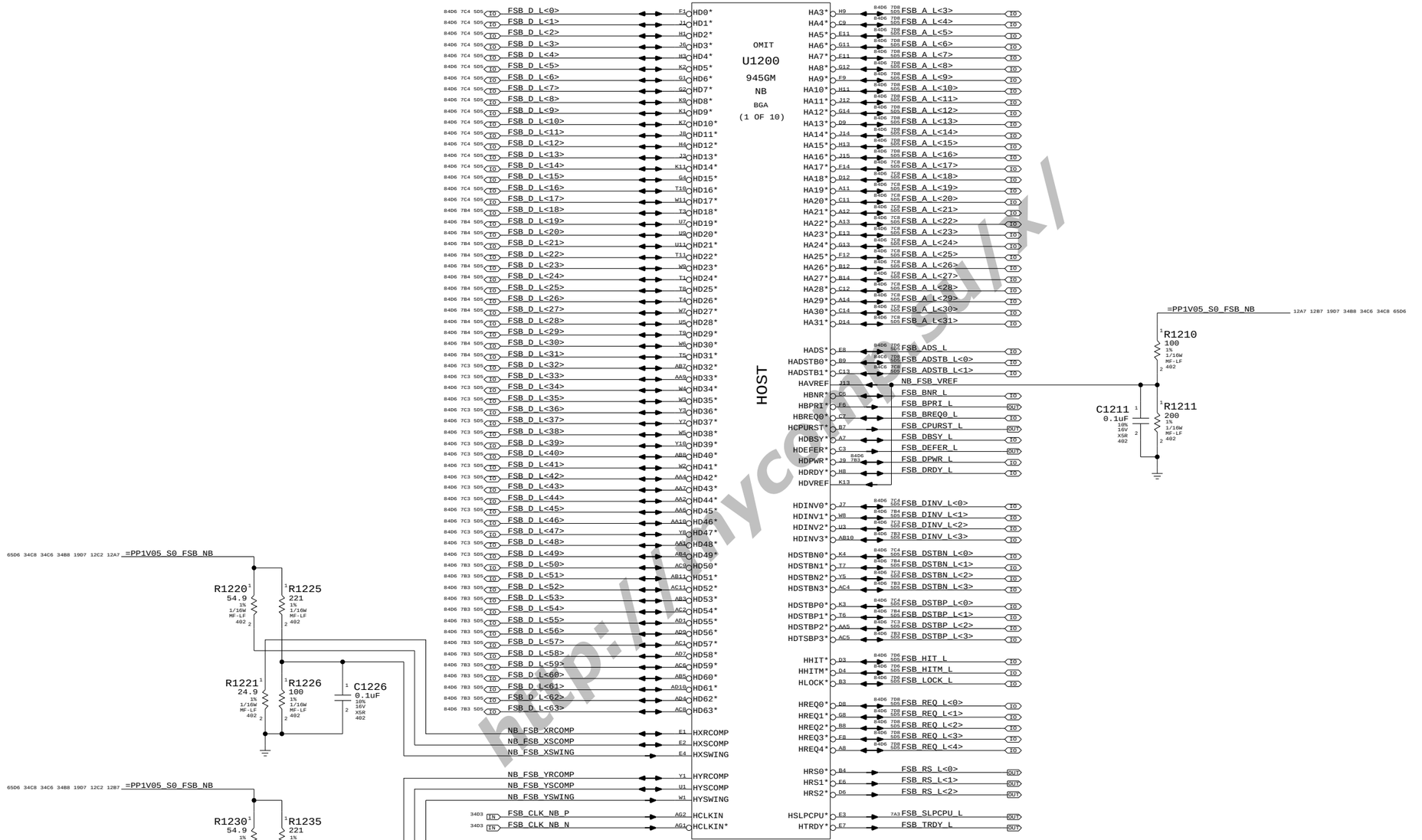
ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 11 OF 84	



APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
	SCALE: NONE	SHT 12 OF 84	

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

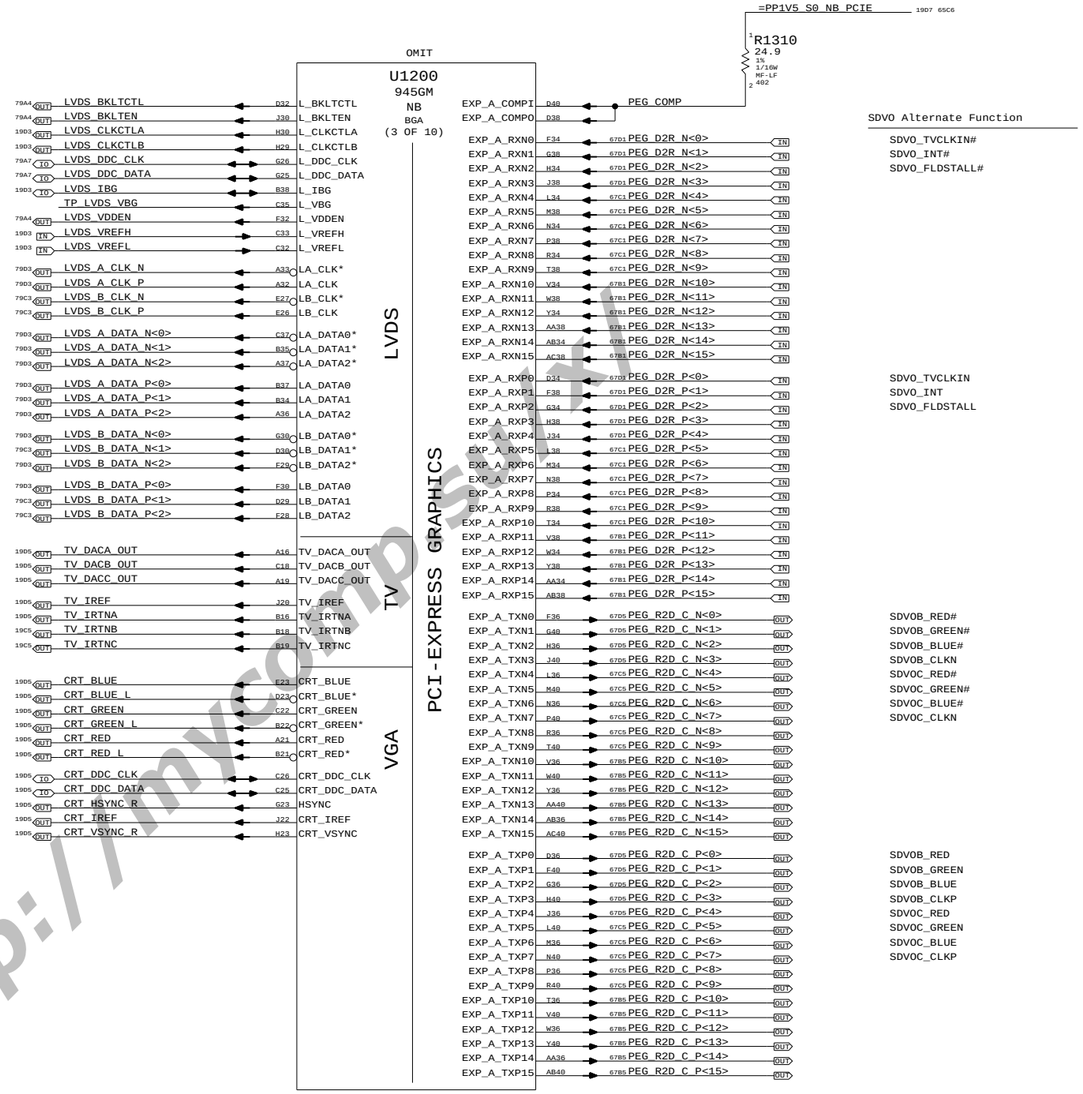
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.

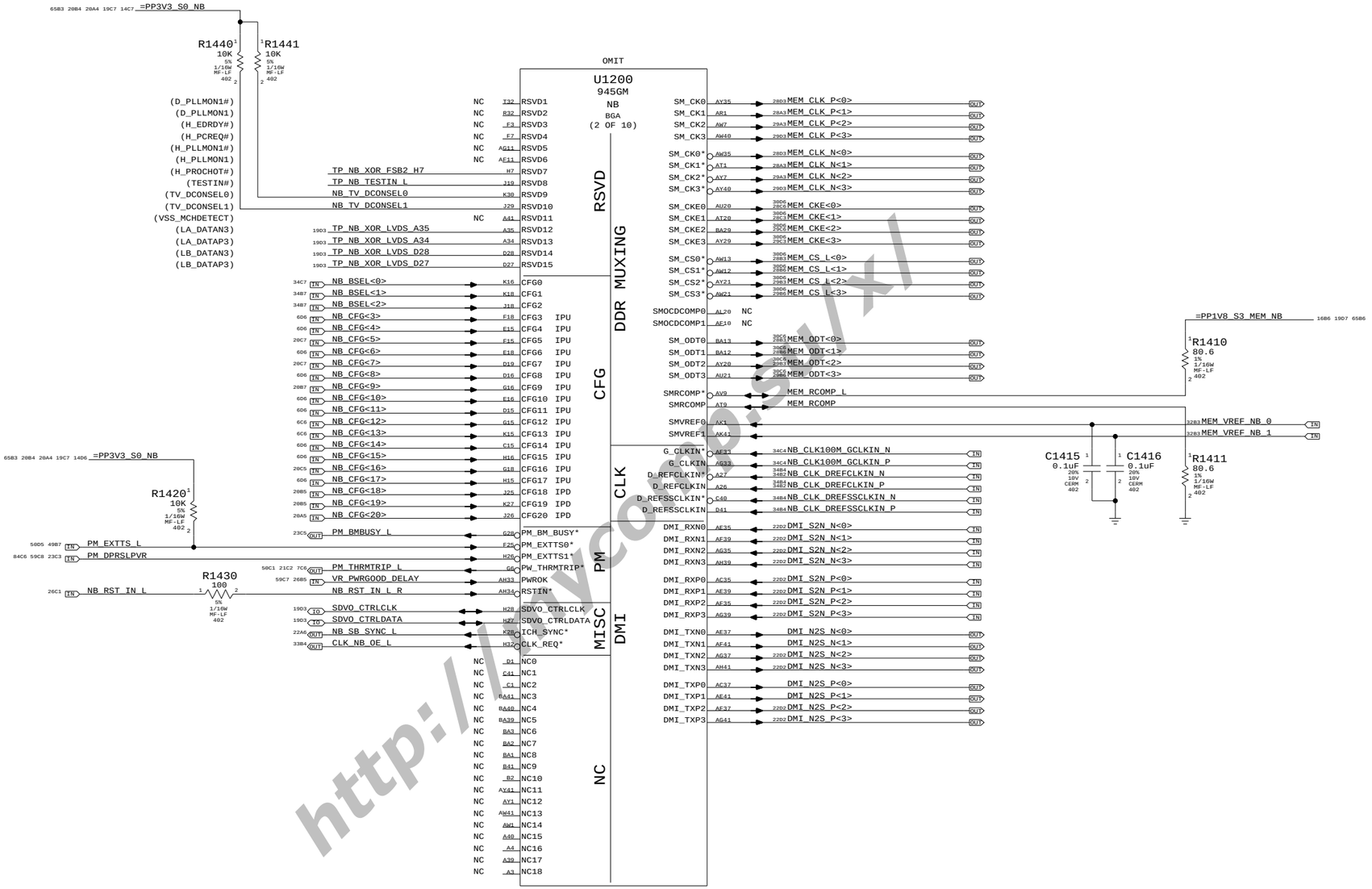


NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 13 OF 84	



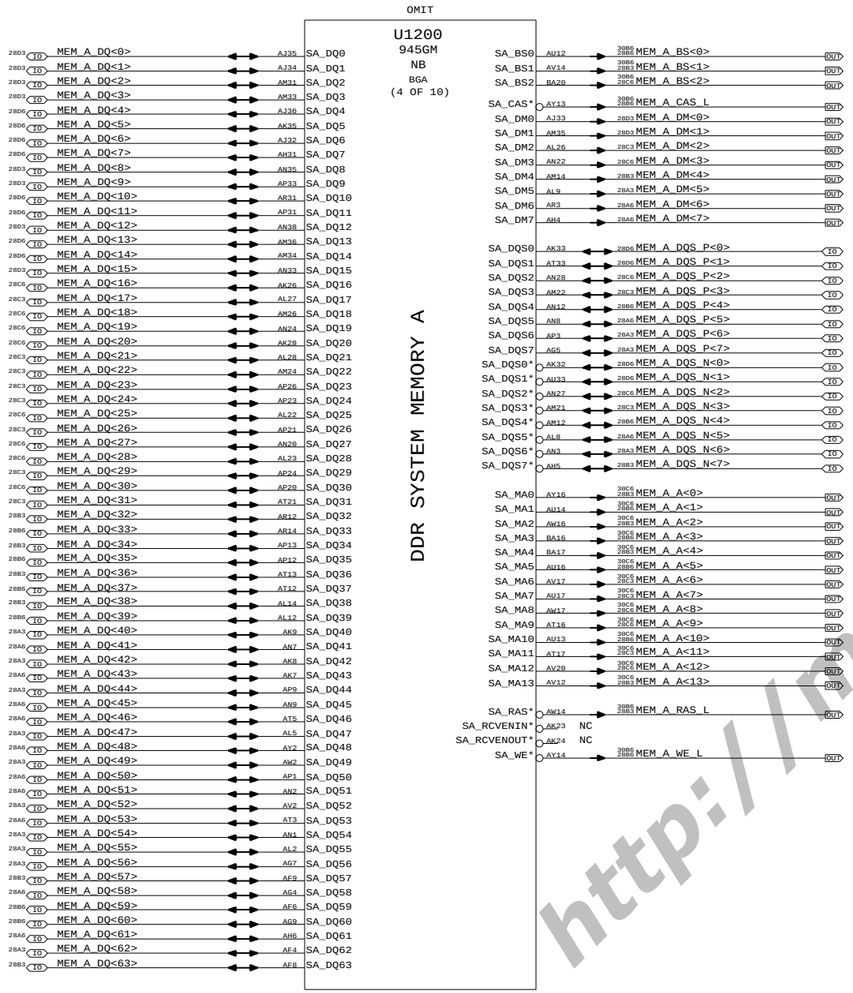
NB Misc Interfaces

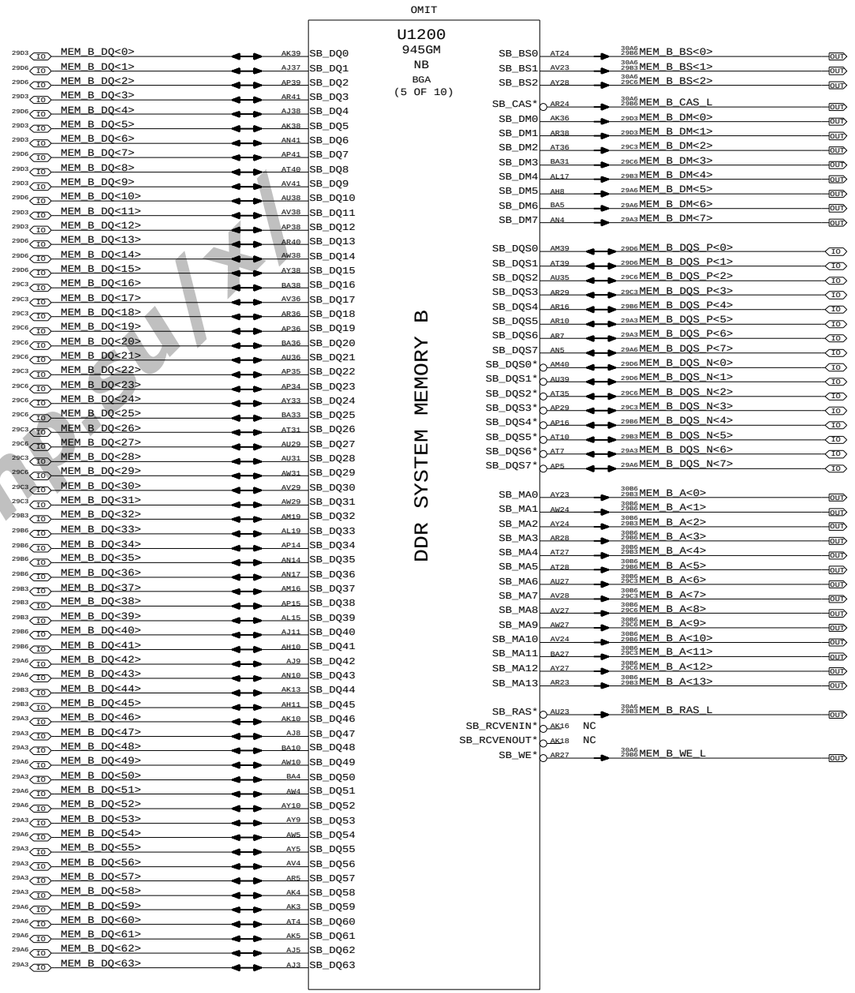
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 14 OF 84





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

=PPVCORE_S0_NB 16D3 19C8 19D2 19D7 65D6

1.05V or 1.5V

U1200
945GM
NB
BGA
(6 OF 10)

OMIT

VCC

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47UF 10% 6.3V CERM-X5R 402
C1613 0.47UF 10% 6.3V CERM-X5R 402

C1615 0.47UF 10% 6.3V CERM-X5R 402
65B6 19D7 14C2 =PP1V8_S3_MEM_NB
Layout Note:
Place near pin BA23

C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
Layout Note:
Place in cavity

C1610 0.47UF 10% 6.3V CERM-X5R 402
Layout Note:
Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 0.47UF 10% 6.3V CERM-X5R 402
C1611 0.47UF 10% 6.3V CERM-X5R 402

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

65D6 19D7 19D2 19C8 16C8 =PPVCORE_S0_NB

OMIT

U1200
945GM
NB
BGA
(7 OF 10)

NCTF

=PP1V5_S0_NB_VCCAUX 17B6 19C4 19D7 65B6

NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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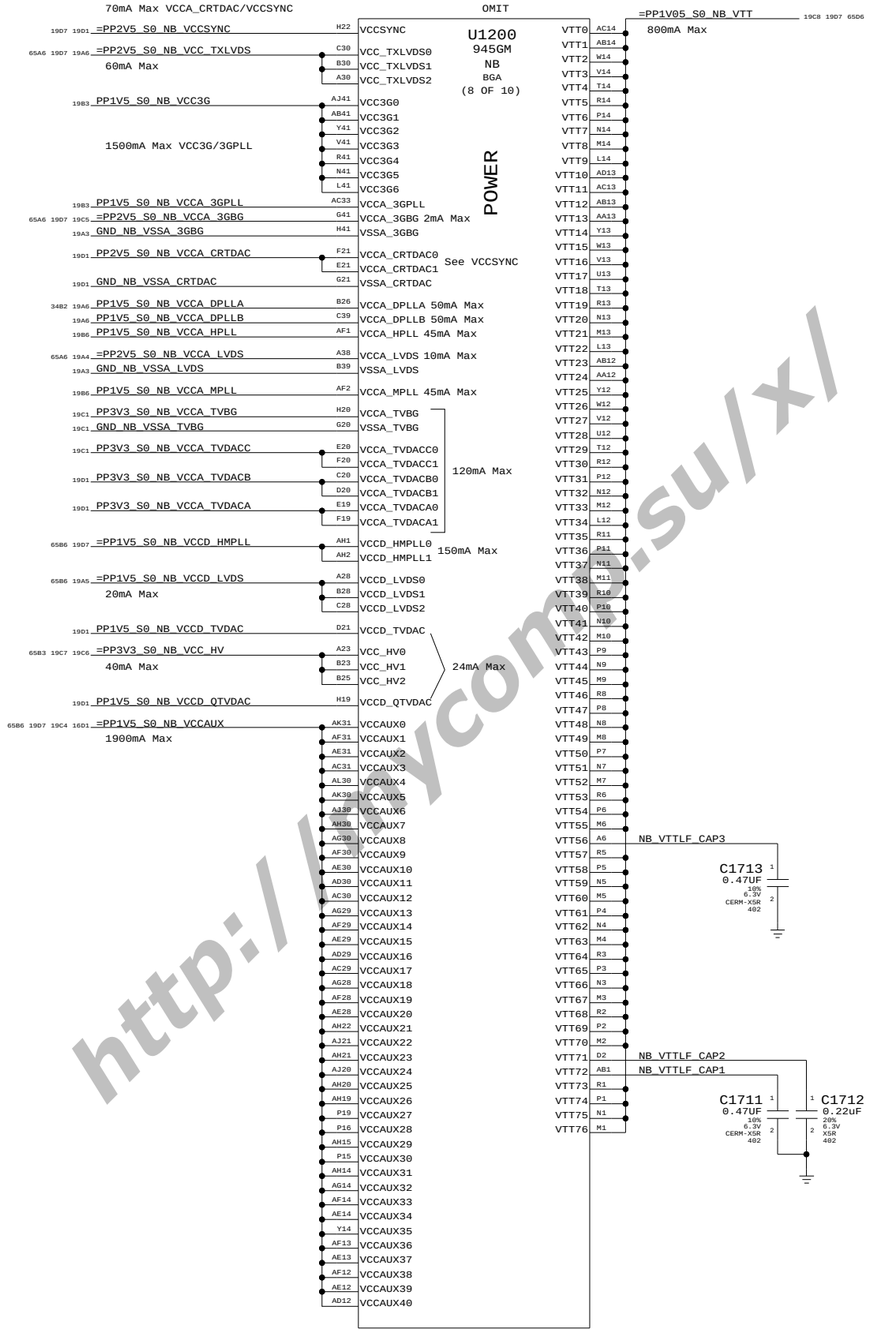
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 16 OF 84	

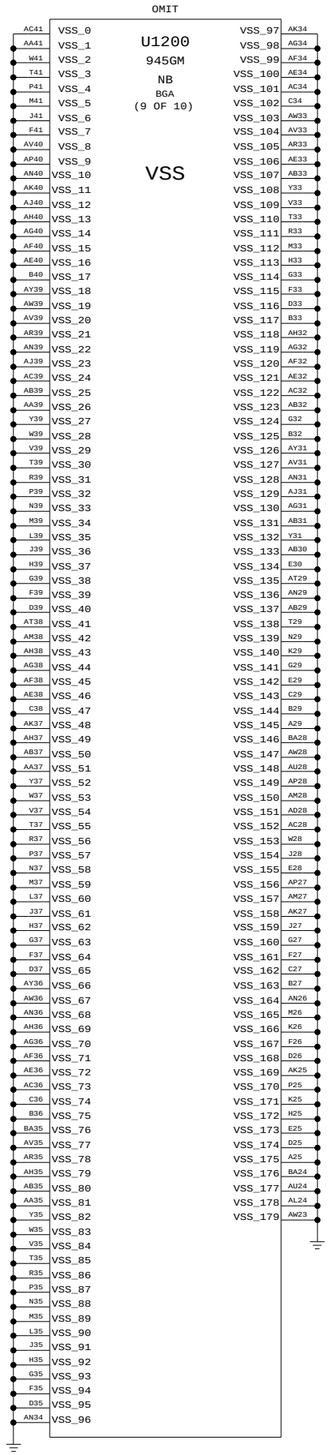


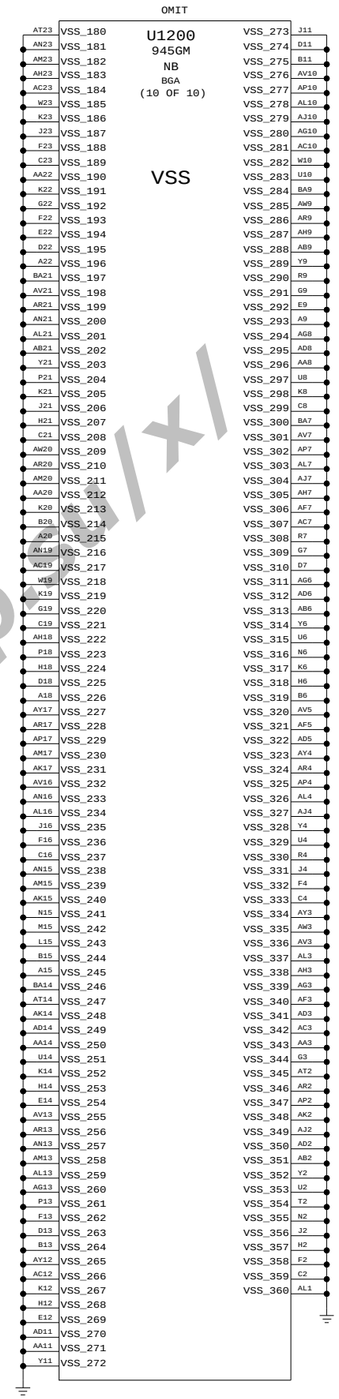
NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 17 OF 84	





NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 18 OF 84	

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	16C8 16D3 19C8 19D2 65D6	1500mA Max
	=PP1V05_S0_FSB_NB	12A7 12B7 12C2 14B8 34C6 34C8 65D5	10mA Max?
	=PP1V05_S0_NB_VTT	17D3 19C8 65D6	800mA Max
	=PP1V05_S0_NB_CRT	19D6 65D6	?mA Max
3674mA Max	=PP1V5_S0_NB	60A7 65C6 65C8	?mA Max
	=PP1V5_S0_NB_3G	19B5 65C6	1500mA Max
	=PP1V5_S0_NB_3GPLL	19B5 65C6	
	=PP1V5_S0_NB_PCIE	13D2 65C6	?mA Max
	=PP1V5_S0_NB_PLL	19B8 65B6	100mA Max
	=PP1V5_S0_NB_TVDAC	19D2 19D6 65B6	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	17C6 65B6	150mA Max
	=PP1V5_S0_NB_VCCAUX	16D1 17B6 19C4 65B6	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	14C2 16B6 65B6	3200mA Max
132mA Max	=PP2V5_S0_NB_VCCSYNC	17D6 19D1	70mA Max
	=PP2V5_S0_NB_VCC_TXLVDS	17D6 19A6 65A6	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	17D6 19C5 65A6	2mA Max
40mA Max?	=PP3V3_S0_NB	14C7 14D6 20A4 20B4 65B3	?mA Max
	=PP3V3_S0_NB_VCC_HV	17C6 19C6 65B3	40mA Max

65D6 19D7 =PP1V05_S0_NB_CRT

- CRT_RED — 13B5
- CRT_GREEN — 13B5
- CRT_BLUE — 13B5
- CRT_RED_L — 13B5
- CRT_GREEN_L — 13B5
- CRT_BLUE_L — 13B5
- CRT_IREF — 13B5
- CRT_HSYNC_R — 13B5
- CRT_VSYNC_R — 13B5

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK — 13B5

TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA — 13B5

65B6 19D7 19D2 =PP1V5_S0_NB_TVDAC

- TV_DACA_OUT — 13C5
- TV_DACB_OUT — 13C5
- TV_DACC_OUT — 13C5
- TV_IREF — 13C5
- TV_IRTNA — 13C5
- TV_IRTNB — 13C5
- TV_IRTNC — 13C5

TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA — 13D5

TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB — 13D5

NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 — 14C6

NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 — 14C6

NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 — 14C6

NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE, NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 — 14C6

TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK — 14B6

TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA — 14B6

LVDS_IBG — 13D5

R1990 1.5K 1% 1/16W MF-LF 402

- LVDS_VREFH — 13D5
- LVDS_VREFL — 13D5

65D6 19D7 19C8 16D3 16C8 =PPVCORE_S0_NB

(MCH CRTDAC ANALOG 2.5V PWR)
- PP2V5_S0_NB_VCCA_CRTDAC — 17D6
- GND_NB_VSSA_CRTDAC — 17D6

(MCH H/V SYNC 2.5V PWR)
- =PP2V5_S0_NB_VCCSYNC — 17D6 19D7

65B6 19D7 19D6 =PP1V5_S0_NB_TVDAC

(MCH TVDAC DEDICATED PWR 1.5V)
- PP1V5_S0_NB_VCCD_TVDAC — 17C6

(MCH TVDAC DIGITAL QUIET 1.5V PWR)
- PP1V5_S0_NB_VCCD_QTVDAC — 17B6

(MCH TV OUT CHANNEL A 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACA — 17C6

(MCH TV OUT CHANNEL B 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACB — 17C6

(MCH TV OUT CHANNEL C 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVDACC — 17C6

(MCH TV DAC BAND GAP 3.3V PWR)
- PP3V3_S0_NB_VCCA_TVBG — 17C6
- GND_NB_VSSA_TVBG — 17C6

65D6 19D7 16C8 16D3 16C7 =PPVCORE_S0_NB — 1500mA Max

GMCH CORE PWR 1.05V BYPASS

CRITICAL
C1900 470uF 20% 2.5V TANT D2T

C1902 10uF 20% 6.3V X5R 603
C1903 10uF 20% 6.3V X5R 603
C1904 1uF 10% 6.3V CERM 402
C1905 0.22uF 20% 6.3V X5R 402
C1906 0.22uF 20% 6.3V X5R 402
C1907 0.22uF 20% 6.3V X5R 402

65D6 19D7 17D3 =PP1V05_S0_NB_VTT — 800mA Max

MCH VTT BYPASS
(MCH FSB 1.05V PWR)
(SHARE C0940 470UF)

C1965 4.7uF 20% 6.3V CERM 603
C1966 2.2uF 20% 6.3V CERM1 603

Layout Note: Place in cavity

C1967 0.22uF 20% 6.3V X5R 402

Layout Note: Place on the edge

65B3 19C7 17C6 =PP3V3_S0_NB_VCC_HV — 40mA Max

MCH VCC_HV BYPASS
(MCH HV BUFFER 3.3V PWR)

C1914 10uF 20% 6.3V X5R 603
C1915 0.1uF 20% 10V CERM 402

65A6 19D7 17D6 =PP2V5_S0_NB_VCCA_3GBG — 2mA Max

MCH VCCA_3GBG BYPASS
(MCH PCIE/DMI BAND GAP 2.5V PWR)

C1916 0.1uF 20% 10V CERM 402

65B6 19D7 17B6 16D1 =PP1V5_S0_NB_VCCAUX — 1900mA Max

GMCH VCCAUX FILTER
(MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)

C1918 0.1uF 20% 10V CERM 402

65D6 19D7 19C8 16D3 16C8 =PPVCORE_S0_NB — 1500mA Max

65C6 19D7 =PP1V5_S0_NB_3G

L1970 91nH 1210

Layout Note: Place L and C close to MCH

C1970 220UF 20% 2.5V POLY CASE-B2

GMCH VCC3G FILTER
(PCI-E/DMI ANALOG 1.5V PWR)

C1971 10uF 20% 6.3V X5R 603
C1972 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

PP1V5_S0_NB_VCC3G — 17D6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

1500mA Max

65C6 19D7 =PP1V5_S0_NB_3GPLL

L1975 1.0UH-220MA-0.12-OHM 0805

PP1V5_S0_NB_3GPLL_F
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.4 mm
VOLTAGE=1.5V

R1975 0.51 1% 1/16W MF-LF 402

GMCH VCCA_3GPLL FILTER
(3GIO PLL 1.5V PWR)

C1975 10uF 20% 6.3V X5R 603
C1976 0.1uF 20% 10V CERM 402

PP1V5_S0_NB_VCCA_3GPLL — 17D6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

GND_NB_VSSA_3GBG — 17D6

Layout Note: 3GPLL 10uF cap should be placed in cavity

Layout Note: Route to caps, then GND

1500mA Max

65B6 19D7 19D1 =PP1V8_S3_MEM_NB — 100mA Max

L1934 FERR-120-OHM-0.2A 0603

GMCH VCCA_HPLL FILTER
(HOST PLL 1.5V PWR)

C1934 22UF 20% 6.3V CERM 805
C1935 0.1uF 20% 10V CERM 402

PP1V5_S0_NB_VCCA_HPLL — 17C6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

45mA Max

65B6 19D7 =PP1V5_S0_NB_PLL — 100mA Max

L1936 FERR-120-OHM-0.2A 0603

GMCH VCCA_MPLL FILTER
(MCH MEMORY PLL 1.5V PWR)

C1936 22UF 20% 6.3V CERM 805
C1937 0.1uF 20% 10V CERM 402

PP1V5_S0_NB_VCCA_MPLL — 17C6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

45mA Max

65A6 =PP2V5_S0_NB_DPLL — 132mA Max

CRITICAL
U1900 TPS73115 SOT23-5
IN, EN, GND, OUT, NR/FB
TPS73115_NR

MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V

C1950 1uF 10% 6.3V CERM 402
C1951 0.01uF 10% 16V CERM 402
C1952 10uF 20% 6.3V X5R 603

NO STUFF
R1953 0 5% 1/16W MF-LF 402
R1954 0 5% 1/16W MF-LF 402

C1953 0.1uF 20% 10V CERM 402
C1954 0.1uF 20% 10V CERM 402

GMCH VCCA_DPLLA FILTER
(CRT/TVOUT PLL 1.5V PWR)

PP1V5_S0_NB_VCCA_DPLLA — 17C6 34B2
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
50MA MAX

GMCH VCCA_DPLLB FILTER
(LVDS PLL 1.5V PWR)

PP1V5_S0_NB_VCCA_DPLLB — 17C6 65A6 19D7 17D6
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.5V
50MA MAX

MCH VCC_TXLVDS BYPASS
(MCH LVDS TRANSMITTER 2.5V PWR)

65A6 19D7 17D6 =PP2V5_S0_NB_VCC_TXLVDS — 60MA MAX

C1990 4.7UF 20% 6.3V CERM 603
C1991 0.1uF 20% 10V CERM 402

MCH VCCD_LVDS BYPASS
(MCH LVDS DIGITAL 1.5V PWR)

65B6 17C6 =PP1V5_S0_NB_VCCD_LVDS — 20MA MAX

C1992 10UF 20% 6.3V XSR 603
C1993 0.1uF 20% 10V CERM 402

MCH VCCA_LVDS BYPASS
(MCH LVDS ANALOG 2.5V PWR)

65A6 17C6 =PP2V5_S0_NB_VCCA_LVDS — 10MA MAX

C1994 0.01UF 20% 16V CERM 402
C1995 0.1uF 20% 10V CERM 402

GND_NB_VSSA_LVDS — 17C6

Layout Note: Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 19 OF 84	

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14C6 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
R2075
2.2K
5%
1/16W
MF-LF
402
1
2

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14C6 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
R2077
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<8>	RESERVED

14C6 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
R2079
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14C6 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
R2085
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 65B3
NBCFG_VCC_1V5
R2058
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14C6 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4 65B3
NBCFG_DMI_REVERSE
R2059
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14C6 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14C7 14D6 19C7 20B4 65B3
NBCFG_SDVO_AND_PCIE
R2060
2.2K
5%
1/16W
MF-LF
402
1
2

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14B6 NB_CFG<20>
Internal pull-down

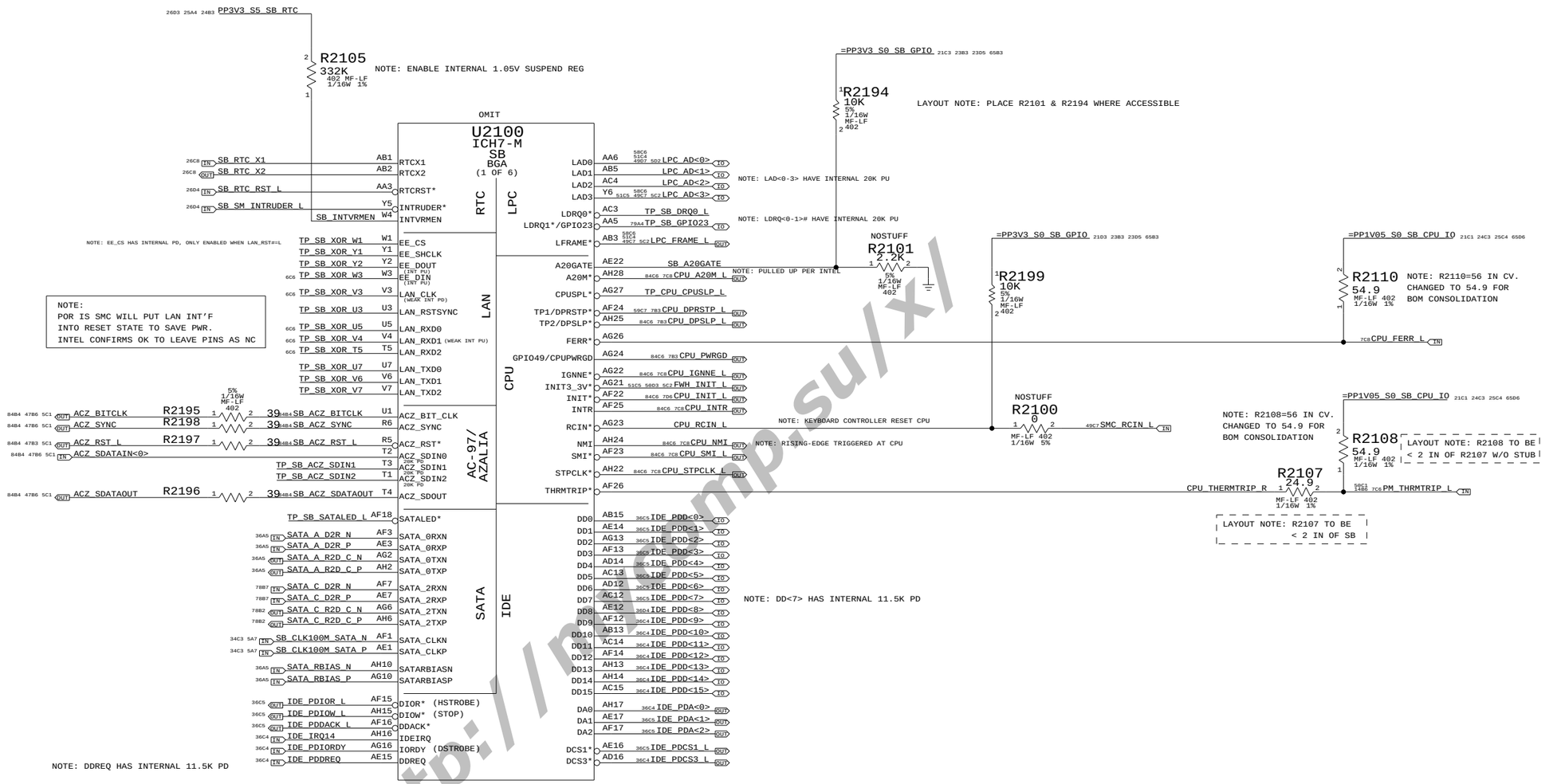
PROBABLY NOT NEEDED

NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 20 OF 84	



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#		NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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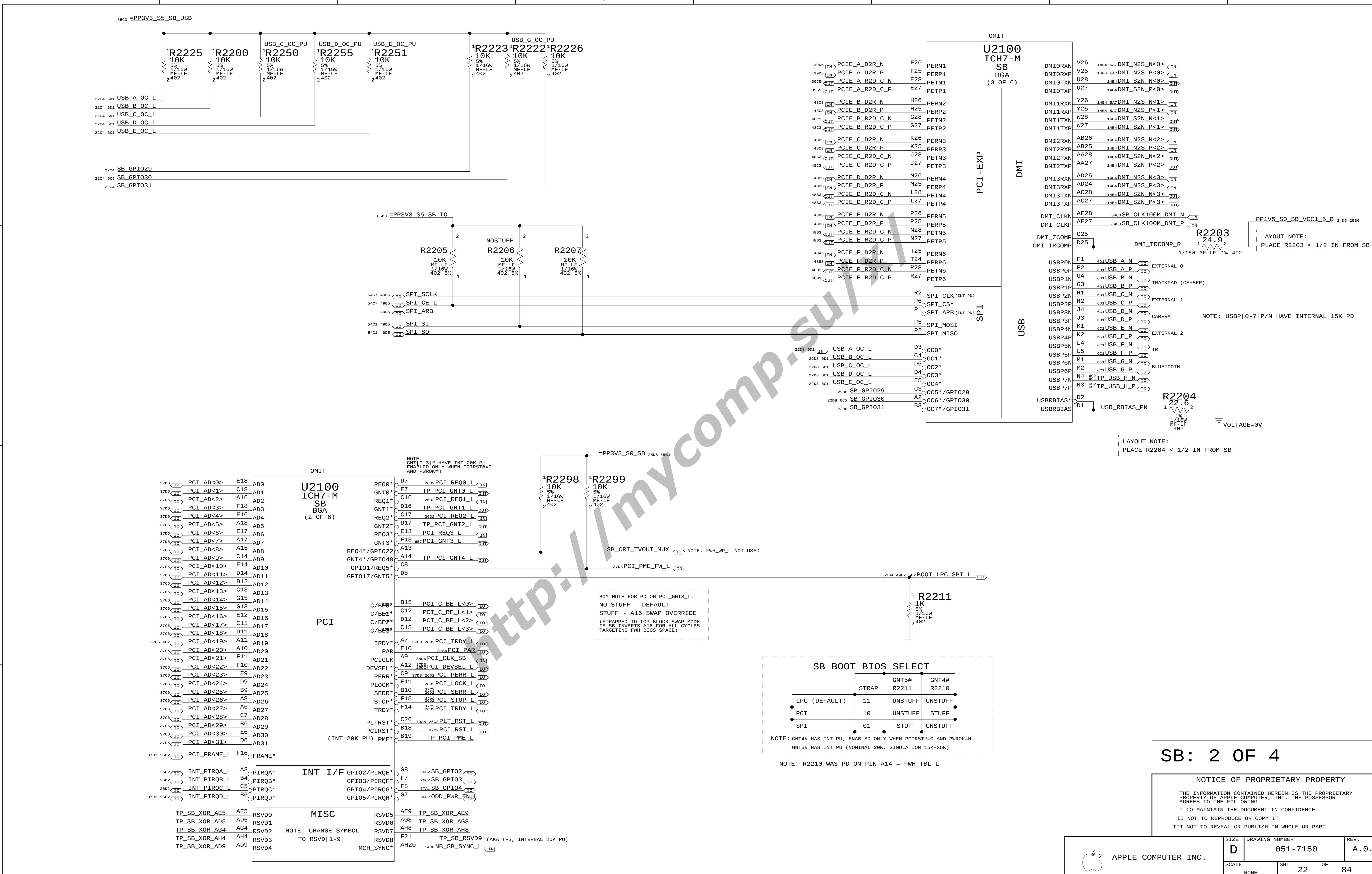
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 21 OF 84	



SB BOOT BIOS SELECT

	STRAP	GNT5# R2211	GNT4# R2210
LPC (DEFAULT)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L

SB: 2 OF 4

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SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE NONE	SHT 22 OF 84	

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21C3 21D3 23B3 65B3

=PP3V3_S5_SB 23A7 23B7 23D8 25C8 65D3

65D3 25C8 23D4 23B7 23A7 =PP3V3_S5_SB

R2398 1K 1/16W 402 MF-LF 5%
R2320 10K 1/16W 402 MF-LF 5%
R2317 10K 1/16W 402 MF-LF 5%
R2316 10K 1/16W 402 MF-LF 5%

R2318 10K 1/16W 402 MF-LF 5%
R2395 8.2K 1/16W 402 MF-LF 5%
R2396 10K 1/16W 402 MF-LF 5%
R2397 8.2K 1/16W 402 MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2323 NO_REBOOT_MODE 1K 1/16W 402 MF-LF 5%

RP2300 10K 5% 1/16W SM-LF

OMIT

U2100
ICH7-M
SB
BGA
(4 OF 6)

SMB

27D8 TO SMB_CLK → C22 SMBCLK
27D8 TO SMB_DATA → B22 SMBDATA
SMB_LINK_ALERT_L → A26 LINKALERT*
SMLINK<0> → B25 SMLINK0
SMLINK<1> → A25 SMLINK1
NOT USED
PM_RI_L → A28 RI*
SB_SPKR → A19 SPKR (INT WEAK PD)
58C6 51B5 50A2 49C5 5C2 OUT PM_SUS_STAT_L → A27 SUS_STAT*
49B7 26C5 58Z IN PM_SYSRST_L → A22 SYS_RST*
14B6 IN PM_BMBUSY_L → AB18 GPIO0/BM_BUSY*
SMB_ALERT_L → B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
33C4 OUT PM_STPPCI_L → AC20 GPIO18/STPPCI*
33C4 OUT PM_STPCPU_L → AF21 GPIO20/STPCPU*
SB_GPIO26 → A21 GPIO26
23A6 BIOS_REC → B21 GPIO27
23A6 FWH_MFG_MODE → E23 GPIO28
58C6 51C4 49C5 5C2 TO PM_CLKRUN_L → AG18 GPIO32/CLKRUN*
26A4 TP_GPU_D3COLD_RST_L → AC19 GPIO33/AZ_DOCK_EN*
TP_AZ_DOCK_RST_L → U2 GPIO34/AZ_DOCK_RST*
47C3 39C6 58I IN PCIE_WAKE_L → F20 WAKE*
58C6 51C5 49C7 5C2 TO INT_SERIRQ → AH21 SERIRQ
49B7 IN PM_THRM_L → AF20 THRM*
26B8 IN VR_PWRGD_CK410 → AD22 VRMPWRGD
TO TP_SB_GPIO6 → AC21 GPIO6
49B7 IN SMC_RUNTIME_SCI_L → AC18 GPIO7
49B7 IN SMC_EXTSMI_L → E21 GPIO8

SYS GPIO
PWR MNGT

SATA GPIO
GPIO21/SATA0GP AF19 SB_GPIO21 100 R2302
GPIO19/SATA1GP AH18 SB_GPIO19 100 R2303
GPIO36/SATA2GP AH19
GPIO37/SATA3GP AE19 SB_GPIO37 100 R2305
36B5 SATA_C_DET_L IN

CLKS
CLK14 AC1 34A6 SB_CLK14P3M_TIMER IN
CLK48 B2 34C7 SB_CLK48M_USBCTLR IN
SUSCLK C20 6C6 SUS_CLK_SB OUT

SLP_S3* B24 64C8 49C5 43B7 42A8 PM_SLP_S3_L OUT
SLP_S4* D23 49C5 64B8 41B6 PM_SLP_S4_L OUT
SLP_S5* F22 50A2 49C5 PM_SLP_S5_L OUT
PWROK AA4 26A6 PM_SB_PWROK IN
GPIO16/DPRSLPVR AC22 59C8 64C9 14B7 PM_DPRSLPVR OUT
TP0/BATLOW* C21 NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
(INT 20K PU) PWRBTN* C23 49D7 PM_PWRBTN_L IN
LAN_RST* C19 49D7 PM_LAN_ENABLE IN NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* Y4

GPIO9 E20 5DB2 49B5 SMS_INT_L IN
GPIO10 A20 49D7 SMC_SB_NMI IN
DEF=GPI GPIO12 F19 48A3 LAN_ENERGY_DET IN
GPIO13 E19
DEF=GPI GPIO14 R4 36D5 IDE_RESET_L OUT
GPIO15 E22 SV_SET_UP 5C2 23B6 51B5
GPIO24 R3 CRB_SV_DET 23B6
GPIO25 D20 TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 AD21 33B4 SB_CLK100M_SATA_OE_L OUT
GPIO38 AD20 TP_SB_GPIO38 TO
DEF=GPI GPIO39 AE20 23A3 SATA_C_PWR_EN_L OUT

GPIO

=PP3V3_S5_SB_PM 11B5 26C5 65D3
R2319 10K 1/16W 402 MF-LF 5%
R2343 8.2K 5% 1/16W 402 MF-LF

49D7 PM_BATLOW_L IN
49D7 PM_RSMRST_L IN
R2399 100K 5% 1/16W 402 MF-LF
49D5 SMC_WAKE_SCI_L IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

65D3 25C8 23D8 23D4 23A7 =PP3V3_S5_SB

R2306 NOSTUFF 10K 1/16W 402 MF-LF 5%
R2308 10K 1/16W 402 MF-LF 5%
R2307 10K 1/16W 402 MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 MF-LF 5%

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

SV_SET_UP 5C2 23C3 51B5
CRB_SV_DET 23C3

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

=PP3V3_S0_SB_GPIO 21C3 21D3 23D5 65B3
R2388 10K 5% 1/16W MF-LF 402
23B3 SATA_C_PWR_EN_L

65D3 25C8 23D8 23D4 23B7 =PP3V3_S5_SB

R2313 10K 1/16W 402 MF-LF 5%
R2310 10K 1/16W 402 MF-LF 5%
R2314 NOSTUFF 0 1/16W 402 MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 MF-LF 5%

FWH_MFG_MODE 23C5
BIOS_REC 23C5

SB: 3 OF 4

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

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D	051-7150	A.0.0

SCALE NONE SHT 23 OF 84

OMIT

U2100
ICH7-M
SB
BGA
(6 OF 6)

VSS

A4 A23 N24 P24 R18 U14 V27 AA24 AB27 AD11 B1 D10 F4 G18 J1 L24 M17 N14 N17 N18 N25 N26 P3 P4 P12 P13 P14 P15 P16 P17 P27 P28 R1 R11 R12 R13 R14 R15 R16 R17 T6 T12 T13 T14 T15 T16 T17 U4 U12 U13 U15 U16 U17 U24 U25 U26 V2 V13 V15 V24 V28 W6 W24 W25 W26 Y3 Y24 Y27 Y28 AA1 AA25 AA26 AB4 AB6 AB11 AB14 AB16 AB19 AB21 AB24 AB28 AC2 AC5 AC9 AC11 AD1 AE24 AE25 AF2 AF4 AF8 AF11 AF27 AF28 AG1 AG3 AG7

AD3 AD4 AD7 AD8 AD15 AD19 AD23 AE2 AE4 AE8 AE11 AE13 AE18 AE21 B8 B11 B14 B17 B20 B26 B28 C2 C6 C27 D13 D18 D21 D24 E1 E2 E4 E8 E15 F3 F5 F12 F27 F28 G1 G2 G5 G6 G9 G14 G21 G24 G25 G26 H3 H4 H5 H24 H27 H28 J2 J5 J24 J25 J26 K24 K27 K28 L13 L15 L25 L26 M3 M4 M5 M12 M13 M14 M15 M16 M24 M27 M28 N1 N2 N5 N6 N11 N12 N13 N15 N16 AG11 AG14 AG17 AG20 AG25 AH1 AH3 AH7 AH12 AH23 AH27

0 0

OMIT

U2100
ICH7-M
SB
BGA
(5 OF 6)

25D7 PP5V_S0_SB_V5REF — G10, AD17 — V5REF
25C7 PP5V_S5_SB_V5REF_SUS — F6 — V5REF_SUS
25B6 22C1 PP1V5_S0_SB_VCC1_5_B — AA22

VCCA3GP (VCC1_5_B): AA23 AB22 AB23 AC23 AC24 AC25 AC26 AD26 AD27 AD28 D26 D27 D28 E24 E25 E26 F23 F24 G22 G23 H22 H23 J22 J23 K22 K23 L22 L23 M22 M23 N22 N23 P22 P23 R22 R23 R24 R25 R26 T22 T23 T26 T27 T28 U22 U23 V22 V23 W22 W23 Y22 Y23

65B3 25C6 25B8 24B5 =PP3V3_S0_SB_VCC3_3 — B27 — VCC3_3
25A5 PP1V5_S0_SB_VCCDMIPLL — AG28 — VCCDMIPLL

ARX (VCC1_5_A)
65C6 25D6 =PP1V5_S0_SB_VCC1_5_A_ARX — AB7, AC6, AC7, AD6, AE6, AF5, AF6, AG5, AH5

65C6 25D6 =PP1V5_S0_SB_VCCSATAPLL — AD2 — VCCSATAPLL
65B3 25C6 25B8 24B5 =PP3V3_S0_SB_VCC3_3 — AH11 — VCC3_3

ATX (VCC1_5_A)
65C6 25C6 =PP1V5_S0_SB_VCC1_5_A_ATX — AB10, AB9, AC10, AD10, AE10, AF10, AF9, AG9, AH9

65C3 25D2 25B6 24B3 =PP3V3_S5_SB_VCCSUS3_3 — E3 — VCCSUS3_3
65C6 25B6 =PP1V5_S0_SB_VCCUSBPLL — C1 — VCCUSBPLL

VOLTAGE GENERATED INTERNALLY
SO NO CONNECT HERE
AA2, Y7 — VCCLAN1_5 — CHANGE SYMBOL TO 1.05

CORE (VCC1_05): L11 L12 L14 L16 L17 L18 M11 M18 P11 P18 T11 T18 U11 U18 V11 V12 V14 V16 V17 V18 — =PPVCORE_S0_SB 25D3 65D6

NOTE FOR VCCLAN_3_3:
S3 IF INTERNAL LAN IS USED
S0 OR S3 IF NOT

VCC_PAUX (VCCLAN_3_3): V5, V1, W2, W7 — =PP3V3_S0_SB_VCCLAN3_3 25D3 65B3

VCC3_3/VCCHDA: U6 — =PP3V3_S0_SB_3V3_1V5_VCCHDA 25C4 65B3
VCCSUS3_3/VCCSUSHDA: R7 — =PP3V3_S5_SB_3V3_1V5_VCCSUSHDA 65D3

NOTE:
VCCHDA AND VCCSUSHDA CAN BE 1.5V OR 3.3V
DEPENDING ON VIO OF AZALIA INTERFACE
CODEC IC'S CONSIDERED SO FAR ARE 3.3V

V_CPU_IO: AE23, AE26, AH26 — =PP1V05_S0_SB_CPU_IO 21C1 25C4 65D6

IDE (VCC3_3): AA7, AB12, AB20, AC16, AD13, AD18, AG12, AG15, AG19 — =PP3V3_S0_SB_VCC3_3_IDE 25B4 65B3

PCI (VCC3_3): A5, B13, B16, B7, C10, D15, F9, G11, G12, G16 — =PP3V3_S0_SB_VCC3_3_PCI 25A4 65B3

VCCRTC: W5 — PP3V3_S5_SB_RTC 21D6 25A4 26D3

VCCSUS3_3: P7, A24, C24, D19, D22, G19 — =PP3V3_S5_SB_VCCSUS3_3 24A5 25B6 25D2 65C3

USB (VCCSUS3_3): K3, K4, K5, K6, L1, L2, L3, L6, L7, M6, M7, N7 — =PP3V3_S5_SB_VCCSUS3_3_USB 25D2 65C3

VCC1_5_A: AB17, AC17, T7, F17, G17, AB8, AC8 — =PP1V5_S0_SB_VCC1_5_A 25C2 65C6

VCCSAUS1_5 (CHANGE SYMBOL TO 1.05): K7, C28, G20 — VOLTAGE GENERATED INTERNALLY, SO NO CONNECT HERE

USB CORE (VCC1_5_A): A1, H6, H7, J6, J7 — =PP1V5_S0_SB_VCC1_5_A_USB_CORE 25B2 65C6

SB: 4 OF 4

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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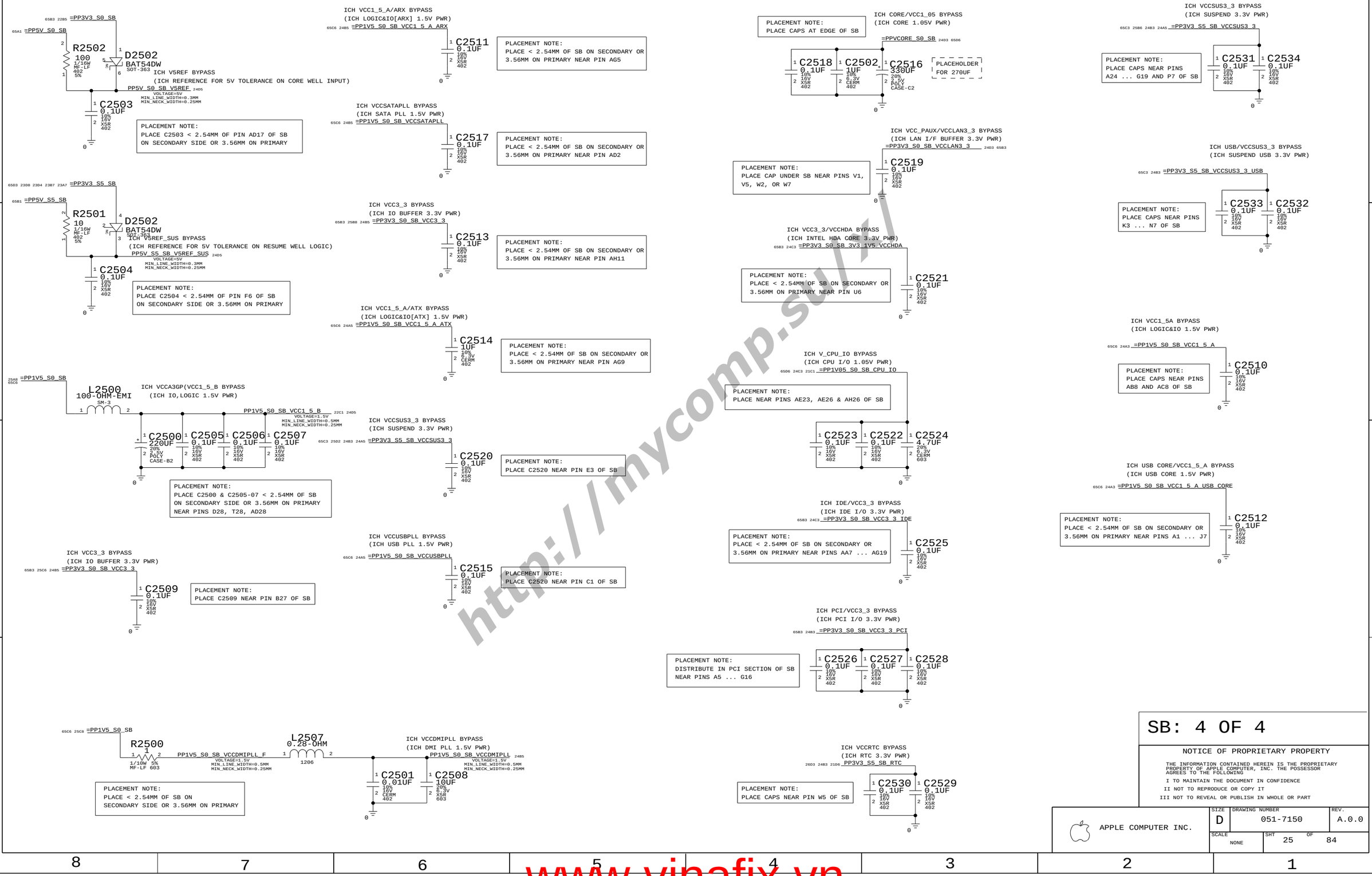
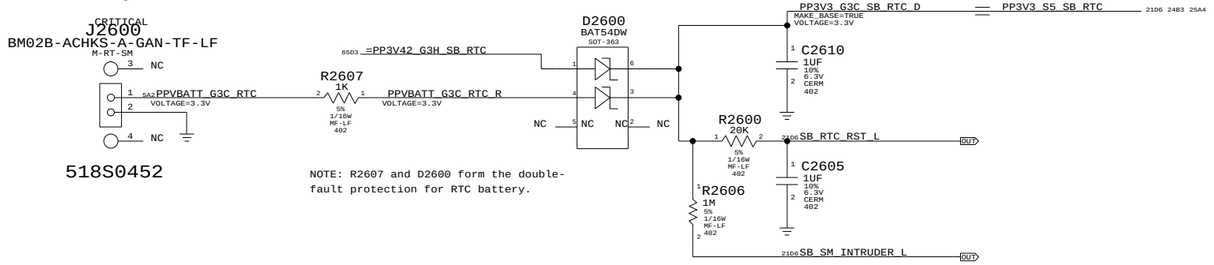
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

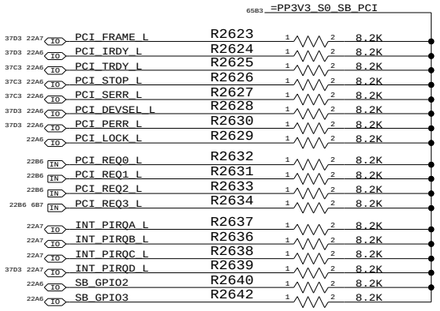
SCALE: NONE — SHT 24 OF 84



RTC Battery Connector

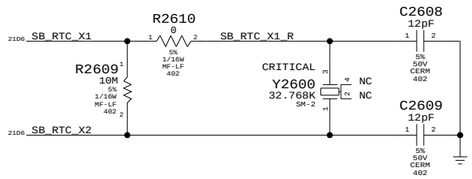


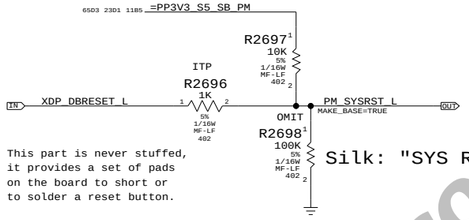
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



Pullup on SB_GPIO4 removed as it now defaults low for use as DVI_HPD in muxed graphics solution.

SB RTC Crystal Circuit

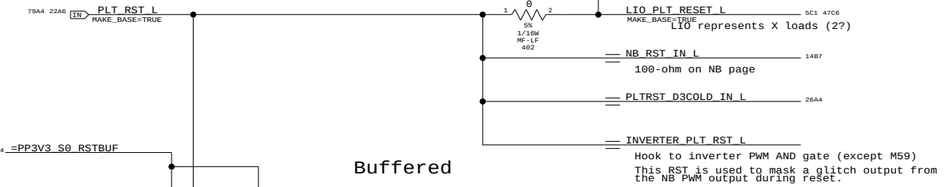




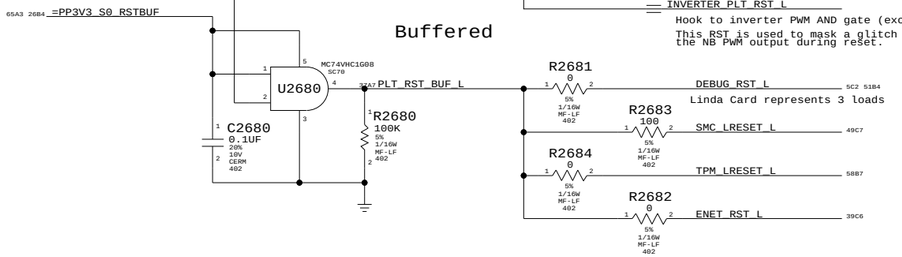
This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

Platform Reset Connections

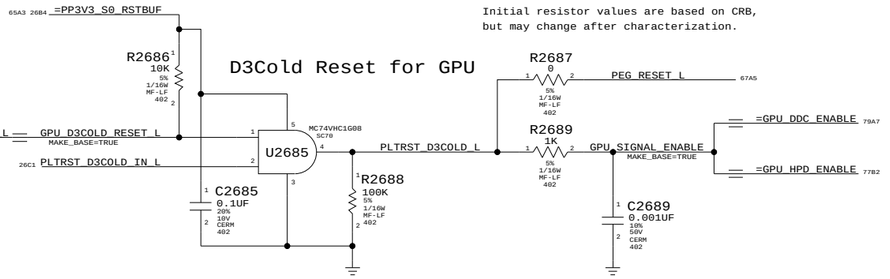
Unbuffered

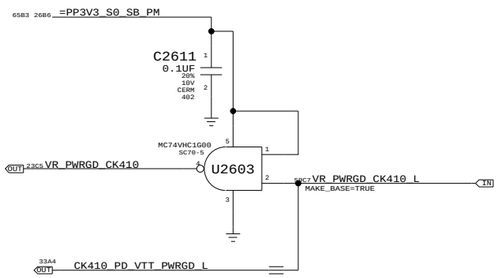


Buffered

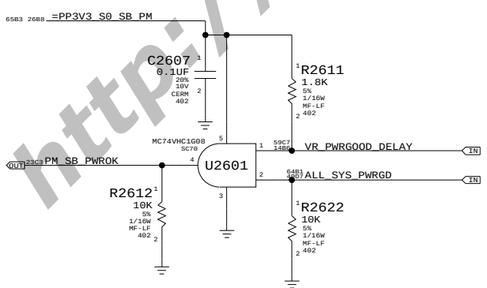


Initial resistor values are based on CRB, but may change after characterization.





1G00 used as small & cheap inverter



SB Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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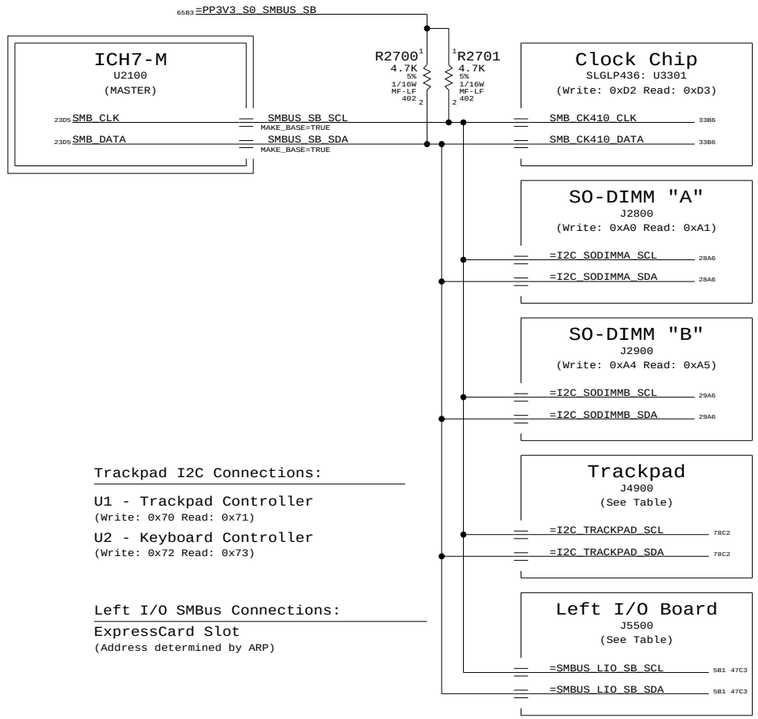
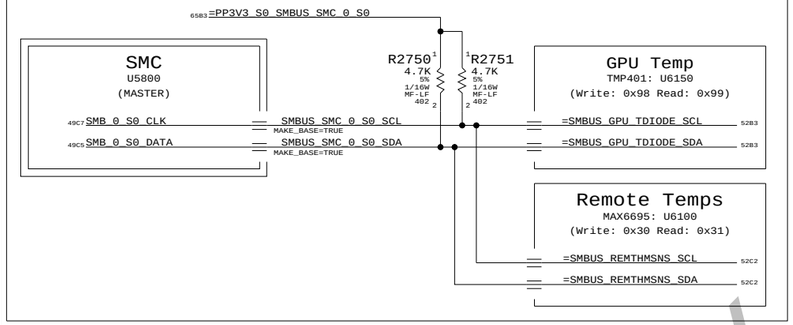
SIZE	DRAWING NUMBER	REV.
D	051-7164	A.0.0
SCALE: NONE	SHT 26 OF 84	

ICH7-M SMBus Connections

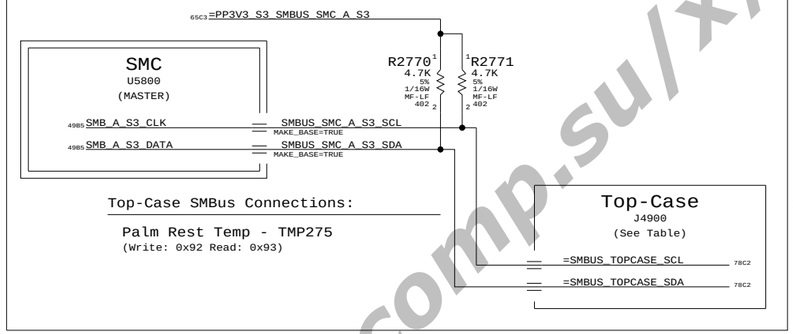


SMC "0" SMBus Connections

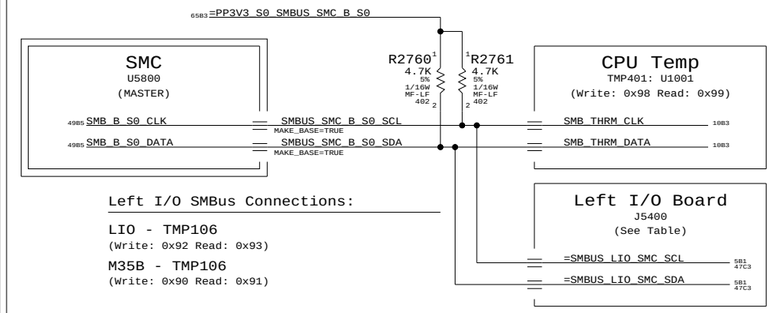


SMC "A" SMBus Connections

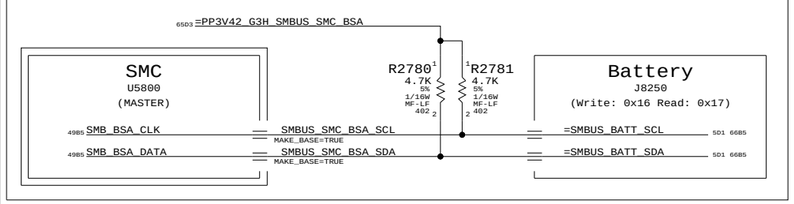
NOTE: SMC RMT bus remains powered and may be active in S3 state



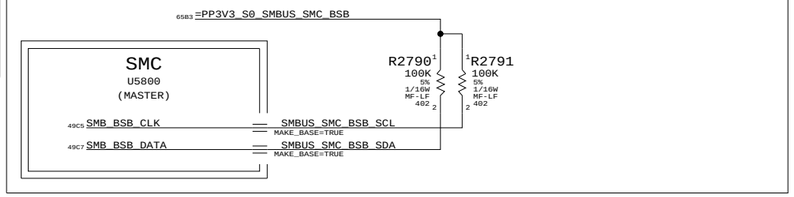
SMC "B" SMBus Connections



SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 27 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.

"Expansion" (surface-mount) slot

65B6 29D6 29D3 29B2 28D3 28B2 =PP1V8_S3_MEM

32B3 29D6 MEM_VREF

C2801 2.2uF 20% 6.3V CERM1 603

C2800 0.1uF 20% 10V CERM 402

CRITICAL
J2800
F-RT-SM-M9
DDR2-SODIMM-DUAL

203 NC
201 NC

		1A	VREF			2A	VSS0		
		3A	VSS1			4A	DQ4	15C7	MEM_A_DQ<8>
15C7	MEM_A_DQ<14>	5A	DQ0			6A	DQ5	15C7	MEM_A_DQ<12>
15C7	MEM_A_DQ<13>	7A	DQ1			8A	VSS2		
		9A	VSS4			10A	DM0	15D5	MEM_A_DM<1>
15C5	MEM_A_DQS_N<1>	11A	DQS0*			12A	VSS5		
15C5	MEM_A_DQS_P<1>	13A	DQS0			14A	DQ6	15C7	MEM_A_DQ<15>
		15A	VSS6			16A	DQ7	15C7	MEM_A_DQ<9>
15C7	MEM_A_DQ<10>	17A	DQ2			18A	VSS7		
15C7	MEM_A_DQ<11>	19A	DQ3			20A	DQ12	15D7	MEM_A_DQ<2>
		21A	VSS8			22A	DQ13	15D7	MEM_A_DQ<3>
15D7	MEM_A_DQ<5>	23A	DQ8			24A	VSS9		
15D7	MEM_A_DQ<4>	25A	DQ9			26A	DM1	15D5	MEM_A_DM<0>
		27A	VSS10			28A	VSS11		
15C5	MEM_A_DQS_N<0>	29A	DQS1*			30A	CK0	14D4	MEM_CLK_P<0>
15C5	MEM_A_DQS_P<0>	31A	DQS1			32A	CK0*	14D4	MEM_CLK_N<0>
		33A	VSS12			34A	VSS13		
15D7	MEM_A_DQ<6>	35A	DQ10			36A	DQ14	15D7	MEM_A_DQ<1>
15D7	MEM_A_DQ<7>	37A	DQ11			38A	DQ15	15D7	MEM_A_DQ<0>
		39A	VSS14			40A	VSS15		
				KEY					
		41A	VSS16			42A	VSS17		
15C7	MEM_A_DQ<19>	43A	DQ16			44A	DQ20	15C7	MEM_A_DQ<23>
15C7	MEM_A_DQ<18>	45A	DQ17			46A	DQ21	15C7	MEM_A_DQ<22>
		47A	VSS18			48A	VSS19		
15C5	MEM_A_DQS_N<2>	49A	DQS2*			50A	NC0	29C3 50D3	DIMM_OVERTEMP_L
15C5	MEM_A_DQS_P<2>	51A	DQS2			52A	DM2	15D5	MEM_A_DM<2>
		53A	VSS21			54A	VSS22		
15C7	MEM_A_DQ<20>	55A	DQ18			56A	DQ22	15C7	MEM_A_DQ<21>
15C7	MEM_A_DQ<16>	57A	DQ19			58A	DQ23	15C7	MEM_A_DQ<17>
		59A	VSS23			60A	VSS24		
15C7	MEM_A_DQ<28>	61A	DQ24			62A	DQ28	15C7	MEM_A_DQ<29>
15C7	MEM_A_DQ<25>	63A	DQ25			64A	DQ29	15C7	MEM_A_DQ<24>
		65A	VSS25			66A	VSS26		
15C5	MEM_A_DM<3>	67A	DM3			68A	DQS3*	15C5	MEM_A_DQS_N<3>
NC		69A	NC1			70A	DQS3	15C5	MEM_A_DQS_P<3>
		71A	VSS27			72A	VSS28		
15C7	MEM_A_DQ<27>	73A	DQ26			74A	DQ30	15C7	MEM_A_DQ<26>
15C7	MEM_A_DQ<30>	75A	DQ27			76A	DQ31	15C7	MEM_A_DQ<31>
		77A	VSS29			78A	VSS30		
30D6 14C4	MEM_CKE<0>	79A	CKE0			80A	NC/CKE1	14C4 30D6	MEM_CKE<1>
		81A	VDD0			82A	VDD1		
NC		83A	NC2			84A	NC/A15	6D6	MEM_A_A<15>
30B6 15D5	MEM_A_BS<2>	85A	BA2			86A	NC/A14	6D6	MEM_A_A<14>
		87A	VDD2			88A	VDD3		
30C6 15B5	MEM_A_A<12>	89A	A12			90A	A11	15B5 30C6	MEM_A_A<11>
30C6 15B5	MEM_A_A<9>	91A	A9			92A	A7	15B5 30C6	MEM_A_A<7>
30C6 15B5	MEM_A_A<8>	93A	A8			94A	A6	15B5 30C6	MEM_A_A<6>
		95A	VDD4			96A	VDD5		
30C6 15B5	MEM_A_A<5>	97A	A5			98A	A4	15B5 30C6	MEM_A_A<4>
30C6 15B5	MEM_A_A<3>	99A	A3			100A	A2	15C5 30C6	MEM_A_A<2>
30C6 15C5	MEM_A_A<1>	101A	A1			102A	A0	15C5 30C6	MEM_A_A<0>
		103A	VDD6			104A	VDD7		
30C6 15B5	MEM_A_A<10>	105A	A10/AP			106A	BA1	15D5 30B6	MEM_A_BS<1>
30B6 15D5	MEM_A_BS<0>	107A	BA0			108A	RAS*	15B5 30B6	MEM_A_RAS_L
30B6 15B5	MEM_A_WE_L	109A	WE*			110A	S0*	14C4 30D6	MEM_CS_L<0>
		111A	VDD8			112A	VDD9		
30B6 15D5	MEM_A_CAS_L	113A	CAS*			114A	ODT0	14C4 30C6	MEM_ODT<0>
30D6 14C4	MEM_CS_L<1>	115A	NC/S1*			116A	NC/A13	15B5 30C6	MEM_A_A<13>
		117A	VDD10			118A	VDD11		
30C6 14C4	MEM_ODT<1>	119A	NC/ODT1			120A	NC3	NC	
		121A	VSS31			122A	VSS32		
15B7	MEM_A_DQ<35>	123A	DQ32			124A	DQ36	15B7	MEM_A_DQ<38>
15B7	MEM_A_DQ<39>	125A	DQ33			126A	DQ37	15B7	MEM_A_DQ<34>
		127A	VSS33			128A	VSS34		
15C5	MEM_A_DQS_N<4>	129A	DQS4*			130A	DM4	15C5	MEM_A_DM<4>
15C5	MEM_A_DQS_P<4>	131A	DQS4			132A	VSS35		
		133A	VSS36			134A	DQ38	15C7	MEM_A_DQ<32>
15B7	MEM_A_DQ<37>	135A	DQ34			136A	DQ39	15B7	MEM_A_DQ<36>
15C7	MEM_A_DQ<33>	137A	DQ35			138A	VSS37		
		139A	VSS38			140A	DQ44	15B7	MEM_A_DQ<57>
15A7	MEM_A_DQ<60>	141A	DQ40			142A	DQ45	15A7	MEM_A_DQ<63>
15B7	MEM_A_DQ<59>	143A	DQ41			144A	VSS39		
		145A	VSS40			146A	DQS5*	15C5	MEM_A_DQS_N<7>
15C5	MEM_A_DM<7>	147A	DM5			148A	DQS5	15C5	MEM_A_DQS_P<7>
		149A	VSS41			150A	VSS42		
15B7	MEM_A_DQ<58>	151A	DQ42			152A	DQ46	15B7	MEM_A_DQ<56>
15A7	MEM_A_DQ<61>	153A	DQ43			154A	DQ47	15A7	MEM_A_DQ<62>
		155A	VSS43			156A	VSS44		
15B7	MEM_A_DQ<43>	157A	DQ48			158A	DQ52	15B7	MEM_A_DQ<40>
15B7	MEM_A_DQ<45>	159A	DQ49			160A	DQ53	15B7	MEM_A_DQ<42>
		161A	VSS45			162A	VSS46		
NC		163A	NC_TEST			164A	CK1	14D4	MEM_CLK_P<1>
		165A	VSS47			166A	CK1*	14D4	MEM_CLK_N<1>
15C5	MEM_A_DQS_N<5>	167A	DQS6*			168A	VSS48		
15C5	MEM_A_DQS_P<5>	169A	DQS6			170A	DM6	15C5	MEM_A_DM<5>
		171A	VSS49			172A	VSS50		
15B7	MEM_A_DQ<41>	173A	DQ50			174A	DQ54	15B7	MEM_A_DQ<47>
15B7	MEM_A_DQ<46>	175A	DQ51			176A	DQ55	15B7	MEM_A_DQ<44>
		177A	VSS51			178A	VSS52		
15B7	MEM_A_DQ<51>	179A	DQ56			180A	DQ60	15B7	MEM_A_DQ<54>
15B7	MEM_A_DQ<50>	181A	DQ57			182A	DQ61	15B7	MEM_A_DQ<55>
		183A	VSS53			184A	VSS54		
15C5	MEM_A_DM<6>	185A	DM7			186A	DQS7*	15C5	MEM_A_DQS_N<6>
		187A	VSS55			188A	DQS7	15C5	MEM_A_DQS_P<6>
15B7	MEM_A_DQ<53>	189A	DQ58			190A	VSS56		
15B7	MEM_A_DQ<48>	191A	DQ59			192A	DQ62	15B7	MEM_A_DQ<52>
		193A	VSS57			194A	DQ63	15B7	MEM_A_DQ<49>
65A3 29A6 29A3	=PPSPD_S0_MEM					196A	VSS58		
27D6	=I2C_SODIMMA_SDA	195A	SDA			198A	SA0		
27D6	=I2C_SODIMMA_SCL	197A	SCL			200A	SA1		ADDR=0xA0(WR)/0xA1(RD)
		199A	VDDSPD						

202 NC
204 NC

516S0471

DDR2 Bypass Caps

(For return current)

65B6 29D6 29D3 29B2 28D6 28D3 =PP1V8_S3_MEM

C2808 10UF 20% 6.3V X5R 603
C2809 10UF 20% 6.3V X5R 603
C2810 1UF 10% 6.3V CERM 402
C2811 1UF 10% 6.3V CERM 402
C2812 1UF 10% 6.3V CERM 402
C2813 1UF 10% 6.3V CERM 402
C2814 1UF 10% 6.3V CERM 402
C2815 1UF 10% 6.3V CERM 402
C2816 1UF 10% 6.3V CERM 402
C2817 1UF 10% 6.3V CERM 402
C2818 1UF 10% 6.3V CERM 402
C2819 1UF 10% 6.3V CERM 402
C2820 1UF 10% 6.3V CERM 402
C2821 1UF 10% 6.3V CERM 402

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 28 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.

"Factory" (thru-hole) slot

65B6 29D3 29B2 28D6 28D3 28B2 =PP1V8_S3_MEM

32B3 28D6 MEM_VREF

C2901 2.2uF 20% 6.3V CERM1 603

C2900 0.1uF 20% 10V CERM 402

DDR2-SODIMM-DUAL

CRITICAL
J2900
F-RT-TH1

		1B	VREF			201	NC		
		3B	VSS1			2B	VSS0		
15C4	MEM_B_DQ<15>	5B	DQ0			4B	DQ4	MEM_B_DQ<9>	15C4
15C4	MEM_B_DQ<14>	7B	DQ1			6B	DQ5	MEM_B_DQ<11>	15C4
		9B	VSS4			8B	VSS2		
15C2	MEM_B_DQS_N<1>	11B	DQS0*			10B	DM0	MEM_B_DM<1>	15D2
15C2	MEM_B_DQS_P<1>	13B	DQS0			12B	VSS5		
		15B	VSS6			14B	DQ6	MEM_B_DQ<12>	15C4
15C4	MEM_B_DQ<10>	17B	DQ2			16B	DQ7	MEM_B_DQ<8>	15C4
15C4	MEM_B_DQ<13>	19B	DQ3			18B	VSS7		
		21B	VSS8			20B	DQ12	MEM_B_DQ<3>	15D4
15D4	MEM_B_DQ<7>	23B	DQ8			22B	DQ13	MEM_B_DQ<6>	15D4
15D4	MEM_B_DQ<2>	25B	DQ9			24B	VSS9		
		27B	VSS10			26B	DM1	MEM_B_DM<0>	15D2
15C2	MEM_B_DQS_N<0>	29B	DQS1*			28B	VSS11		
15C2	MEM_B_DQS_P<0>	31B	DQS1			30B	CK0	MEM_CLK_P<3>	14D4
		33B	VSS12			32B	CK0*	MEM_CLK_N<3>	14D4
15D4	MEM_B_DQ<1>	35B	DQ10			34B	VSS13		
15D4	MEM_B_DQ<4>	37B	DQ11			36B	DQ14	MEM_B_DQ<0>	15D4
		39B	VSS14			38B	DQ15	MEM_B_DQ<5>	15D4
			KEY			40B	VSS15		
		41B	VSS16			42B	VSS17		
15C4	MEM_B_DQ<21>	43B	DQ16			44B	DQ20	MEM_B_DQ<22>	15C4
15C4	MEM_B_DQ<19>	45B	DQ17			46B	DQ21	MEM_B_DQ<18>	15C4
		47B	VSS18			48B	VSS19		
15C2	MEM_B_DQS_N<2>	49B	DQS2*			50B	NC0	DIMM_OVERTEMP_L	29C3 50D3
15C2	MEM_B_DQS_P<2>	51B	DQS2			52B	DM2	MEM_B_DM<2>	15D2
		53B	VSS21			54B	VSS22		
15C4	MEM_B_DQ<20>	55B	DQ18			56B	DQ22	MEM_B_DQ<17>	15C4
15C4	MEM_B_DQ<23>	57B	DQ19			58B	DQ23	MEM_B_DQ<16>	15C4
		59B	VSS23			60B	VSS24		
15C4	MEM_B_DQ<29>	61B	DQ24			62B	DQ28	MEM_B_DQ<26>	15C4
15C4	MEM_B_DQ<24>	63B	DQ25			64B	DQ29	MEM_B_DQ<28>	15C4
		65B	VSS25			66B	VSS26		
15C2	MEM_B_DM<3>	67B	DM3			68B	DQS3*	MEM_B_DQS_N<3>	15C2
	NC	69B	NC1			70B	DQS3	MEM_B_DQS_P<3>	15C2
		71B	VSS27			72B	VSS28		
15C4	MEM_B_DQ<27>	73B	DQ26			74B	DQ30	MEM_B_DQ<31>	15C4
15C4	MEM_B_DQ<25>	75B	DQ27			76B	DQ31	MEM_B_DQ<30>	15C4
		77B	VSS29			78B	VSS30		
30D6 14C4	MEM_CKE<2>	79B	CKE0			80B	NC/CKE1	MEM_CKE<3>	14C4 30D6
		81B	VDD0			82B	VDD1		
	NC	83B	NC2			84B	NC/A15	MEM_B_A<15>	6D6
30A6 15D2	MEM_B_BS<2>	85B	BA2			86B	NC/A14	MEM_B_A<14>	6D6
		87B	VDD2			88B	VDD3		
30B6 15B2	MEM_B_A<12>	89B	A12			90B	A11	MEM_B_A<11>	15B2 30B6
30B6 15B2	MEM_B_A<9>	91B	A9			92B	A7	MEM_B_A<7>	15B2 30B6
30B6 15B2	MEM_B_A<8>	93B	A8			94B	A6	MEM_B_A<6>	15B2 30B6
		95B	VDD4			96B	VDD5		
30B6 15B2	MEM_B_A<5>	97B	A5			98B	A4	MEM_B_A<4>	15B2 30B6
30B6 15B2	MEM_B_A<3>	99B	A3			100B	A2	MEM_B_A<2>	15C2 30B6
30B6 15C2	MEM_B_A<1>	101B	A1			102B	A0	MEM_B_A<0>	15C2 30B6
		103B	VDD6			104B	VDD7		
30B6 15B2	MEM_B_A<10>	105B	A10/AP			106B	BA1	MEM_B_BS<1>	15D2 30A6
30A6 15D2	MEM_B_BS<0>	107B	BA0			108B	RAS*	MEM_B_RAS_L	15B2 30A6
30A6 15B2	MEM_B_WE_L	109B	WE*			110B	S0*	MEM_CS_L<2>	14C4 30D6
		111B	VDD8			112B	VDD9		
30A6 15D2	MEM_B_CAS_L	113B	CAS*			114B	ODT0	MEM_ODT<2>	14C4 30C6
30D6 14C4	MEM_CS_L<3>	115B	NC/S1*			116B	NC/A13	MEM_B_A<13>	15B2 30B6
		117B	VDD10			118B	VDD11		
30C6 14C4	MEM_ODT<3>	119B	NC/ODT1			120B	NC3	NC	
		121B	VSS31			122B	VSS32		
15B4	MEM_B_DQ<36>	123B	DQ32			124B	DQ36	MEM_B_DQ<32>	15C4
15C4	MEM_B_DQ<33>	125B	DQ33			126B	DQ37	MEM_B_DQ<37>	15B4
		127B	VSS33			128B	VSS34		
15C2	MEM_B_DQS_N<4>	129B	DQS4*			130B	DM4	MEM_B_DM<4>	15C2
15C2	MEM_B_DQS_P<4>	131B	DQS4			132B	VSS35		
		133B	VSS36			134B	DQ38	MEM_B_DQ<38>	15B4
15B4	MEM_B_DQ<34>	135B	DQ34			136B	DQ39	MEM_B_DQ<39>	15B4
15B4	MEM_B_DQ<35>	137B	DQ35			138B	VSS37		
		139B	VSS38			140B	DQ44	MEM_B_DQ<44>	15B4
15B4	MEM_B_DQ<40>	141B	DQ40			142B	DQ45	MEM_B_DQ<45>	15B4
15B4	MEM_B_DQ<41>	143B	DQ41			144B	VSS39		
		145B	VSS40			146B	DQS5*	MEM_B_DQS_N<5>	15C2
15C3	MEM_B_DM<5>	147B	DM5			148B	DQS5	MEM_B_DQS_P<5>	15C2
		149B	VSS41			150B	VSS42		
15B4	MEM_B_DQ<42>	151B	DQ42			152B	DQ46	MEM_B_DQ<46>	15B4
15B4	MEM_B_DQ<43>	153B	DQ43			154B	DQ47	MEM_B_DQ<47>	15B4
		155B	VSS43			156B	VSS44		
15A4	MEM_B_DQ<62>	157B	DQ48			158B	DQ52	MEM_B_DQ<58>	15B4
15B4	MEM_B_DQ<59>	159B	DQ49			160B	DQ53	MEM_B_DQ<63>	15A4
		161B	VSS45			162B	VSS46		
	NC	163B	NC_TEST			164B	CK1	MEM_CLK_P<2>	14D4
		165B	VSS47			166B	CK1*	MEM_CLK_N<2>	14D4
15C2	MEM_B_DQS_N<7>	167B	DQS6*			168B	VSS48		
15C2	MEM_B_DQS_P<7>	169B	DQS6			170B	DM6	MEM_B_DM<7>	15C2
		171B	VSS49			172B	VSS50		
15A4	MEM_B_DQ<60>	173B	DQ50			174B	DQ54	MEM_B_DQ<56>	15B4
15A4	MEM_B_DQ<61>	175B	DQ51			176B	DQ55	MEM_B_DQ<57>	15B4
		177B	VSS51			178B	VSS52		
15B4	MEM_B_DQ<54>	179B	DQ56			180B	DQ60	MEM_B_DQ<55>	15B4
15B4	MEM_B_DQ<51>	181B	DQ57			182B	DQ61	MEM_B_DQ<50>	15B4
		183B	VSS53			184B	VSS54		
15C2	MEM_B_DM<6>	185B	DM7			186B	DQS7*	MEM_B_DQS_N<6>	15C2
		187B	VSS55			188B	DQS7	MEM_B_DQS_P<6>	15C2
15B4	MEM_B_DQ<52>	189B	DQ58			190B	VSS56		
15B4	MEM_B_DQ<49>	191B	DQ59			192B	DQ62	MEM_B_DQ<53>	15B4
65A3 29A3 28A6	=PPSPD_S0_MEM	193B	VSS57			194B	DQ63	MEM_B_DQ<48>	15B4
27C6	=I2C_SODIMMB_SDA	195B	SDA			196B	VSS58	Resistor prevents pwr-gnd short	
27C6	=I2C_SODIMMB_SCL	197B	SCL			198B	SA0		
		199B	VDDSPD			200B	SA1	SODIMM_A_SA1	
			516-0140			202	NC	ADDR=0xA4(WR)/0xA5(RD)	

=PP1V8_S3_MEM 28B2 28D3 28D6 29B2 29D6 65B6

65A3 29A6 28A6 =PPSPD_S0_MEM

R2900 10K 5% 1/16W MF-LF 402

DDR2 Bypass Caps

(For return current)

65B6 29D6 29D3 28D6 28D3 28B2 =PP1V8_S3_MEM

C2908 10UF 20% 5.3V XSR 603

C2909 10UF 20% 6.3V XSR 603

C2910 1UF 10% 6.3V CERM 402

C2911 0.1uF 20% 10V CERM 402

C2912 1UF 10% 6.3V CERM 402

C2913 1UF 10% 6.3V CERM 402

C2914 1UF 10% 6.3V CERM 402

C2915 1UF 10% 6.3V CERM 402

C2916 1UF 10% 6.3V CERM 402

C2917 0.1uF 20% 10V CERM 402

C2918 0.1uF 20% 10V CERM 402

C2919 0.1uF 20% 10V CERM 402

C2920 0.1uF 20% 10V CERM 402

C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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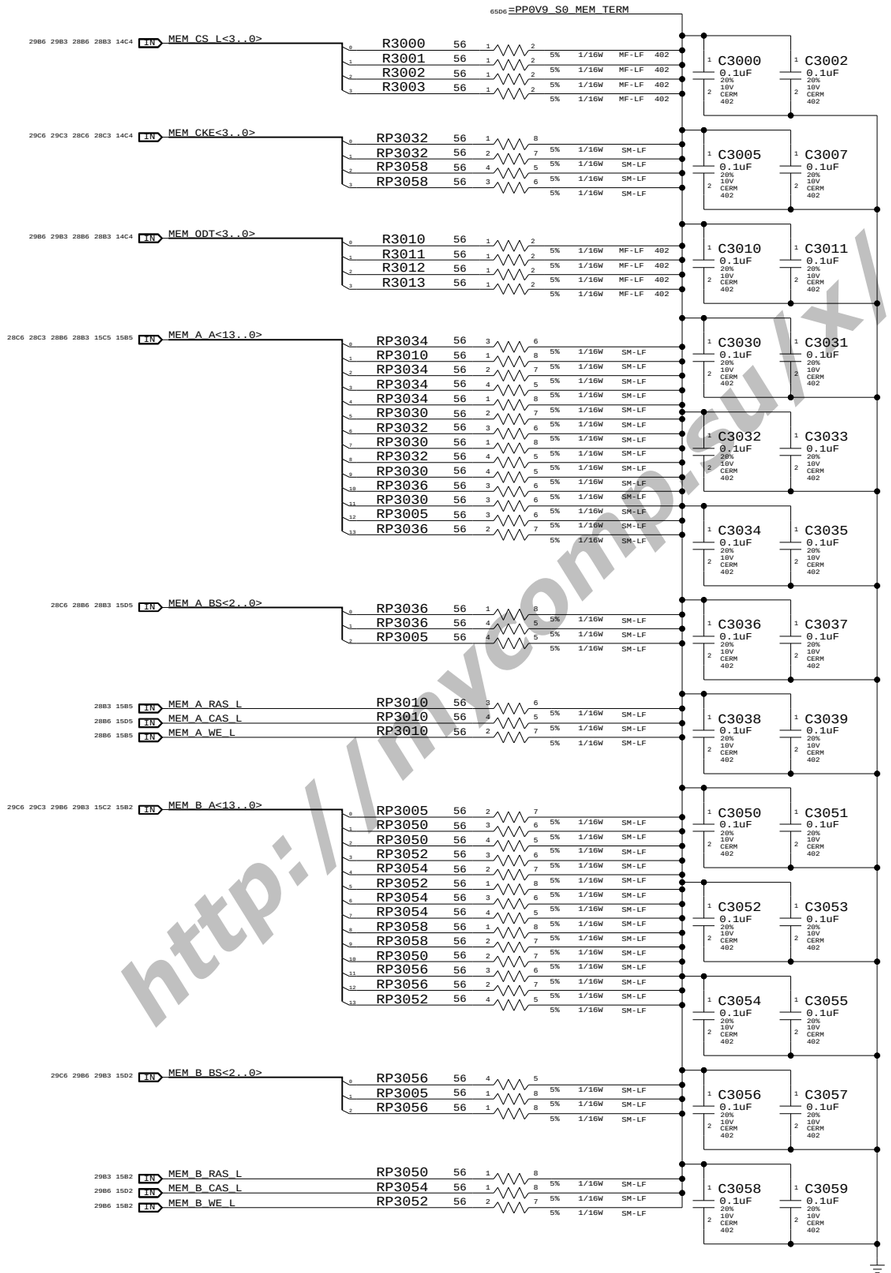
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 29 OF 84	

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 30 OF 84	

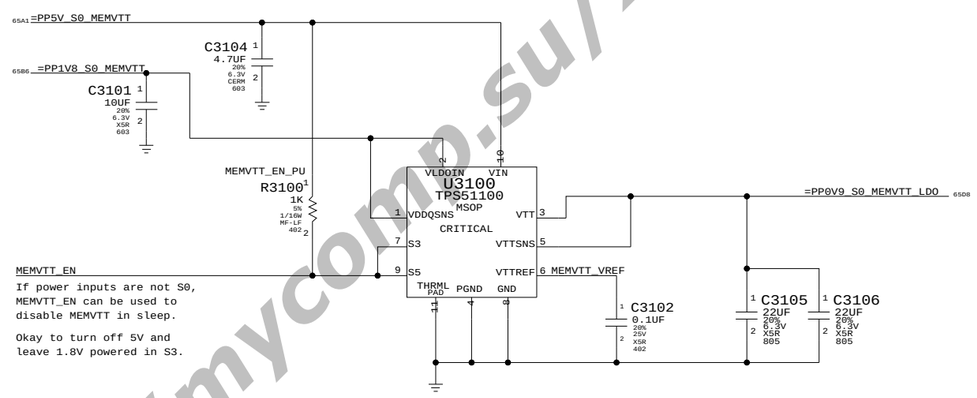
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



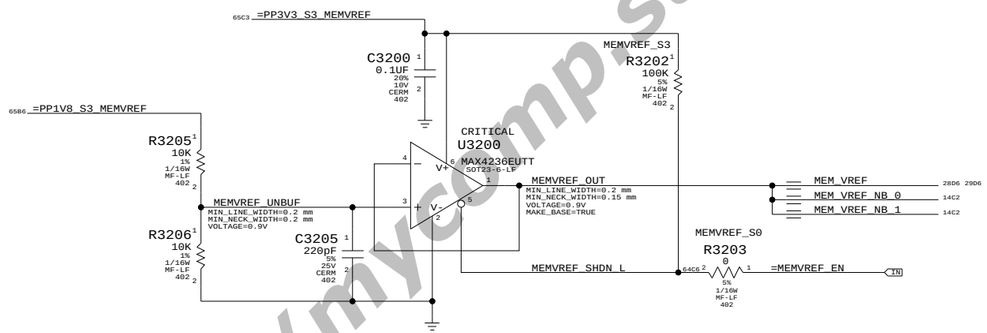
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	31	84

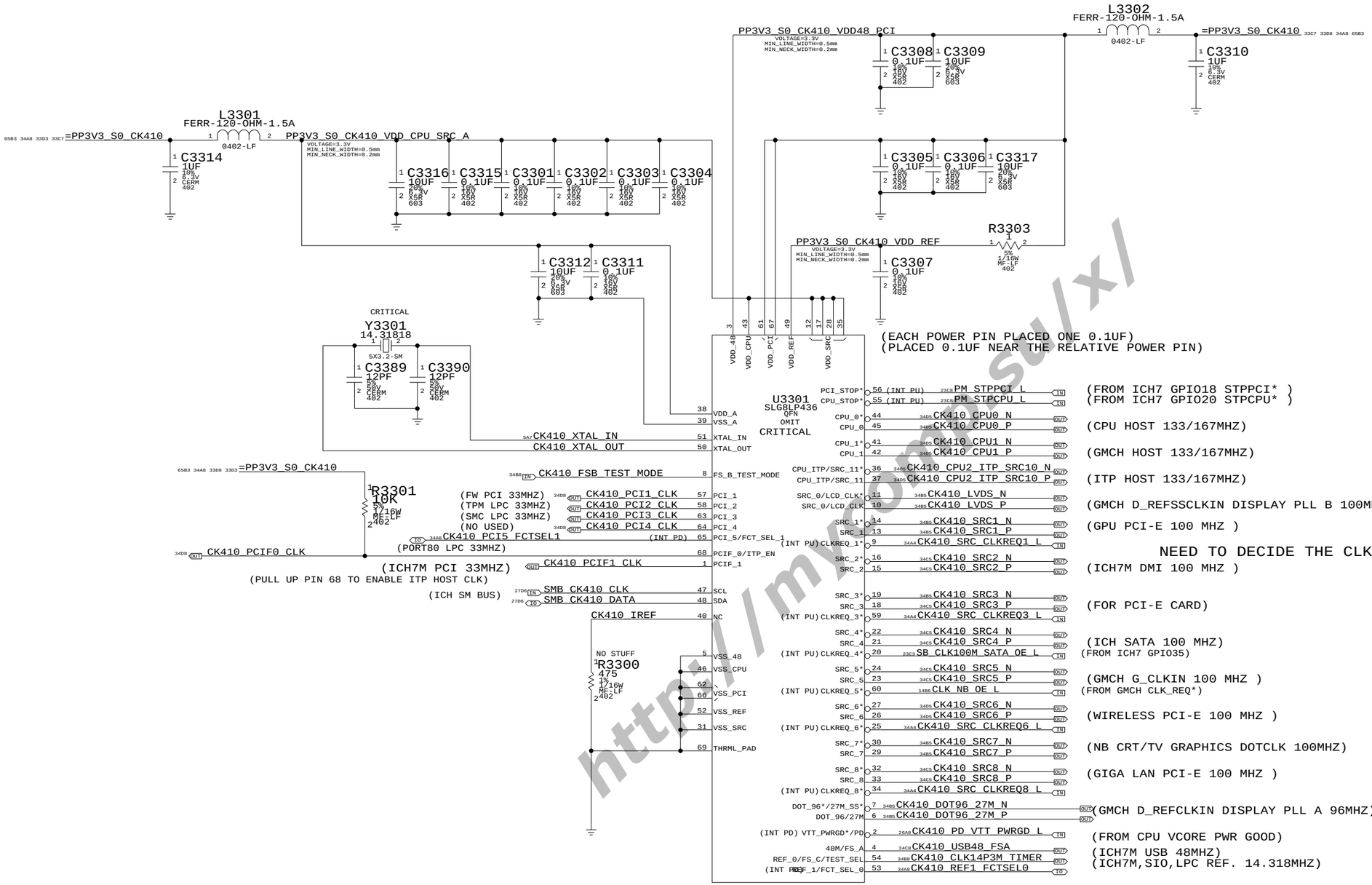


DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 32 OF 84	



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 33 OF 84

R3463 33 5% 1/16W MF-LF 402
CK410_PCIF0_CLK → PCI_CLK_PORT80_LPC → (PORT80 LPC 33MHZ)

R3432 33 5% 1/16W MF-LF 402
CK410_PCIF1_CLK → PCI_CLK_SB → (TO ICH7M PCI 33MHZ)

R3429 33 5% 1/16W MF-LF 402
CK410_PCI1_CLK → PCI_CLK_FW → (TO FIREWIRE PCI 33MHZ)

TPM
R3430 33 5% 1/16W MF-LF 402
CK410_PCI2_CLK → PCI_CLK_TPM → (TO TPM PCI 33MHZ)

R3433 33 5% 1/16W MF-LF 402
CK410_PCI3_CLK → PCI_CLK_SMC → (TO SMC PCI 33MHZ)

CK410_PCI4_CLK → TP_CK410_PCI4_CLK MAKE_BASE=TRUE

PLACEMENT of these caps should be close as possible to the resistors

NOSTUFF C3400 15PF 5% 50V CERM 402
NOSTUFF C3401 15PF 5% 50V CERM 402
NOSTUFF C3402 15PF 5% 50V CERM 402
NOSTUFF C3403 15PF 5% 50V CERM 402
NOSTUFF C3404 15PF 5% 50V CERM 402

R3417 33 5% 1/16W MF-LF 402
CK410_USB48_FSA → SB_CLK48M_USBCTLR → (TO ICH7M USB 48MHZ)

=PP1V05_S0_FSB_NB

NOSTUFF R3480 1K 5% 1/16W MF-LF 402

R3468 1K 5% 1/16W MF-LF 402
NB_BSEL<0> → (TO MCH FS_A)

R3401 2.2K 5% 1/10W MF-LF 402
CPU_BSEL_R<0>

R3450 0 5% 1/16W MF-LF 402
CPU_BSEL<0> → (FROM CPU FS_A)

R3469 1K 5% 1/16W MF-LF 402

=PP1V05_S0_FSB_NB

R3470 1K 5% 1/16W MF-LF 402

NEED TO CHECK THE BSEL PULLS

R3471 1K 5% 1/16W MF-LF 402
CK410_FSB_TEST_MODE

R3472 1K 5% 1/16W MF-LF 402
NB_BSEL<1> → (TO MCH FS_B)

CPU_BSEL_R<1>

R3451 0 5% 1/16W MF-LF 402
CPU_BSEL<1> → (FROM CPU FS_B)

NOSTUFF R3452 1K 5% 1/16W MF-LF 402

=PP1V05_S0_FSB_NB

R3473 1K 5% 1/16W MF-LF 402

R3474 1K 5% 1/16W MF-LF 402
CK410_CLK14P3M_TIMER

R3475 1K 5% 1/16W MF-LF 402
NB_BSEL<2> → (TO MCH FS_C)

CPU_BSEL_R<2>

R3453 0 5% 1/16W MF-LF 402
CPU_BSEL<2> → (FROM CPU FS_C)

NOSTUFF R3454 1K 5% 1/16W MF-LF 402

R3476 33 5% 1/16W MF-LF 402
SB_CLK14P3M_TIMER → (ICH7M 14.318MHZ)

=PP3V3_S0_CK410

R3467 10K 5% 1/16W MF-LF 402
CK410_PCI5_FCTSEL1

R3466 10K 5% 1/16W MF-LF 402
CK410_REF1_FCTSEL0

NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED

CK410_CPU0_P → FSB_CLK_CPU_P MAKE_BASE=TRUE
CK410_CPU0_N → FSB_CLK_CPU_N MAKE_BASE=TRUE
(CPU HOST 133/167MHZ)

CK410_CPU1_P → FSB_CLK_NB_P MAKE_BASE=TRUE
CK410_CPU1_N → FSB_CLK_NB_N MAKE_BASE=TRUE
(GMCH HOST 133/167MHZ)

CK410_CPU2_ITP_SRC10_P → CPU_XDP_CLK_P MAKE_BASE=TRUE
CK410_CPU2_ITP_SRC10_N → CPU_XDP_CLK_N MAKE_BASE=TRUE
(ITP HOST 133/167MHZ)

CK410_SRC6_P → PCIE_CLK100M_MINI_P MAKE_BASE=TRUE
CK410_SRC6_N → PCIE_CLK100M_MINI_N MAKE_BASE=TRUE
(WIRELESS PCI-E MINI 100MHZ)

CK410_SRC5_P → NB_CLK100M_GCLKIN_P MAKE_BASE=TRUE
CK410_SRC5_N → NB_CLK100M_GCLKIN_N MAKE_BASE=TRUE
(GMCH G_CLKIN 100MHZ)

CK410_SRC2_P → SB_CLK100M_DMI_P MAKE_BASE=TRUE
CK410_SRC2_N → SB_CLK100M_DMI_N MAKE_BASE=TRUE
(ICH7M DMI 100MHZ)

CK410_SRC8_P → ENET_CLK100M_PCIE_P MAKE_BASE=TRUE
CK410_SRC8_N → ENET_CLK100M_PCIE_N MAKE_BASE=TRUE
(Yukon PCI-E 100MHZ)

CK410_SRC4_P → SB_CLK100M_SATA_P MAKE_BASE=TRUE
CK410_SRC4_N → SB_CLK100M_SATA_N MAKE_BASE=TRUE
(ICH7M SATA 100MHZ)

CK410_SRC3_P → PCIE_CLK100M_EXCARD_P MAKE_BASE=TRUE
CK410_SRC3_N → PCIE_CLK100M_EXCARD_N MAKE_BASE=TRUE
(ExpressCard Slot)

R3418 121 1% 1/16W MF-LF 402
CK410_DOT96_27M_P → GPU_CLK27M
CK410_27M_NONSPREAD MAKE_BASE=TRUE

R3419 56 5% 1/16W MF-LF 402
CK410_DOT96_27M_N → GPU_CLK27MSS_IN
CK410_27M_SPREAD MAKE_BASE=TRUE
(GPU 27MHz Spread / Non-Spread)

CK410_SRC1_P → PEG_CLK100M_GPU_P MAKE_BASE=TRUE
CK410_SRC1_N → PEG_CLK100M_GPU_N MAKE_BASE=TRUE
(GPU PCI-E Graphics 100MHz)

CK410_LVDS_P → NB_CLK_DREFSSCLKIN_P MAKE_BASE=TRUE
CK410_LVDS_N → NB_CLK_DREFSSCLKIN_N MAKE_BASE=TRUE
(NB LVDS GRAPHICS 100MHZ)

NO STUFF R3443 0 5% 1/16W MF-LF 402
CK410_SRC7_P → NB_CLK_DREFCLKIN_P

NO STUFF R3444 0 5% 1/16W MF-LF 402
CK410_SRC7_N → NB_CLK_DREFCLKIN_N
(NB CRT/TV GRAPHICS DOTCLK 100MHZ)

CK410_SRC_CLKREQ3_L → EXCARD_CLKREQ_L MAKE_BASE=TRUE
CK410_SRC_CLKREQ6_L → MINI_CLKREQ_L MAKE_BASE=TRUE

R3485 1K 5% 1/16W MF-LF 402
CK410_SRC_CLKREQ1_L
GPU CLK OE*

R3486 1K 5% 1/16W MF-LF 402
CK410_SRC_CLKREQ8_L
Yukon CLK OE*

GPU_CLK27M → R3405 71.5 1% 1/16W MF-LF 402
GPU_CLK27MSS_IN → NO STUFF R3402 71.5 1% 1/16W MF-LF 402

PP1V5_S0_NB_VCCA_DPLLA
NO STUFF R3426 100K 5% 1/16W MF-LF 402
NB_CLK_DREFCLKIN_P → R3424 0 5% 1/16W MF-LF 402
NB_CLK_DREFCLKIN_N → R3425 0 5% 1/16W MF-LF 402

Clock Termination

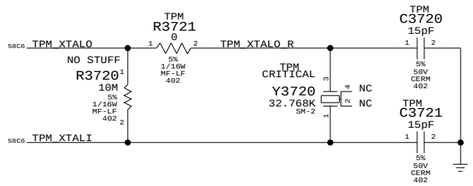
SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

APPLE COMPUTER INC.

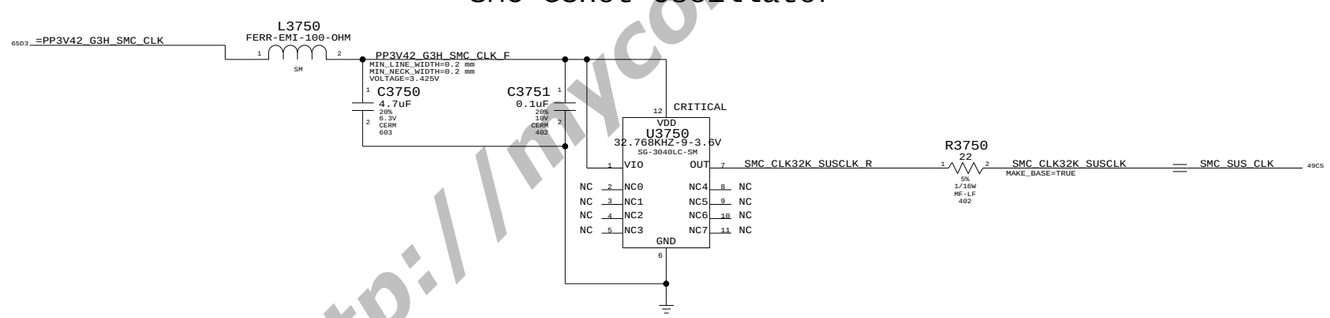
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 34 OF 84

TPM Crystal Circuit



SMC G3Hot Oscillator



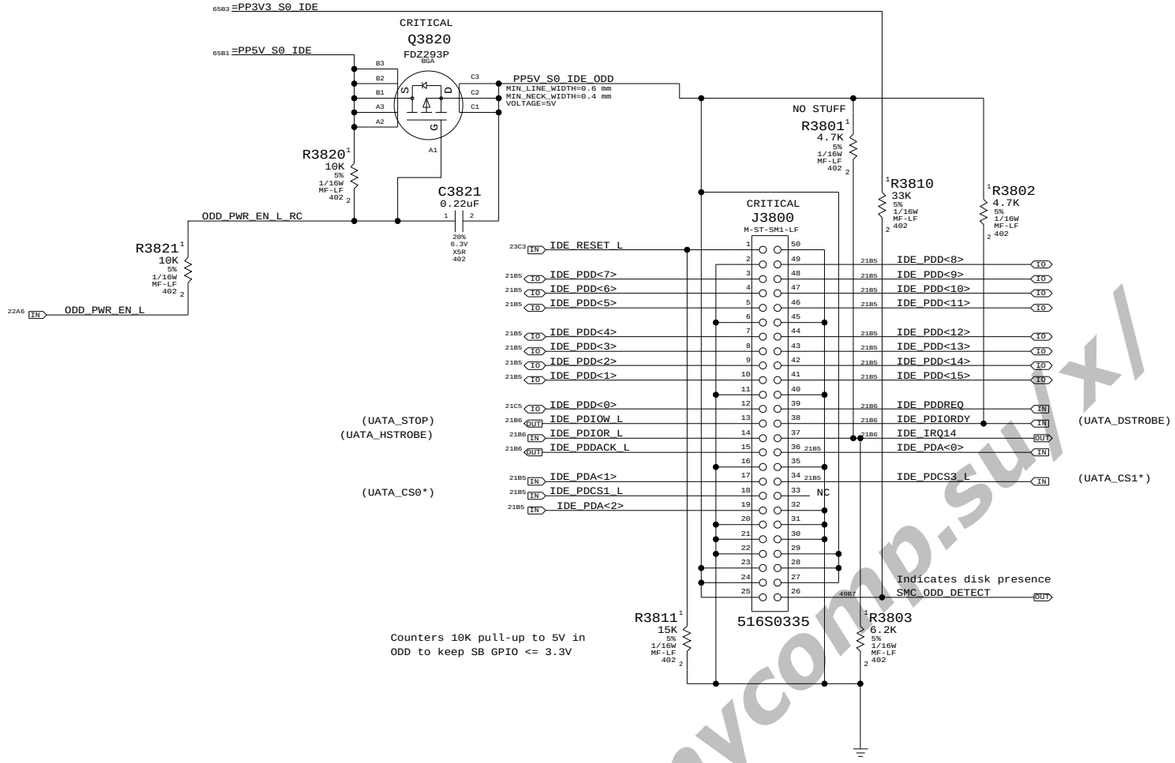
Mobile Clocking

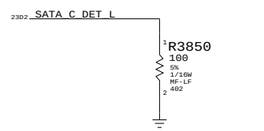
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

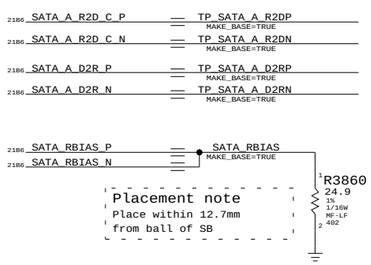
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 35 OF 84	

IDE (ODD) Connector







PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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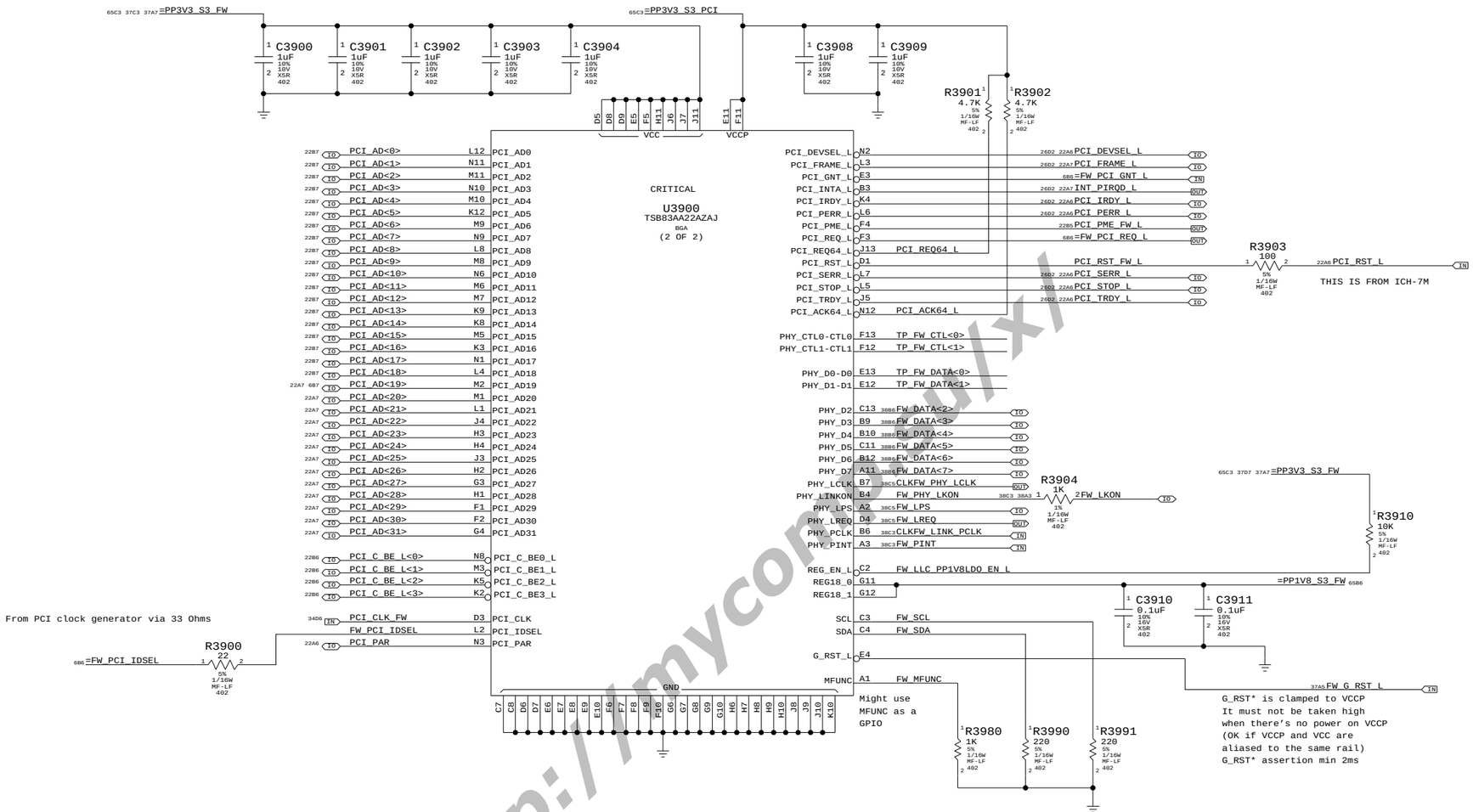
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 36 OF 84



FireWire Link (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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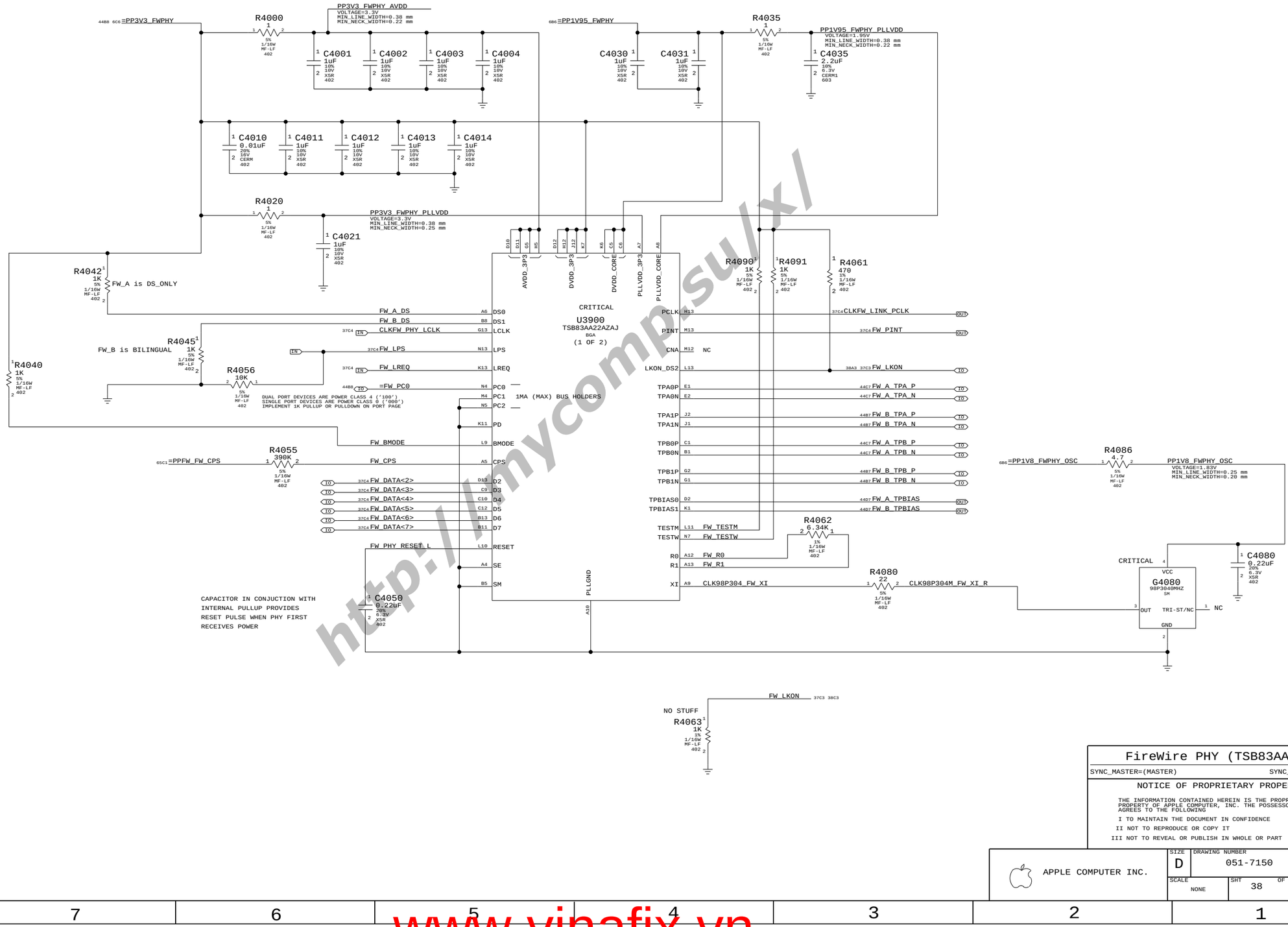
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	37	84



FireWire PHY (TSB83AA22)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	38	84

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.22MM
VOLTAGE=2.5V

L4100
FERR-120-OHM-1.5A
0402-LF

=PP2V5_S3_ENET 65B6

40D5 =PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

PLACE C4107 NEAR U4101 AVDD

39D5 39A1 39A3 39A4 39B8 65D1 =PP3V3_S3_ENET

=PP1V2_S3_ENET 39A8 65D6

=PP3V3_S3_ENET 39D8 65D1 39A5 39B4 39B5 39B8

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402

PCIE_A_D2R_C_P 1 2 22D4 PCIE_A_D2R_P OUT
PCIE_A_D2R_C_N 1 2 22D4 PCIE_A_D2R_N OUT

C4111 0.1UF 10% 16V X5R 402

C4112 0.1UF X5R 10% 16V 402

PCIE_A_R2D_P 1 2 22D4 PCIE_A_R2D_C_P IN
PCIE_A_R2D_N 1 2 22D4 PCIE_A_R2D_C_N IN

C4113 0.1UF 402 X5R 16V 10%

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

VDD7 58
VDD6 48
VDD5 44
VDD4 39
VDD3 33
VDD2 13
VDD1 7
VDD0 2
VDDQ_TTL4 61
VDDQ_TTL3 45
VDDQ_TTL2 40
VDDQ_TTL1 8
VDDQ_TTL0 1
AVDD 23
AVDDL6 57
AVDDL5 52
AVDDL4 51
AVDDL3 32
AVDDL2 28
AVDDL1 22
AVDDL0 19
VDD25 64

OMIT
CRITICAL
U4101
88E8053
QFN

ENET_LOM_DIS_L 39B7 → 10 LOM_DISABLE*
12 VAUX_AVLBL
=ENET_VMAIN_AVLBL 64C6 → 47 VMAIN_AVLBL
NC 11 SWITCH_VCC
NC 9 SWITCH_VAUX
NC 24 HSDACP
NC 25 HSDACN

ANALOG

OPTIONAL EXTERNAL LDO

ENET_CTRL25 6D4 OUT → 4 CTRL25
ENET_CTRL12 6D4 OUT → 3 CTRL12
ENET_RSET → 16 RSET

R4102 4.87K 1% 1/16W MF-LF 402

NO PULL-UP NEEDED

NC 59 LED_ACT*
NC 60 LED_LINK10/100*
NC 62 LED_LINK1000*
NC 63 LINK*

LED

29 TSTPT
46 TESTMODE

TEST

TX_P 49
TX_N 50
RX_P 54
RX_N 53

PCI EXPRESS

REFCLKP 55 ← 34C3 ENET_CLK100M_PCIE_P IN
REFCLKN 56 ← 34C3 ENET_CLK100M_PCIE_N IN
WAKE* 6 → 47C3 23C8 5B1 PCIE_WAKE_L OUT
PERST* 5 ← 26B1 ENET_RST_L IN

MDIP0 17
MDIN0 18
MDIP1 20
MDIN1 21
MDIP2 26
MDIN2 27
MDIP3 30
MDIN3 31

MEDIA

40D4 ENET_MDI_P<0> IO
40C4 40B7 ENET_MDI_N<0> IO
40C4 ENET_MDI_P<1> IO
40C4 40A7 ENET_MDI_N<1> IO
40C4 ENET_MDI_P<2> IO
40C4 ENET_MDI_N<2> IO
40C4 ENET_MDI_P<3> IO
40B4 ENET_MDI_N<3> IO

VPD_CLK 38 ← ENET_VPD_CLK 39A2
VPD_DATA 41 ↔ ENET_VPD_DATA 39A2

TWSI

PU_VDDO_TTL0 42 ← ENET_PU_VDD_TTL0 39A6
PU_VDDO_TTL1 43 ← ENET_PU_VDD_TTL1 39A6

TEST

ASF IS UNAVAILABLE ON 8053

SPI_DI 35 NC
SPI_DO 34 NC
SPI_CLK 37 NC
SPI_CS 36 NC

SPI

INTERNAL PULL-UP

XTALI 15
XTALO 14 → ENET_XTALO

MAIN CLK

CRITICAL
ENET_XTALI

Y4101 SM-3.2X2.5MM 25.0000M

C4150 27pF 5% 50V CERM 402
C4151 27pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

THRML_PAD 65

R4106 49.9 1% 1/16W MF-LF 402
R4105 49.9 1% 1/16W MF-LF 402
R4104 49.9 1% 1/16W MF-LF 402
R4103 49.9 1% 1/16W MF-LF 402
R4120 49.9 1% 1/16W MF-LF 402
R4119 49.9 1% 1/16W MF-LF 402
R4118 49.9 1% 1/16W MF-LF 402
R4117 49.9 1% 1/16W MF-LF 402

ENET_MDI0 VOLTAGE=1.234V
ENET_MDI1 VOLTAGE=1.234V
ENET_MDI2 VOLTAGE=1.234V
ENET_MDI3 VOLTAGE=1.234V

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

Setting attribute VOLTAGE to arbitrary value to help constraint manager find correct topology

PLACE RESISTORS CLOSE TO U4101

65D1 39D8 39D6 39B5 39A4 39A5 =PP3V3_S3_ENET

R4101 4.7K 5% 1/16W MF-LF 402

ENET_LOM_DIS_L 39C8

6C4 ENET_LOWPWR_EN

Q4100 2N7002 SOT23-LF

R4132 100K 5% 1/16W MF-LF 402

=PP3V3_S3_ENET 39A5 39B4 39B8 39D6 39D8 65D1

R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402

39C6 ENET_PU_VDD_TTL0
39B6 ENET_PU_VDD_TTL1

65D1 39D8 39D6 39B8 39B5 39A5 =PP3V3_S3_ENET

PLACE C4140 NEAR U4102 VCC

C4140 0.1UF 10% 16V X5R 402

OMIT
CRITICAL

U4102
M24C08
SO8

VCC 8
E2 3
NC1 2
NC0 1
WC* 7
SDA 5
SCL 6
VSS 4

R4122 10K 5% 1/16W MF-LF 402
R4123 10K 5% 1/16W MF-LF 402

ENET_VPD_DATA 39C6
ENET_VPD_CLK 39C6

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

65D6 39D7 =PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDQ_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

65D1 39D8 39D6 39B8 39B5 39A4 =PP3V3_S3_ENET

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 39 OF 84	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0> 40D3
	ENETCONN	ENET_100D	ENETCONN_N<0> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<1> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<2> 40C3
	ENETCONN	ENET_100D	ENETCONN_P<3> 40C3
	ENETCONN	ENET_100D	ENETCONN_N<3> 40B3

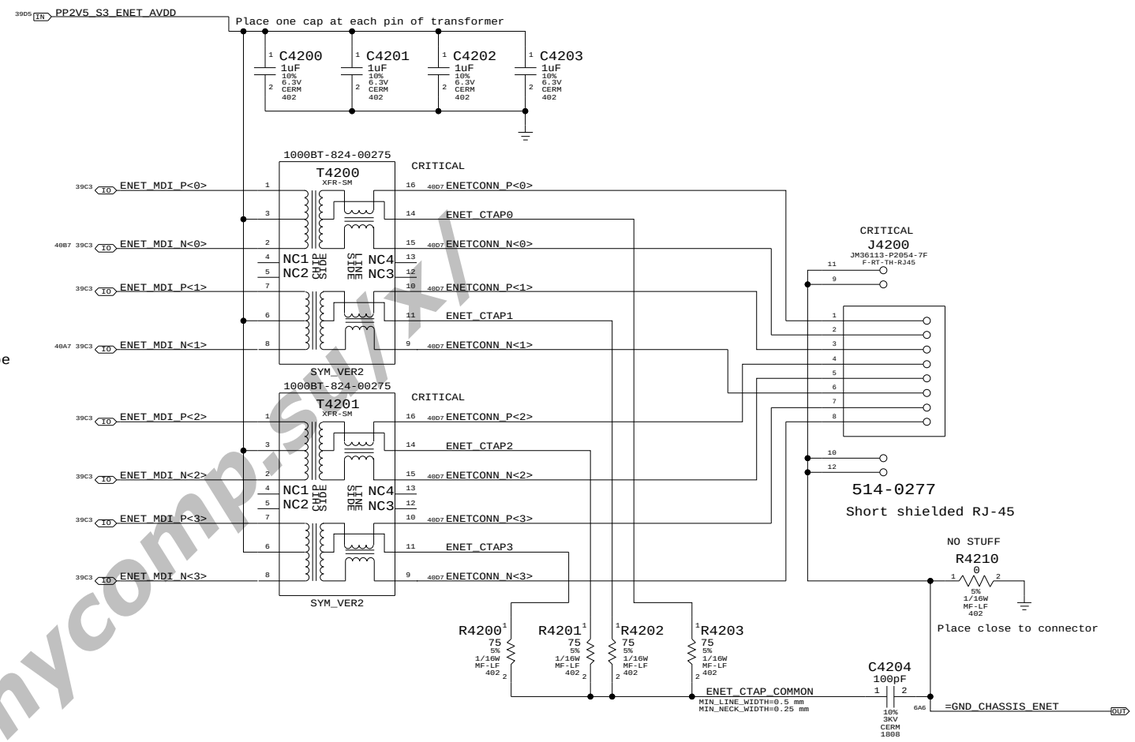
Page Notes

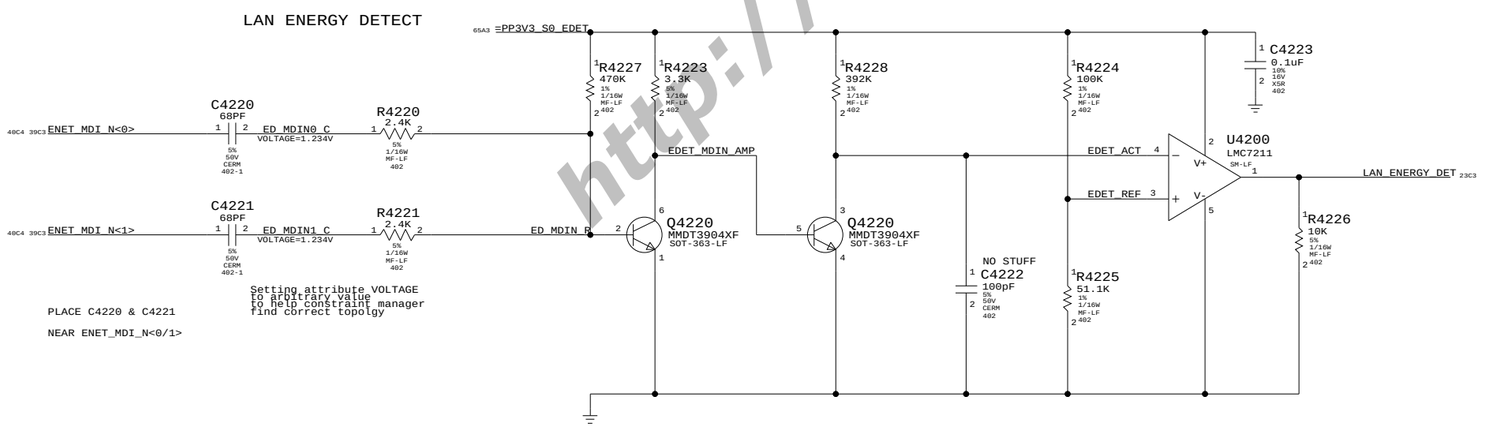
Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



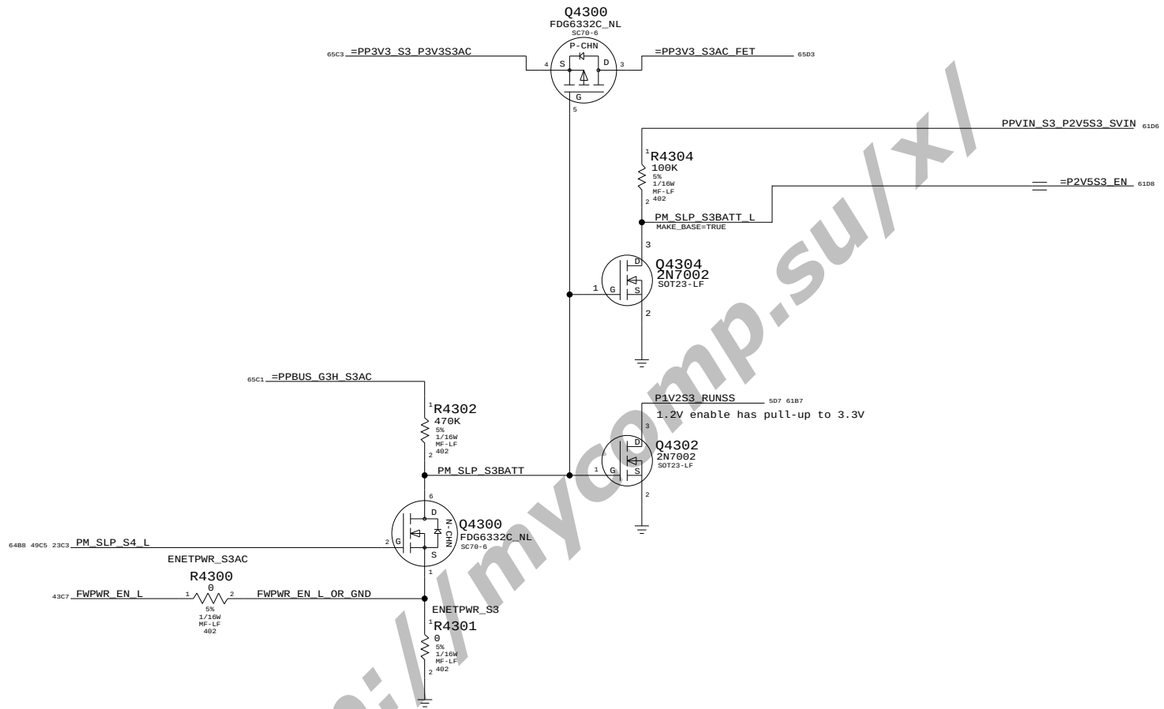


Ethernet Connector		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
	SCALE NONE	SHT 40 OF 84	

Yukon Power Control

Allows powering Yukon down during battery sleep to save power



When ENETPWR_S3AC BOMOPTION is active:

State	FWPWR_EN_L	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S0 Batt	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 AC	0V	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3 Batt	PBUS	3.3V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 AC	0V	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
S5 Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H Batt	PBUS	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

When ENETPWR_S3 BOMOPTION is active:

State	PM_SLP_S4_L	PM_SLP_S3BATT	PM_SLP_S3BATT_L	P2V5S3_EN	P1V2S3_RUNSS
S0	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S3	3.3V	0V (3.3V ON)	3.3V	3.3V (2.5V ON)	3.3V (1.2V ON)
S5	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)
G3H	0V	PBUS (3.3V OFF)	0V	0V (2.5V OFF)	0V (1.2V OFF)

Yukon Power Control

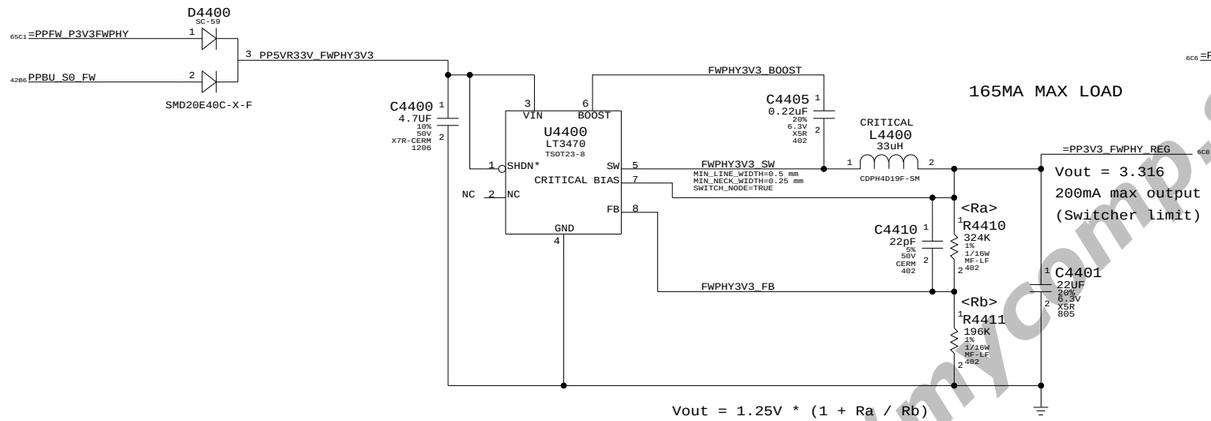
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

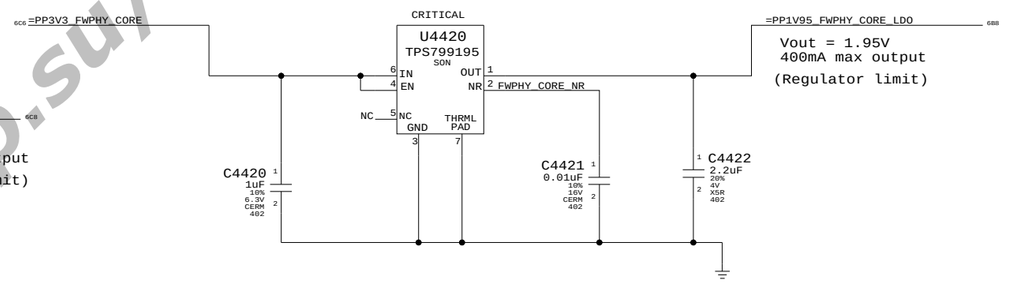
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	41	84

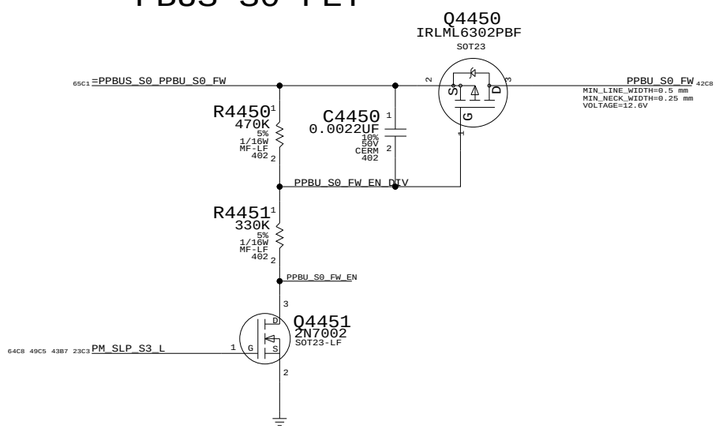
3.3V Supply for FWPHY



1.95V Supply for FW PHY



PBUS S0 FET



FW PHY Power Supply		
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)	

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
	SCALE: NONE	SHT 42 OF 84	

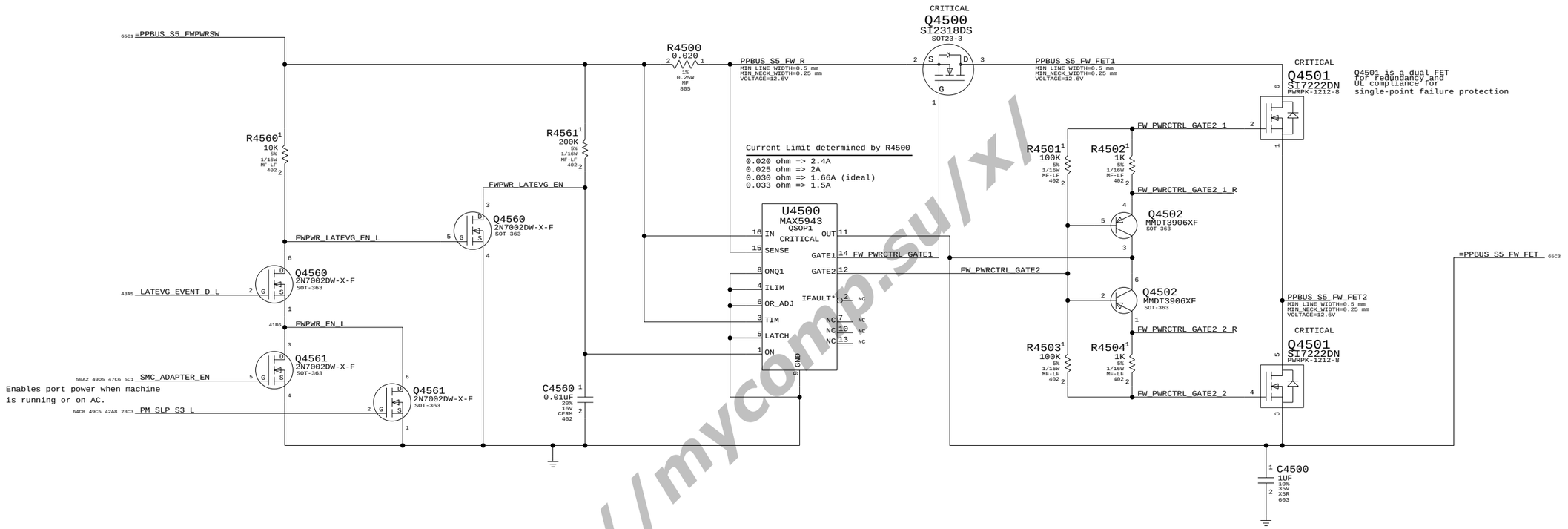
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

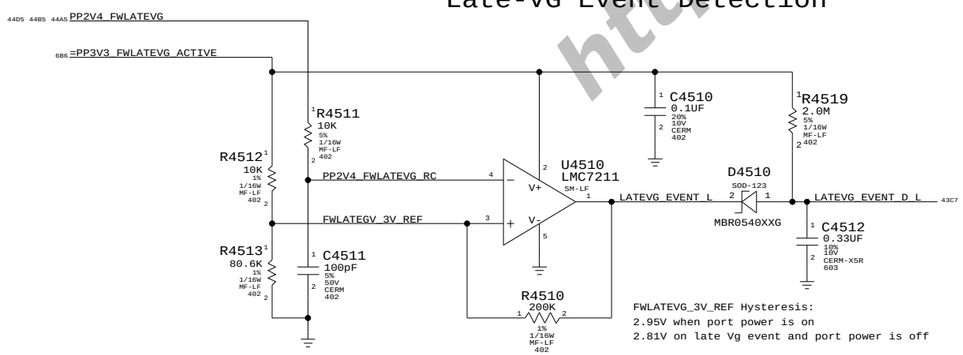
Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Current Limit/Active Late-VG Protection



Late-VG Event Detection



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 43 OF 84	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
PROVIDED	FW	FW_110D	FW_PORT1_TPA_P	44B5 44C5
	FW	FW_110D	FW_PORT1_TPA_N	44B5 44C5
	FW	FW_110D	FW_PORT1_TPB_P	44B5 44C5
BY	FW	FW_110D	FW_PORT1_TPB_N	44B5 44C5
	FW	FW_110D	FW_PORT2_TPA_FL_P	44B2
PHY	FW	FW_110D	FW_PORT2_TPA_FL_N	44B2
	FW	FW_110D	FW_PORT2_TPB_FL_P	44B2
PAGE	FW	FW_110D	FW_PORT2_TPB_FL_N	44B2

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

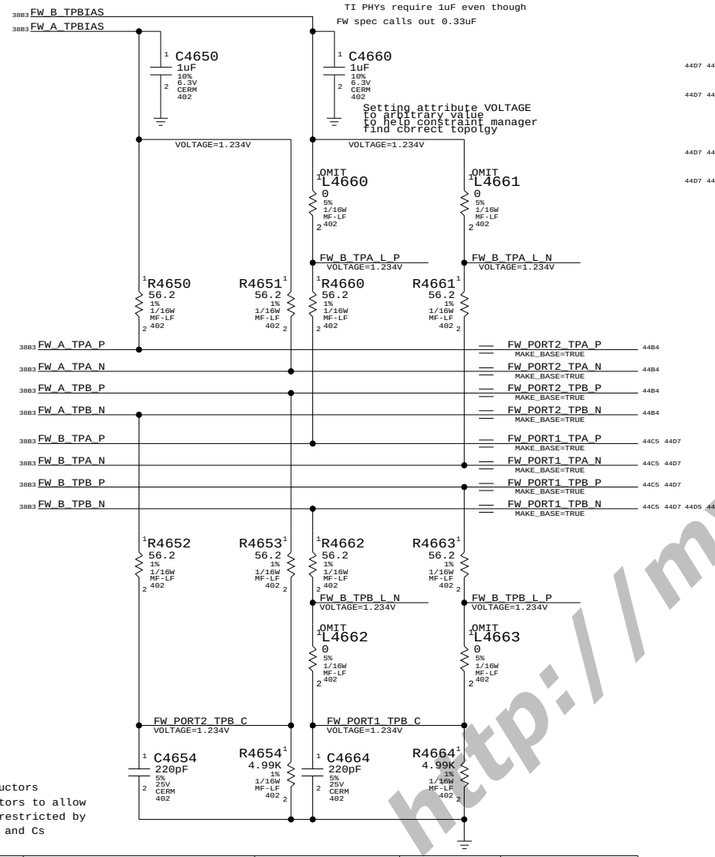
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

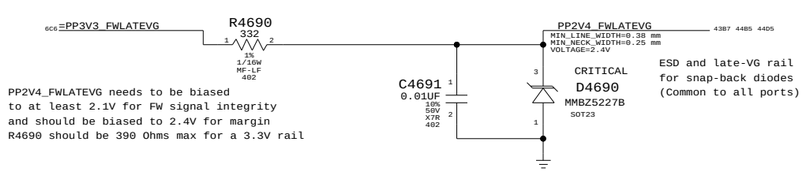
Place close to FireWire PHY



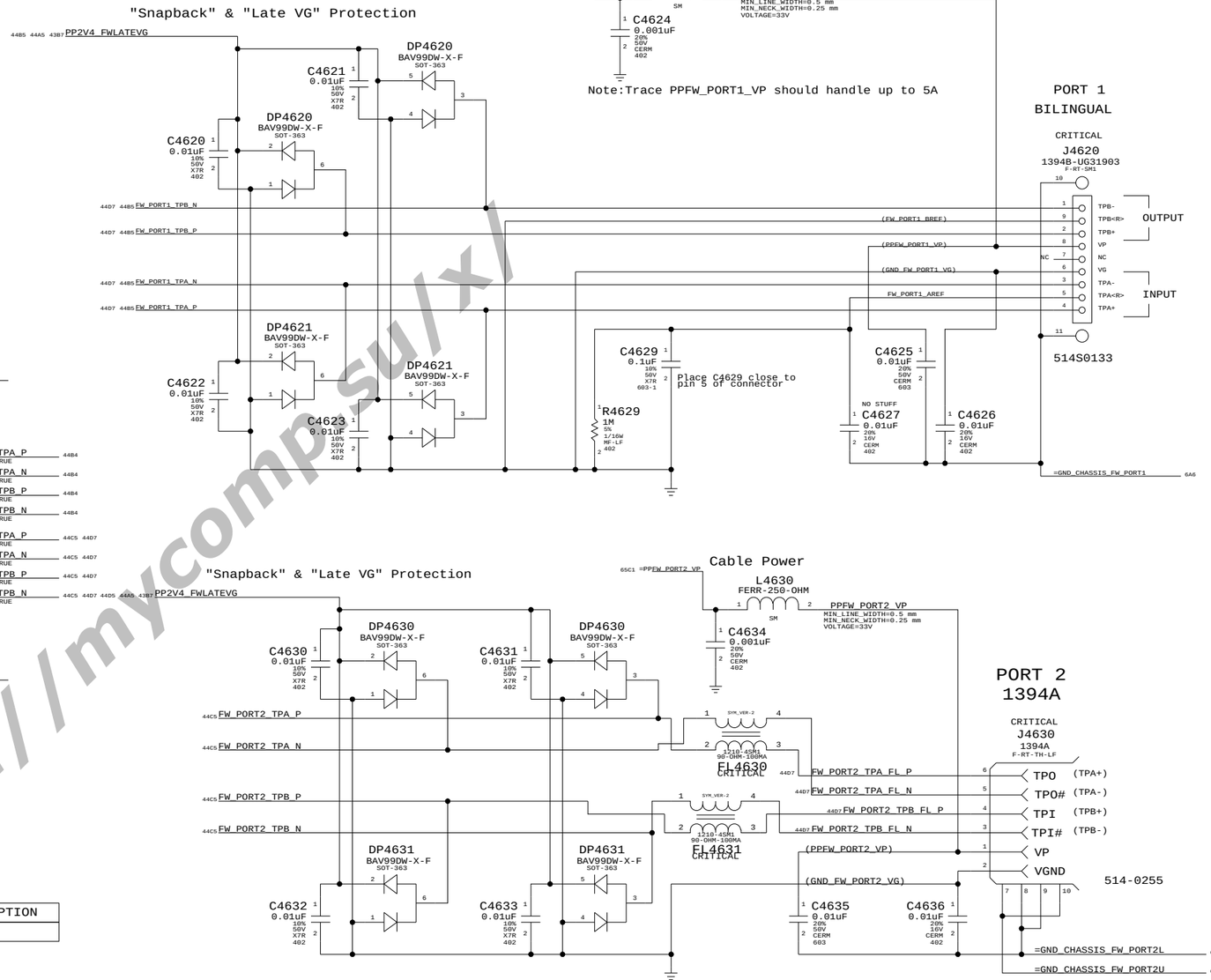
Note: The peaking inductors were changed to resistors to allow placement in an area restricted by DFM rules for only Rs and Cs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S0414	4	IND,18nH-15mA,0402	L4660,L4661,L4662,L4663	CRITICAL	

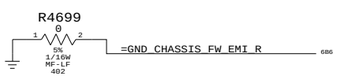
Late-VG Protection Power



"Snapback" & "Late VG" Protection



"Snapback" & "Late VG" Protection

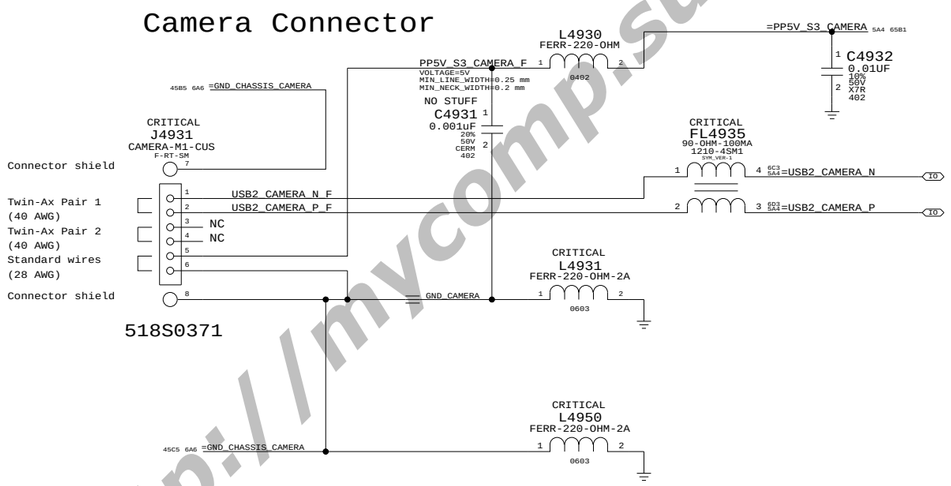


FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7150	A.0.0
	SCALE: NONE	SHT 44 OF 84	

Camera Connector



Camera Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE

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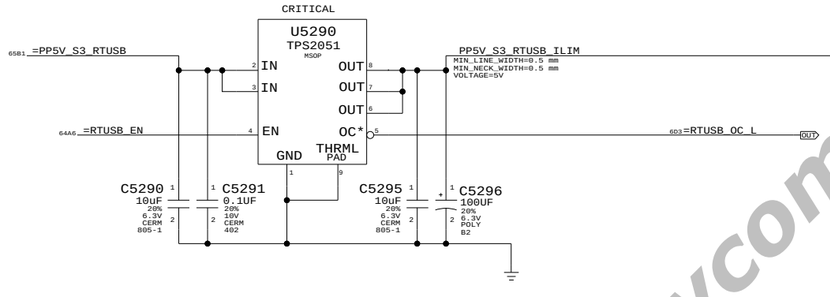
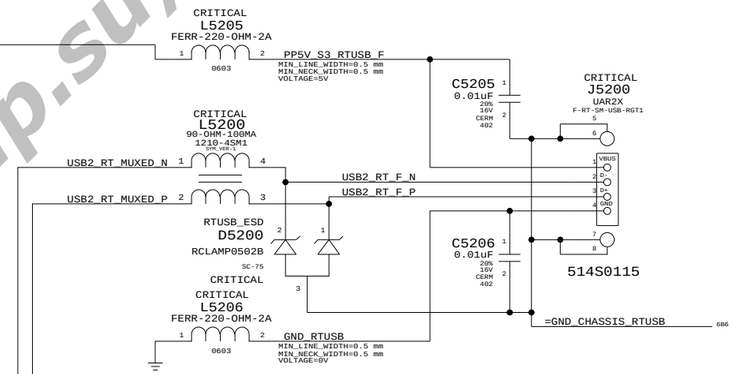
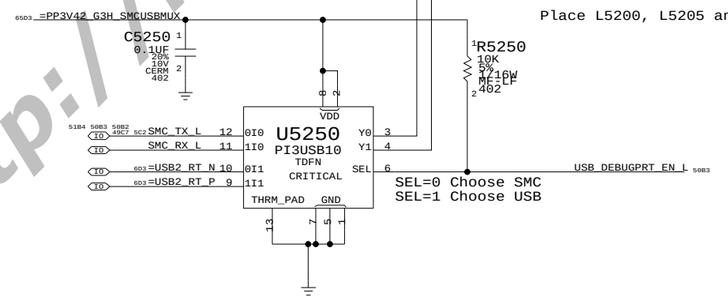
Port Power Switch



Right USB Port



USB/SMC Debug Mux



Place L5200, L5205 and L5206 across moat

External USB Connector

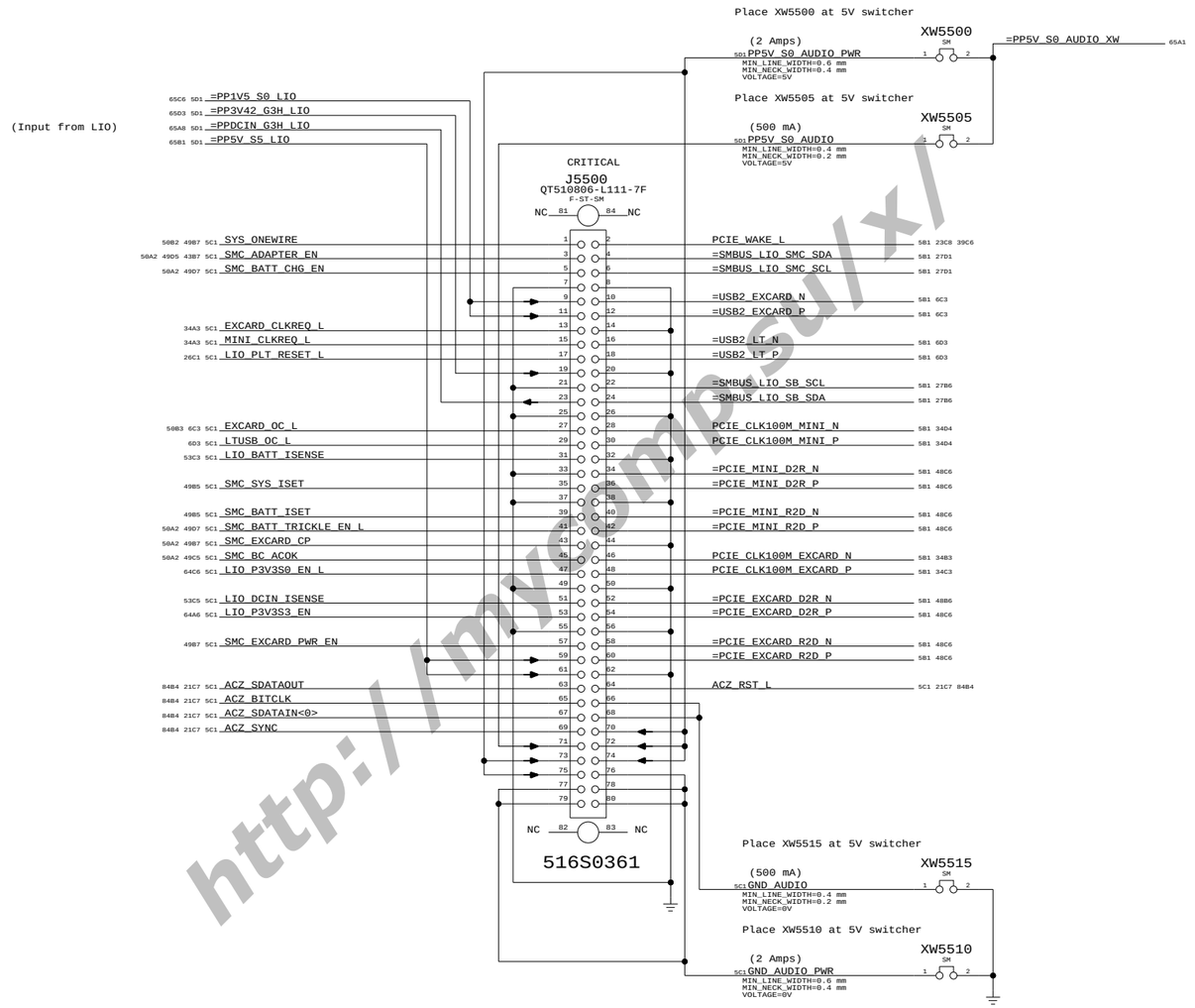
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	46	84

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	47	84

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

47B3 5B1	=PCIE_MINI_R2D_P	PCIE_MINI_R2D_C_P	MAKE_BASE=TRUE	PCIE_B_R2D_C_P	22D4
47B3 5B1	=PCIE_MINI_R2D_N	PCIE_MINI_R2D_C_N	MAKE_BASE=TRUE	PCIE_B_R2D_C_N	22D4
47C3 5B1	=PCIE_MINI_D2R_P	PCIE_MINI_D2R_P	MAKE_BASE=TRUE	PCIE_B_D2R_P	22D4
47C3 5B1	=PCIE_MINI_D2R_N	PCIE_MINI_D2R_N	MAKE_BASE=TRUE	PCIE_B_D2R_N	22D4

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

47B3 5B1	=PCIE_EXCARD_R2D_P	PCIE_EXCARD_R2D_C_P	MAKE_BASE=TRUE	PCIE_C_R2D_C_P	22D4
47B3 5B1	=PCIE_EXCARD_R2D_N	PCIE_EXCARD_R2D_C_N	MAKE_BASE=TRUE	PCIE_C_R2D_C_N	22D4
47B3 5B1	=PCIE_EXCARD_D2R_P	PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	PCIE_C_D2R_P	22D4
47B3 5B1	=PCIE_EXCARD_D2R_N	PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	PCIE_C_D2R_N	22D4

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP	MAKE_BASE=TRUE	PCIE_D_R2D_C_P	22D4
TP_PCIE_D_R2DN	MAKE_BASE=TRUE	PCIE_D_R2D_C_N	22D4
TP_PCIE_D_D2RP	MAKE_BASE=TRUE	PCIE_D_D2R_P	22D4
TP_PCIE_D_D2RN	MAKE_BASE=TRUE	PCIE_D_D2R_N	22D4

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP	MAKE_BASE=TRUE	PCIE_E_R2D_C_P	22C4
TP_PCIE_E_R2DN	MAKE_BASE=TRUE	PCIE_E_R2D_C_N	22C4
TP_PCIE_E_D2RP	MAKE_BASE=TRUE	PCIE_E_D2R_P	22C4
TP_PCIE_E_D2RN	MAKE_BASE=TRUE	PCIE_E_D2R_N	22C4

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP	MAKE_BASE=TRUE	PCIE_F_R2D_C_P	22C4
TP_PCIE_F_R2DN	MAKE_BASE=TRUE	PCIE_F_R2D_C_N	22C4
TP_PCIE_F_D2RP	MAKE_BASE=TRUE	PCIE_F_D2R_P	22C4
TP_PCIE_F_D2RN	MAKE_BASE=TRUE	PCIE_F_D2R_N	22C4

PCI-E Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 48 OF 84

UNUSED PINS HAVE THE FORMAT
SMC_XXX WHERE XXX IS THE PORT NUMBER.
THEY ARE SET BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.

OMIT
U5800
SMC_H8S2116
BGA
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PM_LAN_ENABLE	B12	P10	P60/KIN0*	L13	64A8	SMC_PM_G2_EN
SMC_RSTGATE_L	C13	P11	P61/KIN1*	L14	47C6 50A2 53B7	SMC_ADAPTER_EN
ALL_SYS_PWRGD	A15	P12	P62/KIN2*	L15	22C6	SPI_ARB
RSMRST_PWRGD	B14	P13	P63/KIN3*	K12	54C7 22C6	SPI_SCLK
SMC_SB_NMI	B15	P14	P64/KIN4*	K13	54C1 22C6	SPI_SI
PM_RSMRST_L	C14	P15	P65/KIN5*	K14	54C1 22C6	SPI_SO
IMVP_VR_ON	D12	P16	P66/IRQ6*/KIN6*	J12	50B1	SMC_PROCHOT_3_3_L
PM_PWRBTN_L	C15	P17	P67/IRQ7*/KIN7*	J13	50B5	SMC_CPU_INIT_3_3_L
SMC_P20	D13	P20	P70/AN0	N12	53B7	SMC_CPU_ISENSE
SMC_P21	D14	P21	P71/AN1	R13	53D6	SMC_CPU_VSENSE
SMC_P22	D15	P22	P72/AN2	P13	53B6	SMC_GPU_ISENSE
SMC_P23	E12	P23	P73/AN3	R14	53C6	SMC_GPU_VSENSE
SMC_BATT_TRICKLE_EN_L	E14	P24	P74/AN4	P14	53C4	SMC_DCIN_ISENSE
SMC_BATT_CHG_EN	E15	P25	P75/AN5	R15	53D2	SMC_PBUS_VSENSE
SMC_P26	E13	P26	P76/AN6	N13	53C2	SMC_BATT_ISENSE
SMC_P27	F14	P27	P77/AN7	P15	50D5	SMC_NB1V5_ISENSE
LPC_AD<0>	D9	P30/LAD0	P80/PME*	C7	23C1	SMC_WAKE_SCI_L
LPC_AD<1>	C9	P31/LAD1	P81/GA20	A7	50C5	SMC_TPM_GPIO
LPC_AD<2>	A9	P32/LAD2	P82/CLKRUN*	B7	51C4 23C8 50C6	PM_CLKRUN_L
LPC_AD<3>	B9	P33/LAD3	P83/LPCPD*	D6	50A2 23C5 50C6 51B5	PM_SUS_STAT_L
LPC_FRAME_L	D8	P34/LFRAME*	P84/IRQ3*/TXD1	C6	50B5	SC_TX_L
SMC_LRESET_L	C8	P35/LRESET*	P85/IRQ4*/RXD1	A6	50B5	SC_RX_L
PCI_CLK_SMC	A8	P36/LCLK	P86/IRQ5*/SCK1/SCL1	B6	27B3	SMB_BSB_CLK
INT_SERIRQ	D7	P37/SERIRQ	P90/IRQ2*	K4	50C6 78C2 50B2 50C2	SMC_ONOFF_L
SMC_XDP_TMS	A5	P40/TMIO	P91/IRQ1*	J2	50A2 47B6 5C1	SMC_BC_ACOK
SMC_SYS_LED_16B	B5	P41/TMO0	P92/IRQ0*	J1	66B5 50B2 5D1	SMC_BS_ALRT_L
SMB_BSB_DATA	D5	P42/SDA1	P93/IRQ12*	J3	43B7 42A8 23C8 64C8	PM_SLP_S3_L
SMC_TPM_PP	C3	P43/TMI1/EXSCKX1	P94/IRQ13*	J4	64B8 4186 23C4	PM_SLP_S4_L
SMC_XDP_TRST_L	B1	P44/TMO1	P95/IRQ14*	H2	50A2 23C3	PM_SLP_S5_L
SMC_XDP_TCK	C2	P45	P96/EXCL	H1	35B2	SMC_SUS_CLK
SMC_SYS_LED	D3	P46/PWX0/PWM0	P97/IRQ15*/SDA0	G2	27D6	SMB_0_S0_DATA
SMC_SYS_KBDLED	C1	P47/PWX1/PWM1				
SMC_TX_L	G1	P50				
SMC_RX_L	G4	P51				
SMB_0_S0_CLK	F2	P52/SCL0				

OMIT
U5800
SMC_H8S2116
BGA
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SMC_RCIN_L	R3	PA0/KIN8*/PA2DC	PE0	M3	50A2 SMC_CASE_OPEN
BOOT_LPC_SPI_L	P3	PA1/KIN9*/PA2DD	PE1*/ETCK	M2	51B5 50B2 5C2 SMC_TCK
PM_SYSRST_L	R2	PA2/KIN10*/PS2AC	PE2*/ETDI	M1	51B5 50B2 5C2 SMC_TDI
SMC_USB_DEBUG_MUX	N3	PA3/KIN11*/PS2AD	PE3*/ETDO	L4	51B4 50B2 5C2 SMC_TDO
PM_EXTTS_L	R1	PA4/KIN12*/PS2BC	PE4*/ETMS	L2	51B4 50B2 5C2 SMC_TMS
PM_THRM_L	N2	PA5/KIN13*/PS2BD	PF0/IRQ8*/PWM2	M7	SMC_PF0 50C5
SYS_ONEWIRE	M4	PA6/KIN14*/PS2CC	PF1/IRQ9*/PWM3	P6	SMC_PF1 50C5
PM_BATLOW_L	N1	PA7/KIN15*/PS2CD	PF2/IRQ10*/TMOY	R6	78C3 50B2 SMC_LID
SMC_EXTSMI_L	B10	PB0/LSMI*	PF3/IRQ11*/TMOX	N6	50B2 SMC_CPU_RESET_3_3_L
SMC_RUNTIME_SCI_L	A10	PB1/LSCI	PF4/PWM4	M6	47B6 5C1 SMC_BATT_ISET
SMC_ODD_DETECT	D10	PB2	PF5/PWM5	R5	50D5 SMC_BATT_VSET
ISENSE_CAL_EN	A11	PB3	PF6/PWM6	P5	47C6 5C1 SMC_SYS_ISET
SMC_EXCARD_CP	B11	PB4	PF7/PWM7	N5	50D5 SMC_SYS_VSET
SMC_EXCARD_PWR_EN	C11	PB5	PG0/EXIRQ8*/TMIX	P9	54C7 22C6 SPI_CE_L
SMC_EXCARD_OC_L	A12	PB6	PG1/EXIRQ9*/TMIY	R9	50B2 SMC_XDP_TCK_3_3
SMC_XDP_TDO_3_3	D11	PB7	PG2/EXIRQ10*/SDA2	N9	27C2 SMB_BSA_DATA
SMC_FAN_0_CTL	G14	PC0/TIOCA0/WUE8*	PG3/EXIRQ11*/SCL2	P8	27C1 SMB_BSA_CLK
SMC_FAN_1_CTL	G15	PC1/TIOCB0/WUE9*	PG4/EXIRQ12*/EXSDAA	R8	27C6 SMB_A_S3_DATA
SMC_FAN_2_CTL	G13	PC2/TIOCC0/TCLKA/WUE10*	PG5/EXIRQ13*/EXSCLA	M8	27C5 SMB_A_S3_CLK
SMC_FAN_3_CTL	G12	PC3/TIOCD0/TCLKB/WUE11*	PG6/EXIRQ14*/EXSDAB	P7	27D2 SMB_B_S0_DATA
SMC_FAN_0_TACH	H14	PC4/TIOCA1/WUE12*	PG7/EXIRQ15*/EXSCLB	R7	27D3 SMB_B_S0_CLK
SMC_FAN_1_TACH	H15	PC5/TIOCB1/TCLKC/WUE13*	PH0/EXIRQ6*	E1	50C2 SMC_PROCHOT
SMC_FAN_2_TACH	H13	PC6/TIOCA2/WUE14*	PH1/EXIRQ7*	F3	50C2 SMC_THRMTRIP
SMC_FAN_3_TACH	H12	PC7/TIOCB2/TCLKD/WUE15*	PH2/FWE	K2	50B2 SMC_FWE
SMS_X_AXIS	M11	PD0/AN8	PH3/EXEXCL	C4	78C6 6D5 5B2 ALS_GAIN
SMS_Y_AXIS	P11	PD1/AN9	PH4	D4	50B2 23C3 SMS_INT_L
SMS_Z_AXIS	R11	PD2/AN10	PH5	B3	57C6 SMS_ONOFF_L
SMC_ANALOG_ID	N11	PD3/AN11			
SMC_NB_ISENSE	P10	PD4/AN12			
SMC_MEM_ISENSE	R10	PD5/AN13			
ALS_LEFT	N10	PD6/AN14			
ALS_RIGHT	M10	PD7/AN15			

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SMC_H8S2116
BGA
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G3	NC0	NC12	F15
H3	NC1	NC13	A14
K3	NC2	NC14	C12
L3	NC3	NC15	C10
N4	NC4	NC16	C5
M5	NC5	NC17	A3
N7	NC6	NC18	B8
M12	NC7	NC19	E4
M13	NC8	NC20	H4
L12	NC9	NC21	M9
K15	NC10	NC22	N8
J14	NC11		

65D3 50D7 50B1 49D4 49C2 =PP3V3_S5_SMC

C5802 22UF 20% 6.3V CERM 805
C5803 0.1UF 20% 10V CERM 402
C5804 0.1UF 20% 10V CERM 402
C5805 0.1UF 20% 10V CERM 402
C5806 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

SMC_VCL
C5807 0.47UF 10% 6.3V CERM-X5R 402
VCL IS INTERNAL RAIL

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

65D3 50D7 50B1 49D3 49C2 =PP3V3_S5_SMC
R5899 4.7 5% 1/10W MF-LF 402
PP3V3_AVCC_SMC
MIN_LINE_WIDTH=0.35 MM
MIN_NECK_WIDTH=0.20 MM
C5820 0.1UF 20% 10V CERM 402

PP3V3_AVREF_SMC 50B6
49D4 65D3 49D3 50D7 50B1 =PP3V3_S5_SMC

55C2 53D6 53C6 53C1 53B7 53B5 53B3 53B1 50B6 49B2 55C6 GND_SMC_AVSS

OMIT
U5800
SMC_H8S2116
BGA
(3 OF 4)

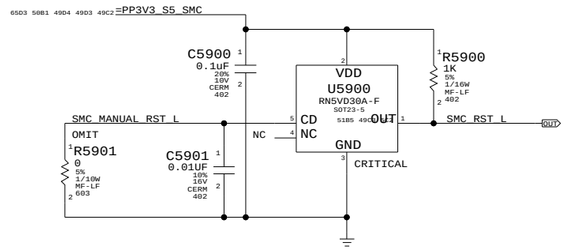
AVCC	N14		
AVCC	N15		
VCC	P2		
VCC	P1		
VCC	J15		
VCC	A1		
VCL	F1		
AVREF	M14		
AVREF	M15		
51B5 50D6 5C2 SMC_RST_L	E3	RES*	
50C8 SMC_XTAL	A2	XTAL	
50C8 SMC_EXTAL	B2	EXTAL	
MD1	F2		SMC_MD1 5C2 51B4
MD2	K1		KBC_MDE
NMI	F4		51B5 5C2 SMC_NMI
ETRST*	L1		51B4 5C2 SMC_TRST_L
AVSS	P12		
AVSS	R12		
VSS	D1		
VSS	F4		
VSS	R4		
VSS	F12		
VSS	F13		
VSS	B13		
VSS	A13		
VSS	A4		
VSS	B4		
VSS	D2		

R5809 10K 5% 1/16W MF-LF 402
R5801 10K 5% 1/16W MF-LF 402
R5898 10K 5% 1/16W MF-LF 402
NOSTUFF
R5803 0 5% 1/16W MF-LF 402
R5802 10K 5% 1/16W MF-LF 402

XW5800 SM
GND_SMC_AVSS 49C4 50B6 53B1 53B3 53B5 53B7 53C1 53C6 53D6 55C2 55C6

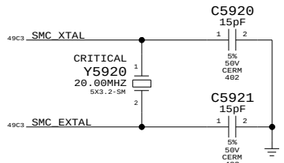
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150	REV. A.0.0
	SCALE NONE	SHT 49 OF 84	

SMC Reset Button / Brownout Detect

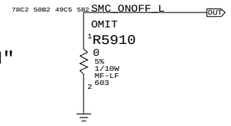


Silk: "SMC RST"

SMC Crystal Circuit

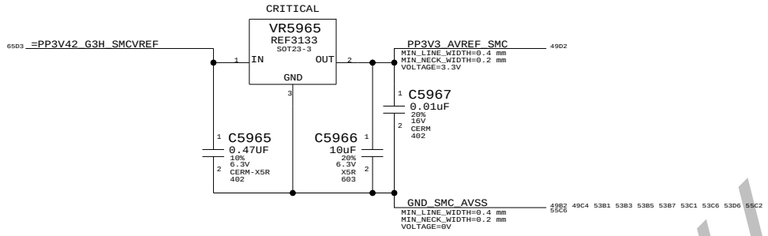


Debug Power Button

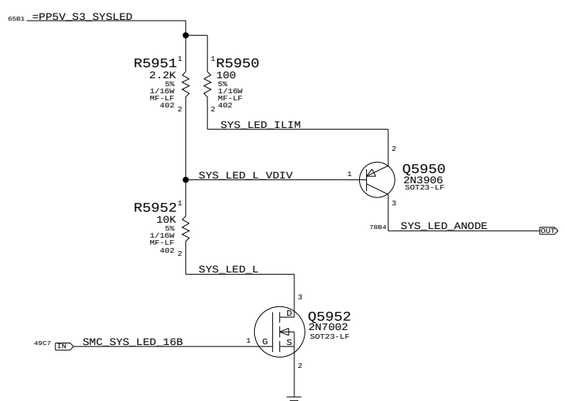


Silk: "PWR BTN"

SMC AVREF Supply

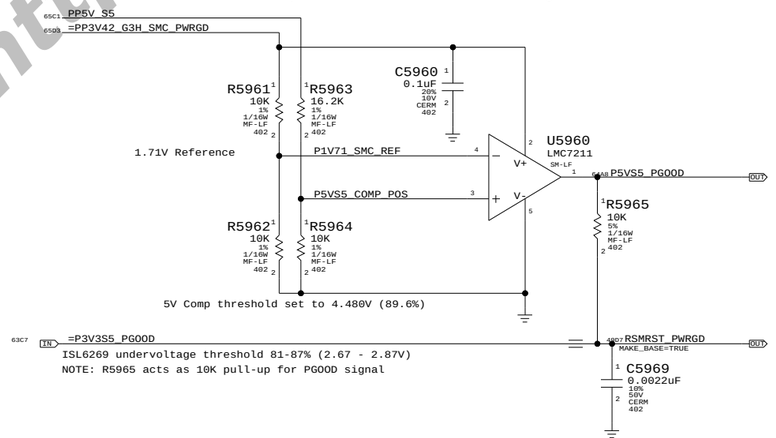


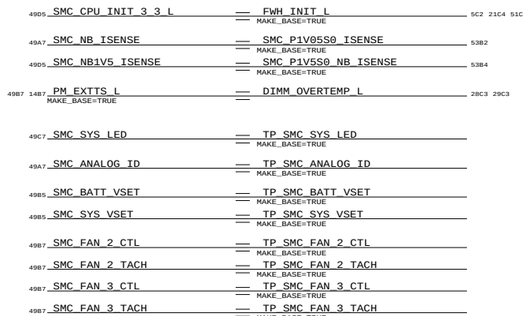
System (Sleep) LED Circuit

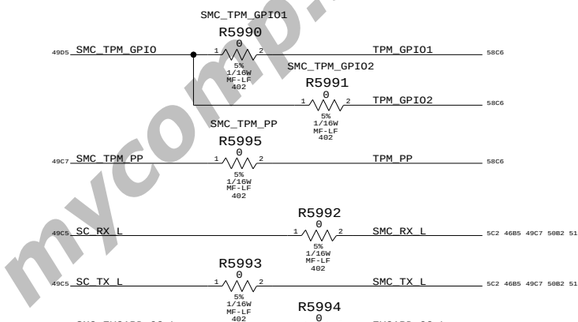


SMC PWRGD Circuit

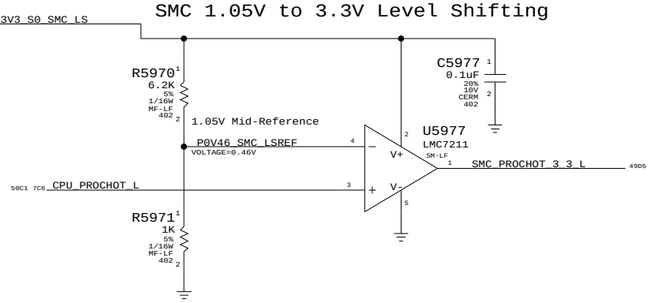
Reports when 5V S5 and 3.3V S5 are in regulation



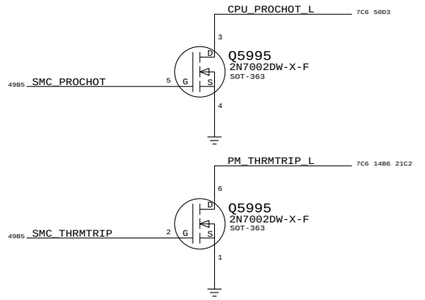


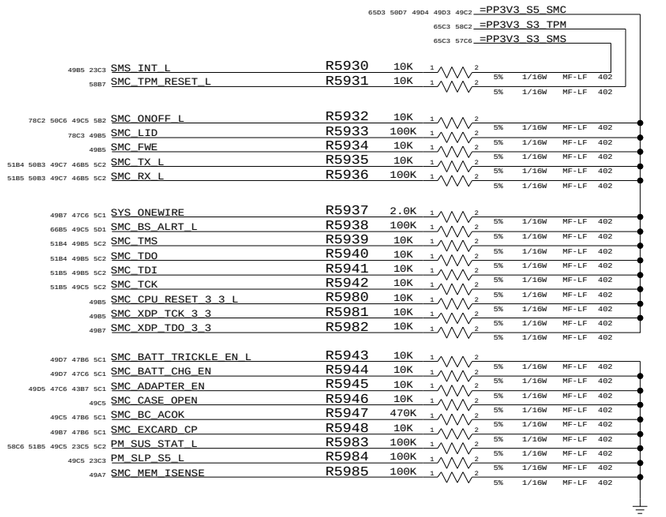


SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting





SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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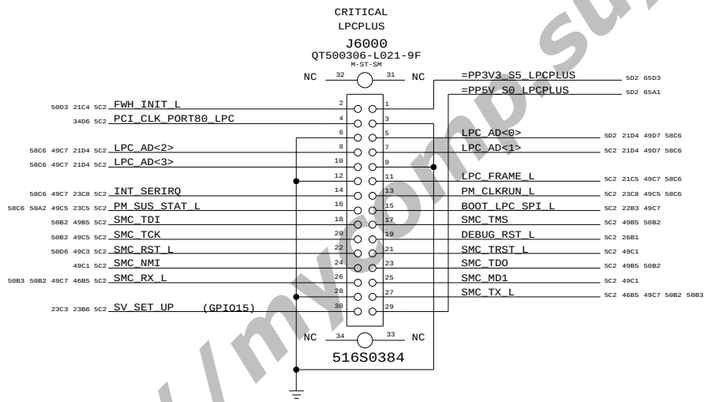
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 50 OF 84	



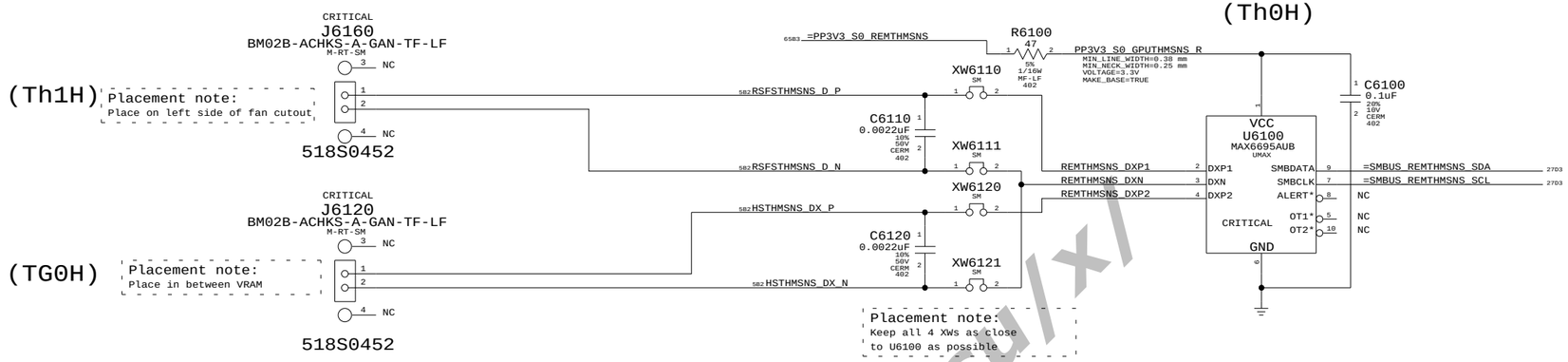
LPC+ Debug Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

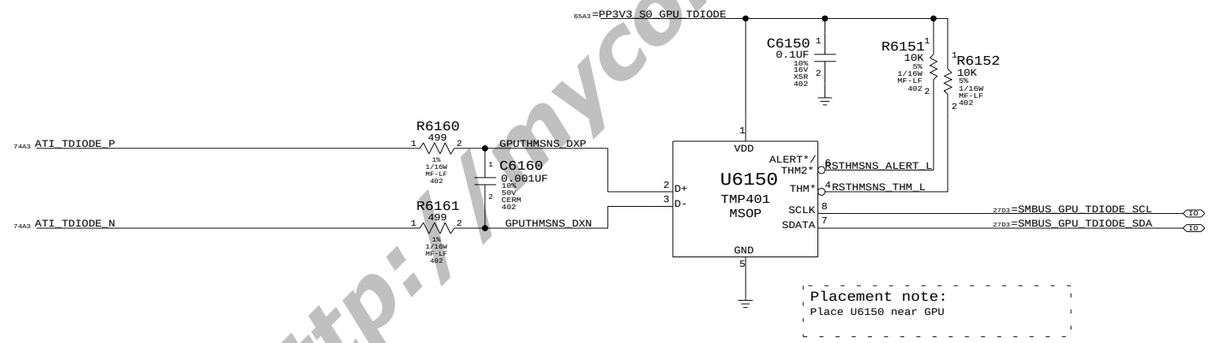
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 51 OF 84	

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor



GPU Die Thermal Sensor



Thermal Sensors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

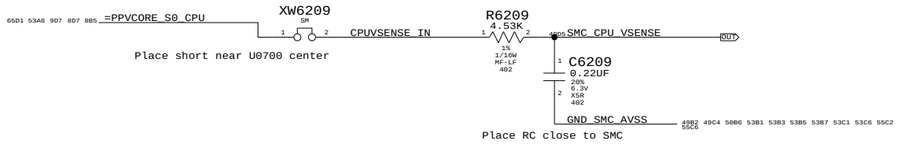
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE

SHT 52 OF 84

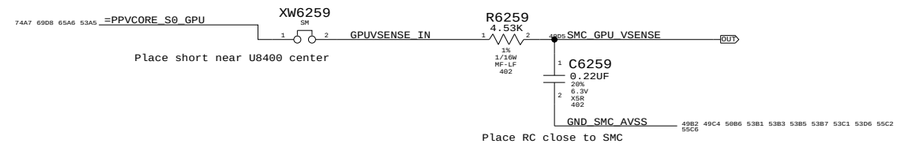
CPU Voltage Sense / Filter



Place short near U0700 center

Place RC close to SMC

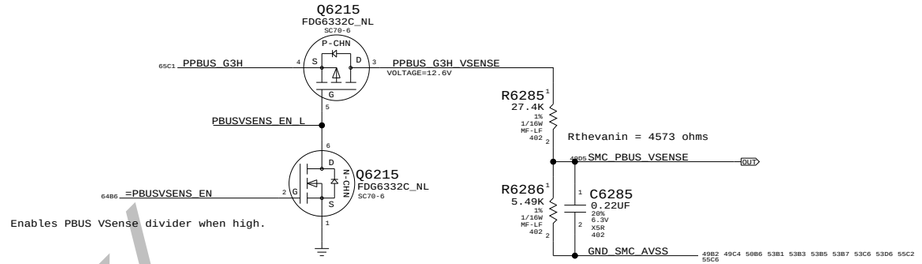
GPU Voltage Sense / Filter



Place short near U8400 center

Place RC close to SMC

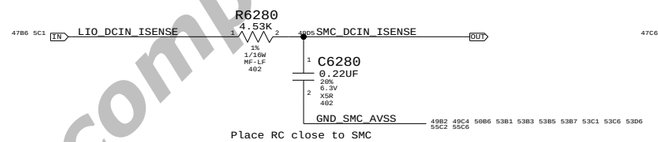
PBUS Voltage Sense Enable & Filter



Enables PBUS VSense divider when high.

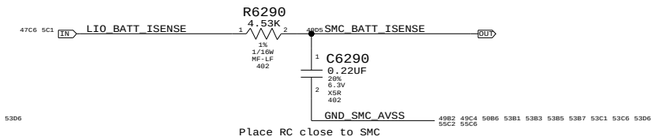
Place RC close to SMC

DCIN Current Sense Filter



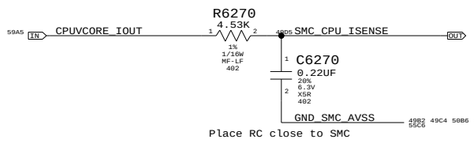
Place RC close to SMC

Battery Current Sense Filter



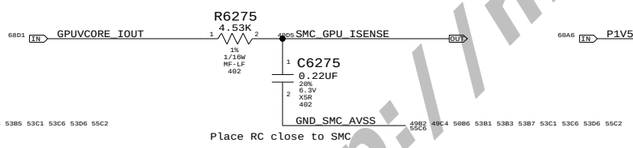
Place RC close to SMC

CPU Current Sense Filter



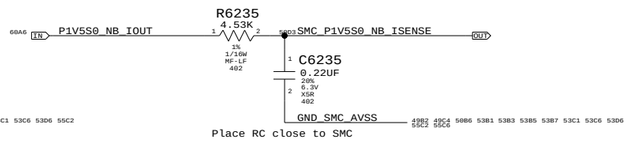
Place RC close to SMC

GPU Current Sense Filter



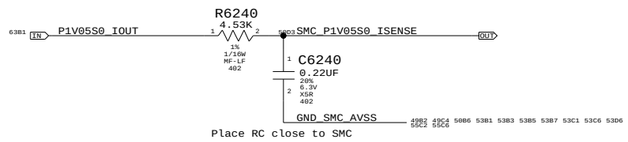
Place RC close to SMC

1.5V S0 (NB) Current Sense Filter



Place RC close to SMC

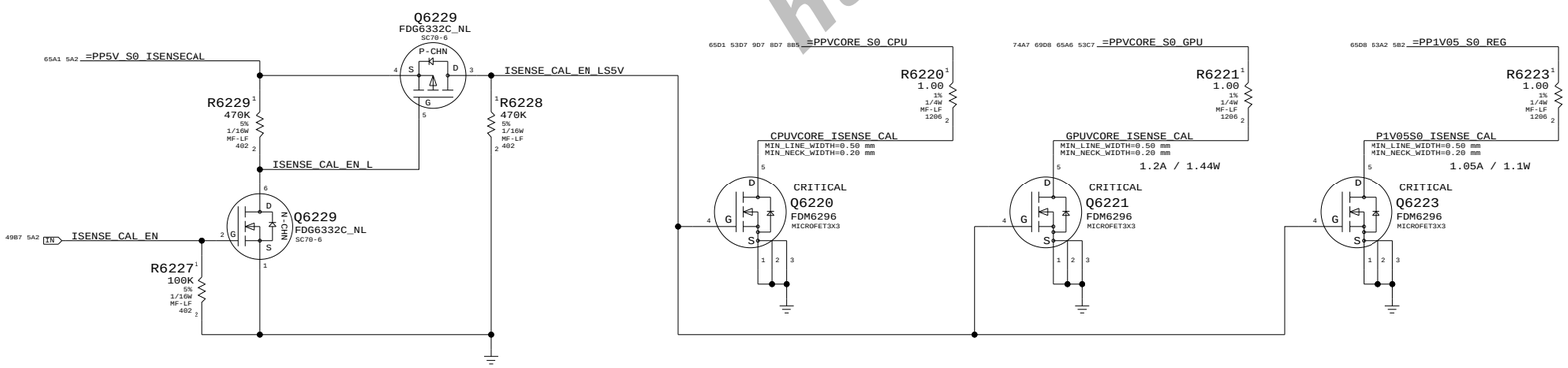
1.05V S0 (NB) Current Sense Filter



Place RC close to SMC

Current Sense Calibration Circuit

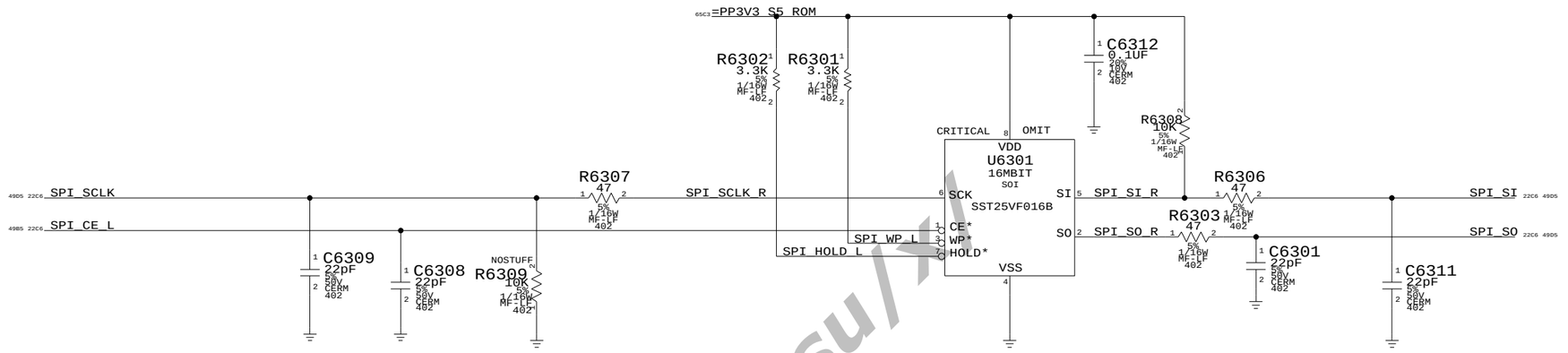
Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing		
SYNC_MASTER=(MASTER)		SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 53 OF 84	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

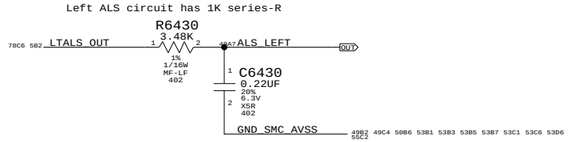
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE

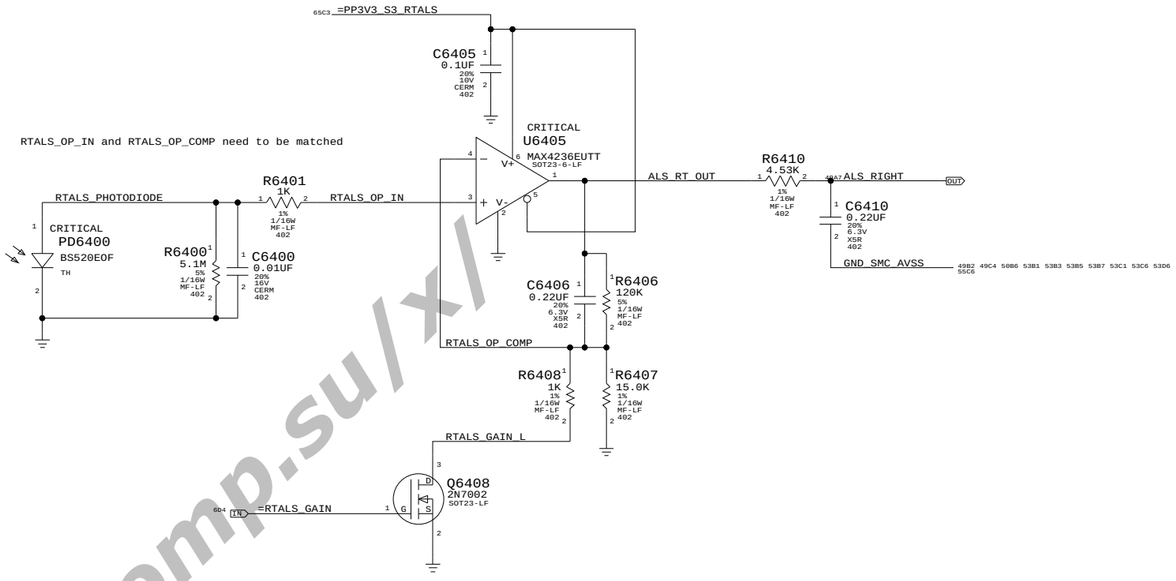
SHT 54 OF 84

Left ALS Filter

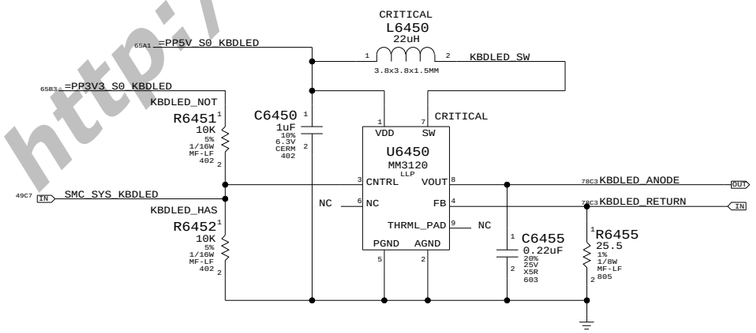
Left ALS circuit has 1K series-R



Right ALS Circuit



Keyboard LED Driver



ALS Support

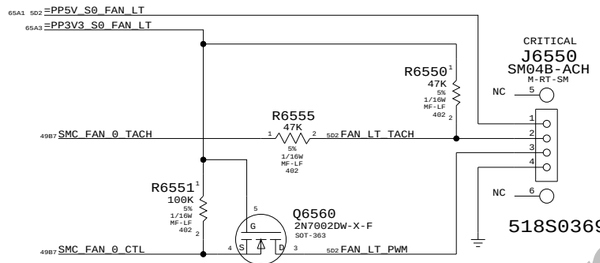
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

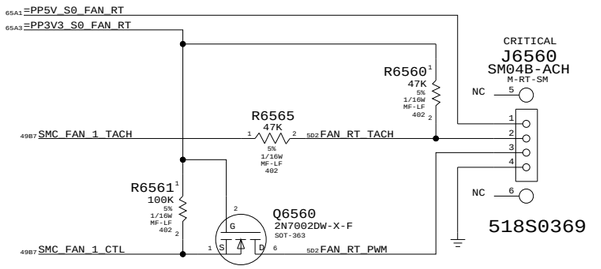
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 55 OF 84

Left Fan



Right Fan



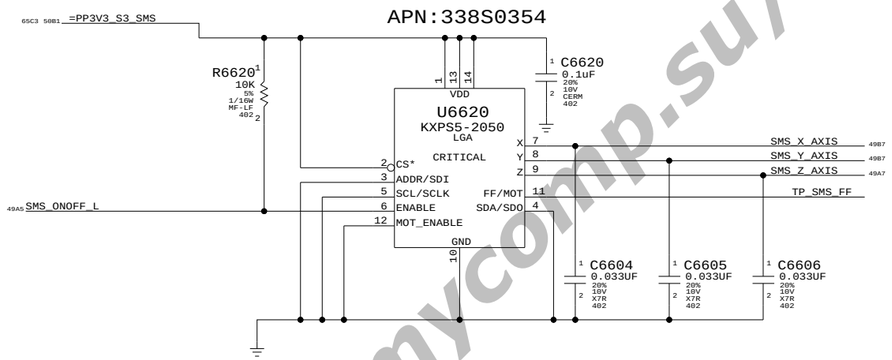
Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

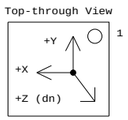
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	56	84



Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:



M59 placement: Bottom-side

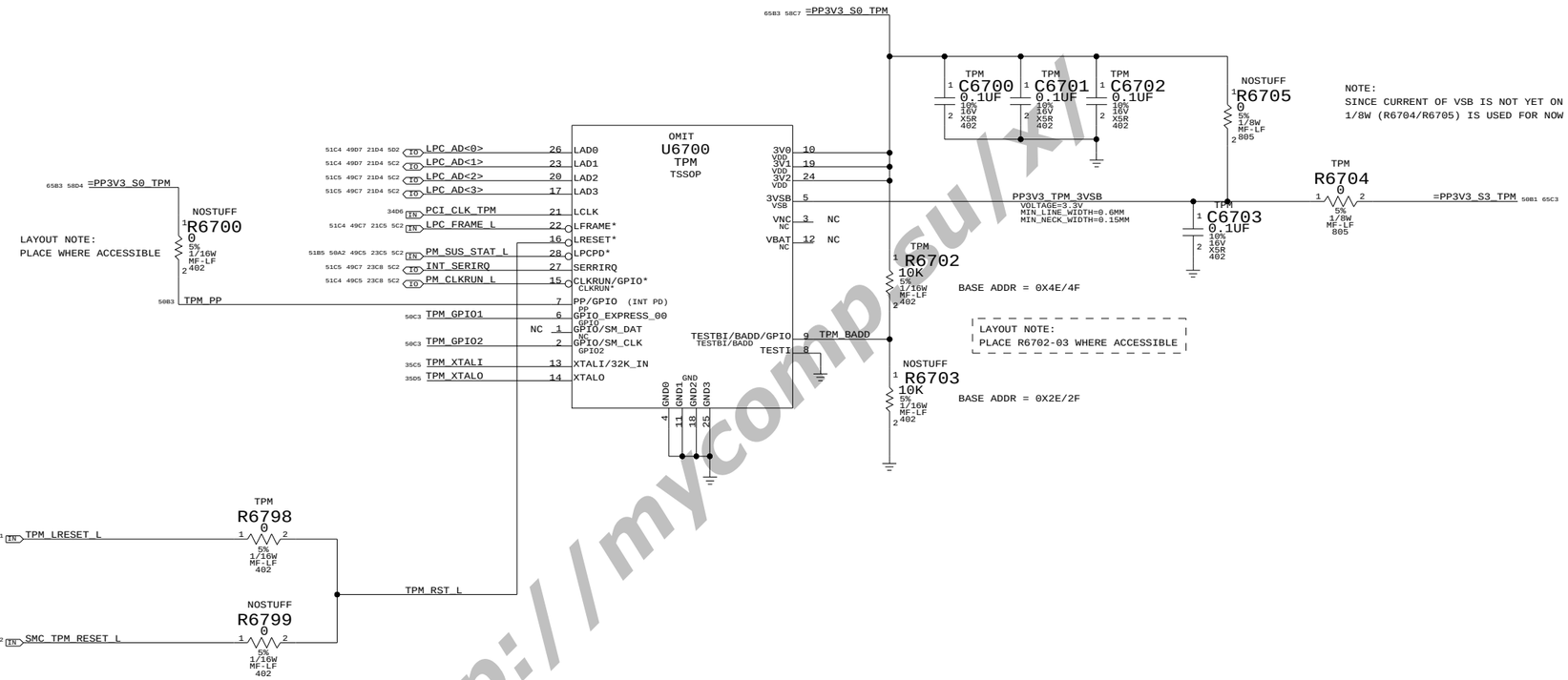
Sudden Motion Sensor (SMS)

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 57 OF 84



TPM

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	58	84

DPRSLPVR	DPRSTP*	PSI*	Operation Mode	
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

These caps for Q7500

These caps for Q7550

Vout = Variable
36A max output
(Inductors limit)

CPU VCore Current Sense

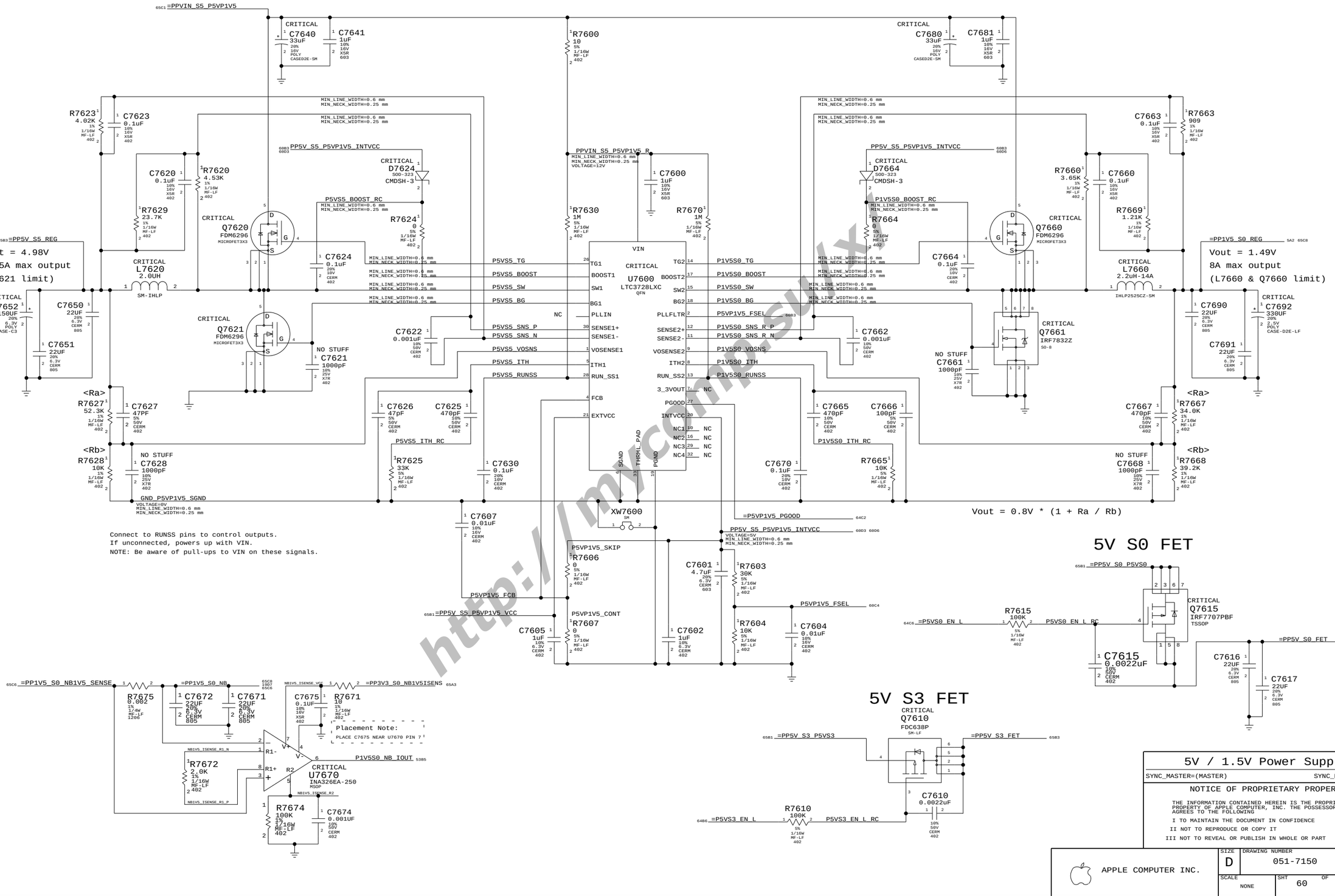
Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

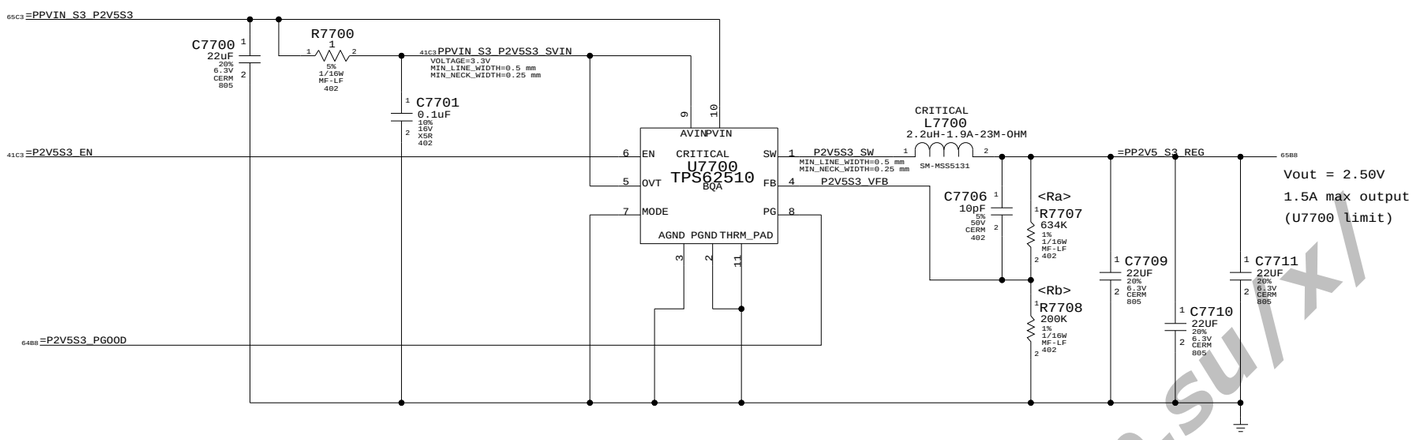
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 59 OF 84	

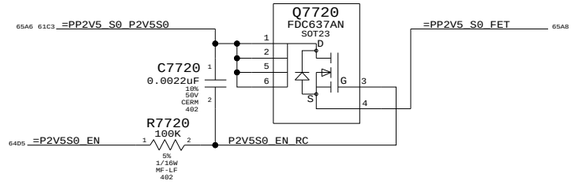


2.5V S3 Regulator

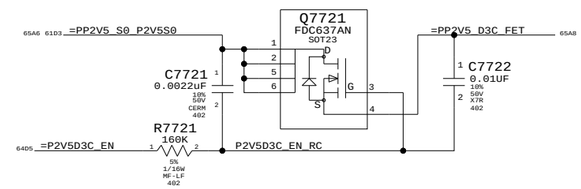


Vout = 0.6V * (1 + Ra / Rb)

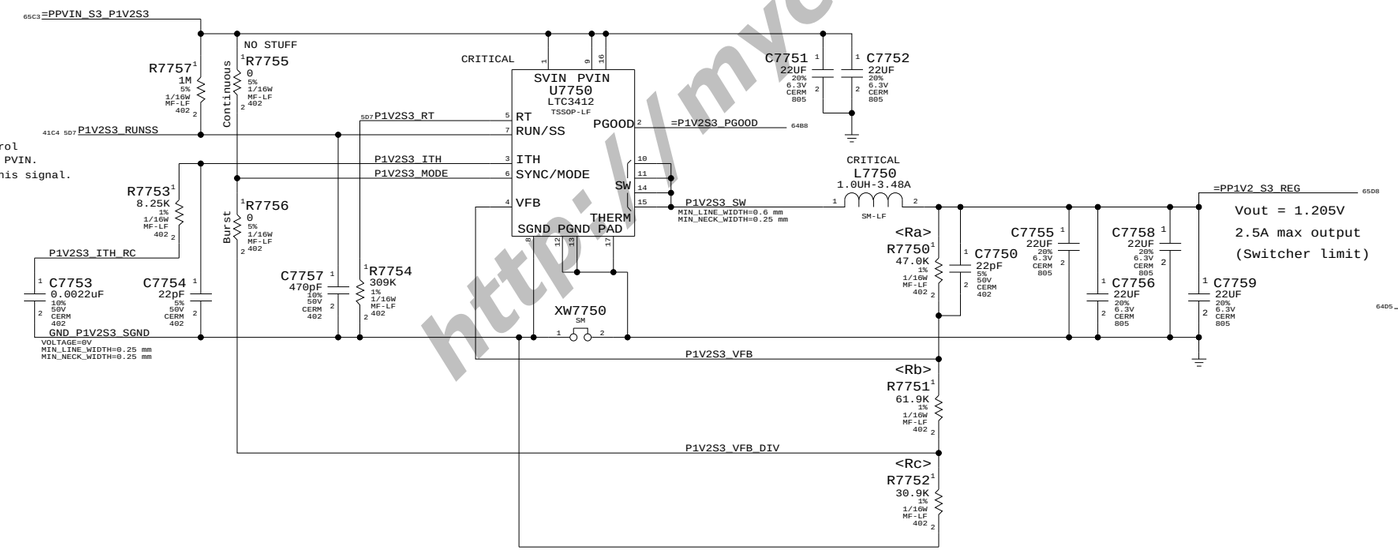
2.5V S0 FET



2.5V D3Cold FET



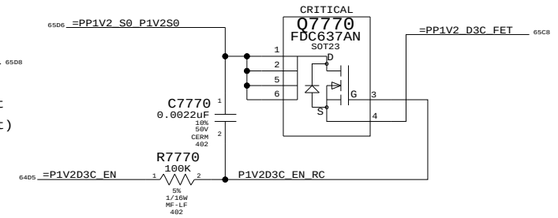
1.2V S3 Regulator



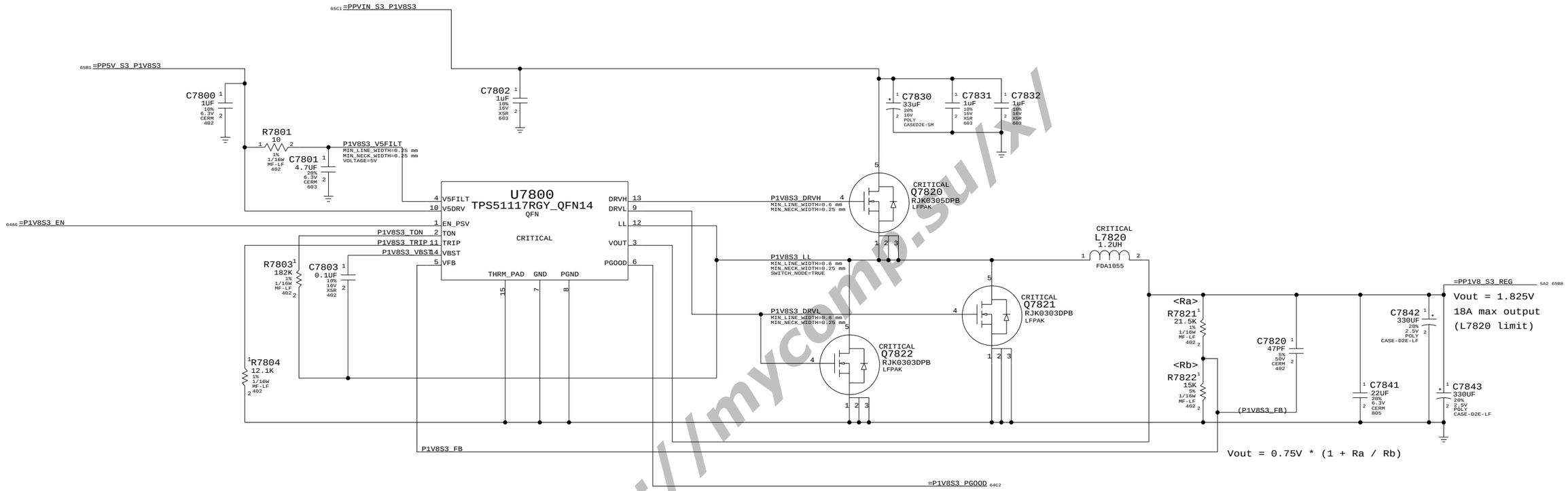
Vout = 0.8V * (1 + Ra / (Rb + Rc))

Connect RUNSS off-page to control
If unconnected, powers up with PVIN.
NOTE: Be aware of pull-up on this signal.

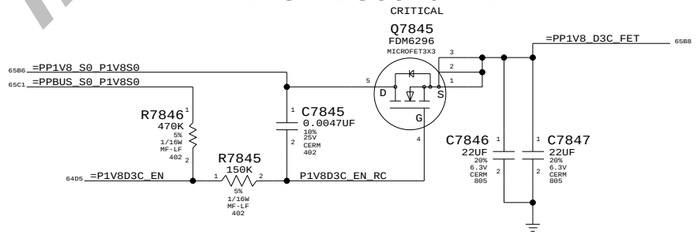
1.2V D3Cold FET



2.5V & 1.2V Regulators		
SYNC_MASTER=M59_MG	SYNC_DATE=05/07/2006	
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7150
	REV: A.0.0	
	SCALE: NONE	SHT 61 OF 84



1.8V D3Cold FET



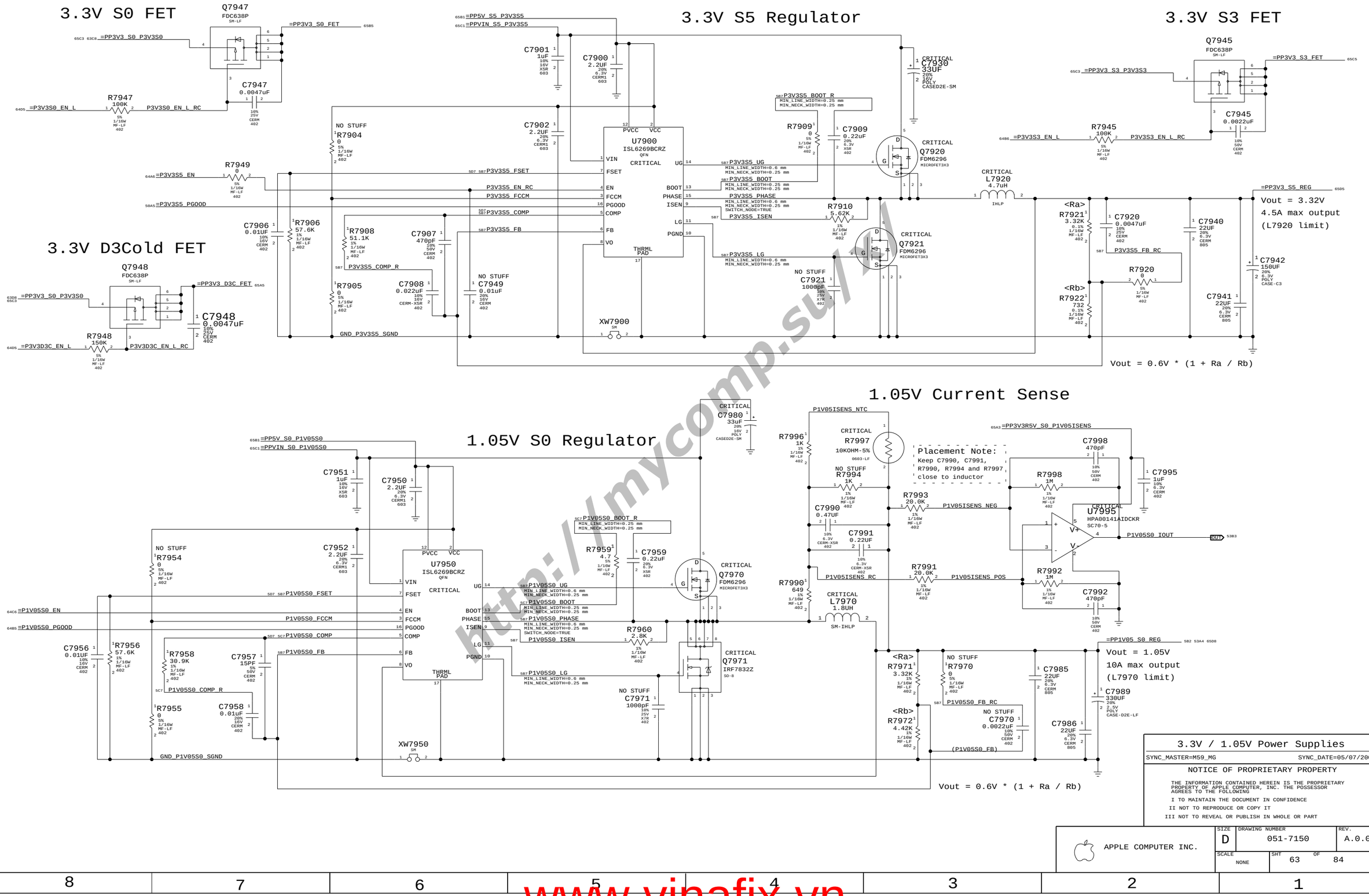
1.8V Supply

SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	62	84



Power Control Signals

65B1 64B8 =PP5V_S5_PWRCTL

R8050 10K 5% 1/16W MF-LF 402
R8051 10K 5% 1/16W MF-LF 402
R8052 10K 5% 1/16W MF-LF 402
R8068 10K 5% 1/16W MF-LF 402
R8069 10K 5% 1/16W MF-LF 402

GPU requires 1.2V, 1.8V, 2.5V and 3.3V rise after VCore is up.

68C8 IN =GPUVCORE_PGOOD

Need to ensure that ISL6269 PGOOD does not deassert while GPU PowerPlay is changing GPU core voltage.

P1V2R2V5D3C_EN_LS5V MAKE_BASE=TRUE
=P2V5D3C_EN 61C3
=P1V2D3C_EN 61B3

P3V3D3C_EN_L MAKE_BASE=TRUE
=P3V3D3C_EN_L 63C8

P1V8D3C_EN MAKE_BASE=TRUE
=P1V8D3C_EN 62A6

1.8V Enable has pull-up to PBUS

Q8055 2N7002DW-X-F SOT-363
Q8056 2N7002DW-X-F SOT-363
Q8050 2N7002DW-X-F SOT-363
Q8058 2N7002DW-X-F SOT-363
Q8058 2N7002DW-X-F SOT-363

PM_SLP_S3_LS5V MAKE_BASE=TRUE
=P2V5S0_EN 61D3
P3V3S0_EN_L MAKE_BASE=TRUE
=P3V3S0_EN_L 63D8

65D3 64A8 =PP3V42_G3H_PWRCTL

PM_SLP_S3_LS5V MAKE_BASE=TRUE
=P5VS0_EN_L 60B3
LIO_P3V3S0_EN_L 5C1 47B6
P1V5S0_RUNSS 5B7 5D7 60C4

1.5V Enable has pull-up to PBUS

Q8050 2N7002DW-X-F SOT-363
R8054 100K 5% 1/16W MF-LF 402
Q8057 2N7002DW-X-F SOT-363
Q8057 2N7002DW-X-F SOT-363

PM_SLP_S3
42A8 23C3 49C5 43B7 IN PM_SLP_S3_L

R8056 100K 5% 1/16W MF-LF 402

(PM_SLP_S3_L) MAKE_BASE=TRUE

=P1V05S0_EN 63B8
=ENET_VMAIN_AVLBL 39C8
=MEMVREF_EN 32B3
=PBUSVSENS_EN 53C3

65A3 =PP3V3_S0_PWRCTL

R8053 10K 5% 1/16W MF-LF 402
R8081 10K 5% 1/16W MF-LF 402

PM_SLP_S3_L_GPUVCORE_EN

C8081 0.1uF 20% 10V CERM 402

C8053 0.047UF 10% 16V CERM 402

TP_SB_GPIO38 SB_GPUVCORE_DISABLE_L MAKE_BASE=TRUE

U8081 MC74VHC1G08 SC70

GPUVCORE_EN MAKE_BASE=TRUE =GPUVCORE_EN 68C8

61C8 IN =P2V5S3_PGOOD
61B5 IN =P1V2S3_PGOOD
TP_P2V5S3_P1V2S3_PGOOD MAKE_BASE=TRUE

This signal was used as an option previously to test for 2v5 and 1v2 S3 valid for GPUVCORE_EN. But was disconnected for C8053 placement.

The SB can turn off the GPUVcore (and by extension all D3Cold rails) by driving GPIO38 low.

65B1 64D8 =PP5V_S5_PWRCTL

R8055 10K 5% 1/16W MF-LF 402

PM_SLP_S4_LS5V MAKE_BASE=TRUE
=P3V3S3_EN_L 63D3
=P5VS3_EN_L 60A4

Q8055 2N7002DW-X-F SOT-363

41B6 23C2 49C6 IN PM_SLP_S4_L

R8057 100K 5% 1/16W MF-LF 402

2.5V S3 and 1.2V S3 supplies are controlled by ethernet power control circuit.

(PM_SLP_S4_L) MAKE_BASE=TRUE
=P1V8S3_EN 62C8
=RTUSB_EN 46C7
LIO_P3V3S3_EN 5C1 47B6

65D3 64C8 =PP3V42_G3H_PWRCTL

50A4 IN P5VS5_PGOOD
(P5VS5_PGOOD) MAKE_BASE=TRUE
=P3V3S5_EN 63D7

R8059 470K 5% 1/16W MF-LF 402

P5VS5_RUNSS 5D7 60C5

5V Enable has pull-up to PBUS

Q8059 2N7002DW-X-F SOT-363

SMC_PM_G2_EN_L

Q8059 2N7002DW-X-F SOT-363

49D5 IN SMC_PM_G2_EN

R8058 100K 5% 1/16W MF-LF 402

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

65A6 =PPVIN_G3H_P3V42G3H

C8000 10UF 10% 25V X5R 1206-1

P3V42G3H5_BOOST

U8000 LT3470 TSOT23-8
VIN BOOST SHDN* SW BIAS NC NC CRITICAL FB GND

C8005 0.22uF 20% 6.3V X5R 402

CRITICAL L8010 33uH CDPH4D19F-SM

P3V42G3H_SW MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm SWITCH_NODE=TRUE

=PP3V42_G3H_REG 65D5

Vout = 3.425
200mA max output
(Switcher limit)

<Ra>
R8010 348K 1% 1/16W MF-LF 402

C8010 22pF 5% 50V CERM 402

5D7 P3V42G3H_FB

<Rb>
R8011 200K 1% 1/16W MF-LF 402

C8015 22UF 20% 6.3V CERM 805

Vout = 1.25V * (1 + Ra / Rb)

1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation

65C3 =PP3V3_S5_P1V5PG
65C6 PP1V5_S0

R8061 27.4K 1% 1/16W MF-LF 402
R8063 4.99K 1% 1/16W MF-LF 402

0.89V Reference

P1V0_P1V5PG_REF
P1V5S0_COMP_POS

U8060 LMC7211 SM-LF

C8060 0.1uF 20% 10V CERM 402

P1V5S0_PGOOD

R8062 10K 1% 1/16W MF-LF 402
R8064 10K 1% 1/16W MF-LF 402

R8065 10K 5% 1/16W MF-LF 402

IMVP_PWRGD_IN OUT 59C7

1.5V Comp threshold set to 1.32V (88%)

63B8 IN =P1V05S0_PGOOD
P1V5P1V05S0_PGOOD MAKE_BASE=TRUE

ISL6269 undervoltage threshold 81-87% (0.85 - 0.91V)
NOTE: R8065 acts as 10K pull-up for PGOOD signal

Unused PGOOD Signals

60B3 =P5VP1V5_PGOOD — TP_P5V_P1V5_PGOOD MAKE_BASE=TRUE
62B4 =P1V8S3_PGOOD — TP_P1V8S3_PGOOD MAKE_BASE=TRUE

Other S0 Rails PWRGD Circuit

Does not include D3C rails for GPU!!

65C3 PP3V3_S0
65B1 PP5V_S0
65A6 PP2V5_S0
65D6 PP0V9_S0

R8074 68.1K 1% 1/16W MF-LF 402
R8072 365K 1% 1/16W MF-LF 402
R8070 845K 1% 1/16W MF-LF 402

C8070 0.1uF 20% 10V CERM 402

R8076 10K 5% 1/16W MF-LF 402

U8070 LTC2903 TSOT-23
V1 V2 V3 V4 GND RST*

CRITICAL

S0PGOOD_5V_DIV
S0PGOOD_2V5_DIV
S0PGOOD_0V9_DIV

S0PGOOD_PWROK 79A4 79D5

R8075 100K 1% 1/16W MF-LF 402
C8075 0.1UF 20% 10V CERM 402

R8073 100K 1% 1/16W MF-LF 402
C8073 0.1UF 20% 10V CERM 402

R8071 100K 1% 1/16W MF-LF 402
C8071 0.1UF 20% 10V CERM 402

LTC2903 guaranteed threshold is 93.5% (3.055V, 4.725V, 2.325V, 0.840V)

=PP3V3_S0_ALLSYSPG 65A3 79D5

U8080 MC74VHC1G08 SC70

79A2 PGOOD_MUXED_S0_OR_S0D3C

ALL_SYS_PWRGD OUT 26A5 49D7

C8080 0.1UF 20% 10V CERM 402

3.3V G3Hot Supply & Power Control

SYNC_MASTER=M59_MG SYNC_DATE=08/01/2006

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-7150 | REV. A.0.0
SCALE NONE | SHT 64 OF 84

"S3AC" rail is ON in S3 on AC, OFF in S3 on battery

PP0V9_S0
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0.9V
MAKE_BASE=TRUE
64B5
31C2 =PP0V9_S0_MEMVTT_LDO
=PP0V9_S0_MEM_TERM 30D5

PP1V05_S0
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE
63A2 53A4 5B2 =PP1V05_S0_REG
=PP1V05_S0_CPU 7B5 7B6 7D5 8C7 9B7 11B3 11C5
=PP1V05_S0_FSB_NB 12A7 12B7 12C2 19D7 34B8 34C6 34C8
=PP1V05_S0_NB_CRT 19D6 19D7
=PP1V05_S0_NB_VTT 17D3 19C8 19D7
=PP1V05_S0_SB_CPU_IO 21C1 24C3 25C4
=PPVCORE_S0_NB 16C8 16D3 19C8 19D2 19D7
=PPVCORE_S0_SB 24D3 25D3

PP1V2_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.22 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
61B3 =PP1V2_S3_REG
=PP1V2_S3_ENET 39A8 39D7
=PP1V2_S0_P1V2S0 61B3

PP1V2_D3C
79D7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
61B1 =PP1V2_D3C_FET
=PP1V2_S0_GPU_VDDPLL 74B8
=PP1V2_S0_PCIE_GPU 67A1
=PP1V2_S0_PCIE_GPU_PVDD 67C7
=PP1V2_S0_PCIE_GPU_VDDR 67C7

PP1V5_S0
64C5
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0
MAKE_BASE=TRUE
60C1 5A2 =PP1V5_S0_REG
=PP1V5_S0_CPU 8B7 9B7
=PP1V5_S0_NB1V5_SENSE 60A8
=PP1V5_S0_SB 25A8 25C8
=PP1V5_S0_SB_VCC1_5_A 24A3 25C2
=PP1V5_S0_SB_VCC1_5_A_ARX 24B5 25D6
=PP1V5_S0_SB_VCC1_5_A_ATX 24A5 25C6
=PP1V5_S0_SB_VCC1_5_A_USB_CORE 24A3 25B2
=PP1V5_S0_SB_VCCSATAPLL 24B5 25D6
=PP1V5_S0_SB_VCCUSBPLL 24A5 25B6
=PP1V5_S0_LIO 5D1 47D6
=PP1V5_S0_ITPMOUNT 11C4

PP1V5_S0_NB
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0
MAKE_BASE=TRUE
65C6 68A7 19D7 =PP1V5_S0_NB
=PP1V5_S0_NB 19D7 68A7 65C8
=PP1V5_S0_NB_3G 19B5 19D7
=PP1V5_S0_NB_3GPLL 19B5 19D7
=PP1V5_S0_NB_PCIE 13D2 19D7
=PP1V5_S0_NB_PLL 19B8 19D7
=PP1V5_S0_NB_VCCD_LVDS 17C6 19A5
=PP1V5_S0_NB_TVDAC 19D2 19D6 19D7
=PP1V5_S0_NB_VCCAUX 16D1 17B6 19C4 19D7
=PP1V5_S0_NB_VCCD_HMPLL 17C6 19D7

PP1V8_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
62C1 5A2 =PP1V8_S3_REG
=PP1V8_S3_MEM 28B2 28D3 28D6 29B2 29D3 29D6
=PP1V8_S3_MEM_NB 14C2 16B6 19D7
=PP1V8_S3_MEMVREF 32C6
=PP1V8_S0_MEMVTT 31C5
=PP1V8_S0_P1V8S0 62A6
=PP1V8_S3_FW 37B2

PP1V8_D3C
79D7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
MAKE_BASE=TRUE
62A4 =PP1V8_D3C_FET
=PP1V8R2V0_S0_FB_GPU 69B8 70A5 70A8 70B5 70B8
=PP1V8_S0_FB_VDD 72D5 72D8 73D5 73D8
=PP1V8_S0_FB_VDDQ 72D5 72D8 73D5 73D8

PP2V5_S3
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE
61D4 =PP2V5_S3_REG
=PP2V5_S3_ENET 39D3
=PP2V5_S0_P2V5S0 61C3 61D3

PP2V5_S0
64B5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=2.5V
MAKE_BASE=TRUE
61D1 =PP2V5_S0_FET
=PP2V5_S0_NB_VCCA_3GBG 17D6 19C5 19D7
=PP2V5_S0_NB_VCC_TXLVDS 17D6 19A6 19D7
=PP2V5_S0_NB_VCCA_LVDS 17C6 19A4
=PP2V5_S0_NB_DPLL 19A8
=PP2V5_S0_LVDS_MUX 79C5 79D3

PP2V5_D3C
79D7
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0
MAKE_BASE=TRUE
61C1 =PP2V5_D3C_FET
=PP2V5_S0_GPU 75C8
=PP2V5_S0_GPU_PVDD 74A8
=PP2V5_S0_GPU_VDD25 74C6
=PP2V5_S0_GPU_VDDC_CT 74C6

PPVCORE_D3C_GPU
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.2V
MAKE_BASE=TRUE
68C1 =PPVCORE_S0_GPU_REG
=PPVCORE_S0_GPU 53A5 53C7 69D8 74A7
=PPVCORE_S0_GPU_BBP 68B7

PPDCIN_G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=18.5V
MAKE_BASE=TRUE
47C6 5D1 =PPDCIN_G3H_LIO
=PPVIN_G3H_P3V42G3H 64D5

GND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=0V

PP3V42_G3H
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.425V
MAKE_BASE=TRUE
64D2 =PP3V42_G3H_REG
=PP3V42_G3H_SMCVREF 50B7
=PP3V42_G3H_SMBUS_SMC_BSA 27C3
=PP3V42_G3H_PWRCTL 64A8 64C8
=PP3V42_G3H_SB_RTC 26D6
=PP3V42_G3H_SMC_PWRGD 50B5
=PP3V42_G3H_SMC_CLK 35B7
=PP3V42_G3H_LIO 5D1 47D6
=PP3V42_G3H_LIDSWITCH 78D3
=PP3V3_S5_SMC 49C2 49D3 49D4 50B1 50D7
=PP3V3_S5_LPCPLUS 5D2 51C4
=PP3V42_G3H_SMCUSBMUX 46B5

PP3V3_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
63D1 =PP3V3_S5_REG
=PP3V3_S5_SB 23A7 23B7 23D4 23D8 25C8
=PP3V3_S5_SB_3V3_1V5_VCCSUSHDA 24C3
=PP3V3_S5_SB_IO 22C6
=PP3V3_S5_SB_PM 11B5 23D1 26C5
=PP3V3_S5_SB_USB 22D8
=PP3V3_S5_SB_VCCSUS3_3 24A5 24B3 25B6 25D2
=PP3V3_S5_SB_VCCSUS3_3_USB 24B3 25D2
=PP3V3_S5_ROM 54D4
=PP3V3_S5_P1V5PG 64C5
=PP3V3_S3_P3V3S3 62D2
=PPVIN_S3_P2V5S3 61D8
=PP3V3_S0_LCD 76D5
=PP3V3_S0_P3V3S0 63C8 63D8

PP3V3_S3
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
63D1 =PP3V3_S3_FET
=PP3V3_S3_P3V3S3AC 41C5
=PP3V3_S3_RTALS 55D4
=PP3V3_S3_SMBUS_SMC_A_S3 27C5
=PP3V3_S3_TPM 50B1 58C2
=PP3V3_S3_SMS 50B1 57C6
=PP3V3_S3_TOPCASE 78D3
=PP3V3_S3_LTALS 5B2 78C5
=PP3V3_S3_MEMVREF 32C5
=PP3V3_S3_FW 37A7 37C3 37D7
=PP3V3_S3_PCI 37D5
=PPVIN_S3_P1V2S3 61B7
=PP3V3_S3_PWRCTL 64C6

PP3V3_S0
64B5
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
63D6 =PP3V3_S0_FET
=PP3V3_S0_DDC_LCD 76D3
=PP3V3_S0_CK410 33C7 33D3 33D8 34A8
=PP3V3_S0_IDE 36D6
=PP3V3_S0_IMVP6 59D8
=PP3V3_S0_INVERTER 76A8
=PP3V3_S0_NB 14C7 14D6 19C7 20A4 20B4
=PP3V3_S0_NB_VCC_HV 17C6 19C6 19C7
=PP3V3_S0_SB 22B5 25D8
=PP3V3_S0_SB_3V3_1V5_VCCHDA 24C3 25C4
=PP3V3_S0_SB_GPIO 21C3 21D3 23B3 23D5
=PP3V3_S0_SB_PCI 26D1
=PP3V3_S0_SB_PM 26B6 26B8
=PP3V3_S0_SB_VCC3_3 24B5 25B8 25C6
=PP3V3_S0_SB_VCC3_3_IDE 24C3 25B4
=PP3V3_S0_SB_VCC3_3_PCI 24B3 25A4
=PP3V3_S0_SB_VCCLAN3_3 24D3 25D3
=PP3V3_S0_TPM 58C7 58D4
=PP3V3_S0_KBDLED 55B6
=PP3V3_S0_THRM_SNR 10C5
=PP3V3_S0_REMTHMSNS 52D4
=PP3V3_S0_SMBUS_SB 27D8
=PP3V3_S0_SMBUS_SMC_0_S0 27D5
=PP3V3_S0_SMBUS_SMC_B_S0 27D3
=PP3V3_S0_SMBUS_SMC_BSB 27C3
=PP3V3_S0_RSTBUF 26B4
=PP3V3_S0_SMC_LS 50D3
=PP3V3_S0_ALLSYSPG 64B1 79D5
=PP3V3_S0_FAN_LT 56C7
=PP3V3_S0_FAN_RT 56C4
=PP3V3R5V_S0_CPUISENS 59A5
=PP3V3R5V_S0_GPUISENS 68D2
=PP3V3R5V_S0_P1V05ISENS 63B3
=PPSPD_S0_MEM 28A6 29A3 29A6
=PP3V3_S0_EDET 40B6
=PP3V3_S0_LVDS_MUX 79A4 79B3 79C6
=PP3V3_S0_NB1V5ISENS 60A6
=PP3V3_S0_GPU_TDIODE 52B5
=PP3V3_S0_PWRCTL 64B6

PP3V3_D3C
79D7
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
63C7 =PP3V3_D3C_FET
=PP3V3_S0_GPU 68C4 74D2
=PP3V3_S0_GPUBBP 68B8
=PP3V3_S0_GPUBBN 68A4
=PP3V3_S0_GPU_VDDR3 74C6
=PP3V3_D3C_GPU_GPIOS 71D6
=PP1V8R3V3_S0_GPU_VDDR4 74B7
=PP1V8R3V3_S0_GPU_VDDR5 74B7
=PP3V3_D3C_DDC_DVI 77B2
=PP3V3_D3C_VGASYNC 77D5
=PP3V3_D3C_GPU_LVDS_DDC 79A7
=PP3V3_D3C_GPU 71B2

PP3V3_S3AC
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.22 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
41C4 =PP3V3_S3AC_FET
=PP3V3_S3_ENET 39A5 39B4 39B5 39B8 39D6 39D8

PNBB_S0_GPU
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=-0.7V
MAKE_BASE=TRUE
68A2 =PNVOUT_S0_GPUBBN_REG
=PNBB_S0_GPU 69D2

PPBB_S0_GPU
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.9V
MAKE_BASE=TRUE
68B5 =PPVOUT_S0_GPUBBP_LDO
=PPBB_S0_GPU 69D6

PPVCORE_S0_CPU
5A2
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.1V
MAKE_BASE=TRUE
59D1 =PPVOUT_S0_IMVP6_REG
=PPVCORE_S0_CPU 8B5 8D7 9D7 53A6 53D7

PPBUS_G3H
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
53D3
66C4 5A1 =PPBUS_G3H_LIO_CONN
=PPBUS_G3H_S3AC 41C6
=PPVIN_S5_P5VP1V5 60D7
=PPVIN_S0_IMVP6 59D4 59D7
=PPVIN_S5_P3V3S5 63D6
=PPBUS_S5_FWPWRSW 43D7
=PPVIN_S3_P1V8S3 62D7
=PPVIN_S0_P1V05S0 63B7
=PPVIN_S0_GPUVCORE 68D7
=PPBUS_S0_INVERTER 76B7
=PPBUS_S0_P1V8S0 62A6
=PPBUS_S0_PPBU_S0_FW 42B8

PPBUS_S5_FW_FET
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.3 mm
VOLTAGE=33V
MAKE_BASE=TRUE
43C1 =PPBUS_S5_FW_FET
=PPFW_PORT1_VP 44D3
=PPFW_PORT2_VP 44B3
=PPFW_FW_CPS 38B7
=PPFW_P3V3FWPHY 42C8

PP5V_S5
50B5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
60C8 =PP5V_S5_REG
=PP5V_S5_SB 25C8
=PP5V_S5_P3V3S5 63D6
=PP5V_S5_P5VP1V5_VCC 60B6
=PP5V_S5_LIO 5D1 47C6
=PP5V_S5_PWRCTL 64B8 64D8
=PP5V_S3_P5VS3 60A4
=PP5V_S3_P1V8S3 62C8
=PP5V_S3_RTUSB 46C7
=PP5V_S0_P5VS0 60B2
=PP5V_S0_GPUVCORE 68D7
=PP5V_S0_P1V05S0 63B7

PP5V_S3
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
60A2 =PP5V_S3_FET
=PP5V_S3_SYSLED 50B8
=PP5V_S3_CAMERA 5A4 45C3
=PP5V_S3_IR 78B5
=PP5V_S3_TOPCASE 78D3

PP5V_S0
64B5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
MAKE_BASE=TRUE
60B1 =PP5V_S0_FET
=PP5V_S0_DVI_DDC 77B5
=PP5V_S0_IDE 36D6
=PP5V_S0_HDD 78B5
=PP5V_S0_IMVP6 59D7
=PP5V_S0_INVERTER 76B8
=PP5V_S0_MEMVTT 31C5
=PP5V_S0_SB 25D8
=PP5V_S0_FAN_LT 5D2 56C7
=PP5V_S0_FAN_RT 56C4
=PP5V_S0_KBDLED 55B5
=PP5V_S0_GPUBBCTL 68A6
=PP5V_S0_LPCPLUS 5D2 51C4
=PP5V_S0_AUDIO_XW 47D3
=PP5V_S0_ISENSECAL 5A2 53A8
=PP5V_S0_SB_HPD 77A1

Power Aliases

SYNC_MASTER=M59_MG SYNC_DATE=05/07/2006

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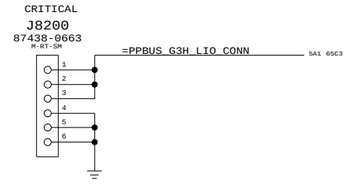
APPLE COMPUTER INC.

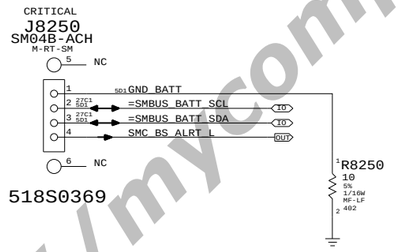
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 65 OF 84	

Left I/O Power Connector



518S0458

Battery Connector (Digital Signals)



518S0369

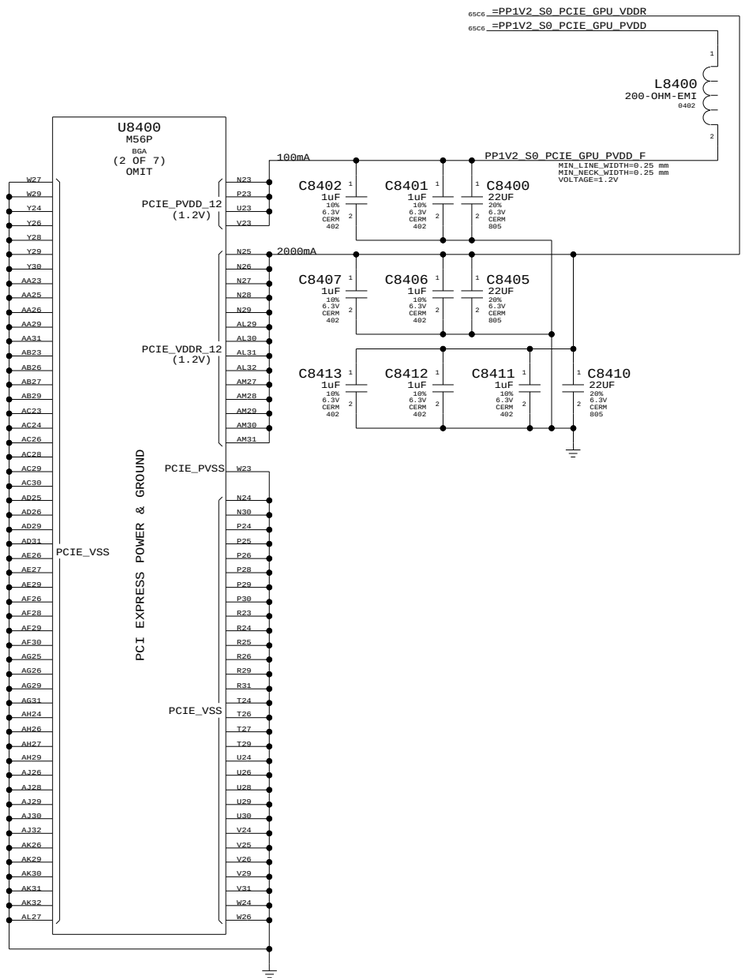
PBus-In,Batt. & 3G Pwr Connectors

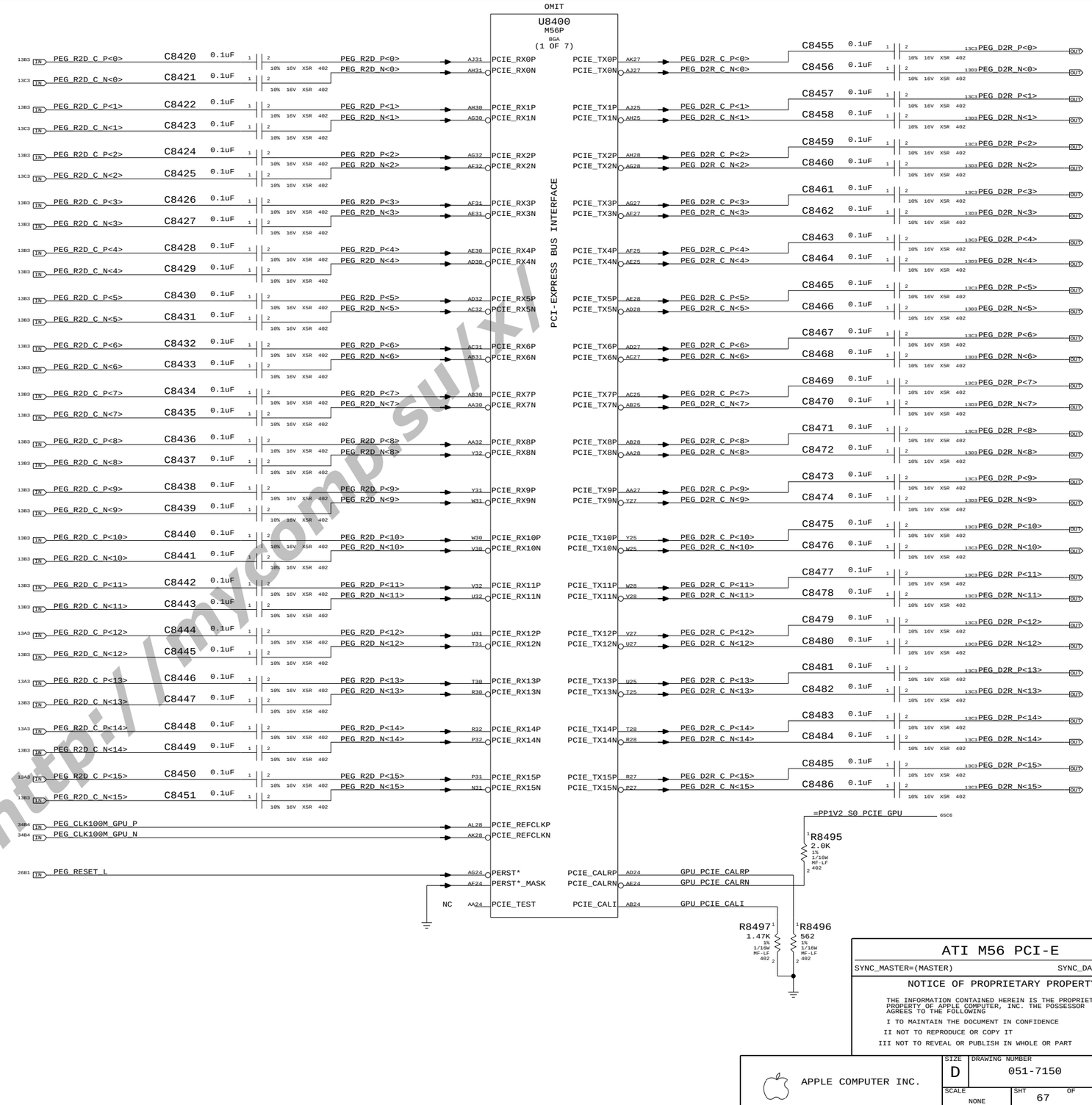
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	66	84





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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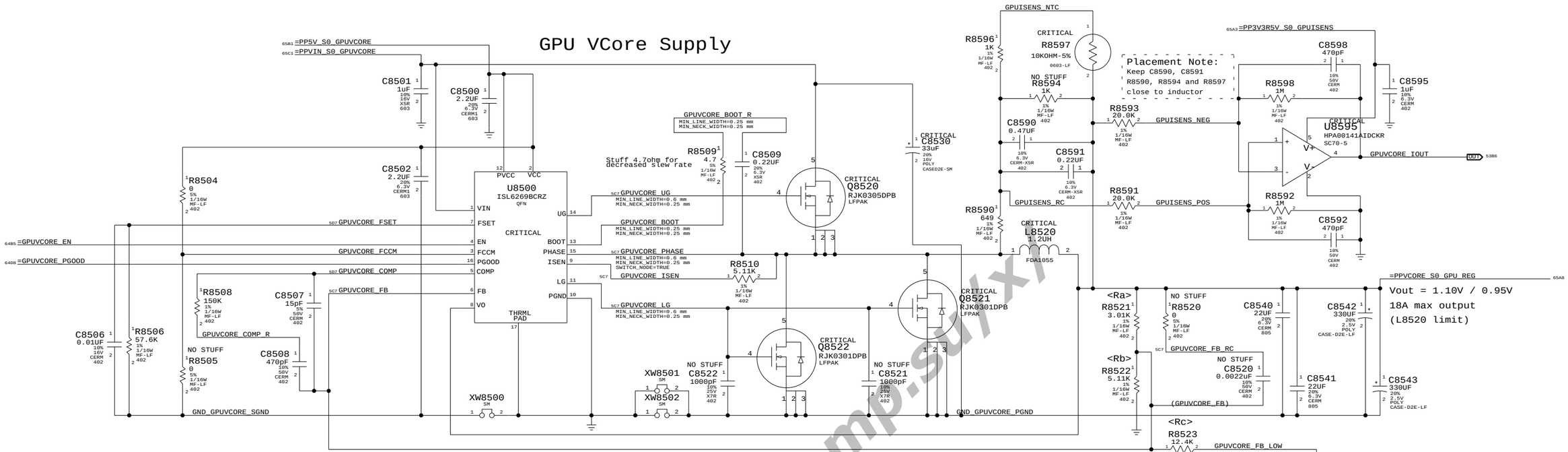
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 67 OF 84	

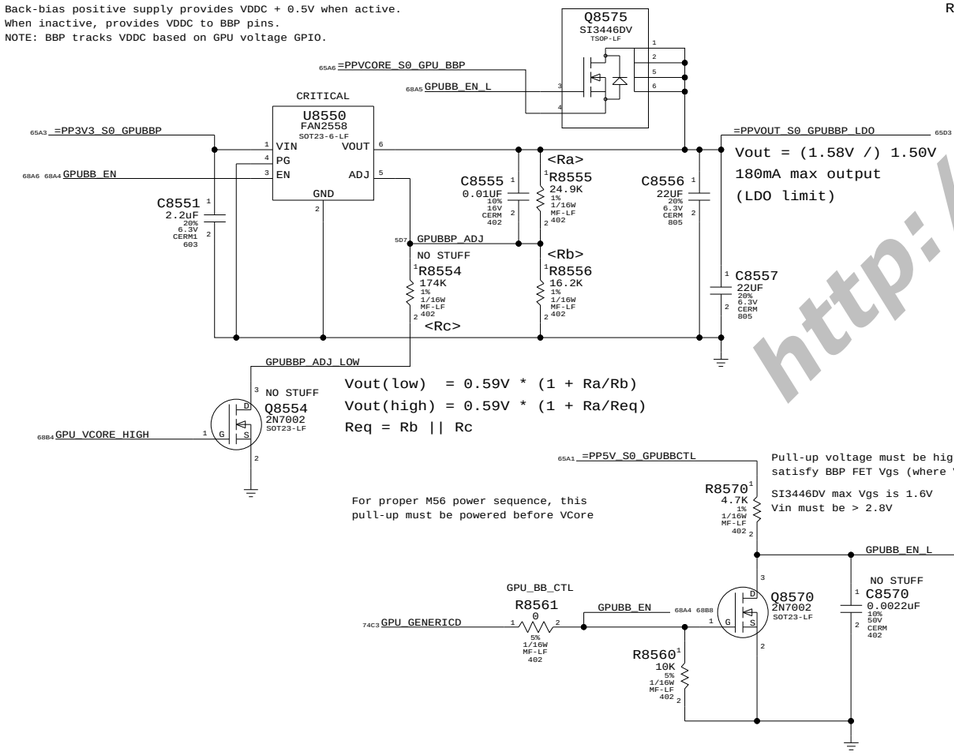
GPU VCore Current Sense

GPU VCore Supply



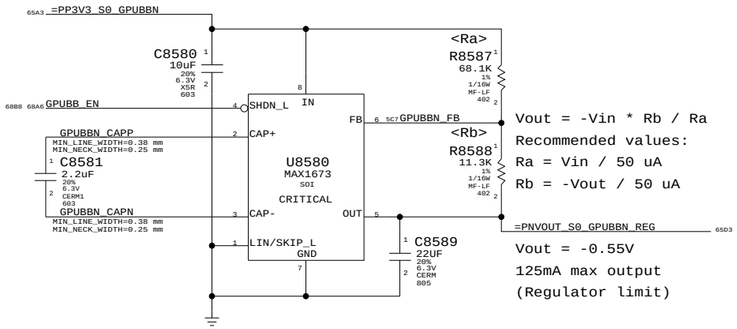
Back-Bias Positive Supply

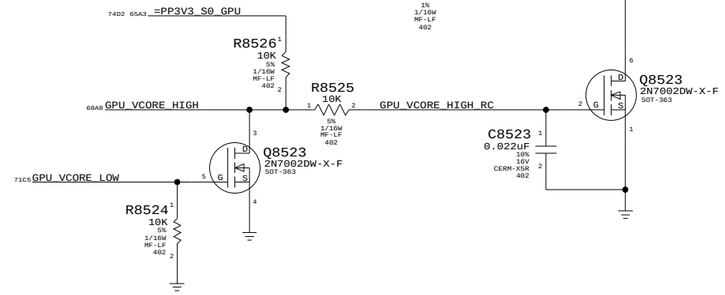
Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.



Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.55V when active.
When inactive, provides VSS to BBN pins.





GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

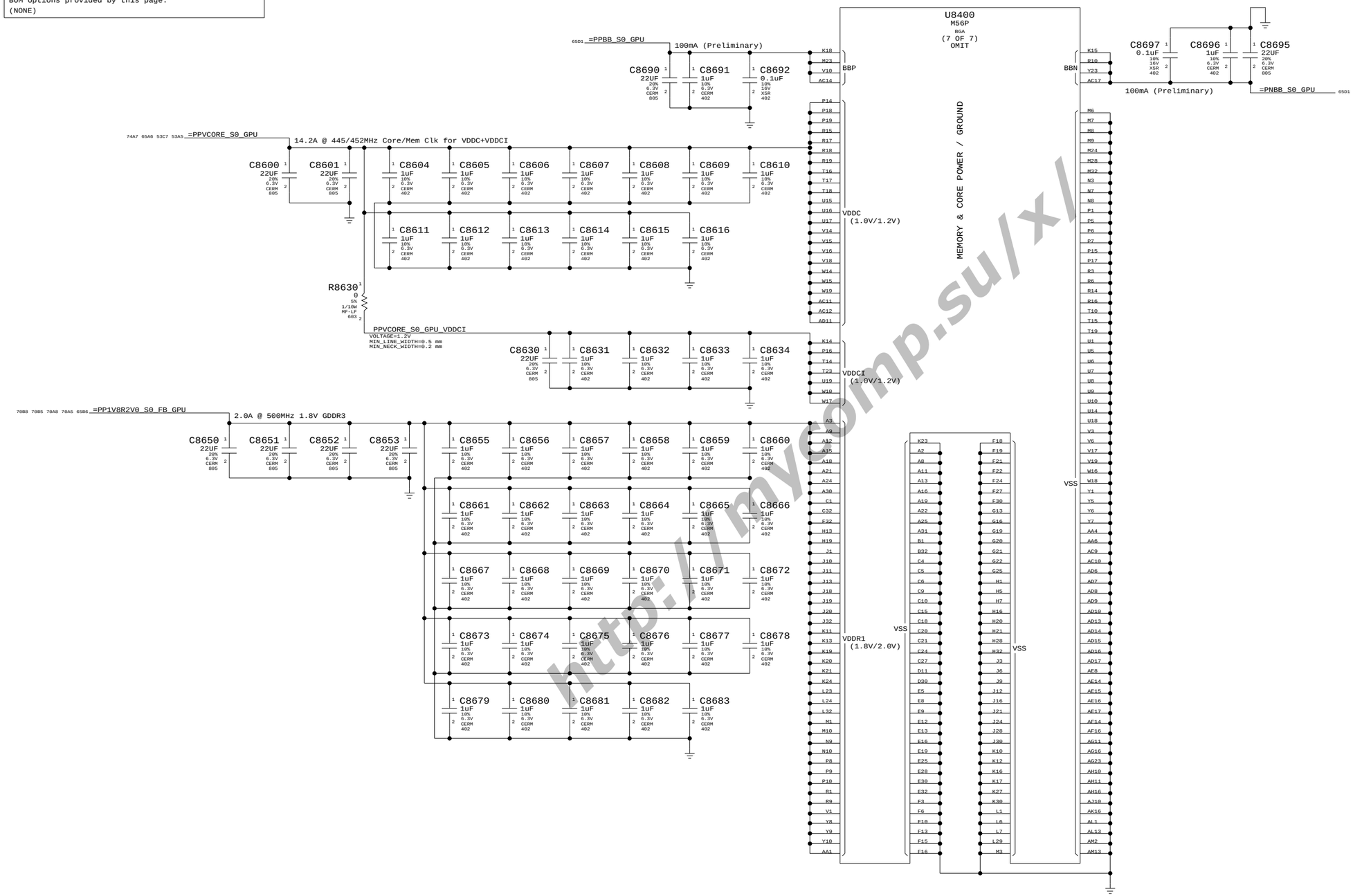
SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 68 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 69 OF 84	

Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U8400
M56P
BGA
(3 OF 7)

MEMORY INTERFACE A

FB_A_DQ<0>	M31	DQA_0	
FB_A_DQ<1>	M30	DQA_1	
FB_A_DQ<2>	L31	DQA_2	
FB_A_DQ<3>	L30	DQA_3	
FB_A_DQ<4>	H30	DQA_4	
FB_A_DQ<5>	G31	DQA_5	
FB_A_DQ<6>	G30	DQA_6	
FB_A_DQ<7>	F31	DQA_7	
FB_A_DQ<8>	M27	DQA_8	
FB_A_DQ<9>	M29	DQA_9	
FB_A_DQ<10>	L28	DQA_10	
FB_A_DQ<11>	L27	DQA_11	
FB_A_DQ<12>	J27	DQA_12	
FB_A_DQ<13>	H29	DQA_13	
FB_A_DQ<14>	G29	DQA_14	
FB_A_DQ<15>	G27	DQA_15	
FB_A_DQ<16>	M26	DQA_16	
FB_A_DQ<17>	L26	DQA_17	
FB_A_DQ<18>	M25	DQA_18	
FB_A_DQ<19>	L25	DQA_19	
FB_A_DQ<20>	J25	DQA_20	
FB_A_DQ<21>	G28	DQA_21	
FB_A_DQ<22>	H27	DQA_22	
FB_A_DQ<23>	H26	DQA_23	
FB_A_DQ<24>	F26	DQA_24	
FB_A_DQ<25>	G26	DQA_25	
FB_A_DQ<26>	H25	DQA_26	
FB_A_DQ<27>	H24	DQA_27	
FB_A_DQ<28>	H23	DQA_28	
FB_A_DQ<29>	H22	DQA_29	
FB_A_DQ<30>	J23	DQA_30	
FB_A_DQ<31>	J22	DQA_31	
FB_A_DQ<32>	E23	DQA_32	
FB_A_DQ<33>	D22	DQA_33	
FB_A_DQ<34>	D23	DQA_34	
FB_A_DQ<35>	E22	DQA_35	
FB_A_DQ<36>	E20	DQA_36	
FB_A_DQ<37>	F20	DQA_37	
FB_A_DQ<38>	D19	DQA_38	
FB_A_DQ<39>	D18	DQA_39	
FB_A_DQ<40>	B19	DQA_40	
FB_A_DQ<41>	B18	DQA_41	
FB_A_DQ<42>	C17	DQA_42	
FB_A_DQ<43>	B17	DQA_43	
FB_A_DQ<44>	C14	DQA_44	
FB_A_DQ<45>	B14	DQA_45	
FB_A_DQ<46>	C13	DQA_46	
FB_A_DQ<47>	B13	DQA_47	
FB_A_DQ<48>	D17	DQA_48	
FB_A_DQ<49>	E18	DQA_49	
FB_A_DQ<50>	E17	DQA_50	
FB_A_DQ<51>	F17	DQA_51	
FB_A_DQ<52>	E15	DQA_52	
FB_A_DQ<53>	E14	DQA_53	
FB_A_DQ<54>	F14	DQA_54	
FB_A_DQ<55>	D13	DQA_55	
FB_A_DQ<56>	H18	DQA_56	
FB_A_DQ<57>	H17	DQA_57	
FB_A_DQ<58>	G18	DQA_58	
FB_A_DQ<59>	G17	DQA_59	
FB_A_DQ<60>	G15	DQA_60	
FB_A_DQ<61>	G14	DQA_61	
FB_A_DQ<62>	H14	DQA_62	
FB_A_DQ<63>	J14	DQA_63	

MAA_0	D26	FB_A_MA<0>	OUT
MAA_1	F28	FB_A_MA<1>	OUT
MAA_2	D28	FB_A_MA<2>	OUT
MAA_3	D25	FB_A_MA<3>	OUT
MAA_4	E24	FB_A_MA<4>	OUT
MAA_5	E26	FB_A_MA<5>	OUT
MAA_6	D27	FB_A_MA<6>	OUT
MAA_7	F25	FB_A_MA<7>	OUT
MAA_8	C26	FB_A_MA<8>	OUT
MAA_9	B26	FB_A_MA<9>	OUT
MAA_10	D29	FB_A_MA<10>	OUT
MAA_11	B27	FB_A_MA<11>	OUT
MAA_12	E27	TP_FB_A_MA12	OUT
MAA_13	E29	FB_A_BA<2>	OUT
MAA_14	B25	FB_A_BA<0>	OUT
MAA_15	C25	FB_A_BA<1>	OUT

READ STROBE

DQMA_0	H31	FB_A_DQM_L<0>	IO
DQMA_1	J29	FB_A_DQM_L<1>	IO
DQMA_2	J26	FB_A_DQM_L<2>	IO
DQMA_3	G23	FB_A_DQM_L<3>	IO
DQMA_4	E21	FB_A_DQM_L<4>	IO
DQMA_5	B15	FB_A_DQM_L<5>	IO
DQMA_6	D14	FB_A_DQM_L<6>	IO
DQMA_7	J17	FB_A_DQM_L<7>	IO
QSA_0	J31	FB_A_RDQS<0>	IN
QSA_1	K29	FB_A_RDQS<1>	IN
QSA_2	K25	FB_A_RDQS<2>	IN
QSA_3	F23	FB_A_RDQS<3>	IN
QSA_4	D20	FB_A_RDQS<4>	IN
QSA_5	B16	FB_A_RDQS<5>	IN
QSA_6	D16	FB_A_RDQS<6>	IN
QSA_7	H15	FB_A_RDQS<7>	IN

WRITE STROBE

QSA_0*	K31	FB_A_WDQS<0>	OUT
QSA_1*	K28	FB_A_WDQS<1>	OUT
QSA_2*	K26	FB_A_WDQS<2>	OUT
QSA_3*	G24	FB_A_WDQS<3>	OUT
QSA_4*	D21	FB_A_WDQS<4>	OUT
QSA_5*	C16	FB_A_WDQS<5>	OUT
QSA_6*	D15	FB_A_WDQS<6>	OUT
QSA_7*	J15	FB_A_WDQS<7>	OUT

CLKA0	D31	FB_A_CLK_P<0>	OUT
CLKA0*	E31	FB_A_CLK_N<0>	OUT
CSA0_0*	B29	FB_A_CS_L<0>	OUT
CSA0_1*	C28	NC	
CKEA0	B30	FB_A_CKE<0>	OUT
RASA0*	B28	FB_A_RAS_L<0>	OUT
CASA0*	C29	FB_A_CAS_L<0>	OUT
WEA0*	B31	FB_A_WE_L<0>	OUT
ODTA0	F29	TP_FB_A_ODT<0>	OUT
CLKA1	B20	FB_A_CLK_P<1>	OUT
CLKA1*	C19	FB_A_CLK_N<1>	OUT
CSA1_0*	B23	FB_A_CS_L<1>	OUT
CSA1_1*	C23	NC	
CKEA1	C22	FB_A_CKE<1>	OUT
RASA1*	B24	FB_A_RAS_L<1>	OUT
CASA1*	B22	FB_A_CAS_L<1>	OUT
WEA1*	B21	FB_A_WE_L<1>	OUT
ODTA1	D24	TP_FB_A_ODT<1>	OUT

=PP1V8R2V0_S0_FB_GPU

R8710 40.2 1% 1/16W MF-LF 402
R8712 40.2 1% 1/16W MF-LF 402
R8711 100 1% 1/16W MF-LF 402
C8711 0.1uF 10% 16V X5R 402
R8713 100 1% 1/16W MF-LF 402
C8713 0.1uF 10% 16V X5R 402

GPU_MVREFD0
GPU_MVREFS0
MVREFD_0
MVREFS_0
VDDRH0 (1.8V/ 2.0V)
VSSRH0

=PP1V8R2V0_S0_FB_GPU

L8715 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V
PP1V8R2V0_S0_GPU_VDDRH0

C8715 1uF 10% 6.3V CERM 402
C8716 1uF 10% 6.3V CERM 402

XW8715 SM
GND_GPU_VSSRH0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

OMIT
U8400
M56P
BGA
(4 OF 7)

MEMORY INTERFACE B

FB_B_DQ<0>	B12	DQB_0	
FB_B_DQ<1>	C12	DQB_1	
FB_B_DQ<2>	B11	DQB_2	
FB_B_DQ<3>	C11	DQB_3	
FB_B_DQ<4>	C8	DQB_4	
FB_B_DQ<5>	B7	DQB_5	
FB_B_DQ<6>	C7	DQB_6	
FB_B_DQ<7>	B6	DQB_7	
FB_B_DQ<8>	F12	DQB_8	
FB_B_DQ<9>	D12	DQB_9	
FB_B_DQ<10>	E11	DQB_10	
FB_B_DQ<11>	F11	DQB_11	
FB_B_DQ<12>	F9	DQB_12	
FB_B_DQ<13>	D8	DQB_13	
FB_B_DQ<14>	D7	DQB_14	
FB_B_DQ<15>	F7	DQB_15	
FB_B_DQ<16>	G12	DQB_16	
FB_B_DQ<17>	G11	DQB_17	
FB_B_DQ<18>	H12	DQB_18	
FB_B_DQ<19>	H11	DQB_19	
FB_B_DQ<20>	H9	DQB_20	
FB_B_DQ<21>	E7	DQB_21	
FB_B_DQ<22>	F8	DQB_22	
FB_B_DQ<23>	G8	DQB_23	
FB_B_DQ<24>	G6	DQB_24	
FB_B_DQ<25>	G7	DQB_25	
FB_B_DQ<26>	H8	DQB_26	
FB_B_DQ<27>	J8	DQB_27	
FB_B_DQ<28>	K8	DQB_28	
FB_B_DQ<29>	L8	DQB_29	
FB_B_DQ<30>	K9	DQB_30	
FB_B_DQ<31>	L9	DQB_31	
FB_B_DQ<32>	K5	DQB_32	
FB_B_DQ<33>	L4	DQB_33	
FB_B_DQ<34>	K4	DQB_34	
FB_B_DQ<35>	L5	DQB_35	
FB_B_DQ<36>	N5	DQB_36	
FB_B_DQ<37>	N6	DQB_37	
FB_B_DQ<38>	P4	DQB_38	
FB_B_DQ<39>	R4	DQB_39	
FB_B_DQ<40>	P2	DQB_40	
FB_B_DQ<41>	R2	DQB_41	
FB_B_DQ<42>	T3	DQB_42	
FB_B_DQ<43>	T2	DQB_43	
FB_B_DQ<44>	W3	DQB_44	
FB_B_DQ<45>	W2	DQB_45	
FB_B_DQ<46>	Y3	DQB_46	
FB_B_DQ<47>	Y2	DQB_47	
FB_B_DQ<48>	T4	DQB_48	
FB_B_DQ<49>	R5	DQB_49	
FB_B_DQ<50>	T5	DQB_50	
FB_B_DQ<51>	T6	DQB_51	
FB_B_DQ<52>	V5	DQB_52	
FB_B_DQ<53>	W5	DQB_53	
FB_B_DQ<54>	W6	DQB_54	
FB_B_DQ<55>	Y4	DQB_55	
FB_B_DQ<56>	R8	DQB_56	
FB_B_DQ<57>	T8	DQB_57	
FB_B_DQ<58>	R7	DQB_58	
FB_B_DQ<59>	T7	DQB_59	
FB_B_DQ<60>	V7	DQB_60	
FB_B_DQ<61>	W7	DQB_61	
FB_B_DQ<62>	W8	DQB_62	
FB_B_DQ<63>	W9	DQB_63	

MAB_0	G4	FB_B_MA<0>	OUT
MAB_1	E6	FB_B_MA<1>	OUT
MAB_2	E4	FB_B_MA<2>	OUT
MAB_3	H4	FB_B_MA<3>	OUT
MAB_4	J5	FB_B_MA<4>	OUT
MAB_5	G5	FB_B_MA<5>	OUT
MAB_6	F4	FB_B_MA<6>	OUT
MAB_7	H6	FB_B_MA<7>	OUT
MAB_8	G3	FB_B_MA<8>	OUT
MAB_9	G2	FB_B_MA<9>	OUT
MAB_10	D4	FB_B_MA<10>	OUT
MAB_11	F2	FB_B_MA<11>	OUT
MAB_12	F5	TP_FB_B_MA12	OUT
MAB_13	D5	FB_B_BA<2>	OUT
MAB_14	H2	FB_B_BA<0>	OUT
MAB_15	H3	FB_B_BA<1>	OUT

READ STROBE

DQMB_0	B8	FB_B_DQM_L<0>	IO
DQMB_1	D9	FB_B_DQM_L<1>	IO
DQMB_2	G9	FB_B_DQM_L<2>	IO
DQMB_3	K7	FB_B_DQM_L<3>	IO
DQMB_4	M5	FB_B_DQM_L<4>	IO
DQMB_5	V2	FB_B_DQM_L<5>	IO
DQMB_6	W4	FB_B_DQM_L<6>	IO
DQMB_7	T9	FB_B_DQM_L<7>	IO
QSB_0	B9	FB_B_RDQS<0>	IN
QSB_1	D10	FB_B_RDQS<1>	IN
QSB_2	H10	FB_B_RDQS<2>	IN
QSB_3	K6	FB_B_RDQS<3>	IN
QSB_4	N4	FB_B_RDQS<4>	IN
QSB_5	U2	FB_B_RDQS<5>	IN
QSB_6	U4	FB_B_RDQS<6>	IN
QSB_7	V8	FB_B_RDQS<7>	IN

WRITE STROBE

QSB_0*	B10	FB_B_WDQS<0>	IN
QSB_1*	E10	FB_B_WDQS<1>	IN
QSB_2*	G10	FB_B_WDQS<2>	IN
QSB_3*	J7	FB_B_WDQS<3>	IN
QSB_4*	M4	FB_B_WDQS<4>	IN
QSB_5*	U3	FB_B_WDQS<5>	IN
QSB_6*	V4	FB_B_WDQS<6>	IN
QSB_7*	V9	FB_B_WDQS<7>	IN

CLKB0	B4	FB_B_CLK_P<0>	OUT
CLKB0*	B5	FB_B_CLK_N<0>	OUT
CSB0_0*	D2	FB_B_CS_L<0>	OUT
CSB0_1*	E3	NC	
CKEB0	C2	FB_B_CKE<0>	OUT
RASB0*	E2	FB_B_RAS_L<0>	OUT
CASB0*	D3	FB_B_CAS_L<0>	OUT
WEB0*	B2	FB_B_WE_L<0>	OUT
ODTB0	D6	TP_FB_B_ODT<0>	OUT
CLKB1	N2	FB_B_CLK_P<1>	OUT
CLKB1*	P3	FB_B_CLK_N<1>	OUT
CSB1_0*	K2	FB_B_CS_L<1>	OUT
CSB1_1*	K3	NC	
CKEB1	L3	FB_B_CKE<1>	OUT
RASB1*	J2	FB_B_RAS_L<1>	OUT
CASB1*	L2	FB_B_CAS_L<1>	OUT
WEB1*	M2	FB_B_WE_L<1>	OUT
ODTB1	J4	TP_FB_B_ODT<1>	OUT

=PP1V8R2V0_S0_FB_GPU

R8720 40.2 1% 1/16W MF-LF 402
R8722 40.2 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
C8721 0.1uF 10% 16V X5R 402
R8723 100 1% 1/16W MF-LF 402
C8723 0.1uF 10% 16V X5R 402

GPU_MVREFD1
GPU_MVREFS1
MVREFD_1
MVREFS_1
PP1V8R2V0_S0_GPU_VDDRH1
VDDRH1 (1.8V/ 2.0V)
VSSRH1

GPU_TEST_MCLK
GPU_TEST_YCLK
GPU_MEMTEST
TEST_MCLK
TEST_YCLK
MEMTEST
DRAM_RST
FB_DRAM_RST

R8731 4.7K 5% 1/16W MF-LF 402
R8730 4.7K 5% 1/16W MF-LF 402
R8732 243 1% 1/16W MF-LF 402
R8733 4.7K 5% 1/16W MF-LF 402

=PP1V8R2V0_S0_FB_GPU

L8725 FERR-220-OHM 0402
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

C8725 1uF 10% 6.3V CERM 402
C8726 1uF 10% 6.3V CERM 402

XW8725 SM
GND_GPU_VSSRH1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

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	Serial ROM	TestBus	Misc	Straps
GPU_GPIO_0	IPD	TESTIN[0]		TX_PWRS_ENb
GPU_GPIO_1	IPD	TESTIN[1]		TX_DEEMPH_EN
GPU_GPIO_2	VDD_VCL	TESTIN[2]		Reserved
GPU_GPIO_3		TESTIN[3]		Reserved
GPU_GPIO_4	IPD	TESTIN[4]		DEBUG_ACCESS
GPU_GPIO_5		TESTIN[5]		Reserved
GPU_GPIO_6		TESTIN[6]		Reserved
GPU_GPIO_7	ENA_BL	TESTIN[7]		
GPU_GPIO_8	ROMSO	TESTWR		Reserved
GPU_GPIO_9	IPD ROMSI			ROMIDCFG[3]
GPU_GPIO_10	ROMSCK	TESTOUT[8]		
GPU_GPIO_11	IPD	TESTOUT[9]		ROMIDCFG[0]
GPU_GPIO_12	IPD	TESTOUT[10]		ROMIDCFG[1]
GPU_GPIO_13	IPD	TESTOUT[11]		ROMIDCFG[2]
GPU_GPIO_14		TESTIN[8]		
GPU_GPIO_15		TESTIN[9]	PWRCNTL	
GPU_GPIO_16			SS_IN	
GPU_GPIO_17			Thm Mon	Int

GPU_GPIO_18 — NC_GPU_GPIO_18 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_19 — NC_GPU_GPIO_19 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_20 — NC_GPU_GPIO_20 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_21 — NC_GPU_GPIO_21 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_22 — NC_GPU_GPIO_22 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_23 — NC_GPU_GPIO_23 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_24 — GPU_MEM_256M (MAKE_BASE=TRUE)
GPU_GPIO_25 — NC_GPU_GPIO_25 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_26 — NC_GPU_GPIO_26 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_27 — GPU_MEMID (MAKE_BASE=TRUE)
GPU_GPIO_28 — NC_GPU_GPIO_28 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_29 — NC_GPU_GPIO_29 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_30 — NC_GPU_GPIO_30 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_31 — NC_GPU_GPIO_31 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_32 — NC_GPU_GPIO_32 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_33 — NC_GPU_GPIO_33 (MAKE_BASE=TRUE, NO_TEST=TRUE)
GPU_GPIO_34 — NC_GPU_GPIO_34 (MAKE_BASE=TRUE, NO_TEST=TRUE)

65A3 =PP3V3_D3C_GPU_GPIOS

ROMCFGID[3..0]
0000 = 128MB
0010 = 256MB
0100 = 64MB
0110 = Reserved

R8800 10K 5% 1/16W MF-LF 402 — GPU_DEEPMH_EN
R8801 10K 5% 1/16W MF-LF 402 — NO STUFF
R8802 10K 5% 1/16W MF-LF 402 — NO STUFF
R8803 10K 5% 1/16W MF-LF 402 — NO STUFF
R8804 10K 5% 1/16W MF-LF 402 — GPU_MEM_64M
R8805 10K 5% 1/16W MF-LF 402 — NO STUFF
R8806 10K 5% 1/16W MF-LF 402 — GPU_MEM_256M
R8808 10K 5% 1/16W MF-LF 402 — NO STUFF
R8809 10K 5% 1/16W MF-LF 402 — GPU_MEM_256M
R8811 10K 5% 1/16W MF-LF 402
R8812 10K 5% 1/16W MF-LF 402
R8813 10K 5% 1/16W MF-LF 402
R8824 10K 5% 1/16W MF-LF 402
R8827 10K 5% 1/16W MF-LF 402 — GPU_MEM_NOT_SAM

GPU_BLON — MAKE_BASE=TRUE (79A4)
TP_GPU_GPIO_10 — MAKE_BASE=TRUE — Required for debug access
Required for debug access
Required for debug access
Required for debug access
NC_GPU_GPIO_14 — MAKE_BASE=TRUE, NO_TEST=TRUE
GPU_VCORE_LOW — MAKE_BASE=TRUE (68B4)
GPU_CLK27MSS_IN — MAKE_BASE=TRUE (34B2 34B4)
NC_GPU_GPIO_17 — MAKE_BASE=TRUE, NO_TEST=TRUE

Renamed signals

34B4 34B2 GPU_CLK27M — MAKE_BASE=TRUE — GPU_XTALIN (74A5)

Unused signals

NC_GPU_XTALOUT (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_XTALOUT (74A5)
NC_ATI_ROMCS_L (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_ATI_ROMCS_L (74A3)
NC_FB_A_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_A_MA12 (70D5)
NC_FB_B_MA12 (MAKE_BASE=TRUE)	NO_TEST=TRUE	TP_FB_B_MA12 (70D1)
NC_GPU_GENERICA (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICA (74C3)
NC_GPU_GENERICB (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICB (74C3)
NC_GPU_GENERICC (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_GENERICC (74C3)
NC_GPU_VGA_R (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_R (75C3)
NC_GPU_VGA_G (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_G (75C3)
NC_GPU_VGA_B (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_VGA_B (75C3)
TP_GPU_VGA_HSYNC (MAKE_BASE=TRUE)		GPU_VGA_HSYNC (75B3)
TP_GPU_VGA_VSYNC (MAKE_BASE=TRUE)		GPU_VGA_VSYNC (75B3)
NC_GPU_TV_Y (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_Y (75B3)
NC_GPU_TV_C (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_C (75B3)
NC_GPU_TV_COMP (MAKE_BASE=TRUE)	NO_TEST=TRUE	GPU_TV_COMP (75B3)
NC_LVDS_U_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_P<3> (75B3)
NC_LVDS_U_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_U_DATA_N<3> (75B3)
NC_LVDS_L_DATAP<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_P<3> (75A3)
NC_LVDS_L_DATAN<3> (MAKE_BASE=TRUE)	NO_TEST=TRUE	LVDS_L_DATA_N<3> (75A3)
NC_ATI_DVPCLK (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCLK (74C3)
NC_ATI_DVPCNTL<2..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPCNTL<2..0> (74B3 74C3)
NC_ATI_DVPDATA<15..0> (MAKE_BASE=TRUE)	NO_TEST=TRUE	ATI_DVPDATA<15..0> (74B3)

Required for debug access

TP_ATI_DVPDATA<23..16> (MAKE_BASE=TRUE) — ATI_DVPDATA<23..16> (74A3 74B3)

Also required: GPIO10 - GPIO13

65A3 =PP3V3_D3C_GPU
R8890 4.7K 5% 1/16W MF-LF 402
R8891 4.7K 5% 1/16W MF-LF 402
75A3 GPU_DDC_B_CLK
75A3 GPU_DDC_B_DATA

GPU Straps

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

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Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

=PP1V8_S0_FB_VDD

=PP1V8_S0_FB_VDDQ

CRITICAL
OMIT

U8900
FBGA
(2 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

U8950
FBGA
(1 OF 2)
16MX32-GDDR3-500MHZ
K4J52324QC-BC20

C8900 22UF 20% 6.3V CERM 805
C8901 C8902 C8903 C8904 C8905 C8906 C8907 0.1UF 10% 16V X5R 402

L8910 FERR-220-OHM 0402
PP1V8_S0_FB_A0_VDDA0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

L8915 FERR-220-OHM 0402
PP1V8_S0_FB_A0_VDDA1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

Connect to designated pin, then GND

C8910 C8915 0.1UF 10% 16V X5R 402
U8900.J1
U8900.J12

C8920 22UF 20% 6.3V CERM 805
C8921 C8922 C8923 C8924 C8925 C8926 C8927 0.1UF 10% 16V X5R 402

R8930 R8932 2.37K 1% 1/16W MF-LF 402
R8931 R8933 5.49K 1% 1/16W MF-LF 402

FB_A0_VREF0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
FB_A0_VREF1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

C8931 C8933 0.1UF 10% 16V X5R 402

R8940 R8942 R8944 121 1% 1/16W MF-LF 402
R8946 60.4 1% 1/16W MF-LF 402
R8941 1K 5% 1/16W MF-LF 402
R8943 121 1% 1/16W MF-LF 402
R8945 60.4 1% 1/16W MF-LF 402
R8947 121 1% 1/16W MF-LF 402

NOTE: U8900 DQ0-7 MUST connect to GPU DQA0-7 or DQA8-15. Bits can be swapped within byte-lane, but software must know how these bits are mapped for GPU to support GDDR3 vendor/device identification scheme.

FB_A_MA<0>
FB_A_MA<1>
FB_A_MA<2>
FB_A_MA<3>
FB_A_MA<4>
FB_A_MA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE<0>
FB_A_CLK_P<0>
FB_A_CLK_N<0>
FB_A_CS_L<0>
FB_A_WE_L<0>
FB_A_CAS_L<0>
FB_A_RAS_L<0>
FB_DRAM_RST
FB_A_RDQS<0>
FB_A_RDQS<1>
FB_A_RDQS<2>
FB_A_RDQS<3>
FB_A_WDQS<0>
FB_A_WDQS<1>
FB_A_WDQS<2>
FB_A_WDQS<3>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>

FB_A0_ZQ
FB_A0_MF
FB_A0_SEN

R8948 243 1% 1/16W MF-LF 402
R8949 100 5% 1/16W MF-LF 402

FB_A_DQM_L<0>
FB_A_DQM_L<1>
FB_A_DQM_L<2>
FB_A_DQM_L<3>
FB_A_DQ<0>
FB_A_DQ<1>
FB_A_DQ<2>
FB_A_DQ<3>
FB_A_DQ<4>
FB_A_DQ<5>
FB_A_DQ<6>
FB_A_DQ<7>
FB_A_DQ<8>
FB_A_DQ<9>
FB_A_DQ<10>
FB_A_DQ<11>
FB_A_DQ<15>
FB_A_DQ<14>
FB_A_DQ<12>
FB_A_DQ<13>
FB_A_DQ<19>
FB_A_DQ<16>
FB_A_DQ<18>
FB_A_DQ<17>
FB_A_DQ<23>
FB_A_DQ<21>
FB_A_DQ<20>
FB_A_DQ<22>
FB_A_DQ<24>
FB_A_DQ<25>
FB_A_DQ<26>
FB_A_DQ<27>
FB_A_DQ<29>
FB_A_DQ<30>
FB_A_DQ<28>
FB_A_DQ<31>

C8950 22UF 20% 6.3V CERM 805
C8951 C8952 C8953 C8954 C8955 C8956 C8957 0.1UF 10% 16V X5R 402

L8960 FERR-220-OHM 0402
PP1V8_S0_FB_A1_VDDA0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

L8965 FERR-220-OHM 0402
PP1V8_S0_FB_A1_VDDA1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=1.8V

Connect to designated pin, then GND

C8960 C8965 0.1UF 10% 16V X5R 402
U8900.J1
U8900.J12

C8970 22UF 20% 6.3V CERM 805
C8971 C8972 C8973 C8974 C8975 C8976 C8977 0.1UF 10% 16V X5R 402

R8980 R8982 2.37K 1% 1/16W MF-LF 402
R8981 R8983 5.49K 1% 1/16W MF-LF 402

FB_A1_VREF0
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
FB_A1_VREF1
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm

C8981 C8983 0.1UF 10% 16V X5R 402

R8990 R8992 R8994 121 1% 1/16W MF-LF 402
R8996 60.4 1% 1/16W MF-LF 402
R8991 1K 5% 1/16W MF-LF 402
R8993 121 1% 1/16W MF-LF 402
R8995 60.4 1% 1/16W MF-LF 402
R8997 121 1% 1/16W MF-LF 402

FB_A_MA<0>
FB_A_MA<1>
FB_A_MA<2>
FB_A_MA<3>
FB_A_MA<4>
FB_A_MA<5>
FB_A_MA<6>
FB_A_MA<7>
FB_A_MA<8>
FB_A_MA<9>
FB_A_MA<10>
FB_A_MA<11>
FB_A_CKE<1>
FB_A_CLK_P<1>
FB_A_CLK_N<1>
FB_A_CS_L<1>
FB_A_WE_L<1>
FB_A_CAS_L<1>
FB_A_RAS_L<1>
FB_DRAM_RST
FB_A_RDQS<4>
FB_A_RDQS<5>
FB_A_RDQS<6>
FB_A_RDQS<7>
FB_A_WDQS<4>
FB_A_WDQS<5>
FB_A_WDQS<6>
FB_A_WDQS<7>
FB_A_BA<0>
FB_A_BA<1>
FB_A_BA<2>

FB_A1_ZQ
FB_A1_MF
FB_A1_SEN

R8998 243 1% 1/16W MF-LF 402
R8999 100 5% 1/16W MF-LF 402

FB_A_DQM_L<4>
FB_A_DQM_L<5>
FB_A_DQM_L<6>
FB_A_DQM_L<7>
FB_A_DQ<32>
FB_A_DQ<34>
FB_A_DQ<33>
FB_A_DQ<35>
FB_A_DQ<36>
FB_A_DQ<37>
FB_A_DQ<38>
FB_A_DQ<39>
FB_A_DQ<40>
FB_A_DQ<41>
FB_A_DQ<42>
FB_A_DQ<43>
FB_A_DQ<46>
FB_A_DQ<44>
FB_A_DQ<47>
FB_A_DQ<45>
FB_A_DQ<48>
FB_A_DQ<49>
FB_A_DQ<50>
FB_A_DQ<51>
FB_A_DQ<52>
FB_A_DQ<55>
FB_A_DQ<54>
FB_A_DQ<53>
FB_A_DQ<60>
FB_A_DQ<59>
FB_A_DQ<61>
FB_A_DQ<57>
FB_A_DQ<62>
FB_A_DQ<56>
FB_A_DQ<63>
FB_A_DQ<58>

GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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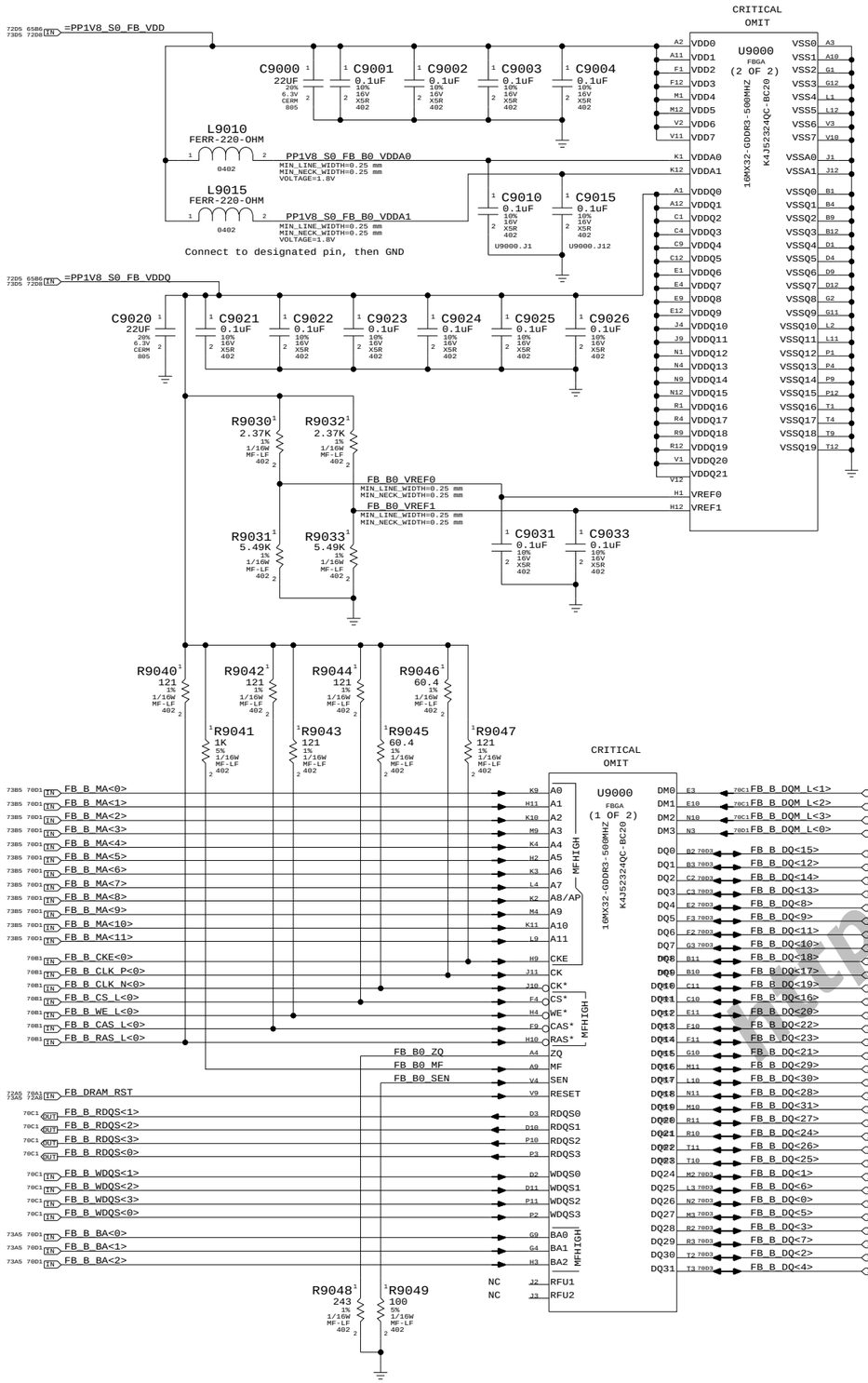
SCALE: NONE	SHT 72 OF 84	

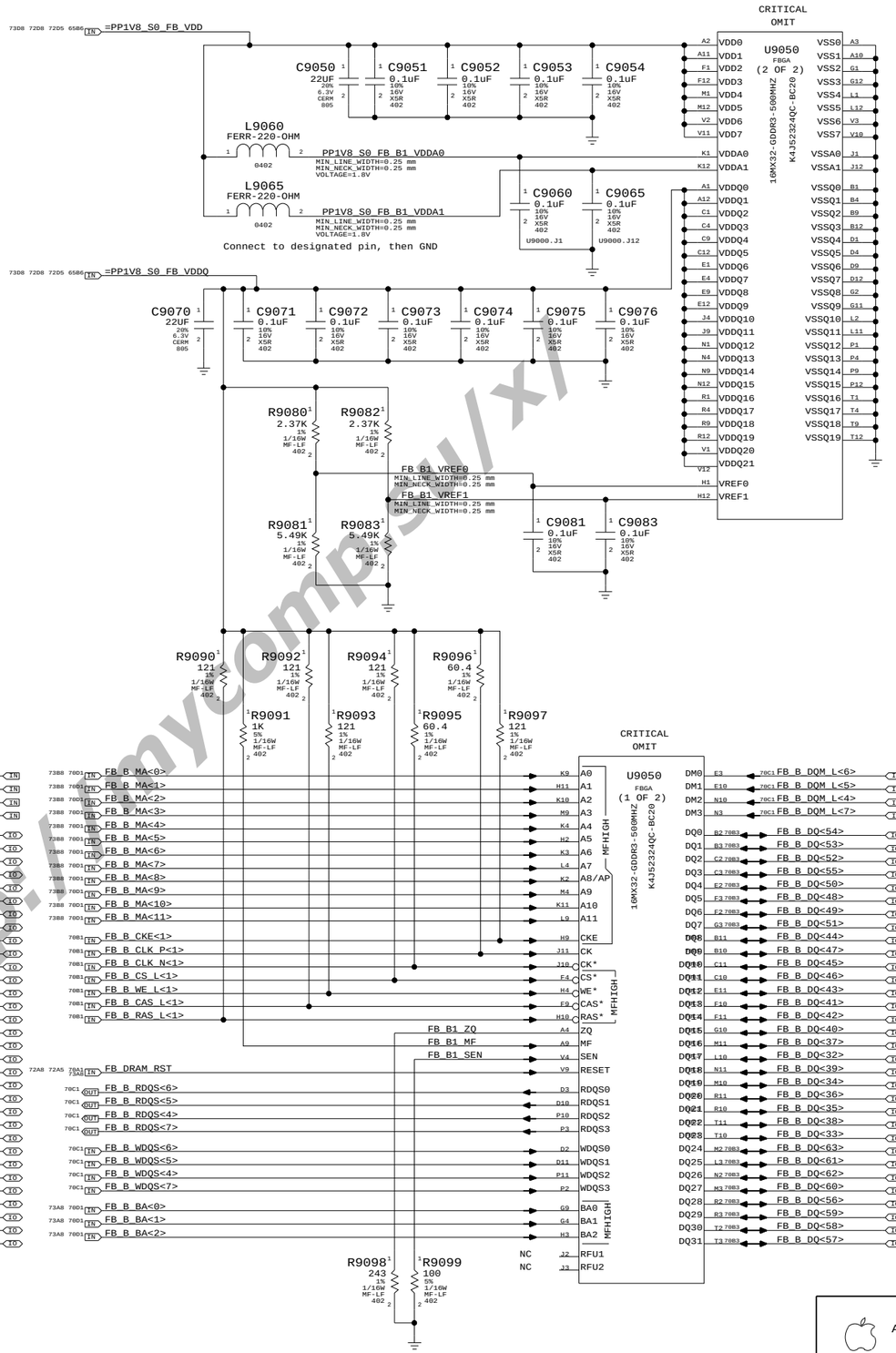
Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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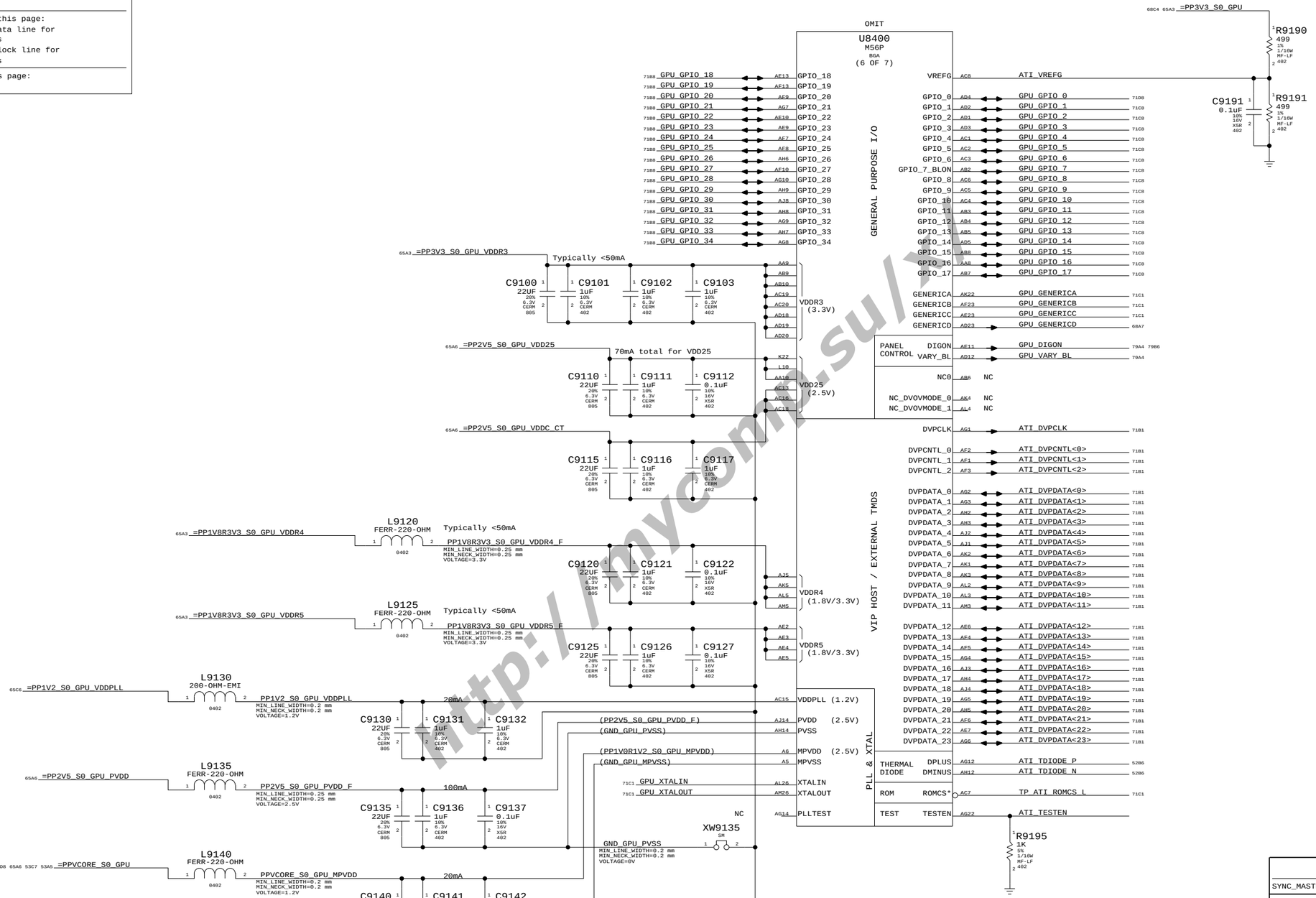
D	051-7150	A.0.0
SCALE: NONE	SHT 73 OF 84	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

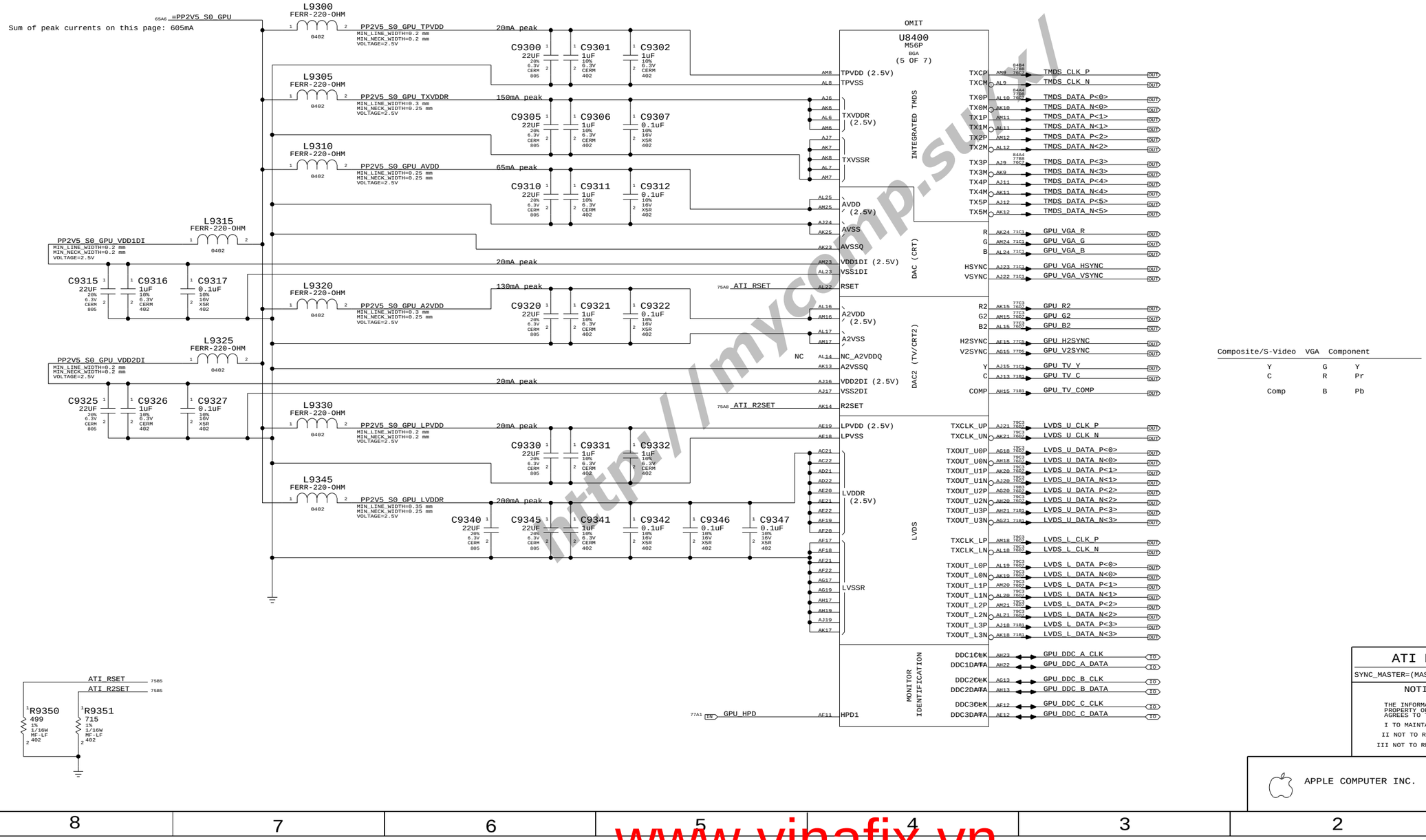
SCALE	SHT	OF
NONE	74	84

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

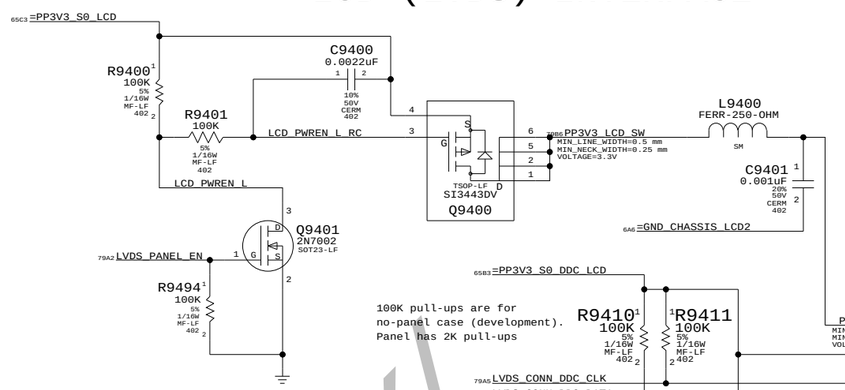
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

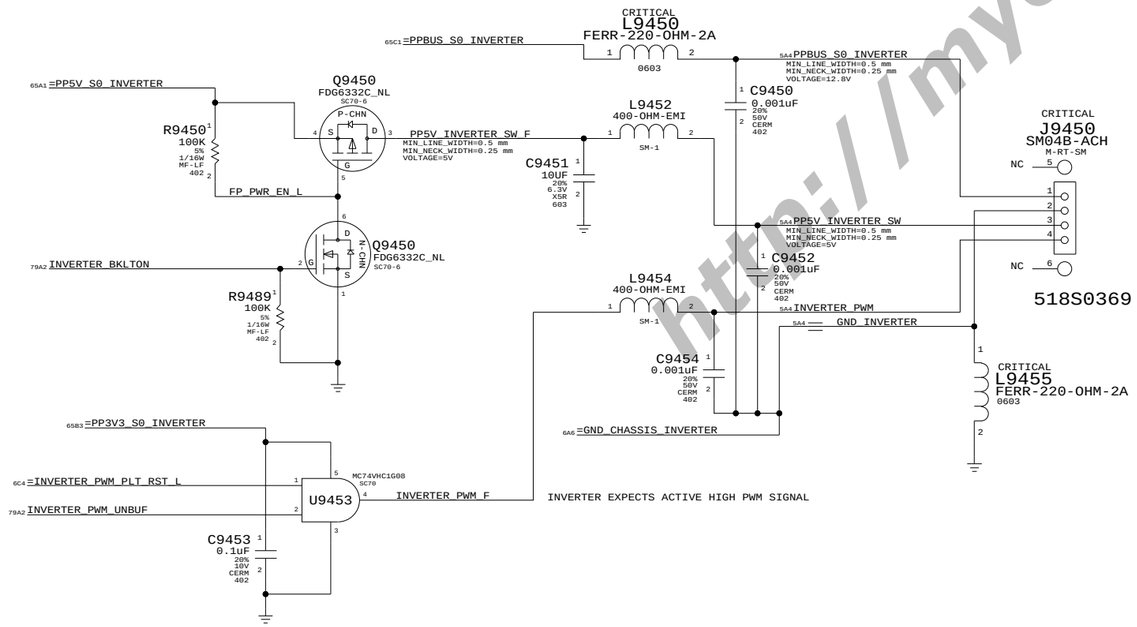


LCD (LVDS) INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL		
	VGA	VGA	GPU_R2	75B3 77C3
	VGA	VGA	GPU_G2	75B3 77C3
	VGA	VGA	GPU_B2	75B3 77C3
	LVDS	LVDS	LVDS_U_CLK_P	75B3 79C3
	LVDS	LVDS	LVDS_U_CLK_N	75B3 79C3
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	75B3 79B3 79C3
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	75B3 79C3
	LVDS	LVDS	LVDS_L_CLK_P	75A3 79C3
	LVDS	LVDS	LVDS_L_CLK_N	75A3 79C3
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	75A3 79C3
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	75A3 79C3
	LVDS	LVDS	LVDS_U_CLK_CONN_P	6B1 76B2 79C1
	LVDS	LVDS	LVDS_U_CLK_CONN_N	6B1 76B2 79C1
	LVDS	LVDS	LVDS_U_DATA_CONN_P<2..0>	6B1 76B2 76C2 79C1 79D1
	LVDS	LVDS	LVDS_U_DATA_CONN_N<2..0>	6B1 76C2 79C1 79D1
	LVDS	LVDS	LVDS_L_CLK_CONN_P	6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_CLK_CONN_N	6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_DATA_CONN_P<2..0>	6A1 6B1 76C2 79C1
	LVDS	LVDS	LVDS_L_DATA_CONN_N<2..0>	6A1 76C2 79C1
	TMDS	TMDS	TMDS_CLK_P	75C3 77B8 84B4
	TMDS	TMDS	TMDS_CLK_N	75C3 77C8 84B4
	TMDS	TMDS	TMDS_DATA_P<5..3>	75C3 77A8 77B8 84A4
	TMDS	TMDS	TMDS_DATA_N<5..3>	75C3 77A8 77B8 84A4
	TMDS	TMDS	TMDS_DATA_P<2..0>	75C3 77C8 77D8 84A4
	TMDS	TMDS	TMDS_DATA_N<2..0>	75C3 77C8 77D8 84A4



INVERTER INTERFACE



Internal Display Connectors

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

APPLE COMPUTER INC.

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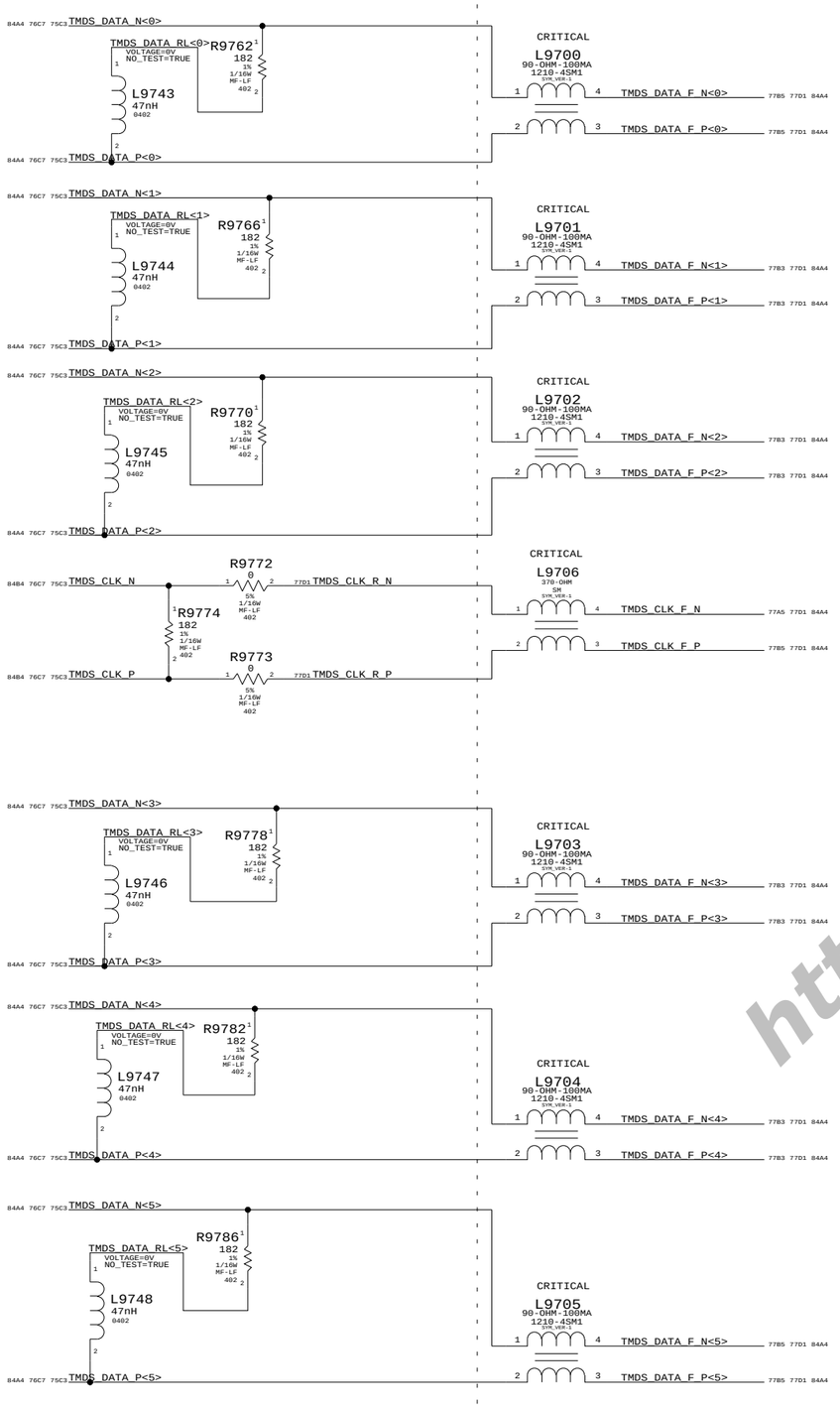
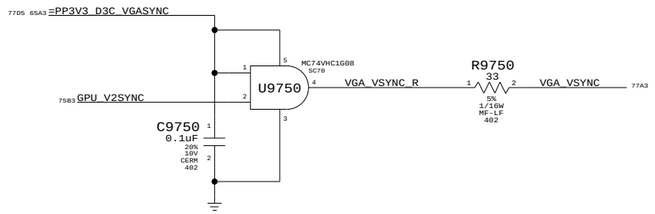
TMDS Filtering

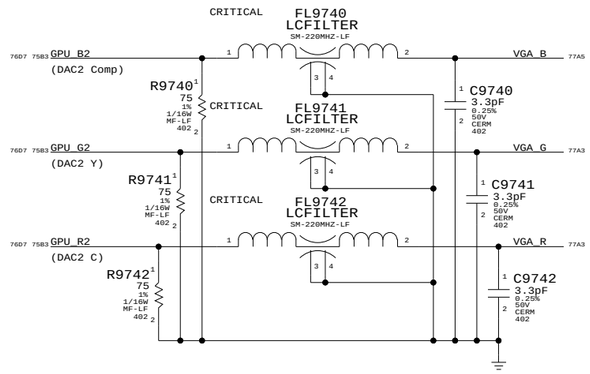
Place termination components close to GPU, common mode chokes near connector.



VGA SYNC BUFFERS

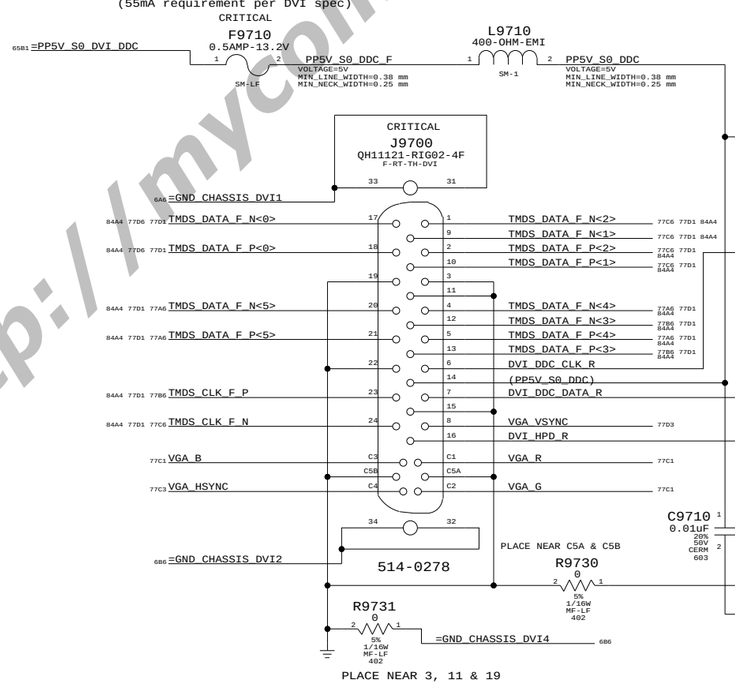


ANALOG FILTERING
PLACE CLOSE TO CONNECTOR



DVI INTERFACE

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	
	TMDS	TMDS	TMDS_CLK_R_P 77B7
	TMDS	TMDS	TMDS_CLK_R_N 77C7
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P 77B5 77B6 84A4
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N 77A5 77C6 84A4
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..0> 77A6 77B3 77B5 77B6 77C6 77D6 84A4
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..0> 77A6 77B3 77B5 77B6 77C6 77D6 84A4

External Display Connector

SYNC_MASTER=M59_MG SYNC_DATE=07/25/2006

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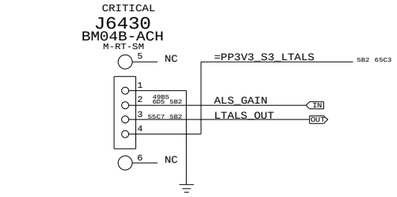
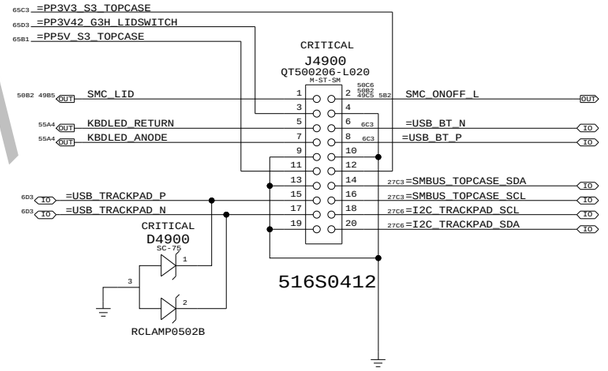
Left ALS Connector



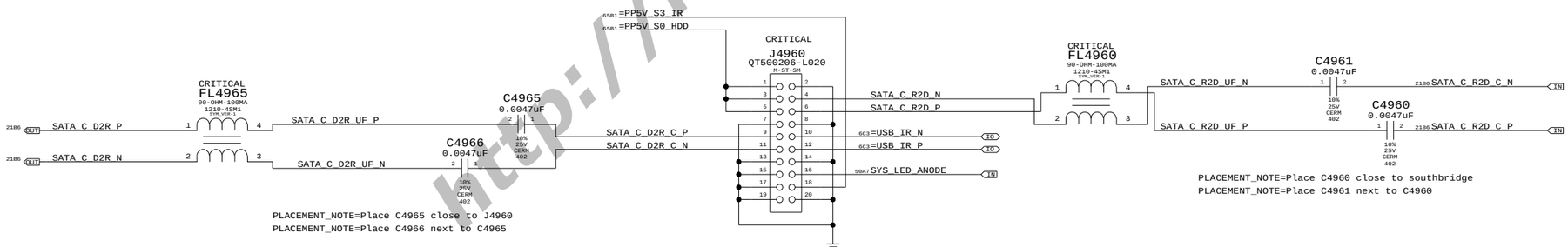
518S0469
white colored version of 518S0369

Top-Case Connector



516S0412

SATA HDD & IR & SIL Flex Connector



PLACEMENT_NOTE=Place C4965 close to J4960
PLACEMENT_NOTE=Place C4966 next to C4965

PLACEMENT_NOTE=Place C4960 close to southbridge
PLACEMENT_NOTE=Place C4961 next to C4960

516S0412

NOTE: _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.

M59 Specific Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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D	051-7150	A.0.0

SCALE: NONE

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LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when they should be tri-stated to meet panel power sequence requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be 0V.

LVDS_PD RP9900 8.2K
=LVDS_PD_L_DATA_P<0>
=LVDS_PD_L_DATA_N<0>
=LVDS_PD_L_DATA_P<1>
=LVDS_PD_L_DATA_N<1>
LVDS_PD RP9901 8.2K
=LVDS_PD_L_DATA_P<2>
=LVDS_PD_L_DATA_N<2>
=LVDS_PD_L_CLK_P
=LVDS_PD_L_CLK_N
LVDS_PD RP9902 8.2K
=LVDS_PD_U_DATA_P<0>
=LVDS_PD_U_DATA_N<0>
=LVDS_PD_U_DATA_P<1>
=LVDS_PD_U_DATA_N<1>
LVDS_PD RP9903 8.2K
=LVDS_PD_U_DATA_P<2>
=LVDS_PD_U_DATA_N<2>
=LVDS_PD_U_CLK_P
=LVDS_PD_U_CLK_N
5% 1/16W SM-LF

PGOOD Monitor for GPU Rails

D3CPGOOD_ALL BOM option stuffs LTC2903 circuit to monitor all D3C rails to qualify D3CPGOOD.
D3CPGOOD_3V3 BOM option uses only PP3V3_D3C to qualify D3CPGOOD.

PP3V3_D3C
PP2V5_D3C
PP1V8_D3C
PP1V2_D3C
=PP3V3_S0_ALLSYSPG
R9994 124K 1% 1/16W MF-LF 402
R9992 237K 1% 1/16W MF-LF 402
R9990 365K 1% 1/16W MF-LF 402
C9990 0.1UF 20% 10V CERM 402
R9997 10K 5% 1/16W MF-LF 402
C9991 0.1UF 20% 10V CERM 402
U9990 LTC2903 TSOT-23
CRITICAL
D3CPGOOD_2V5_DIV
D3CPGOOD_1V8_DIV
D3CPGOOD_1V2_DIV
GND
RST*
R9995 100K 1% 1/16W MF-LF 402
R9993 100K 1% 1/16W MF-LF 402
R9991 100K 1% 1/16W MF-LF 402
C9995 0.1UF 20% 10V CERM 402
C9993 0.1UF 20% 10V CERM 402
C9992 0.1UF 20% 10V CERM 402
R9996 470K 5% 1/16W MF-LF 402
C9996 1UF 10% 6.3V CERM 402
D3CPGOOD_3V3
S0PGOOD_PWROK
D3CPGOOD_PWROK
S0D3CPGOOD_PWROK
U9991 MC74VHC1G08 SC70

LTC2903 guaranteed threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

NB LVDS I/F

LVDS Mux Selection Qualification

Enables the GPU LVDS path in the mux with the qualification that the GPU has turned on panel power and that the panel power has risen to (near) 3.3V. This should eliminate need for LVDS pulldowns

=PP3V3_S0_LVDS_MUX
C9985 0.1UF 20% 10V CERM 402
U9985 MC74VHC1G08 SC70
GPU_DIGON
=LVDS_MUX_SEL_GPU
GPU_DIGON_AND_SELECTED
=PP2V5_S0_LVDS_MUX
C9980 0.1UF 20% 10V CERM 402
CRITICAL
U9980 SN74LVC1G132 SC70-5
R9980 10K 5% 1/16W MF-LF 402
PP3V3_LCD_SW
PANEL_PWR_ON
R9981 13.3K 1% 1/16W MF-LF 402

Divider set to rise to 1.88V nom/1.74V min when panel power is at 3.3V/3.315V. Schmitt trigger voltage max is 1.70V (@2.625V Vcc). R9981 can also be used as pad for cap, creating an RC filter.

GPU LVDS I/F

LVDS I/F Mux

=PP2V5_S0_LVDS_MUX
C9950 0.1UF 20% 10V CERM 402
VDD
CRITICAL
U9950 CBTV4020 BGA-LF

LVDS_B_DATA_N<2>	F1	DA0	
LVDS_B_DATA_N<0>	H1	DA1	
LVDS_B_DATA_P<0>	K1	DA2	
	K3	DA3	
LVDS_A_CLK_P	K4	DA4	
LVDS_A_CLK_N	K6	DA5	
	J7	DA6	
LVDS_A_DATA_N<0>	K9	DA7	
LVDS_A_DATA_P<0>	J10	DA8	
LVDS_A_DATA_P<2>	G10	DA9	
LVDS_A_DATA_N<2>	E10	DA10	
LVDS_A_DATA_N<1>	C10	DA11	
LVDS_A_DATA_P<1>	A10	DA12	
	A8	DA13	
LVDS_B_DATA_P<1>	A7	DA14	
LVDS_B_DATA_N<1>	A5	DA15	
	B4	DA16	
LVDS_B_CLK_N	A2	DA17	
LVDS_B_CLK_P	B1	DA18	
LVDS_B_DATA_P<2>	D1	DA19	
LVDS_U_DATA_N<2>	G1	DB0*	
LVDS_U_DATA_N<0>	J1	DB1*	
LVDS_U_DATA_P<0>	K2	DB2*	
	J4	DB3*	
LVDS_L_CLK_P	K5	DB4*	
LVDS_L_CLK_N	K7	DB5*	
	K8	DB6*	
LVDS_L_DATA_N<0>	K10	DB7*	
LVDS_L_DATA_P<0>	H10	DB8*	
LVDS_L_DATA_P<2>	F10	DB9*	
LVDS_L_DATA_N<2>	D10	DB10*	
LVDS_L_DATA_N<1>	B10	DB11*	
LVDS_L_DATA_P<1>	A9	DB12*	
	B7	DB13*	
LVDS_U_DATA_P<1>	A6	DB14*	
LVDS_U_DATA_N<1>	A4	DB15*	
	A3	DB16*	
LVDS_U_CLK_N	A1	DB17*	
LVDS_U_CLK_P	C1	DB18*	
LVDS_U_DATA_P<2>	E1	DB19*	

GND
H6 H5 G3 G2 D4 D3 C4 C3

DH0	F2	LVDS_U_DATA_CONN_N<2>	6B1 76C2 76D7
DH1	H2	LVDS_U_DATA_CONN_N<0>	6B1 76C2 76D7
DH2	J2	LVDS_U_DATA_CONN_P<0>	6B1 76C2 76D7
DH3	J3	NC	
DH4	J5	LVDS_L_CLK_CONN_P	6B1 76C2 76D7
DH5	J6	LVDS_L_CLK_CONN_N	6B1 76C2 76D7
DH6	J8	NC	
DH7	J9	LVDS_L_DATA_CONN_N<0>	6A1 76C2 76D7
DH8	H9	LVDS_L_DATA_CONN_P<0>	6B1 76C2 76D7
DH9	F9	LVDS_L_DATA_CONN_P<2>	6A1 76C2 76D7
DH10	E9	LVDS_L_DATA_CONN_N<2>	6A1 76C2 76D7
DH11	C9	LVDS_L_DATA_CONN_N<1>	6A1 76C2 76D7
DH12	B9	LVDS_L_DATA_CONN_P<1>	6A1 76C2 76D7
DH13	B8	NC	
DH14	B6	LVDS_U_DATA_CONN_P<1>	6B1 76C2 76D7
DH15	B5	LVDS_U_DATA_CONN_N<1>	6B1 76C2 76D7
DH16	B3	NC	
DH17	B2	LVDS_U_CLK_CONN_N	6B1 76B2 76D7
DH18	C2	LVDS_U_CLK_CONN_P	6B1 76B2 76D7
DH19	E2	LVDS_U_DATA_CONN_P<2>	6B1 76B2 76D7
SEL	E3	LVDS_MUX_SEL_GPU_L	

NOTE: SEL = LOW selects port B

GPU DDC Pass FETs

=GPU_DDC_ENABLE
=PP3V3_D3C_GPU_LVDS_DDC
R9970 15.8K 1% 1/16W MF-LF 402
Q9970 2N7002DW-X-F SOT-363
GPU_DDC_C_CLK
LVDS_CONN_DDC_CLK
MAKE_BASE=TRUE
LVDS_DDC_CLK
R9971 15.8K 1% 1/16W MF-LF 402
Q9970 2N7002DW-X-F SOT-363
GPU_DDC_C_DATA
LVDS_CONN_DDC_DATA
MAKE_BASE=TRUE
LVDS_DDC_DATA

Panel/Backlight Control Mux

=PP3V3_S0_LVDS_MUX
C9960 0.1UF 20% 10V CERM 402
CRITICAL
VCC
U9960 74CBTLV3257 QFN

LVDS_VDDEN	2	1B1	1A	4	LVDS_PANEL_EN
GPU_DIGON	3	1B2			
LVDS_BKLTEN	5	2B1	2A	7	INVERTER_BKLTON
GPU_BLON	6	2B2			
LVDS_BKLTCTL	11	3B1	3A	9	INVERTER_PWM_UNBUF
GPU_VARY_BL	10	3B2			
S0PGOOD_PWROK	14	4B1	4A	12	PGOOD_MUXED_S0_OR_S0D3C
S0D3CPGOOD_PWROK	13	4B2			
LVDS_MUX_SEL_GPU_MUXED	1	S			
	15	OE*			
	8	GND	THRML PAD	17	

NOTE: S = HIGH selects xB2

=PP3V3_S0_LVDS_MUX
C9961 0.1UF 20% 10V CERM 402
PLT_RST_L
=LVDS_MUX_SEL_GPU
U9961 MC74VHC1G08 SC70
NO STUFF
R9962 0 5% 1/16W MF-LF 402
R9961 100K 5% 1/16W MF-LF 402
R9960 10K 5% 1/16W MF-LF 402
TP_SB_GPIO23
LVDS_MUX_SEL_GPU
MAKE_BASE=TRUE
=LVDS_MUX_SEL_GPU

NOTE: SB_GPIO23 has internal 20K PU to default selection to GPU

LVDS Interface Pull-downs		
SYNC_MASTER=M59_MG	SYNC_DATE=08/01/2006	
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7150 REV. A.0.0
	SCALE NONE	SHT 79 OF 84

Date	- Radar # - Description

DMS Release #01000

2006/05/26 - 4508681 - Release for Proto

DMS Release #04000

2006/06/30 - 4566939 - Release for EVT

DMS Release #07000

2006/08/07 - 4607952 - Release for DVT

DMS Release #0A000

2006/09/19 - 4726575 - Release for PVT

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 80 OF 84

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR	*	=3:1_SPACING	
FSB_ADDR2ADDR	*	=2:1_SPACING	
FSB_ADSTB	*	=3:1_SPACING	
FSB_ADDR2ADSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=3:1_SPACING	
FSB_DATA2DATA	*	=2:1_SPACING	
FSB_DSTB	*	=3:1_SPACING	
FSB_DATA2DSTB	*	=3:1_SPACING	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_COMMON	*	=2:1_SPACING	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_2TO1	*	=2:1_SPACING	
CPU_COMP	*	25 MIL	
CPU_GTLREF	*	25 MIL	
CPU_ITP	*	=2:1_SPACING	
CPU_VCCSENSE	*	25 MIL	

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	
MEM_CTRL2CTRL	*	=2:1_SPACING	
MEM_CTRL2MEM	*	=3:1_SPACING	
MEM_CMD2CMD	*	=1.5:1_SPACING	
MEM_CMD2MEM	*	=3:1_SPACING	
MEM_DATA2DATA	*	=1.5:1_SPACING	
MEM_DATA2MEM	*	=3:1_SPACING	
MEM_DQS2MEM	*	=3:1_SPACING	
MEM_2OTHER	*	25 MIL	

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	20 MIL	
DMI	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
IDE	*	=1.8:1_SPACING	
SATA	*	20 MIL	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	
USB2_2CLK	*	25 MIL	

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=3:1_SPACING	
SPI	*	=1.8:1_SPACING	

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	25 MIL	
CLK_PCIE	*	20 MIL	
CLK_MED	*	20 MIL	
CLK_SLOW	*	10 MIL	

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE	SHT	OF
NONE	81	84

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_3SS_TO_5SS	*	Y	=3S_OHM_SE	=5S_OHM_SE	=3S_5S_OHM_SE	=STANDARD	=STANDARD
FB_4QS	*	Y	=4Q_OHM_SE	=4Q_OHM_SE	=4Q_OHM_SE	=STANDARD	=STANDARD
FB_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FB_ADCTRL	*	=2.5:1_SPACING	
FB_CLK	*	=2.5:1_SPACING	
FB_DATA	*	=2.5:1_SPACING	

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS	*	=3:1_SPACING	
TMDS	*	=3:1_SPACING	
VGA	*	15 MIL	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LVDS_PAIR2PAIR	*	25 MIL	
TMDS_PAIR2PAIR	*	25 MIL	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET	*	=3:1_SPACING	
FW	*	=3:1_SPACING	

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_5SS	*	Y	=5S_OHM_SE	=5S_OHM_SE	=5S_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=2:1_SPACING	

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE: NONE SHT 82 OF 84

M59 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.077 MM	0.077 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	
STANDARD	*	=DEFAULT	
BGA_P1MM	*	=DEFAULT	
BGA_P2MM	*	=DEFAULT	
BGA_P3MM	*	=DEFAULT	

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	
1.8:1_SPACING	*	0.18 MM	
2:1_SPACING	*	0.2 MM	
2.5:1_SPACING	*	0.25 MM	
3:1_SPACING	*	0.3 MM	
4:1_SPACING	*	0.4 MM	

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	ISL2,ISL11	0.1 MM	
1.8:1_SPACING	ISL2,ISL11	0.1 MM	
2:1_SPACING	ISL2,ISL11	0.1 MM	
2.5:1_SPACING	ISL2,ISL11	0.1 MM	
3:1_SPACING	ISL2,ISL11	0.1 MM	
4:1_SPACING	ISL2,ISL11	0.1 MM	

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	ISL2,ISL11	0.1 MM	
CLK_PCIE	ISL2,ISL11	0.1 MM	
CLK_MED	ISL2,ISL11	0.1 MM	
CLK_SLOW	ISL2,ISL11	0.1 MM	
CPU_COMP	ISL2,ISL11	0.1 MM	
CPU_GTLREF	ISL2,ISL11	0.1 MM	
CPU_VCCSENSE	ISL2,ISL11	0.1 MM	
DMI	ISL2,ISL11	0.1 MM	
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
MEM_2OTHER	ISL2,ISL11	0.1 MM	
PCIE	ISL2,ISL11	0.1 MM	
SATA	ISL2,ISL11	0.1 MM	
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM	
VGA	ISL2,ISL11	0.1 MM	

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE	OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE	OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE	OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI_2PCI OVERRIDE	* OVERRIDE	0.1 MM OVERRIDE	OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	PCI	*	PCI_2PCI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_5SS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_4SS OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_7OD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_8SD OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M59 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0

SCALE NONE SHT 83 OF 84

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BNR_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7D6 12C4
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5D5 7D6 12C4
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7D6 12B4
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7B3 12B4
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HIT_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_HITM_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5D5 7D6 12B4
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7D6 12A4
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7D6 11B5 12C4
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5D5 7B3 7B4 7C3 7C4 12B6 12C6 12D6
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5D5 7B3 7B4 7C3 7C4 12B4
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5D5 7C8 7D8 12C4 12D4
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5D5 7D8 12A4 12B4
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5D5 7C8 7D8 12C4
	CPU_55S		FSB_IERR_L	7D6
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7B3 21C4
	CPU_55S		CPU_INTR	7C8 21C4
	CPU_55S		CPU_NMI	7C8 21C4
	CPU_55S		CPU_A20M_L	7C8 21C4
	CPU_55S		CPU_DPSLP_L	7B3 21C4
	CPU_55S		CPU_IGNNE_L	7C8 21C4
	CPU_55S		CPU_INIT_L	7D6 21C4
	CPU_55S		CPU_SMI_L	7C8 21C4
	CPU_55S		CPU_STPCLK_L	7C8 21C4
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14B7 23C3 59C8
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	59C7
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7B4
	CPU_55S	CPU_COMP	CPU_COMP<3>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7B3
	CPU_55S	CPU_COMP	CPU_COMP<1>	7B3
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7B3
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7C6 11B3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11B3 34D3
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11B3 34D3
	CPU_55S	CPU_ITP	ITPRESET_L	11B3
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 84B6
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8B7 9C2 84B6
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8B6 59B1
THERM	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8B6 59A1
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	59A3
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	59A3

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_108D	
TMDS	TMDS_108D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21C6
AUDIO_55S	AUDIO	ACZ_BITCLK	5C1 21C7 47B6
AUDIO_55S	AUDIO	SB_ACZ_SYNC	21C6
AUDIO_55S	AUDIO	ACZ_SYNC	5C1 21C7 47B6
AUDIO_55S	AUDIO	SB_ACZ_RST_L	21C6
AUDIO_55S	AUDIO	ACZ_RST_L	5C1 21C7 47B3
AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5C1 21C7 47B6
AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21C6
AUDIO_55S	AUDIO	ACZ_SDATAOUT	5C1 21C7 47B6

TMDS	TMDS	TMDS_CLK_P	75C3 76C7 77B8
TMDS	TMDS	TMDS_CLK_N	75C3 76C7 77C8
TMDS	TMDS	TMDS_DATA_P<5..3>	75C3 76C7 77A8 77B8
TMDS	TMDS	TMDS_DATA_N<5..3>	75C3 76C7 77A8 77B8
TMDS	TMDS	TMDS_DATA_P<2..0>	75C3 76C7 77C8 77D8
TMDS	TMDS	TMDS_DATA_N<2..0>	75C3 76C7 77C8 77D8
TMDSCONN	TMDSCONN	TMDS_CLK_F_P	77B5 77B6 77D1
TMDSCONN	TMDSCONN	TMDS_CLK_F_N	77A5 77C6 77D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	77A6 77B3 77B5 77B6 77D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	77A6 77B3 77B5 77B6 77D1
TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	77B3 77B5 77C6 77D1 77D6
TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	77B3 77B5 77C6 77D1 77D6

M59 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-7150	A.0.0
SCALE: NONE	SHT 84 OF 84	