1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION

SCHEM,FLYING_CLOUD,MLB,K90i

"EVT3" 11/22/10

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8658	1	SCHEM,MLB,K90i	SCH	CRITICAL	
820-2936	1	PCBF,MLB,K90i	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Nov 22 19:21:11 2010

DRAWING TITLE: SCHEM,FLYING_CLOUD,MLB,K90i

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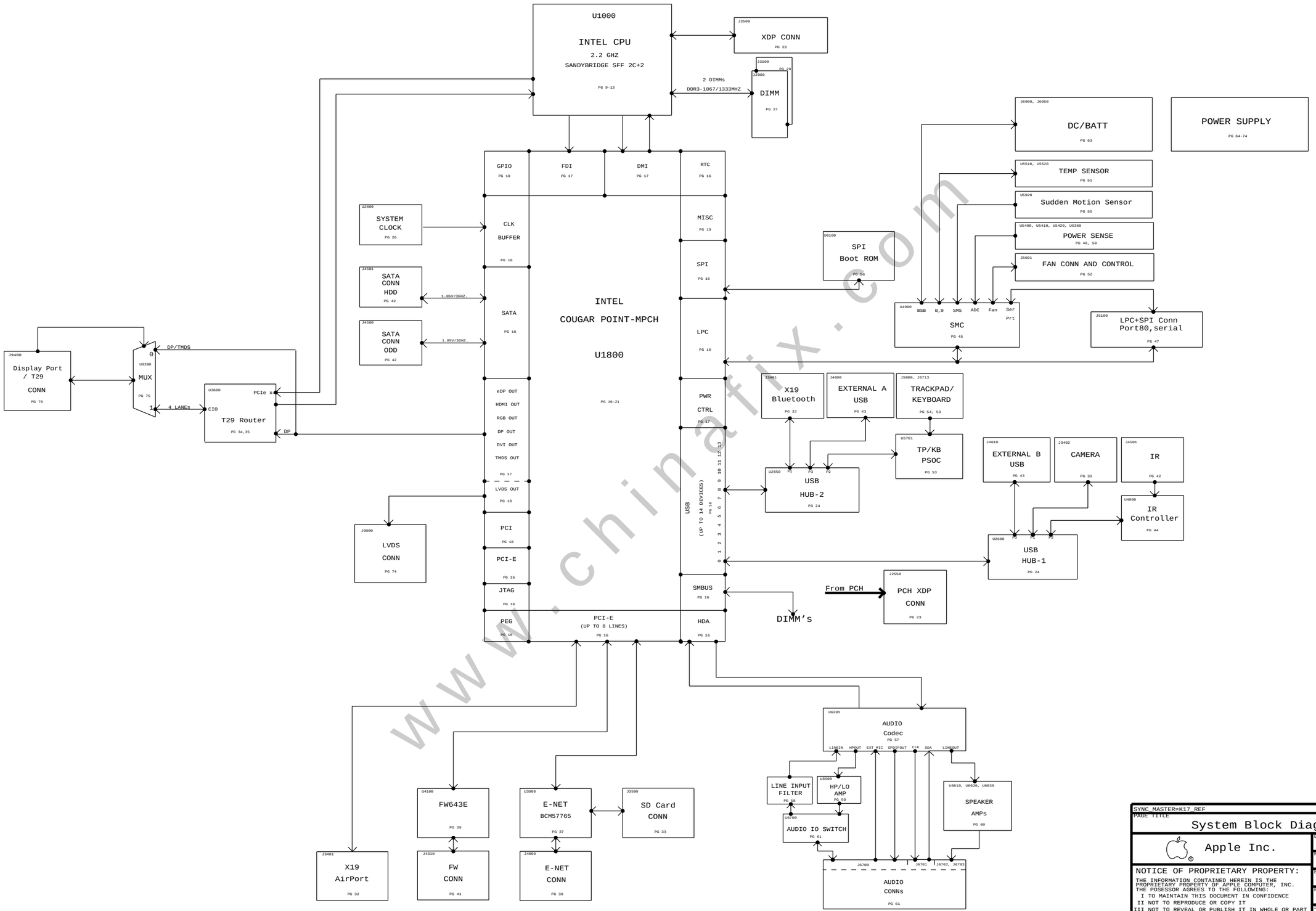

SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

PAGE TITLE

System Block Diagram

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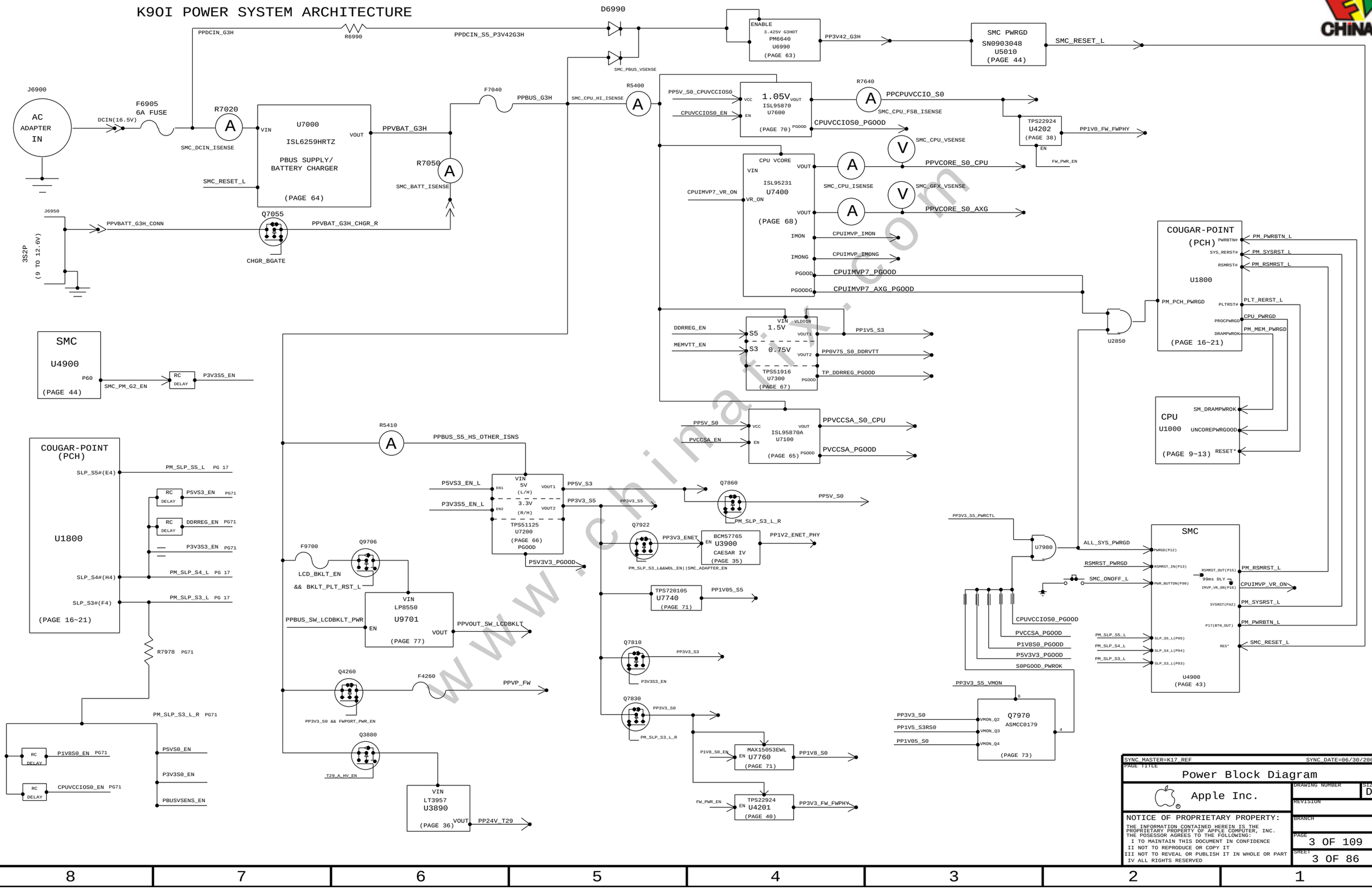
K90I POWER SYSTEM ARCHITECTURE



SYNC_MASTER=K17_REF SYNC_DATE=06/30/2009

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Power Block Diagram

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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1294	PCBA,2.5G,K90i	K90i_COMMON,CPU_2_5GHZ,EEEE_DDRQ
639-1581	PCBA,2.7G,K90i	K90i_COMMON,CPU_2_7GHZ,EEEE_DH78
639-1698	PCBA,2.6G,K90i	K90i_COMMON,CPU_2_6GHZ,EEEE_DH8F
639-1699	PCBA,2.3G,K90i	K90i_COMMON,CPU_2_3GHZ,EEEE_DH8G
085-1998	K90i MLB DEVELOPMENT BOM	K90i_DEVEL:ENG

K90i BOM GROUPS

BOM GROUP	BOM OPTIONS
K90i_COMMON	ALTERNATE,COMMON,K90i_COMMON1,K90i_COMMON2,K90i_DEBUG:ENG,K90i_PROGPARTS,USBHUB_2513B,T29BST:Y
K90i_COMMON1	BATT_3S,CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM,T29:YES,DP_SDRV:A2,SDRV_PD,SDRVI2C:MCU
K90i_COMMON2	MIKEY,KB_BL
K90i_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
K90i_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,VREFMRGN,S0PGOOD_ISL,IMVPISNS_ENG
K90i_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K90i_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K90i_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT
K90i_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT,LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3934	1	SNB,2C,QXXX,ES1,2.2,35W,R2,3M,GT1,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S4058	1	SNB,Q1RA,QS,J1,2.5,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4057	1	SNB,Q1R3,QS,J1,2.7,35W,2+2,1.30,4M,BGA	U1000	CRITICAL	CPU_2_7GHZ
337S4024	1	SNB,Q1R9,QS,J1,2.3,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_3GHZ
337S4064	1	SNB,Q1R7,QS,J1,2.6,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_6GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
343S0534	1	IC,BCM57765B0,ENET&SD,8X8	U3900	CRITICAL	
338S0753	1	IC,FW643-E2,1394B PHY/OHCI LINK/PCI-E,32	U4100	CRITICAL	
338S0921	1	IC,T29-C0,220 FCBGA,15x15MM	U3600	CRITICAL	T29:YES
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0663	1	IC,FLASH,SERIAL,SPI,1MBIT,2V7,8P,SOIC	U3990	CRITICAL	ENET_BLANK
341S3026	1	IC ENET,1!MBITFLAH,CIV REV01,K60/K62	U3990	CRITICAL	ENET_PROG
335S0777	1	IC,EEPROM,SERIAL,SPI,1Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341T0317	1	IC,T29 ASSY	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,HVQFN25	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC,SMC,HS8/2117/9MMx9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0300	1	IC,SMC,K90i	U4900	CRITICAL	SMC_PROG
335S0770	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
335S0769	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341T0299	1	IC,EFI ROM,K90i	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
341S3024	1	IC,TP PSOC,K90,K90i,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1998	1	K90i MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DDRQ]	CRITICAL	EEEE_DDRQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH78]	CRITICAL	EEEE_DH78
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH8F]	CRITICAL	EEEE_DH8F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH8G]	CRITICAL	EEEE_DH8G

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
516S0805	516S0806		ALL	Molex alt to Foxconn
128S0303	128S0282		ALL	Panasonic alt to Sanyo
138S0676	138S0691		ALL	Murata alt to Samsung
152S0778	152S0693		ALL	Cyntec alt to Vishay
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
376S0927	376S0966		ALL	Fairchild alt to Renesas
376S0927	376S0790		ALL	Fairchild alt to CICLON
376S0960	376S0801		ALL	Renesas alt to Renesas
376S0790	376S0928		ALL	CICLON alt to Fairchild
376S0928	376S0895		ALL	Fairchild alt to Renesas
376S0937	376S0845		ALL	Fairchild alt to Renesas
376S0777	376S0761		ALL	AON alt to Siliconix
376S0957	376S0958		ALL	Fairchild alt to Fairchild
376S0953	376S0958		ALL	Fairchild alt to Renesas
353S3085	353S1658		ALL	STmicro alt to LT

SYNC_MASTER=K17_REF SYNC_DATE=05/28/2009

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Functional Test Points

Fan Connectors

J4500	TRUE	PP5V_S0	6 7 22 42 47 52 54 65 68 70 72 73 77
J4501	TRUE	FAN_RT_PWM	52
J4502	TRUE	FAN_RT_TACH	52

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

J4505	TRUE	BI_MIC_LO	61 62
J4506	TRUE	BI_MIC_HI	61 62
J4508	TRUE	BI_MIC_SHIELD	61 62

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

J2270	TRUE	SPKRAMP_L_N_OUT	60 61 85
J2260	TRUE	SPKRAMP_L_P_OUT	60 61 85
J2230	TRUE	SPKRAMP_R_N_OUT	60 61 85
J2280	TRUE	SPKRAMP_R_P_OUT	60 61 85
J2250	TRUE	SPKRAMP_SUB_N_OUT	60 61 85
J2310	TRUE	SPKRAMP_SUB_P_OUT	60 61 85

LVDS FUNC_TEST

J7900	TRUE	PP3V3_LCDVDD_SW_F (NEED 2 TP)	6 74
J7901	TRUE	PP3V3_S0_LCD_F	6 74
J7902	TRUE	PPVOUT_SW_LCDBKLT (NEED 2 TP)	74 77
J7903	TRUE	BKL_VSYNC	74 77
J7400	TRUE	LVDS_DDC_CLK	8 18 74
J7401	TRUE	LVDS_DDC_DATA	8 18 74
J7904	TRUE	LVDS_IG_A_DATA_N<0>	18 74 80
J7905	TRUE	LVDS_IG_A_DATA_P<0>	18 74 80
J7906	TRUE	LVDS_IG_A_DATA_N<1>	18 74 80
J7907	TRUE	LVDS_IG_A_DATA_P<1>	18 74 80
J7908	TRUE	LVDS_IG_A_DATA_N<2>	18 74 80
J7909	TRUE	LVDS_IG_A_DATA_P<2>	18 74 80
J7910	TRUE	LVDS_CONN_A_CLK_F_N	74 85
J7911	TRUE	LVDS_CONN_A_CLK_F_P	74 85
J7912	TRUE	LED_RETURN_1	74 77
J7913	TRUE	LED_RETURN_2	74 77
J7914	TRUE	LED_RETURN_3	74 77
J7915	TRUE	LED_RETURN_4	74 77
J7916	TRUE	LED_RETURN_5	74 77
J7917	TRUE	LED_RETURN_6	74 77

(NEED TO ADD 5 GND TP)

SATA ODD CONN

J7200	TRUE	PP5V_SW_ODD (NEED 2 TP)	6 42
J7201	TRUE	SMC_ODD_DETECT	42 45
J7202	TRUE	SATA_ODD_D2R_UF_P	42 85
J7203	TRUE	SATA_ODD_D2R_UF_N	42 85
J7204	TRUE	SATA_ODD_R2D_P	42 80
J7205	TRUE	SATA_ODD_R2D_N	42 80

(NEED TO ADD 3 GND TP)

SATA HDD/IR/SIL

J7310	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	6 42
J7314	TRUE	SATA_HDD_R2D_P	42 80
J7315	TRUE	SATA_HDD_R2D_N	42 80
J7316	TRUE	SATA_HDD_D2R_C_P	42 80
J7317	TRUE	SATA_HDD_D2R_C_N	42 80
J7307	TRUE	SYS_LED_ANODE_R	42
J7306	TRUE	IR_RX_OUT	42 44
J7311	TRUE	PP5V_S3_IR_R	42

(NEED TO ADD 3 GND TP)

BATT POWER CONN

J7322	TRUE	SMBUS_SMC_BSA_SCL	6 45 48 63 64 84
J7321	TRUE	SMBUS_SMC_BSA_SDA	6 45 48 63 64 84
J7320	TRUE	SYS_DETECT_L	63
J7305	TRUE	PPVBAT_G3H_CONN (NEED 5 TP)	63 64

(NEED TO ADD 5 GND TP)

BIL CONN

J7325	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
J7324	TRUE	SMBUS_SMC_BSA_SCL	6 45 48 63 64 84
J7323	TRUE	SMBUS_SMC_BSA_SDA	6 45 48 63 64 84
J7326	TRUE	SMC_BIL_BUTTON_L	45 46 63
J7308	TRUE	SMC_LID_R	63

(NEED TO ADD 2 GND TP)

X19 CONN

J7900	TRUE	PP3V3_WLAN (NEED 3 TP)	6 32 46
J7901	TRUE	PCIE_AP_D2R_PI_P	32 81
J7902	TRUE	PCIE_AP_D2R_PI_N	32 81
J7903	TRUE	PCIE_AP_R2D_P	32 81
J7904	TRUE	PCIE_AP_R2D_N	32 81
J7905	TRUE	PCIE_CLK100M_AP_CONN_P	32 85
J7906	TRUE	PCIE_CLK100M_AP_CONN_N	32 85
J7907	TRUE	PP3V3_S3_BT_F	32
J7908	TRUE	PCIE_WAKE_L	17 26 32
J7909	TRUE	SMBUS_SMC_0_S0_SCL	32 45 48 51 84
J7910	TRUE	SMBUS_SMC_0_S0_SDA	32 45 48 51 84
J7911	TRUE	USB_BT_P	24 32 80
J7912	TRUE	USB_BT_N	24 32 80
J7913	TRUE	AP_CLKREQ_O_L	32
J7914	TRUE	AP_RESET_CONN_L	32
J7915	TRUE	AP_TEMP_SMB_SDA_R	32
J7916	TRUE	AP_TEMP_SMB_SCL_R	32
J7917	TRUE	WIFI_EVENT_L_R	32

(NEED TO ADD 5 GND TP)

IPD_FLEX_CONN

J7370	TRUE	PP3V3_S5	76 85 6 7 8 17 19 20 22 23 24 26 30 46 56 66 72 73 74 76 85
J7371	TRUE	PP18V5_S5	6 54
J7372	TRUE	Z2_CS_L	53 54
J7373	TRUE	Z2_DEBUG3	53 54
J7374	TRUE	Z2_MOSI	53 54
J7375	TRUE	Z2_MISO	53 54
J7376	TRUE	Z2_SCLK	53 54
J7377	TRUE	Z2_BOOST_EN	54
J7378	TRUE	Z2_HOST_INTN	53 54
J7379	TRUE	Z2_CLKIN	53 54
J7380	TRUE	Z2_KEY_ACT_L	53 54
J7381	TRUE	Z2_RESET	53 54
J7382	TRUE	PSOC_MISO	53 54
J7383	TRUE	PSOC_MOSI	53 54
J7384	TRUE	PSOC_SCLK	53 54
J7385	TRUE	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55 84
J7386	TRUE	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55 84
J7387	TRUE	PSOC_F_CS_L	53 54
J7500	TRUE	PICKB_L	53 54

(NEED TO ADD 2 GND TP)

KEYBOARD CONN

J7340	TRUE	PP3V3_S5	6 7 8 17 19 20 22 23 24 26 30 46 56 66 72 73 74 76 85
J7341	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
J7342	TRUE	WS_KBD1	53
J7343	TRUE	WS_KBD2	53
J7344	TRUE	WS_KBD3	53
J7345	TRUE	WS_KBD4	53
J7346	TRUE	WS_KBD5	53
J7347	TRUE	WS_KBD6	53
J7348	TRUE	WS_KBD7	53
J7349	TRUE	WS_KBD8	53
J7350	TRUE	WS_KBD9	53
J7351	TRUE	WS_KBD10	53
J7352	TRUE	WS_KBD11	53
J7353	TRUE	WS_KBD12	53
J7354	TRUE	WS_KBD13	53
J7355	TRUE	WS_KBD14	53
J7356	TRUE	WS_KBD15_CAP	53
J7357	TRUE	WS_KBD16_NUM	53
J7358	TRUE	WS_KBD17	53
J7359	TRUE	WS_KBD18	53
J7360	TRUE	WS_KBD19	53
J7361	TRUE	WS_KBD20	53
J7362	TRUE	WS_KBD21	53
J7363	TRUE	WS_KBD22	53
J7364	TRUE	WS_KBD23	53
J7365	TRUE	WS_KBD_ONOFF_L	53
J7366	TRUE	WS_LEFT_SHIFT_KBD	53
J7367	TRUE	WS_LEFT_OPTION_KBD	53
J7368	TRUE	WS_CONTROL_KBD	53

(NEED TO ADD 2 GND TP)

KBD BACKLIGHT CONN

J7354	TRUE	KBDLED_ANODE	54
J7394	TRUE	SMC_KDBLED_PRESENT_L	54

(NEED TO ADD 1 GND TP)

CAMERA/ALS CONN

J7400	TRUE	PP5V_S3_ALSCAMERA_F	32
J7409	TRUE	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55 84
J7410	TRUE	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55 84
J7397	TRUE	USB_CAMERA_CONN_P	32 80
J7396	TRUE	USB_CAMERA_CONN_N	32 80

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

J7200	TRUE	PPVCORE_S0_CPU	7 9 12 14 49 69
J7201	TRUE	PPVCORE_S0_AXG	7 9 12 15 49 69
J7430	TRUE	PP1V2_S3_ENET_INTREG	37 71
J7202	TRUE	PP1V05_S0	45 60 70 73
J7203	TRUE	PP1V5_S3RS0	7 9 10 12 14 16 17 20 22 23 36 40 85
J7204	TRUE	PP1V8_S0	7 14 17 20 22 26 71
J7205	TRUE	PP3V3_S0	29 33 36 37 40 48 6 7 8 12 16 17 50 18 19 20 22 23 26 27 51 52 54 57 61 65 71 74 75 77 85
J7206	TRUE	PP5V_S0	18 6
J7207	TRUE	PP3V3_S3	7 8 18 24 26 30 31 32 33 48 50 54 55 72 73
J7208	TRUE	PP5V_S3	7 30 32 42 43 44 46 57 59 60 61 66 67 72
J7410	TRUE	PPVCCSA_S0_CPU	7 12 15 16 6 65
J7211	TRUE	PP3V3_S5	47 48 53 63 64 73
J7212	TRUE	PP3V42_G3H	6 7 26 43 45 46 6
J7213	TRUE	PPBUS_G3H	7 8 36 40 49 50 63 64 77
J7417	TRUE	PP3V3_ENET	7 26 37 71 73
J7214	TRUE	PP3V3_WLAN	6 32 46
J7215	TRUE	PP5V_SW_ODD	6 42
J7216	TRUE	PP5V_S0_HDD_FLT	6 42
J7217	TRUE	PP18V5_S5	6 54
J7218	TRUE	PP3V3_S0_LCD_F	6 74
J7410	TRUE	PP3V3_LCDVDD_SW_F	6 74
J7219	TRUE	PP4V5_AUDIO_ANALOG	57
J7410	TRUE	PP1V5_S3	7 27 29 30 67 72
J7220	TRUE	SMC_PM_G2_EN	45 73
J7545	TRUE	PM_SLP_S4_L	17 30 45 73
J7546	TRUE	PM_SLP_S3_L	17 30 45 73

(NEED TO ADD 6 GND TP)

DC POWER CONN

(NEED 3 TP)

J7552	TRUE	PP18V5_DCIN_FUSE	63
J7554	TRUE	ADAPTER_SENSE	63

(NEED TO ADD 4 GND TP)

LPC+SPI DEBUG_CONN

J6500	TRUE	LPC_AD<0>	16 45 47 81
J6501	TRUE	LPC_AD<1>	16 45 47 81
J6502	TRUE	LPC_AD<2>	16 45 47 81
J6503	TRUE	LPC_AD<3>	16 45 47 81
J6504	TRUE	LPC_CLK33M_LPCPLUS	26 47 81
J6505	TRUE	LPC_FRAME_L	16 45 47 81
J6506	TRUE	LPC_PWRDWN_L	17 45 47
J6507	TRUE	LPC_SERIRQ	16 45 47
J6508	TRUE	LPCPLUS_GPIO	19 47
J6509	TRUE	LPCPLUS_RESET_L	26 47 81
J6510	TRUE	PM_CLKRUN_L	17 45 47
J6511	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
J6512	TRUE	PP5V_S0	6 7 22 42 47 52 54 65 68 70 72 73 77
J6513	TRUE	SMC_MD1	45 47
J6514	TRUE	SMC_RX_L	43 45 46 47
J6515	TRUE	SMC_TCK	45 46 47
J6516	TRUE	SMC_TDI	45 46 47
J6517	TRUE	SMC_TDO	45 46 47
J6518	TRUE	SMC_TMS	45 46 47
J6519	TRUE	SMC_TRST_L	45 47
J6520	TRUE	SMC_TX_L	43 45 46 47
J6521	TRUE	SPI_ALT_CLK	47
J6522	TRUE	SPI_ALT_CS_L	47
J6523	TRUE	SPI_ALT_MISO	47
J6524	TRUE	SPI_ALT_MOSI	47
J6525	TRUE	SPIROM_USE_MLB	19 47 56

(NEED TO ADD 2 GND TP)

NC NO_TESTs

NO_TEST

17 6	NC_CRT_IG_BLUE	TRUE MAKE_BASE=TRUE	NC_CRT_IG_BLUE 6 17
17 6	NC_CRT_IG_GREEN	TRUE MAKE_BASE=TRUE	NC_CRT_IG_GREEN 6 17
17 6	NC_CRT_IG_RED	TRUE MAKE_BASE=TRUE	NC_CRT_IG_RED 6 17
17 6	NC_CRT_IG_DDC_CLK	TRUE MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK 6 17
17 6	NC_CRT_IG_DDC_DATA	TRUE MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA 6 17
17 6	NC_CRT_IG_HSYNC	TRUE MAKE_BASE=TRUE	NC_CRT_IG_HSYNC 6 17
17 6	NC_CRT_IG_VSYNC	TRUE MAKE_BASE=TRUE	NC_CRT_IG_VSYNC 6 17
6	NC_LVDS_IG_CTRL_CLK	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK 6 18
6	NC_LVDS_IG_CTRL_DATA	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA 6 18
6	NC_PCH_LVDS_VBG	TRUE MAKE_BASE=TRUE	NC_PCH_LVDS_VBG 6 18
6	NC_HDA_SDIN1	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN1 6 9 16
6	NC_HDA_SDIN2	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN2 6 16
6	NC_HDA_SDIN3	TRUE MAKE_BASE=TRUE	NC_HDA_SDIN3 6 16
18 6	NC_PCI_PME_L	TRUE MAKE_BASE=TRUE	NC_PCI_PME_L 6 18
18 6	NC_PCI_CLK33M_OUT3	TRUE MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3 6 18
16 6	NC_CLINK_CLK	MAKE_BASE=TRUE	NC_CLINK_CLK 6 16
16 6	NC_CLINK_DATA	MAKE_BASE=TRUE	NC_CLINK_DATA 6 16
16 6	NC_CLINK_RESET_L	TRUE MAKE_BASE=TRUE	NC_CLINK_RESET_L 6 16
16 6	NC_PCIE_CLK100M_PEBN	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN 6 16
16 6	NC_PCIE_CLK100M_PEBP	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP 6 16
39 6	NC_FW643_SDA	MAKE_BASE=TRUE	NC_FW643_SDA 6 39
39 6	NC_FW643_SM	TRUE MAKE_BASE=TRUE	NC_FW643_SM 6 39
39 6	NC_FW643_TCK	TRUE MAKE_BASE=TRUE	NC_FW643_TCK 6 39
39 6	NC_FW643_TMS	TRUE MAKE_BASE=TRUE	NC_FW643_TMS 6 39
39 6	NC_FW643_FW620_L	TRUE MAKE_BASE=TRUE	NC_FW643_FW620_L 6 39
39 6	NC_FW643_VBUF	TRUE MAKE_BASE=TRUE	NC_FW643_VBUF 6 39
39 6	NC_FW643_OCR10_CTL	TRUE MAKE_BASE=TRUE	NC_FW643_OCR10_CTL 6 39
39 6	NC_FW643_AVREG	TRUE MAKE_BASE=TRUE	NC_FW643_AVREG 6 39
39 6	NC_FW643_TDI	TRUE MAKE_BASE=TRUE	NC_FW643_TDI 6 39
23 6	TP_XDP_PCH_OBSFN_A<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1> 6 23
23 6	TP_XDP_PCH_OBSFN_B<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1> 6 23
23 6	NC_TP_XDPPCH_HOOK2	TRUE MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2 6 23
23 6	NC_TP_XDPPCH_HOOK3	TRUE MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3 6 23
23 6	TP_XDP_PCH_OBSFN_D<0..1>	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1> 6 23
23 6	NC_TP_XDP_PCH_HOOK4	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4 6 23
23 6	NC_TP_XDP_PCH_HOOK5	TRUE MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5 6 23
16 6	NC_PCH_GPIO64_CLKOUTFLEX0	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0 6 16
16 6	NC_PCH_GPIO65_CLKOUTFLEX1	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1 6 16
16 6	NC_PCH_GPIO66_CLKOUTFLEX2	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2 6 16
16 6	NC_PCH_GPIO67_CLKOUTFLEX3	TRUE MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3 6 16

NC NO_TESTs

NO_TEST

J4600	TRUE	NC_FW2_TPBP	39 41
J4598	TRUE	NC_FW2_TPBN	39 41
J4596	TRUE	NC_FW2_TPBIAS	39 41
J4597	TRUE	NC_FW2_TPAP	39 41
J4595	TRUE	NC_FW2_TPAN	39 41
J4594	TRUE	NC_FW0_TPBP	39 41 82
J4592	TRUE	NC_FW0_TPBN	39 41 82
J4593	TRUE	NC_FW0_TPAP	39 41 82

J4492	TRUE	XDP_PCH_AP_PWR_EN	
J4493	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	23
J4494	TRUE	XDP_PCH_SDCONN_STATE_RST_L	23
J4488	TRUE	XDP_PCH_ENET_PWR_EN	23
J4489	TRUE	XDP_PCH_SDCONN_DET_L	23
J4482	TRUE	XDP_PCH_S5_PWRGD	23
J4483	TRUE	XDP_PCH_PWRBTN_L	23
J4484	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	23
J4485	TRUE	XDP_FW_CLKREQ_L	23
J4486	TRUE	XDP_AP_CLKREQ_L	23
J4487	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	23

17 6	NC_SDVO_TVCLKINN	TRUE MAKE_BASE=TRUE	NC_SDVO_TVCLKINN 6 17
17 6	NC_SDVO_TVCLKINP	TRUE MAKE_BASE=TRUE	NC_SDVO_TVCLKINP 6 17
17 6	NC_SDVO_STALLN	TRUE MAKE_BASE=TRUE	NC_SDVO_STALLN 6 17
17 6	NC_SDVO_STALLP	TRUE MAKE_BASE=TRUE	NC_SDVO_STALLP 6 17
17 6	NC_SDVO_INTN	TRUE MAKE_BASE=TRUE	NC_SDVO_INTN 6 17
17 6	NC_SDVO_INTP	TRUE MAKE_BASE=TRUE	NC_SDVO_INTP 6 17

9	NC_EDP_TXP<0..3>	TRUE MAKE_BASE=TRUE	TP_EDP_TX_P<0..3>
9	NC_EDP_TXN<0..3>	TRUE MAKE_BASE=TRUE	TP_EDP_TX_N<0..3>
9 6	NC_EDP_AUXP	TRUE MAKE_BASE=TRUE	NC_EDP_AUXP
9 6	NC_EDP_AUXN	TRUE MAKE_BASE=TRUE	NC_EDP_AUXN 6 9
6	NC_CPU_THERMDA	TRUE MAKE_BASE=TRUE	NC_CPU_THERMDA
6	NC_CPU_THERMDC	TRUE MAKE_BASE=TRUE	NC_CPU_THERMDC
	NC_CPU_RSVD<30..45>	TRUE MAKE_BASE=TRUE	TP_CPU_RSVD<30..45>
	NC_CPU_RSVD<8..27>	TRUE MAKE_BASE=TRUE	TP_CPU_RSVD<8..27>
9	NC_PEG_R2D_CP<0..7>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_P<0..7> 9
9	NC_PEG_R2D_CN<0..7>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_N<0..7> 9
9	NC_PEG_D2RP<0..7>	TRUE MAKE_BASE=TRUE	=PEG_D2R_P<0..7> 9
9	NC_PEG_D2RN<0..7>	TRUE MAKE_BASE=TRUE	=PEG_D2R_N<0..7> 9
9	NC_PEG_R2D_CP<12..15>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_P<12..15> 9
9	NC_PEG_R2D_CN<12..15>	TRUE MAKE_BASE=TRUE	=PEG_R2D_C_N<12..15> 9
9	NC_PEG_D2RP<12..15>	TRUE MAKE_BASE=TRUE	=PEG_D2R_P<12..15> 9
9	NC_PEG_D2RN<12..15>	TRUE MAKE_BASE=TRUE	=PEG_D2R_N<12..15> 9
6	NC_PCIE_CLK100M_PE4N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N 6
6	NC_PCIE_CLK100M_PE4P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P 6
6 16	NC_PCIE_CLK100M_PE5N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N 6 16
6 16	NC_PCIE_CLK100M_PE5P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P 6 16
6 19	NC_PCIE_CLK100M_PE6N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N 6 19
6 19	NC_PCIE_CLK100M_PE6P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P 6 19
6 19	NC_PCIE_CLK100M_PE7N	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N 6 19
6 19	NC_PCIE_CLK100M_PE7P	TRUE MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P 6 19
53 6	NC_PSOC_P1_3	TRUE MAKE_BASE=TRUE	NC_PSOC_P1_3 6 53
16 6	NC_SATA_B_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_B_D2RN 6 16
16 6	NC_SATA_B_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_B_D2RP 6 16
16 6	NC_SATA_B_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_B_R2D_CN 6 16
16 6	NC_SATA_B_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_B_R2D_CP 6 16
16 6	NC_SATA_D_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RN 6 16
16 6	NC_SATA_D_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_D_D2RP 6 16
16 6	NC_SATA_D_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CN 6 16
16 6	NC_SATA_D_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_D_R2D_CP 6 16
16 6	NC_SATA_E_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RN 6 16
16 6	NC_SATA_E_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_E_D2RP 6 16
16 6	NC_SATA_E_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CN 6 16
16 6	NC_SATA_E_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_E_R2D_CP 6 16
16 6	NC_SATA_F_D2RN	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RN 6 16
16 6	NC_SATA_F_D2RP	TRUE MAKE_BASE=TRUE	NC_SATA_F_D2RP 6 16
16 6	NC_SATA_F_R2D_CN	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CN 6 16
16 6	NC_SATA_F_R2D_CP	TRUE MAKE_BASE=TRUE	NC_SATA_F_R2D_CP 6 16
6	NC_PCH_TP18	TRUE MAKE_BASE=TRUE	NC_PCH_TP18 6
6	NC_PCH_TP17	TRUE MAKE_BASE=TRUE	NC_PCH_TP17 6
6	NC_PCH_TP16	TRUE MAKE_BASE=TRUE	NC_PCH_TP16 6
6	NC_PCH_TP15	TRUE MAKE_BASE=TRUE	NC_PCH_TP15 6
6	NC_PCH_TP14	TRUE MAKE_BASE=TRUE	NC_PCH_TP14 6
6	NC_PCH_TP13	TRUE MAKE_BASE=TRUE	NC_PCH_TP13 6
6	NC_PCH_TP12	TRUE MAKE_BASE=TRUE	NC_PCH_TP12 6
6	NC_PCH_TP10	TRUE MAKE_BASE=TRUE	NC_PCH_TP10 6
6	NC_PCH_TP9	TRUE MAKE_BASE=TRUE	NC_PCH_TP9 6
6	NC_PCH_TP8	TRUE MAKE_BASE=TRUE	NC_PCH_TP8 6
6	NC_PCH_TP7	TRUE MAKE_BASE=TRUE	NC_PCH_TP7 6
6	NC_PCH_TP6	TRUE MAKE_BASE=TRUE	NC_PCH_TP6 6
6	NC_PCH_TP5	TRUE MAKE_BASE=TRUE	NC_PCH_TP5 6
6	NC_PCH_TP4	TRUE MAKE_BASE=TRUE	NC_PCH_TP4 6
6	NC_PCH_TP3	TRUE MAKE_BASE=TRUE	NC_PCH_TP3 6
6	NC_PCH_TP2	TRUE MAKE_BASE=TRUE	NC_PCH_TP2 6
6	NC_PCH_TP1	TRUE MAKE_BASE=TRUE	NC_PCH_TP1 6
81	PCH_VSS_NCTF<1>	TRUE	PCH_VSS_NCTF<15> 6 81
81	PCH_VSS_NCTF<2>	TRUE	PCH_VSS_NCTF<17> 6 81
81	PCH_VSS_NCTF<5>	TRUE	PCH_VSS_NCTF<19> 6 81
81	PCH_VSS_NCTF<9>	TRUE	PCH_VSS_NCTF<19> 6 81
81	PCH_VSS_NCTF<11>	TRUE	PCH_VSS_NCTF<21> 6 81
81	PCH_VSS_NCTF<12>	TRUE	PCH_VSS_NCTF<25> 6 81
		TRUE	PCH_VSS_NCTF<27> 6 81
		TRUE	PCH_VSS_NCTF<29> 6 81
80 18 8	TP_LVDS_IG_B_CLKN	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN
80 18 8	TP_LVDS_IG_B_CLKP	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
6	NC_LVDS_IG_BKL_PWM	TRUE MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
6	NC_SMC_BS_ALRT_L	TRUE MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L 6

SYNC_MASTER=K24_MLB

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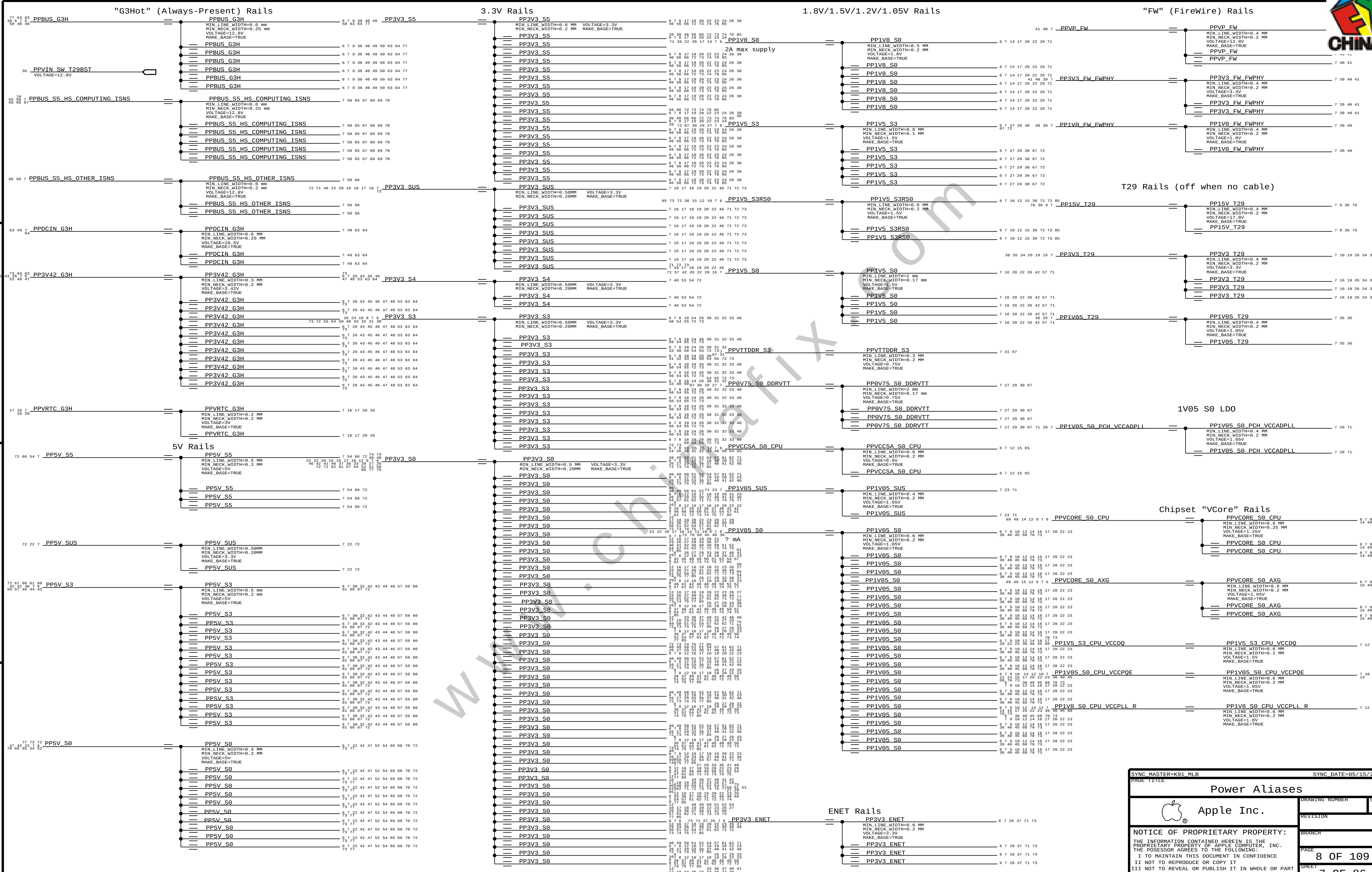

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

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Power Aliases

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HEATSINK STANDOFFS

Z0902
STDOFF-4.50D.98H-1.1-3.48-TH

Z0904
STDOFF-4.50D.98H-1.1-3.48-TH

BELOW CPU

Z0920
STDOFF-4.50D.98H-1.1-3.48-TH

LEFT OF CPU

FAN STANDOFF

Z0905
STDOFF-4.50D.98H-1.1-3.48-TH

MLB MOUNTING (TO C. BRACKET) SCREW HOLES

OMIT Z0906 3R2P5

OMIT Z0907 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT Z0908 3R2P5

OMIT Z0909 3R2P5

OMIT Z0910 3R2P5

OMIT Z0911 3R2P5

OMIT Z0912 3R2P5

EMI IO (SHORT) POGO PINS

ZS0900 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0901 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0902 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0903 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0908 1.4DIA-SHORT-EMI-MLB-K19-K24

ZS0909 1.4DIA-SHORT-EMI-MLB-K19-K24

EMI TALL POGO PINS

ZS0904 2.0DIA-TALL-EMI-MLB-M97-M98

ZS0905 2.0DIA-TALL-EMI-MLB-M97-M98

ZS0906 2.0DIA-TALL-EMI-MLB-M97-M98

ZS0907 2.0DIA-TALL-EMI-MLB-M97-M98

Heat Spreader Holes for T29, PCH

Z0950 STDOFF-4.00D1.85H-SM

Z0951 STDOFF-4.00D1.85H-SM

Z0952 STDOFF-4.00D1.85H-SM

CPU signals

MEMVTT_EN = MEMVTT_EN (MAKE_BASE=TRUE)

DP_EXTA_ML_C_P<3..0> → DP_IG_ML_P<3..0> → TP_DP_IG_B_MLP<3..0>

DP_EXTA_ML_C_N<3..0> → DP_IG_ML_N<3..0> → TP_DP_IG_B_MLN<3..0>

DP_EXTA_AUXCH_C_P → DP_EXTA_AUXCH_C_P

DP_EXTA_AUXCH_C_N → DP_EXTA_AUXCH_C_N

=PEG_R2D_C_P<11..8> → PEG_R2D_C_P<11..8> → PCIE_T29_R2D_C_P<3..0>

=PEG_R2D_C_N<11..8> → PEG_R2D_C_N<11..8> → PCIE_T29_R2D_C_N<3..0>

=PEG_D2R_P<11..8> → PEG_D2R_P<11..8> → PCIE_T29_D2R_P<3..0>

=PEG_D2R_N<11..8> → PEG_D2R_N<11..8> → PCIE_T29_D2R_N<3..0>

FW_PLUG_DET_L = FW_PLUG_DET_L

FW643_WAKE_L = FW643_WAKE_L

TP_SMC_EXCARD_PWR_EN = TP_SMC_EXCARD_PWR_EN

NC_PCIE_EXCARD_D2RN = NC_PCIE_EXCARD_D2RN

NC_PCIE_EXCARD_D2RP = NC_PCIE_EXCARD_D2RP

NC_PCIE_EXCARD_R2D_CN = NC_PCIE_EXCARD_R2D_CN

NC_PCIE_EXCARD_R2D_CP = NC_PCIE_EXCARD_R2D_CP

NC_PCIE_CLK100M_EXCARDN = NC_PCIE_CLK100M_EXCARDN

NC_PCIE_CLK100M_EXCARDP = NC_PCIE_CLK100M_EXCARDP

PCIE_PCH_D2R_N<5..8> → NC_PCIE_PCH_D2RN<5..8>

PCIE_PCH_D2R_P<5..8> → NC_PCIE_PCH_D2RP<5..8>

PCIE_PCH_R2D_C_N<5..8> → NC_PCIE_PCH_R2D_CN<5..8>

PCIE_PCH_R2D_C_P<5..8> → NC_PCIE_PCH_R2D_CP<5..8>

NC_PEG_CLK100MP = NC_PEG_CLK100MP

NC_PEG_CLK100MN = NC_PEG_CLK100MN

NC_PCH_CLKOUT_DPN = NC_PCH_CLKOUT_DPN (TRUE, MAKE_BASE=TRUE)

NC_PCH_CLKOUT_DPP = NC_PCH_CLKOUT_DPP (TRUE, MAKE_BASE=TRUE)

TP_ISSP_SCLK_P1_1 = TP_ISSP_SCLK_P1_1

TP_ISSP_SDATA_P1_0 = TP_ISSP_SDATA_P1_0

NC_FSB_CLK133M_PCH_P = NC_FSB_CLK133M_PCH_P (NO_TEST=TRUE)

NC_FSB_CLK133M_PCH_N = NC_FSB_CLK133M_PCH_N (NO_TEST=TRUE)

T29BST:N
R0960 0 5% 1/16W MF-LF 805
PPBUS_G3H — PP15V_T29

T29_A_BIAS
C0960 0.01UF 10% 10V X5R 201

DP_A_BIAS0
C0962 0.01UF 10% 10V X5R 201

DP_A_BIAS2
C0964 0.01UF 10% 10V X5R 201

T29_A_BIAS_R2DP1
T29_A_BIAS_R2DN0
R0971 51 1/20W 2 5% MF VOLTAGE=3.3V — T29_A_BIAS_R2DN1
T29_A_BIAS — R0970 51 1/20W 2 5% MF VOLTAGE=3.3V — T29_A_BIAS_R2DP0
C0971 0.01UF 10% 10V X5R 201
C0970 0.01UF 10% 10V X5R 201

R0973 51 1/20W 2 5% MF VOLTAGE=3.3V — T29_A_BIAS_D2RN1
R0972 51 1/20W 2 5% MF VOLTAGE=3.3V — T29_A_BIAS_D2RP1
C0973 0.01UF 10% 10V X5R 201
C0972 0.01UF 10% 10V X5R 201

T29 JTAG

JTAG_ISP_TCK = JTAG_ISP_TCK
JTAG_ISP_TDI = JTAG_ISP_TDI
JTAG_ISP_TDO = JTAG_ISP_TDO

T29 DP Ports

DP_T29SNK0_HPD = DP_T29SNK0_HPD

TP_DP_IG_C_MLP<3..0> → DP_T29SNK0_ML_C_P<3..0>

TP_DP_IG_C_MLN<3..0> → DP_T29SNK0_ML_C_N<3..0>

DP_T29SNK0_AUXCH_C_P = DP_T29SNK0_AUXCH_C_P

DP_T29SNK0_AUXCH_C_N = DP_T29SNK0_AUXCH_C_N

DP_T29SNK1_HPD = DP_T29SNK1_HPD

TP_DP_IG_D_MLP<3..0> → DP_T29SNK1_ML_C_P<3..0>

TP_DP_IG_D_MLN<3..0> → DP_T29SNK1_ML_C_N<3..0>

DP_T29SNK1_AUXCH_C_P = DP_T29SNK1_AUXCH_C_P

DP_T29SNK1_AUXCH_C_N = DP_T29SNK1_AUXCH_C_N

PP3V3_S0
R0920 2.2K 5% 1/16W MF-LF 402
R0921 2.2K 5% 1/16W MF-LF 402
R0922 2.2K 5% 1/16W MF-LF 402
R0923 2.2K 5% 1/16W MF-LF 402

DP_IG_C_CTRL_CLK = DP_IG_C_CTRL_CLK
DP_IG_C_CTRL_DATA = DP_IG_C_CTRL_DATA
DP_IG_D_CTRL_CLK = DP_IG_D_CTRL_CLK
DP_IG_D_CTRL_DATA = DP_IG_D_CTRL_DATA

PP3V3_S0
R0924 2.2K 5% 1/16W MF-LF 402
R0925 2.2K 5% 1/16W MF-LF 402

DP_EXTA_DDC_CLK = DP_EXTA_DDC_CLK
DP_EXTA_DDC_DATA = DP_EXTA_DDC_DATA
DP_EXTA_HPD = DP_EXTA_HPD

R0908 100K 5% 1/16W MF-LF 402

R0910 0 5% 1/16W MF-LF 402
PPBUS_SW_LCDBKLT_PWR — PPBUS_SW_BKL (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE) — PPBUS_SW_BKL

NC_USB_HUB1_OCS4 = NC_USB_HUB1_OCS4
NC_USB_HUB2_OCS4 = NC_USB_HUB2_OCS4
PU_USB_HUB2_PRT4_P = PU_USB_HUB2_PRT4_P
PU_USB_HUB2_PRT4_N = PU_USB_HUB2_PRT4_N

TP_BCM57765_TRAFFICLED_L = TP_BCM57765_TRAFFICLED_L

NC_BCM57765_CE_L_MS_INS_L = NC_BCM57765_CE_L_MS_INS_L (NO_TEST=TRUE)

TP_LVDS_IG_B_CLKP = TP_LVDS_IG_B_CLKP
TP_LVDS_IG_B_CLKN = TP_LVDS_IG_B_CLKN

NC_LVDS_IG_B_DATAP<0..3> → LVDS_IG_B_DATA_P<0..3>

NC_LVDS_IG_B_DATAN<0..3> → LVDS_IG_B_DATA_N<0..3>

NC_LVDS_IG_A_DATAP<3> → NC_LVDS_IG_A_DATAP<3>

NC_LVDS_IG_A_DATAN<3> → NC_LVDS_IG_A_DATAN<3>

LVDS_DDC_CLK = LVDS_DDC_CLK
LVDS_DDC_DATA = LVDS_DDC_DATA
LCD_BKLT_PWM = LCD_BKLT_PWM
LCD_IG_PWR_EN = LCD_IG_PWR_EN
LCD_BKLT_EN = LCD_BKLT_EN

DPA PWR SW : Nostuff, Backup

U0950 TPS2553 SOT-23 NOSTUFF
PP3V3_S5 — IN
SMC_S4_WAKESRC_EN — EN
GND
OUT — PP3V3_SW_DPAPWR
ILIM — DPAPWR_ILIM
FAULT* — T29_A_HV_EN
NOSTUFF R0950 20K 5% 1/16W MF-LF 402

PP3V3_S3
R0915 10K 5% 1/16W MF-LF 402 NO STUFF
R0916 10K 5% 1/16W MF-LF 402
R0903 10K 5% 1/16W MF-LF 402 NO STUFF
R0904 10K 5% 1/16W MF-LF 402 NO STUFF
R0905 10K 5% 1/16W MF-LF 402 NO STUFF
R0906 10K 5% 1/16W MF-LF 402 NO STUFF

T29_A_RSVD_N — R0917 0 1/20W — USB_T29A_N
T29_A_RSVD_P — R0918 0 1/20W — USB_T29A_P
NO STUFF

USB_EXTC_N
USB_EXTC_P
PU_USB_HUB2_PRT4_N
PU_USB_HUB2_PRT4_P

TP_CPU_VTT_SELECT = TP_CPU_VTT_SELECT

Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V)

Unused T29 Ports

T29_D2R_P<2..3> → NC_T29_D2RP<2..3> (NO_TEST=TRUE)
T29_D2R_N<2..3> → NC_T29_D2RN<2..3> (NO_TEST=TRUE)
T29_R2D_C_P<2..3> → NC_T29_R2D_CP<2..3> (NO_TEST=TRUE)
T29_R2D_C_N<2..3> → NC_T29_R2D_CN<2..3> (NO_TEST=TRUE)
T29_LSEO<2> → T29_LSOE<2>
T29_LSEO<3> → T29_LSOE<3>

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE = TP_P1V5S3RS0_RAMP_DONE
TP_DDRREG_PGOOD = TP_DDRREG_PGOOD

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

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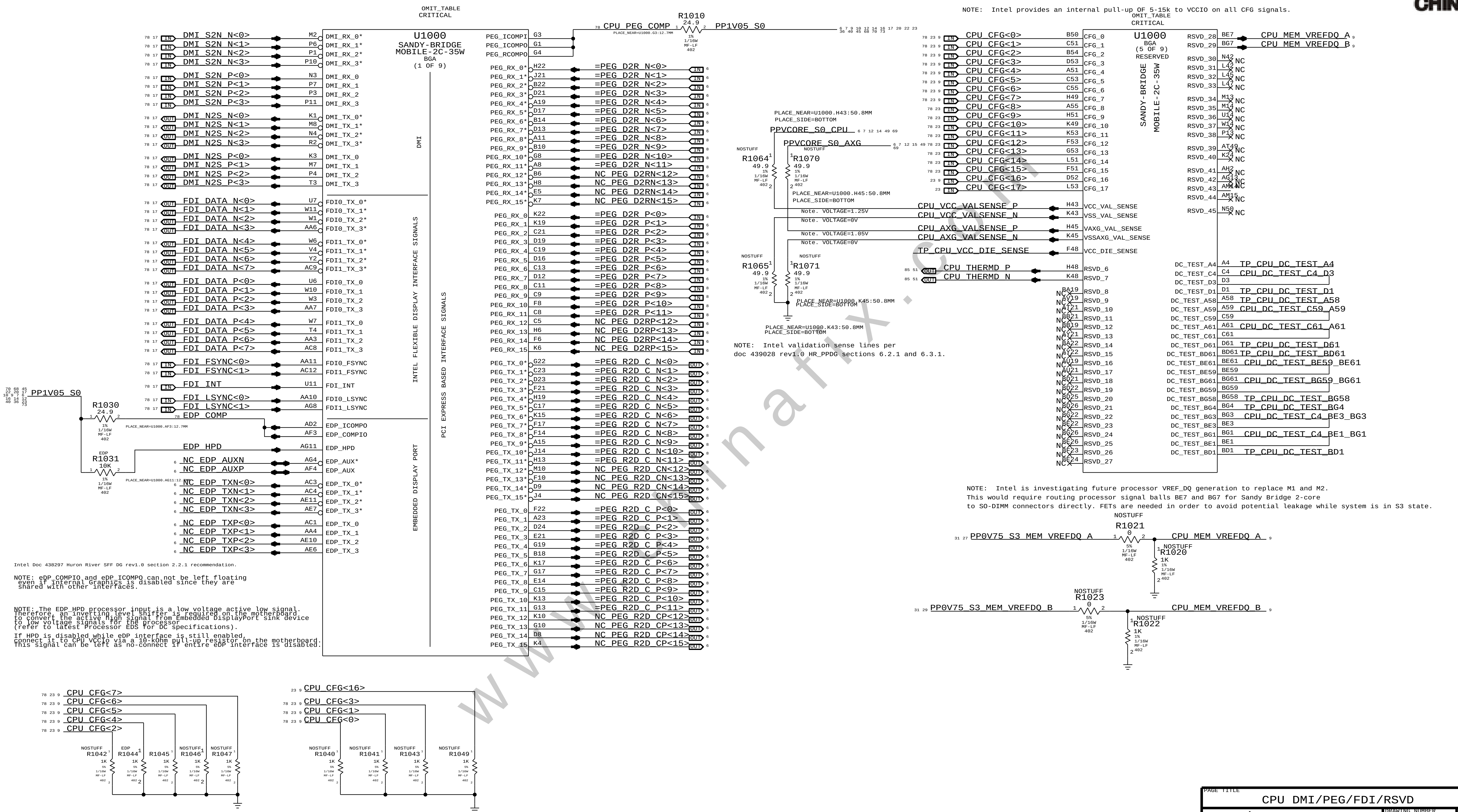

NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.

NOTE: Intel is investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls BE7 and BG7 for Sandy Bridge 2-core to SO-DIMM connectors directly. FETs are needed in order to avoid potential leakage while system is in S3 state.

Intel Doc 438297 Huron River SFF DG rev1.0 section 2.2.1 recommendation.

NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

These can be Placed close to J2500 and Only for debug access

FOR SANDYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION 0 = LANES REVERSED

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CPU DMI/PEG/FDI/RSVD

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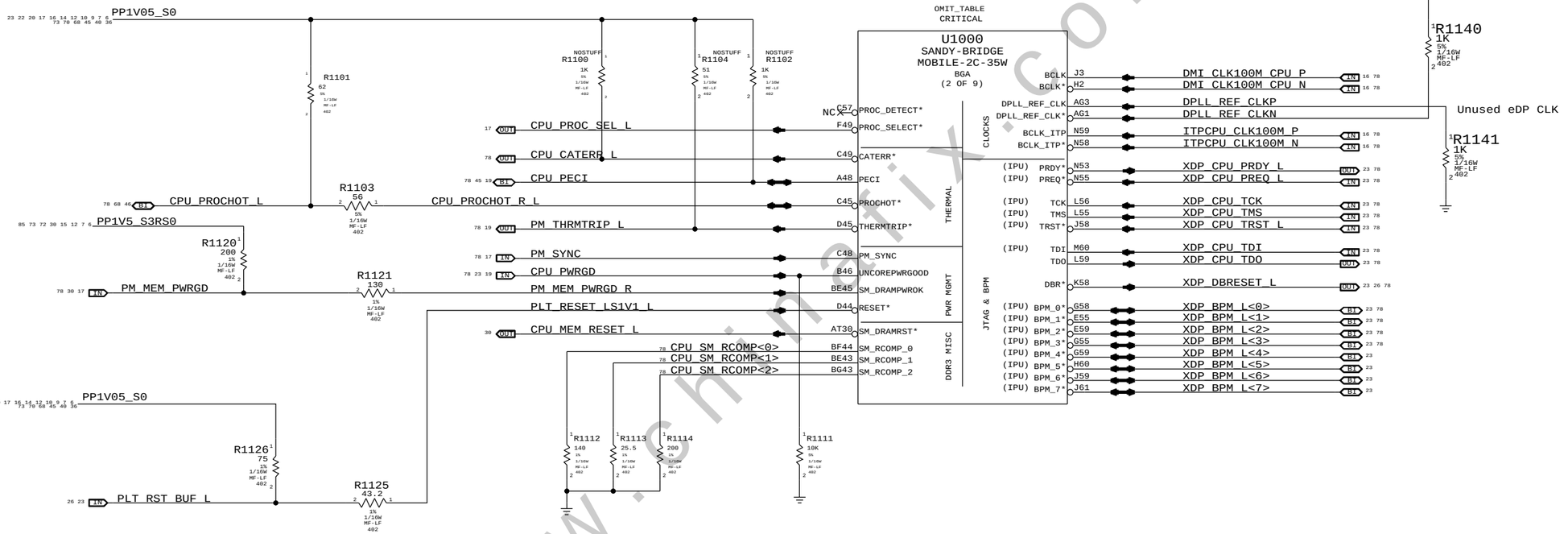

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OMIT_TABLE
CRITICAL

U1000
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SANDY-BRIDGE
MOBILE-2C-35W

MEMORY CHANNEL A

MEM_A_DQ<0>	AG6	SA_DQ_0	
MEM_A_DQ<1>	AJ6	SA_DQ_1	
MEM_A_DQ<2>	AP11	SA_DQ_2	
MEM_A_DQ<3>	AL6	SA_DQ_3	
MEM_A_DQ<4>	AJ10	SA_DQ_4	
MEM_A_DQ<5>	AJ8	SA_DQ_5	
MEM_A_DQ<6>	AL8	SA_DQ_6	
MEM_A_DQ<7>	AL7	SA_DQ_7	
MEM_A_DQ<8>	AR11	SA_DQ_8	
MEM_A_DQ<9>	AP6	SA_DQ_9	
MEM_A_DQ<10>	AU6	SA_DQ_10	
MEM_A_DQ<11>	AV9	SA_DQ_11	
MEM_A_DQ<12>	AR6	SA_DQ_12	
MEM_A_DQ<13>	AP8	SA_DQ_13	
MEM_A_DQ<14>	AT13	SA_DQ_14	
MEM_A_DQ<15>	AU13	SA_DQ_15	
MEM_A_DQ<16>	BC7	SA_DQ_16	
MEM_A_DQ<17>	BB7	SA_DQ_17	
MEM_A_DQ<18>	BA13	SA_DQ_18	
MEM_A_DQ<19>	BB11	SA_DQ_19	
MEM_A_DQ<20>	BA7	SA_DQ_20	
MEM_A_DQ<21>	BA9	SA_DQ_21	
MEM_A_DQ<22>	BB9	SA_DQ_22	
MEM_A_DQ<23>	AY13	SA_DQ_23	
MEM_A_DQ<24>	AV14	SA_DQ_24	
MEM_A_DQ<25>	AR14	SA_DQ_25	
MEM_A_DQ<26>	AY17	SA_DQ_26	
MEM_A_DQ<27>	AR19	SA_DQ_27	
MEM_A_DQ<28>	BA14	SA_DQ_28	
MEM_A_DQ<29>	AU14	SA_DQ_29	
MEM_A_DQ<30>	BB14	SA_DQ_30	
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MEM_A_DQ<32>	BA45	SA_DQ_32	
MEM_A_DQ<33>	AR43	SA_DQ_33	
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MEM_A_DQ<35>	BC48	SA_DQ_35	
MEM_A_DQ<36>	BC45	SA_DQ_36	
MEM_A_DQ<37>	AR45	SA_DQ_37	
MEM_A_DQ<38>	AT48	SA_DQ_38	
MEM_A_DQ<39>	AY48	SA_DQ_39	
MEM_A_DQ<40>	BA49	SA_DQ_40	
MEM_A_DQ<41>	AV49	SA_DQ_41	
MEM_A_DQ<42>	BB51	SA_DQ_42	
MEM_A_DQ<43>	AY53	SA_DQ_43	
MEM_A_DQ<44>	BB49	SA_DQ_44	
MEM_A_DQ<45>	AU49	SA_DQ_45	
MEM_A_DQ<46>	BA53	SA_DQ_46	
MEM_A_DQ<47>	BB55	SA_DQ_47	
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MEM_A_DQ<50>	AP50	SA_DQ_50	
MEM_A_DQ<51>	AP53	SA_DQ_51	
MEM_A_DQ<52>	AV54	SA_DQ_52	
MEM_A_DQ<53>	AT54	SA_DQ_53	
MEM_A_DQ<54>	AP56	SA_DQ_54	
MEM_A_DQ<55>	AP52	SA_DQ_55	
MEM_A_DQ<56>	AN57	SA_DQ_56	
MEM_A_DQ<57>	AN53	SA_DQ_57	
MEM_A_DQ<58>	AG56	SA_DQ_58	
MEM_A_DQ<59>	AG53	SA_DQ_59	
MEM_A_DQ<60>	AN55	SA_DQ_60	
MEM_A_DQ<61>	AN52	SA_DQ_61	
MEM_A_DQ<62>	AG55	SA_DQ_62	
MEM_A_DQ<63>	AK56	SA_DQ_63	
MEM_A_BA<0>	BD37	SA_BS_0	
MEM_A_BA<1>	BF36	SA_BS_1	
MEM_A_BA<2>	BA28	SA_BS_2	
MEM_A_CAS_L	BE39	SA_CAS*	
MEM_A_RAS_L	BD39	SA_RAS*	
MEM_A_WE_L	AT41	SA_WE*	

SA_CK_0	AU36	MEM_A_CLK_P<0>	
SA_CK_0*	AV36	MEM_A_CLK_N<0>	
SA_CKE_0	AY26	MEM_A_CKE<0>	
SA_CK_1	AT40	MEM_A_CLK_P<1>	
SA_CK_1*	AU40	MEM_A_CLK_N<1>	
SA_CKE_1	BB26	MEM_A_CKE<1>	
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SA_CS_1*	BC41	MEM_A_CS_L<1>	
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SA_ODT_1	BA41	MEM_A_ODT<1>	
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SA_DQS_1*	AR8	MEM_A_DQS_N<1>	
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SA_DQS_3*	AT17	MEM_A_DQS_N<3>	
SA_DQS_4*	AV45	MEM_A_DQS_N<4>	
SA_DQS_5*	AY51	MEM_A_DQS_N<5>	
SA_DQS_6*	AT55	MEM_A_DQS_N<6>	
SA_DQS_7*	AK55	MEM_A_DQS_N<7>	
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SA_DQS_1	AR10	MEM_A_DQS_P<1>	
SA_DQS_2	AY11	MEM_A_DQS_P<2>	
SA_DQS_3	AU17	MEM_A_DQS_P<3>	
SA_DQS_4	AW45	MEM_A_DQS_P<4>	
SA_DQS_5	AV51	MEM_A_DQS_P<5>	
SA_DQS_6	AT56	MEM_A_DQS_P<6>	
SA_DQS_7	AK54	MEM_A_DQS_P<7>	
SA_MA_0	BG35	MEM_A_A<0>	
SA_MA_1	BB34	MEM_A_A<1>	
SA_MA_2	BE35	MEM_A_A<2>	
SA_MA_3	BD35	MEM_A_A<3>	
SA_MA_4	AT34	MEM_A_A<4>	
SA_MA_5	AU34	MEM_A_A<5>	
SA_MA_6	BB32	MEM_A_A<6>	
SA_MA_7	AT32	MEM_A_A<7>	
SA_MA_8	AY32	MEM_A_A<8>	
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SA_MA_11	BA30	MEM_A_A<11>	
SA_MA_12	BC30	MEM_A_A<12>	
SA_MA_13	AW41	MEM_A_A<13>	
SA_MA_14	AY28	MEM_A_A<14>	
SA_MA_15	AU26	MEM_A_A<15>	

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MEMORY CHANNEL B

MEM_B_DQ<0>	AL4	SB_DQ_0	
MEM_B_DQ<1>	AL1	SB_DQ_1	
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MEM_B_DQ<4>	AK4	SB_DQ_4	
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MEM_B_DQ<6>	AN4	SB_DQ_6	
MEM_B_DQ<7>	AR1	SB_DQ_7	
MEM_B_DQ<8>	AU4	SB_DQ_8	
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MEM_B_DQ<10>	AV4	SB_DQ_10	
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MEM_B_DQ<16>	BE9	SB_DQ_16	
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MEM_B_DQ<53>	AU61	SB_DQ_53	
MEM_B_DQ<54>	AN58	SB_DQ_54	
MEM_B_DQ<55>	AR58	SB_DQ_55	
MEM_B_DQ<56>	AK58	SB_DQ_56	
MEM_B_DQ<57>	AL58	SB_DQ_57	
MEM_B_DQ<58>	AG58	SB_DQ_58	
MEM_B_DQ<59>	AG59	SB_DQ_59	
MEM_B_DQ<60>	AM60	SB_DQ_60	
MEM_B_DQ<61>	AL59	SB_DQ_61	
MEM_B_DQ<62>	AF61	SB_DQ_62	
MEM_B_DQ<63>	AH60	SB_DQ_63	
MEM_B_BA<0>	BG39	SB_BS_0	
MEM_B_BA<1>	BD42	SB_BS_1	
MEM_B_BA<2>	AT22	SB_BS_2	
MEM_B_CAS_L	AV43	SB_CAS*	
MEM_B_RAS_L	BF40	SB_RAS*	
MEM_B_WE_L	BD45	SB_WE*	

SB_CK_0	BA34	MEM_B_CLK_P<0>	
SB_CK_0*	AY34	MEM_B_CLK_N<0>	
SB_CKE_0	AR22	MEM_B_CKE<0>	
SB_CK_1	BA36	MEM_B_CLK_P<1>	
SB_CK_1*	BB36	MEM_B_CLK_N<1>	
SB_CKE_1	BF27	MEM_B_CKE<1>	
SB_CS_0*	BE41	MEM_B_CS_L<0>	
SB_CS_1*	BE47	MEM_B_CS_L<1>	
SB_ODT_0	AT43	MEM_B_ODT<0>	
SB_ODT_1	BG47	MEM_B_ODT<1>	
SB_DQS_0*	AL3	MEM_B_DQS_N<0>	
SB_DQS_1*	AV3	MEM_B_DQS_N<1>	
SB_DQS_2*	BG11	MEM_B_DQS_N<2>	
SB_DQS_3*	BD17	MEM_B_DQS_N<3>	
SB_DQS_4*	BG51	MEM_B_DQS_N<4>	
SB_DQS_5*	BA59	MEM_B_DQS_N<5>	
SB_DQS_6*	AT60	MEM_B_DQS_N<6>	
SB_DQS_7*	AK59	MEM_B_DQS_N<7>	
SB_DQS_0	AM2	MEM_B_DQS_P<0>	
SB_DQS_1	AV1	MEM_B_DQS_P<1>	
SB_DQS_2	BE11	MEM_B_DQS_P<2>	
SB_DQS_3	BD18	MEM_B_DQS_P<3>	
SB_DQS_4	BE51	MEM_B_DQS_P<4>	
SB_DQS_5	BA61	MEM_B_DQS_P<5>	
SB_DQS_6	AR59	MEM_B_DQS_P<6>	
SB_DQS_7	AK61	MEM_B_DQS_P<7>	
SB_MA_0	BF32	MEM_B_A<0>	
SB_MA_1	BE33	MEM_B_A<1>	
SB_MA_2	BD33	MEM_B_A<2>	
SB_MA_3	AU30	MEM_B_A<3>	
SB_MA_4	BD30	MEM_B_A<4>	
SB_MA_5	AV30	MEM_B_A<5>	
SB_MA_6	BG30	MEM_B_A<6>	
SB_MA_7	BD29	MEM_B_A<7>	
SB_MA_8	BE30	MEM_B_A<8>	
SB_MA_9	BE28	MEM_B_A<9>	
SB_MA_10	BD43	MEM_B_A<10>	
SB_MA_11	AT28	MEM_B_A<11>	
SB_MA_12	AV28	MEM_B_A<12>	
SB_MA_13	BD46	MEM_B_A<13>	
SB_MA_14	AT26	MEM_B_A<14>	
SB_MA_15	AU22	MEM_B_A<15>	

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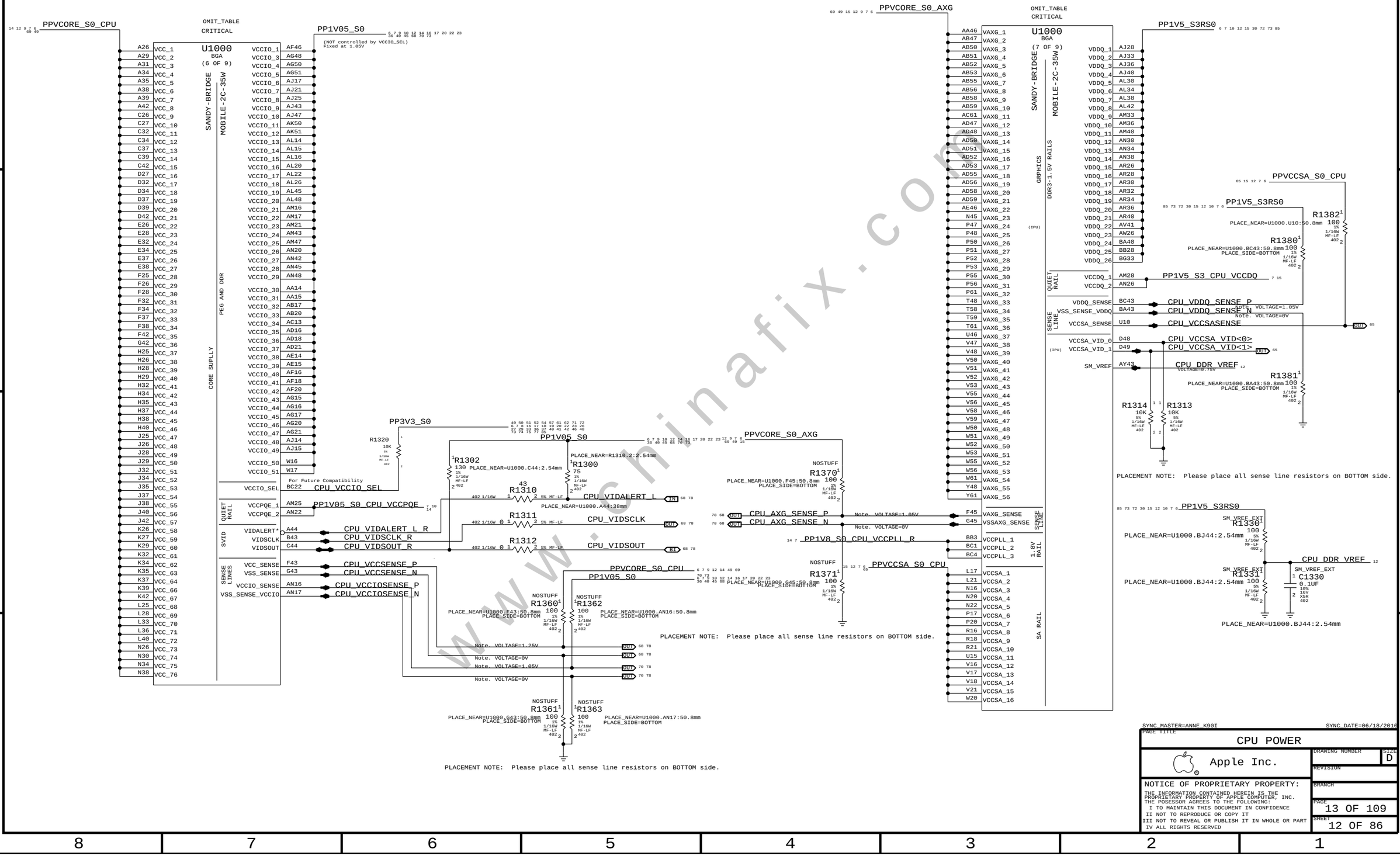

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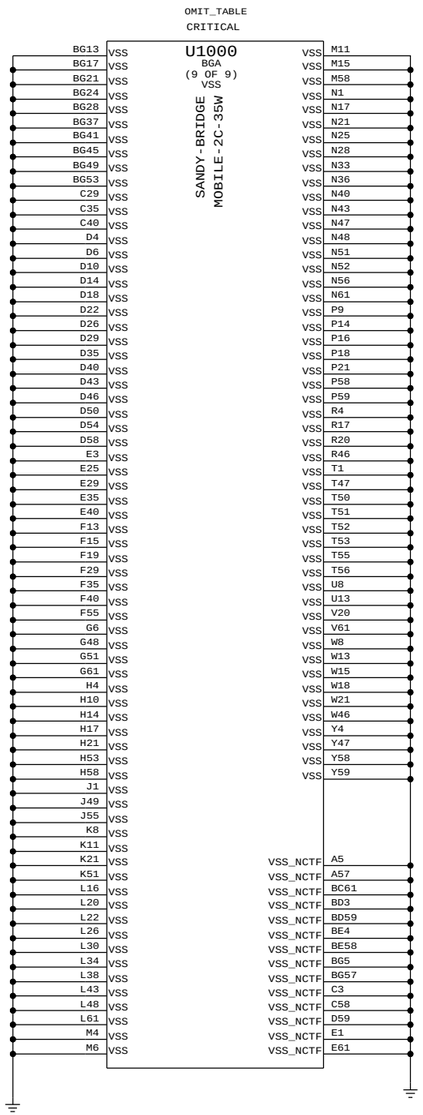

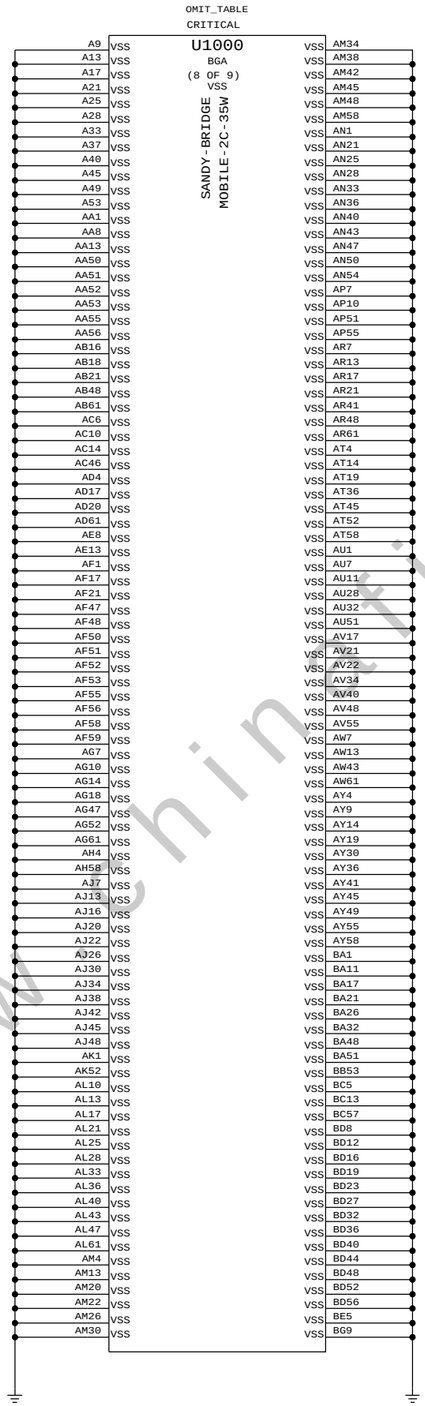

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

69 49 12 9 7 6 PPVCORE_S0_CPU

C1600 C1601 NOSTUFF C1602 NOSTUFF C1603 C1604 NOSTUFF C1605 C1606 C1607 C1608 C1609 C1610 NOSTUFF C1611 C1612 C1613 NOSTUFF C1614 C1615 NOSTUFF C1616 C1617 NOSTUFF C1618 NOSTUFF C1619 NOSTUFF C1620 NOSTUFF C1621 C1622 C1623 C1624
C1625 NOSTUFF C1626 C1627 C1628 NOSTUFF C1629 NOSTUFF C1630 C1631 C1632 NOSTUFF C1633 NOSTUFF C1634 C1635 NOSTUFF C1636 C1637 C1638 C1639 C1640 C1641 C1642 C1643 C1644 C1645 NOSTUFF C1646 C1647 C1648 NOSTUFF C1649
C1650 C1651 C1652 C1653 C1654

2.2UF 20% 4V X5R 402 — CRITICAL

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 C1656 NOSTUFF C1657 NOSTUFF C1658 NOSTUFF C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666
22UF 20% 6.3V X5R-CERM-1 603 — CRITICAL, OMIT_TABLE

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

C1667 C1668 NOSTUFF C1669 C1670 C1671 NOSTUFF C1672 NOSTUFF C1673 C1674 NOSTUFF C1675 C1676 C1677 C1678 C1679
22UF 20% 6.3V X5R-CERM-1 603 — CRITICAL, OMIT_TABLE

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 C1681 C1682 C1683
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1655,C1660,C1661,C1662,C1663,C1664,C1665,C1666,C1667,C1670,C1671,C1674,C1676,C1677,C1678,C1679	CRITICAL	

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

45 40 36 23 12 10 7 6 PP1V05_S0

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696
C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near ~~U1000~~ on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C
10UF 20% 6.3V CERM-X5R 0402-1

C167D 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C167E 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603 — PP1V05_S0_CPU_VCCPQE — 7 10 12

C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

71 26 22 20 17 7 6 PP1VR_S0

R1600 0 5% 1/10W MF-LF 402

PP1VR_S0_CPU_VCCPLL_R — 7 12

C160X C160Y 1UF 10% 10V X5R 402

C160Z 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

PLACE_NEAR=U1000.AK61:5mm
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

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VAXG DECOUPLING

Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

69 49 12 9 7 6 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R 402
CRITICAL C1701 1UF 10% 10V X5R 402
CRITICAL C1702 1UF 10% 10V X5R 402
CRITICAL C1703 1UF 10% 10V X5R 402
CRITICAL C1704 1UF 10% 10V X5R 402
CRITICAL C1705 1UF 10% 10V X5R 402
CRITICAL C1706 1UF 10% 10V X5R 402
CRITICAL C1707 1UF 10% 10V X5R 402
CRITICAL C1708 1UF 10% 10V X5R 402
CRITICAL C1709 1UF 10% 10V X5R 402
CRITICAL C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL OMIT C1717 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1718 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1719 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1720 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1721 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1722 22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1724 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	6	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1717,C1718,C1719,C1720,C1721,C1722	CRITICAL	

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

85 73 72 30 12 10 7 6 PP1V5_S3RS0

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

65 12 7 6 PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=JACK_K90I SYNC_DATE=06/28/2010

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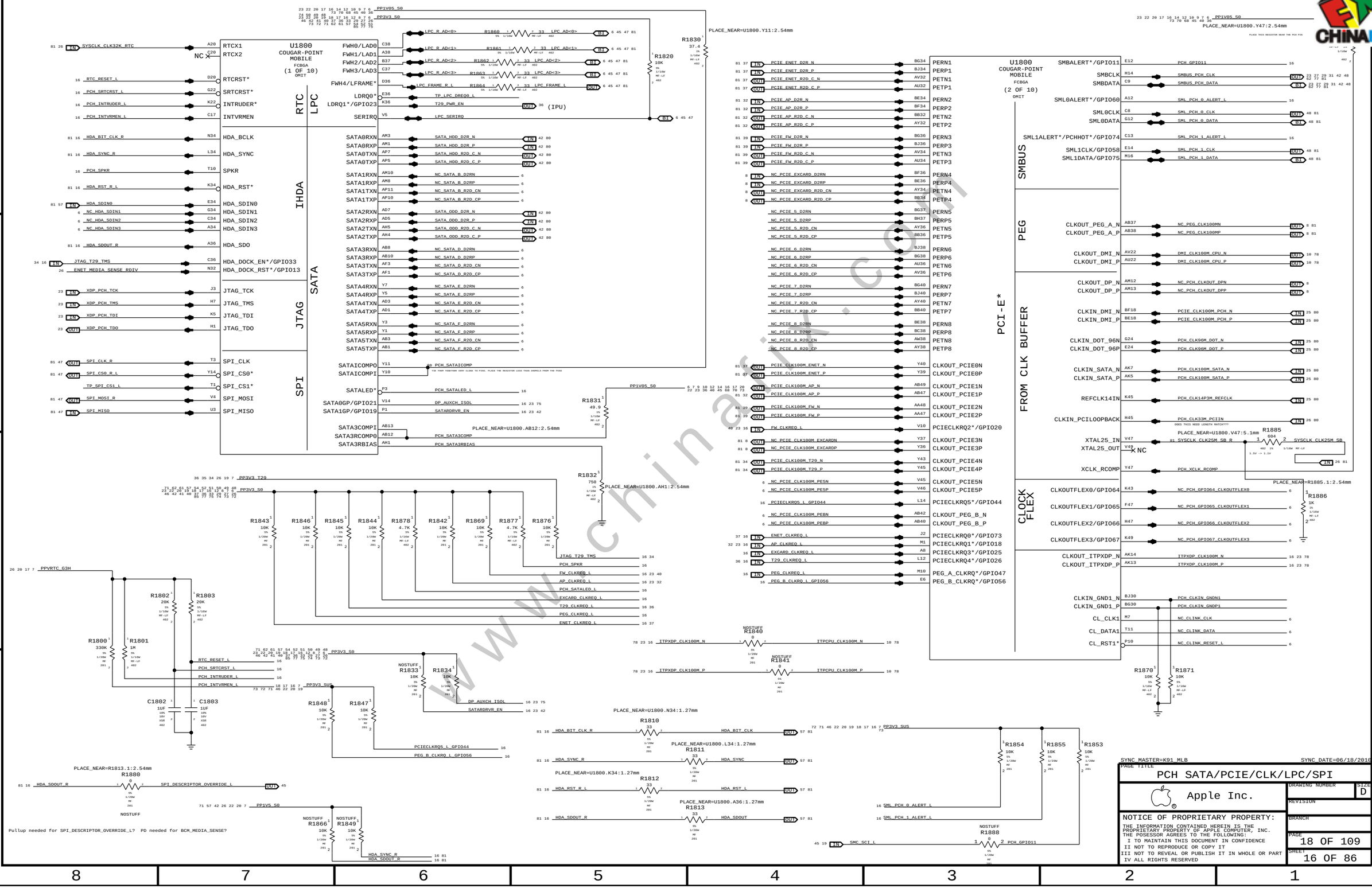
U1800
COUGAR-POINT MOBILE
FCBGA
(1 OF 10)
OMIT
RTC
LPC
IHDA
SATA
JTAG
SPI
SYSCLK_CLK32K_RTC
RTCX1
RTCX2
RTC_RESET_L
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
HDA_BIT_CLK_R
HDA_SYNC_R
SPKR
HDA_RST_R_L
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT_R
JTAG_T29_TMS
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
SPI_CLK_R
SPI_CS0_R_L
TP_SPI_CS1_L
SPI_MOSI_R
SPI_MISO
LPC_R_AD<0>
LPC_R_AD<1>
LPC_R_AD<2>
LPC_R_AD<3>
LPC_FRAME_R_L
LPC_FRAME_L
TP_LPC_DREQ0_L
T29_PWR_EN
LPC_SERIRQ
SATA_HDD_D2R_N
SATA_HDD_D2R_P
SATA_HDD_R2D_C_N
SATA_HDD_R2D_C_P
SATA_ODD_D2R_N
SATA_ODD_D2R_P
SATA_ODD_R2D_C_N
SATA_ODD_R2D_C_P
PCH_SATAICOMP
PCH_SATALED_L
DP_AUXCH_ISOL
SATARDRVR_EN
PCH_SATA3COMP
PCH_SATA3RBIAS
PLACE_NEAR=U1800.AB12:2.54mm
PLACE_NEAR=U1800.Y11:2.54mm
PLACE_NEAR=U1800.AH1:2.54mm
PP1V05_S0
PP3V3_S0
R1830 37.4
R1820 10K
R1831 49.9
R1832 750
R1843 10K
R1846 10K
R1845 10K
R1844 10K
R1878 4.7K
R1842 10K
R1869 10K
R1877 4.7K
R1876 10K
JTAG_T29_TMS
PCH_SPKR
FW_CLKREQ_L
AP_CLKREQ_L
PCH_SATALED_L
EXCARD_CLKREQ_L
T29_CLKREQ_L
PEG_CLKREQ_L
ENET_CLKREQ_L
(IPU)
PPVRTC_G3H
R1802 20K
R1803 20K
R1800 330K
R1801 1M
C1802 1UF
C1803 1UF
PP3V3_SUS
R1848 10K
R1847 10K
R1833 10K
R1834 10K
NOSTUFF
PCIECLKRQ5_L_GPIO44
PEG_B_CLKRQ_L_GPIO56
PLACE_NEAR=R1813.1:2.54mm
R1880 0
NOSTUFF
Pullup needed for SPI_DESCRIPTOR_OVERRIDE_L? PD needed for BCM_MEDIA_SENSE?
PP1V5_S0
R1866 10K
R1849 10K
HDA_SYNC_R
HDA_SDOUT_R
PLACE_NEAR=U1800.N34:1.27mm
R1810 33
R1811 33
R1812 33
R1813 33
PLACE_NEAR=U1800.L34:1.27mm
PLACE_NEAR=U1800.K34:1.27mm
PLACE_NEAR=U1800.A36:1.27mm
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
R1840 0
R1841 0
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
ITPCPU_CLK100M_N
ITPCPU_CLK100M_P
PCI-E*
PERN1
PERP1
PETN1
PETP1
PERN2
PERP2
PETN2
PETP2
PERN3
PERP3
PETN3
PETP3
PERN4
PERP4
PETN4
PETP4
PERN5
PERP5
PETN5
PETP5
PERN6
PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
PCIECLKRQ2*/GPIO20
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
PCIECLKRQ5*/GPIO44
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PCIECLKRQ0*/GPIO73
PCIECLKRQ1*/GPIO18
PCIECLKRQ3*/GPIO25
PCIECLKRQ4*/GPIO26
PEG_A_CLKRQ*/GPIO47
PEG_B_CLKRQ*/GPIO56
SMBUS
SMBALERT*/GPIO11
SMBCLK
SMBDATA
SML0ALERT*/GPIO60
SML0CLK
SML0DATA
SML1ALERT*/PCHHOT*/GPIO74
SML1CLK/GPIO58
SML1DATA/GPIO75
PEG
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
FROM CLK BUFFER
CLKOUT_DP_N
CLKOUT_DP_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_PCILOOPBACK
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
CLOCK FLEX
CLKOUTFLEX0/GPIO64
CLKOUTFLEX1/GPIO65
CLKOUTFLEX2/GPIO66
CLKOUTFLEX3/GPIO67
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKIN_GND1_N
CLKIN_GND1_P
CL_CLK1
CL_DATA1
CL_RST1*
PLACE_NEAR=U1800.Y47:2.54mm
PLACE_NEAR=U1800.Y47:5.1mm
R1885 604
PLACE_NEAR=R1885.1:2.54mm
R1886 1K
R1870 10K
R1871 10K
R1854 10K
R1855 10K
R1853 10K
R1888 0
NOSTUFF
SYSCLK_CLK25M_SB
SYSCLK_CLK25M_SB_R
PCH_XCLK_RCOMP
SML_PCH_0_ALERT_L
SML_PCH_0_CLK
SML_PCH_0_DATA
SML_PCH_1_ALERT_L
SML_PCH_1_CLK
SML_PCH_1_DATA
NC_PEG_CLK100MN
NC_PEG_CLK100MP
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
NC_PCH_CLKOUT_DPN
NC_PCH_CLKOUT_DPP
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
NC_PCH_GPIO64_CLKOUTFLEX0
NC_PCH_GPIO65_CLKOUTFLEX1
NC_PCH_GPIO66_CLKOUTFLEX2
NC_PCH_GPIO67_CLKOUTFLEX3
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
PCH_CLKIN_GNDN1
PCH_CLKIN_GNDP1
NC_CLINK_CLK
NC_CLINK_DATA
NC_CLINK_RESET_L
SMC_SCI_L
PCH_GPIO11
SYNC_MASTER=K91_MLB
SYNC_DATE=06/18/2010
PAGE TITLE
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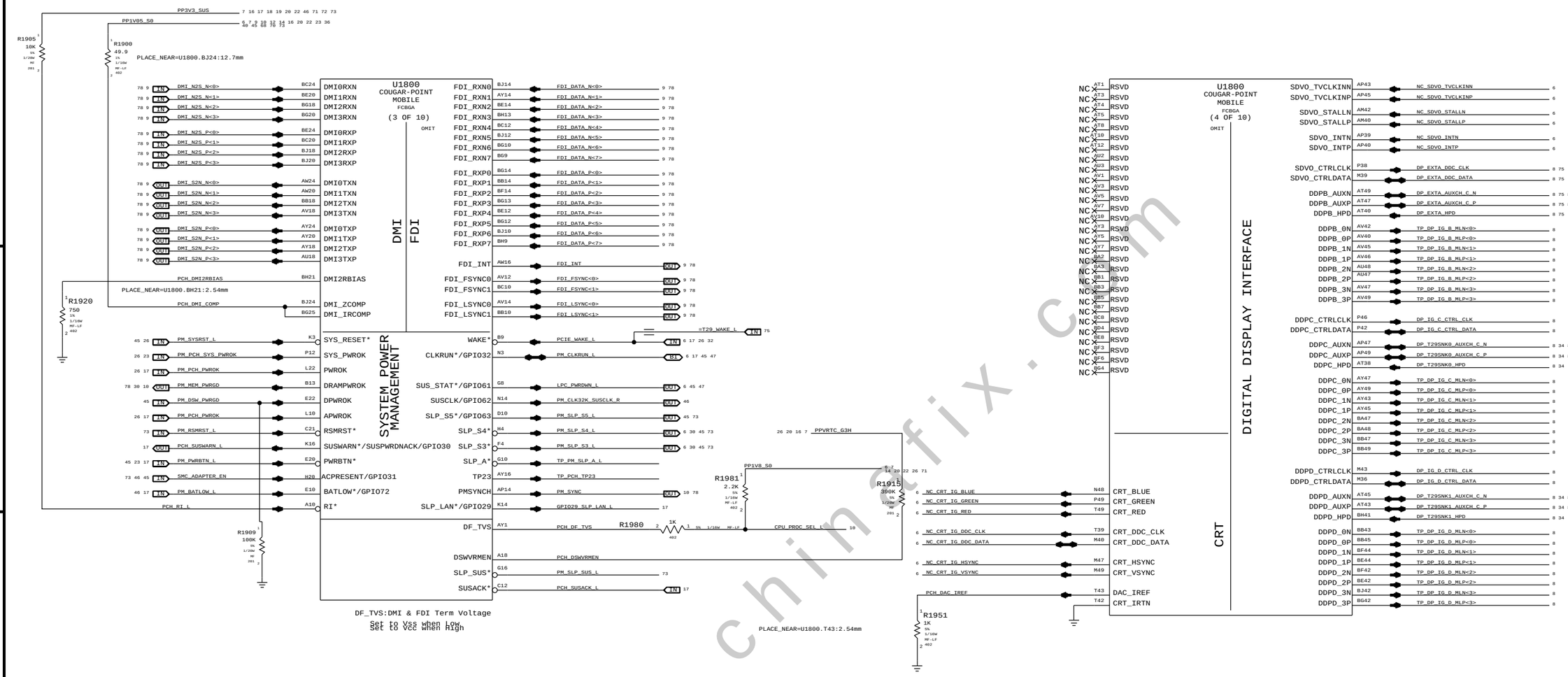

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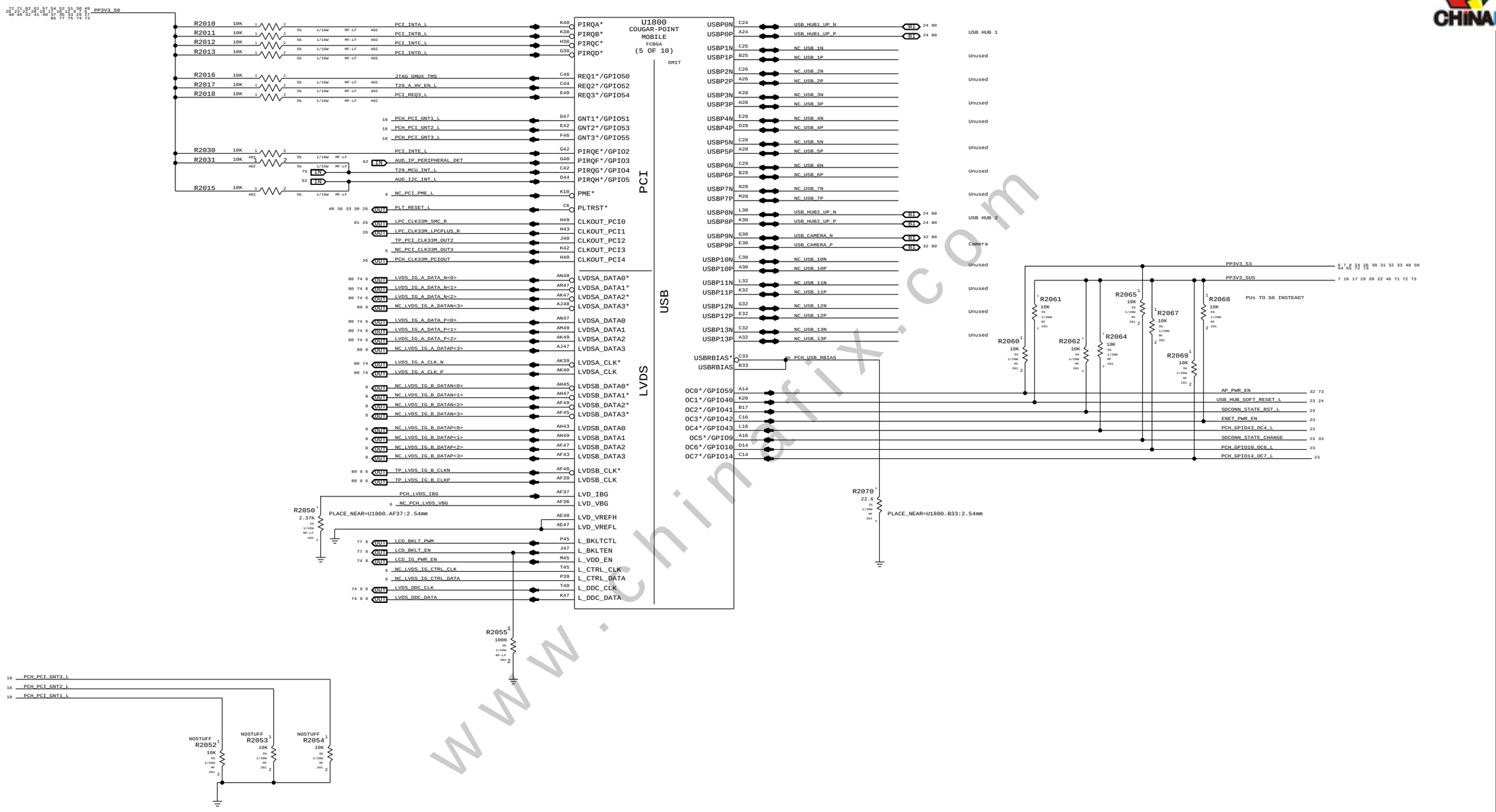

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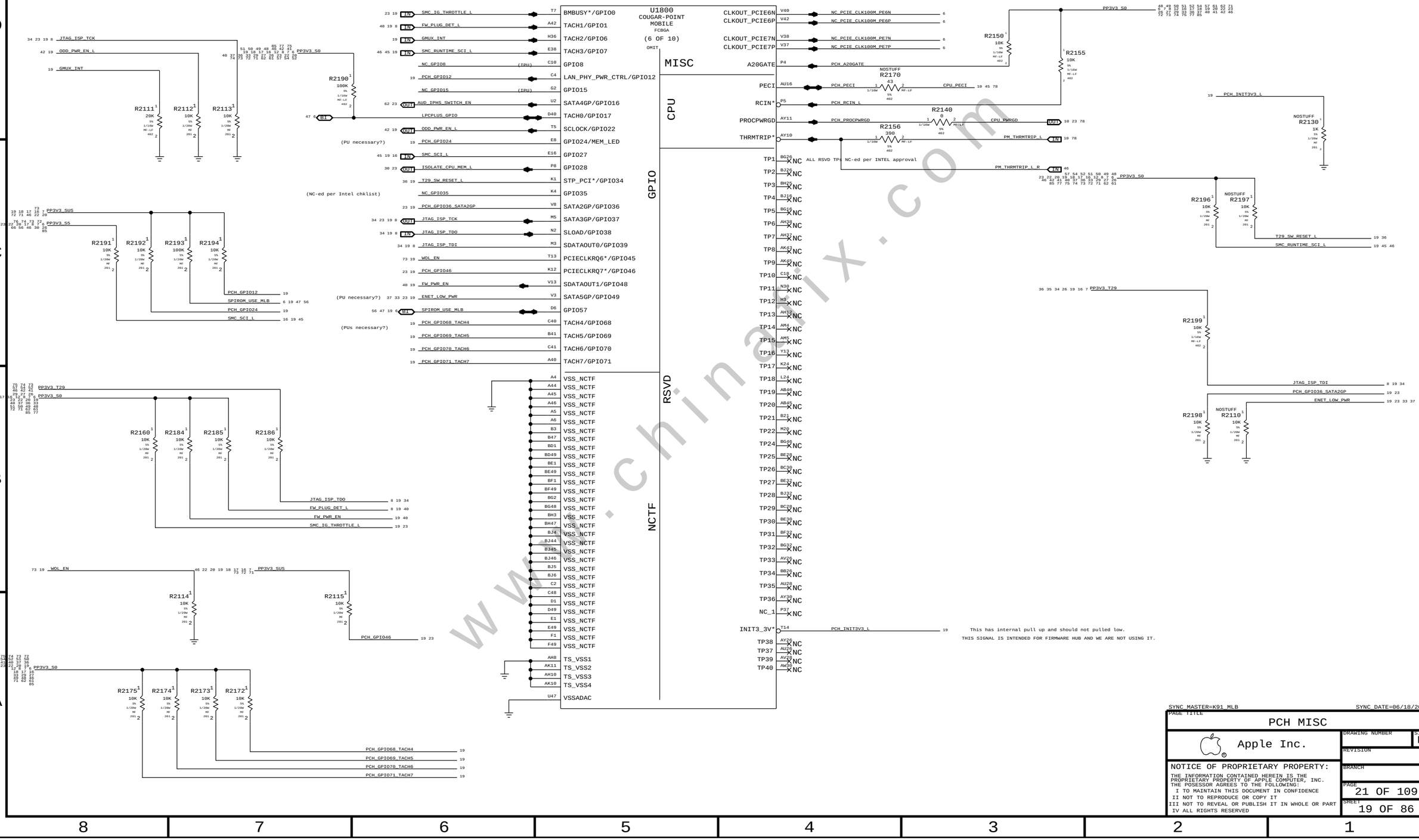

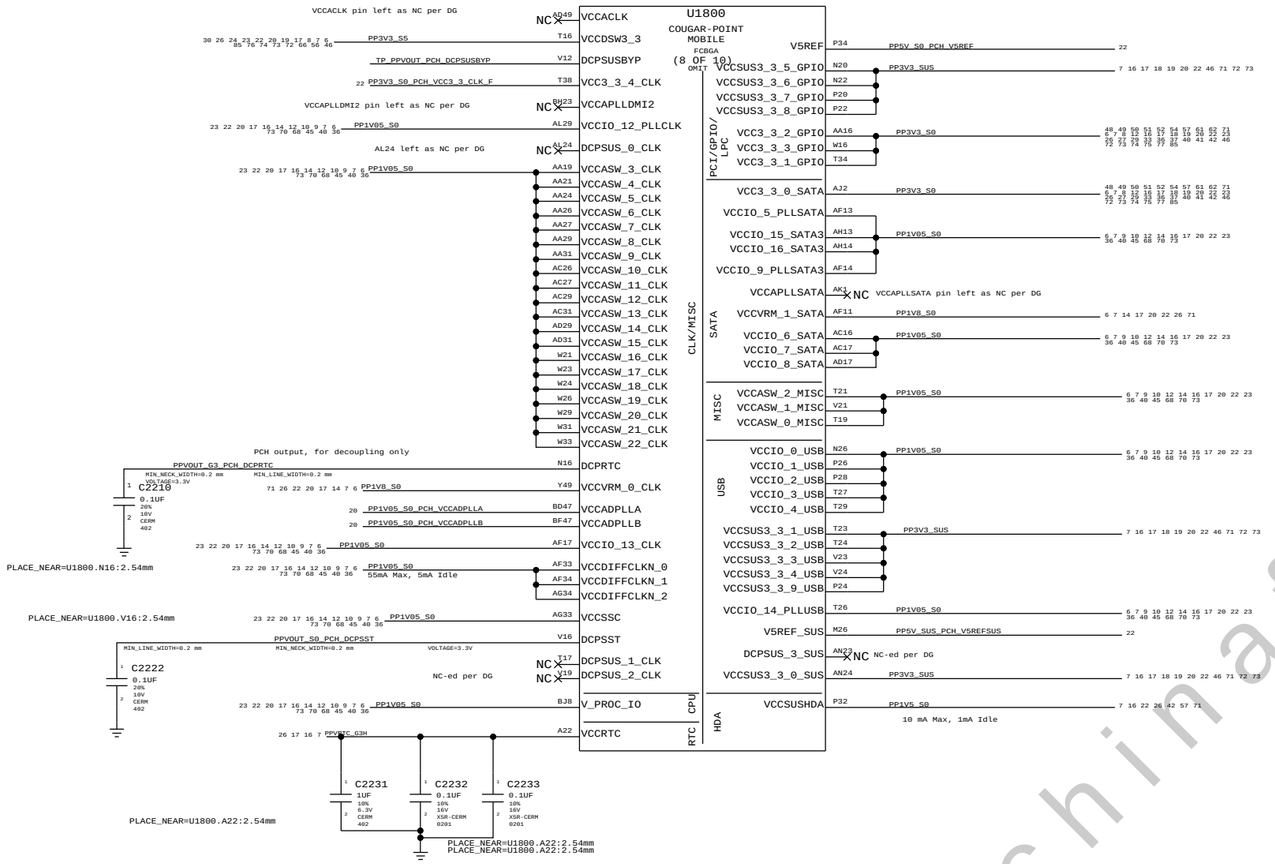

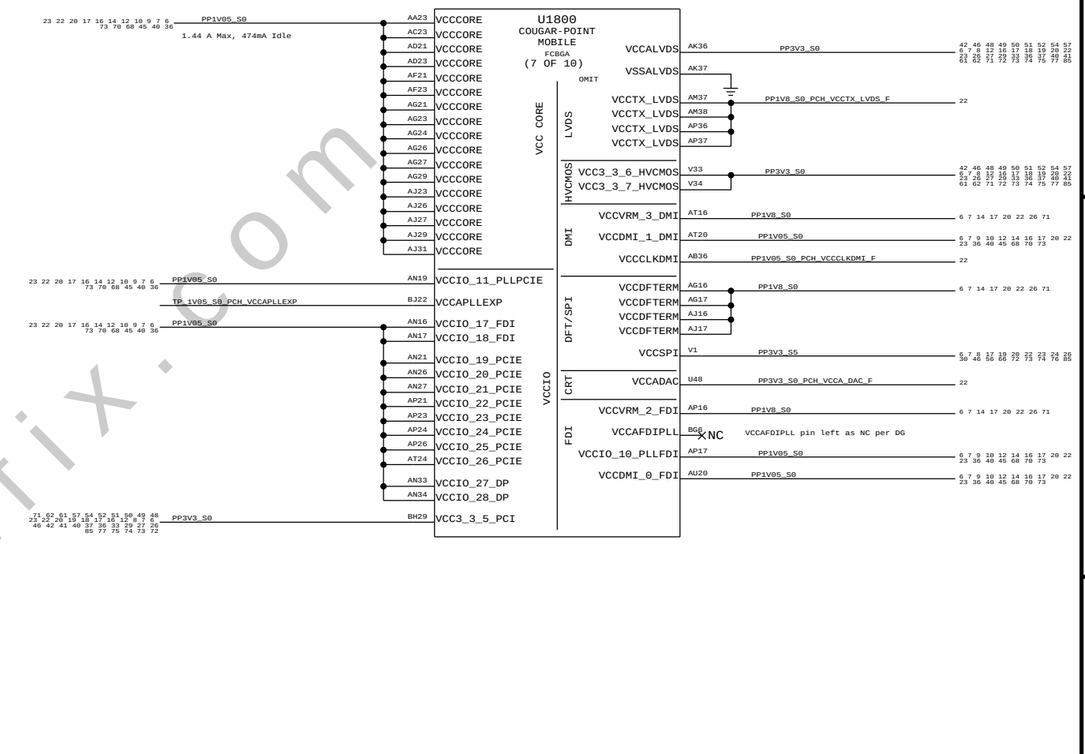

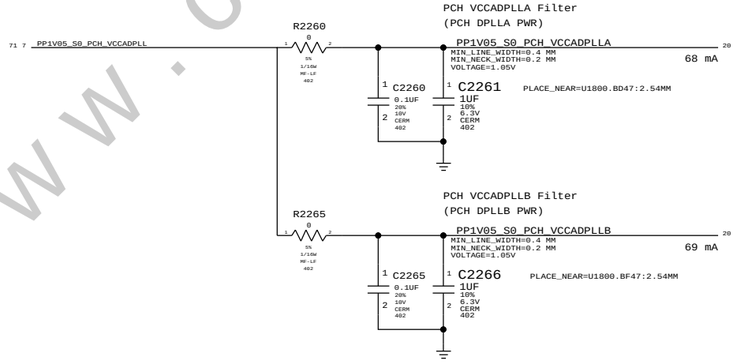

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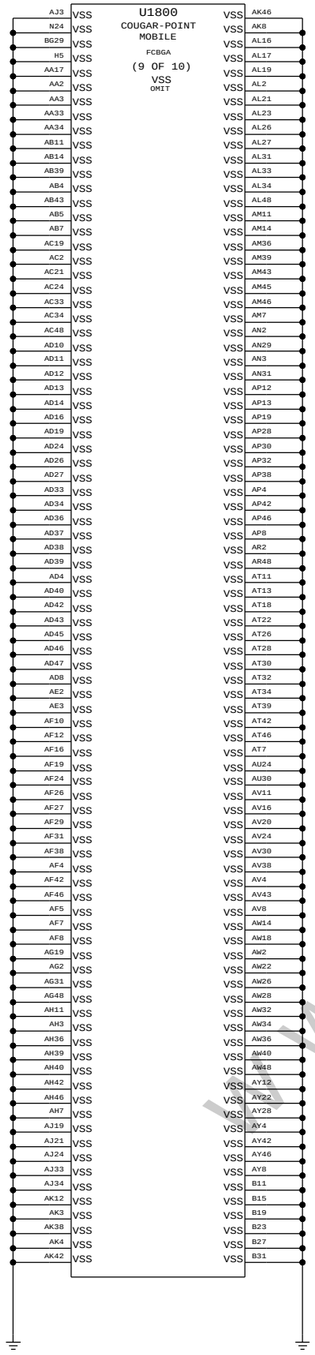

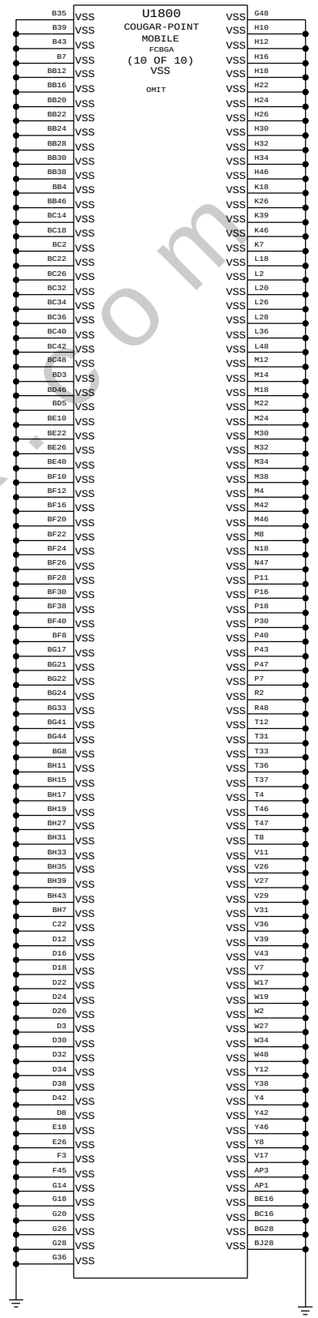

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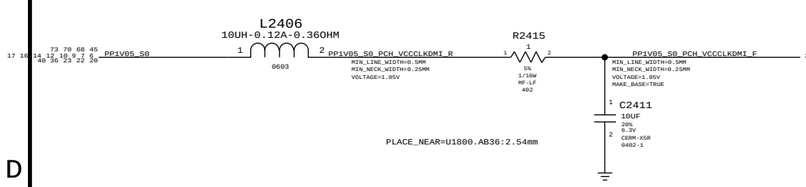

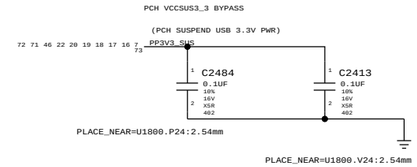

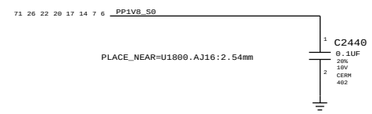

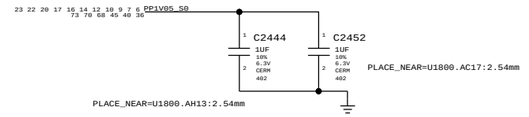

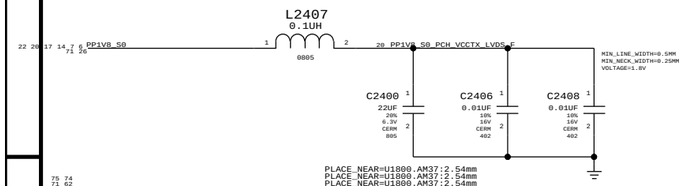

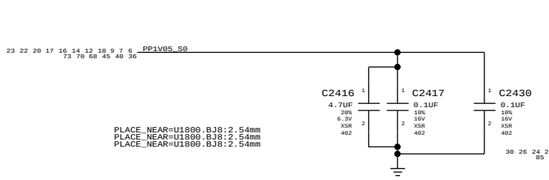

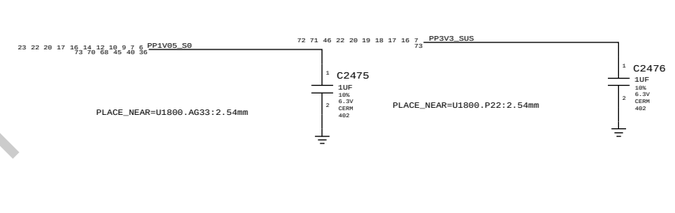

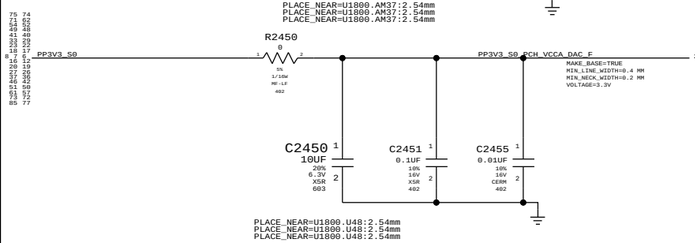

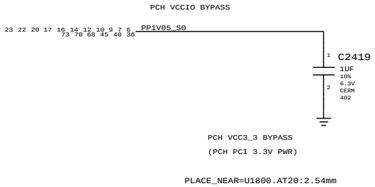

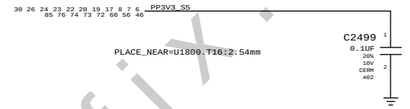

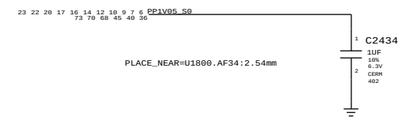

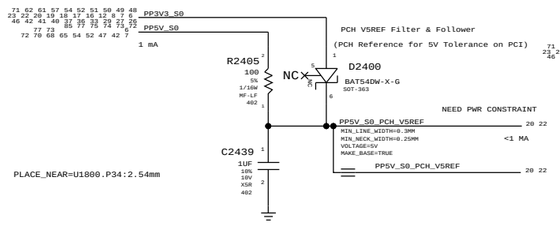

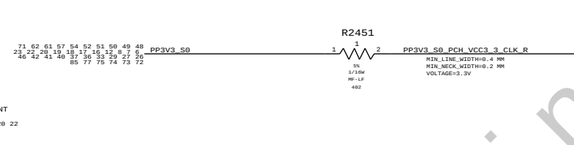

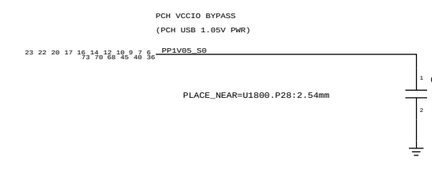

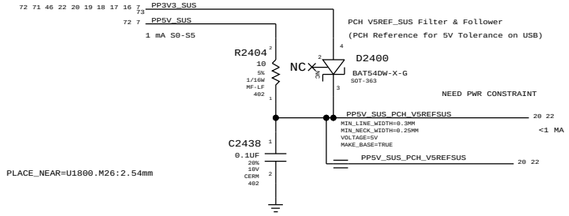

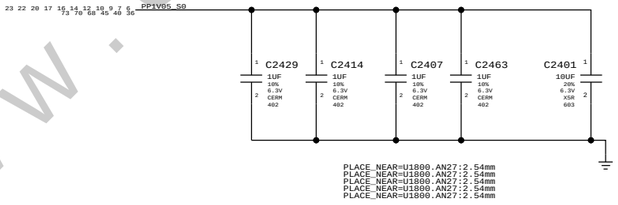

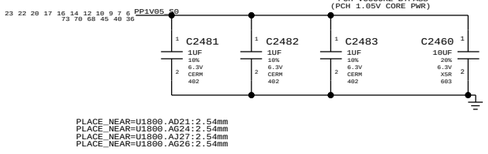

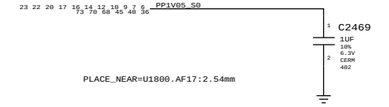

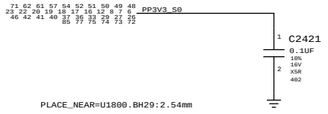

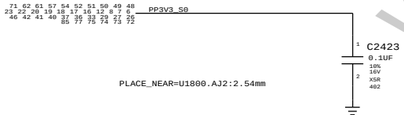

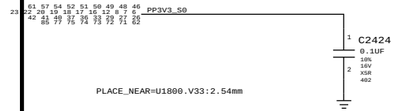

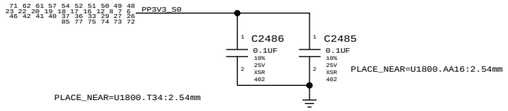

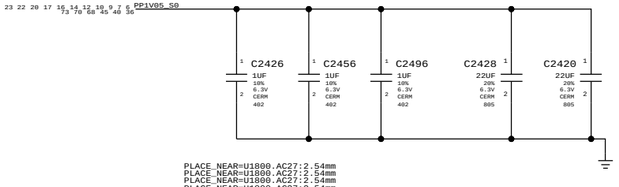

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PAGE TITLE

PCH DECOUPLING

Apple Inc.

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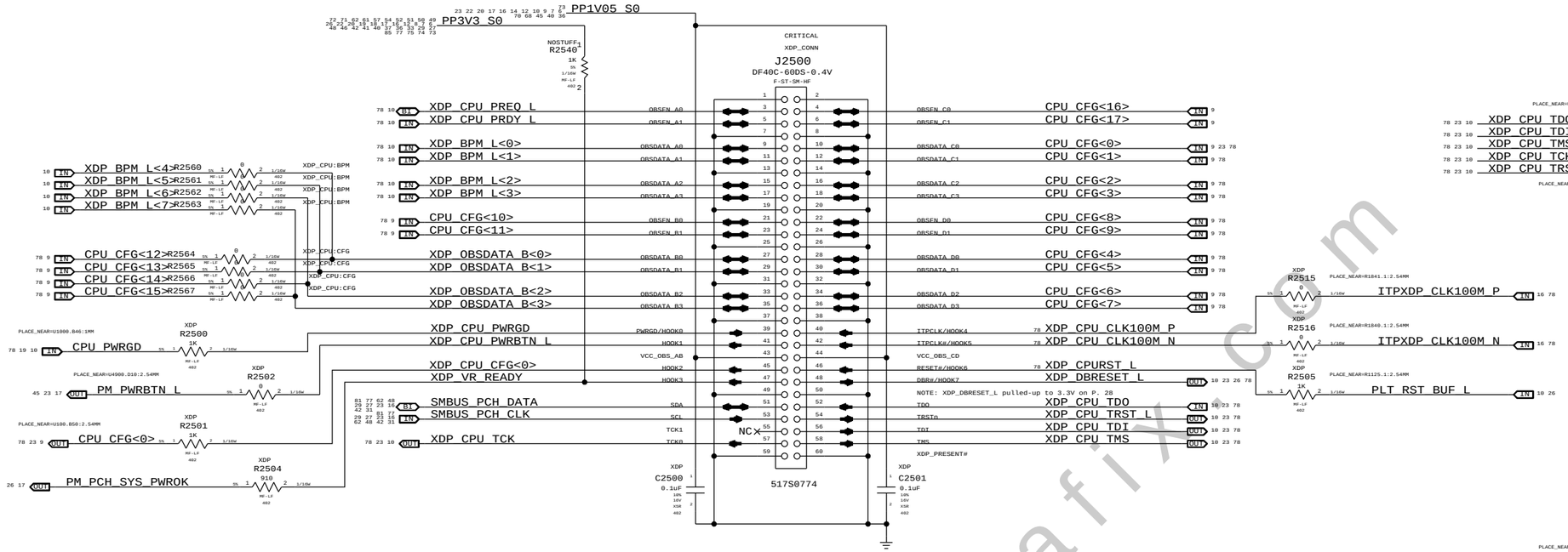
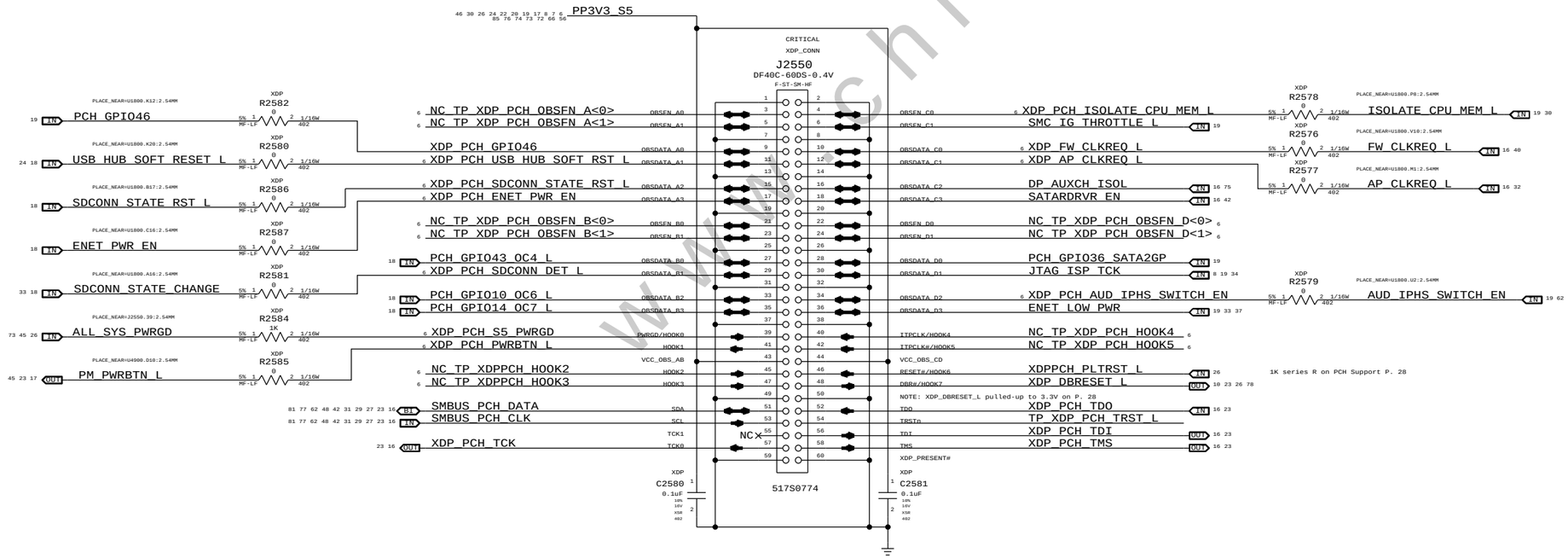
PROCESSOR MINI XDP



PCH MINI XDP



SYNC_MASTER=ANNE_K90I SYNC_DATE=06/22/2010

PAGE TITLE	CPU & PCH XDP
Apple Inc.	DRAWING NUMBER: — SIZE: D
	REVISION: —
	BRANCH: —
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BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC_MASTER=K91_MLB SYNC_DATE=06/08/2010

PAGE TITLE: USB HUBS

Apple Inc.

DRAWING NUMBER | SIZE: D

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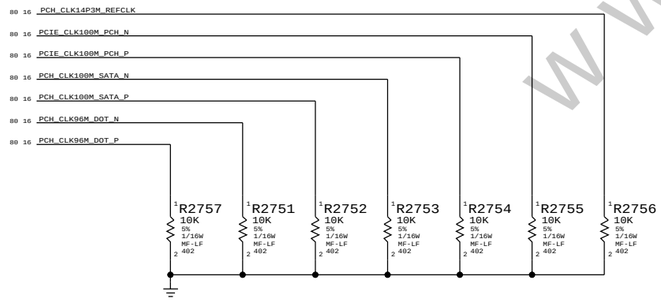
UNUSED clock terminations for FCIM MODE



SYNC_MASTER=K91_MLB SYNC_DATE=06/21/2010

PAGE TITLE

Clock (CK505)

Apple Inc.

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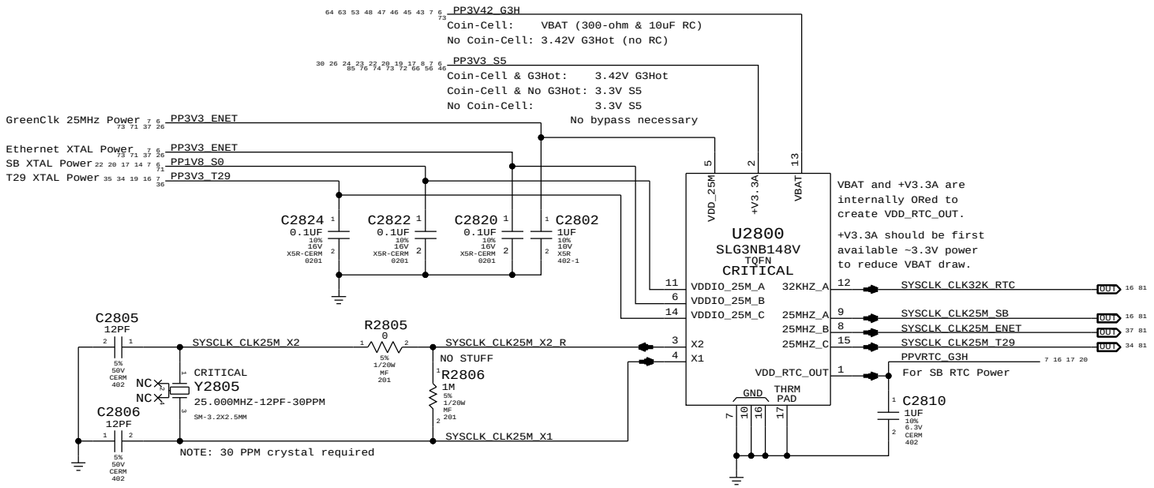
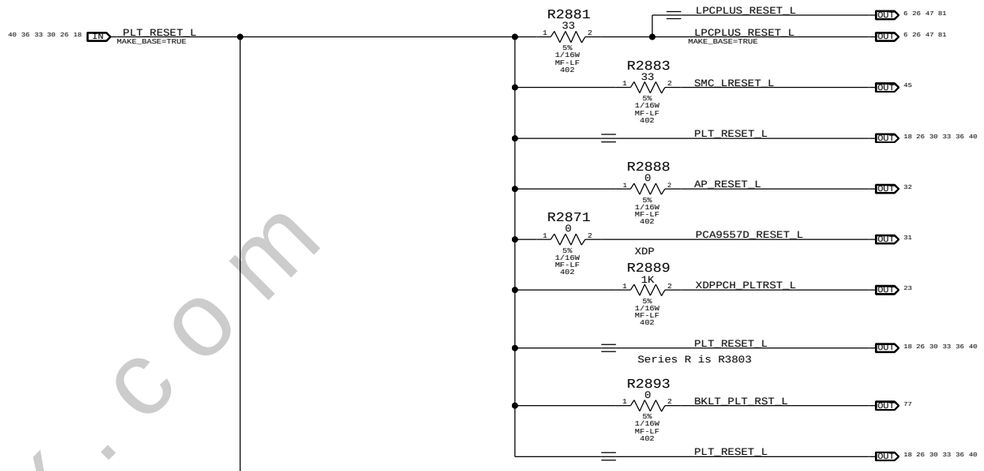
System RTC Power Source & 32kHz / 25MHz Clock Generator

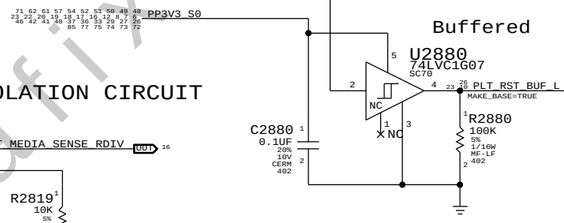


Platform Reset Connections

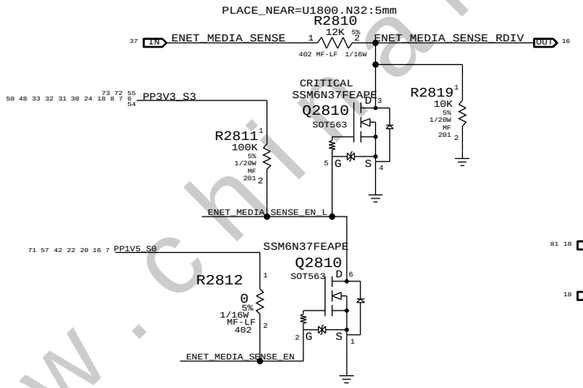
Unbuffered



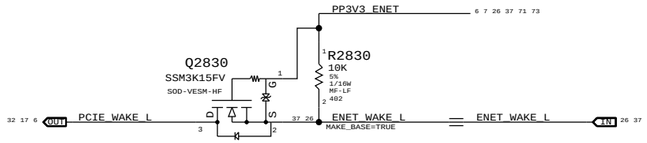
Buffered

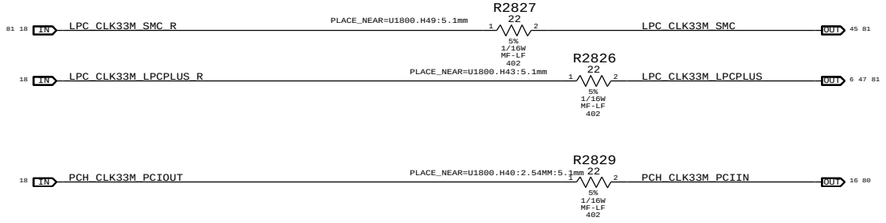


ENET_MEDIA_SENSE ISOLATION CIRCUIT

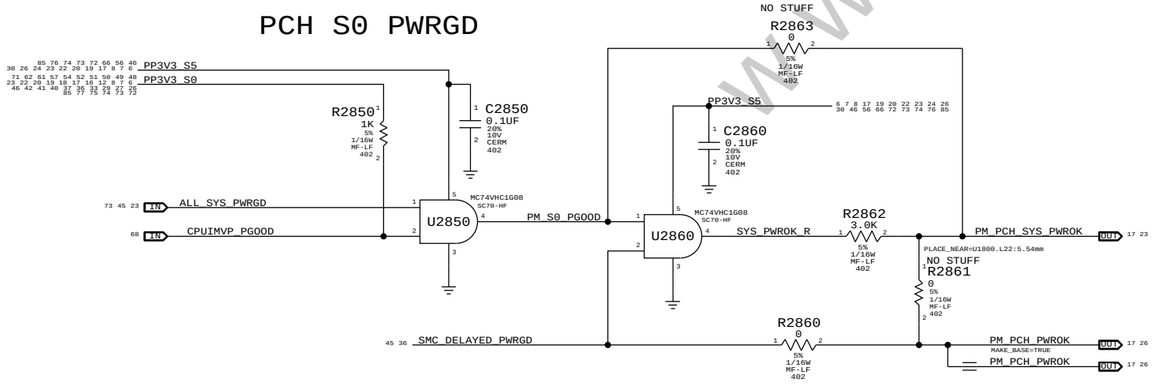


Ethernet WAKE# Isolation

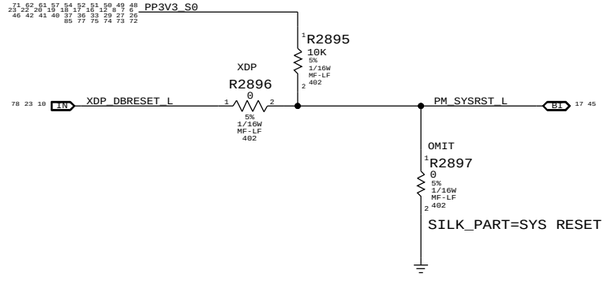




PCH S0 PWRGD



PCH Reset Button



SYNC_MASTER=LINDA_K90I	SYNC_DATE=07/08/2010
PAGE TITLE	Chipset Support
Apple Inc.	DRAWING NUMBER / SIZE D
	REVISION
	BRANCH
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Page Notes

Power aliases required by this page:

- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:

- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:

(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

PP1V5_S3

C2900 10UF 20% 6.3V X5R 603

C2901 10UF 20% 6.3V X5R 603

C2910 C2911 C2912 C2913 C2914 C2915 C2916 C2917 C2918 C2919 C2920 C2921 C2922 C2923 0.1UF 20% 10V CERM 402

PP0V75_S3_MEM_VREFDQ_A

C2930 2.2UF 20% 6.3V CERM 402-LF

C2931 0.1UF 20% 10V CERM 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 2 OF 2) F-RT-THB

KEY

73	CKE0	CKE1	74		MEM_A_CKE<1>
75	VDD	VDD	76		
77	NC	A15	78		MEM_A_A<15>
79	BA2	A14	80		MEM_A_A<14>
81	VDD	VDD	82		
83	A12/BC*	A11	84		MEM_A_A<11>
85	A9	A7	86		MEM_A_A<7>
87	VDD	VDD	88		
89	A8	A6	90		MEM_A_A<6>
91	A5	A4	92		MEM_A_A<4>
93	VDD	VDD	94		
95	A3	A2	96		MEM_A_A<2>
97	A1	A0	98		MEM_A_A<0>
99	VDD	VDD	100		
101	CK0	CK1	102		MEM_A_CLK_P<1>
103	CK0*	CK1*	104		MEM_A_CLK_N<1>
105	VDD	VDD	106		
107	A10/AP	BA1	108		MEM_A_BA<1>
109	BA0	RAS*	110		MEM_A_RAS_L
111	VDD	VDD	112		
113	WE*	S0*	114		MEM_A_CS_L<0>
115	CAS*	ODT0	116		MEM_A_ODT<0>
117	VDD	VDD	118		
119	A13	ODT1	120		MEM_A_ODT<1>
121	S1*	NC	122	NC	
123	VDD	VDD	124		
125	TEST	VREFCA	126		
127	VSS	VSS	128		
129	DQ32	DQ36	130		MEM_A_DQ<36>
131	DQ33	DQ37	132		MEM_A_DQ<37>
133	VSS	VSS	134		
135	DQS4*	DM4	136		GND
137	DQS4	VSS	138		
139	VSS	DQ38	140		MEM_A_DQ<38>
141	DQ34	DQ39	142		MEM_A_DQ<39>
143	DQ35	VSS	144		
145	VSS	DQ44	146		MEM_A_DQ<44>
147	DQ40	DQ45	148		MEM_A_DQ<45>
149	DQ41	VSS	150		
151	VSS	DQS5*	152		MEM_A_DQS_N<5>
153	DM5	DQS5	154		MEM_A_DQS_P<5>
155	VSS	VSS	156		
157	DQ42	DQ46	158		MEM_A_DQ<46>
159	DQ43	DQ47	160		MEM_A_DQ<47>
161	VSS	VSS	162		
163	DQ48	DQ52	164		MEM_A_DQ<52>
165	DQ49	DQ53	166		MEM_A_DQ<53>
167	VSS	VSS	168		
169	DQS6*	DM6	170		GND
171	DQS6	VSS	172		
173	VSS	DQ54	174		MEM_A_DQ<54>
175	DQ50	DQ55	176		MEM_A_DQ<55>
177	DQ51	VSS	178		
179	VSS	DQ60	180		MEM_A_DQ<60>
181	DQ56	DQ61	182		MEM_A_DQ<61>
183	DQ57	VSS	184		
185	VSS	DQS7*	186		MEM_A_DQS_N<7>
187	DM7	DQS7	188		MEM_A_DQS_P<7>
189	VSS	VSS	190		
191	DQ58	DQ62	192		MEM_A_DQ<62>
193	DQ59	DQ63	194		MEM_A_DQ<63>
195	VSS	VSS	196		
197	SA0	EVENT*	198		MEM_EVENT_L
199	VDDSPD	SDA	200		SMBUS_PCH_DATA
201	SA1	SCL	202		SMBUS_PCH_CLK
203	VTT	VTT	204		PP0V75_S0_DDRVTT

NC

516-0229

SPD ADDR=0xA0(WR)/0xA1(RD)

PP3V3_S0

MEM_A_SA<0>

MEM_A_SA<1>

C2940 2.2UF 20% 6.3V CERM 402-LF

R2940 10K 5% 1/16W MF-LF 402

R2941 10K 5% 1/16W MF-LF 402

J2900 DDR3-SODIMM-DUAL-K6 (SYMBOL 1 OF 2) CRITICAL F-RT-THB

KEY

1	VREFDQ	VSS	2		
3	VSS	DQ4	4		MEM_A_DQ<4>
5	DQ0	DQ5	6		MEM_A_DQ<5>
7	DQ1	VSS	8		
9	VSS	DQS0*	10		MEM_A_DQS_N<0>
11	DM0	DQS0	12		MEM_A_DQS_P<0>
13	VSS	VSS	14		
15	DQ2	DQ6	16		MEM_A_DQ<6>
17	DQ3	DQ7	18		MEM_A_DQ<7>
19	VSS	VSS	20		
21	DQ8	DQ12	22		MEM_A_DQ<12>
23	DQ9	DQ13	24		MEM_A_DQ<13>
25	VSS	VSS	26		
27	DQS1*	DM1	28		GND
29	DQS1	RESET*	30		MEM_RESET_L
31	VSS	VSS	32		
33	DQ10	DQ14	34		MEM_A_DQ<14>
35	DQ11	DQ15	36		MEM_A_DQ<15>
37	VSS	VSS	38		
39	DQ16	DQ20	40		MEM_A_DQ<20>
41	DQ17	DQ21	42		MEM_A_DQ<21>
43	VSS	VSS	44		
45	DQS2*	DM2	46		GND
47	DQS2	VSS	48		
49	VSS	DQ22	50		MEM_A_DQ<22>
51	DQ18	DQ23	52		MEM_A_DQ<23>
53	DQ19	VSS	54		
55	VSS	DQ28	56		MEM_A_DQ<28>
57	DQ24	DQ29	58		MEM_A_DQ<29>
59	DQ25	VSS	60		
61	VSS	DQS3*	62		MEM_A_DQS_N<3>
63	DM3	DQS3	64		MEM_A_DQS_P<3>
65	VSS	VSS	66		
67	DQ26	DQ30	68		MEM_A_DQ<30>
69	DQ27	DQ31	70		MEM_A_DQ<31>
71	VSS	VSS	72		

GND

516-0229

PP0V75_S3_MEM_VREFCA_A

C2935 2.2UF 20% 6.3V CERM 402-LF

C2936 0.1UF 20% 10V CERM 402

C2950 C2951 C2952 C2953 1UF 10% 10V X5R 402

"Factory" (top) slot

SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE	DDR3 SO-DIMM Connector A
Apple Inc.	DRAWING NUMBER: D
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	BRANCH:
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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_N<0>
MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_A_DQS_P<0>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<7>	MAKE_BASE=TRUE	=	=MEM_A_DQ<3>
MEM_A_DQ<6>	MAKE_BASE=TRUE	=	=MEM_A_DQ<6>
MEM_A_DQ<5>	MAKE_BASE=TRUE	=	=MEM_A_DQ<1>
MEM_A_DQ<4>	MAKE_BASE=TRUE	=	=MEM_A_DQ<5>
MEM_A_DQ<3>	MAKE_BASE=TRUE	=	=MEM_A_DQ<2>
MEM_A_DQ<2>	MAKE_BASE=TRUE	=	=MEM_A_DQ<7>
MEM_A_DQ<1>	MAKE_BASE=TRUE	=	=MEM_A_DQ<0>
MEM_A_DQ<0>	MAKE_BASE=TRUE	=	=MEM_A_DQ<4>
	MAKE_BASE=TRUE	=	

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<1>
MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<1>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<15>	MAKE_BASE=TRUE	=	=MEM_A_DQ<11>
MEM_A_DQ<14>	MAKE_BASE=TRUE	=	=MEM_A_DQ<10>
MEM_A_DQ<13>	MAKE_BASE=TRUE	=	=MEM_A_DQ<12>
MEM_A_DQ<12>	MAKE_BASE=TRUE	=	=MEM_A_DQ<9>
MEM_A_DQ<11>	MAKE_BASE=TRUE	=	=MEM_A_DQ<15>
MEM_A_DQ<10>	MAKE_BASE=TRUE	=	=MEM_A_DQ<14>
MEM_A_DQ<9>	MAKE_BASE=TRUE	=	=MEM_A_DQ<13>
MEM_A_DQ<8>	MAKE_BASE=TRUE	=	=MEM_A_DQ<8>
	MAKE_BASE=TRUE	=	

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<2>
MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<2>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<23>	MAKE_BASE=TRUE	=	=MEM_A_DQ<23>
MEM_A_DQ<22>	MAKE_BASE=TRUE	=	=MEM_A_DQ<22>
MEM_A_DQ<21>	MAKE_BASE=TRUE	=	=MEM_A_DQ<21>
MEM_A_DQ<20>	MAKE_BASE=TRUE	=	=MEM_A_DQ<20>
MEM_A_DQ<19>	MAKE_BASE=TRUE	=	=MEM_A_DQ<18>
MEM_A_DQ<18>	MAKE_BASE=TRUE	=	=MEM_A_DQ<19>
MEM_A_DQ<17>	MAKE_BASE=TRUE	=	=MEM_A_DQ<16>
MEM_A_DQ<16>	MAKE_BASE=TRUE	=	=MEM_A_DQ<17>
	MAKE_BASE=TRUE	=	

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<3>
MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<3>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<31>	MAKE_BASE=TRUE	=	=MEM_A_DQ<26>
MEM_A_DQ<30>	MAKE_BASE=TRUE	=	=MEM_A_DQ<24>
MEM_A_DQ<29>	MAKE_BASE=TRUE	=	=MEM_A_DQ<28>
MEM_A_DQ<28>	MAKE_BASE=TRUE	=	=MEM_A_DQ<25>
MEM_A_DQ<27>	MAKE_BASE=TRUE	=	=MEM_A_DQ<31>
MEM_A_DQ<26>	MAKE_BASE=TRUE	=	=MEM_A_DQ<27>
MEM_A_DQ<25>	MAKE_BASE=TRUE	=	=MEM_A_DQ<30>
MEM_A_DQ<24>	MAKE_BASE=TRUE	=	=MEM_A_DQ<29>
	MAKE_BASE=TRUE	=	

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<4>
MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<4>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<39>	MAKE_BASE=TRUE	=	=MEM_A_DQ<38>
MEM_A_DQ<38>	MAKE_BASE=TRUE	=	=MEM_A_DQ<39>
MEM_A_DQ<37>	MAKE_BASE=TRUE	=	MEM_A_DQ<37>
MEM_A_DQ<36>	MAKE_BASE=TRUE	=	=MEM_A_DQ<33>
MEM_A_DQ<35>	MAKE_BASE=TRUE	=	=MEM_A_DQ<34>
MEM_A_DQ<34>	MAKE_BASE=TRUE	=	=MEM_A_DQ<35>
MEM_A_DQ<33>	MAKE_BASE=TRUE	=	=MEM_A_DQ<32>
MEM_A_DQ<32>	MAKE_BASE=TRUE	=	=MEM_A_DQ<36>
	MAKE_BASE=TRUE	=	

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<5>
MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<5>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<47>	MAKE_BASE=TRUE	=	=MEM_A_DQ<46>
MEM_A_DQ<46>	MAKE_BASE=TRUE	=	=MEM_A_DQ<43>
MEM_A_DQ<45>	MAKE_BASE=TRUE	=	=MEM_A_DQ<45>
MEM_A_DQ<44>	MAKE_BASE=TRUE	=	=MEM_A_DQ<41>
MEM_A_DQ<43>	MAKE_BASE=TRUE	=	=MEM_A_DQ<47>
MEM_A_DQ<42>	MAKE_BASE=TRUE	=	=MEM_A_DQ<42>
MEM_A_DQ<41>	MAKE_BASE=TRUE	=	=MEM_A_DQ<40>
MEM_A_DQ<40>	MAKE_BASE=TRUE	=	=MEM_A_DQ<44>
	MAKE_BASE=TRUE	=	

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<6>
MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<6>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<55>	MAKE_BASE=TRUE	=	=MEM_A_DQ<51>
MEM_A_DQ<54>	MAKE_BASE=TRUE	=	=MEM_A_DQ<54>
MEM_A_DQ<53>	MAKE_BASE=TRUE	=	=MEM_A_DQ<49>
MEM_A_DQ<52>	MAKE_BASE=TRUE	=	=MEM_A_DQ<53>
MEM_A_DQ<51>	MAKE_BASE=TRUE	=	=MEM_A_DQ<50>
MEM_A_DQ<50>	MAKE_BASE=TRUE	=	=MEM_A_DQ<55>
MEM_A_DQ<49>	MAKE_BASE=TRUE	=	=MEM_A_DQ<48>
MEM_A_DQ<48>	MAKE_BASE=TRUE	=	=MEM_A_DQ<52>
	MAKE_BASE=TRUE	=	

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_N<7>
MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_A_DQS_P<7>
	MAKE_BASE=TRUE	=	GND
MEM_A_DQ<63>	MAKE_BASE=TRUE	=	=MEM_A_DQ<58>
MEM_A_DQ<62>	MAKE_BASE=TRUE	=	=MEM_A_DQ<59>
MEM_A_DQ<61>	MAKE_BASE=TRUE	=	=MEM_A_DQ<60>
MEM_A_DQ<60>	MAKE_BASE=TRUE	=	=MEM_A_DQ<57>
MEM_A_DQ<59>	MAKE_BASE=TRUE	=	=MEM_A_DQ<63>
MEM_A_DQ<58>	MAKE_BASE=TRUE	=	=MEM_A_DQ<62>
MEM_A_DQ<57>	MAKE_BASE=TRUE	=	=MEM_A_DQ<61>
MEM_A_DQ<56>	MAKE_BASE=TRUE	=	=MEM_A_DQ<56>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_N<0>
MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=	MEM_B_DQS_P<0>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<7>	MAKE_BASE=TRUE	=	=MEM_B_DQ<3>
MEM_B_DQ<6>	MAKE_BASE=TRUE	=	=MEM_B_DQ<2>
MEM_B_DQ<5>	MAKE_BASE=TRUE	=	=MEM_B_DQ<0>
MEM_B_DQ<4>	MAKE_BASE=TRUE	=	=MEM_B_DQ<4>
MEM_B_DQ<3>	MAKE_BASE=TRUE	=	=MEM_B_DQ<7>
MEM_B_DQ<2>	MAKE_BASE=TRUE	=	=MEM_B_DQ<6>
MEM_B_DQ<1>	MAKE_BASE=TRUE	=	=MEM_B_DQ<5>
MEM_B_DQ<0>	MAKE_BASE=TRUE	=	=MEM_B_DQ<1>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<1>
MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<1>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<15>	MAKE_BASE=TRUE	=	=MEM_B_DQ<15>
MEM_B_DQ<14>	MAKE_BASE=TRUE	=	=MEM_B_DQ<14>
MEM_B_DQ<13>	MAKE_BASE=TRUE	=	=MEM_B_DQ<13>
MEM_B_DQ<12>	MAKE_BASE=TRUE	=	=MEM_B_DQ<8>
MEM_B_DQ<11>	MAKE_BASE=TRUE	=	=MEM_B_DQ<11>
MEM_B_DQ<10>	MAKE_BASE=TRUE	=	=MEM_B_DQ<10>
MEM_B_DQ<9>	MAKE_BASE=TRUE	=	=MEM_B_DQ<12>
MEM_B_DQ<8>	MAKE_BASE=TRUE	=	=MEM_B_DQ<9>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<2>
MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<2>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<23>	MAKE_BASE=TRUE	=	=MEM_B_DQ<23>
MEM_B_DQ<22>	MAKE_BASE=TRUE	=	=MEM_B_DQ<18>
MEM_B_DQ<21>	MAKE_BASE=TRUE	=	=MEM_B_DQ<16>
MEM_B_DQ<20>	MAKE_BASE=TRUE	=	=MEM_B_DQ<17>
MEM_B_DQ<19>	MAKE_BASE=TRUE	=	=MEM_B_DQ<22>
MEM_B_DQ<18>	MAKE_BASE=TRUE	=	=MEM_B_DQ<19>
MEM_B_DQ<17>	MAKE_BASE=TRUE	=	=MEM_B_DQ<21>
MEM_B_DQ<16>	MAKE_BASE=TRUE	=	=MEM_B_DQ<20>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<3>
MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<3>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<31>	MAKE_BASE=TRUE	=	=MEM_B_DQ<26>
MEM_B_DQ<30>	MAKE_BASE=TRUE	=	=MEM_B_DQ<30>
MEM_B_DQ<29>	MAKE_BASE=TRUE	=	=MEM_B_DQ<28>
MEM_B_DQ<28>	MAKE_BASE=TRUE	=	=MEM_B_DQ<29>
MEM_B_DQ<27>	MAKE_BASE=TRUE	=	=MEM_B_DQ<27>
MEM_B_DQ<26>	MAKE_BASE=TRUE	=	=MEM_B_DQ<31>
MEM_B_DQ<25>	MAKE_BASE=TRUE	=	=MEM_B_DQ<25>
MEM_B_DQ<24>	MAKE_BASE=TRUE	=	=MEM_B_DQ<24>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<4>
MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<4>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<39>	MAKE_BASE=TRUE	=	=MEM_B_DQ<38>
MEM_B_DQ<38>	MAKE_BASE=TRUE	=	=MEM_B_DQ<39>
MEM_B_DQ<37>	MAKE_BASE=TRUE	=	MEM_B_DQ<37>
MEM_B_DQ<36>	MAKE_BASE=TRUE	=	=MEM_B_DQ<37>
MEM_B_DQ<35>	MAKE_BASE=TRUE	=	=MEM_B_DQ<34>
MEM_B_DQ<34>	MAKE_BASE=TRUE	=	=MEM_B_DQ<35>
MEM_B_DQ<33>	MAKE_BASE=TRUE	=	=MEM_B_DQ<32>
MEM_B_DQ<32>	MAKE_BASE=TRUE	=	=MEM_B_DQ<36>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<5>
MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<5>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<47>	MAKE_BASE=TRUE	=	=MEM_B_DQ<43>
MEM_B_DQ<46>	MAKE_BASE=TRUE	=	=MEM_B_DQ<46>
MEM_B_DQ<45>	MAKE_BASE=TRUE	=	=MEM_B_DQ<40>
MEM_B_DQ<44>	MAKE_BASE=TRUE	=	=MEM_B_DQ<45>
MEM_B_DQ<43>	MAKE_BASE=TRUE	=	=MEM_B_DQ<47>
MEM_B_DQ<42>	MAKE_BASE=TRUE	=	=MEM_B_DQ<42>
MEM_B_DQ<41>	MAKE_BASE=TRUE	=	=MEM_B_DQ<41>
MEM_B_DQ<40>	MAKE_BASE=TRUE	=	=MEM_B_DQ<44>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<6>
MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<6>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<55>	MAKE_BASE=TRUE	=	=MEM_B_DQ<54>
MEM_B_DQ<54>	MAKE_BASE=TRUE	=	=MEM_B_DQ<55>
MEM_B_DQ<53>	MAKE_BASE=TRUE	=	=MEM_B_DQ<53>
MEM_B_DQ<52>	MAKE_BASE=TRUE	=	=MEM_B_DQ<49>
MEM_B_DQ<51>	MAKE_BASE=TRUE	=	=MEM_B_DQ<51>
MEM_B_DQ<50>	MAKE_BASE=TRUE	=	=MEM_B_DQ<50>
MEM_B_DQ<49>	MAKE_BASE=TRUE	=	=MEM_B_DQ<48>
MEM_B_DQ<48>	MAKE_BASE=TRUE	=	=MEM_B_DQ<52>
	MAKE_BASE=TRUE	=	

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_N<7>
MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=	=MEM_B_DQS_P<7>
	MAKE_BASE=TRUE	=	GND
MEM_B_DQ<63>	MAKE_BASE=TRUE	=	=MEM_B_DQ<56>
MEM_B_DQ<62>	MAKE_BASE=TRUE	=	=MEM_B_DQ<59>
MEM_B_DQ<61>	MAKE_BASE=TRUE	=	=MEM_B_DQ<61>
MEM_B_DQ<60>	MAKE_BASE=TRUE	=	=MEM_B_DQ<60>
MEM_B_DQ<59>	MAKE_BASE=TRUE	=	=MEM_B_DQ<63>
MEM_B_DQ<58>	MAKE_BASE=TRUE	=	=MEM_B_DQ<58>
MEM_B_DQ<57>	MAKE_BASE=TRUE	=	=MEM_B_DQ<57>
MEM_B_DQ<56>	MAKE_BASE=TRUE	=	=MEM_B_DQ<62>
	MAKE_BASE=TRUE	=	

NOTE: Sandybridge does not use DM signals per doc 438297 Huron River SFF DG rev1.0 Section 2.6.13

SYNC_MASTER=ANNE_K90I SYNC_DATE=06/22/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

DRAWING NUMBER

SIZE D

REVISION

BRANCH

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DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PP5PO_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMM0_SCL
- =I2C_SODIMM0_SDA

BOM options provided by this page:
(NONE)

72 67 30 27 7 6 PP1V5_S3

C3100 10UF 20% 6.3V X5R 603
C3101 10UF 20% 6.3V X5R 603
C3110 0.1UF 20% 10V CERM 402
C3111 0.1UF 20% 10V CERM 402
C3112 0.1UF 20% 10V CERM 402
C3113 0.1UF 20% 10V CERM 402
C3114 0.1UF 20% 10V CERM 402
C3115 0.1UF 20% 10V CERM 402
C3116 0.1UF 20% 10V CERM 402
C3117 0.1UF 20% 10V CERM 402
C3118 0.1UF 20% 10V CERM 402
C3119 0.1UF 20% 10V CERM 402
C3120 0.1UF 20% 10V CERM 402
C3121 0.1UF 20% 10V CERM 402
C3122 0.1UF 20% 10V CERM 402
C3123 0.1UF 20% 10V CERM 402

31 9 PP0V75_S3_MEM_VREFDQ_B

C3130 2.2UF 20% 6.3V CERM 402-LF
C3131 0.1UF 20% 10V CERM 402

J3100 DDR3-SODIMM (2 OF 2) F-RT-BGA6

79 11 IN	MEM_B_CKE<0>	73	CKE0	CKE1	74	MEM_B_CKE<1>	IN 11 79
NC		75	VDD	VDD	76		
		77	NC	A15	78	MEM_B_A<15>	IN 11 79
79 11 IN	MEM_B_BA<2>	79	BA2	A14	80	MEM_B_A<14>	IN 11 79
		81	VDD	VDD	82		
79 11 IN	MEM_B_A<12>	83	A12/BC*	A11	84	MEM_B_A<11>	IN 11 79
79 11 IN	MEM_B_A<9>	85	A9	A7	86	MEM_B_A<7>	IN 11 79
		87	VDD	VDD	88		
79 11 IN	MEM_B_A<8>	89	A8	A6	90	MEM_B_A<6>	IN 11 79
79 11 IN	MEM_B_A<5>	91	A5	A4	92	MEM_B_A<4>	IN 11 79
		93	VDD	VDD	94		
79 11 IN	MEM_B_A<3>	95	A3	A2	96	MEM_B_A<2>	IN 11 79
79 11 IN	MEM_B_A<1>	97	A1	A0	98	MEM_B_A<0>	IN 11 79
		99	VDD	VDD	100		
79 11 IN	MEM_B_CLK_P<0>	101	CK0	CK1	102	MEM_B_CLK_P<1>	IN 11 79
79 11 IN	MEM_B_CLK_N<0>	103	CK0*	CK1*	104	MEM_B_CLK_N<1>	IN 11 79
		105	VDD	VDD	106		
79 11 IN	MEM_B_A<10>	107	A10/AP	BA1	108	MEM_B_BA<1>	IN 11 79
79 11 IN	MEM_B_BA<0>	109	BA0	RAS*	110	MEM_B_RAS_L	IN 11 79
		111	VDD	VDD	112		
79 11 IN	MEM_B_WE_L	113	WE*	S0*	114	MEM_B_CS_L<0>	IN 11 79
79 11 IN	MEM_B_CAS_L	115	CAS*	ODT0	116	MEM_B_ODT<0>	IN 11 79
		117	VDD	VDD	118		
79 11 IN	MEM_B_A<13>	119	A13	ODT1	120	MEM_B_ODT<1>	IN 11 79
79 11 IN	MEM_B_CS_L<1>	121	S1*	NC	122	NC	
		123	VDD	VDD	124		
NC		125	TEST	VREFCA	126		
		127	VSS	VSS	128		
28 BI	=MEM_B_DQ<32>	129	DQ32	DQ36	130	=MEM_B_DQ<36>	BI 28
79 28 11 BI	MEM_B_DQ<37>	131	DQ33	DQ37	132	=MEM_B_DQ<37>	BI 28
		133	VSS	VSS	134		
28 BI	=MEM_B_DQS_N<4>	135	DQS4*	DM4	136	GND	IN
28 BI	=MEM_B_DQS_P<4>	137	DQS4	VSS	138		
		139	VSS	DQ38	140	=MEM_B_DQ<38>	BI 28
28 BI	=MEM_B_DQ<34>	141	DQ34	DQ39	142	=MEM_B_DQ<39>	BI 28
28 BI	=MEM_B_DQ<35>	143	DQ35	VSS	144		
		145	VSS	DQ44	146	=MEM_B_DQ<44>	BI 28
28 BI	=MEM_B_DQ<40>	147	DQ40	DQ45	148	=MEM_B_DQ<45>	BI 28
28 BI	=MEM_B_DQ<41>	149	DQ41	VSS	150		
		151	VSS	DQS5*	152	=MEM_B_DQS_N<5>	BI 28
IN	GND	153	DM5	DQS5	154	=MEM_B_DQS_P<5>	BI 28
		155	VSS	VSS	156		
28 BI	=MEM_B_DQ<42>	157	DQ42	DQ46	158	=MEM_B_DQ<46>	BI 28
28 BI	=MEM_B_DQ<43>	159	DQ43	DQ47	160	=MEM_B_DQ<47>	BI 28
		161	VSS	VSS	162		
28 BI	=MEM_B_DQ<48>	163	DQ48	DQ52	164	=MEM_B_DQ<52>	BI 28
28 BI	=MEM_B_DQ<49>	165	DQ49	DQ53	166	=MEM_B_DQ<53>	BI 28
		167	VSS	VSS	168		
28 BI	=MEM_B_DQS_N<6>	169	DQS6*	DM6	170	GND	IN
28 BI	=MEM_B_DQS_P<6>	171	DQS6	VSS	172		
		173	VSS	DQ54	174	=MEM_B_DQ<54>	BI 28
28 BI	=MEM_B_DQ<50>	175	DQ50	DQ55	176	=MEM_B_DQ<55>	BI 28
28 BI	=MEM_B_DQ<51>	177	DQ51	VSS	178		
		179	VSS	DQ60	180	=MEM_B_DQ<60>	BI 28
28 BI	=MEM_B_DQ<56>	181	DQ56	DQ61	182	=MEM_B_DQ<61>	BI 28
28 BI	=MEM_B_DQ<57>	183	DQ57	VSS	184		
		185	VSS	DQS7*	186	=MEM_B_DQS_N<7>	BI 28
IN	GND	187	DM7	DQS7	188	=MEM_B_DQS_P<7>	BI 28
		189	VSS	VSS	190		
28 BI	=MEM_B_DQ<58>	191	DQ58	DQ62	192	=MEM_B_DQ<62>	BI 28
28 BI	=MEM_B_DQ<59>	193	DQ59	DQ63	194	=MEM_B_DQ<63>	BI 28
		195	VSS	VSS	196		
MEM_B_SA<0>		197	SA0	EVENT*	198	MEM_EVENT_L	OUT 27 45
49 48 46 42 41 39 PP3V3_S0		199	VDDSPD	SDA	200	SMBUS_PCH_DATA	BI 16 23 27 31 42 48 62 77 81
37 36 34 19 17 16 12 8 7 6		201	SA1	SCL	202	SMBUS_PCH_CLK	IN 16 23 27 31 42 48 62 77 81
72 71 62 61 57 54 52 51 50	MEM_B_SA<1>	203	VTT	VTT	204	PP0V75_S0_DDRVTT	7 27 30 67
		MTG PINS					
		205	MTG PIN	MTG PIN	206		
		207	MTG PIN	MTG PIN	208		
		209	MTG PIN	MTG PIN	210		
		211	MTG PIN	MTG PIN	212		

516S0806
SPD ADDR=0xA4(WR)/0xA5(RD)

C3140 2.2UF 20% 6.3V CERM 402-LF
R3140 10K 5% 1/16W MF-LF 402
R3141 10K 5% 1/16W MF-LF 402

J3100 DDR3-SODIMM (1 OF 2) F-RT-BGA6 CRITICAL

		1	VREFDQ	VSS	2		
		3	VSS	DQ4	4	=MEM_B_DQ<4>	BI 28
28 BI	=MEM_B_DQ<0>	5	DQ0	DQ5	6	=MEM_B_DQ<5>	BI 28
28 BI	=MEM_B_DQ<1>	7	DQ1	VSS	8		
		9	VSS	DQS0*	10	MEM_B_DQS_N<0>	BI 11 28 79
IN	GND	11	DM0	DQS0	12	MEM_B_DQS_P<0>	BI 11 28 79
		13	VSS	VSS	14		
28 BI	=MEM_B_DQ<2>	15	DQ2	DQ6	16	=MEM_B_DQ<6>	BI 28
28 BI	=MEM_B_DQ<3>	17	DQ3	DQ7	18	=MEM_B_DQ<7>	BI 28
		19	VSS	VSS	20		
28 BI	=MEM_B_DQ<8>	21	DQ8	DQ12	22	=MEM_B_DQ<12>	BI 28
28 BI	=MEM_B_DQ<9>	23	DQ9	DQ13	24	=MEM_B_DQ<13>	BI 28
		25	VSS	VSS	26		
28 BI	=MEM_B_DQS_N<1>	27	DQS1*	DM1	28	GND	IN
28 BI	=MEM_B_DQS_P<1>	29	DQS1	RESET*	30	MEM_RESET_L	IN 27 30
		31	VSS	VSS	32		
28 BI	=MEM_B_DQ<10>	33	DQ10	DQ14	34	=MEM_B_DQ<14>	BI 28
28 BI	=MEM_B_DQ<11>	35	DQ11	DQ15	36	=MEM_B_DQ<15>	BI 28
		37	VSS	VSS	38		
28 BI	=MEM_B_DQ<16>	39	DQ16	DQ20	40	=MEM_B_DQ<20>	BI 28
28 BI	=MEM_B_DQ<17>	41	DQ17	DQ21	42	=MEM_B_DQ<21>	BI 28
		43	VSS	VSS	44		
28 BI	=MEM_B_DQS_N<2>	45	DQS2*	DM2	46	GND	IN
28 BI	=MEM_B_DQS_P<2>	47	DQS2	VSS	48		
		49	VSS	DQ22	50	=MEM_B_DQ<22>	BI 28
28 BI	=MEM_B_DQ<18>	51	DQ18	DQ23	52	=MEM_B_DQ<23>	BI 28
28 BI	=MEM_B_DQ<19>	53	DQ19	VSS	54		
		55	VSS	DQ28	56	=MEM_B_DQ<28>	BI 28
28 BI	=MEM_B_DQ<24>	57	DQ24	DQ29	58	=MEM_B_DQ<29>	BI 28
28 BI	=MEM_B_DQ<25>	59	DQ25	VSS	60		
		61	VSS	DQS3*	62	=MEM_B_DQS_N<3>	BI 28
IN	GND	63	DM3	DQS3	64	=MEM_B_DQS_P<3>	BI 28
		65	VSS	VSS	66		
28 BI	=MEM_B_DQ<26>	67	DQ26	DQ30	68	=MEM_B_DQ<30>	BI 28
28 BI	=MEM_B_DQ<27>	69	DQ27	DQ31	70	=MEM_B_DQ<31>	BI 28
		71	VSS	VSS	72		

KEY
516S0806

PP0V75_S3_MEM_VREFCA_B 31

C3135 2.2UF 20% 6.3V CERM 402-LF
C3136 0.1UF 20% 10V CERM 402

C3150 1UF 10% 10V X5R 402
C3151 1UF 10% 10V X5R 402
C3152 1UF 10% 10V X5R 402
C3153 1UF 10% 10V X5R 402

"Expansion" (bottom) slot

SYNC_MASTER=MASTER SYNC_DATE=MASTER
PAGE TITLE: DDR3 SO-DIMM Connector B
Apple Inc.
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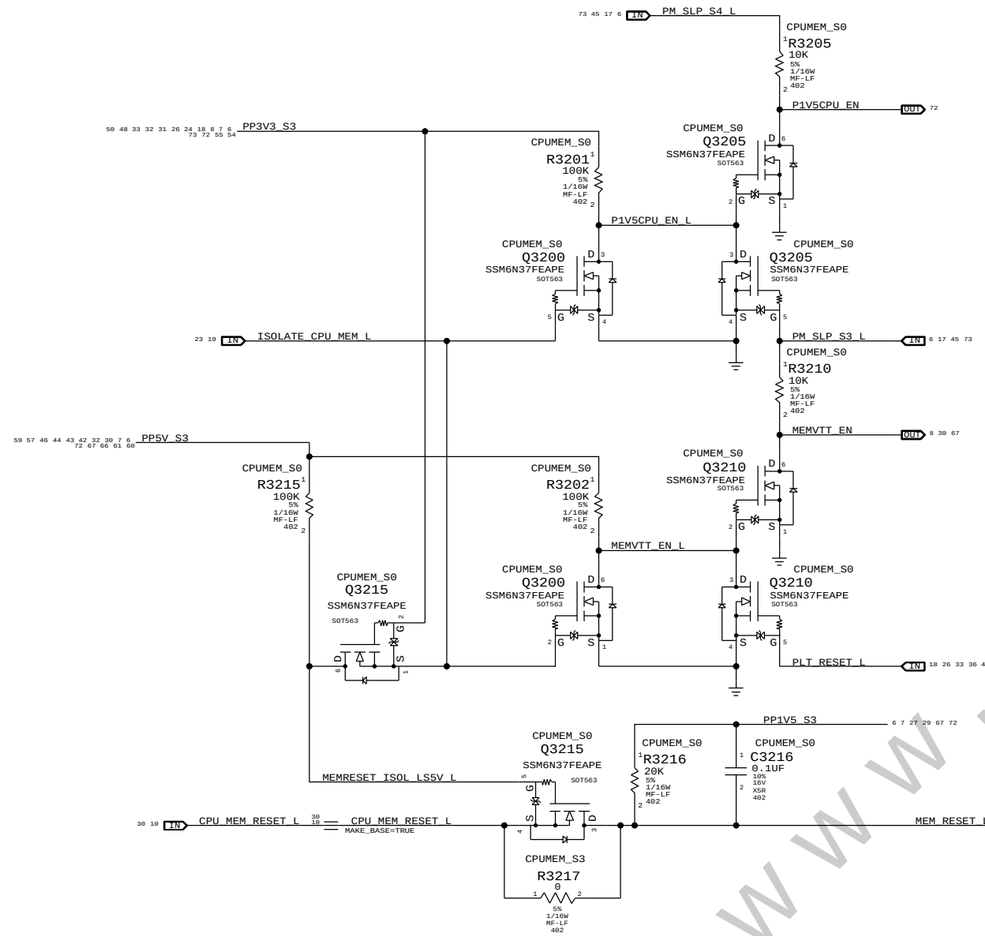
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

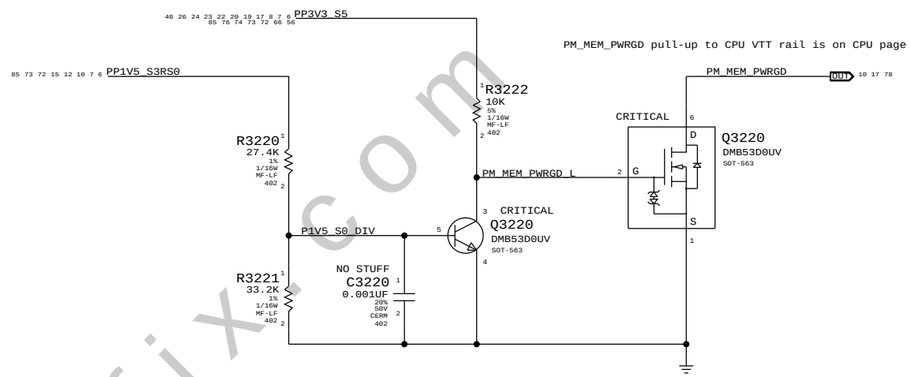


	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
S3	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

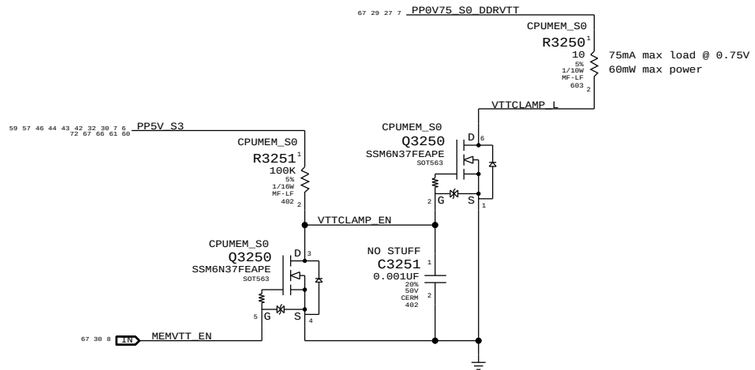
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=ANNE_K90I SYNC_DATE=06/22/2010

PAGE TITLE: CPU Memory S3 Support

Apple Inc.

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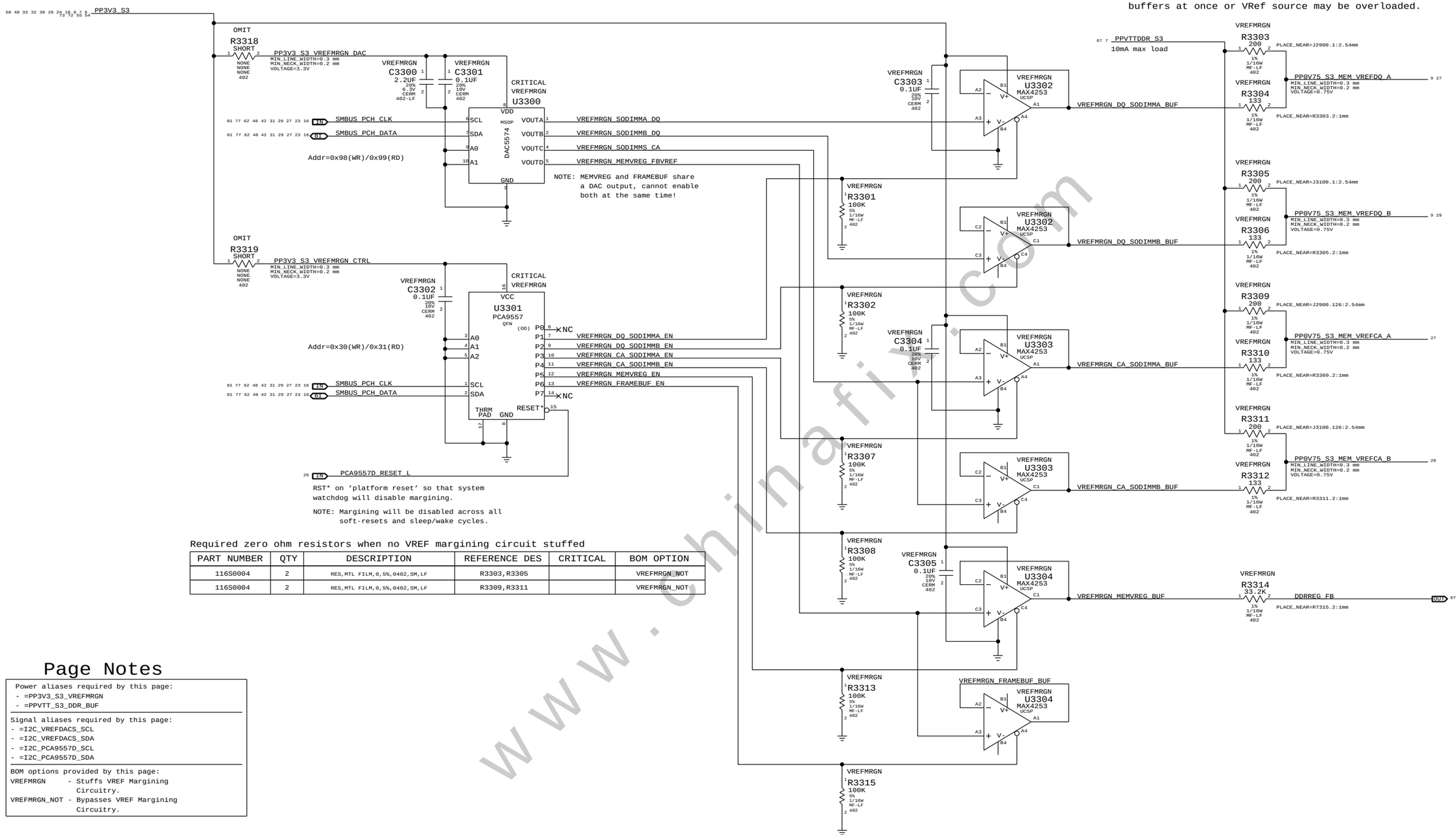

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC_MASTER=K91_MLB SYNC_DATE=06/01/2010

PAGE TITLE: FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

DRAWING NUMBER: SIZE D

REVISION:

BRANCH:

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0ohm, 0201	L3470,L3471,L3472,L3473		

3V S3 WLAN FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	20-30 MOHM @2.5V
LOADING	0.727 A (EDP)

AIRPORT

BLUETOOTH

ALS CAMERA

Supervisor & CLKFREG # ISolation

Delay = 60 ms +/- 20%

SYNC_MASTER=K91_MLB	SYNC_DATE=05/15/2010
PAGE TITLE	X19/ALS/CAMERA CONNECTOR
Apple Inc.	DRAWING NUMBER: D
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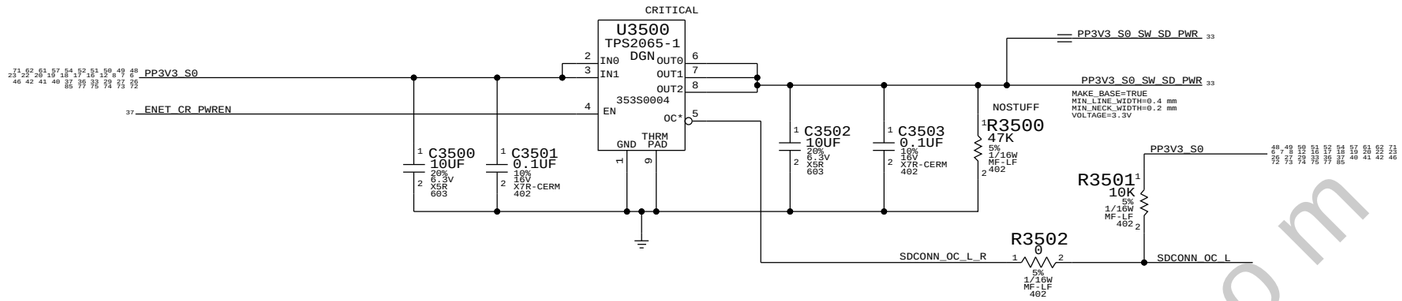
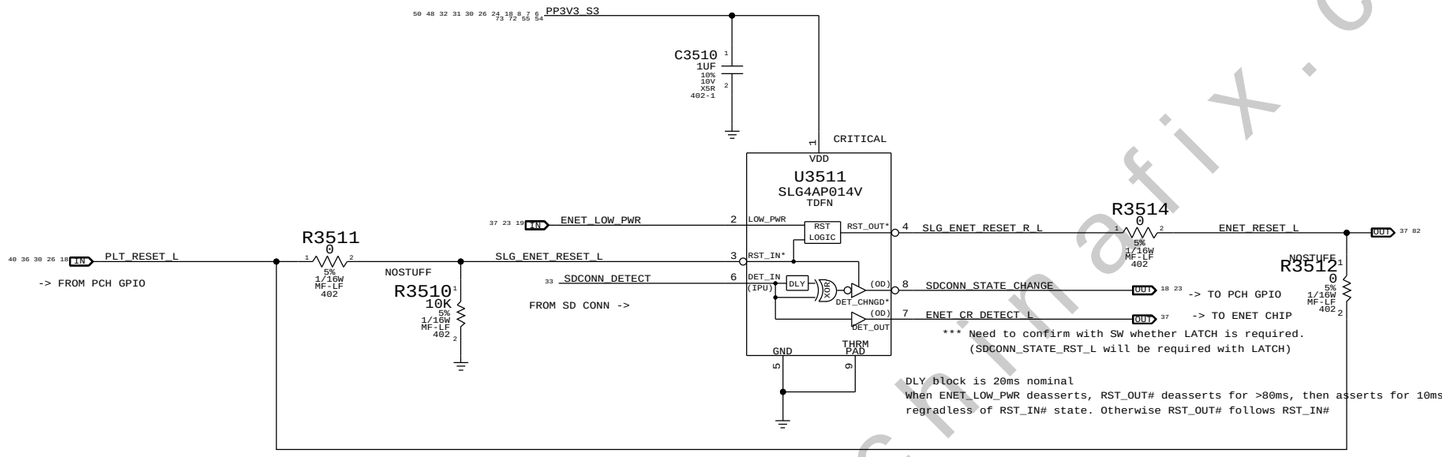
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

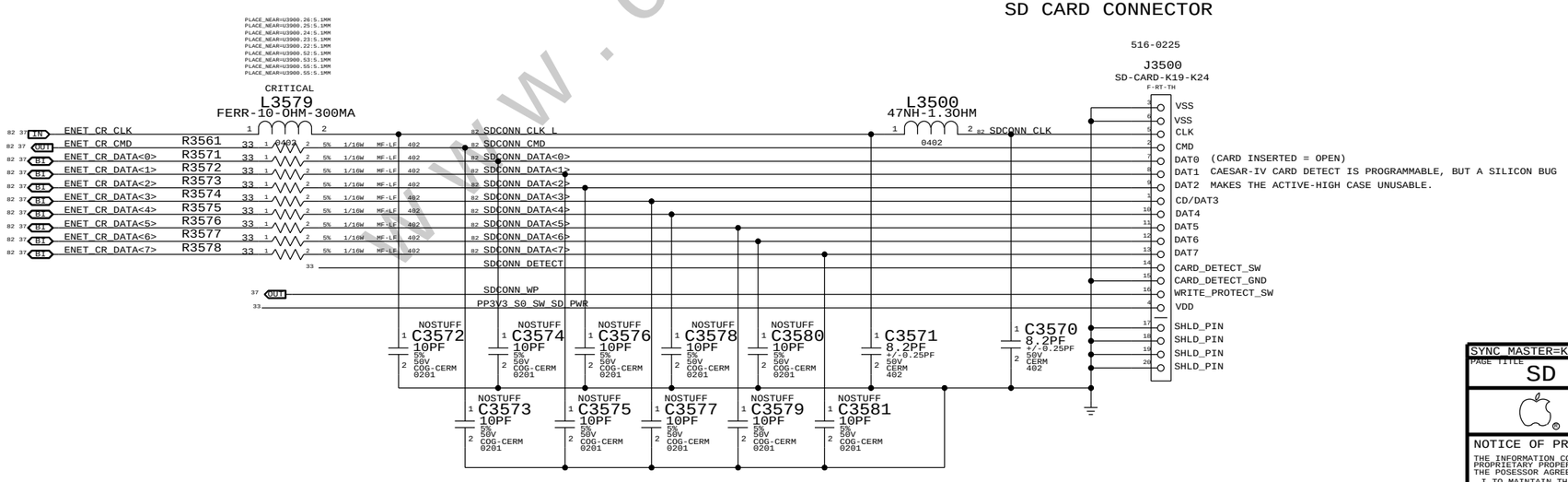
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SD CARD CONNECTOR



SYNC_MASTER=K91_MLB SYNC_DATE=05/26/2016

PAGE TITLE: SD READER CONNECTOR

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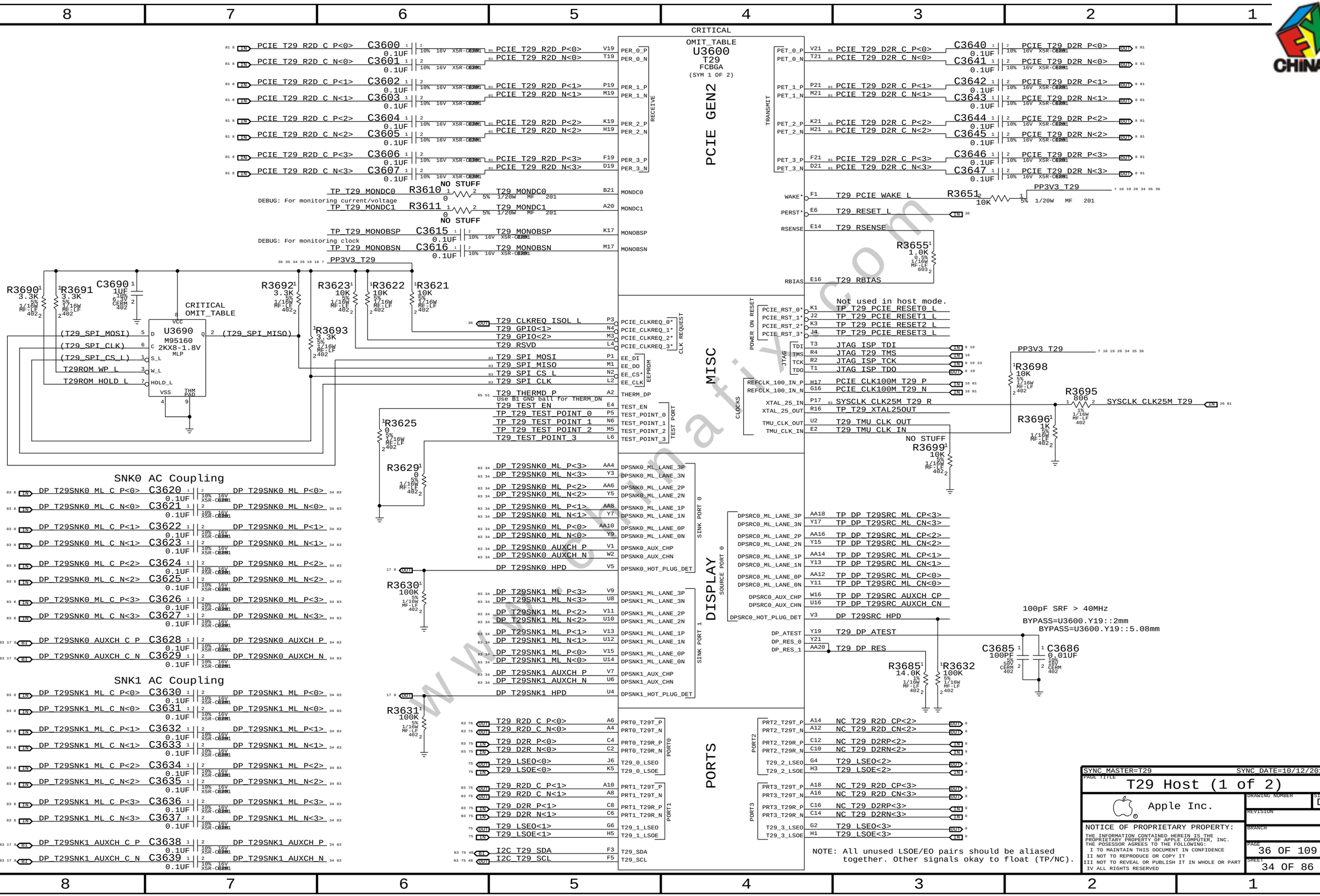
CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)
PCIE GEN2
RECEIVE
TRANSMIT
PCIE T29 R2D C P<0>
PCIE T29 R2D C N<0>
PCIE T29 R2D C P<1>
PCIE T29 R2D C N<1>
PCIE T29 R2D C P<2>
PCIE T29 R2D C N<2>
PCIE T29 R2D C P<3>
PCIE T29 R2D C N<3>
PCIE T29 R2D P<0>
PCIE T29 R2D N<0>
PCIE T29 R2D P<1>
PCIE T29 R2D N<1>
PCIE T29 R2D P<2>
PCIE T29 R2D N<2>
PCIE T29 R2D P<3>
PCIE T29 R2D N<3>
PCIE T29 D2R C P<0>
PCIE T29 D2R C N<0>
PCIE T29 D2R C P<1>
PCIE T29 D2R C N<1>
PCIE T29 D2R C P<2>
PCIE T29 D2R C N<2>
PCIE T29 D2R C P<3>
PCIE T29 D2R C N<3>
PCIE T29 D2R P<0>
PCIE T29 D2R N<0>
PCIE T29 D2R P<1>
PCIE T29 D2R N<1>
PCIE T29 D2R P<2>
PCIE T29 D2R N<2>
PCIE T29 D2R P<3>
PCIE T29 D2R N<3>
NO STUFF
TP_T29_MONDC0
TP_T29_MONDC1
DEBUG: For monitoring current/voltage
TP_T29_MONOBSP
TP_T29_MONOBSN
DEBUG: For monitoring clock
PP3V3_T29
CRITICAL
OMIT_TABLE
U3690
M95160
2KX8-1.8V
MLP
(T29_SPI_MOSI)
(T29_SPI_CLK)
(T29_SPI_CS_L)
T29ROM_WP_L
T29ROM_HOLD_L
(T29_SPI_MISO)
T29_CLKREQ_ISOL_L
T29_GPIO<1>
T29_GPIO<2>
T29_RSVD
T29_SPI_MOSI
T29_SPI_MISO
T29_SPI_CS_L
T29_SPI_CLK
T29_THERMD_P
Use B1 GND ball for THERM_DN
T29_TEST_EN
TP_T29_TEST_POINT_0
TP_T29_TEST_POINT_1
TP_T29_TEST_POINT_2
T29_TEST_POINT_3
CLK REQUEST
EEPROM
TEST PORT
MISC
POWER ON RESET
JTAG
CLOCKS
Not used in host mode.
TP_T29_PCIE_RESET0_L
TP_T29_PCIE_RESET1_L
TP_T29_PCIE_RESET2_L
TP_T29_PCIE_RESET3_L
JTAG_ISP_TDI
JTAG_T29_TMS
JTAG_T29_TCK
JTAG_ISP_TDO
PCIE_CLK100M_T29_P
PCIE_CLK100M_T29_N
SYSCLK_CLK25M_T29_R
TP_T29_XTAL25OUT
T29_TMU_CLK_OUT
T29_TMU_CLK_IN
SYSCLK_CLK25M_T29
NO STUFF
WAKE*
PERST*
RSENSE
RBIAS
T29_PCIE_WAKE_L
T29_RESET_L
T29_RSENSE
T29_RBIAS
SNK0 AC Coupling
SNK1 AC Coupling
DP_T29SNK0_ML_C_P<0>
DP_T29SNK0_ML_C_N<0>
DP_T29SNK0_ML_C_P<1>
DP_T29SNK0_ML_C_N<1>
DP_T29SNK0_ML_C_P<2>
DP_T29SNK0_ML_C_N<2>
DP_T29SNK0_ML_C_P<3>
DP_T29SNK0_ML_C_N<3>
DP_T29SNK0_AUXCH_C_P
DP_T29SNK0_AUXCH_C_N
DP_T29SNK1_ML_C_P<0>
DP_T29SNK1_ML_C_N<0>
DP_T29SNK1_ML_C_P<1>
DP_T29SNK1_ML_C_N<1>
DP_T29SNK1_ML_C_P<2>
DP_T29SNK1_ML_C_N<2>
DP_T29SNK1_ML_C_P<3>
DP_T29SNK1_ML_C_N<3>
DP_T29SNK1_AUXCH_C_P
DP_T29SNK1_AUXCH_C_N
DP_T29SNK0_ML_P<3>
DP_T29SNK0_ML_N<3>
DP_T29SNK0_ML_P<2>
DP_T29SNK0_ML_N<2>
DP_T29SNK0_ML_P<1>
DP_T29SNK0_ML_N<1>
DP_T29SNK0_ML_P<0>
DP_T29SNK0_ML_N<0>
DP_T29SNK0_AUXCH_P
DP_T29SNK0_AUXCH_N
DP_T29SNK0_HPD
DP_T29SNK1_ML_P<3>
DP_T29SNK1_ML_N<3>
DP_T29SNK1_ML_P<2>
DP_T29SNK1_ML_N<2>
DP_T29SNK1_ML_P<1>
DP_T29SNK1_ML_N<1>
DP_T29SNK1_ML_P<0>
DP_T29SNK1_ML_N<0>
DP_T29SNK1_AUXCH_P
DP_T29SNK1_AUXCH_N
DP_T29SNK1_HPD
SINK PORT 0
SINK PORT 1
SOURCE PORT 0
DISPLAY
TP_DP_T29SRC_ML_CP<3>
TP_DP_T29SRC_ML_CN<3>
TP_DP_T29SRC_ML_CP<2>
TP_DP_T29SRC_ML_CN<2>
TP_DP_T29SRC_ML_CP<1>
TP_DP_T29SRC_ML_CN<1>
TP_DP_T29SRC_ML_CP<0>
TP_DP_T29SRC_ML_CN<0>
TP_DP_T29SRC_AUXCH_CP
TP_DP_T29SRC_AUXCH_CN
DP_T29SRC_HPD
T29_DP_ATEST
T29_DP_RES
100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm
PORTS
PORT0
PORT1
PORT2
PORT3
T29_R2D_C_P<0>
T29_R2D_C_N<0>
T29_D2R_P<0>
T29_D2R_N<0>
T29_LSEO<0>
T29_LSOE<0>
T29_R2D_C_P<1>
T29_R2D_C_N<1>
T29_D2R_P<1>
T29_D2R_N<1>
T29_LSEO<1>
T29_LSOE<1>
I2C_T29_SDA
I2C_T29_SCL
NC_T29_R2D_CP<2>
NC_T29_R2D_CN<2>
NC_T29_D2RP<2>
NC_T29_D2RN<2>
T29_LSEO<2>
T29_LSOE<2>
NC_T29_R2D_CP<3>
NC_T29_R2D_CN<3>
NC_T29_D2RP<3>
NC_T29_D2RN<3>
T29_LSEO<3>
T29_LSOE<3>
NOTE: All unused LSOE/EO pairs should be aliased together. Other signals okay to float (TP/NC).
SYNC_MASTER=T29
SYNC_DATE=10/12/2010
PAGE TITLE
T29 Host (1 of 2)
Apple Inc.
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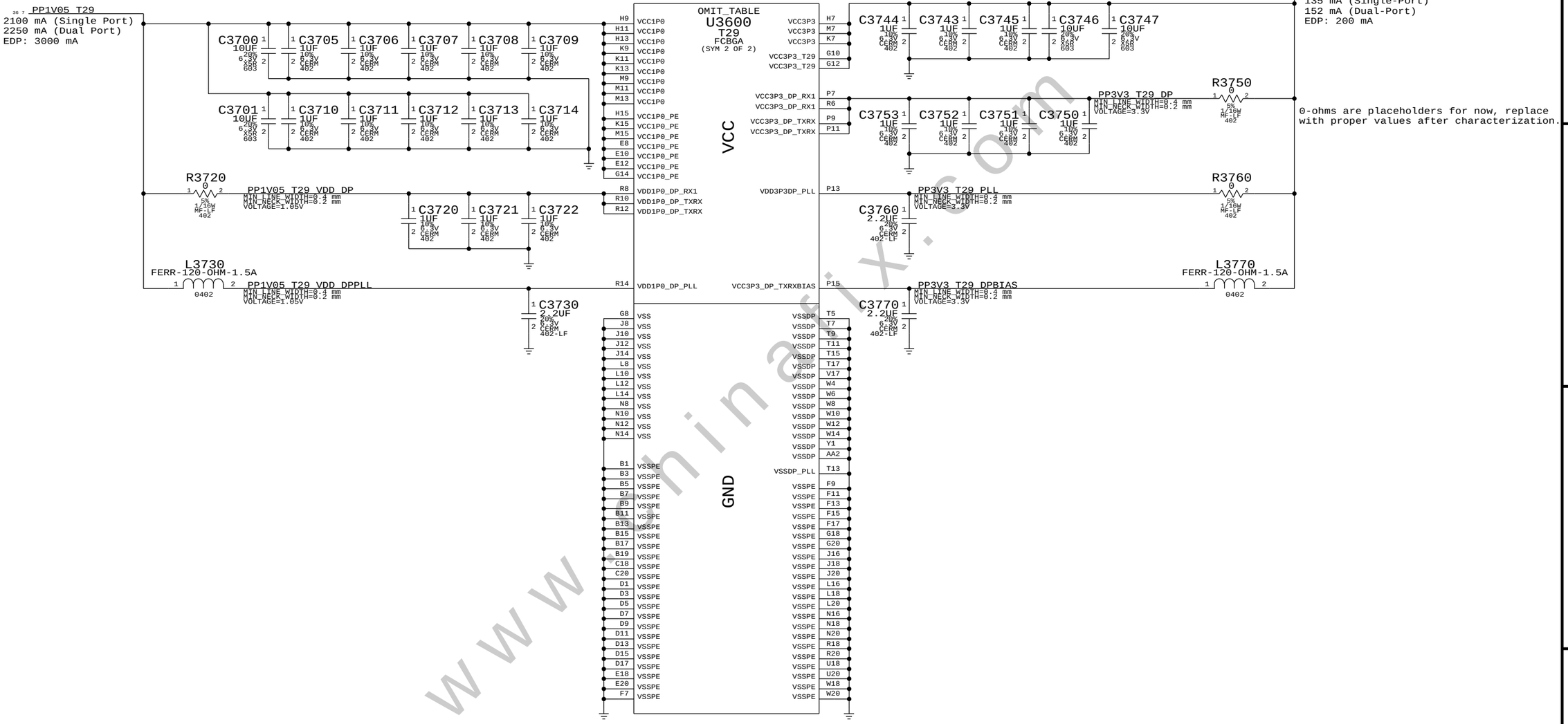

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29 SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (2 of 2)

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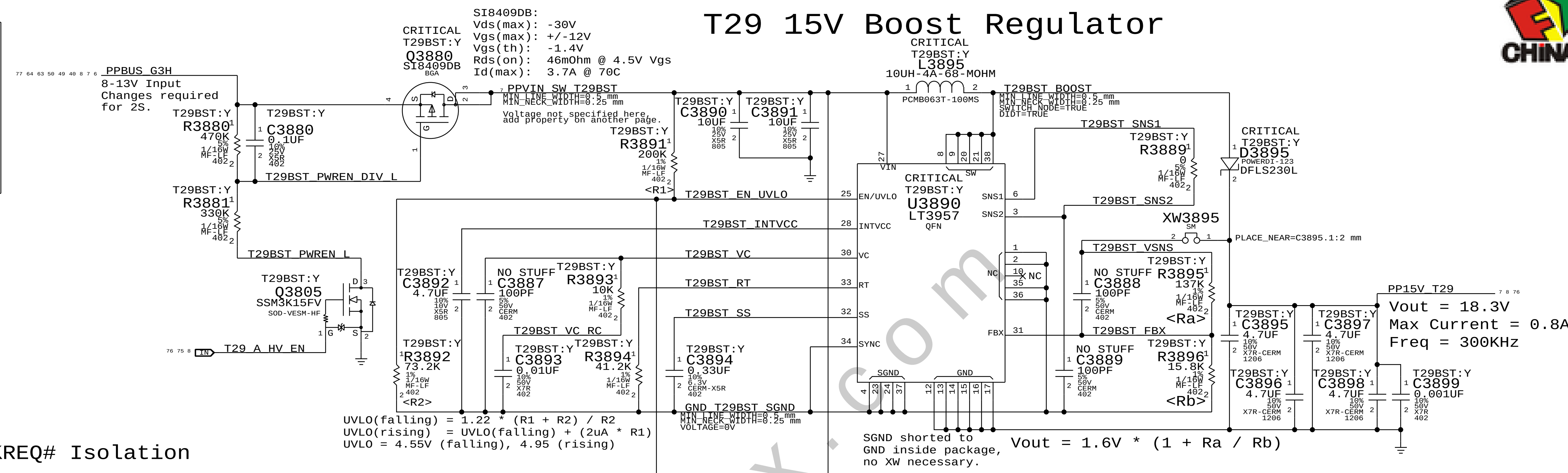
T29 15V Boost Regulator

Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

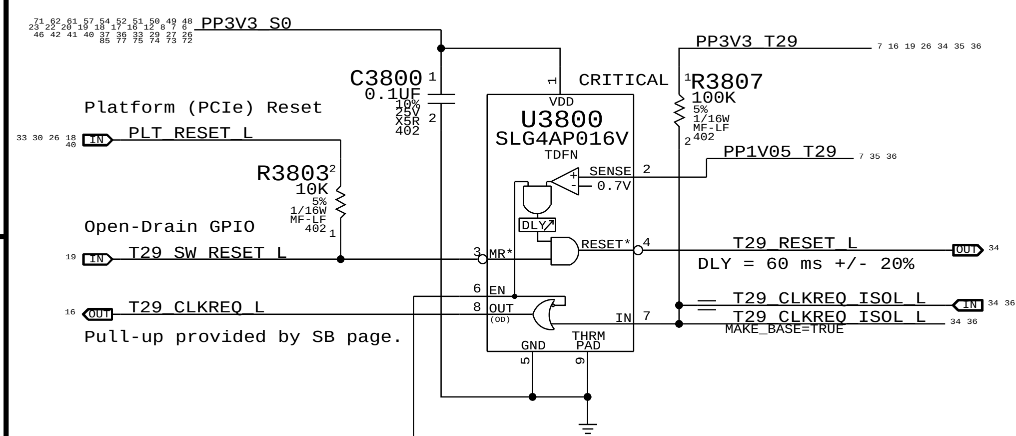
Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.



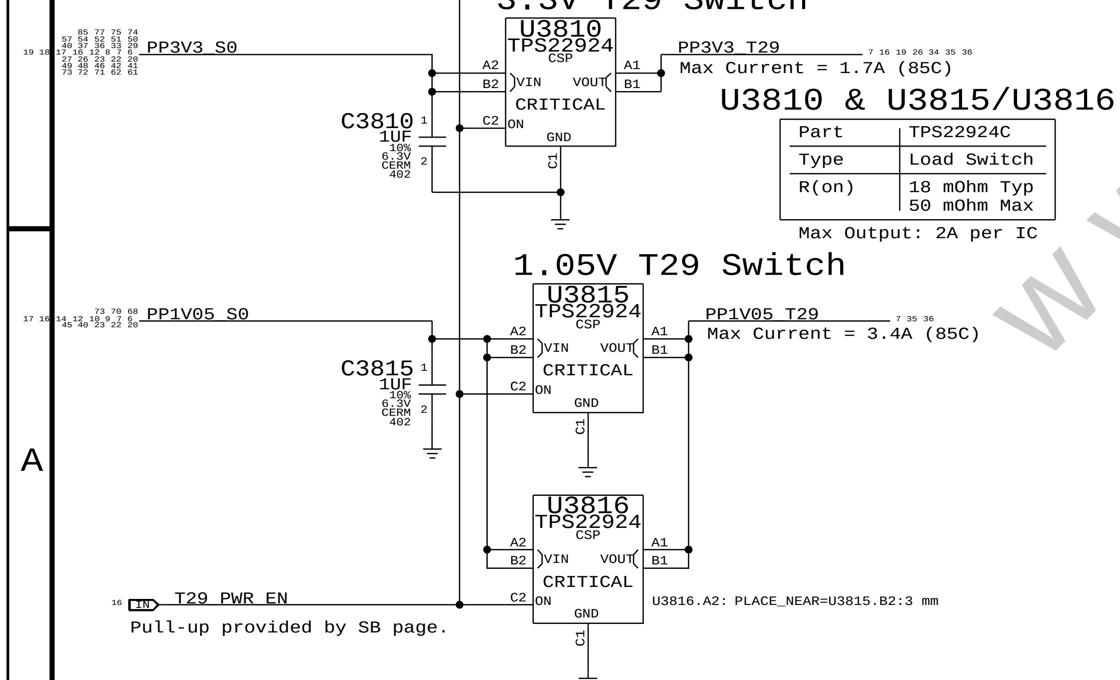
PPBUS_G3H
8-13V Input
Changes required for 2S.
SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C
CRITICAL T29BST:Y Q3880 SI8409DB BGA
PPVIN_SW_T29BST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here, add property on another page.
CRITICAL T29BST:Y L3895 10UH-4A-68-MOHM PCMB063T-100MS
T29BST_BOOST
SWITCH_NODE=TRUE
DIDT=TRUE
T29BST:Y R3880 470K
T29BST:Y C3880 0.1UF
T29BST_PWREN_DIV_L
T29BST:Y R3881 330K
T29BST_PWREN_L
T29BST:Y Q3805 SSM3K15FV SOD-VESM-HF
T29_A_HV_EN
T29BST:Y C3890 10UF
T29BST:Y C3891 10UF
T29BST:Y R3891 200K
<R1>
T29BST_EN_UVLO
T29BST_INTVCC
T29BST_VC
T29BST_RT
T29BST_SS
CRITICAL T29BST:Y U3890 LT3957 QFN
VIN EN/UVLO INTVCC VC RT SS SYNC SW SNS1 SNS2 FBX NC SGND GND
T29BST_SNS1
T29BST_SNS2
T29BST:Y R3889 0
CRITICAL T29BST:Y D3895 POWERDI-123 DFLS230L
XW3895 SM
PLACE_NEAR=C3895.1:2 mm
T29BST_VSNS
NO STUFF C3888 100PF
R3895 137K <Ra>
T29BST_FBX
NO STUFF C3889 100PF
T29BST:Y R3896 15.8K <Rb>
T29BST:Y C3892 4.7UF
NO STUFF C3887 100PF
T29BST:Y R3893 10K
T29BST_VC_RC
T29BST:Y C3893 0.01UF
T29BST:Y R3894 41.2K
T29BST:Y R3892 73.2K <R2>
T29BST:Y C3894 0.33UF
GND_T29BST_SGND
VOLTAGE=0V
UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)
SGND shorted to GND inside package, no XW necessary.
Vout = 1.6V * (1 + Ra / Rb)
PP15V_T29
Vout = 18.3V
Max Current = 0.8A
Freq = 300KHz
T29BST:Y C3895 4.7UF
T29BST:Y C3897 4.7UF
T29BST:Y C3896 4.7UF
T29BST:Y C3898 4.7UF
T29BST:Y C3899 0.001UF
T29BST:Y Q3888 SSM6N37FEAPE SOT563
Max Vgs: 10V
T29BST:Y R3888 330K
T29BST_SHDN_DIV
T29BST:Y R3887 330K
SMC_DELAYED_PWRGD

Supervisor & CLKREQ# Isolation



PP3V3_S0
C3800 0.1UF
CRITICAL
U3800 SLG4AP016V TDFN
PP3V3_T29
R3807 100K
Platform (PCIe) Reset
PLT_RESET_L
R3803 10K
Open-Drain GPIO
T29_SW_RESET_L
SENSE 0.7V
PP1V05_T29
RESET*
T29_RESET_L
DLY = 60 ms +/- 20%
T29_CLKREQ_L
Pull-up provided by SB page.
T29_CLKREQ_ISOL_L
MAKE_BASE=TRUE

3.3V T29 Switch



PP3V3_S0
U3810 TPS22924 CSP
CRITICAL
PP3V3_T29
Max Current = 1.7A (85C)
C3810 1UF
1.05V T29 Switch
PP1V05_S0
U3815 TPS22924 CSP
PP1V05_T29
Max Current = 3.4A (85C)
C3815 1UF
U3816 TPS22924 CSP
T29_PWR_EN
Pull-up provided by SB page.
U3816.A2: PLACE_NEAR=U3815.B2:3 mm

U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

SYNC_MASTER=T29 SYNC_DATE=10/12/2010

PAGE TITLE: T29 Power Support

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BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

73 71 37 26 7 6 PP3V3_ENET
281mA (1000base-T max power, Caesar IV)

VDD for Card Reader I/O
37 PP3V3R1V8_ENET_LR_OUT_REG

CRITICAL L3900 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V
C3900 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3905 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V
C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL L3910 FERR-600-OHM-0.5A — PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V
R3910 4.7K 5% 1/16W MF-LF 402
C3910 0.1UF 10% 16V X7R-CERM 402
C3911 0.1UF 10% 16V X7R-CERM 402

R3940 4.7K 5% 1/16W MF-LF 402
R3941 4.7K 5% 1/16W MF-LF 402
C3915 4.7UF 10% 6.3V X5R-CERM 603
C3916 0.1UF 10% 16V X7R-CERM 402

42 AVDDH, 48 BIASVDDH, 37 XTALVDDH, 17 VDDO, 7 SR_VDD, 20 SR_VDDP, 56 SR_LX, 62 SR_VFB, 14 AVDDL, 15 PCIE_PLLVDDL, 16 GPHY_PLLVDDL, 13 VDDC

ENET_SR_LX 71
ENET_SR_VFB 71

Internal 1.2V Switching Regulator pins.

PP1V2_S3_ENET_INTREG 6 71
???mA (1000base-T, Caesar V)

CRITICAL L3920 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V
C3921 0.1UF 10% 16V X7R-CERM 402
C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3925 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V
C3926 0.1UF 10% 16V X7R-CERM 402
C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL L3930 FERR-600-OHM-0.5A — PP1V2_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=1.2V
C3931 0.1UF 10% 16V X7R-CERM 402
C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402
C3935 10UF 10% 6.3V X5R 805

LR_OUT/GPIO1 is used as a 3.3V/1.8V internal LDO out for the card reader on-chip I/O.
Connect only to U3900 pin 20.

72 71 62 61 57 54 52 51 50 49 23 22 20 19 18 17 16 12 8 7 5 48 46 42 41 40 38 33 28 27 26 85 77 75 74 73 PP3V3_S0

R3942 1K 5% 1/16W MF-LF 402 — Current Limiting Resistor

OMIT
U3900
BCM57765
QFN-8X8

C3950 0.1uF — 81 16 OUT PCIE_ENET_D2R_N
C3951 0.1uF — 81 16 OUT PCIE_ENET_D2R_P
C3955 0.1uF — 81 16 IN PCIE_ENET_R2D_C_P
C3956 0.1uF — 81 16 IN PCIE_ENET_R2D_C_N
R3943 0 5% 1/16W MF-LF 402 — 26 OUT ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested. If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

BCM57765_VMAIN_PRSNT	58	VMAIN_PRSNT (IPD)	
PCIE_ENET_D2R_C_N	27	PCIE_TXD_N	81
PCIE_ENET_D2R_C_P	28	PCIE_TXD_P	81
PCIE_ENET_R2D_P	33	PCIE_RXD_P	81
PCIE_ENET_R2D_N	34	PCIE_RXD_N	81
PCIE_CLK100M_ENET_P	31	PCIE_REFCLK_P	81 16 IN
PCIE_CLK100M_ENET_N	30	PCIE_REFCLK_N	81 16 IN
ENET_RESET_L	11	PERST* (IPD)	82 33 IN
ENET_CLKREQ_L	12	CLKREQ* (OD)	16 OUT
BCM57765_WAKE_R_L	3	WAKE* (OD)	
ENET_LOW_PWR	4	LOW_PWR (IPD)	33 23 19 IN
BCM57765_SMB_CLK	6	SMB_CLK	
BCM57765_SMB_DATA	10	SMD_DATA (IPD)	
BCM57765_SCLK	66	SCLK	37 B1
BCM57765_MISO	64	SI/LINKLED*	37 IN
BCM57765_MOSI	65	SO	37 B1
BCM57765_CS_L	63	CS*	37 B1
TP_BCM57765_SPD100LED_L	2	SPD100LED*/SERIAL_DO (OD)	
TP_BCM57765_TRAFFICLED_L	67	TRAFFICLED*/SERIAL_DI (OD)	8 OUT
SYSCLK_CLK25M_ENET	18	XTALI	81 26 IN
NC	19	XTALO	
BCM57765_RDAC	38	RDAC	

R3965 1.24K 1% 1/16W MF-LF 402

THRM_PAD 69

TRD0_P	40	ENET_MDI_P<0>	B1 38 82
TRD0_N	41	ENET_MDI_N<0>	B1 38 82
TRD1_P	44	ENET_MDI_P<1>	B1 38 82
TRD1_N	43	ENET_MDI_N<1>	B1 38 82
TRD2_P	46	ENET_MDI_P<2>	B1 38 82
TRD2_N	47	ENET_MDI_N<2>	B1 38 82
TRD3_P	50	ENET_MDI_P<3>	B1 38 82
TRD3_N	49	ENET_MDI_N<3>	B1 38 82
GPIO_0	5	NC	
GPIO_1/CR_BUS_PWR	8		(IPD)
RE*/GPIO_2	9	ENET_MEDIA_SENSE	OUT 26
SD_DETECT/WE*	1	ENET_CR_DETECT_L	(IPD) IN 33
CR_CMD/CLE	26	ENET_CR_CMD	(IPU) IN 33 82
CR_CLK/RY_BY*	21	ENET_CR_CLK	OUT 33 82
CR_DATA0	25	ENET_CR_DATA<0>	B1 33 82
CR_DATA1	24	ENET_CR_DATA<1>	B1 33 82
CR_DATA2	23	ENET_CR_DATA<2>	B1 33 82
CR_DATA3	22	ENET_CR_DATA<3>	B1 33 82
CR_DATA4	52	ENET_CR_DATA<4>	B1 33 82
CR_DATA5	53	ENET_CR_DATA<5>	B1 33 82
CR_DATA6	54	ENET_CR_DATA<6>	B1 33 82
CR_DATA7	55	ENET_CR_DATA<7>	B1 33 82
CE*/MS_INS*	59	NC_BCM57765_CE_L_MS_INS_L	NO_TEST=TRUE 8
CR_LED/ALE	60	ENET_CR_PWREN	OUT 33
CR_WP*/XD_WP*	57	SDCONN_WP	IN 33
XD_DETECT	68	BDM57765_SR_DISABLE	R3980 1K 5% 1/16W MF-LF 402

(IPU) GPIO_1/CR_BUS_PWR, RE*/GPIO_2, SD_DETECT/WE*, CR_CMD/CLE, CR_CLK/RY_BY*, CR_DATA0–7, CE*/MS_INS*, CR_LED/ALE, CR_WP*/XD_WP*

NOTE: "IPx" == Programmable pull-up/down

SD_DETECT can only be used active low due to errata.

No MS (Memory Stick) Insert feature needed.
Control signal to light LED or control SD bus power.

ENET 1.2V SR IS ENABLED IF SR_DISABLE is PULLed-DOWN.

ENET_CR Signals

BCM requests SD CR[0:7], CMD, CLK termination.

ENET supports both active-levels for WP.

PP3V3R1V8_ENET_LR_OUT_REG 37
PP3V3R1V8_ENET_LR_OUT_REG 37
MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=3.3V, MAKE_BASE=TRUE
C3970 4.7UF 10% 6.3V X5R-CERM 603
C3971 0.1UF 10% 16V X7R-CERM 402
C3972 0.1UF 10% 16V X7R-CERM 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)

73 71 37 26 7 6 PP3V3_ENET

U3990 AT45DB011D SOIC-8S1 — OMIT
VCC, SCK, CS*, WP*, RESET*, SI, SO, GND
C3990 0.1UF 10% 16V X7R-CERM 402

37 IN BCM57765_SCLK
37 IN BCM57765_CS_L
BCM57765_MOSI IN 37
BCM57765_MISO OUT 37

NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402
R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K91_MLB SYNC_DATE=05/26/2010
PAGE TITLE
ETHERNET PHY (CAESAR IV)

Apple Inc.

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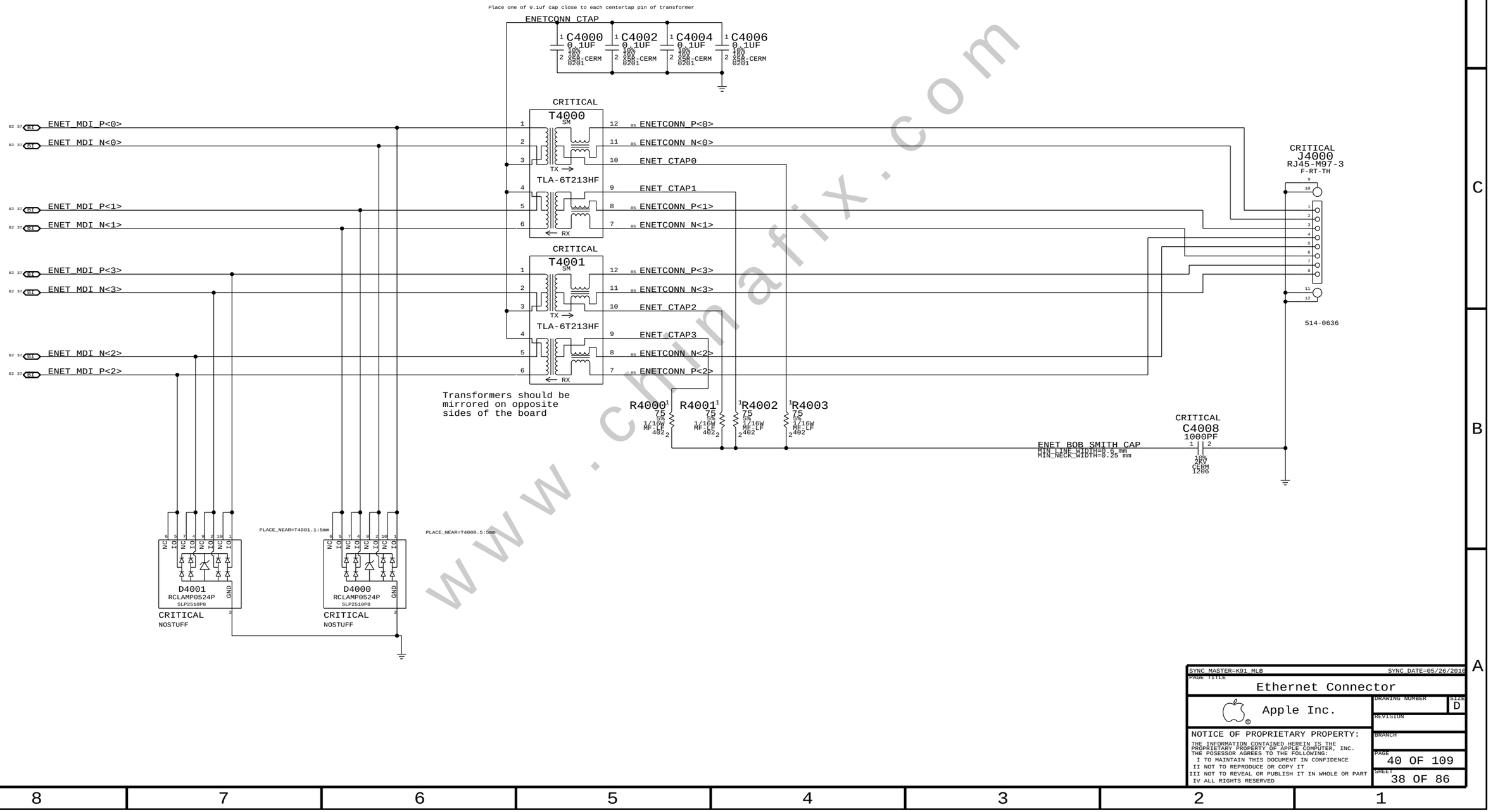
SHEET 37 OF 86

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC_MASTER=K91_MLB SYNC_DATE=05/26/2010

PAGE TITLE

Ethernet Connector

Apple Inc.

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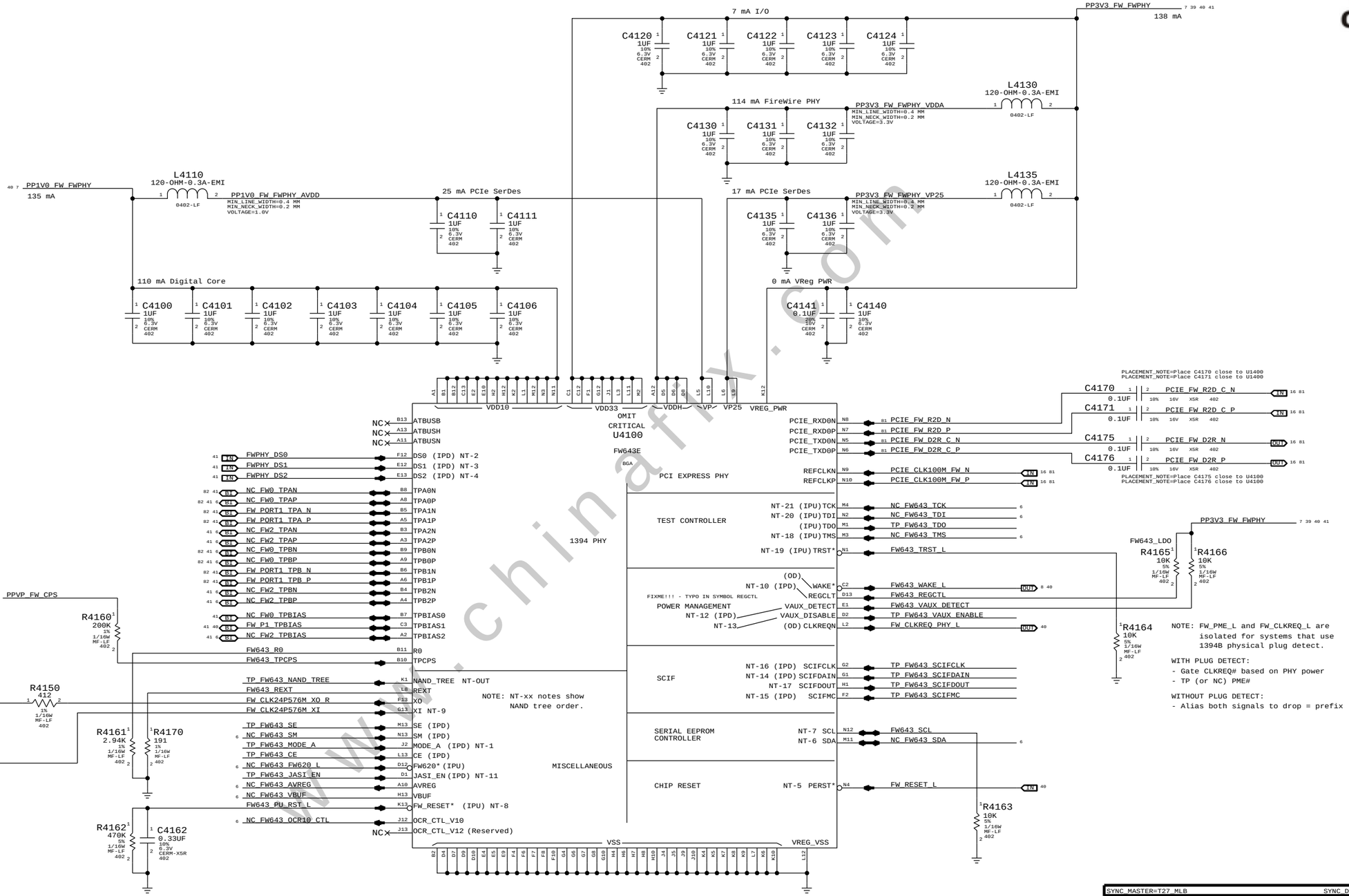

SYNC MASTER=T27_MLB SYNC_DATE=07/20/2005

PAGE TITLE

FireWire LLC/PHY (FW643E)

Apple Inc.

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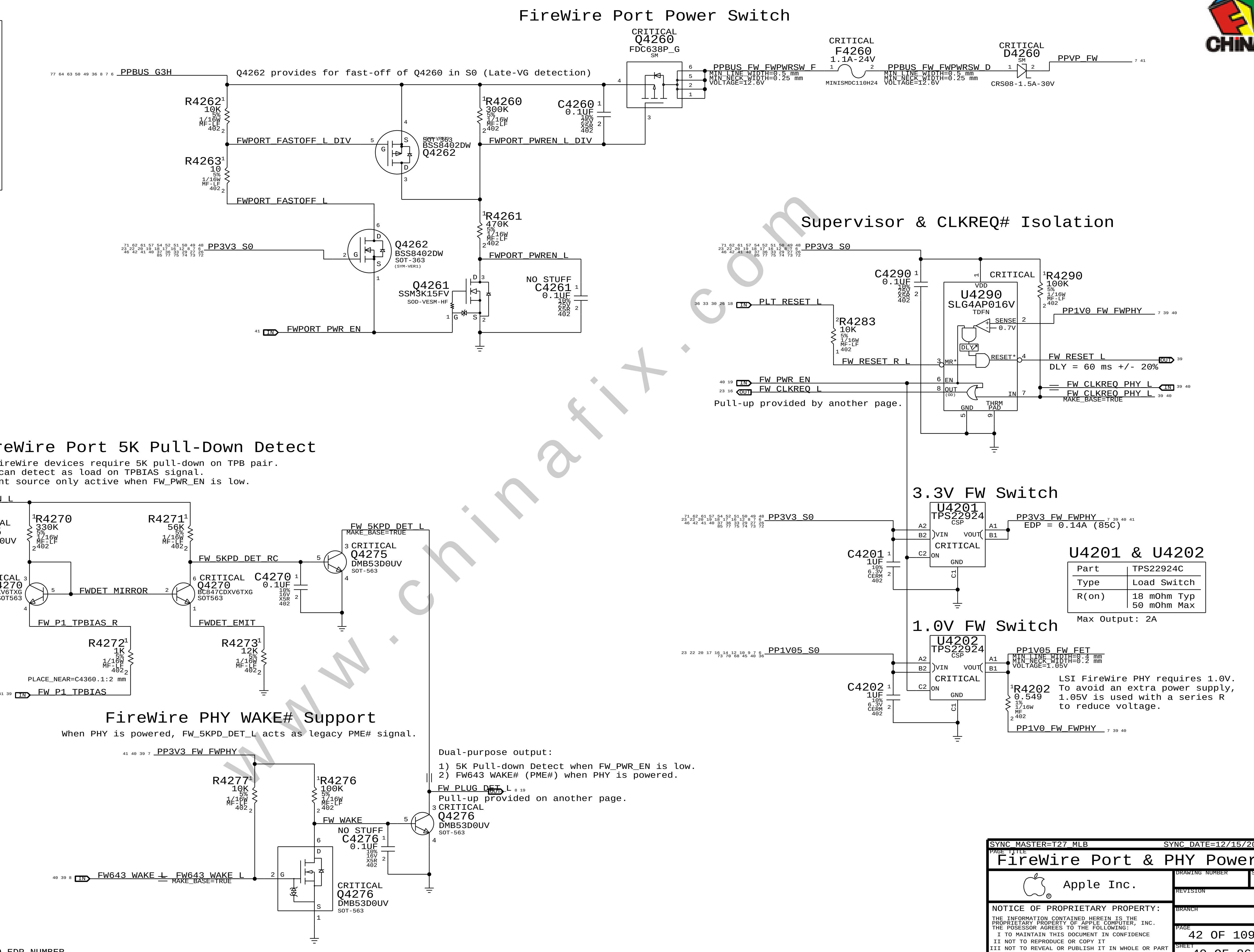
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)



FireWire Port Power Switch
Q4262 provides for fast-off of Q4260 in S0 (Late-VG detection)
CRITICAL Q4260 FDC638P_G
CRITICAL F4260 1.1A-24V
CRITICAL D4260 CRS08-1.5A-30V
PPBUS_G3H
PPBUS_FW_FWPWRSW_F
PPBUS_FW_FWPWRSW_D
PPVP_FW
FWPORT_FASTOFF_L_DIV
FWPORT_FASTOFF_L
FWPORT_PWREN_L_DIV
FWPORT_PWREN_L
FWPORT_PWR_EN
Q4262 BSS8402DW
Q4261 SSM3K15FV
NO STUFF C4261
Supervisor & CLKREQ# Isolation
CRITICAL U4290 SLG4AP016V
PLT_RESET_L
FW_RESET_R_L
FW_RESET_L
DLY = 60 ms +/- 20%
FW_PWR_EN
FW_CLKREQ_L
FW_CLKREQ_PHY_L
Pull-up provided by another page.
FireWire Port 5K Pull-Down Detect
All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.
PP1V05_S0
FW_PWR_EN_L
FWDET_MIRROR
FW_5KPD_DET_RC
FW_5KPD_DET_L
FW_P1_TPBIAS_R
FWDET_EMIT
FW_P1_TPBIAS
PLACE_NEAR=C4360.1:2 mm
3.3V FW Switch
U4201 TPS22924
PP3V3_FW_FWPHY
EDP = 0.14A (85C)
1.0V FW Switch
U4202 TPS22924
PP1V05_FW_FET
PP1V0_FW_FWPHY
LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.
FireWire PHY WAKE# Support
When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.
PP3V3_FW_FWPHY
FW_WAKE
FW643_WAKE_L
Dual-purpose output:
1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.
FW_PLUG_DET_L
Pull-up provided on another page.
CRITICAL Q4276 DMB53D0UV

U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC_MASTER=T27_MLB SYNC_DATE=12/15/2009

PAGE TITLE: FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER — SIZE D

Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

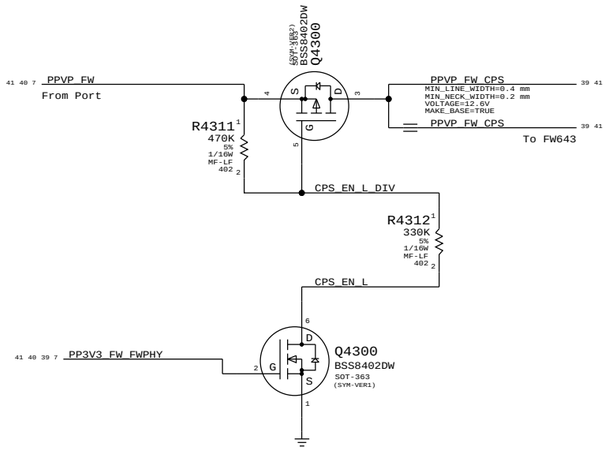
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

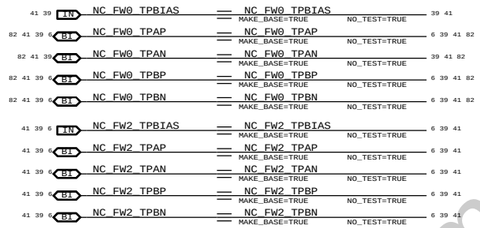
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



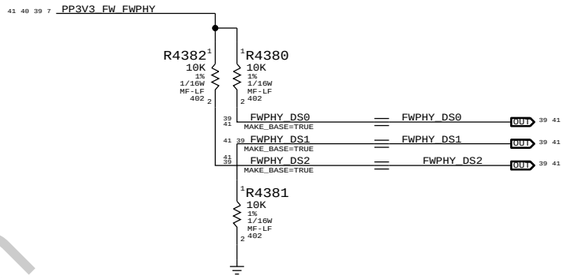
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



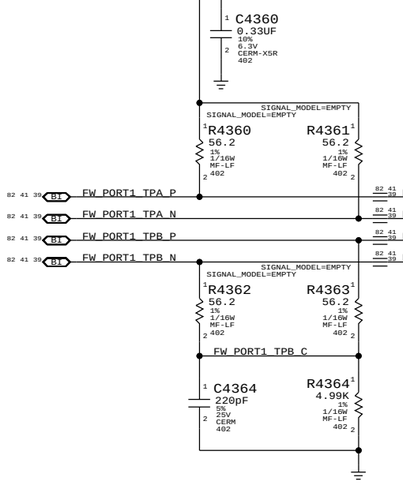
FireWire PHY Config Straps

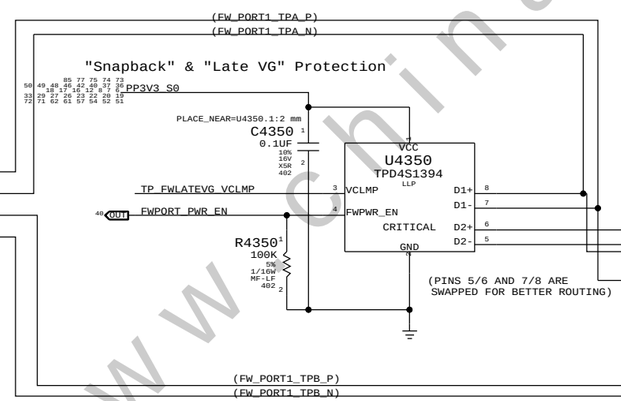
Configures PHY for:
- Port "1" Bilingual (1394B)

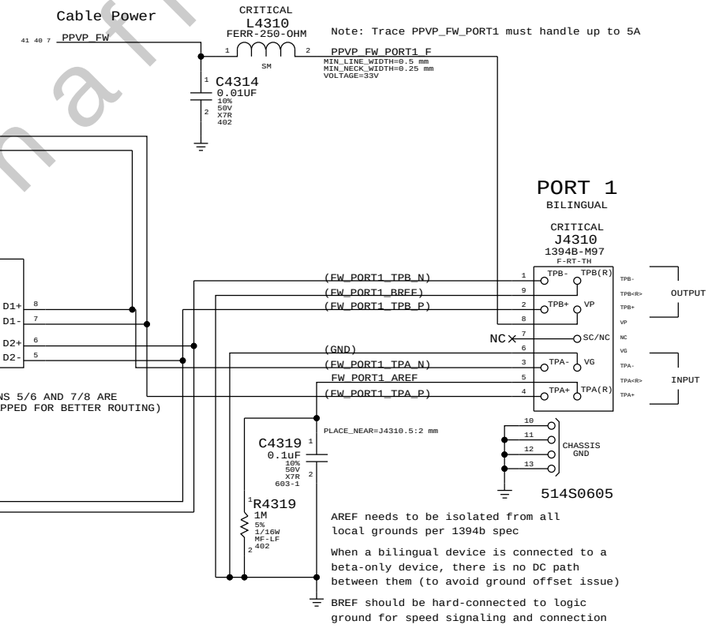


Termination

Place close to FireWire PHY







CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC_MASTER=T27_MLB SYNC_DATE=07/28/2009

PAGE TITLE: FireWire Connector

Apple Inc.

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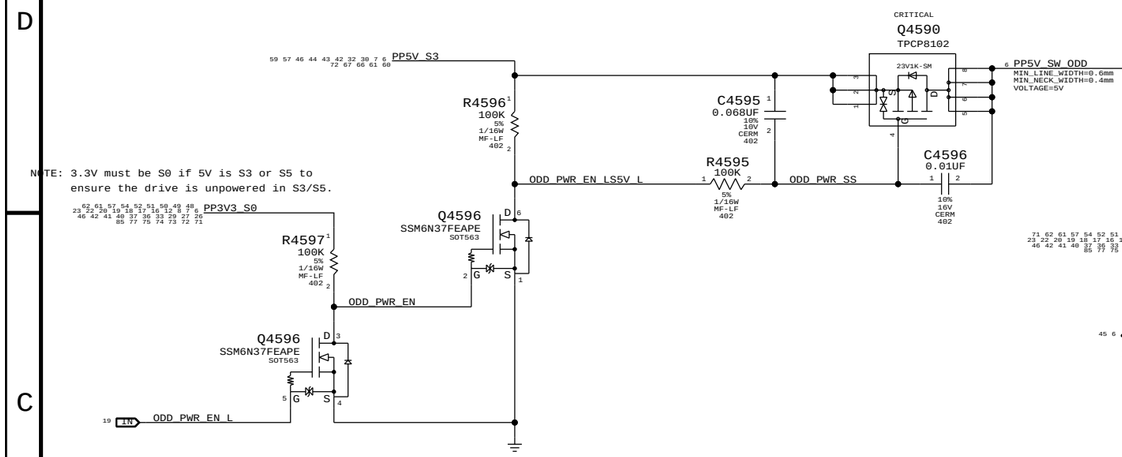
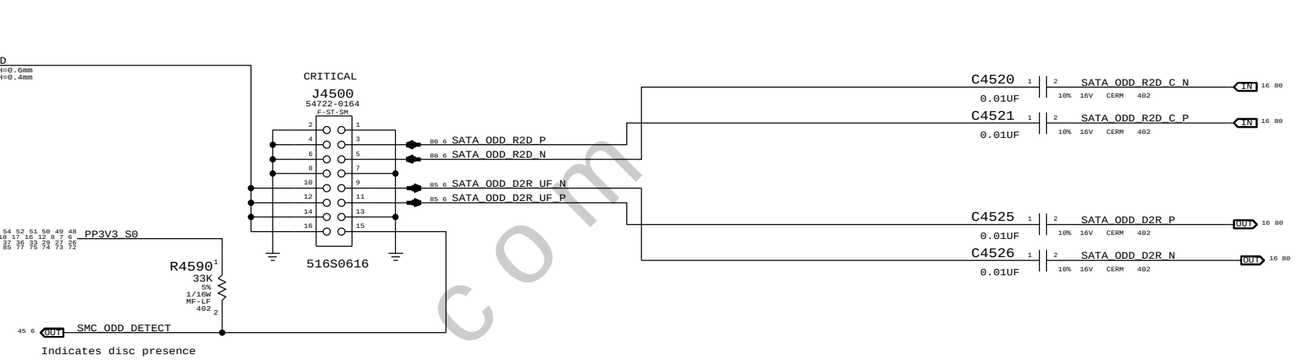
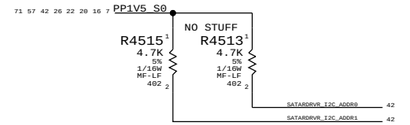
ODD Power Control



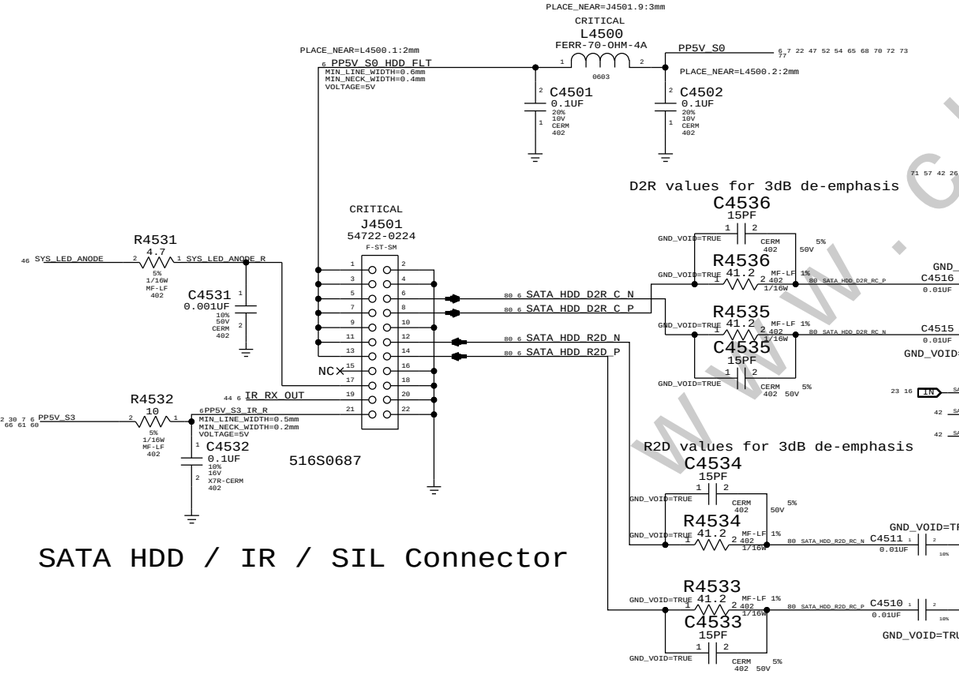
SATA ODD Connector





Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (W/R)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9



SATA HDD / IR / SIL Connector

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

PAGE TITLE: SATA/IR/SIL Connectors

Apple Inc.

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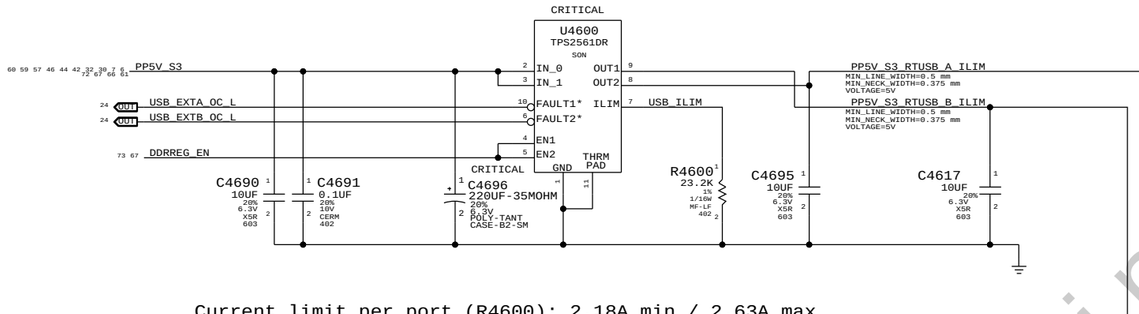
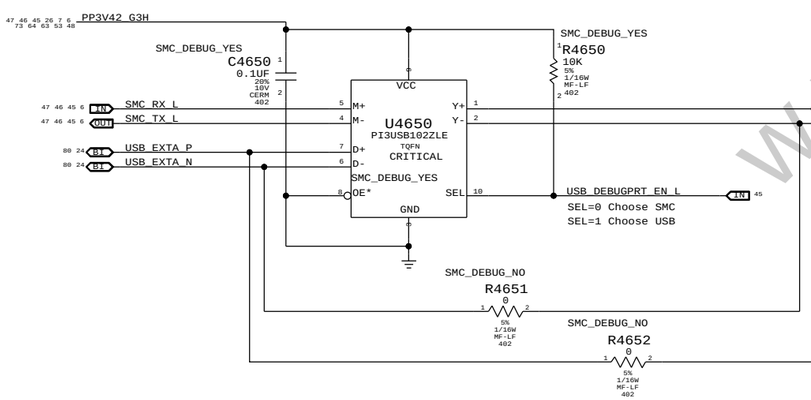
USB Port Power Switch

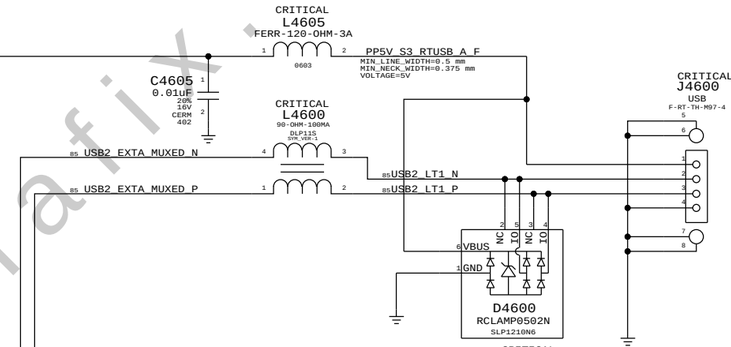


Current limit per port (R4600): 2.18A min / 2.63A max

USB/SMC Debug Mux

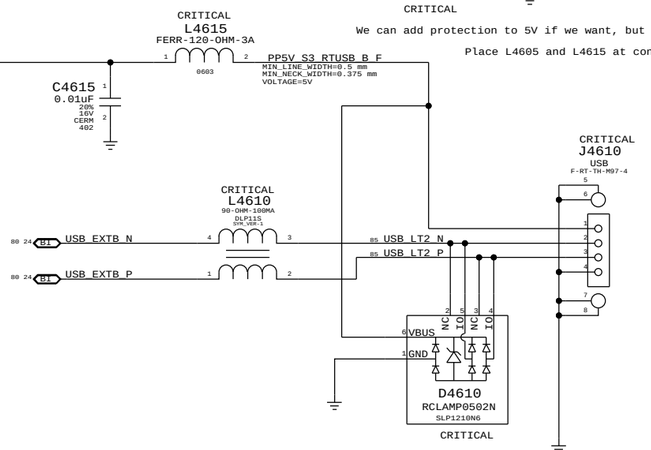


Left USB Port A



We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



Left USB Port B

SYNC_MASTER=K91_MLB SYNC_DATE=06/01/2010

PAGE TITLE: External USB Connectors

Apple Inc.

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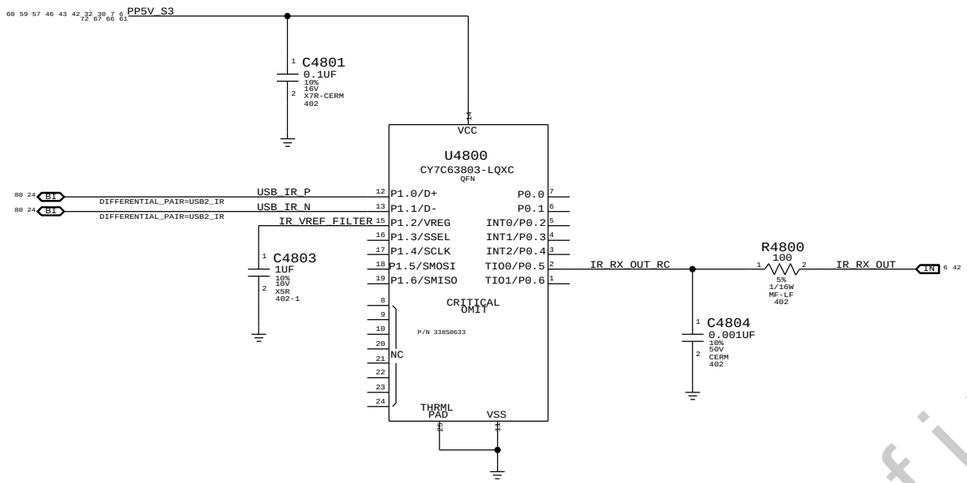
IR SUPPORT



SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

PAGE TITLE: Front Flex Support

Apple Inc.

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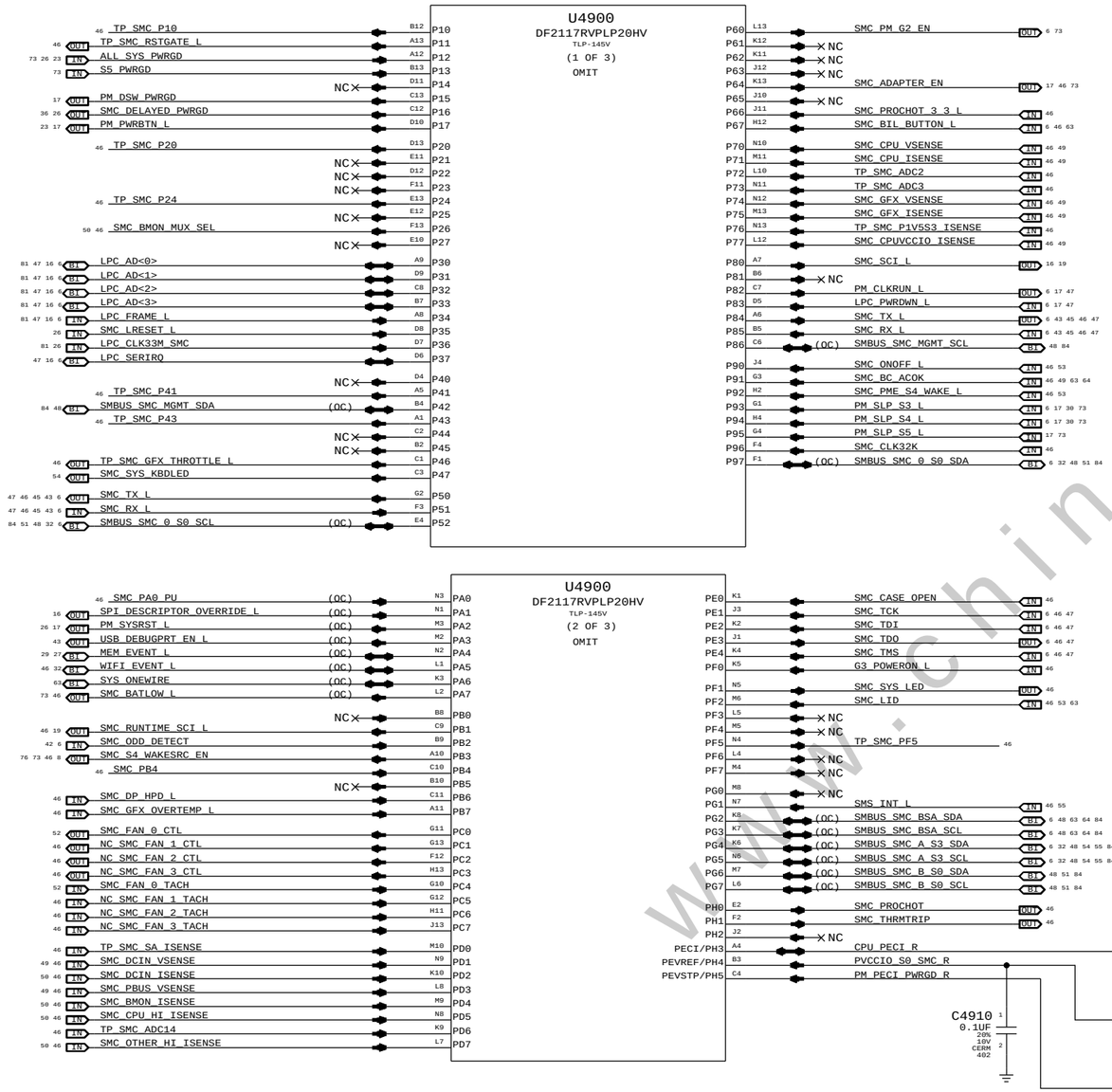
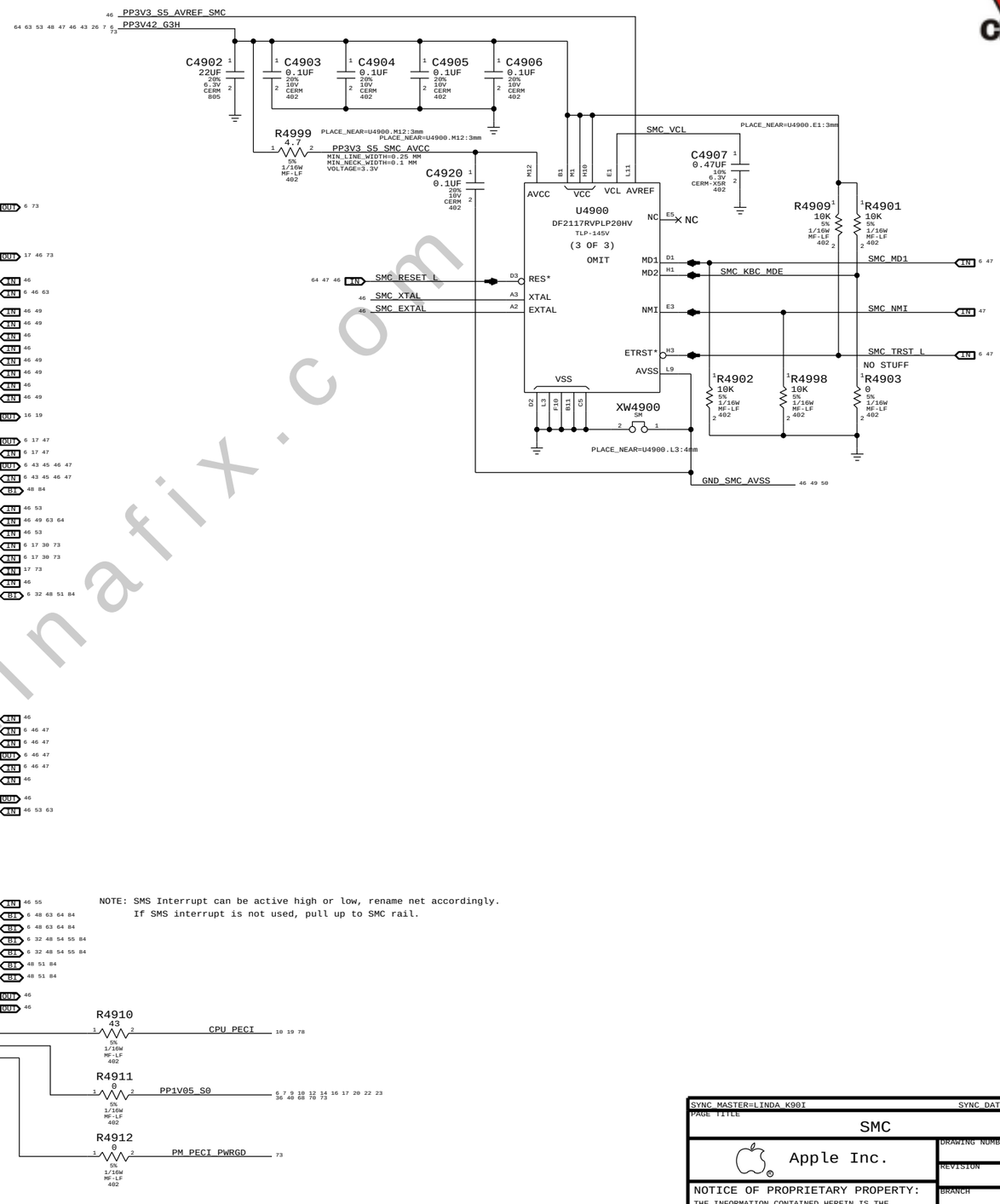
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



SYNC_MASTER=LINDA_K90I SYNC_DATE=07/07/2010

PAGE TITLE: SMC

Apple Inc.

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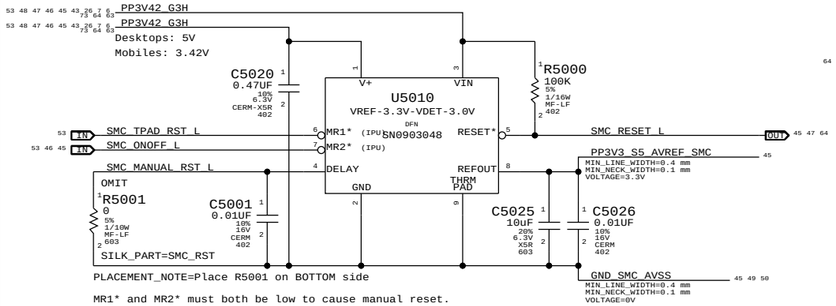
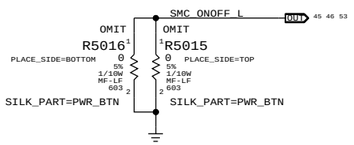
SMC Reset "Button", Supervisor & AVREF Supply



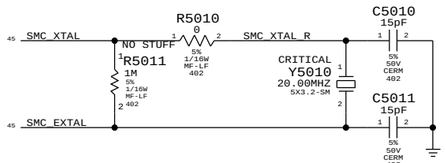
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

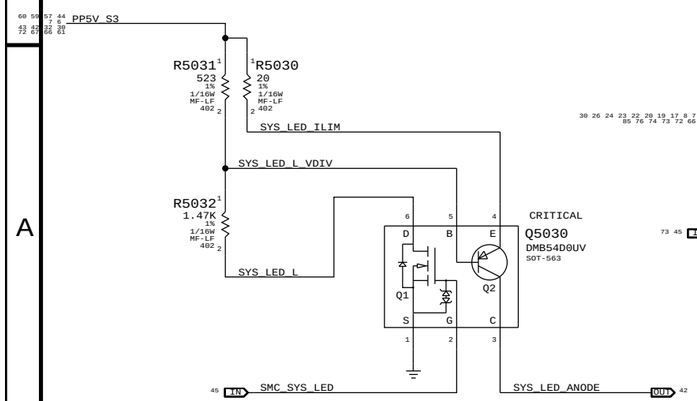
Debug Power "Buttons"



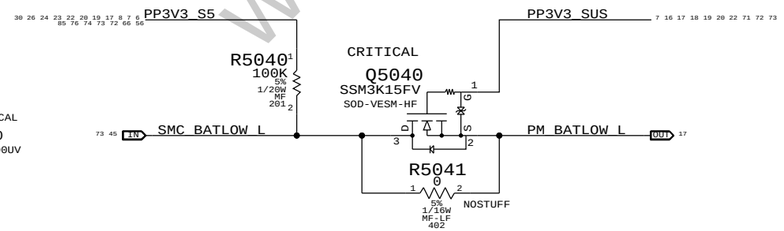
SMC Crystal Circuit



System (Sleep) LED Circuit

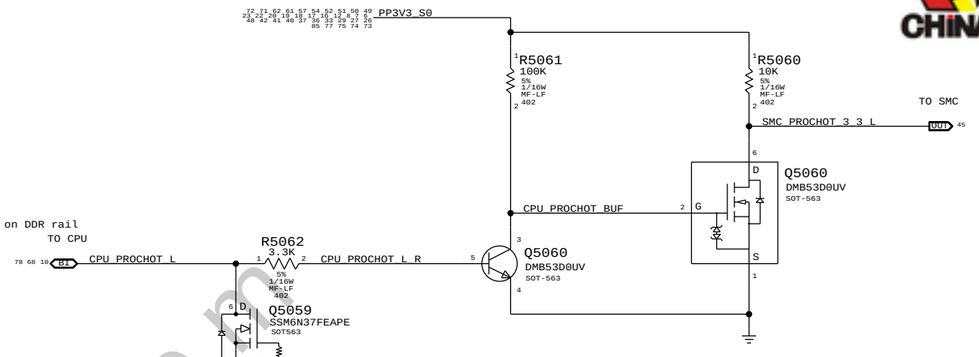


BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

SMC FSB to 3.3V Level Shifting



confirm if K90 needs Isense on DDR rail

Below connections are different from K91

NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE	45 46
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE	45 46
TP_SMC_ADC2	TP_SMC_ADC2	MAKE_BASE=TRUE	45 46
TP_SMC_ADC3	TP_SMC_ADC3	MAKE_BASE=TRUE	45 46
TP_SMC_ADC14	TP_SMC_ADC14	MAKE_BASE=TRUE	45 46
TP_SMC_GFX_THROTTLE_L	TP_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	45 46

PP3V42_G3H
SMC_GFX_OVERTEMP_L — R5095 10K 5% 1/16W MF-LF 402

NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE	45 46
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE	45 46
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE	45 46
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE	45 46
SMC_BC_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE	45 46 49 63 64
SMS_INT_L	SMS_INT_L	MAKE_BASE=TRUE	45 46 55
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE	45 46 49
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE	45 46 49
SMC_GFX_VSENSE	SMC_GFX_VSENSE	MAKE_BASE=TRUE	45 46 49
SMC_GFX_ISENSE	SMC_GFX_ISENSE	MAKE_BASE=TRUE	45 46 49
TP_SMC_P1V5S3_ISENSE	TP_SMC_P1V5S3_ISENSE	MAKE_BASE=TRUE	45 46
SMC_CPUVCCIO_ISENSE	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE	45 46 49
TP_SMC_SA_ISENSE	TP_SMC_SA_ISENSE	MAKE_BASE=TRUE	45 46
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE	45 46 49
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE	45 46 50
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE	45 46 49
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE	45 46 50
SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	45 46 50
SMC_OTHER_HI_ISENSE	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE	45 46 50
TP_SMC_P10	TP_SMC_P10	MAKE_BASE=TRUE	45 46
TP_SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE	45 46
TP_SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	45 46
SMC_BMON_MUX_SEL	SMC_BMON_MUX_SEL	MAKE_BASE=TRUE	45 46 50
TP_SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	45 46
TP_SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE	45 46
TP_SMC_PF5	TP_SMC_PF5	MAKE_BASE=TRUE	45 46
TP_SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	45 46

PM_CLK32K_SUSCLK_R — PLACE_NEAR=U1800.N14:5.1mm — R5012 22 5% 1/16W MF-LF 402 — SMC_CLK32K

PP3V3_S4 — R5020 100K 5% 1/16W MF-LF 402 — SMC_DP_HPD_L
Q5020 SSM3K15FV SOD-VESM-HF
DP_A_EXT_HPD

PP3V3_S4 — R5076 100K 5% 1/16W MF-LF 402 — SMC_PME_S4_WAKE_L — SMC_PME_S4_WAKE_L MAKE_BASE=TRUE

PP3V42_G3H

SMC_ONOFF_L	R5070	10K	5% 1/16W MF-LF 402
G3_POWERON_L	R5072	10K	5% 1/16W MF-LF 402
SMC_LID	R5071	100K	5% 1/16W MF-LF 402
SMC_TX_L	R5073	10K	5% 1/16W MF-LF 402
SMC_RX_L	R5074	100K	5% 1/16W MF-LF 402
SMC_TMS	R5077	10K	5% 1/16W MF-LF 402
SMC_TDO	R5078	10K	5% 1/16W MF-LF 402
SMC_TDI	R5079	10K	5% 1/16W MF-LF 402
SMC_TCK	R5080	10K	5% 1/16W MF-LF 402
SMC_BIL_BUTTON_L	R5081	10K	5% 1/16W MF-LF 402
SMC_BC_ACOK	R5087	470K	5% 1/16W MF-LF 402
SMS_INT_L	R5093	10K	NOSTUFF 5% 1/16W MF-LF 402
SMC_PA0_PU	R5091	100K	5% 1/16W MF-LF 402
SMC_RUNTIME_SCI_L	R5094	100K	NOSTUFF 5% 1/16W MF-LF 402
SMC_ADAPTER_EN	R5085	10K	5% 1/16W MF-LF 402
SMC_CASE_OPEN	R5086	10K	5% 1/16W MF-LF 402
SMC_PB4	R5088	10K	5% 1/16W MF-LF 402
SMC_S4_WAKESRC_EN	R5090	100K	5% 1/16W MF-LF 402

PP3V3_WLAN

WIFI_EVENT_L	R5089	10K	5% 1/16W MF-LF 402

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/08/2010

PAGE TITLE: SMC Support

Apple Inc.

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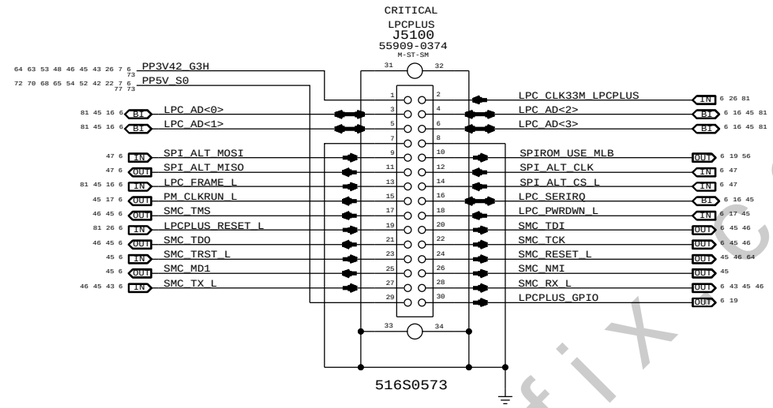
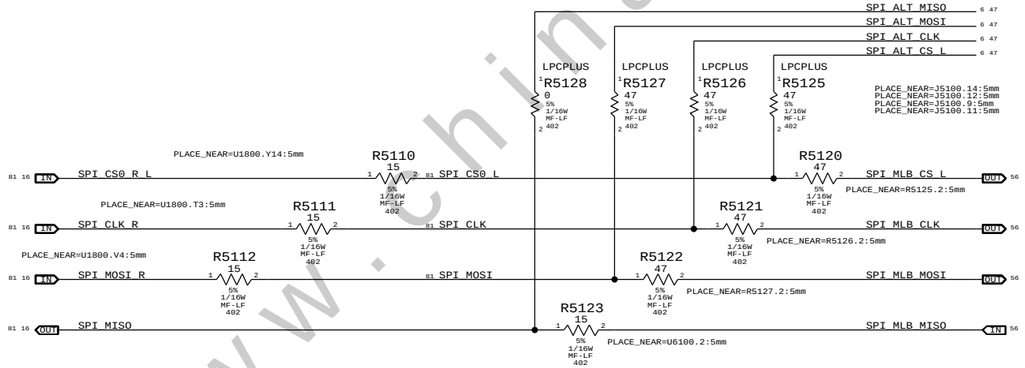
LPC+SPI Connector



SPI Bus Series Termination



SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

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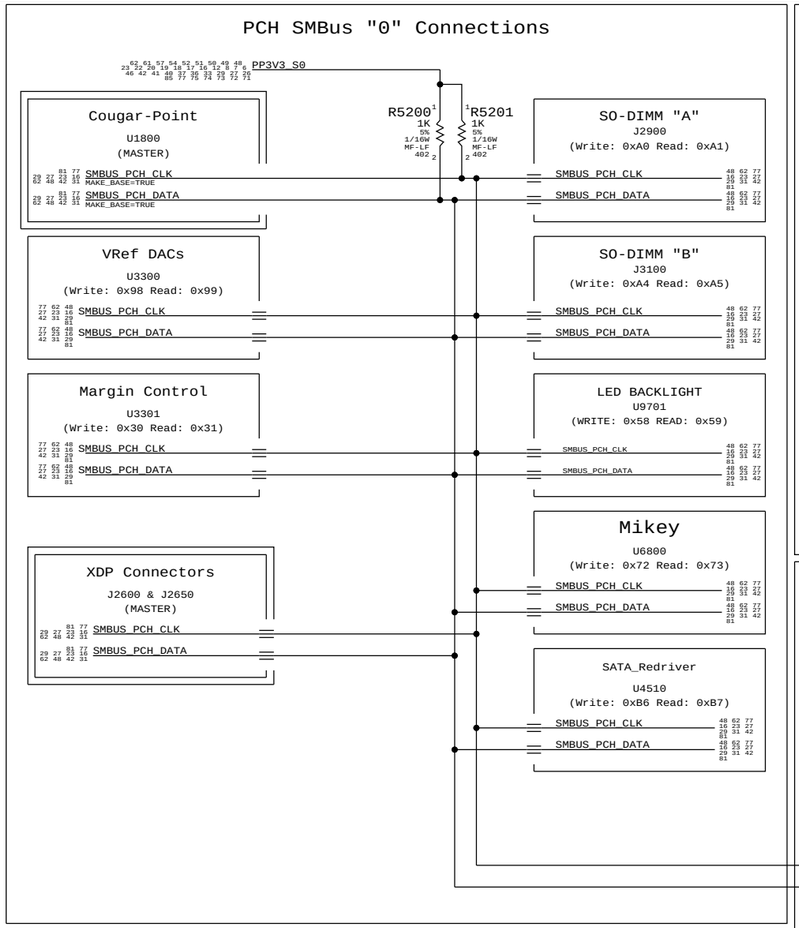

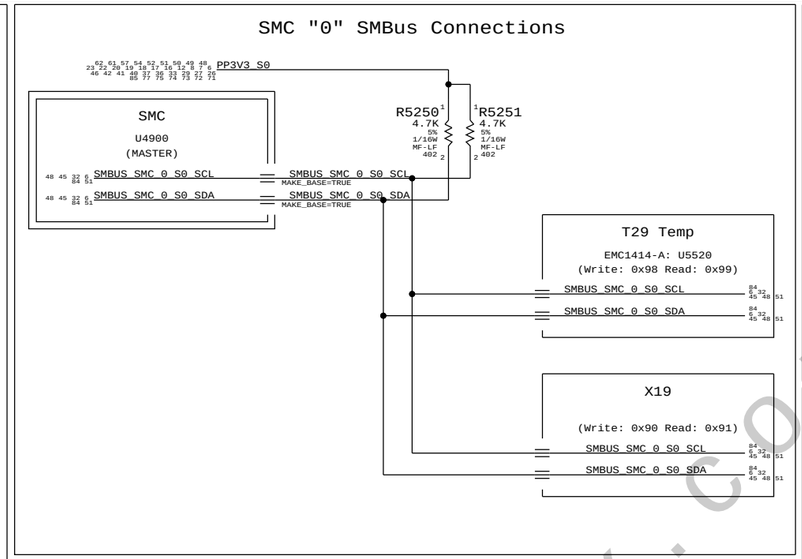

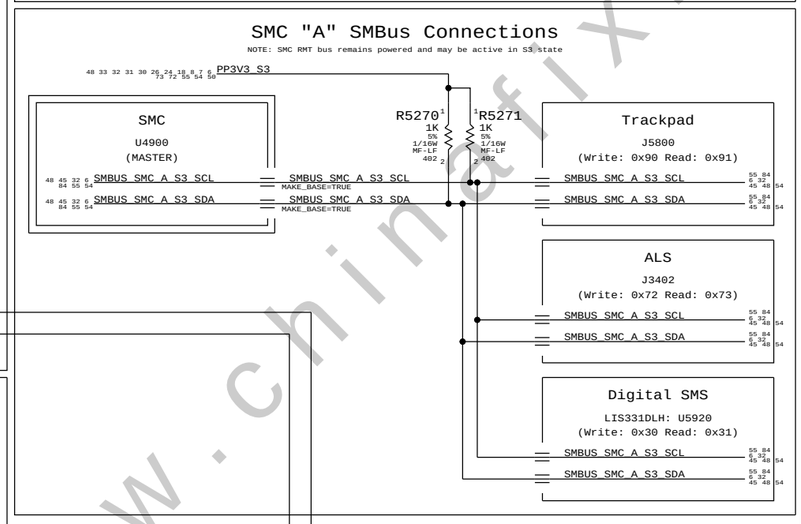

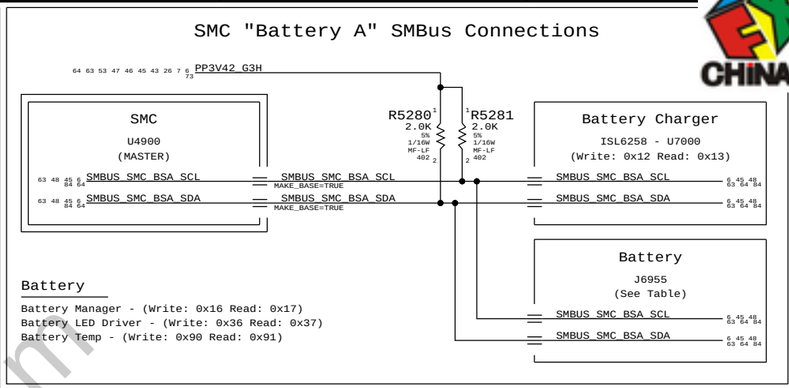

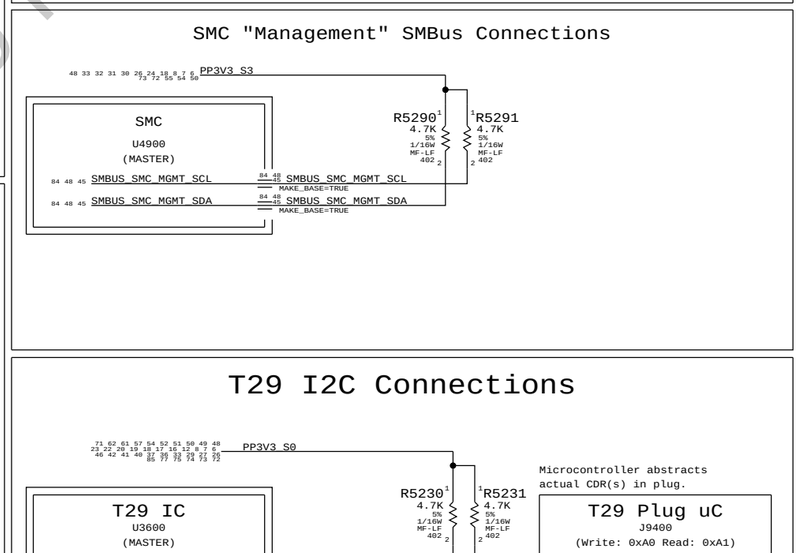

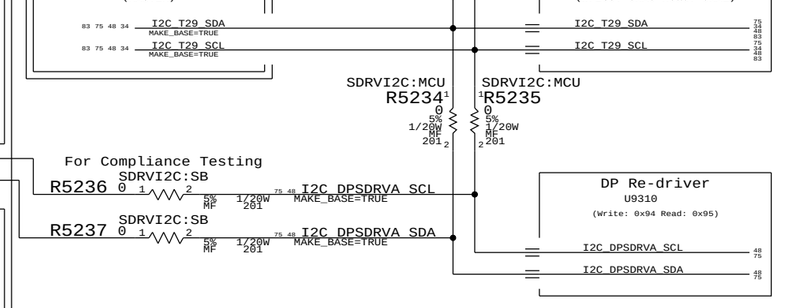

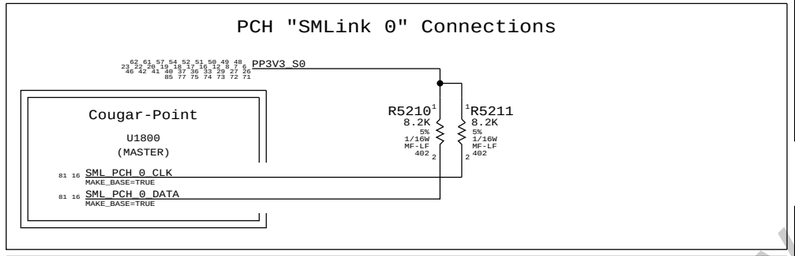

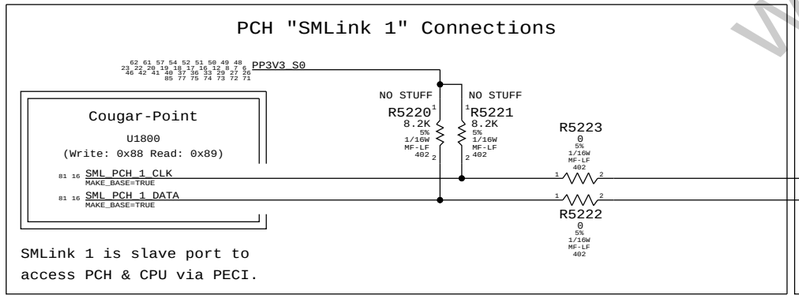

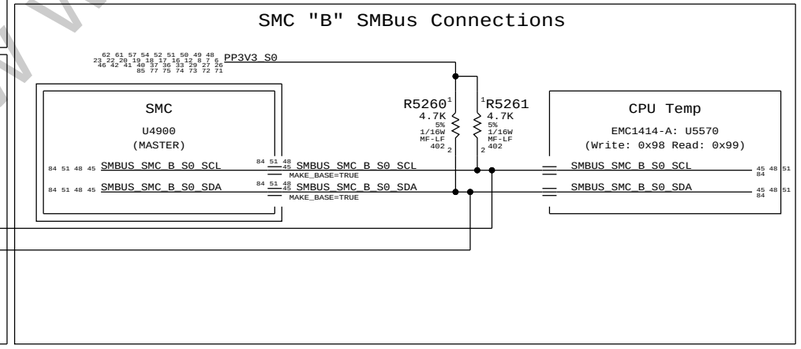

SYNC_MASTER=K91_MLB SYNC_DATE=05/26/2010

PAGE TITLE
SMBus Connections

Apple Inc.

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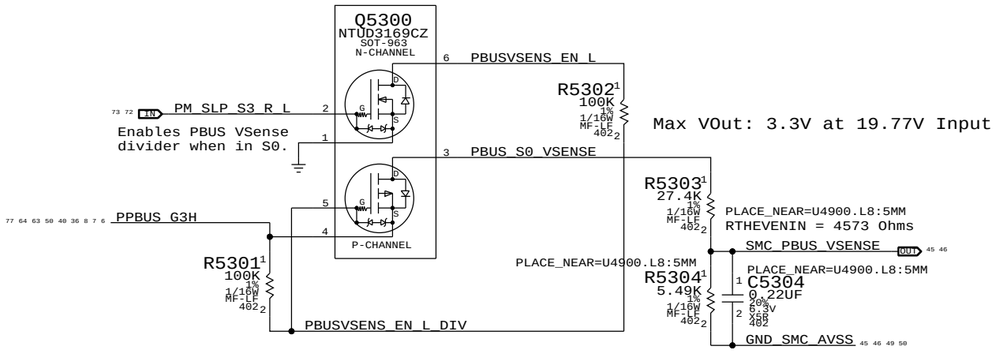
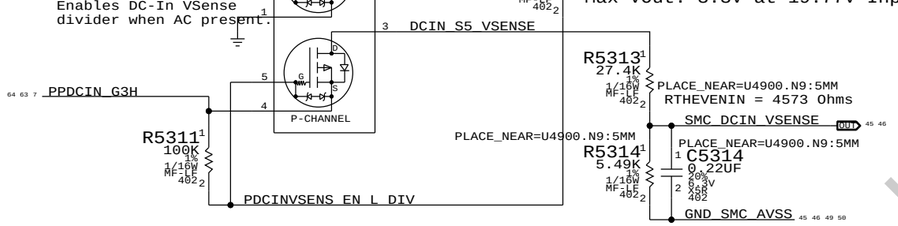
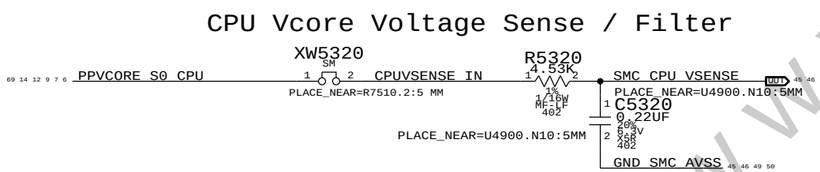
PBUS Voltage Sense Enable & Filter



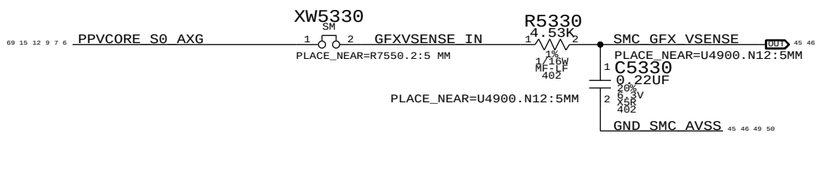
DC-In Voltage Sense Enable & Filter



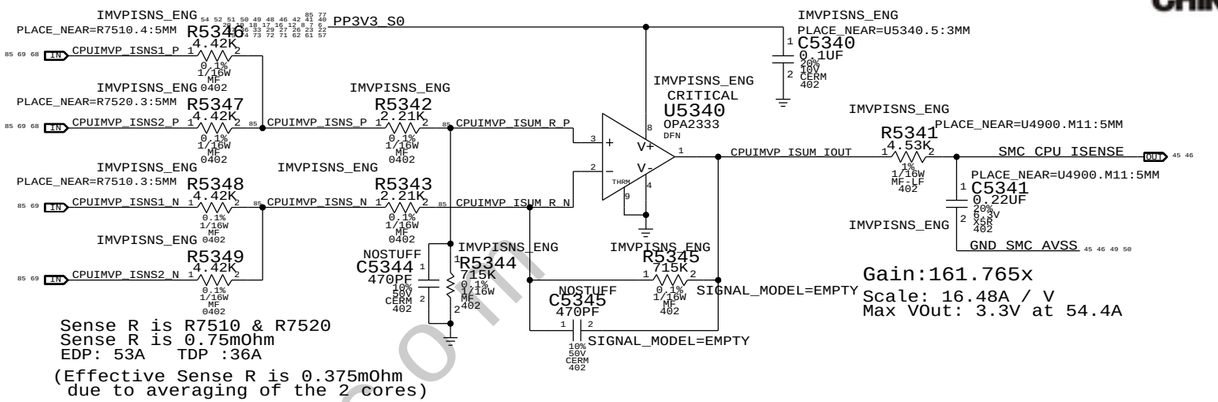
CPU Vcore Voltage Sense / Filter



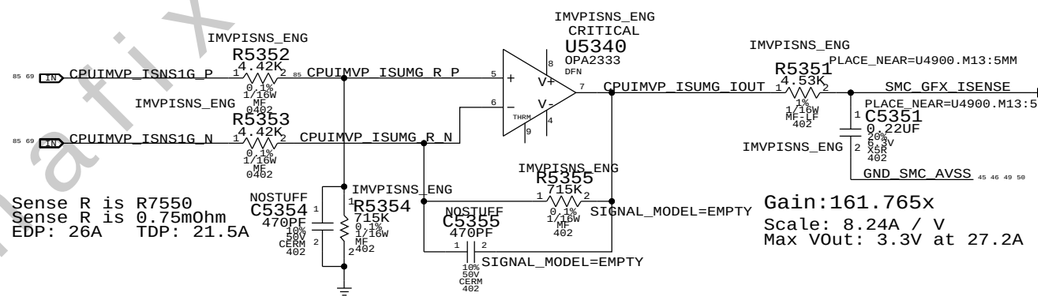
GFX/IG Vcore Voltage Sense / Filter



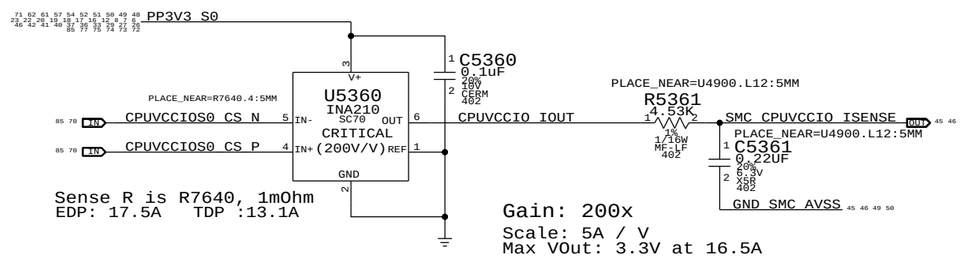
CPU VCore Load Side Current Sense / Filter



GFX/IG VCore Load Side Current Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter



SYNC_MASTER=LINDA K90I SYNC_DATE=10/22/2010

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

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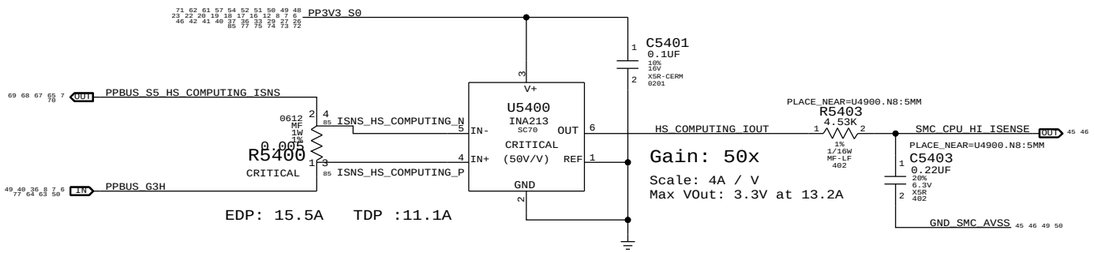
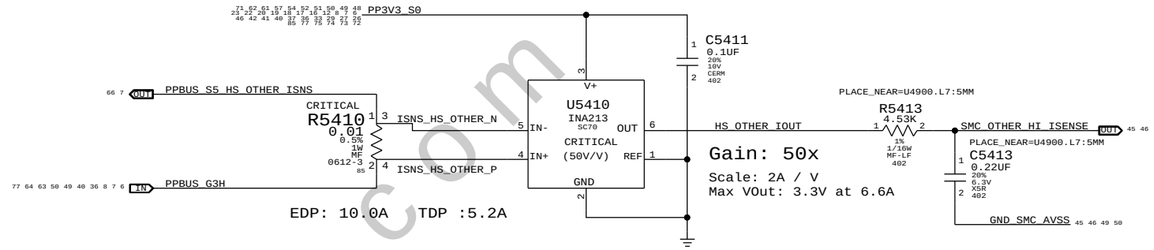
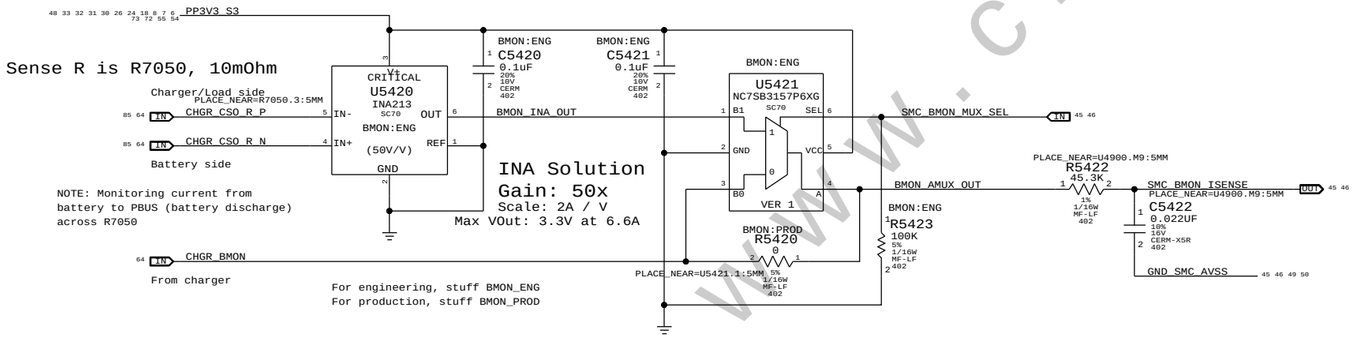
COMPUTING High Side Current Sense / Filter



OTHER High Side Current Sense / Filter



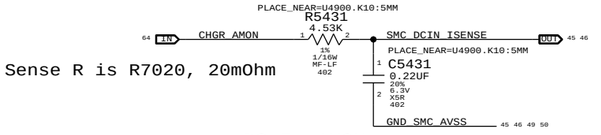
CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter



INA (Engineering) Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A

DC-IN (AMON) Current Sense Filter



Sense R is R7020, 20mOhm

DC-In AMON
ISL6259 Gain: 20x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

SYNC_MASTER=LINDA_K90I SYNC_DATE=10/22/2010

PAGE TITLE: High Side Current Sensing

Apple Inc.

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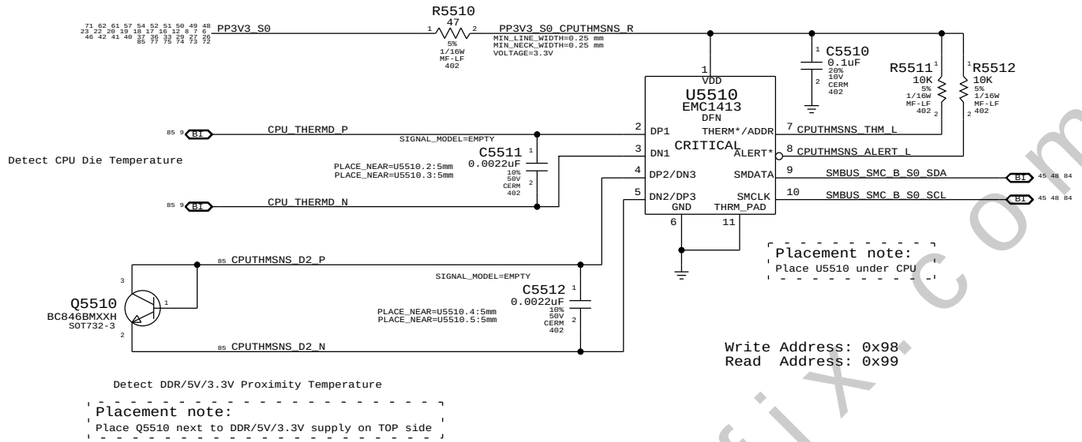
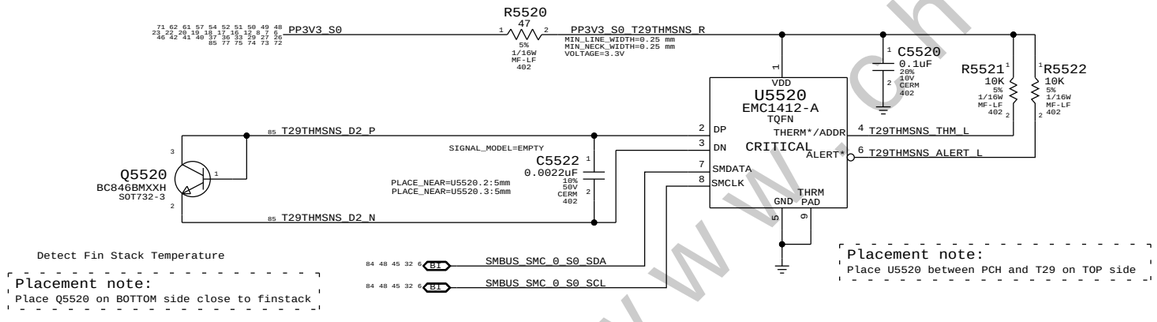
CPU Proximity/CPU Die/5V-3.3V Proximity



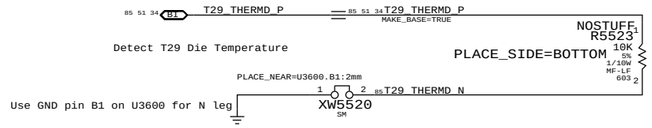
Write Address: 0x98
Read Address: 0x99

PCH-T29 Proximity/FinStack



Write Address: 0x98
Read Address: 0x99

T29 Die



SYNC_MASTER=LINDA_K90I SYNC_DATE=10/22/2010

PAGE TITLE: Thermal Sensors

Apple Inc.

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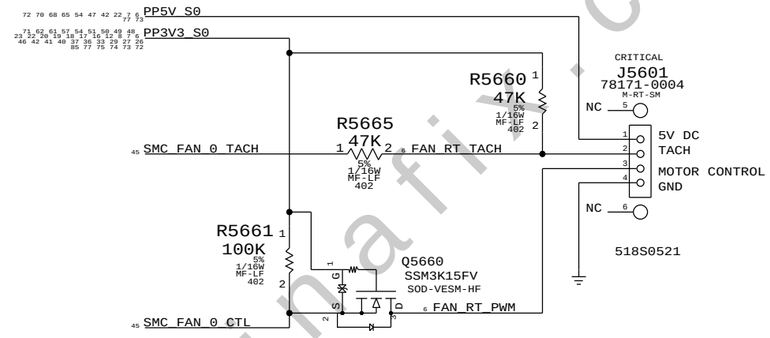

SYNC_MASTER=K24_MLB SYNC_DATE=07/20/2009

PAGE TITLE

Fan

Apple Inc.

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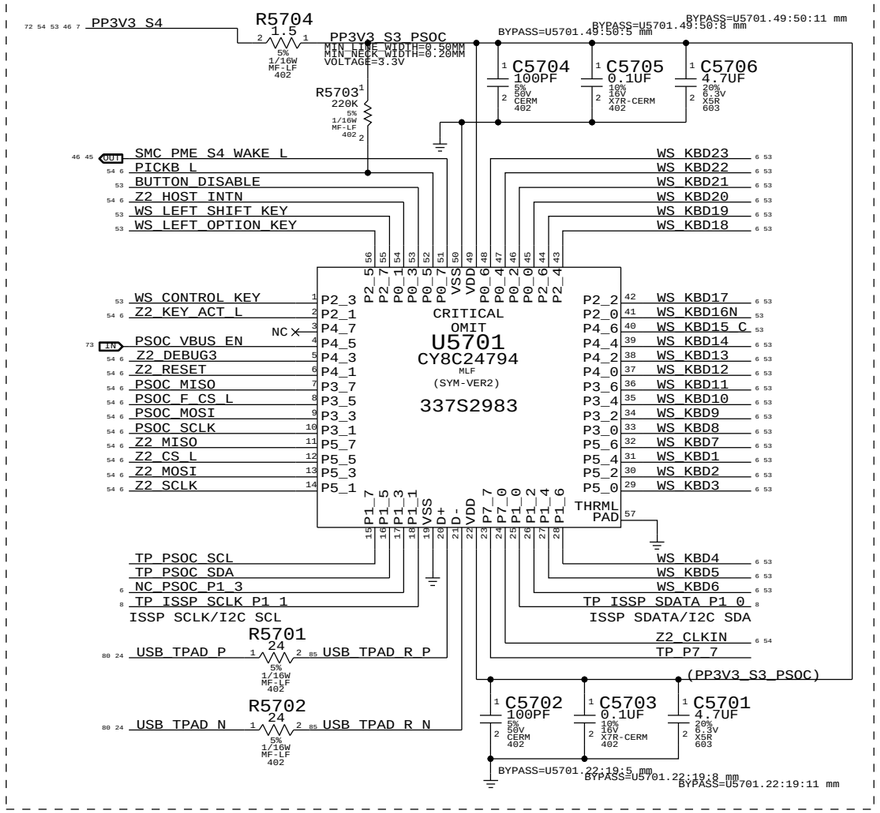
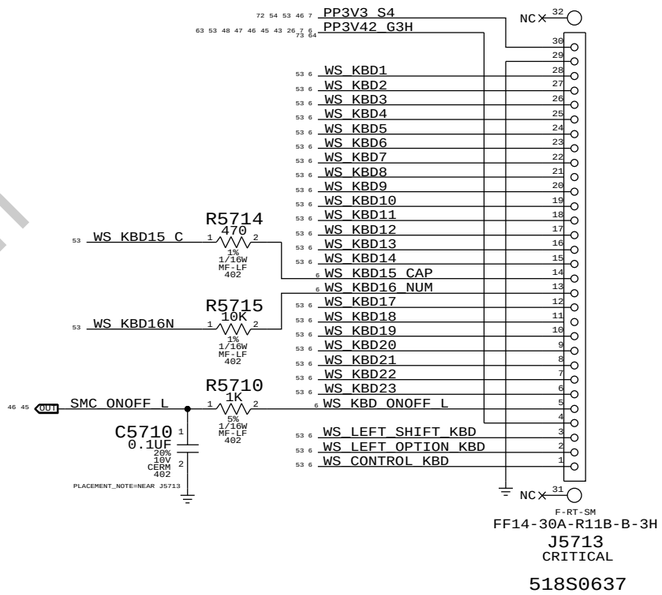
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



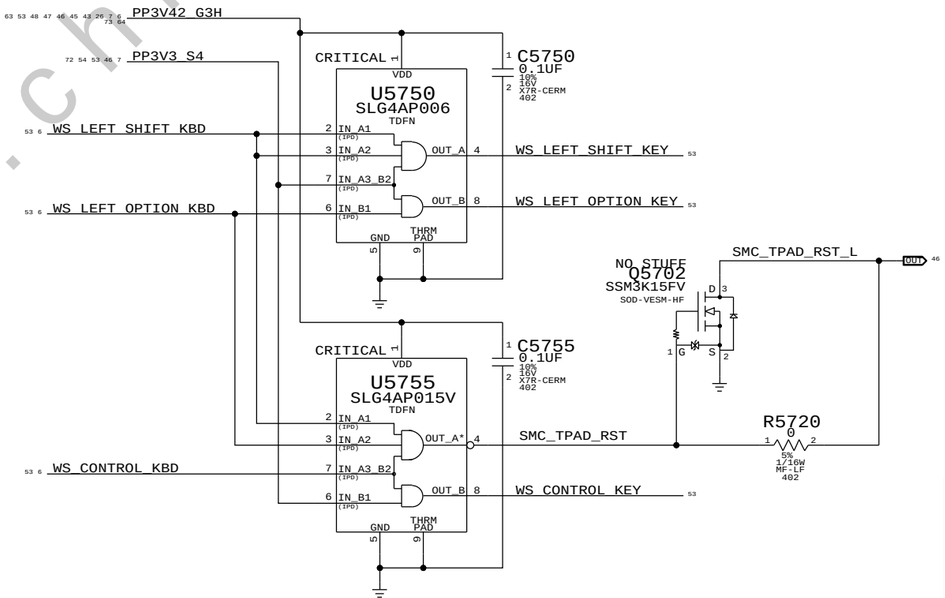
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

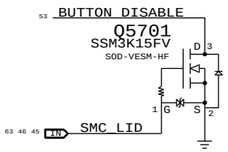


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/12/2010

PAGE TITLE: WELLSPRING 1

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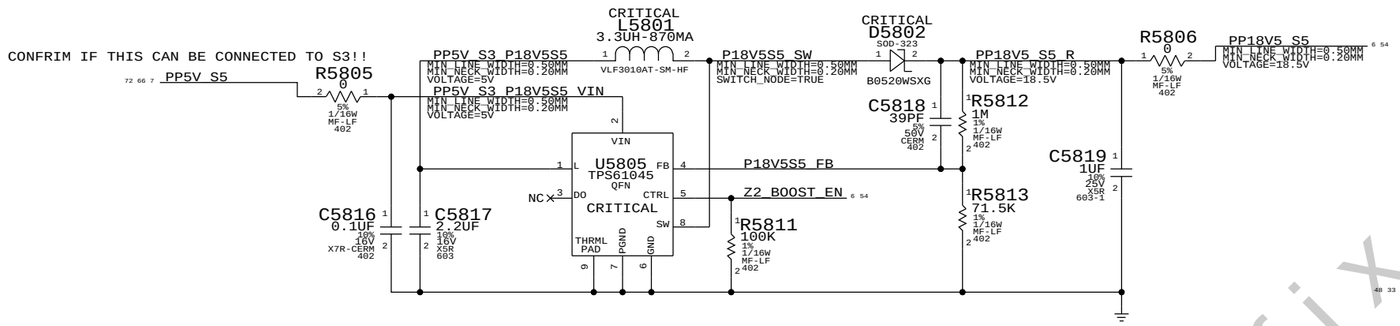
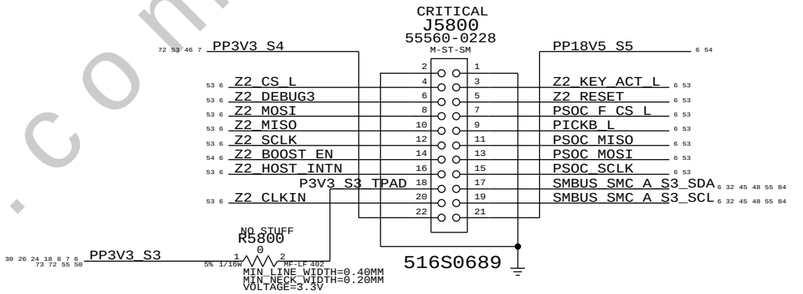
BOOSTER +18.5VDC FOR SENSORS

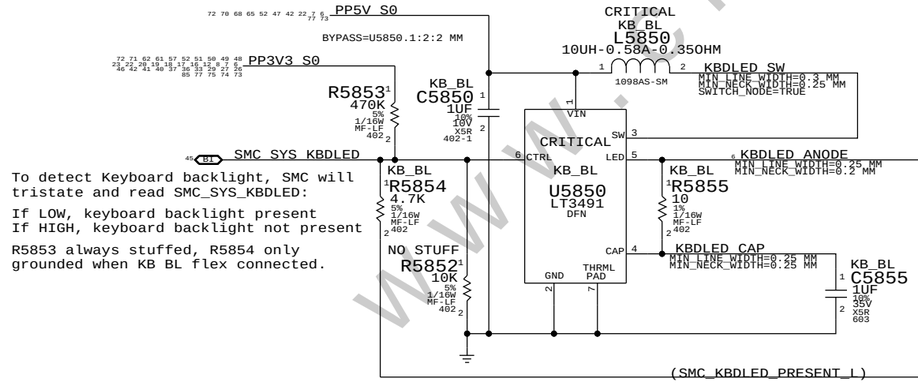
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

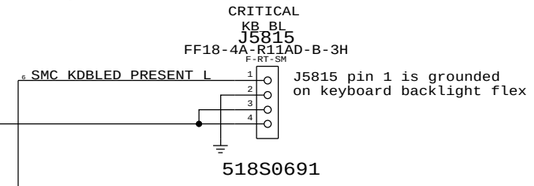


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/12/2010

PAGE TITLE: WELLSPRING 2

Apple Inc.

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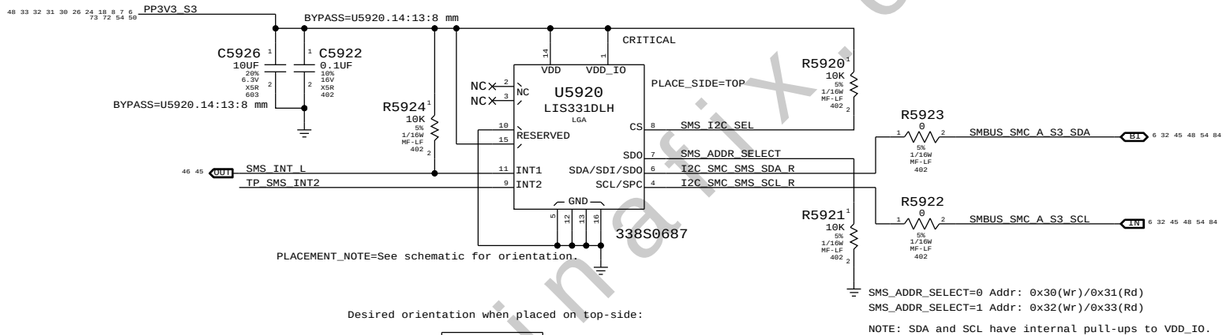
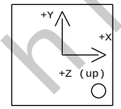


PLACEMENT_NOTE=See schematic for orientation.

Desired orientation when placed on top-side:



Front of system

Circle indicates pin 1 location when placed in correct orientation

SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/08/2010

PAGE TITLE: Digital Accelerometer

Apple Inc.

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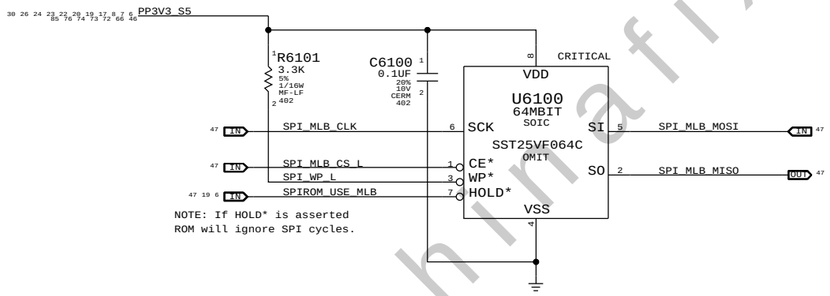

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

PAGE TITLE

SPI ROM

Apple Inc.

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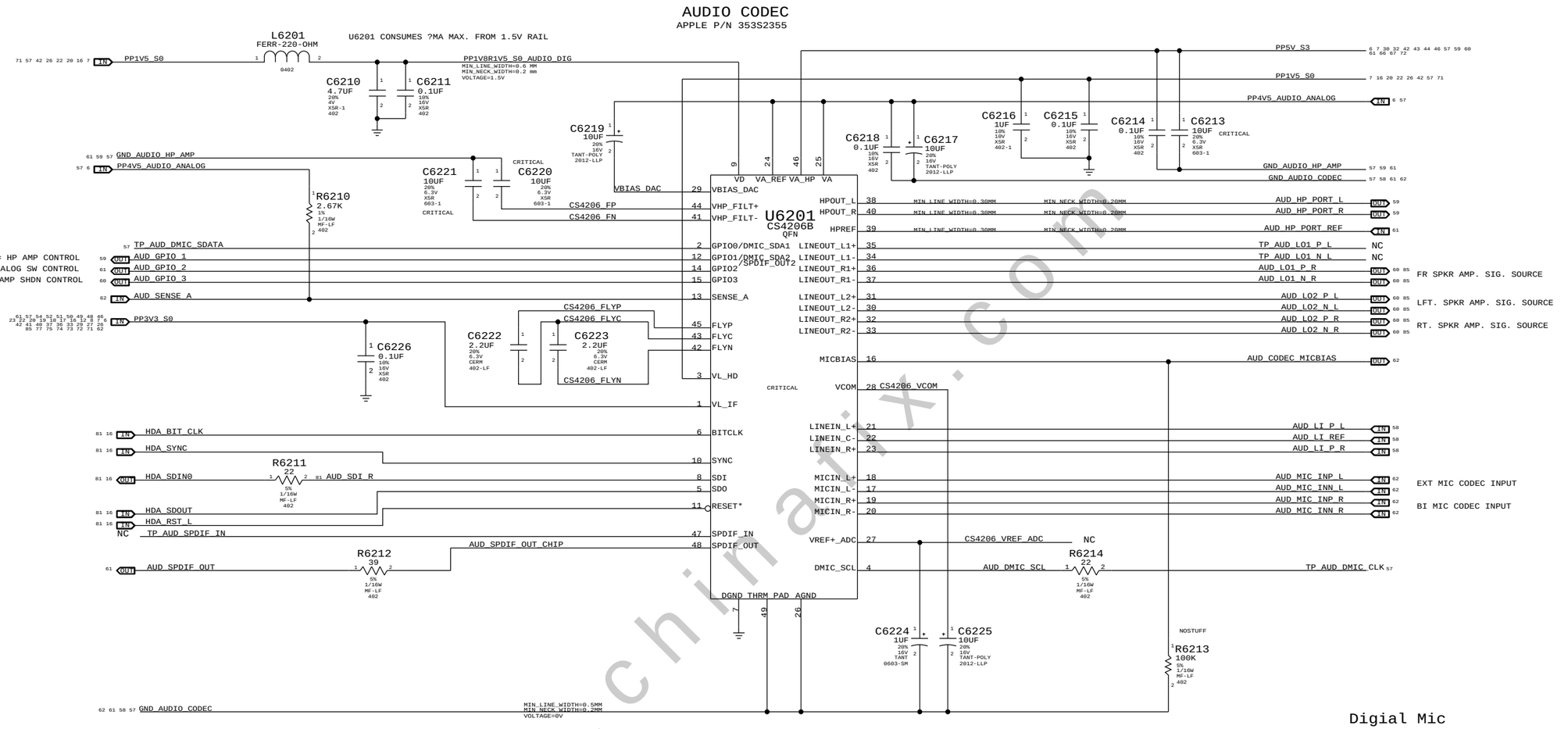
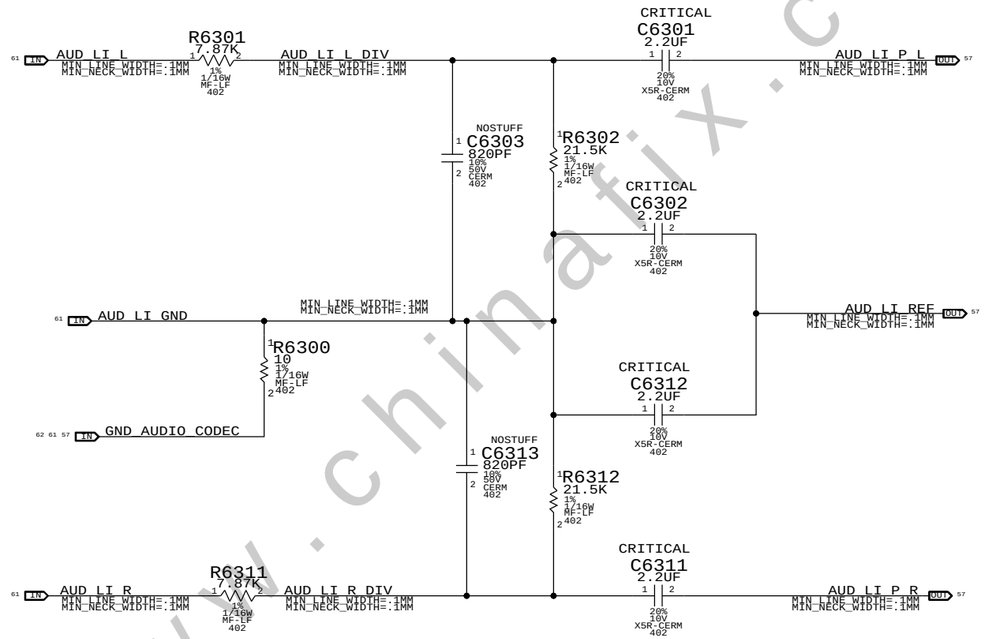


LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

Apple Inc.

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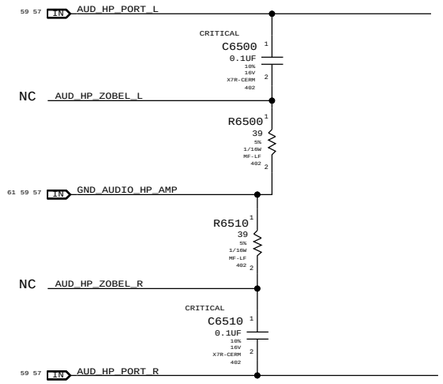
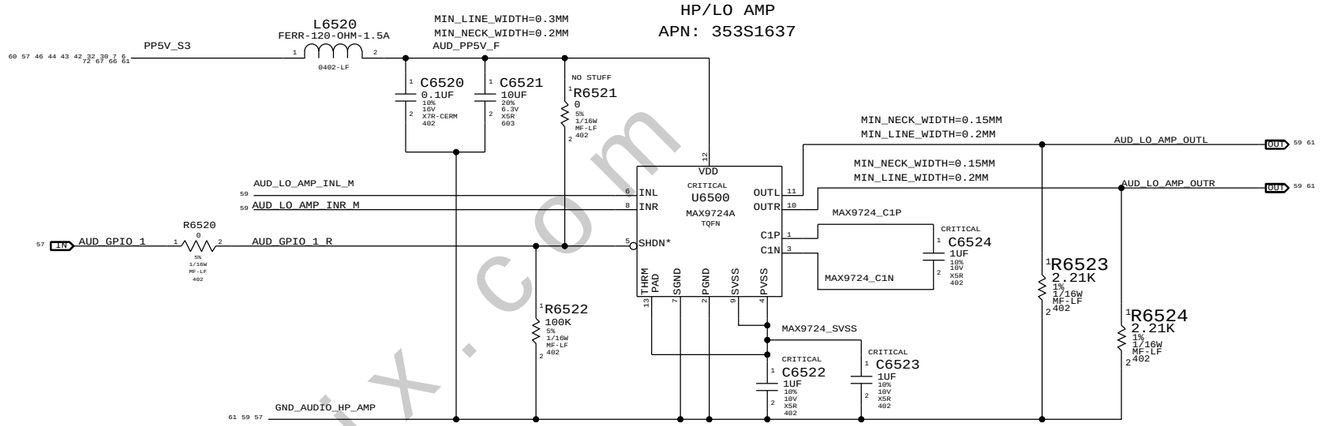
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



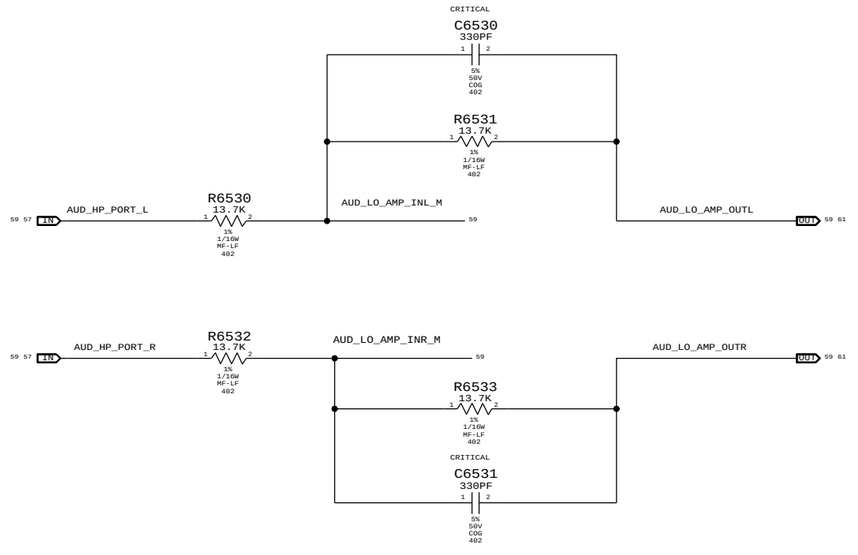
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

HP/LO AMP
APN: 353S1637



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC_MASTER=LENG_K90I SYNC_DATE=08/10/2010

PAGE TITLE

AUDIO: HEADPHONE FILTER

Apple Inc.

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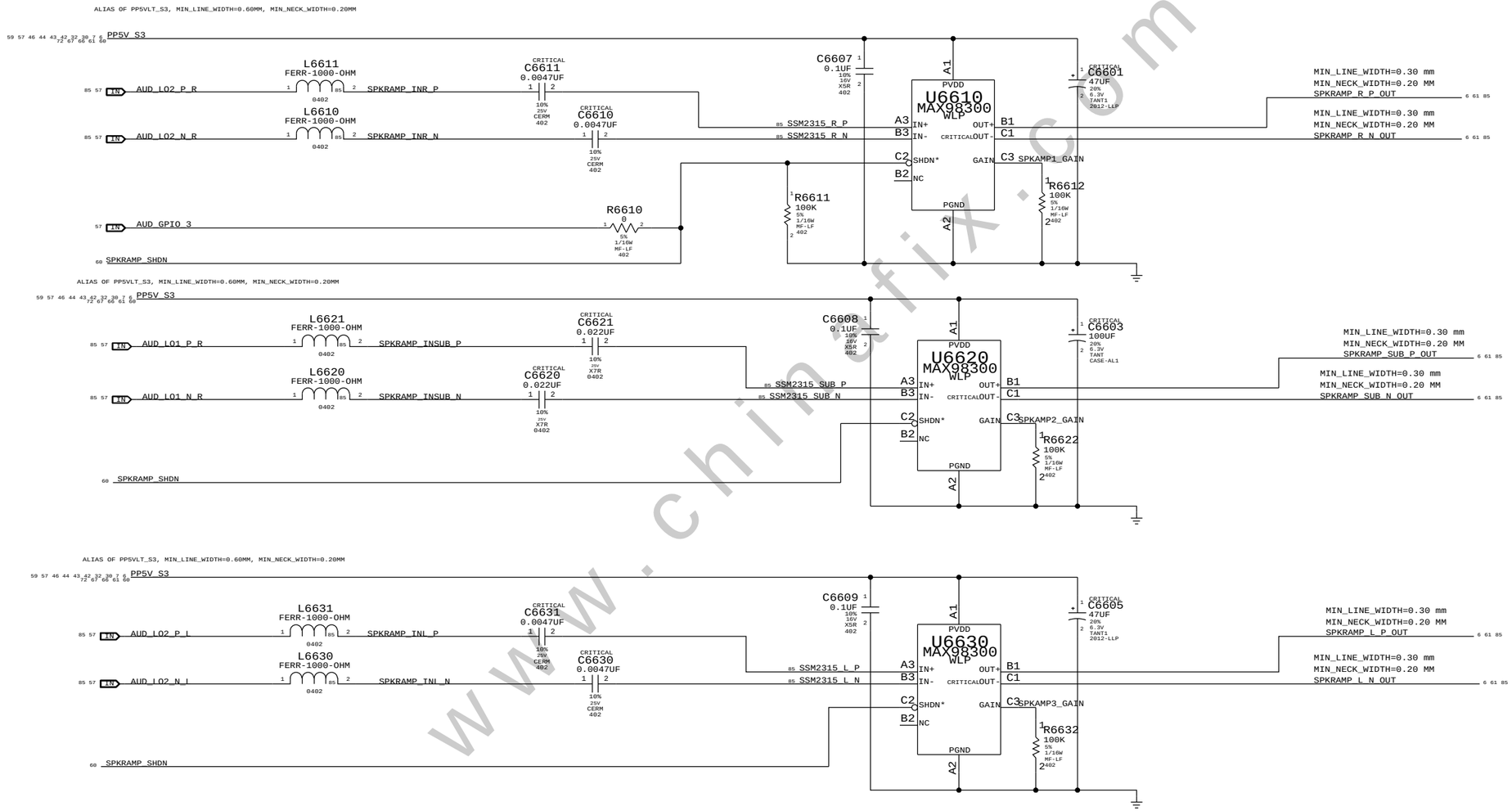
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2888

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	3DB



SYNC_MASTER=LENG_K90I SYNC_DATE=08/10/2010

PAGE TITLE

AUDI0: SPEAKER AMP

Apple Inc.

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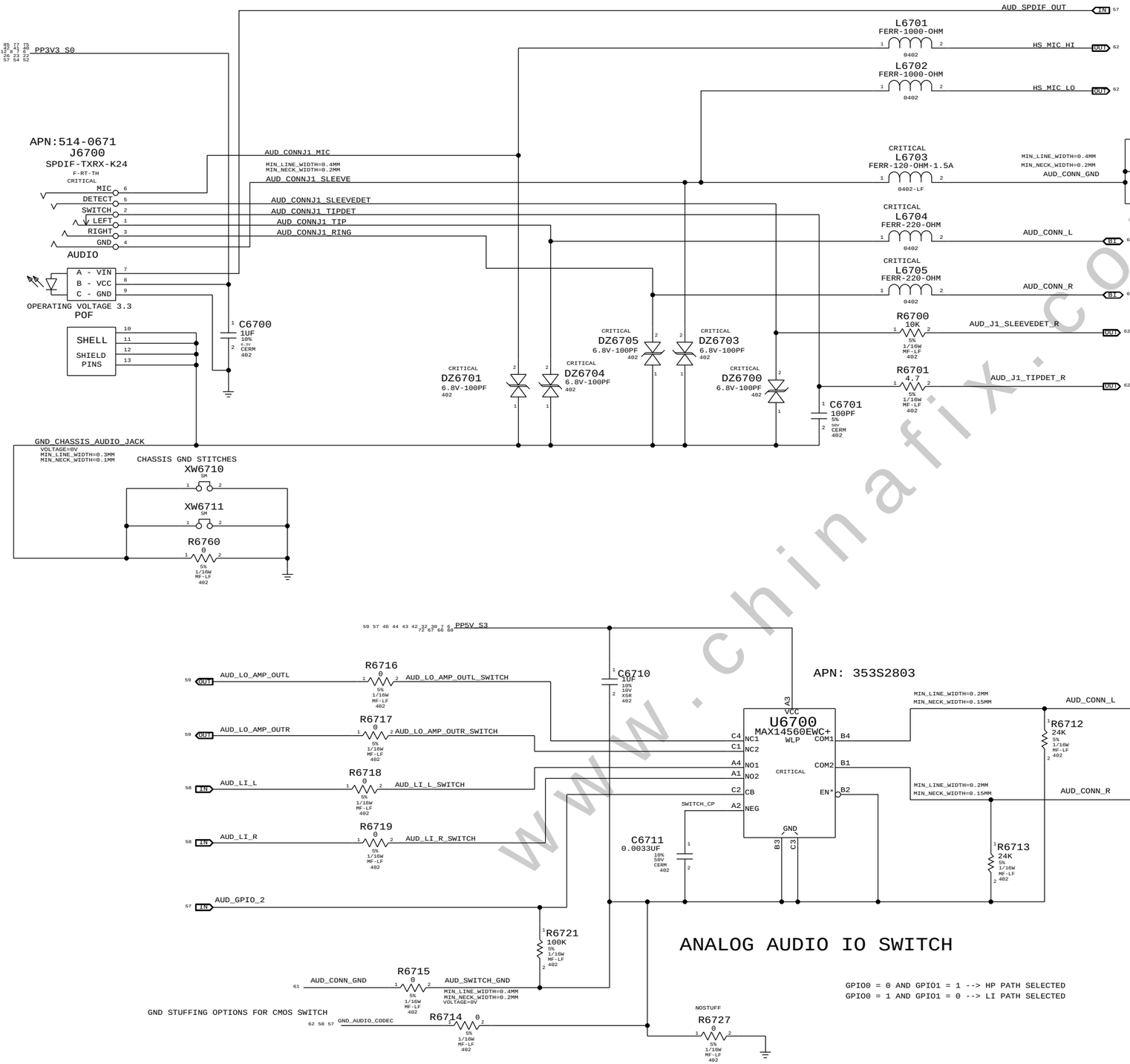
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SYNC_MASTER=LENG_K90I SYNC_DATE=08/10/2010

PAGE TITLE: AUDIO: JACK

Apple Inc.

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_2 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_2 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

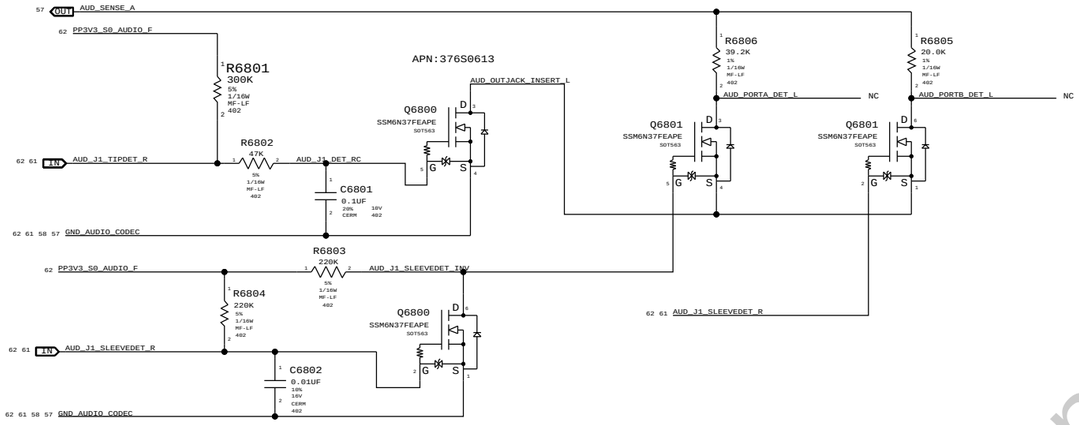
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

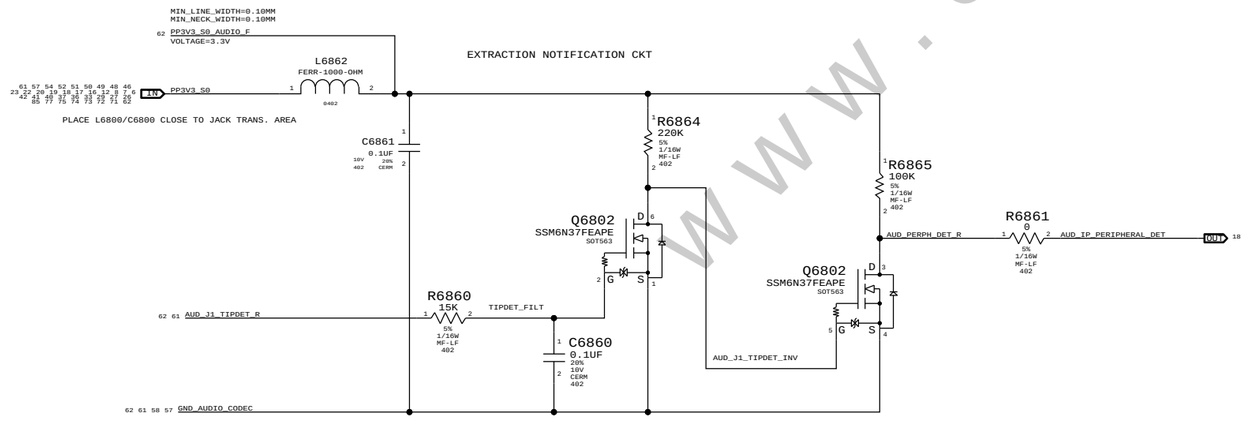
SOUTHBRIDGE RESOURCES

FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	COUGAR_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	COUGAR_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	COUGAR_POINT GPIO3/PIRQH

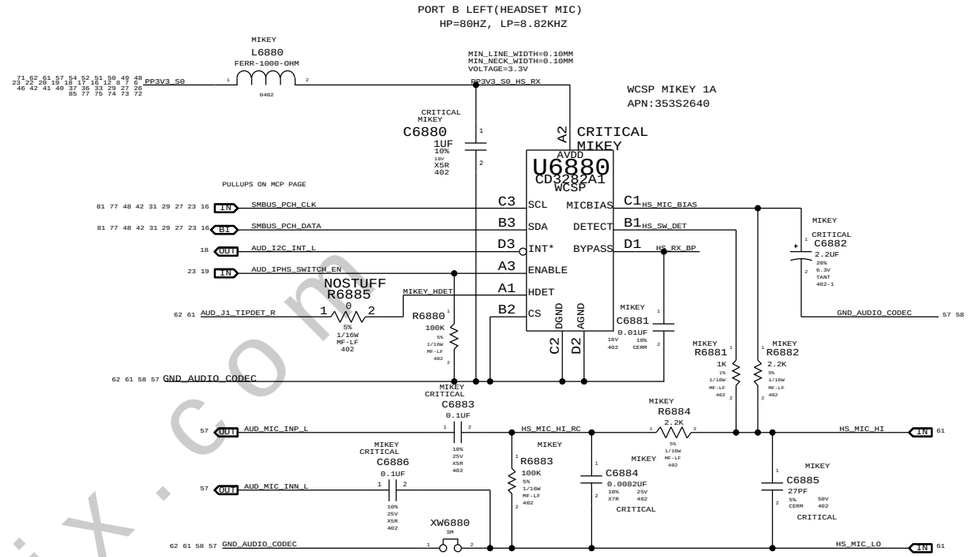
PORT A DETECT (HEADPHONES)

PORT B DETECT(SPDIF DELEGATE)

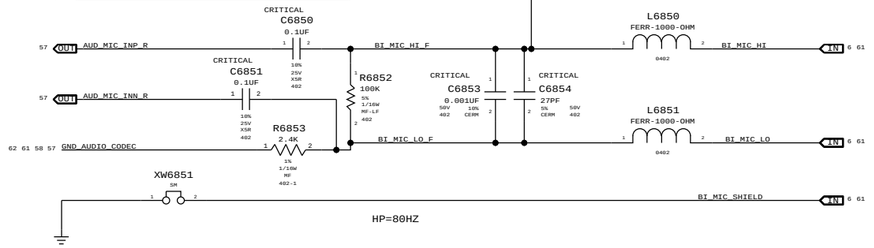




PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



SYNC_MASTER=LENG_K90I SYNC_DATE=08/10/2010

PAGE TITLE: AUDIO: JACK TRANSLATORS

Apple Inc.

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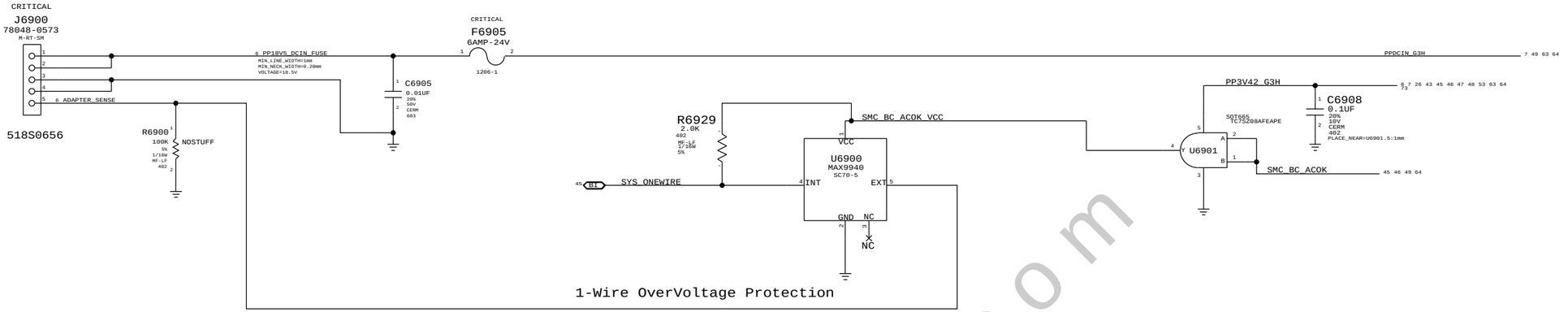
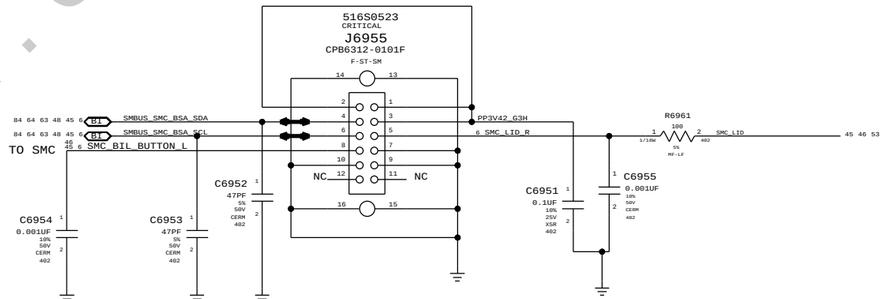
MagSafe DC Power Jack



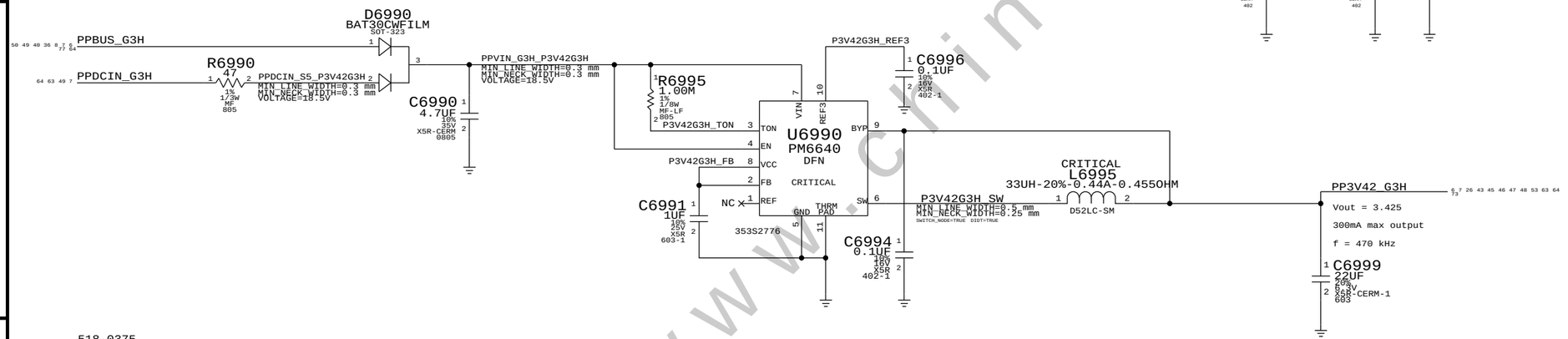
1-Wire OverVoltage Protection

BIL CONNECTOR

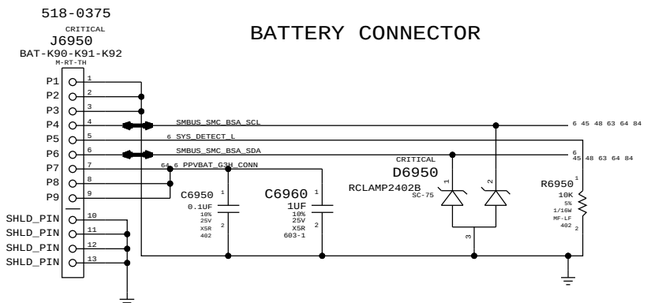


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=JACK_K90I SYNC_DATE=08/20/2010

PAGE TITLE: DC-In & Battery Connectors

Apple Inc.

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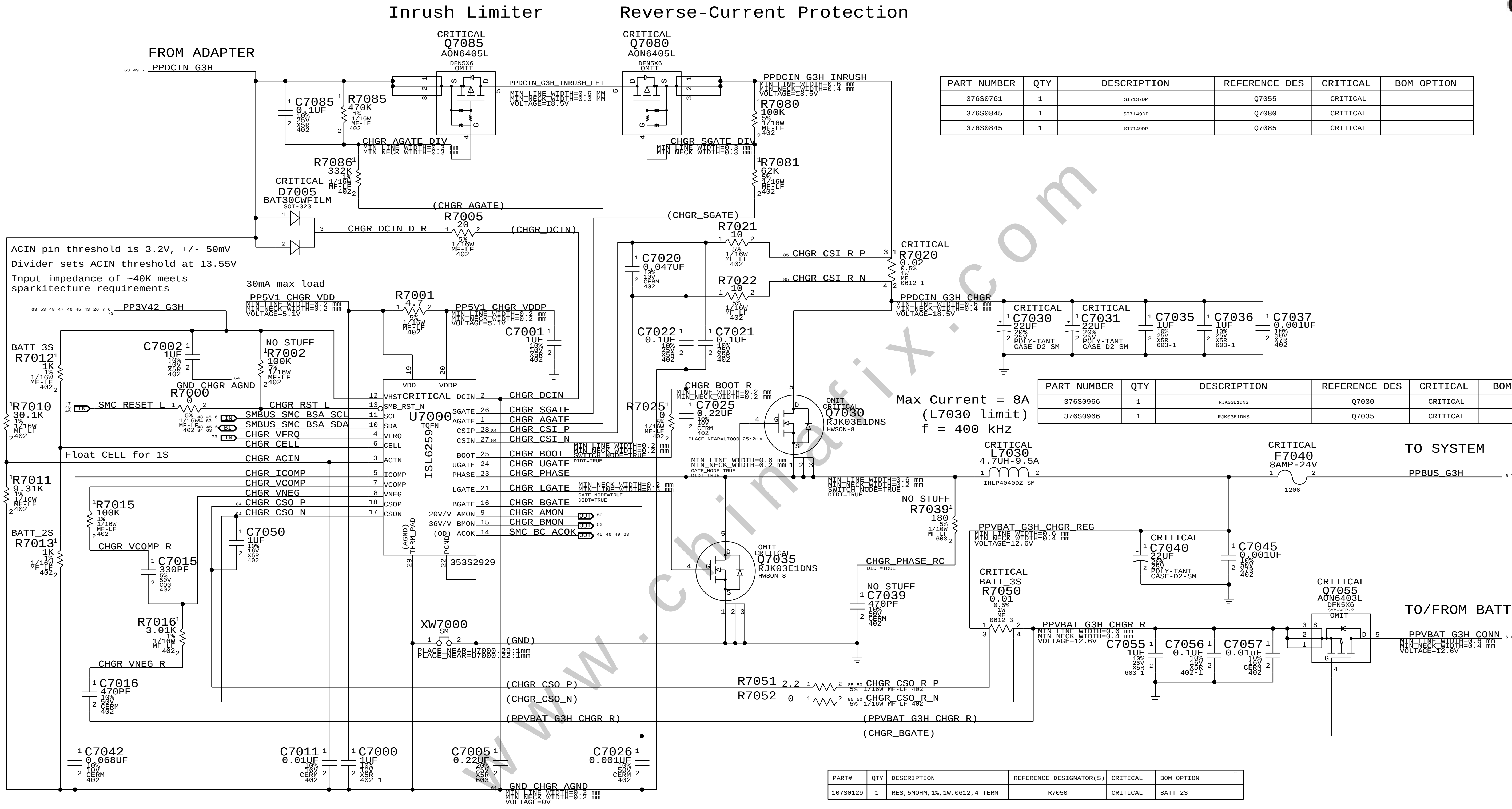

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0761	1	SI7137DP	Q7055	CRITICAL	
376S0845	1	SI7149DP	Q7080	CRITICAL	
376S0845	1	SI7149DP	Q7085	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7030	CRITICAL	
376S0966	1	RJK03E1DNS	Q7035	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0129	1	RES,5MOHM,1%,1W,0612,4-TERM	R7050	CRITICAL	BATT_2S

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC_MASTER=JACK_K90I SYNC_DATE=10/11/2010

PAGE TITLE

PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER

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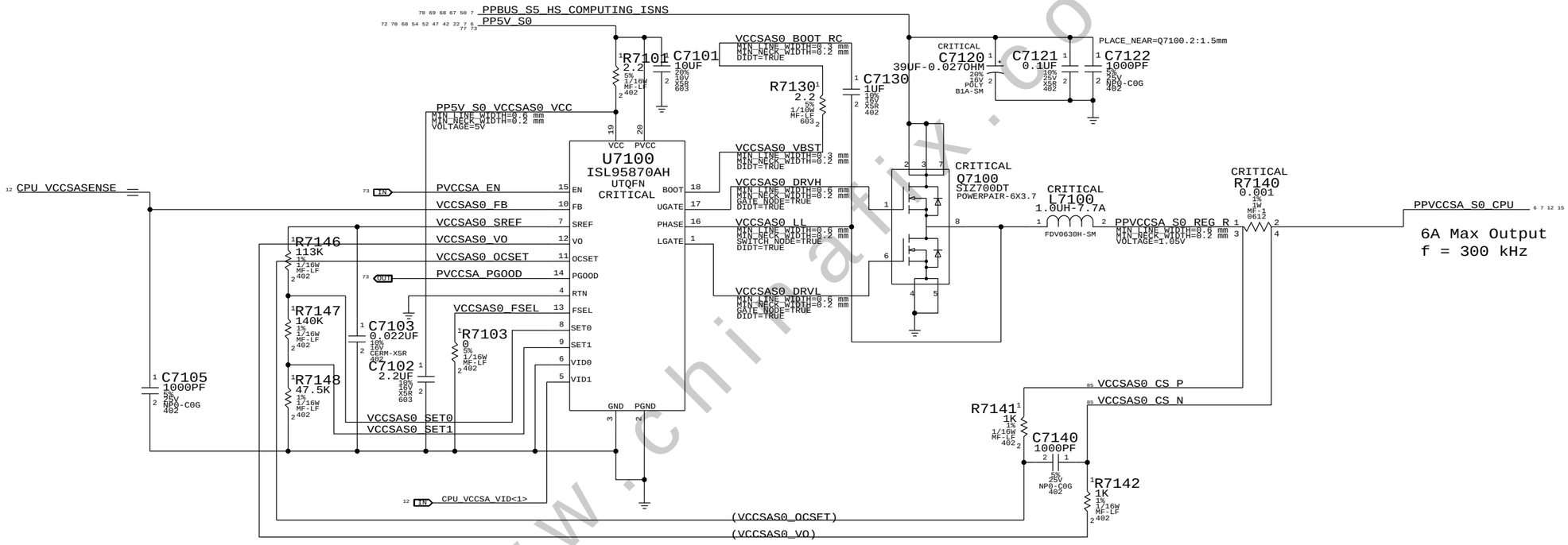
System Agent Power Supply



SYNC_MASTER=JACK_K90I SYNC_DATE=08/19/2010

PAGE TITLE: System Agent Supply

Apple Inc.

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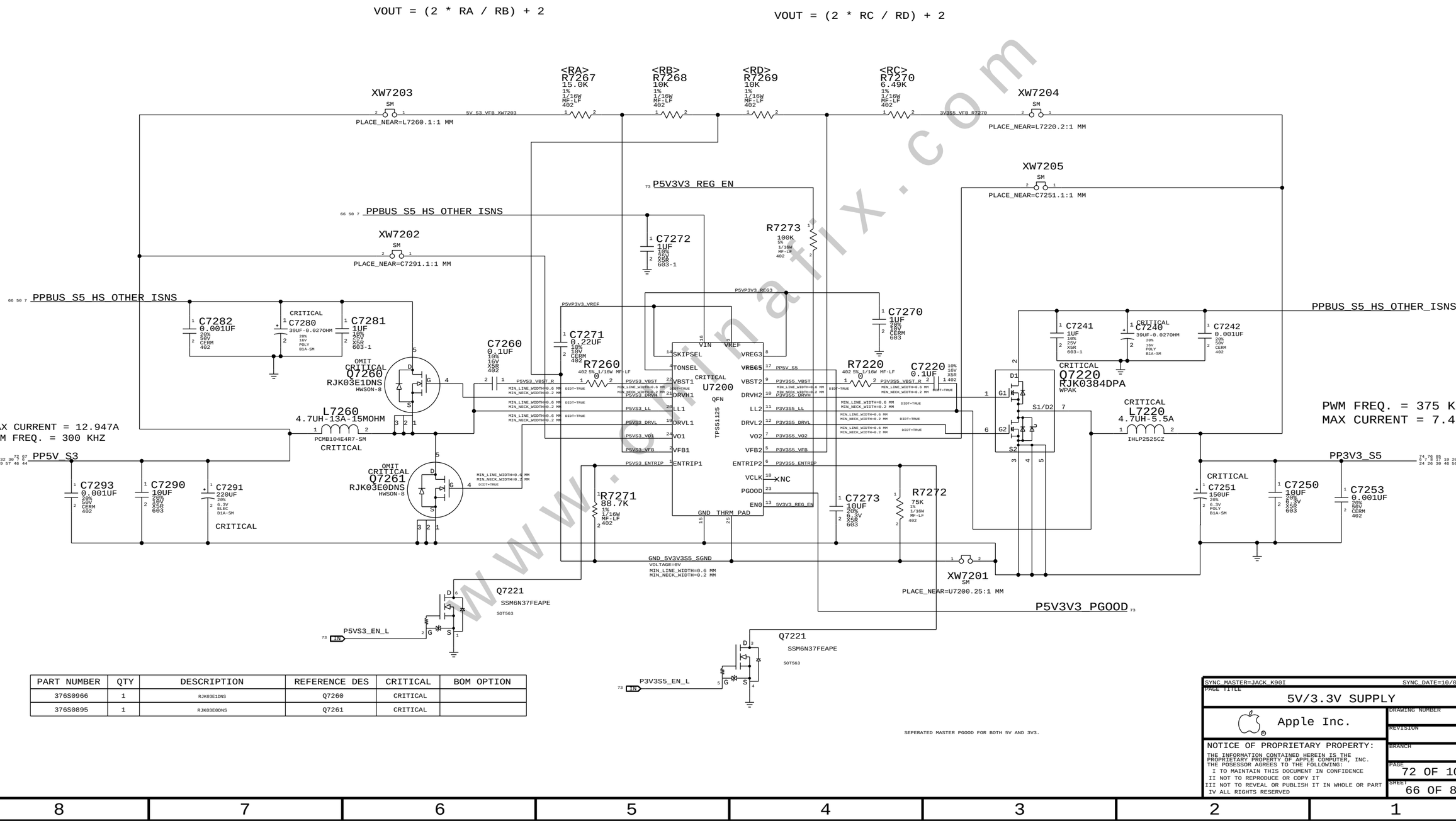
5V_S3/3.3V_S5 POWER SUPPLY

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

SYNC MASTER=JACK K90I SYNC DATE=10/04/2010

PAGE TITLE: 5V/3.3V SUPPLY

Apple Inc.

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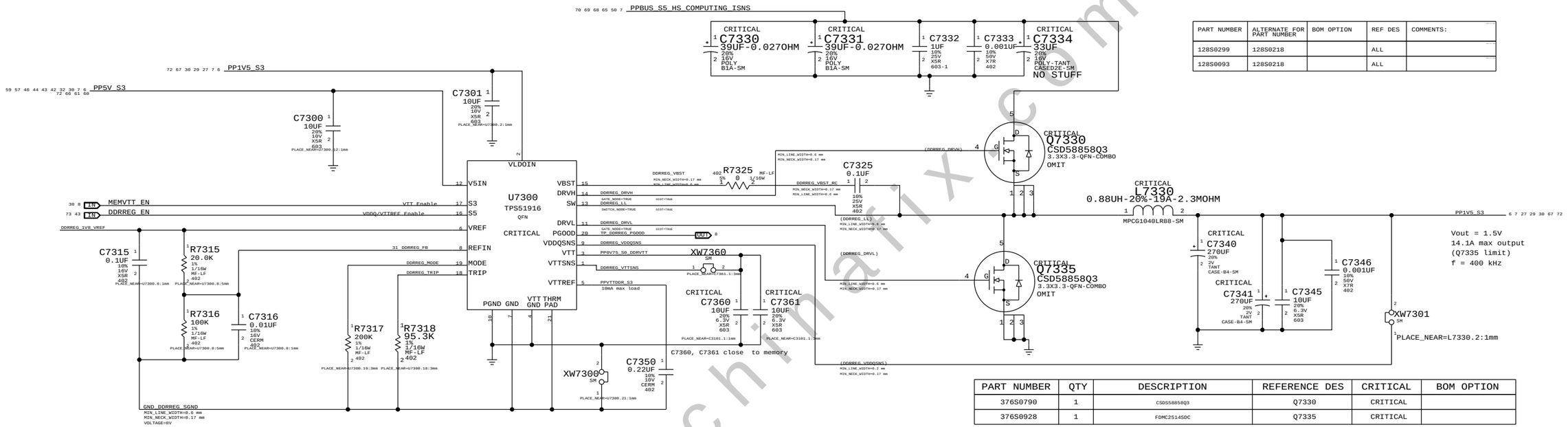

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0790	1	CSD55885Q3	Q7330	CRITICAL	
376S0928	1	FDMC2514SDC	Q7335	CRITICAL	

SYNC_MASTER=JACK_K90I SYNC_DATE=10/11/2010

PAGE TITLE: 1.5V DDR3 Supply

Apple Inc.

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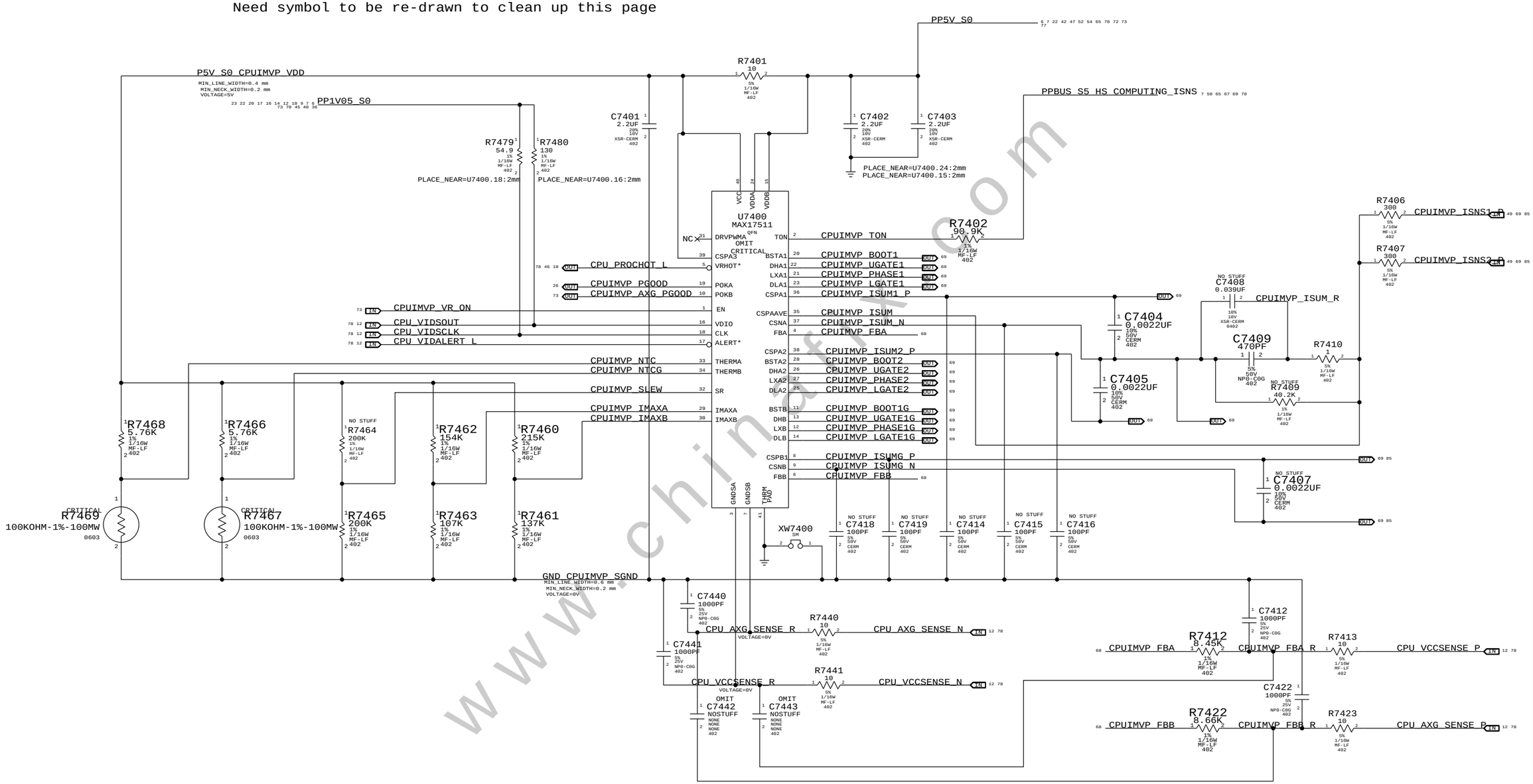
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OP
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	

Need symbol to be re-drawn to clean up this page



SYNC_MASTER=JACK_K90I SYNC_DATE=10/14/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

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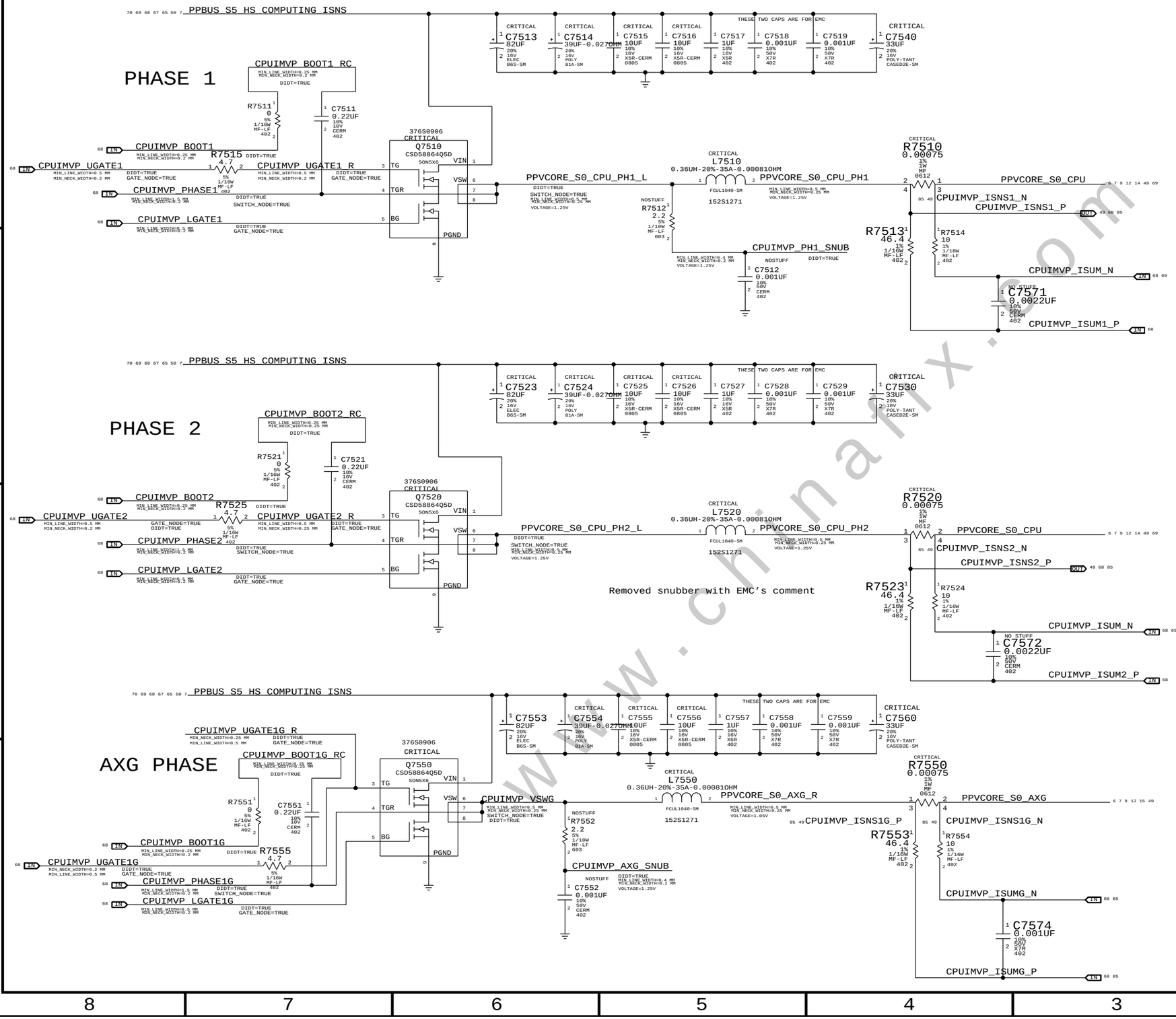

SYNC_MASTER=JACK_K90I SYNC_DATE=09/03/2010

PAGE TITLE: CPU IMVP7 & AXG VCore Output

Apple Inc.

DRAWING NUMBER: D

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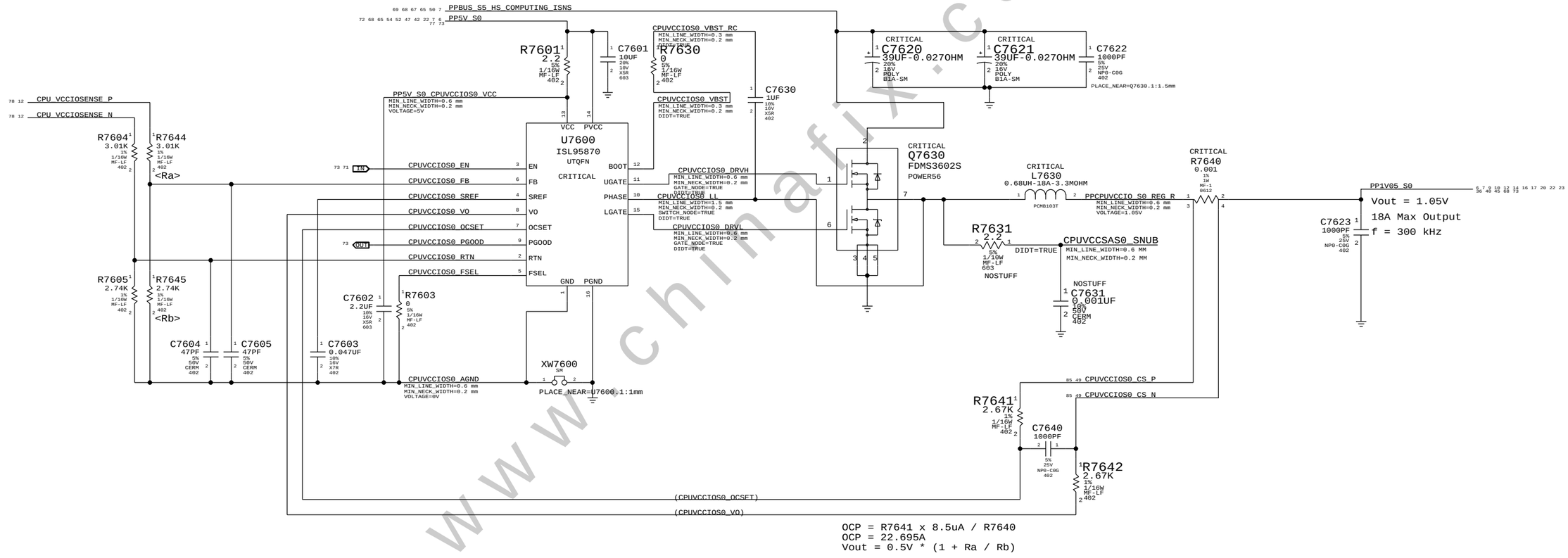
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=JACK K90I SYNC_DATE=08/19/2010

PAGE TITLE

CPUVCCIO (1.05V) Power Supply

Apple Inc.

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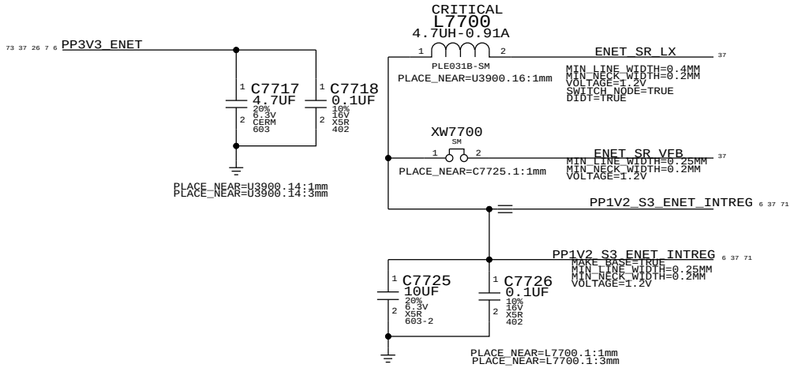
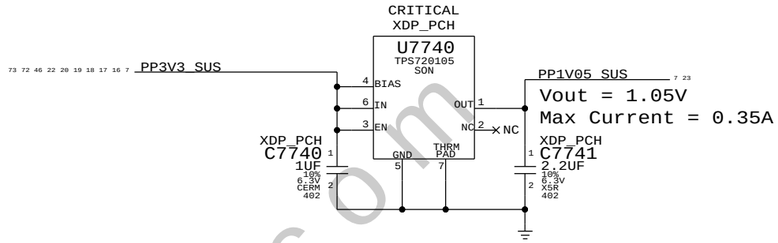
CAESAR IV 1.2V INT.VR CMPTS



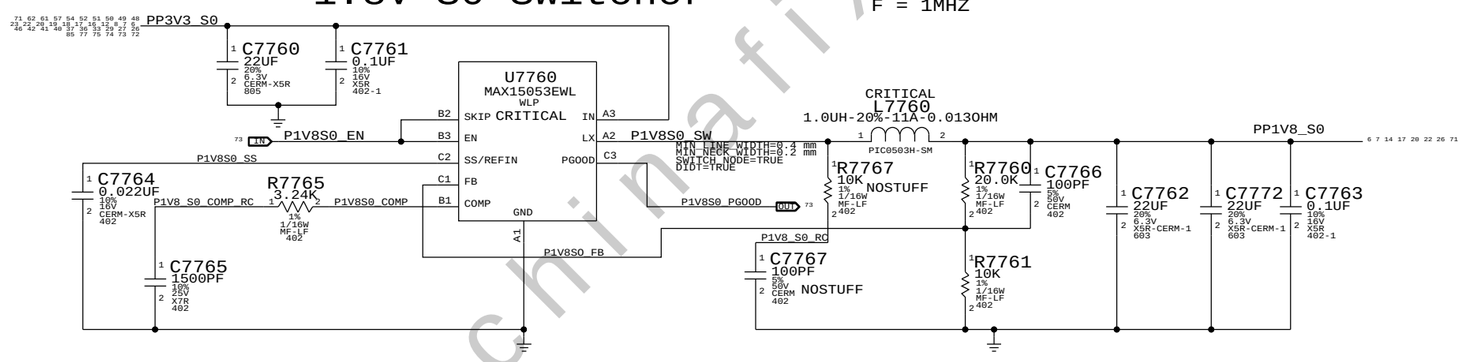
1.05V S5 LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

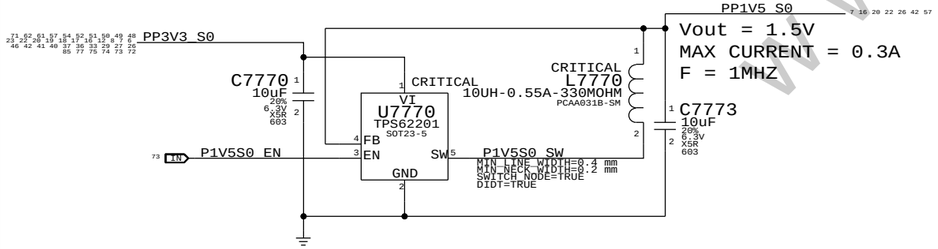


1.8V S0 Switcher

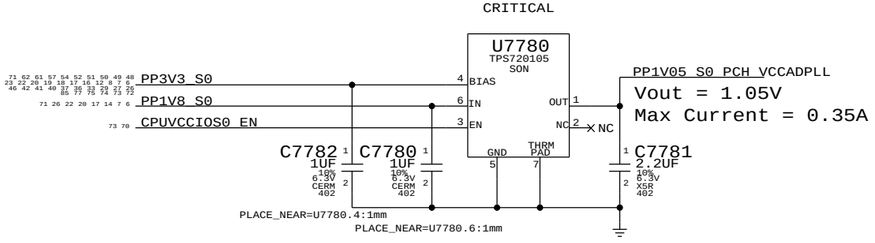
Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.5V S0 Switcher



1.05V S0 LDO



SYNC_MASTER=JACK_K90I SYNC_DATE=08/19/2010

PAGE TITLE
Misc Power Supplies

Apple Inc.

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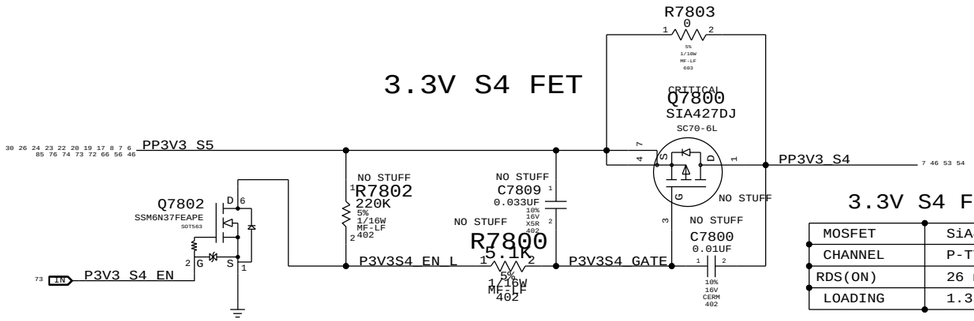
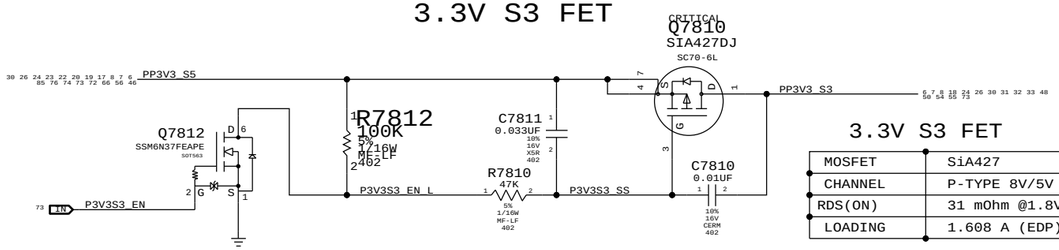
3.3V S4 FET



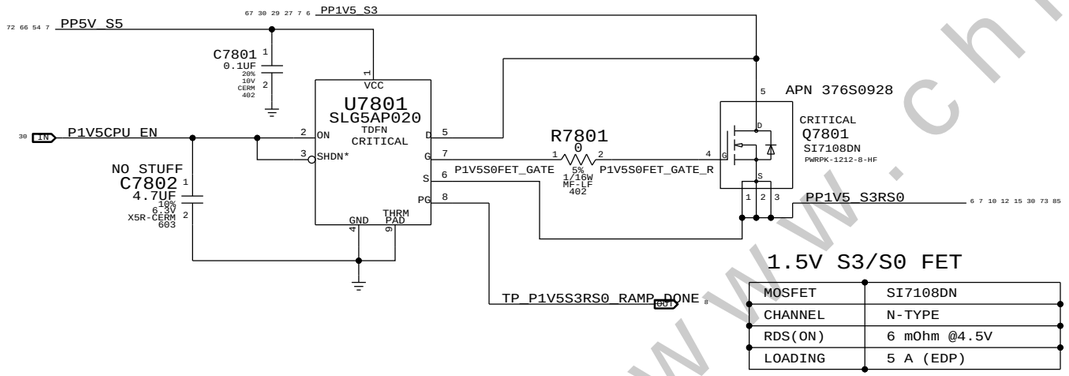
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)

3.3V S3 FET



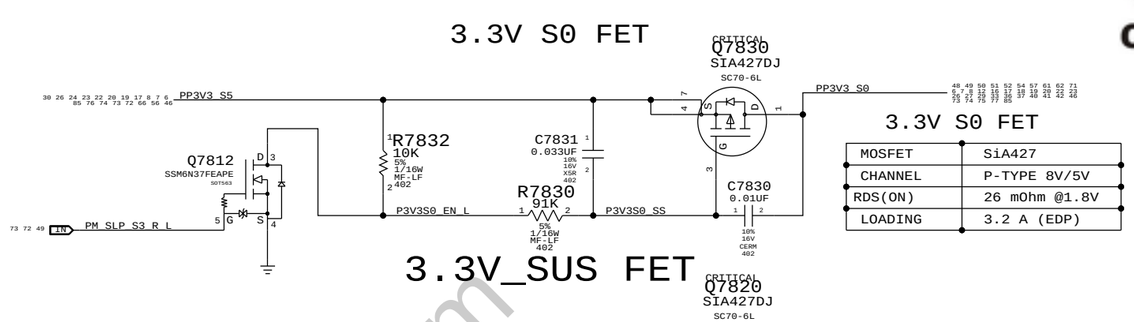
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

1.5V S3/S0 FET



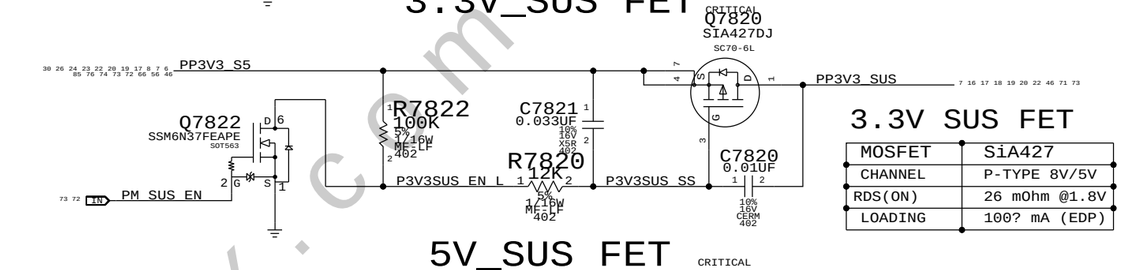
1.5V S3/S0 FET	
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

3.3V S0 FET



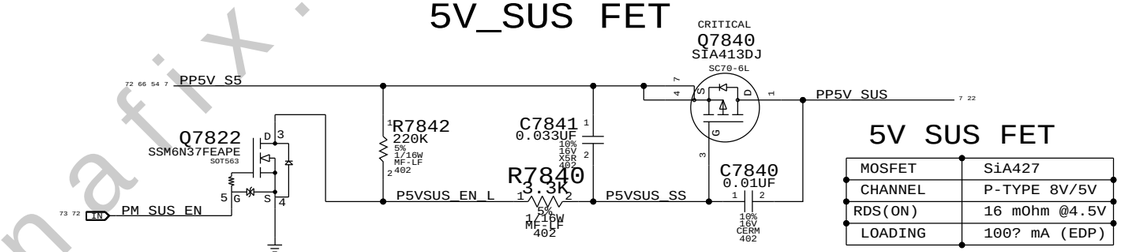
3.3V S0 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

3.3V_SUS FET



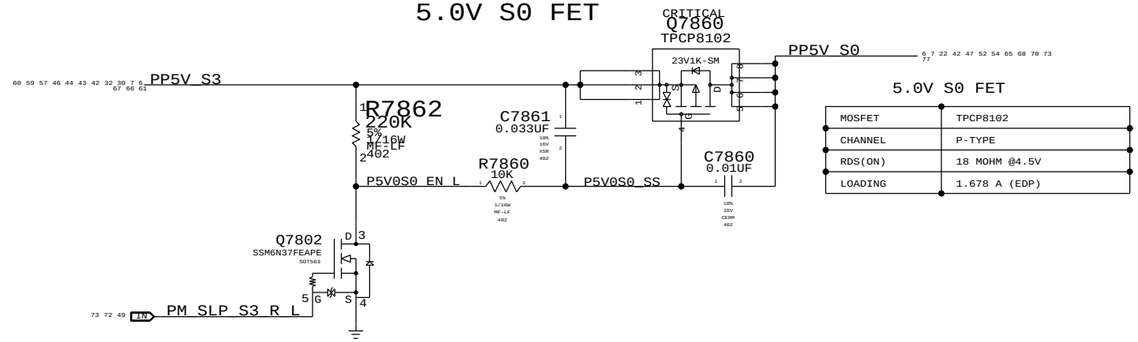
3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

5V_SUS FET



5V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	16 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET



5.0V S0 FET	
MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=JACK K90I SYNC DATE=10/22/2010

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Power FETs

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S5 Rail Enables & PGOOD

Internal pull-ups 100K +/- 20%

PP3V42_G3H

C7940 0.1UF 20% 16V CERM 402

U7941 SLG4AP012 TDFN — CRITICAL — VDD 343S0497

SMC_PM_G2_EN (45 6) — MAKE_BASE=TRUE

PP3V3_S5 (85 76 74 73 72 66 56 46 30 26 24 23)

Threshold: ??

DLY > 10 ms

S5PGOOD_DLY

C7941 220PF 50V CERM 402

IN A (1H0) — IN B — DLY 1C — GND — THRM PAD

OUT A (00,1H0) — P3V3S5_EN_L_R — MAKE_BASE=TRUE

OUT B (00,1P0) — P5V3V3_REG_EN — MAKE_BASE=TRUE

2:1 1.3V

R7941 100 1% 1/16W MF-LF 402 — P3V3S5_EN_L — MAKE_BASE=TRUE

C7942 0.033UF 10% 16V X5R 402 — NO STUFF

P3V3S5_EN_L — OUT (66 73)

P5V3V3_REG_EN — OUT (66 73)

S5_PWRGD — MAKE_BASE=TRUE — OUT (45)

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PP_SLP_S5_L	PP_SLP_S4_L	PP_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V,5V S3 ENABLE

PP3V42_G3H (63 53 48 47 46 45 43 26 7 6 73 64)

R7913 68K 5% 1/16W MF-LF 402 — P5V3_EN_L — MAKE_BASE=TRUE — OUT (66 73)

C7913 0.068UF 10% 16V CERM 402 — NO STUFF

PM_SLP_S4_L (45 30 17 6) — MAKE_BASE=TRUE

R7914 3.3K 5% 1/16W MF-LF 402 — PSOC_VBUS_EN — MAKE_BASE=TRUE — OUT (53 73)

PLACE_NEAR=U5701.3:6mm

R7910 100K 5% 1/16W MF-LF 402 — Delete R when pull-down added to PCH page

R7911 5.1K 5% 1/16W MF-LF 402

R7912 9.1K 5% 1/16W MF-LF 402 — PLACE_NEAR=Q7812.2:6mm

D3

Q7911 SSM3K15FV SOD-VESM-HF

PLACE_NEAR=U7300.16:6mm

P3V3S3_EN — MAKE_BASE=TRUE — OUT (72 73)

DDRREG_EN — MAKE_BASE=TRUE — OUT (43 67 73)

C7910 0.47UF 10% 6.3V CERM-XSR 402 — PLACE_NEAR=U7300.16:6mm

C7912 0.47UF 10% 6.3V CERM-XSR 402 — PLACE_NEAR=Q7812.2:6mm

3.3V S4 ENABLE

NO STUFF

R7916 0 5% 1/16W MF-LF 402 — P3V3_S4_EN — MAKE_BASE=TRUE — P3V3_S4_EN — OUT (72 73)

PM_SLP_S5_L (45 17) — IN

R7915 100K 5% 1/16W MF-LF 402 — PLACE_NEAR=U1800.G18:5mm

Delete R when pull-down added to PCH page

NO STUFF R7919 0 5% 1/16W MF-LF 402 — PLACE_NEAR=U1800.G18:5mm

SMC_S4_WAKESRC_EN (76 73 46 45 8)

S0 ENABLE

R7978 100 5% 1/16W MF-LF 402

PM_SLP_S3 (73 45 30 17 6) — IN

R7979 100K 5% 1/16W MF-LF 402 — Delete R when pull-down added to PCH page

PLACE_NEAR=U1800.P12:5mm

(PM_SLP_S3_R_L)

R7987 33K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7100.15:6mm

R7981 20K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7600.3:6mm

R7988 39K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7770.3:6mm

R7986 5.1K 5% 1/16W MF-LF 402 — PLACE_NEAR=U7760.B3:6mm

PM_SLP_S3_R_L — MAKE_BASE=TRUE — OUT (49 72 73)

P1V8S0_EN — MAKE_BASE=TRUE — OUT (71 73)

P1V5S0_EN — MAKE_BASE=TRUE — OUT (71 73)

CPUVCCIOS0_EN — MAKE_BASE=TRUE — OUT (70 71 73)

PVCCSA_EN — MAKE_BASE=TRUE — OUT (65 73)

C7987 0.47UF 10% 6.3V CERM-XSR 402 — PLACE_NEAR=U7100.15:6mm

C7981 0.47UF 10% 6.3V CERM-XSR 402 — PLACE_NEAR=U7600.3:6mm

C7988 0.47UF 10% 6.3V CERM-XSR 402 — PLACE_NEAR=U7770.3:6mm

C7986 0.47UF 10% 6.3V CERM-XSR 402 — PLACE_NEAR=U7760.B3:6mm

CPUVCORE ENABLE

ALL_SYS_PWRGD (73 45 26 23)

R7974 0 5% 1/16W MF-LF 402 — PLACE_NEAR=U7400.7:5mm — CPUIMVP_VR_ON — OUT (68)

PLACE_NEAR=U7400.7:5mm

R7976 0 5% 1/16W MF-LF 402

NO STUFF R7975 0 5% 1/16W MF-LF 402 — PLACE_NEAR=U7400.7:5mm

CPUVCCIOS0_PGOOD (73 70) — PM_PECI_PWRGD — OUT (45)

3.3V/5.0V Sus ENABLE

PP3V3_S5 (30 26 24 23 22 20 19 17 8 7 6 85 76 74 73 72 66 56 46)

PLACE_NEAR=U7940.1:2.3mm

C7943 0.1UF 20% 10V CERM 402

SMC_BATLOW_L:100K pull up on SMC page

SMC_BATLOW_L (46 45) — IN

U7940 74AUP1G3208 SOT891 — VCC — GND — A B C Y

ALL_SYS_PWRGD (23 26 45 73)

PM_SLP_SUS_L (17) — IN

PLACE_NEAR=U1800.G16:5mm

R7918 100K 5% 1/16W MF-LF 402 — Delete R when pull-down added to PCH page

NO STUFF R7917 0 5% 1/16W MF-LF 402

PM_SUS_EN — MAKE_BASE=TRUE — PM_SUS_EN — OUT (72 73)

S0 Rail PGOOD (BJT Version)

PP3V3_S5 (30 26 24 23 22 20 19 17 8 7 6 85 76 74 73 72 66 56 46)

PP3V3_S0 (67 26 74 73 72 66 56 46 45 43 42 41 40 37 36 33 29 27 26 85 77 75)

R7956 150K 1% 1/16W MF-LF 402

R7951 15.0K 1% 1/16W MF-LF 402

R7953 1K 5% 1/16W MF-LF 402 — VMON_3V3_DIV — VMON_Q2_BASE

R7952 7.15K 1% 1/16W MF-LF 402

R7954 1K 5% 1/16W MF-LF 402 — PP1V5_S3RS0 (85 73 72 30 15 12 10 7 6)

R7955 1K 5% 1/16W MF-LF 402 — PP1V05_S0 (23 22 20 17 16 14 12 10 9 7 6 73 70 68 45 40 36) — VMON_Q4_BASE

S0PGD_C

Q7950 ASMCC0179 DFN2015H4-8 — Q1 Q2 Q3 Q4 — CRITICAL — NC NC

353S2809 — S0PGD_BJT_GND_R

R7957 100 5% 1/16W MF-LF 402

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V SUS Detect

PP3V3_S5 (30 26 24 23 22 20 19 17 8 7 6 85 76 74 73 72 66 56 46)

PLACE_NEAR=U7930.6:2.3mm

No stuff C7931, 12ms Min delay time

U7930 Sense input threshold is 3.67V

C7930 0.1UF 20% 10V CERM 402

PP3V3_SUS (7 16 17 18 19 20 22 46 71 72 73)

R7933 100K 5% 1/16W MF-LF 402

CRITICAL

U7930 TPS3808G33DBVRG4 SOT23-6 — VDD — SENSE — RESET — CT — GND — MR — (90K IPU)

PP3V3_SUS (72 71 46 22 20 19 18 17 16 7 73)

S4_PGOOD_CT

C7931 0.001UF 20% 6.3V CERM 402 — NO STUFF

PM_RSMRST_L — OUT (17)

PM_RSMRST_L goes to U1800.C21

CHGR VFRQ Generation

PP3V42_G3H (63 53 48 47 46 45 43 26 7 6 73 64)

R7931 10K 5% 1/16W MF-LF 402

Q7931 SSM3K15FV SOD-VESM-HF

CHGR_VFRQ — OUT (64)

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

3.3V ENET FET

CRITICAL

Q7922 NTR4101P SOT-23-HF

PP3V3_S3 (48 33 32 31 30 26 24 18 8 7 5 72 55 54 50)

R7921 10K 5% 1/16W MF-LF 402

C7921 0.033UF 10% 16V X5R 402

R7922 100K 5% 1/16W MF-LF 402

C7922 0.01UF 10% 16V CERM 402

PP3V3_ENET (6 7 26 37 71)

PM_ENET_EN_L

P3V3ENET_SS

S0 Rail PGOOD Circuitry (ISL Version in development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

PP3V3_S0 (67 62 61 57 54 52 51 50 49 48 46 42 41 40 37 36 33 29 27 26)

PP5V_S0 (67 62 47 42 22 7 6 72 70 68 65 54 85 73 72 30 15 12 10 7 6)

PP1V5_S3RS0

PP1V05_S0

S0PGOOD_ISL

R7960 6.04K 1% 1/16W MF-LF 402

R7970 10K 1% 1/16W MF-LF 402

R7972 6.04K 1% 1/16W MF-LF 402

C7960 0.1UF 20% 10V CERM 402

U7960 ISL88042IRTEZ TDFN (TPU) — VDD — V2MON — V3MON — V4MON — RST — CRITICAL — NC

P5V_DIV_VMON — P1V5_DIV_VMON — P1V05_DIV_VMON

R7961 15.0K 1% 1/16W MF-LF 402

R7971 10K 1% 1/16W MF-LF 402

R7973 15.0K 1% 1/16W MF-LF 402

GND THRM_PAD — 353S2310

ALL_SYS_PWRGD_R

R7962 330 5% 1/16W MF-LF 402 — S0PGOOD_ISL — ALL_SYS_PWRGD — OUT (23 26 45 73)

P1V5S0_PGOOD from U7710

CPUIMVP_AXG_PGOOD (68) — R7967 10K 5% 1/16W MF-LF 402 — NO STUFF R7968 100 5% 1/16W MF-LF 402

P1V8S0_PGOOD (73) — R7966 100 5% 1/16W MF-LF 402

P5V3V3_PGOOD (66) — R7965 100 5% 1/16W MF-LF 402

CPUVCCIOS0_PGOOD (73 70) — R7964 100 5% 1/16W MF-LF 402

PVCCSA_PGOOD (65) — R7963 100 5% 1/16W MF-LF 402

DP S4 Power Enable

SMC_S4_WAKESRC_EN (76 73 46 45 8) — MAKE_BASE=TRUE — SMC_S4_WAKESRC_EN — OUT (8 45 46 73 76)

PSOC USB Power Enable

SMC_ADAPTER_EN (46 45 17) — IN

Q7920 2N7002DW-X-G SOT-363 — AC_EN_L — (AC_EN_L)

R7929 0 5% 1/16W MF-LF 402 — NO STUFF

(PM_SLP_S3_L)

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

WOL_EN — IN (19)

Q7925 2N7002DW-X-G SOT-363

Q7921 SSM3K15FV SOD-VESM-HF

PM_WLAN_EN_L — OUT (32)

Q7925 2N7002DW-X-G SOT-363

AP_PWR_EN — IN (18 32)

PM_SLP_S3_L (73 45 30 17 6) — IN

SYNC_MASTER=JACK_K90I SYNC_DATE=10/22/2010

PAGE TITLE: Power Control 1/ENABLE

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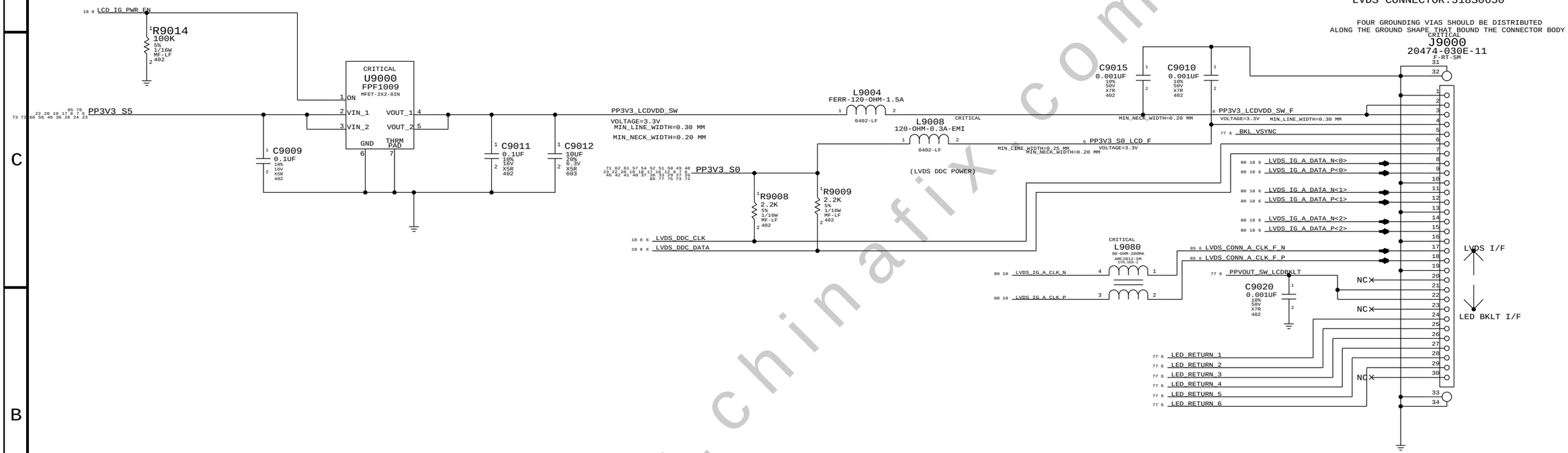
LCD CONNECTOR

LVDS CONNECTOR:518S0650

FOUR GROUNDING VIAS SHOULD BE DISTRIBUTED
ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY



SYNC_MASTER=K24_MLB	SYNC_DATE=07/20/2009
PAGE TITLE: LVDS CONNECTOR	
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T29 A High-Speed Sig

DP EXTA ML C P<0> C9300 0.1UF DP EXTA ML P<0>
DP EXTA ML C N<0> C9301 0.1UF DP EXTA ML N<0>
DP EXTA ML C P<1> C9302 0.1UF DP EXTA ML P<1>
DP EXTA ML C N<1> C9303 0.1UF DP EXTA ML N<1>
DP EXTA ML C P<2> C9304 0.1UF DP EXTA ML P<2>
DP EXTA ML C N<2> C9305 0.1UF DP EXTA ML N<2>
DP EXTA ML C P<3> C9306 0.1UF DP EXTA ML P<3>
DP EXTA ML C N<3> C9307 0.1UF DP EXTA ML N<3>
DP EXTA AUXCH C P C9308 0.1UF DP EXTA AUXCH P
DP EXTA AUXCH C N C9309 0.1UF DP EXTA AUXCH N

PP3V3_S0 R9309 1M 5% MF 1/20W 201 DP EXTA AUXCH P
DP EXTA AUXCH N R9308 1M 5% MF 1/20W 201

If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.

R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.

T29 A BIAS R2DP0
T29 A BIAS R2DN0
GND_VOID=TRUE (C9370/C9371)
T29 D2R N<0> C9370 0.47UF
T29 D2R P<0> C9371 0.47UF
OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29 R2D C N<0> L9372 1.0NH+/-0.1NH 0201-1 T29 R2D C F N<0> C9372 0.47UF (C9372.2) GND_VOID=TRUE
T29 R2D C P<0> L9373 1.0NH+/-0.1NH 0201-1 T29 R2D C F P<0> C9373 0.47UF (C9373.2) GND_VOID=TRUE

T29 signals are P/N-swapped after AC caps to improve layout.

T29 A BIAS R2DP1
T29 A BIAS R2DN1
GND_VOID=TRUE (C9380/C9381)
T29 D2R N<1> C9380 0.47UF
T29 D2R P<1> C9381 0.47UF
OVERSIZE_PAD=0.875 mm^2 (Both L's)
T29 R2D C N<1> L9382 1.0NH+/-0.1NH 0201-1 T29 R2D C F N<1> C9382 0.47UF (C9383.2) GND_VOID=TRUE
T29 R2D C P<1> L9383 1.0NH+/-0.1NH 0201-1 T29 R2D C F P<1> C9383 0.47UF (C9383.2) GND_VOID=TRUE

GND_VOID=TRUE R9372 1.5K 5% MF 1/20W 201 T29 R2D P<0>
GND_VOID=TRUE R9373 1.5K 5% MF 1/20W 201 T29 R2D N<0>
GND_VOID=TRUE R9382 1.5K 5% MF 1/20W 201 T29 R2D P<1>
GND_VOID=TRUE R9383 1.5K 5% MF 1/20W 201 T29 R2D N<1>

T29 Path Biasing

D9364 BAR90-02LRH GND_VOID=TRUE (D9364.2)
D9372 BAR90-02LRH
D9373 BAR90-02LRH
D9365 BAR90-02LRH
CRITICAL (All 4 D's)
D9372/D9373: SIGNAL_MODEL=T29PIN
D9364/D9365: SIGNAL_MODEL=EMPTY
T29: TX_0
T29DPA_ML_C_P<0> OUT 76 83
T29DPA_ML_C_N<0> OUT 76 83
GND_VOID=TRUE (D9372/D9373)
GND_VOID=TRUE (D9365.2)
R9374 1.5K 5% MF 1/20W 201
R9375 1.5K 5% MF 1/20W 201

T29 D2R C P<0>
T29 D2R C N<0>
T29 D2R C P<1> IN 76 83
T29 D2R C N<1> IN 76 83

D9360 BAR90-02LRH GND_VOID=TRUE (D9360.2)
D9382 BAR90-02LRH
D9383 BAR90-02LRH
D9361 BAR90-02LRH
CRITICAL (All 4 D's)
SIGNAL_MODEL=T29PIN (D9382/D9383)
SIGNAL_MODEL=EMPTY (D9360/D9361)
T29: TX_1
T29DPA_ML_C_P<2> OUT 76 83
T29DPA_ML_C_N<2> OUT 76 83
GND_VOID=TRUE (D9382/D9383)
GND_VOID=TRUE (D9361.2)
R9384 1.5K 5% MF 1/20W 201
R9385 1.5K 5% MF 1/20W 201

Both R's must connect to C in star topology.

DP Path Biasing

R9361 1.5K 5% MF 1/20W 201
R9360 1.5K 5% MF 1/20W 201
R9365 1.5K 5% MF 1/20W 201
R9364 1.5K 5% MF 1/20W 201

DP A BIAS0 VOLTAGE=3.3V
DP A BIAS2 VOLTAGE=3.3V
R9362 51 5% 1/20W MF 201
R9363 51 5% 1/20W MF 201
Both R's: PLACE_NEAR=C9361.1:2mm
C9358 0.1UF 10% 16V X5R 402

DP A Super-Driver

PP3V3_S0
C9310 2.2UF 20% 6.3V CERM 402-LF
C9311 0.1UF 10% 16V X5R-CERM 0201
C9312 0.1UF 10% 16V X5R-CERM 0201

PS8301 I2C Addresses:

A1	A0	Addr (W/R)
0	0	0x96/0x97
0	1	0xB6/0xB7
1	0	0x94/0x95
1	1	0xB4/0xB5

Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.

NO STUFF R9311 1K
R9310 1K 5% 1/16W MF-LF 402
R9312 1K 5% 1/16W MF-LF 402

U9310 PS8301TQFN40GTR-A2 QFN CRITICAL

DP EXTA ML P<0>	1 IN_D0P	OUT_D0P 30	DP SDRVA ML C P<0>
DP EXTA ML N<0>	2 IN_D0N	OUT_D0N 29	DP SDRVA ML C N<0>
DP EXTA ML P<1>	4 IN_D1P	OUT_D1P 28	DP SDRVA ML C P<1>
DP EXTA ML N<1>	5 IN_D1N	OUT_D1N 27	DP SDRVA ML C N<1>
DP EXTA ML P<2>	7 IN_D2P	OUT_D2P 25	DP SDRVA ML C P<2>
DP EXTA ML N<2>	8 IN_D2N	OUT_D2N 24	DP SDRVA ML C N<2>
DP EXTA ML P<3>	9 IN_D3P	OUT_D3P 23	DP SDRVA ML C P<3>
DP EXTA ML N<3>	10 IN_D3N	OUT_D3N 22	DP SDRVA ML C N<3>
DP EXTA DDC CLK	14 IN_SCL	AC_AUXP 20	DP SDRVA AUXCH C P
DP EXTA DDC DATA	13 IN_SDA	AC_AUXN 19	DP SDRVA AUXCH C N
DP EXTA AUXCH P	16 IN_AUXP	OUT_AUXP_SCL 18	(DP_SDRVA_AUXCH_P)
DP EXTA AUXCH N	15 IN_AUXN	OUT_AUXN_SDA 17	(DP_SDRVA_AUXCH_N)
DP EXTA HPD	3 IN_HPD	(IPD) OUT_HPD 31	(DP_SDRVA_HPD)
DPSDRVA I2C CTL EN	26 I2C_CTL_EN (IPU)	CA_DET 32	DP A CA DET
DPSDRVA I2C ADDR0	36 I2C_ADDR0 (IPD)	CEXT 11	DPSDRVA CEXT
DPSDRVA I2C ADDR1	35 I2C_ADDR1 (IPD)		
I2C DPSDRVA SCL	38 SCL_CTL		
I2C DPSDRVA SDA	37 SDA_CTL		
DPSDRVA REXT	12 REXT		
DP AUXCH ISOL	39 AUXDDC_OFF (IPD)		
DP A PWRDWN R	34 PD (IPD)		

PLACE_NEAR=U9310.11:2 mm
C9319 2.2UF 20% 6.3V CERM 402-LF
GND THMPAD 6 33 41

SDRV_PD R9318 0 5% 1/20W MF 201
R9319 4.22K 1% 1/16W MF-LF 402

PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).

R9354 30 5% 1/20W MF 201 DP SDRVA ML R P<0>
R9355 30 DP SDRVA ML R N<0>
R9350 30 DP SDRVA ML R P<2>
R9351 30 DP SDRVA ML R N<2>
C9364 0.22UF 20% 6.3V X5R 201 DP SDRVA ML P<0>
C9365 0.22UF DP SDRVA ML N<0>
C9360 0.22UF DP SDRVA ML P<2>
C9361 0.22UF DP SDRVA ML N<2>

R9352 270 5% 1/20W MF 201
R9353 270 5% 1/20W MF 201 PP3V3_S0

C9363 0.1UF 10% 16V X5R-CERM 0201
C9362 0.1UF
C9367 0.1UF
C9366 0.1UF
C9369 0.1UF
C9368 0.1UF

AUXCH Snoop Port, used by PS8301 during training.

C9359 0.1UF 10% 16V X5R 402
CRITICAL U9359 74LVC1G04DBVCK SC70
DP A PWRDWN DP A BIAS
IC supports input high while Vcc = 0V.

DP/T29 A Low-Speed MUX

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power

OMIT_TABLE U9390 CBTL04DP081 HVQFN

DP SDRVA ML N<3>	31 DIN1_0+	DOUT_0+ 1	T29DPA ML N<3>
DP SDRVA ML P<3>	30 DIN1_0-	DOUT_0- 2	T29DPA ML P<3>
DP SDRVA ML N<1>	27 DIN1_1+		T29: Unused
DP SDRVA ML P<1>	26 DIN1_1-		
DP SDRVA AUXCH P	19 AUX1+	DOUT_1+ 4	T29DPA ML N<1>
DP SDRVA AUXCH N	18 AUX1-	DOUT_1- 5	T29DPA ML P<1>
DP SDRVA HPD	17 HPD_1		T29: LSX_A_R2P/P2R (P/N)
CKPLUS_WAIVE=NdifPr_badTerm		AUX+ 6	DP A EXT AUXCH P
T29 A RSVD N	25 DIN2_0+	AUX- 7	DP A EXT AUXCH N
T29 A RSVD P	24 DIN2_0-		T29: RX_1 Bias Sink
(T29_A_LSX_P2R)	23 DIN2_1+	HPD_IN 8	DP A EXT HPD
(T29_A_LSX_R2P)	22 DIN2_1-		
T29_D2R1_BIASP	15 AUX2+		
T29_D2R1_BIASN	14 AUX2-		
NC	13 HPD_2		
DP A PWRDWN	10 GPU_SEL		
T29 A BIAS	32 AUX_SEL	LO=Port A HI=Port B	
	11 NC		

THMPAD GND 33 28 21

R9399 100K 5% 1/20W MF 201
R9398 100K 5% 1/20W MF 201
R9396 1K 5% 1/20W MF 201
R9397 1K 5% 1/20W MF 201

CBTL04DP081 (353S3151) and PI3VEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.

SIGNAL_MODEL=T29DP_MUX

Port A MCU

PP3V3_SW_DPAPWR
Must be 3.3V DP A port power
C9330 0.1UF 20% 16V CERM 402
C9331 0.1UF 20% 16V CERM 402

U9330 LPC1112A HVQFN25 CRITICAL OMIT_TABLE

DP A CA DET	1 RESET#/PIO0_0	R/PIO1_0/AD1 16	T29DPA CONFIG1 RC
	2 PIO0_1/CLKOUT	R/PIO1_1/AD2 17	T29DPA CONFIG2 RC
T29 LSEO<0>	7 PIO0_2/SSEL/CT16B0_CAP0	R/PIO1_2/AD3 18	T29 A HV EN R
I2C T29 SCL	8 PIO0_4/SCL (OD)	(IPU) SWDIO/PIO1_3/AD4 19	T29 A UC ADDR
I2C T29 SDA	9 PIO0_5/SDA (OD)	PIO1_4/AD5/WAKEUP 20	DP A EXT HPD
T29DPA HPD	10 PIO0_6/SCK	PIO1_6/RXD 23	T29 A LSX P2R
T29 A BIAS R	11 PIO0_7/CTS#	PIO1_7/TXD 24	T29 A LSX R2P
T29 LSOE<0>	12 PIO0_8/MISO/CT16B0_MAT0	PIO1_8/CT16B1_CAP0 6	T29 LSEO<1>
T29 LSOE<1>	13 PIO0_9/MOSI/CT16B0_MAT1		
	14 SWCLK/PIO0_10/SCK/CT16B0_MAT2 (OD)		
T29 MCU INT L	15 R/PIO0_11/AD0 (OD)	XTALIN 4	
	VSS 3	THRM PAD 25	

R9392 51 5% 1/20W MF 201
R9393 51 5% 1/20W MF 201
R9338 10K 5% 1/16W MF-LF 402
R9334 10K 5% 1/16W MF-LF 402
T29 A HV EN OUT 8 36 76
R9335 1K 5% 1/16W MF-LF 402
R9336 10K 5% 1/16W MF-LF 402
R9339 1M 5% 1/16W MF-LF 402

P2R = Plug to Receptacle
R2P = Receptacle to Plug

I2C Addr: 0x26/0x27 (Wr/Rd)

=T29_WAKE_L:
Desktops use PCIe WAKE#
Mobiles use S4 WAKE#

=T29_WAKE_L
OMIT R9330 0 5% 1/16W MF-LF 402
SWCLK
SWDIO
T29_A_UC_ADDR

R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.

Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100 ohm pull-downs would defeat DP Sink's detection of DP Source.

SYNC_MASTER=T29 SYNC_DATE=10/16/2016
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Port A HV Power Switch

PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

PP15V_T29
20V Max

R9416 470K 5% 1/16W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 TPS2590 QFN
EN* (IPU-Weak!) FLT*
RTRY* ILIM
CT IFLT
GND THRM PAD
CRITICAL

C9411 0.1UF 10% 50V X7R 603-1
PPHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

D9410 SM STPS2L30AF
CRITICAL

DPAPWRSW_HVEN_L_R
TP_DPAPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT
DPAPWRSW_CT

C9412 0.47UF 10% 16V CERM-X5R 402 <CT>

R9410 100K 1% 1/16W MF-LF 402 <RFLT>

R9411 200K 1% 1/16W MF-LF 402 <RLIM>

	Nominal	Min	Max
IFLT	885mA	876mA	894mA (*)
ILIM	935mA	925mA	944mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance unknown

IFLT = 200k / RFLT = 885mA
ILIM = 201k / RLIM = 935mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

Bleeder Resistor
2.5V / 249 ohm = 10mA
R9419 249 1% 1/16W MF-LF 402 P = ~27mW
DPAPWR_BLDR_E
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Q9419 DMB53D0UV SOT-563
DPAPWR_BLDR_B

Note: Bleeder active when DPAPWRSW_HV_DET is HIGH and T29_A_HV_EN is LOW.

T29_A_HV_EN

3.3V/HV Power MUX

B1100 chosen for high Vf for 2.9V mode.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

CRITICAL D9425 POWERDI-123 DFLS1100
CRITICAL Q9425 SI8409DB 8GA

3.3V/HV MUXed

3.3V Always

Blocking FET, off when Source >3.4V or HV_EN high.

R9427 100K 1% 1/16W MF-LF 402
R9428 21.5K 1% 1/16W MF-LF 402
R9425 4.7K 5% 1/16W MF-LF 402
R9426 1K 5% 1/16W MF-LF 402
R9430 4.7K 5% 1/16W MF-LF 402

DPAPWRSW_VREF
DPAPWRSW_P3V3_ON_L
DPAPWRSW_HV_DET_R_L

CRITICAL U9426 ZXRE060A SOT353 GND PGND FB IN OUT

R9429 4.7K 5% 1/16W MF-LF 402
C9424 0.47UF 10% 16V X5R 402
DPAPWRSW_ON_L_C
DPAPWRSW_HV_DET_L

C9426 0.1UF 20% 10V CERM 402
NO STUFF C9429 0.1UF 20% 10V CERM 402
R9424 22 5% 1/10W MF-LF 402

Q9426 MMDT3946XG SOT363

R9418 1K 5% 1/10W MF-LF 402 DPAPWRSW_HV_DET

ZXRE060A REF range: 0.595-0.605V (0.600V nominal)
Circuit threshold range: 3.363-3.439V (3.395V nominal)

DPAPWRSW_NPN_E

R9433 220 5% 1/16W MF-LF 402
R9432 10K 5% 1/16W MF-LF 402

Q9430 SSM6N37FEAPE SOT563
Q9430 SSM6N37FEAPE SOT563

DPAPWRSW_P3V3_ON
DPAPWRSW_ON
T29_A_HV_EN

R9437 82 5% 1/16W MF-LF 402

R9435 100K 1% 1/16W MF-LF 402
DPAPWR_FB_DIV
R9436 24.9K 1% 1/16W MF-LF 402

Port A 3.3V Power Switch

DP_PWR must be S4 to wake from T29 devices.

CRITICAL U9480 TPS2051B SOT23 OUT OC* IN EN GND

T29_A_HV_EN
PP3V3_S5
SMC_S4_WAKESRC_EN

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 20% 10V CERM 402
C9481 0.1UF 20% 10V CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

T29_A_BIAS

CRITICAL C9435 0.1UF 20% 10V CERM 402
CRITICAL U9435 ZXRE060A SOT353 PGND GND FB IN OUT
C9436 1UF 10% 10V X5R 402

DisplayPort/T29 A Connector

L9400 FERR-120-OHM-3A 0603
PP3V3R3V_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

PP3V3R3V_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=18V

C9400 0.01UF 10% 50V X7R 402

Circuit threshold range: 2.877-2.941V (2.903V nominal)

C9490 0.1uF 10% 16V X5R 402
T29_A_BIAS_R

R9491 51 5% 1/20W MF 201
T29_A_BIAS VOLTAGE=3.3V

T29_D2R_C_P<0>
T29_D2R_C_N<0>

R9494 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/20W MF 201 SIGNAL_MODEL=EMPTY

T29 Dir DP Dir

R9403 12 5% 1/20W MF 201
R9404 12 5% 1/20W MF 201

GND_DPACONN_8
GND_DPACONN_14
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

T29DPA_ML_P<3>
T29DPA_ML_N<3>
T29: Unused

T29_A_BIAS_D2RN1
T29_A_BIAS_D2RP1

R9498 2.2K 5% 1/20W MF 201
R9499 2.2K 5% 1/20W MF 201

T29_D2R_C_P<1>
T29_D2R_C_N<1>

D9498 BAR90-02LRH TSLP-2-7
D9499 BAR90-02LRH TSLP-2-7

CRITICAL L9498 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY
CRITICAL L9499 650NH-5%-0.430MA-0.052OHM 0603 SIGNAL_MODEL=EMPTY

T29DPA_D2R1_AUXCH_P
T29DPA_D2R1_AUXCH_N

CRITICAL GND_VOID=TRUE SIGNAL_MODEL=T29PIN (Both L's)
DP_A_EXT_AUXCH_P
DP_A_EXT_AUXCH_N

R9402 12 5% 1/20W MF 201
T29DPA_HPD_R

C9498 30PF 5% 50V CERM 402
C9499 30PF 5% 50V CERM 402
C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402

DPCONN_20_RC
R9401 12 5% 1/20W MF 201

T29DPA_HPD
T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC

R9452 1M 5% 1/16W MF-LF 402
R9451 1M 5% 1/16W MF-LF 402
C9494 330PF 10% 50V CERM 402
C9495 330PF 10% 50V CERM 402

DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/16W MF-LF 402

For J9400 T29 SMT pads (3, 5, 17 & 19):
GND_VOID=TRUE

CRITICAL J9400 DSPLYPRT-M97-1 F-RT-THSM

BOT ROW TH PINS		TOP ROW SM PINS
2	HOT_PLUG_DETECT	1 GND
4	CONFIG1	3 ML_LANE0P
6	CONFIG2	5 ML_LANE0N
8	GND	7 GND
10	ML_LANE3P	9 ML_LANE1P
12	ML_LANE3N	11 ML_LANE1N
14	GND	13 GND
16	AUX_CHP	15 ML_LANE2P
18	AUX_CHN	17 ML_LANE2N
20	DP_PWR	19 RETURN
SHIELD PINS		22 21

GND_DPACONN_1 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
R9405 12 5% 1/20W MF 201
DP Dir T29 Dir
T29DPA_ML_P<0>
T29DPA_ML_N<0>
T29: TX_0

GND_DPACONN_7 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
R9406 12 5% 1/20W MF 201
T29DPA_ML_P<1>
T29DPA_ML_N<1>
T29: LSX_R2P/P2R (P/N)

GND_DPACONN_13 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
R9407 12 5% 1/20W MF 201
T29DPA_ML_P<2>
T29DPA_ML_N<2>
T29: TX_1

GND_DPACONN_19 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=0V
L9408 FERR-120-OHM-3A 0603
R9408 12 5% 1/20W MF 201

GND_VOID=TRUE (Both C's)
C9470 0.47UF 20% 4V CERM-X5R-1 201
C9471 0.47UF 20% 4V CERM-X5R-1 201
C9472 0.47UF 20% 4V CERM-X5R-1 201
C9473 0.47UF 20% 4V CERM-X5R-1 201

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection on AC-coupled signals.

SYNC_MASTER=T29 SYNC_DATE=10/16/2016
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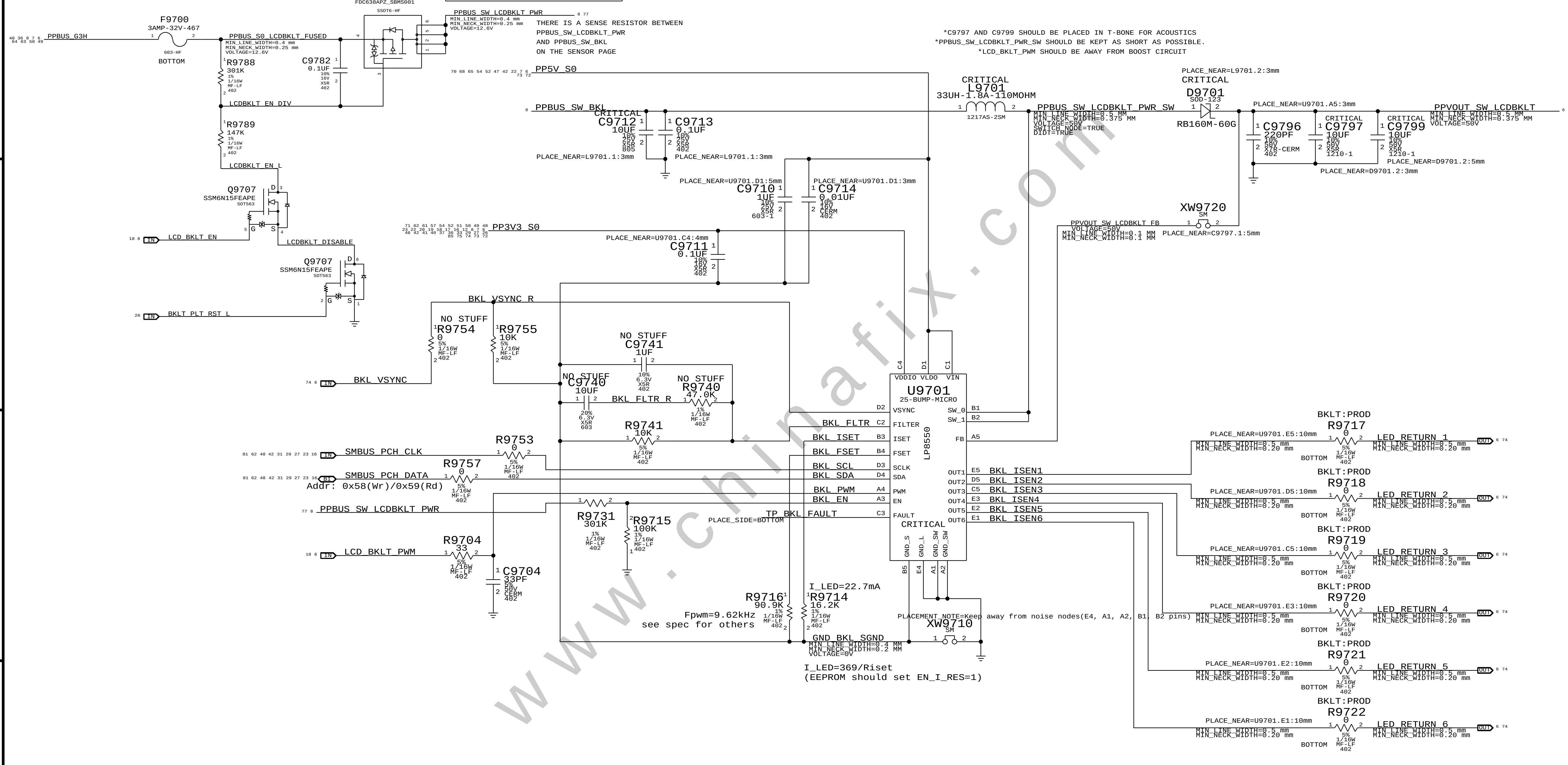
PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.65 A (EDP)



PPBUS_G3H
F9700
3AMP-32V-467
BOTTOM
PPBUS_S0_LCDBKLT_FUSED
CRITICAL
Q9706
FDC638APZ_SBMS001
PPBUS_SW_LCDBKLT_PWR
THERE IS A SENSE RESISTOR BETWEEN
PPBUS_SW_LCDBKLT_PWR
AND PPBUS_SW_BKL
ON THE SENSOR PAGE
R9788 301K
C9782 0.1UF
LCDBKLT_EN_DIV
R9789 147K
LCDBKLT_EN_L
Q9707 SSM6N15FEAPE
LCD_BKLT_EN
LCDBKLT_DISABLE
BKLT_PLT_RST_L
PP5V_S0
PPBUS_SW_BKL
CRITICAL
C9712 10UF
C9713 0.1UF
PLACE_NEAR=L9701.1:3mm
*C9797 AND C9799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS
*PPBUS_SW_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.
*LCD_BKLT_PWM SHOULD BE AWAY FROM BOOST CIRCUIT
CRITICAL
L9701
33UH-1.8A-110MOHM
PPBUS_SW_LCDBKLT_PWR_SW
D9701
RB160M-60G
PPVOUT_SW_LCDBKLT
C9796 220PF
C9797 10UF
C9799 10UF
C9710 1UF
C9714 0.01UF
XW9720
PPVOUT_SW_LCDBKLT_FB
PP3V3_S0
C9711 0.1UF
BKL_VSYNC_R
NO STUFF
R9754 0
R9755 10K
NO STUFF
C9741 1UF
BKL_VSYNC
NO STUFF
C9740 10UF
BKL_FLTR_R
NO STUFF
R9740 47.0K
R9741 10K
U9701
25-BUMP-MICRO
LP8550
VDDIO VLDO VIN
VSYNC SW_0 SW_1 FILTER ISET FB SCLK SDA PWM EN FAULT
OUT1 OUT2 OUT3 OUT4 OUT5 OUT6
CRITICAL
GND_S GND_L GND_SW GND_SW
BKL_FLTR
BKL_ISET
BKL_FSET
BKL_SCL
BKL_SDA
BKL_PWM
BKL_EN
TP_BKL_FAULT
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
SMBUS_PCH_CLK
R9753 0
SMBUS_PCH_DATA
R9757 0
Addr: 0x58(Wr)/0x59(Rd)
PPBUS_SW_LCDBKLT_PWR
R9731 301K
R9715 100K
PLACE_SIDE=BOTTOM
LCD_BKLT_PWM
R9704 33
C9704 33PF
R9716 90.9K
Fpwm=9.62kHz
see spec for others
I_LED=22.7mA
R9714 16.2K
PLACEMENT_NOTE=Keep away from noise nodes(E4, A1, A2, B1, B2 pins)
XW9710
GND_BKL_SGND
I_LED=369/Riset
(EEPROM should set EN_I_RES=1)
BKLT:PROD
R9717 0
LED_RETURN_1
R9718 0
LED_RETURN_2
R9719 0
LED_RETURN_3
R9720 0
LED_RETURN_4
R9721 0
LED_RETURN_5
R9722 0
LED_RETURN_6

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=VEMURI_K90I SYNC_DATE=06/25/2010

PAGE TITLE
LCD Backlight Driver

Apple Inc.

DRAWING NUMBER SIZE D
REVISION
BRANCH

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 30
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 26
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_AGTL	PM_THRMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 68
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 68
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 68
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC_MASTER=ANNE_K90I SYNC_DATE=06/08/2010

PAGE TITLE: CPU Constraints

Apple Inc.

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines
per Huron River SFF DG rev1.0 (#438297).
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQ to DQS matching per byte lane should be within 0.127mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 27 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 27 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 27 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 28 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 28 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 28 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 28

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 17 75 81
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 17 75 81
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	18 74
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	6 18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	6 18 74
	LVDS_90D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
	LVDS_90D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<3..0>	8
T21	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<3..0>	8
T21	LVDS_90D	LVDS	TP_LVDS_IG_B_CLKP	6 8 18
T21	LVDS_90D	LVDS	TP_LVDS_IG_B_CLKN	6 8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_P	6 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	16 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_N	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	16 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_N	16 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_RC_P	42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_RC_N	42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_RC_P	42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_RC_N	42
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 43
USB_EXTA	USB_85D	USB	USB_EXTA_N	24 43
USB_EXTB	USB_85D	USB	USB_EXTB_P	24 43
	USB_85D	USB	USB_EXTB_N	24 43
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 24
	USB_85D	USB	USB_EXTC_N	8 24
USB_EXTD	USB_85D	USB	USB_T29A_P	8 24
T21	USB_85D	USB	USB_T29A_N	8 24
T21	USB_85D	USB	T29_A_RSVD_P	8 75
	USB_85D	USB	T29_A_RSVD_N	8 75
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	18 32
	USB_85D	USB	USB_CAMERA_N	18 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 32
	USB_85D	USB	USB_CAMERA_CONN_N	6 32
USB_BT	USB_85D	USB	USB_BT_P	6 24 32
USB_BT	USB_85D	USB	USB_BT_N	6 24 32
USB_TPAD	USB_85D	USB	USB_TPAD_P	24 53
	USB_85D	USB	USB_TPAD_N	24 53
USB_IR	USB_85D	USB	USB_IR_P	24 44
	USB_85D	USB	USB_IR_N	24 44
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	
	USB_85D	USB	USB_SDCARD_N	
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_P	8
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_N	8
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 26
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 26 47
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 26
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	26 45
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 26 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 27 29 31 42 48 62 77
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 27 29 31 42 48 62 77
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	57
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 32
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	16 32
	PCIE_85D	PCIE	PCIE_AP_D2R_N	16 32
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	6 32
	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	32
	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	32
	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MP	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MN	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 32
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 39
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDP	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDN	8 16
U39	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<1>	6
U40	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<2>	6
U37	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<5>	6
U38	CPU_27P45	CPU_COMP	TP_PCH_VSS_NCTF<7>	
U39	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<9>	6 81
U40	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<9>	6 81
U41	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<11>	6
U42	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<12>	6
U43	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<15>	6
U44	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<17>	6
U45	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<19>	6
U46	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<21>	6
U47	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<22>	
U48	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<25>	6
U49	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<27>	6
U50	CPU_27P45	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
U262	DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	
U263	DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 75
U263		DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	75
U265		DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	75
U264	DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 17 75 80
U265	DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 17 75 80
U267		DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	75
U268		DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	75
U267	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	
U268	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	
U269	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	
U270	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	
U271	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 34
U271	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 34
U272		PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	34
U274		PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	34
U270	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 34
U275	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 34
U272		PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	34
U274		PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	34
U275	PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 34
U280	PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 34

Clock Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
U281	SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 26
U282	SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 26
U283		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
U284		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	26 37
U285		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
U286	SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	26 34
U287		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	34

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	33 37
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>	33 37
CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD	33 37
CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK	33 37
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>	33
CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD	33
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK	33
CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK_L	33

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 39 41
FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 41
FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 41
FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 41

Port 2 Not Used

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
1	T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	75
2	T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	75
3	T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	75
4	T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	75
5		T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	75
6		T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	75
7	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	75 76
8	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	75 76
9	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	75 76
10	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	75 76
11		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	76
12		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	76
13		T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	75
14		T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	75
15		T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	75
16		T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	75
17	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	75 83
18	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	75 83
19	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	75
20	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	75
21	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	75
22	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	75
23		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	75
24		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	75
25		T29DP_80D	T29DP	T29DPA_ML_P<3..0>	75 76
26		T29DP_80D	T29DP	T29DPA_ML_N<3..0>	75 76
27		T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	75 76
28		T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	75 76
29		T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	75 76
30		T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	75 76
31	T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
32	T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
33	T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
34	T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
35		T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
36		T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
37	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
38	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
39	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
40	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
41		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
42		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
43		T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
44		T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
45		T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
46		T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
47	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	83
48	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	83
49	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
50	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
51	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
52	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
53		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
54		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
55		T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
56		T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
57		T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
58		T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
59		T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
60		T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
162		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	8 34
161		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	8 34
163	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	34
164	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	34
165		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	8 17 34
166		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	8 17 34
167	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	34
168	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	34
169		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	8 34
170		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	8 34
171	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	34
172	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	34
174		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	8 17 34
173		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	8 17 34
175	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	34
176	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	34
177		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
178		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
179		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
180		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
181		T29_I2C_55S	T29_I2C	I2C_T29_SCL	34 48 75
182		T29_I2C_55S	T29_I2C	I2C_T29_SDA	34 48 75
183	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	34
184	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	34
185	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	34
186	T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	34
187		T29DP_80D	T29DP	T29_R2D_C_P<3..0>	8 34 75
188		T29DP_80D	T29DP	T29_R2D_C_N<3..0>	8 34 75
189		T29DP_100D	T29DP	T29_D2R_P<3..0>	8 34 75
190		T29DP_100D	T29DP	T29_D2R_N<3..0>	8 34 75

Only used on hosts supporting T29 video-in

SYNC_MASTER=Master SYNC_DATE=06/21/2010

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1TO1_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	6 32 45 48 51
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	6 32 45 48 51
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 45 48 63 64
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 45 48 63 64
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	45 48
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	64
	1TO1_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	64
	1TO1_DIFFPAIR		CHGR_CSO_N	64

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	38
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	38
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N	42
L291	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P	42
L290	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N	42
L293	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P	42
L296	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N	42
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
L287 SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
L288	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	34 51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29THMSNS_D2_P	51
	THERM_1TO1_55S	THERM	T29THMSNS_D2_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
L249 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	65
L250	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	65
L257 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P	68 69
L251	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N	68 69
L253 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	
L254	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	
L256 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
L255	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
L281 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	
L282	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	
L283 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
L284	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
L285 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
L286	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N	
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P	
L292 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	
L291	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	
L297	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_N	6 74
L294	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_P	6 74

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 32
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	50 64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	50 64
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	43
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	43
	USB_85D	USB	USB_LT2_N	43
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	6 60 61
1588 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N	60
1590 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P	60
1592 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N	60
1594 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P	60
1596 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N	60
1598 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P	60
1600 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R	57 60
1597 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R	57 60
1599 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R	57 60
1601 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R	57 60
1603 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L	57 60
1605 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L	57 60
1611 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P	60
1612 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N	60
1613 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	60
1614 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	60
1615 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P	60
1616 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N	60
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
	SB_POWER		PP3V3_S5	6 7 8 11 12 13 20 21 22 24 26 30 45 58 71 72 73 74 76 48 49 50
	SB_POWER		PP3V3_S0	6 7 8 12 16 17 18 19 20 22 25 26 27 29 31 36 37 40 41 52 54
	SB_POWER		PP1V5_S3RS0	6 7 10 12 15 30 72 73 57 61 62 71
	GND		GND	71 73 74 77

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	ISL10	N	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	ISL3,ISL4,ISL9	Y	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SE	ISL10	N	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	ISL3,ISL4,ISL9	Y	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.235 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

SYNC_MASTER=ANNE_K90I SYNC_DATE=06/08/2010

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