

SCHEM, MBP 15" MLB

08/18/2008

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD DATE	ENG APPD DATE
?		?	?	?	?

Page	Contents	Sync	Date
1	Table of Contents	N/A	N/A
2	System Block Diagram	T18_MLB	12/12/2007
3	Power Block Diagram	T18_MLB	12/12/2007
4	Power Block Diagram	N/A	N/A
5	BOM Configuration	N/A	N/A
6	JTAG Scan Chain	DDR	07/22/2008
7	Functional / ICT Test	N/A	N/A
8	Power Aliases	(MASTER)	(MASTER)
9	Signal Aliases	(MASTER)	(MASTER)
10	CPU FSB	M87_MLB	10/17/2007
11	CPU Power & Ground	M87_MLB	10/17/2007
12	CPU Decoupling & VID	M87_MLB	10/17/2007
13	eXtended Debug Port(MiniXDP)	M99_MLB	01/08/2008
14	MCP CPU Interface	T18_MLB	06/18/2008
15	MCP Memory Interface	T18_MLB	06/18/2008
16	MCP Memory Misc	T18_MLB	06/18/2008
17	MCP PCIe Interfaces	T18_MLB	06/18/2008
18	MCP Ethernet & Graphics	T18_MLB	06/18/2008
19	MCP PCI & LPC	T18_MLB	06/18/2008
20	MCP SATA & USB	T18_MLB	06/18/2008
21	MCP HDA & MISC	T18_MLB	06/18/2008
22	MCP Power & Ground	T18_MLB	06/18/2008
23	MCP79 A01 Silicon Support	T18_MLB	03/31/2008
24	MCP Standard Decoupling	T18_MLB	06/18/2008
25	MCP Graphics Support	AMASON_M98_MLB	06/18/2008
26	SB Misc	T18_MLB	12/17/2007
27	FSB/DDR3/FRAMEBUF Vref Margining	DDR	07/22/2008
28	DDR3 SO-DIMM Connector A	DDR	07/22/2008
29	DDR3 SO-DIMM Connector B	DDR	07/22/2008
30	DDR3 Support	T18_MLB	06/18/2008
31	Right Clutch Connector	YITE_M98_MLB	07/02/2008
32	ExpressCard Connector	YITE_M98_MLB	07/02/2008
33	Ethernet PHY (RTL8211CL)	SUMA_M98_MLB	07/01/2008
34	Ethernet & AirPort Support	SUMA_M98_MLB	07/01/2008
35	Ethernet Connector	SUMA_M98_MLB	07/01/2008
36	FireWire LLC/PHY (FW643)	SENSOR	08/14/2008
37	FireWire Port Power	SENSOR	08/14/2008
38	FireWire Ports	SENSOR	08/14/2008
39	SATA Connectors	CHANG_M98_MLB	07/01/2008
40	External USB Connectors	AMASON_M98_MLB	07/02/2008
41	Front Flex Support	CHANG_M98_MLB	07/01/2008
42	SMC	T18_MLB	06/18/2008
43	SMC Support	AMASON_M98_MLB	06/18/2008
44	LPC+SPI Debug Connector	CHANG_M98_MLB	07/01/2008
45	M98 SMBus Connections	DDR	07/22/2008

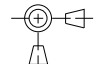
Page	Contents	Sync	Date
46	Current & Voltage Sensing	SENSOR	08/14/2008
47	Current Sensing	SENSOR	08/14/2008
48	Thermal Sensors	SENSOR	08/14/2008
49	Fan Connectors	M87_MLB	10/17/2007
50	WELLSPRING 1	AMASON_M98_MLB	06/18/2008
51	WELLSPRING 2	PWRSQNC	05/12/2008
52	Sudden Motion Sensor (SMS)	SENSOR	08/14/2008
53	SPI ROM	CHANG_M98_MLB	07/01/2008
54	AUDIO:CODEC	AUDIO	07/09/2008
55	AUDIO: LINE IN	AUDIO	07/09/2008
56	AUDIO: HEADPHONE AMP	AUDIO	07/09/2008
57	AUDIO:SPEAKER AMP	AUDIO	07/09/2008
58	AUDIO: JACKS	AUDIO	07/09/2008
59	AUDIO: JACK TRANSLATORS	AUDIO	07/09/2008
60	DC-In & Battery Connectors	T18_MLB	12/06/2007
61	PBus Supply & Battery Charger	M99_MLB	12/10/2007
62	IMVP6 CPU VCore Regulator	M87_MLB	10/17/2007
63	5V / 3.3V Power Supply	M99_MLB	01/09/2008
64	1.5V DDR3 Supply	M99_MLB	12/13/2007
65	1.05V / MCP Core Regulator	M99_MLB	01/08/2008
66	CPU VTT Power Supply	M99_MLB	12/14/2007
67	Misc Power Supplies	M99_MLB	12/14/2007
68	Power Control	PWRSQNC	05/12/2008
69	Power FETs	PWRSQNC	05/12/2008
70	NV G96 PCI-E	MUXGFX	07/10/2008
71	NV G96 Core/FB Power	MUXGFX	07/10/2008
72	NV G96 Frame Buffer I/F	MUXGFX	07/10/2008
73	GDDR3 Frame Buffer A (Top)	MUXGFX	07/10/2008
74	GDDR3 Frame Buffer B (Top)	MUXGFX	07/10/2008
75	NV G96 GPIO/MIO/Misc	MUXGFX	07/10/2008
76	G96 GPIOs & Straps	MUXGFX	07/09/2008
77	NV G96 Video Interfaces	MUXGFX	07/10/2008
78	GPU (G84M) Core Supply	M87_MLB	10/17/2007
79	LVDS Display Connector	MUXGFX	02/25/2008
80	Muxed Graphics Support	MUXGFX	07/10/2008
81	DisplayPort Connector	MUXGFX	07/10/2008
82	1.1V / 1V8 FB Power Supply	MUXGFX	07/10/2008
83	Graphics MUX (GMUX)	MUXGFX	07/10/2008
84	LCD BACKLIGHT DRIVER	YITE_M98_MLB	07/02/2008
85	LCD Backlight Support	YITE_M98_MLB	07/02/2008
86	Misc Power Supplies	MUXGFX	02/01/2008
87	CPU/FSB Constraints	MUXGFX	02/18/2008
88	Memory Constraints	MUXGFX	02/18/2008
89	MCP Constraints 1	MUXGFX	02/18/2008
90	MCP Constraints 2	MUXGFX	02/18/2008

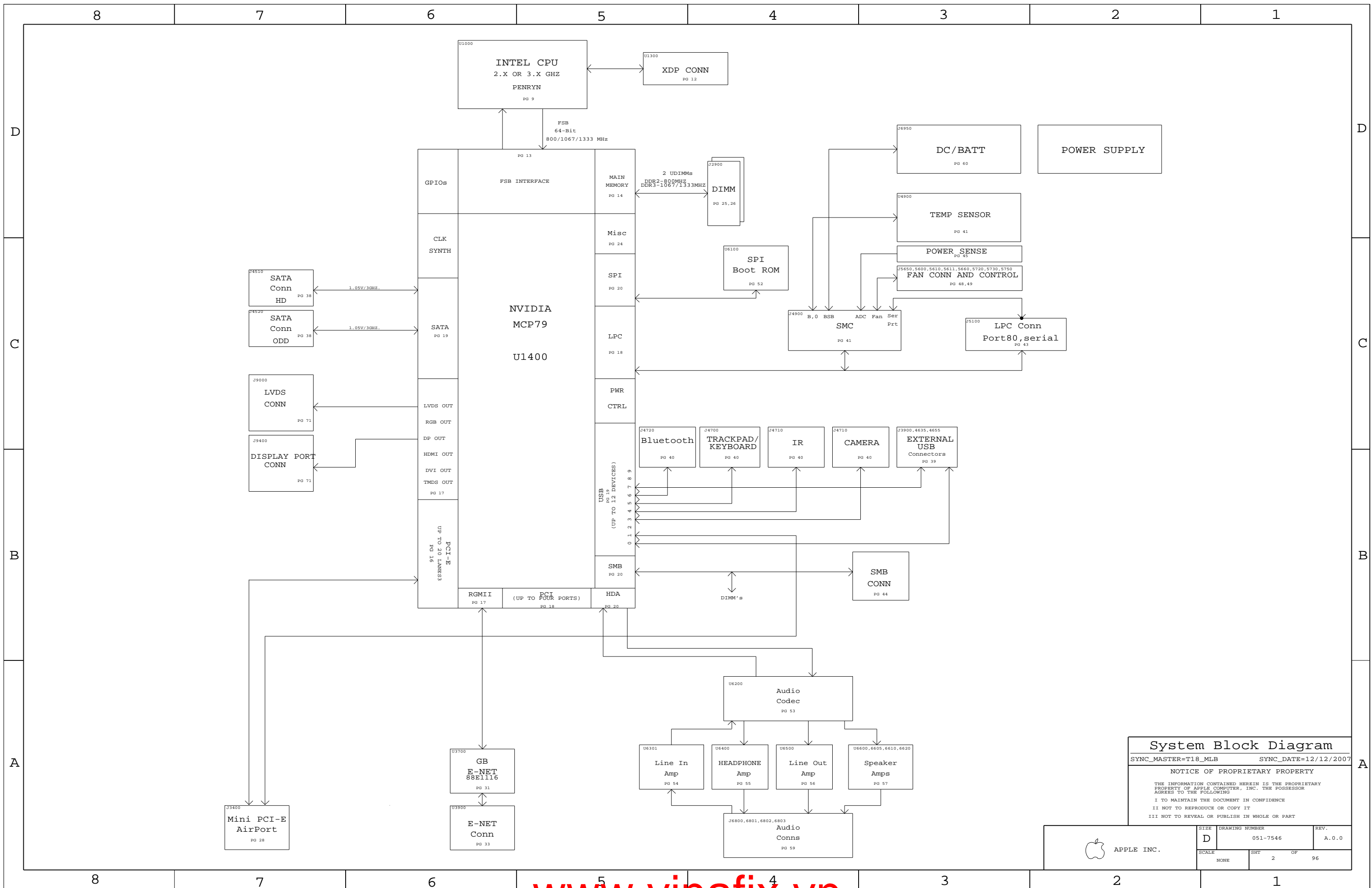
Page	Contents	Sync	Date
91	Ethernet Constraints	MUXGFX	02/18/2008
92	FireWire Constraints	MUXGFX	02/18/2008
93	SMC Constraints	MUXGFX	02/18/2008
94	GPU (G96) Constraints	MUXGFX	02/18/2008
95	Project Specific Constraints	MUXGFX	02/21/2008
96	PCB Rule Definitions	M99_MLB	01/22/2008

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-7546	1	SCHEM, FIBBO, M98	SCH	CRITICAL	
820-2330	1	PCB, FIBBO, M98	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST MODIFIED=Mon Aug 18 01:48:34 2008

DIMENSIONS ARE IN MILLIMETERS		METRIC		APPLE INC.	
XX :	_____	DRAPTER	DESIGN CK	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING: I. TO MAINTAIN THE DOCUMENT IN CONFIDENCE II. NOT TO REPRODUCE OR COPY IT III. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART	
X.XX :	_____	ENG APPD	MFG APPD		
X.XXX :	_____	QA APPD	DESIGNER		
ANGLES :	_____	RELEASE	SCALE		
DO NOT SCALE DRAWING		NONE		TITLE	
 THIRD ANGLE PROJECTION		MATERIAL/FINISH NOTED AS APPLICABLE		DRAWING NUMBER	
		SIZE D		051-7546	
				REV. A.0.0	
				SHT 1 OF 96	



System Block Diagram

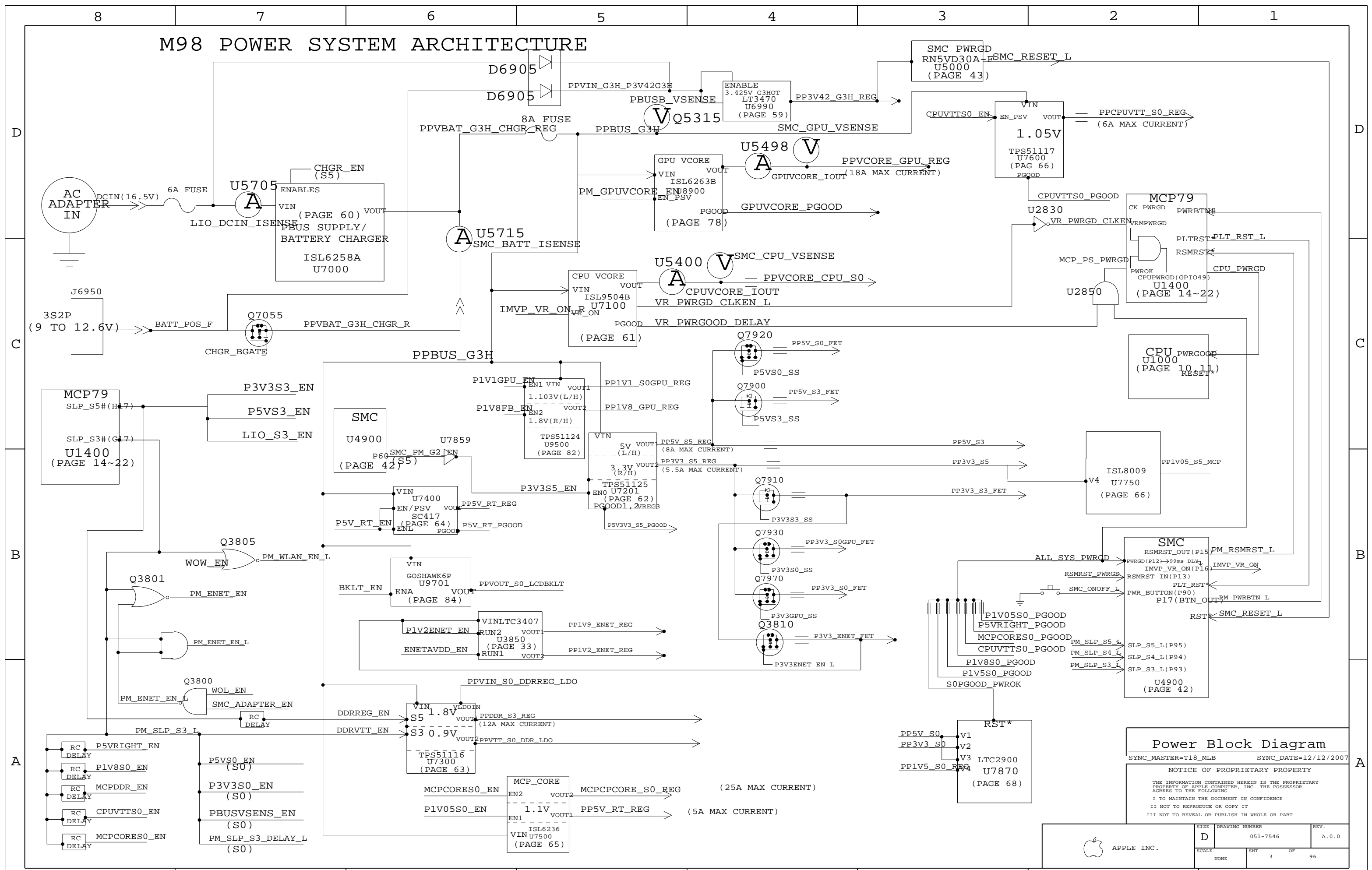
SYNC_MASTER=T18_MLB SYNC_DATE=12/12/2007

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SCALE	SHT	OF	
NONE	2	96	

M98 POWER SYSTEM ARCHITECTURE



Power Block Diagram

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SCALE	NONE	SHT	3 OF 96

8

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D

D

C

C

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B

A

A

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7

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1

Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	4	96

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9334	PCBA, 2.4GHZ, 256SAM_VRAM, M98	M98_COMMON, EEE_OZA, CPU_2_4GHZ, FB_256_SAMSUNG
630-9335	PCBA, 2.4GHZ, 256HYN_VRAM, M98	M98_COMMON, EEE_OZB, CPU_2_4GHZ, FB_256_HYNIX
630-9336	PCBA, 2.5GHZ, 512SAM_VRAM, M98	M98_COMMON, EEE_OZC, CPU_2_5GHZ, FB_512_SAMSUNG
630-9337	PCBA, 2.5GHZ, 512QIM_VRAM, M98	M98_COMMON, EEE_OZD, CPU_2_5GHZ, FB_512_QIMONDA
630-9585	PCBA, 2.8GHZ, 512SAM_VRAM, M98	M98_COMMON, EEE_2NH, CPU_2_8GHZ, FB_512_SAMSUNG
630-9586	PCBA, 2.8GHZ, 512QIM_VRAM, M98	M98_COMMON, EEE_2NJ, CPU_2_8GHZ, FB_512_QIMONDA

M98 BOM Groups

BOM GROUP	BOM OPTIONS
M98_COMMON	ALTERNATE, COMMON, M98_COMMON1, M98_COMMON2, M98_COMMON3, M98_DEBUG, M98_PROGPARTS
M98_COMMON1	ONEWIRE_PU, ISL6258A, MEMRESET_HW, MEMRESET_MCP, MCP_B02, MCP_PROD, MCPSEQ_SMC
M98_COMMON2	BKLT_PLL_NOT, BMON_ENG, MIKEY, BOOT_MODE_USER, GPUVID_1P00V, MUXGFX
M98_COMMON3	DPMUX_EN_S0, DP_ESD, EG_PWRSEQ_HW, DP_CA_DET_EG_PLD, MCP_CS1_NO
M98_DEBUG	SMC_DEBUG_YES, XDP, LPCPLUS, VREFMRGN
M98_PROGPARTS	GMUX_PROG, BOOTROM_PROG, SMC_PROG, TPAD_PROG

BOM GROUP	BOM OPTIONS
FB_256_SAMSUNG	VRAM4, VRAM_256_SAMSUNG
FB_256_HYNIX	VRAM4, VRAM_256_HYNIX
FB_512_SAMSUNG	VRAM4, VRAM_512_SAMSUNG
FB_512_QIMONDA	VRAM4, VRAM_512_QIMONDA

Bar Code Labels / EEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZA]	CRITICAL	EEE_OZA
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZB]	CRITICAL	EEE_OZB
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZC]	CRITICAL	EEE_OZC
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:OZD]	CRITICAL	EEE_OZD
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2NH]	CRITICAL	EEE_2NH
826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:2NJ]	CRITICAL	EEE_2NJ

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3639	1	IC, PDC, SLB4N, FRQ, 2.4G, 25W, 1066, M0, 3M, BGA	U1000	CRITICAL	CPU_2_4GHZ
337S3640	1	IC, PDC, SLB4X, FRQ, 2.53G, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_5GHZ
338S0554	1	IC, GPU, 55nm, NV G96-GS, BGA969, LF	U8000	CRITICAL	
338S0570	1	IC, RTL8211CL, GIGE TRANSCEIVER, 48P TQFP	U3700	CRITICAL	
338S0523	1	IC, FW643-06, 1394B PHY/ONCI LINK/PCI-E, 12	U4100	CRITICAL	
338S0600	1	IC, GMCP, MCP79-B01, 35x35MM, BGA1437	U1400	CRITICAL	MCP_B01
338S0563	1	IC, SMC, HS8/2117, 9MMX9MM, TLP	U4900	CRITICAL	SMC_BLANK
341S2289	1	IC, SMC, DEVELOPMENT, M98	U4900	CRITICAL	SMC_PROG
335S0384	1	IC, 32MBIT 8-PIN SPI SERIAL FLASH, SO1CS	U6100	CRITICAL	BOOTROM_BLANK
341S2366	1	IC, EFI ROM, DEVELOPMENT, M98	U6100	CRITICAL	BOOTROM_PROG
341S2272	1	IC, HDCP ROM, NVG96, 8 PIN SOIC, LP, HF	U8770	CRITICAL	HDCP_YES
341S2384	1	IR, ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
338S0635	1	IC, GMCP, MCP79-B02, 35x35MM, BGA1437	U1400	CRITICAL	MCP_B02
341S2383	1	IC, PSOC +W/USB, 56PIN, MLF, M98	U5701	CRITICAL	TPAD_PROG
337S3641	1	IC, PDC, SLB43, FRQ, 2.8G, 35W, 1066, C0, 6M, BGA	U1000	CRITICAL	CPU_2_8GHZ
333S0482	4	IC, SGRAM, GDDR3, 16Mx32, 800MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_SAMSUNG
333S0483	4	IC, SGRAM, GDDR3, 16Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_256_HYNIX
333S0481	4	IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_SAMSUNG
333S0472	4	IC, SGRAM, GDDR3, 32Mx32, 900MHZ, 136 FBGA	U8400, U8450, U8500, U8550	CRITICAL	VRAM_512_QIMONDA

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Muratec alt to Samsung
353S1681	353S1294		ALL	LMV2011, ORAMP, ORM
152S0276	152S0683		ALL	Maplayers alt to Delta/Vishay
341S2367	341S2366		ALL	Macromia alt to SST
152S0876	152S0867		ALL	Maplayers alt to Delta
157S0058	157S0055		ALL	Delta alt to TOR Magnetics
353S2312	353S1466		ALL	INTERSEIL ALT TO INTERSEIL
514-0612	514-0607		ALL	FUSILINK RCVR ALT TO FUSION
514-0613	514-0608		ALL	FUSILINK RCVR ALT TO FUSION
152S0915	152S0796		ALL	Maplayers alt to Cytosol LTD

BOM Configuration

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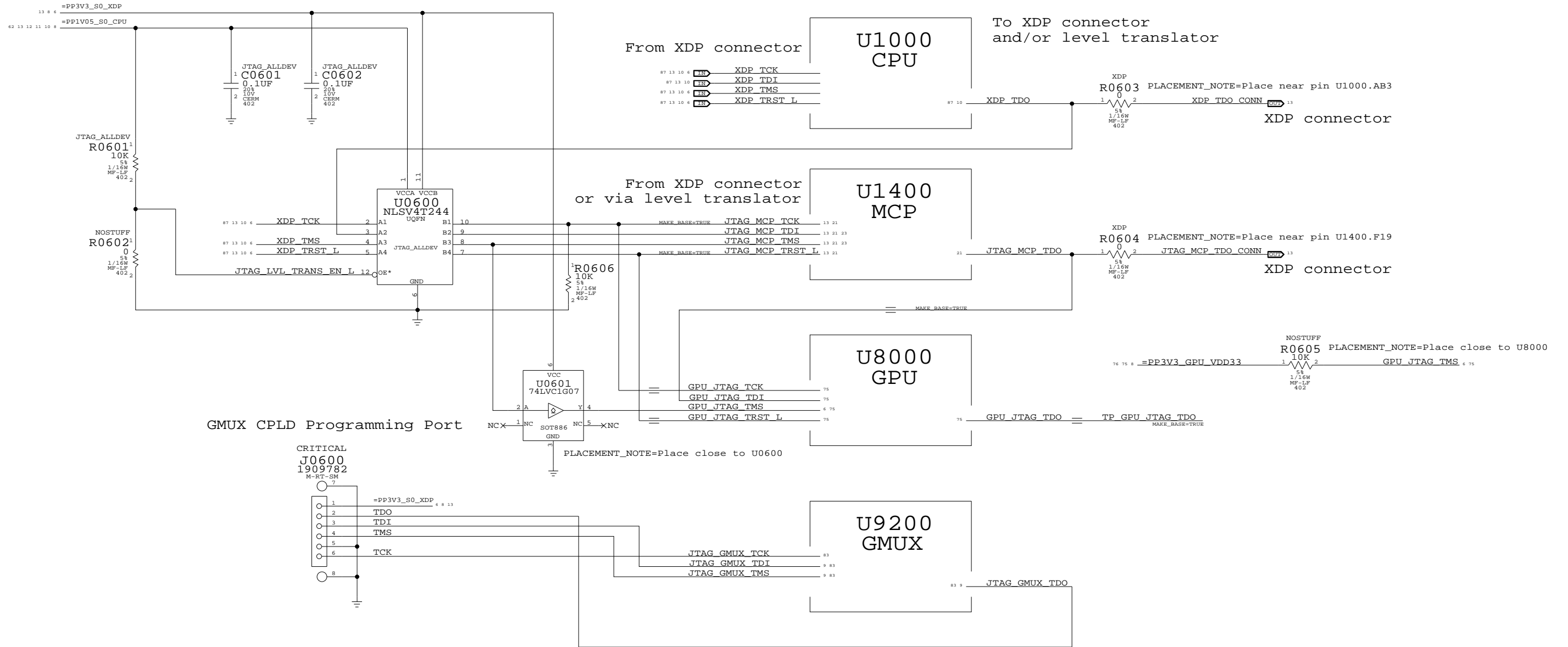
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	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		5	96

1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)



JTAG Scan Chain
 SYNC_MASTER=DDR SYNC_DATE=07/22/2008
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SCALE	SHT 6 OF 96		
NONE			

Functional Test Points

ICT Test Points

Fan Connectors

FUNC_TEST

TRUE	=PP5V_S0_FAN_LT	8 49	3 TPs per Fan
TRUE	FAN_LT_PWM	49	
TRUE	FAN_LT_TACH	49	
TRUE	FAN_RT_PWM	49	5 TPs per Fan
TRUE	FAN_RT_TACH	49	
TRUE	GND	49	

LVDS Connectors

FUNC_TEST

TRUE	=PP3V3_S0_DDC_LCD	8 76 79
TRUE	PP3V3_SW_LCD	79
TRUE	BKL_SYNC	79 84
TRUE	LVDS_DDC_CLK	79 80
TRUE	LVDS_DDC_DATA	79 80
TRUE	LVDS_CONN_A_DATA_N<0>	79 80 94
TRUE	LVDS_CONN_A_DATA_P<0>	79 80 94
TRUE	LVDS_CONN_A_DATA_N<1>	79 80 94
TRUE	LVDS_CONN_A_DATA_P<1>	79 80 94
TRUE	LVDS_CONN_A_DATA_N<2>	79 80 94
TRUE	LVDS_CONN_A_DATA_P<2>	79 80 94
TRUE	LVDS_CONN_A_CLK_F_N	79 94
TRUE	LVDS_CONN_A_CLK_F_P	79 94
TRUE	LVDS_CONN_B_DATA_N<0>	79 80 94
TRUE	LVDS_CONN_B_DATA_P<0>	79 80 94
TRUE	LVDS_CONN_B_DATA_N<1>	79 80 94
TRUE	LVDS_CONN_B_DATA_P<1>	79 80 94
TRUE	LVDS_CONN_B_DATA_N<2>	79 80 94
TRUE	LVDS_CONN_B_DATA_P<2>	79 80 94
TRUE	LVDS_CONN_B_CLK_F_N	79 94
TRUE	LVDS_CONN_B_CLK_F_P	79 94
TRUE	LED_RETURN_1	79 84
TRUE	LED_RETURN_2	79 84
TRUE	LED_RETURN_3	79 84
TRUE	LED_RETURN_4	79 84
TRUE	LED_RETURN_5	79 84
TRUE	LED_RETURN_6	79 84

Speaker Connectors

FUNC_TEST

TRUE	BI_MIC_LO	58 59
TRUE	BI_MIC_SHIELD	58 59
TRUE	BI_MIC_HI	58 59
TRUE	SPKRCONN_L_P_OUT	57 58 95
TRUE	SPKRCONN_L_N_OUT	57 58 95
TRUE	SPKRCONN_R_P_OUT	57 58 95
TRUE	SPKRCONN_R_N_OUT	57 58 95
TRUE	SPKRCONN_S_P_OUT	57 58 95
TRUE	SPKRCONN_S_N_OUT	57 58 95
TRUE	GND	

6 TPs

SATA ODD Connectors

FUNC_TEST

TRUE	PP5V_SW_ODD	39	4 TPs
TRUE	SMC_ODD_DETECT	39 42	
TRUE	SATA_ODD_R2D_P	39 89	
TRUE	SATA_ODD_R2D_N	39 89	
TRUE	SATA_ODD_D2R_C_N	39 89	5 TPs
TRUE	SATA_ODD_D2R_C_P	39 89	
TRUE	GND		

POWER RAILS

TRUE	PM_SLP_S3_L	21 34 37 42 44 68 81 83
TRUE	PPBUS_G3H	8 46
TRUE	PPBUS_CPU_IMVP_ISNS	8
TRUE	PP3V42_G3H	7 8 43
TRUE	PP5V_S3	8
TRUE	PP5V_S0	8
TRUE	PPVCORE_S0_CPU	8
TRUE	PPVCORE_S0_MCP_REG	8
TRUE	PPVCORE_S0_MCP	8
TRUE	PP3V3_S5	8 95
TRUE	PP3V3_S3	8
TRUE	PP3V3_S0	8 95
TRUE	PP2V5_S0	8
TRUE	PP1V2_S0	8
TRUE	PP1V8_S0	8
TRUE	PP1V8R1V5_S3	8
TRUE	PP1V8R1V5_S0_FET	8
TRUE	PPMCPDDR_ISNS	8
TRUE	PP1V05_S0_REG	8
TRUE	PP1V2R1V05_S5	8
TRUE	PPCPUVTT_S0	8
TRUE	PPCPUFSB_ISNS_R	8
TRUE	PP0V9R0V75_S0_DDRVTT	8
TRUE	PP1V2R1V05_ENET	8
TRUE	PP3V3_ENET_PHY	8
TRUE	PPVP_FW	8
TRUE	PP1V0_FW	8
TRUE	PP3V3_S0GPU	8
TRUE	PP1V1_S0GPU_REG	8
TRUE	PP1V8_S0GPU_ISNS	8
TRUE	PPVCORE_GPU	8
TRUE	PP1V8_S0GPU_ISNS_R	8
TRUE	PP3V3_S5_AVREF_SMC	42 43
TRUE	PPVOUT_S0_LCDBKLT	79 84
TRUE	PPDCIN_G3H	8
TRUE	PPVTTDDR_S3	8
TRUE	PP1V8_GPUIFPX	8

EXCARD Connector

FUNC_TEST

TRUE	USB2_EXCARD_CONN_N	32 95
TRUE	USB2_EXCARD_CONN_P	32 95
TRUE	PCIE_CLK100M_EXCARD_CONN_N	32 95
TRUE	PCIE_CLK100M_EXCARD_CONN_P	32 95
TRUE	PCIE_EXCARD_R2D_N	32 89 95
TRUE	PCIE_EXCARD_R2D_P	32 89 95
TRUE	PCIE_EXCARD_D2R_P	17 32 89
TRUE	PCIE_EXCARD_D2R_N	17 32 89
TRUE	PP3V3_S3_EXCARD_SWITCH	32
TRUE	PP3V3_S0_EXCARD_SWITCH	32
TRUE	PP1V5_S0_EXCARD_SWITCH	32
TRUE	PLT_RESET_SWITCH_L	32
TRUE	EXCARD_CPPE_L	32
TRUE	EXCARD_CPUSB_L	32
TRUE	EXCARD_CLKREO_CONN_L	32
TRUE	SMBUS_MCP_0_CLK	13 21 45 90
TRUE	SMBUS_MCP_0_DATA	13 21 45 90

CPU FSB NO_TESTS

NO_TEST

TRUE	FSB_A_L<31..3>	10 14 87
TRUE	FSB_ADS_L	10 14 87
TRUE	FSB_ADSTB_L<1..0>	10 14 87
TRUE	FSB_D_L<63..0>	10 14 87
TRUE	FSB_DINV_L<3..0>	10 14 87
TRUE	FSB_DSTB_L_N<3..0>	10 14 87
TRUE	FSB_DSTB_L_P<3..0>	10 14 87
TRUE	FSB_HIT_L	10 14 87
TRUE	FSB_HITM_L	10 14 87
TRUE	FSB_LOCK_L	10 14 87
TRUE	FSB_REQ_L<4..0>	10 14 87

IPD_FLEX_CONN

TRUE	PP3V3_S3_LDO	51
TRUE	PP18V5_S3	51
TRUE	TPAD_GND_F	7 51
TRUE	Z2_CS_L	50 51
TRUE	Z2_DEBUG3	50 51
TRUE	Z2_MOSI	50 51
TRUE	Z2_MISO	50 51
TRUE	Z2_SCLK	50 51
TRUE	Z2_BOOST_EN	51
TRUE	Z2_HOST_INTN	50 51
TRUE	Z2_BOOT_CFG1	50 51
TRUE	Z2_CLKIN	50 51
TRUE	Z2_KEY_ACT_L	50 51
TRUE	Z2_RESET	50 51
TRUE	PSOC_MISO	50 51
TRUE	PSOC_MOSI	50 51
TRUE	PSOC_SCLK	50 51
TRUE	SMBUS_SMC_A_S3_SDA	45 93
TRUE	SMBUS_SMC_A_S3_SCL	45 93
TRUE	PSOC_F_CS_L	50 51
TRUE	PICKB_L	50 51

KEYBOARD CONN

TRUE	PP3V42_G3H	7 8 43
TRUE	WS_KBD1	50
TRUE	WS_KBD2	50
TRUE	WS_KBD3	50
TRUE	WS_KBD4	50
TRUE	WS_KBD5	50
TRUE	WS_KBD6	50
TRUE	WS_KBD7	50
TRUE	WS_KBD8	50
TRUE	WS_KBD9	50
TRUE	WS_KBD10	50
TRUE	WS_KBD11	50
TRUE	WS_KBD12	50
TRUE	WS_KBD13	50
TRUE	WS_KBD14	50
TRUE	WS_KBD15_CAP	50
TRUE	WS_KBD16_NUM	50
TRUE	WS_KBD17	50
TRUE	WS_KBD18	50
TRUE	WS_KBD19	50
TRUE	WS_KBD20	50
TRUE	WS_KBD21	50
TRUE	WS_KBD22	50
TRUE	WS_KBD23	50
TRUE	WS_KBD_ONOFF_L	50
TRUE	WS_LEFT_SHIFT_KBD	50
TRUE	WS_LEFT_OPTION_KBD	50
TRUE	WS_CONTROL_KBD	50
TRUE	KBDLED_ANODE	51
TRUE	TPAD_GND_F	7 51

Functional / ICT Test

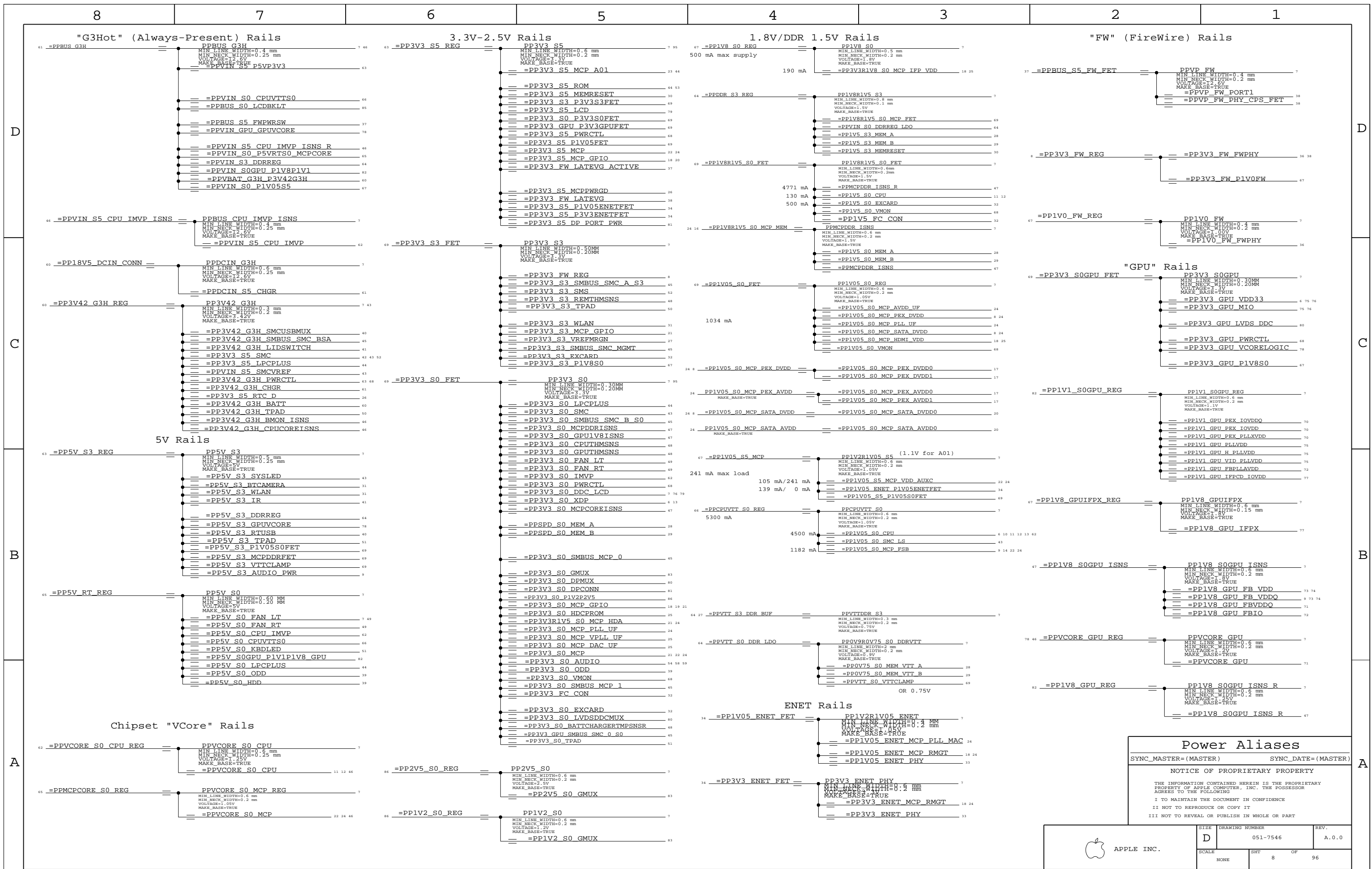
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D	051-7546	A.0.0
SCALE	SHT	OF
NONE	7	96



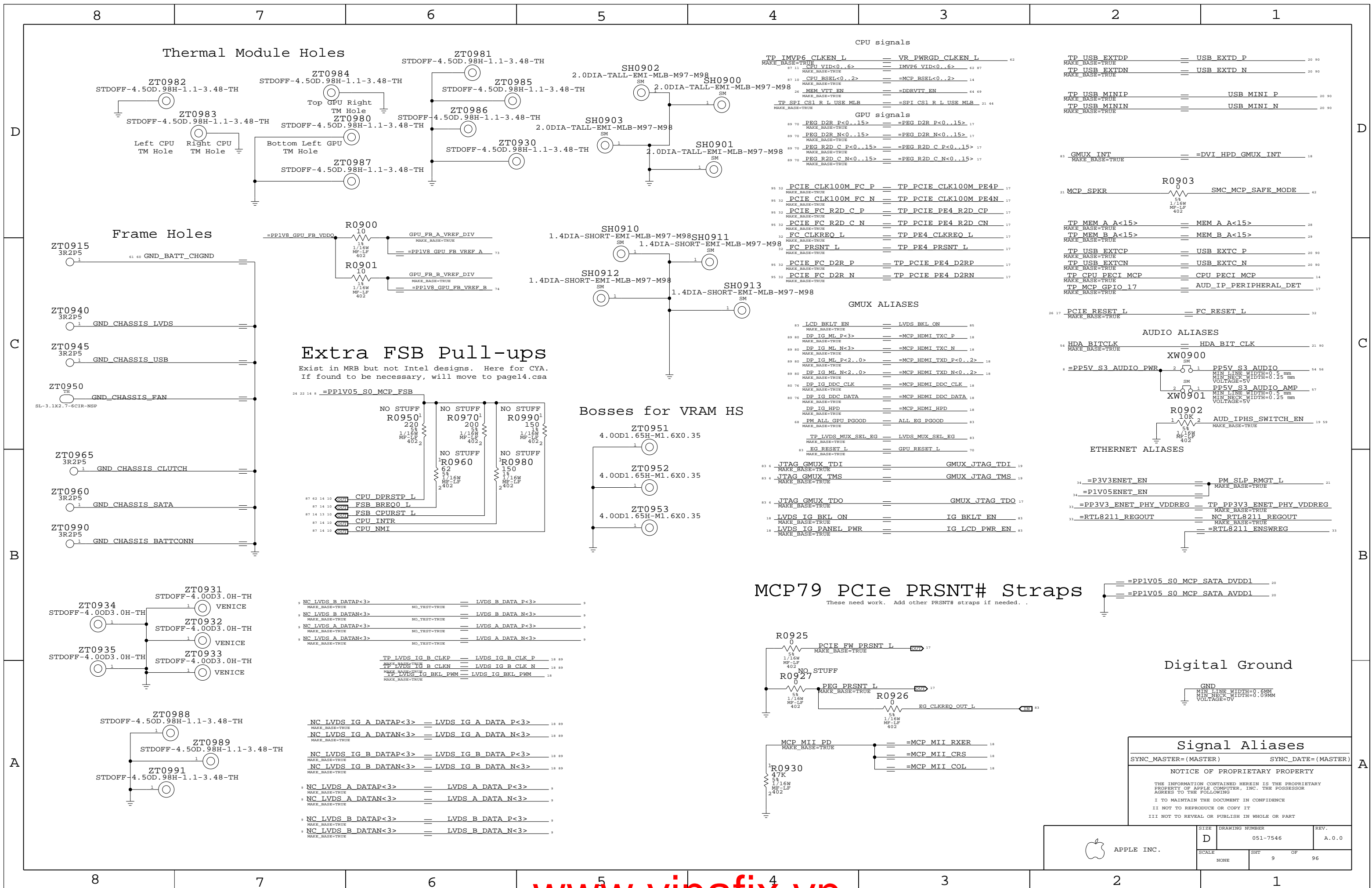
Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

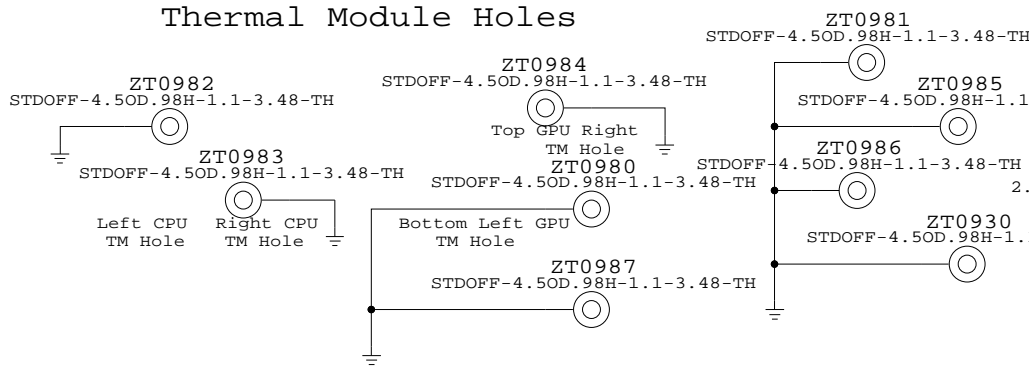
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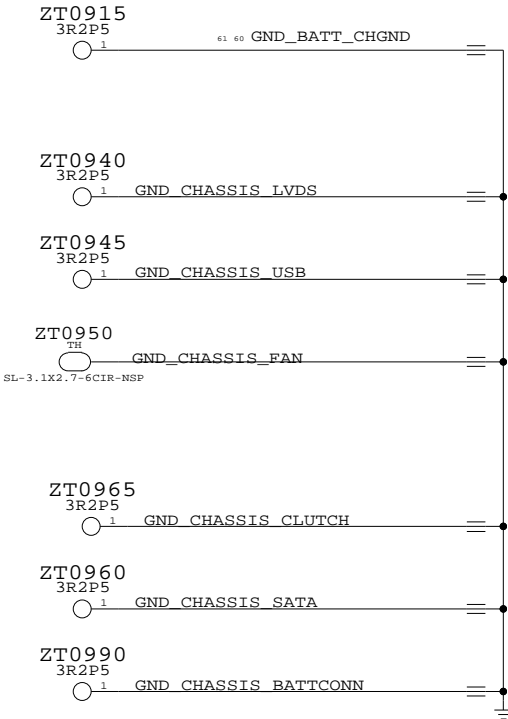
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	D	051-7546	A.0.0
SCALE	SHT	OF	
NONE	8	96	



Thermal Module Holes

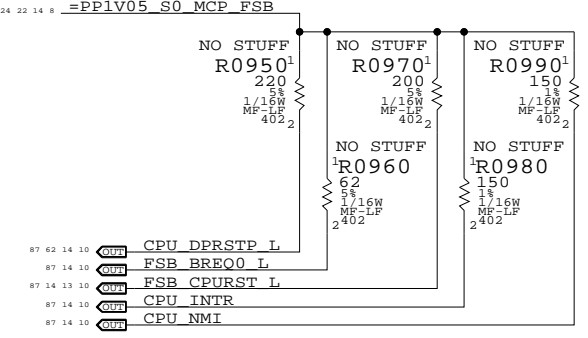


Frame Holes

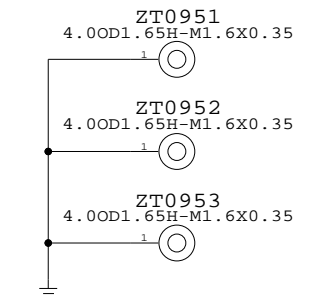


Extra FSB Pull-ups

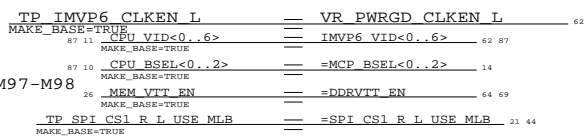
Exist in MRB but not Intel designs. Here for CYA. If found to be necessary, will move to page14.csa



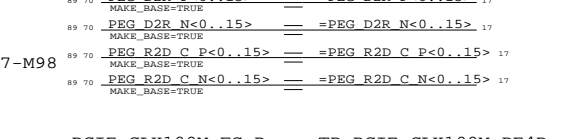
Bosses for VRAM HS



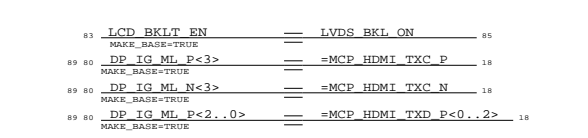
CPU signals



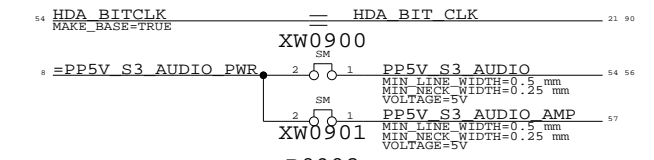
GPU signals



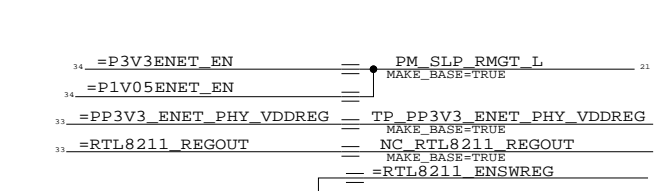
GMUX ALIASES



AUDIO ALIASES

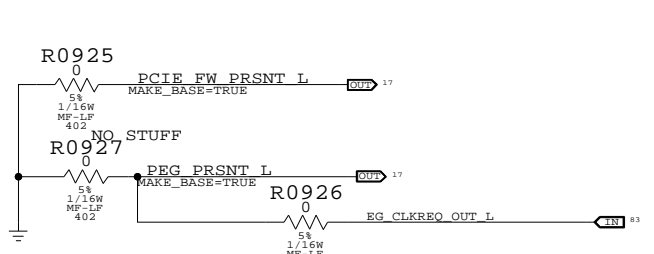


ETHERNET ALIASES

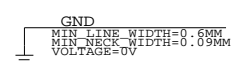


MCP79 PCIe PRSNT# Straps

These need work. Add other PRSNT# straps if needed.



Digital Ground



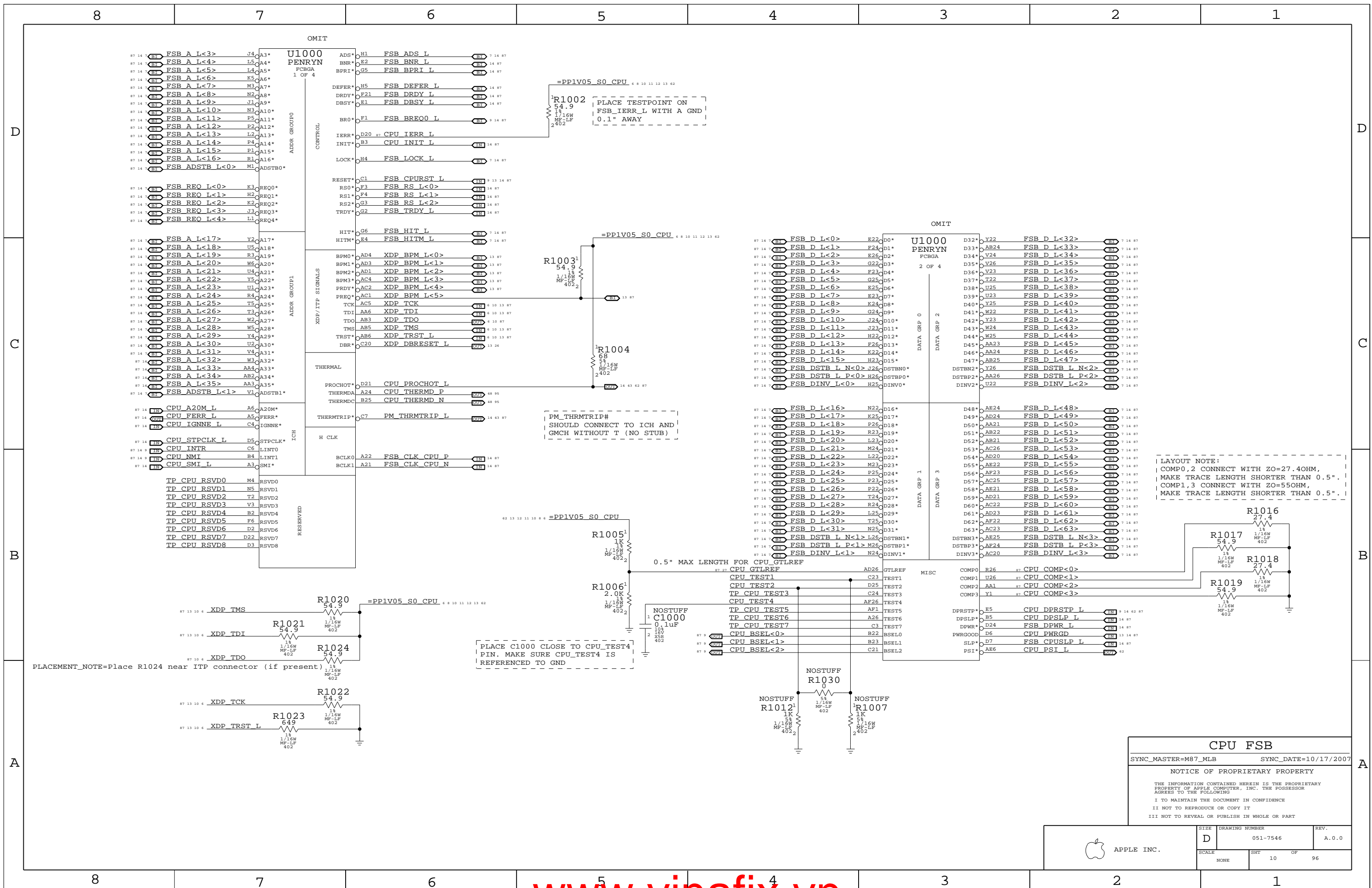
Signal Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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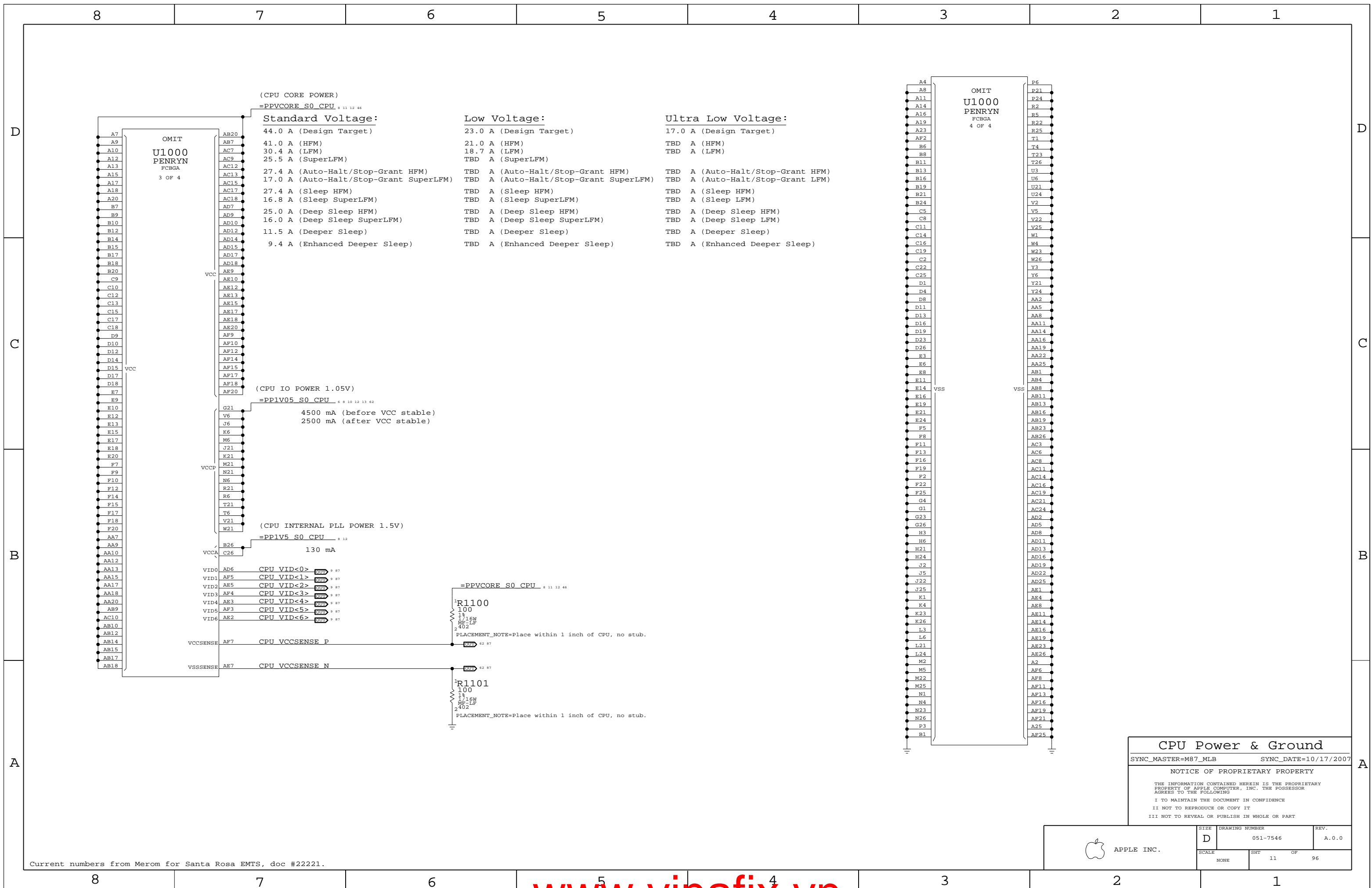
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	9 OF 96



LAYOUT NOTE:
 COMPO,2 CONNECT WITH ZO=27.4OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".
 COMPL,3 CONNECT WITH ZO=55OHM,
 MAKE TRACE LENGTH SHORTER THAN 0.5".

CPU FSB
 SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007
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	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	10		



(CPU CORE POWER)

=PPVCORE_S0_CPU_# 11 12 46

Standard Voltage:

- 44.0 A (Design Target)
- 41.0 A (HFM)
- 30.4 A (LFM)
- 25.5 A (SuperLFM)
- 27.4 A (Auto-Halt/Stop-Grant HFM)
- 17.0 A (Auto-Halt/Stop-Grant SuperLFM)
- 27.4 A (Sleep HFM)
- 16.8 A (Sleep SuperLFM)
- 25.0 A (Deep Sleep HFM)
- 16.0 A (Deep Sleep SuperLFM)
- 11.5 A (Deeper Sleep)
- 9.4 A (Enhanced Deeper Sleep)

Low Voltage:

- 23.0 A (Design Target)
- 21.0 A (HFM)
- 18.7 A (LFM)
- TBD A (SuperLFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant SuperLFM)
- TBD A (Sleep HFM)
- TBD A (Sleep SuperLFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep SuperLFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

Ultra Low Voltage:

- 17.0 A (Design Target)
- TBD A (HFM)
- TBD A (LFM)
- TBD A (Auto-Halt/Stop-Grant HFM)
- TBD A (Auto-Halt/Stop-Grant LFM)
- TBD A (Sleep HFM)
- TBD A (Sleep LFM)
- TBD A (Deep Sleep HFM)
- TBD A (Deep Sleep LFM)
- TBD A (Deeper Sleep)
- TBD A (Enhanced Deeper Sleep)

(CPU IO POWER 1.05V)

=PP1V05_S0_CPU_# 8 10 12 13 62

- 4500 mA (before VCC stable)
- 2500 mA (after VCC stable)

(CPU INTERNAL PLL POWER 1.5V)

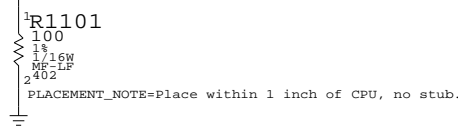
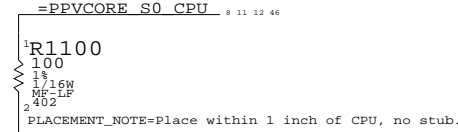
=PP1V5_S0_CPU_# 12

- 130 mA

- VID0 AD6 CPU VID<0>
- VID1 AF5 CPU VID<1>
- VID2 AE5 CPU VID<2>
- VID3 AF4 CPU VID<3>
- VID4 AE3 CPU VID<4>
- VID5 AF3 CPU VID<5>
- VID6 AE2 CPU VID<6>

VCCSENSE AF7 CPU VCCSENSE P

VSSSENSE AE7 CPU VCCSENSE N



CPU Power & Ground

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	11	96	

D

D

C

C

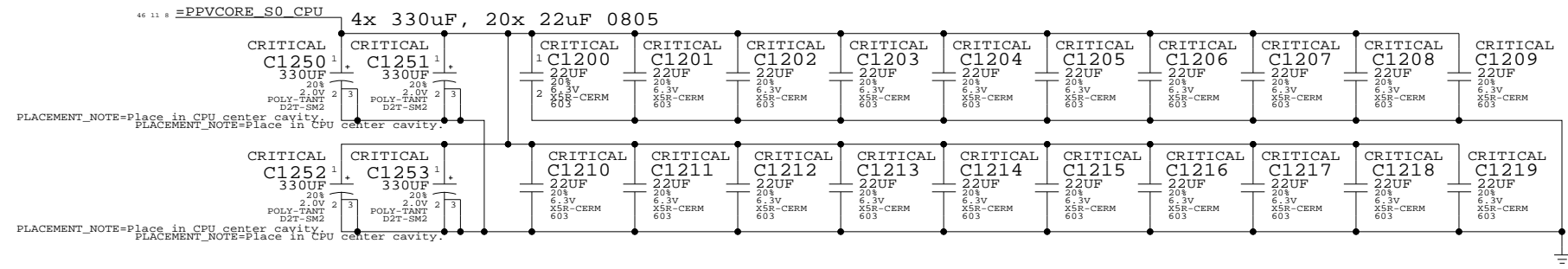
B

B

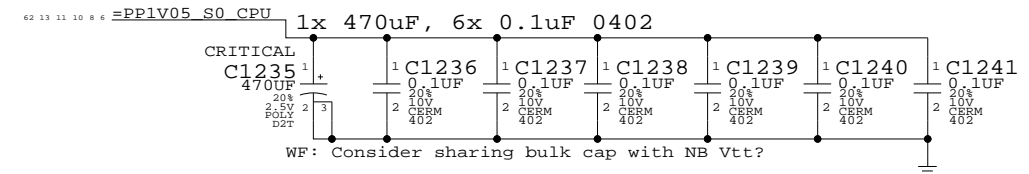
A

A

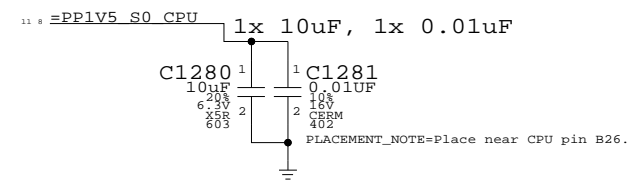
CPU VCORE HF AND BULK DECOUPLING



VCCP (CPU I/O) DECOUPLING



VCCA (CPU AVdd) DECOUPLING



CPU Decoupling & VID
 SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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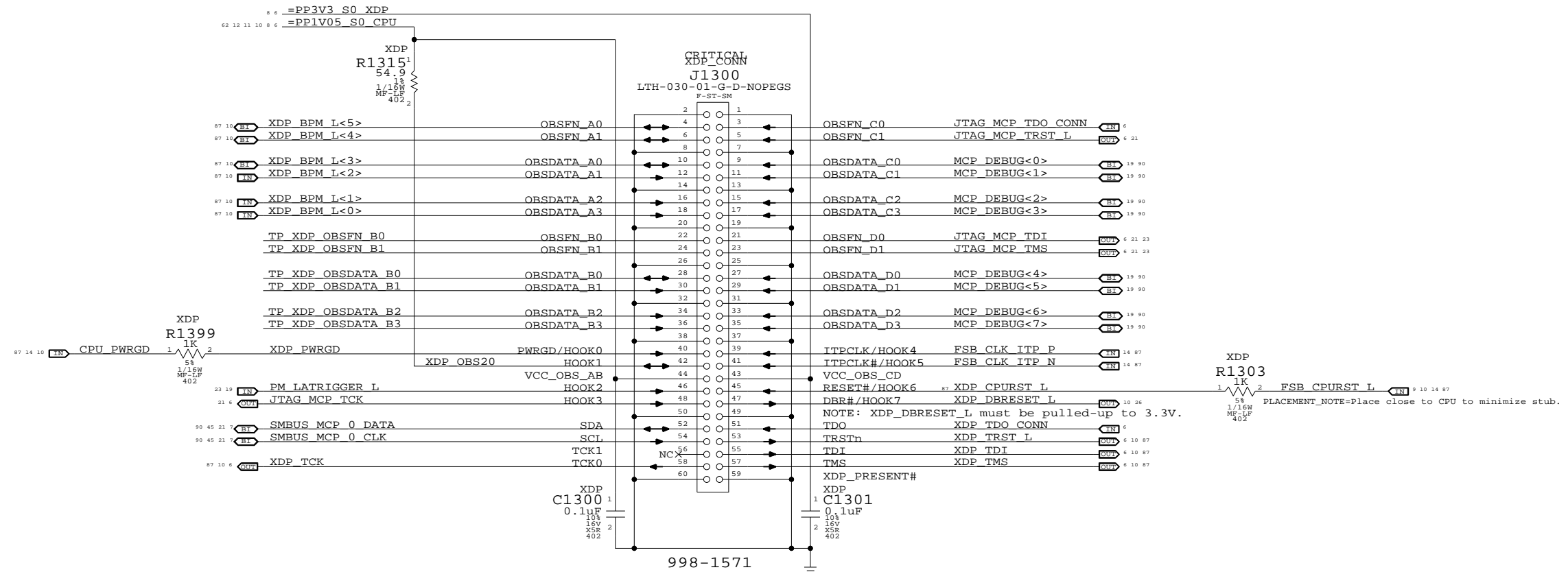
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	
NONE	12	96	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

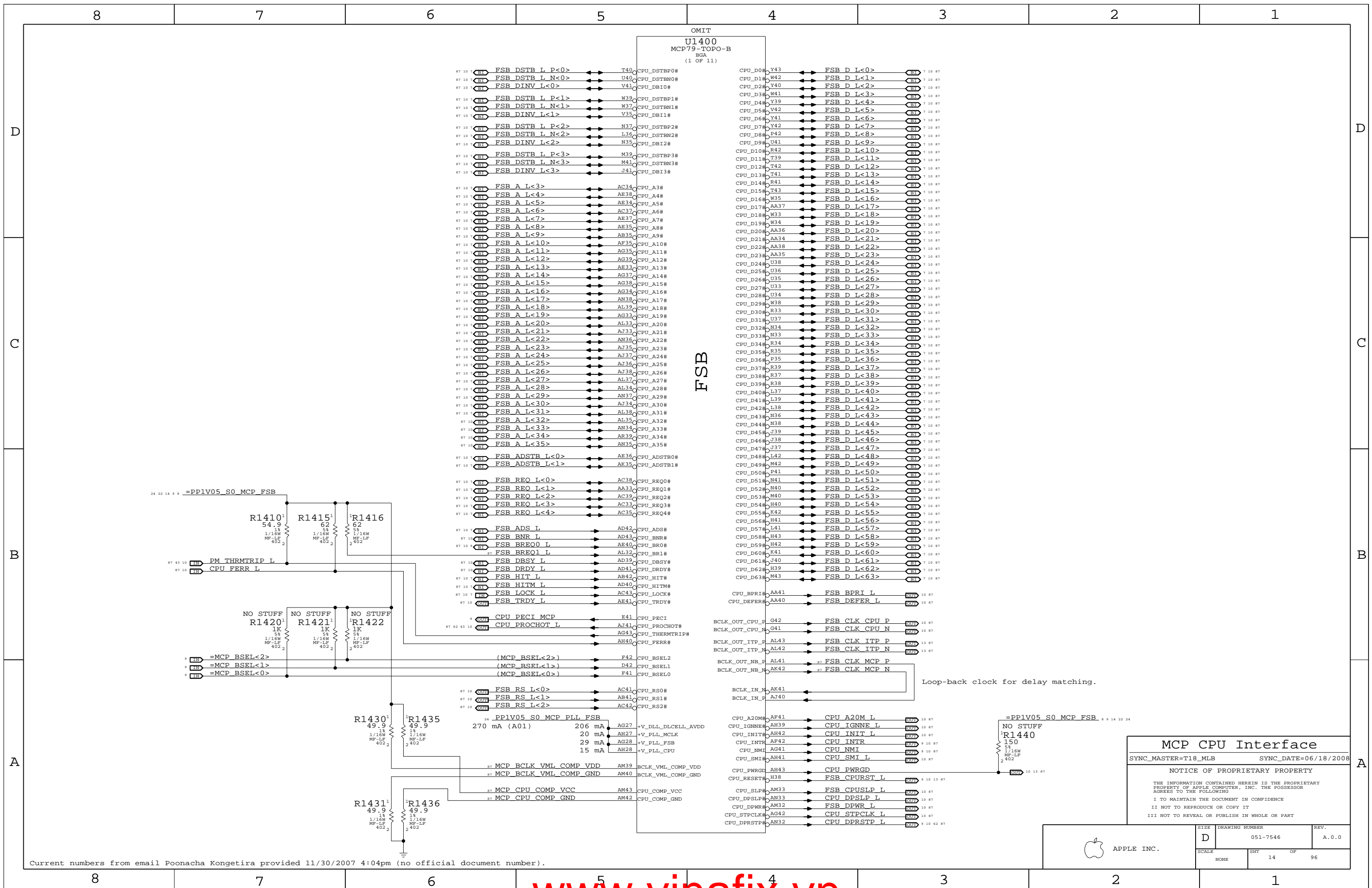


← Direction of XDP module
Please avoid any obstructions on even-numbered side of J1300

eXtended Debug Port (MiniXDP)
SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

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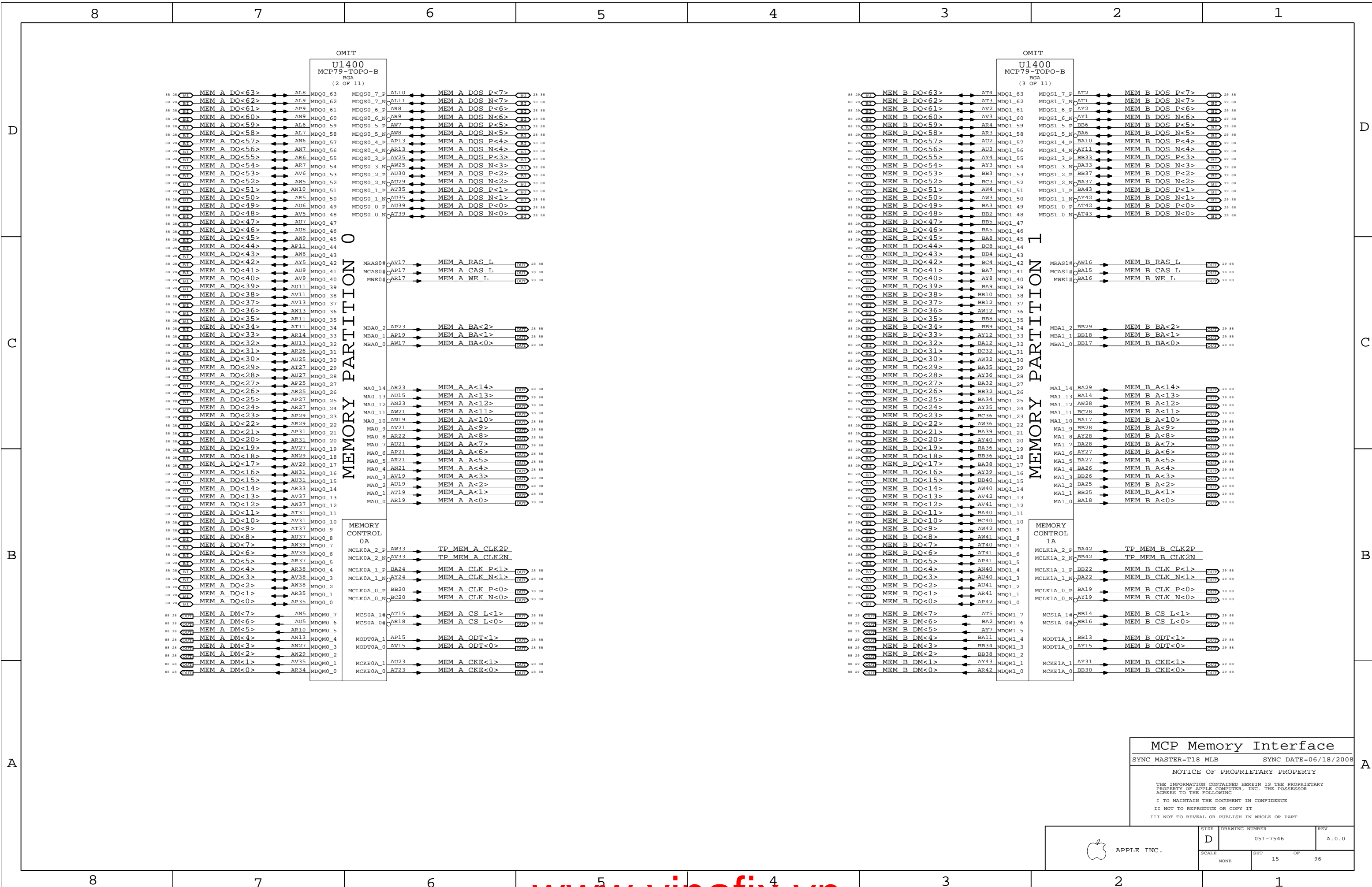
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHT	OF
NONE		13	96



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MCP CPU Interface		
SYNC_MASTER=T18_MLB		SYNC_DATE=06/18/2008
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	D	051-7546	A.0.0
SCALE	SHEET	OF	
NONE	14	96	



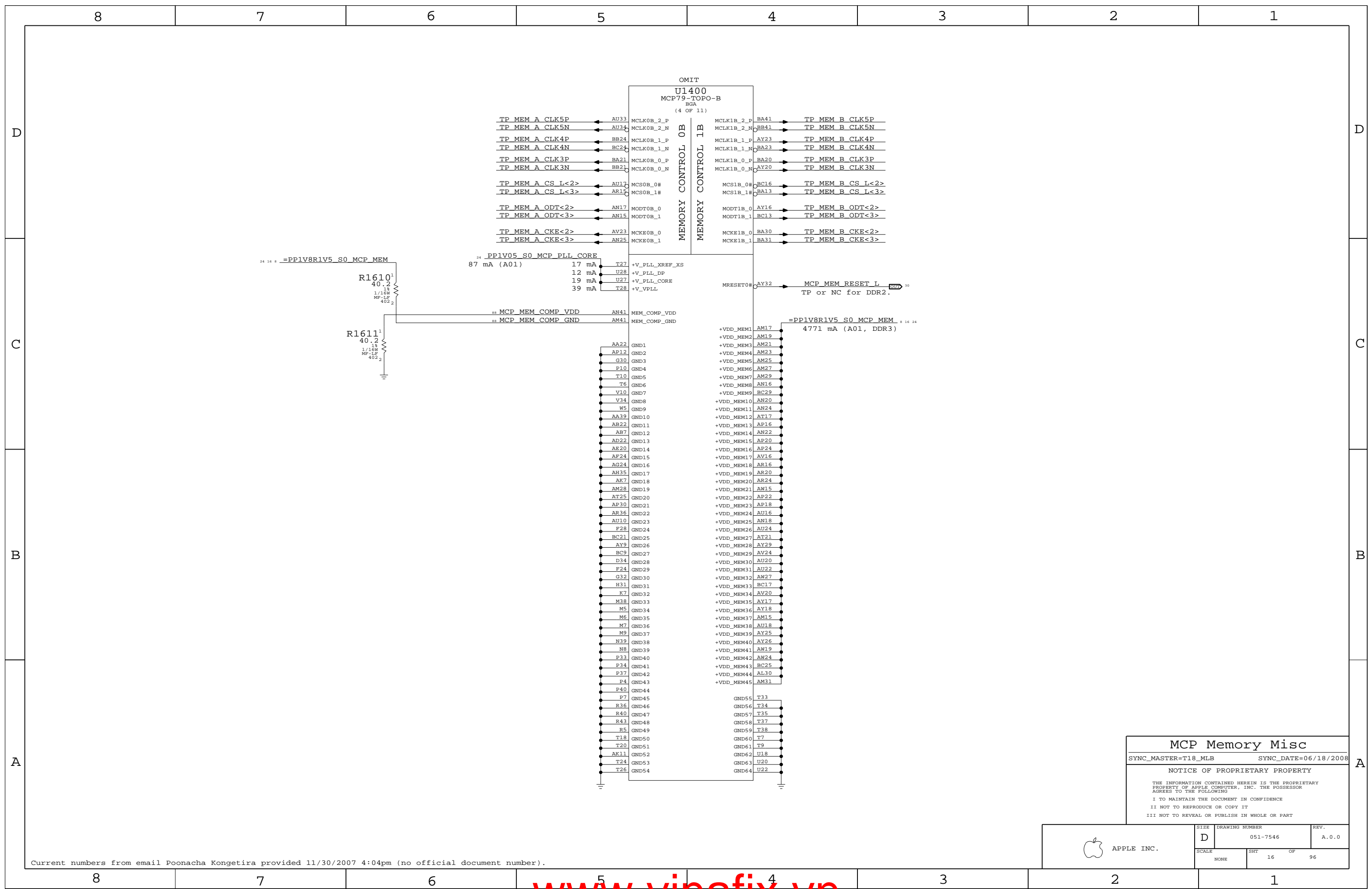
MCP Memory Interface

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
	SCALE NONE	SHEET 15	OF 96

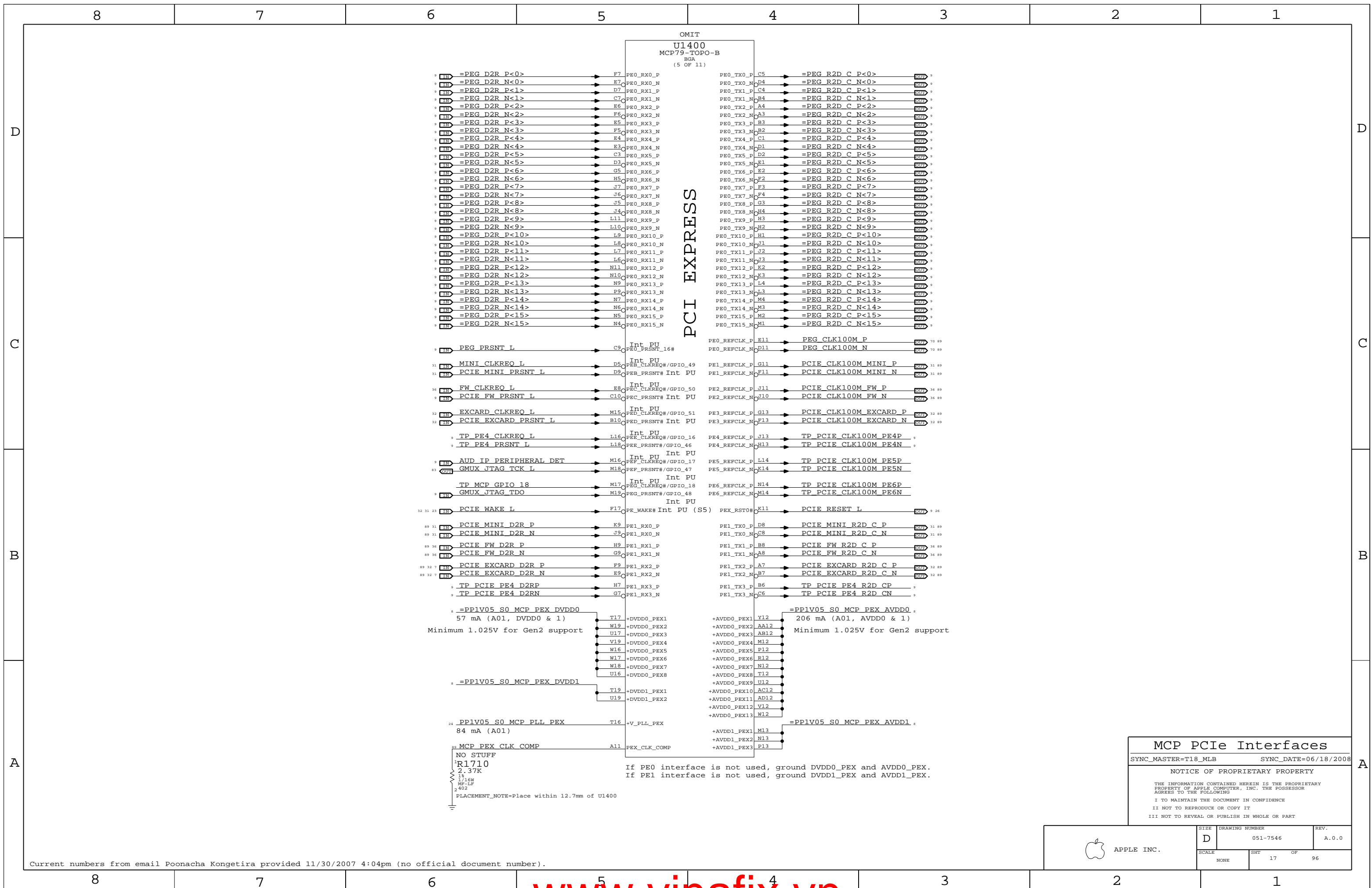


MCP Memory Misc
 SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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SCALE	SHT		OF
NONE	16		96

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PCI EXPRESS

If PE0 interface is not used, ground DVDD0_PEX and AVDD0_PEX.
 If PE1 interface is not used, ground DVDD1_PEX and AVDD1_PEX.

MCP PCIe Interfaces

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

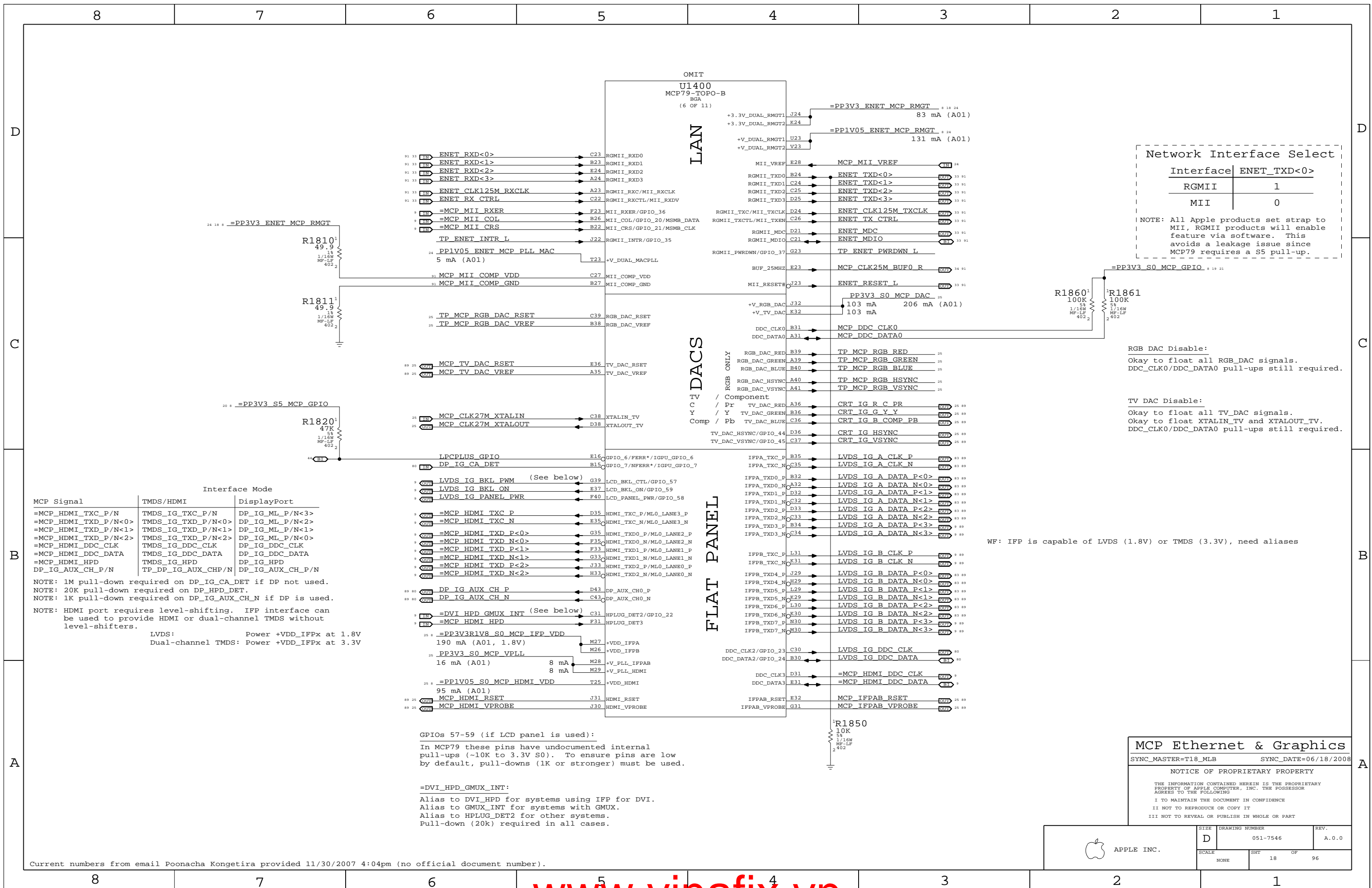
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	SCALE NONE	SHEET 17	OF 96

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Network Interface Select

Interface	ENET_TXD<0>
RGMII	1
MII	0

NOTE: All Apple products set strap to MII, RGMII products will enable feature via software. This avoids a leakage issue since MCP79 requires a S5 pull-up.

RGB DAC Disable:
Okay to float all RGB_DAC signals.
DDC_CLK0/DDC_DATA0 pull-ups still required.

TV DAC Disable:
Okay to float all TV_DAC signals.
Okay to float XTALIN_TV and XTALOUT_TV.
DDC_CLK0/DDC_DATA0 pull-ups still required.

Interface Mode

MCP Signal	TMDS/HDMI	DisplayPort
=MCP_HDMI_TXC_P/N	TMDS_IG_TXC_P/N	DP_IG_ML_P/N<3>
=MCP_HDMI_TXD_P/N<0>	TMDS_IG_TXD_P/N<0>	DP_IG_ML_P/N<2>
=MCP_HDMI_TXD_P/N<1>	TMDS_IG_TXD_P/N<1>	DP_IG_ML_P/N<1>
=MCP_HDMI_TXD_P/N<2>	TMDS_IG_TXD_P/N<2>	DP_IG_ML_P/N<0>
=MCP_HDMI_DDC_CLK	TMDS_IG_DDC_CLK	DP_IG_DDC_CLK
=MCP_HDMI_DDC_DATA	TMDS_IG_DDC_DATA	DP_IG_DDC_DATA
=MCP_HDMI_HPD	TMDS_IG_HPD	DP_IG_HPD
DP_IG_AUX_CH_P/N	TP_DP_IG_AUX_CH_P/N	DP_IG_AUX_CH_P/N

NOTE: 1M pull-down required on DP_IG_CA_DET if DP not used.
NOTE: 20K pull-down required on DP_HPD_DET.
NOTE: 1K pull-down required on DP_IG_AUX_CH_N if DP is used.
NOTE: HDMI port requires level-shifting. IFP interface can be used to provide HDMI or dual-channel TMDS without level-shifters.

LVDS:
Power +VDD_IFPx at 1.8V
Dual-channel TMDS: Power +VDD_IFPx at 3.3V

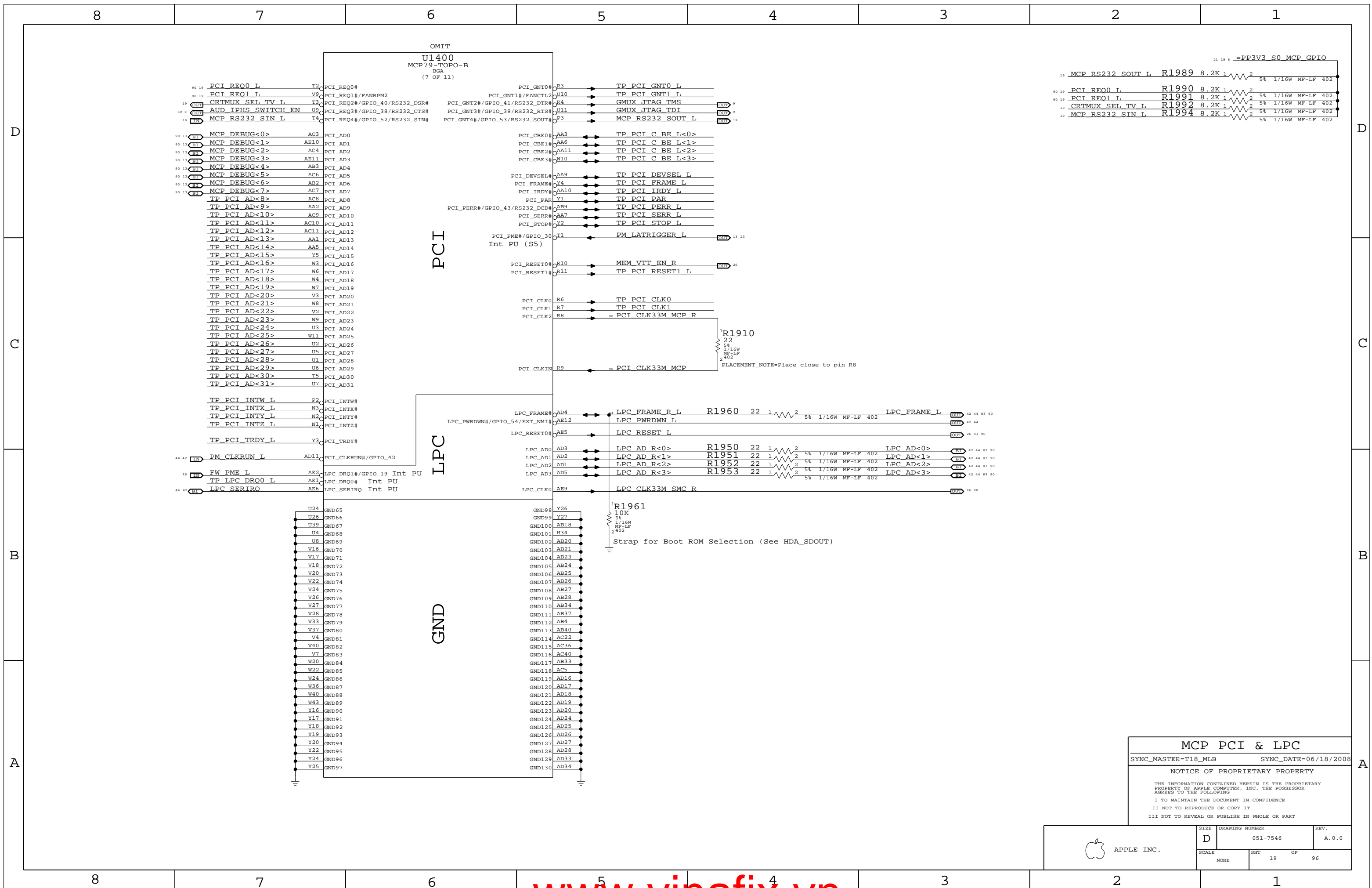
GPIOs 57-59 (if LCD panel is used):
In MCP79 these pins have undocumented internal pull-ups (~10K to 3.3V S0). To ensure pins are low by default, pull-downs (1K or stronger) must be used.

=DVI_HPD_GMUX_INT:
Alias to DVI_HPD for systems using IFP for DVI.
Alias to GMUX_INT for systems with GMUX.
Alias to HPLUG_DET2 for other systems.
Pull-down (20k) required in all cases.

MCP Ethernet & Graphics
SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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SCALE	SHT	OF	96
NONE	18		



MCP PCI & LPC

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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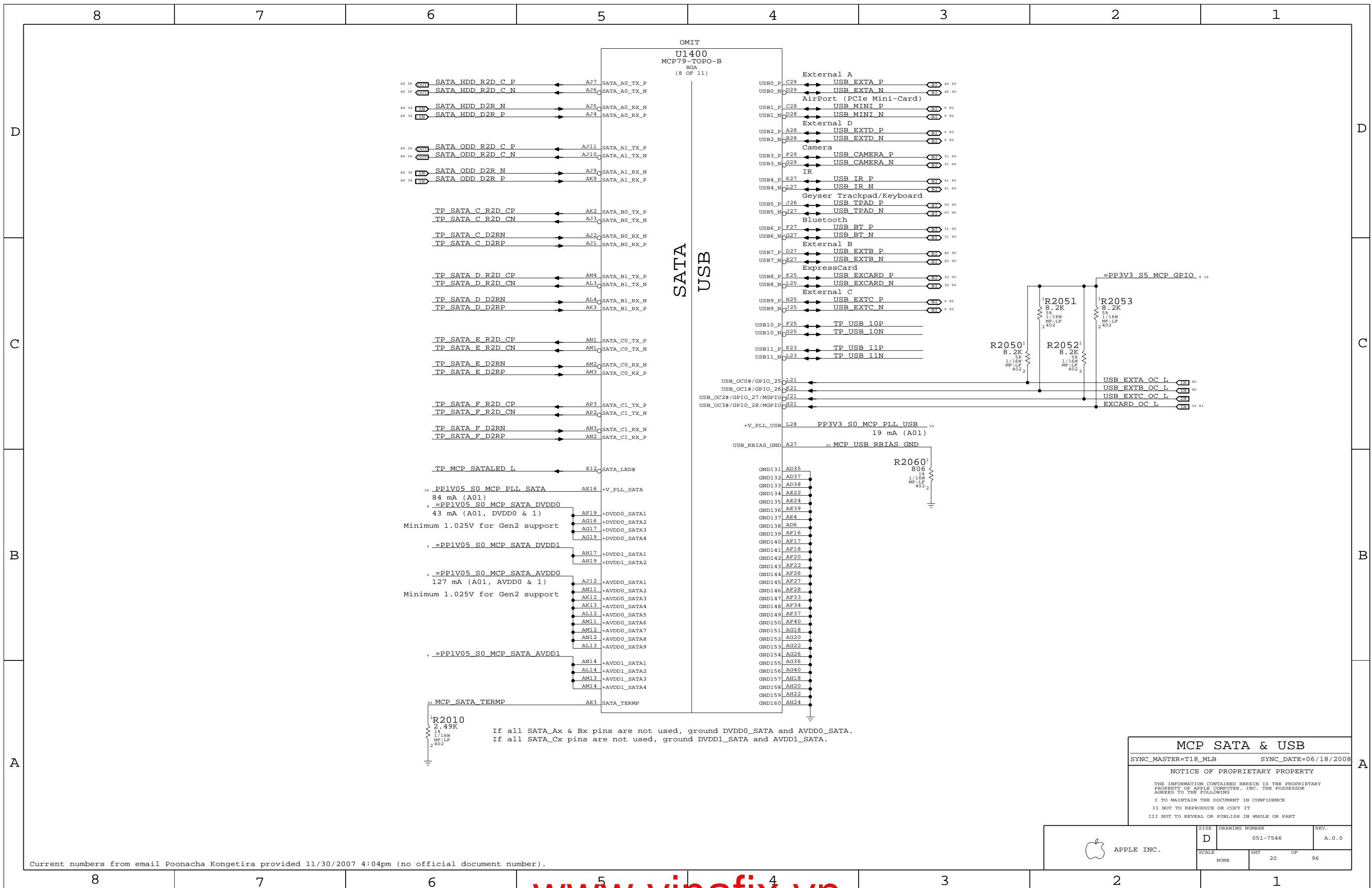
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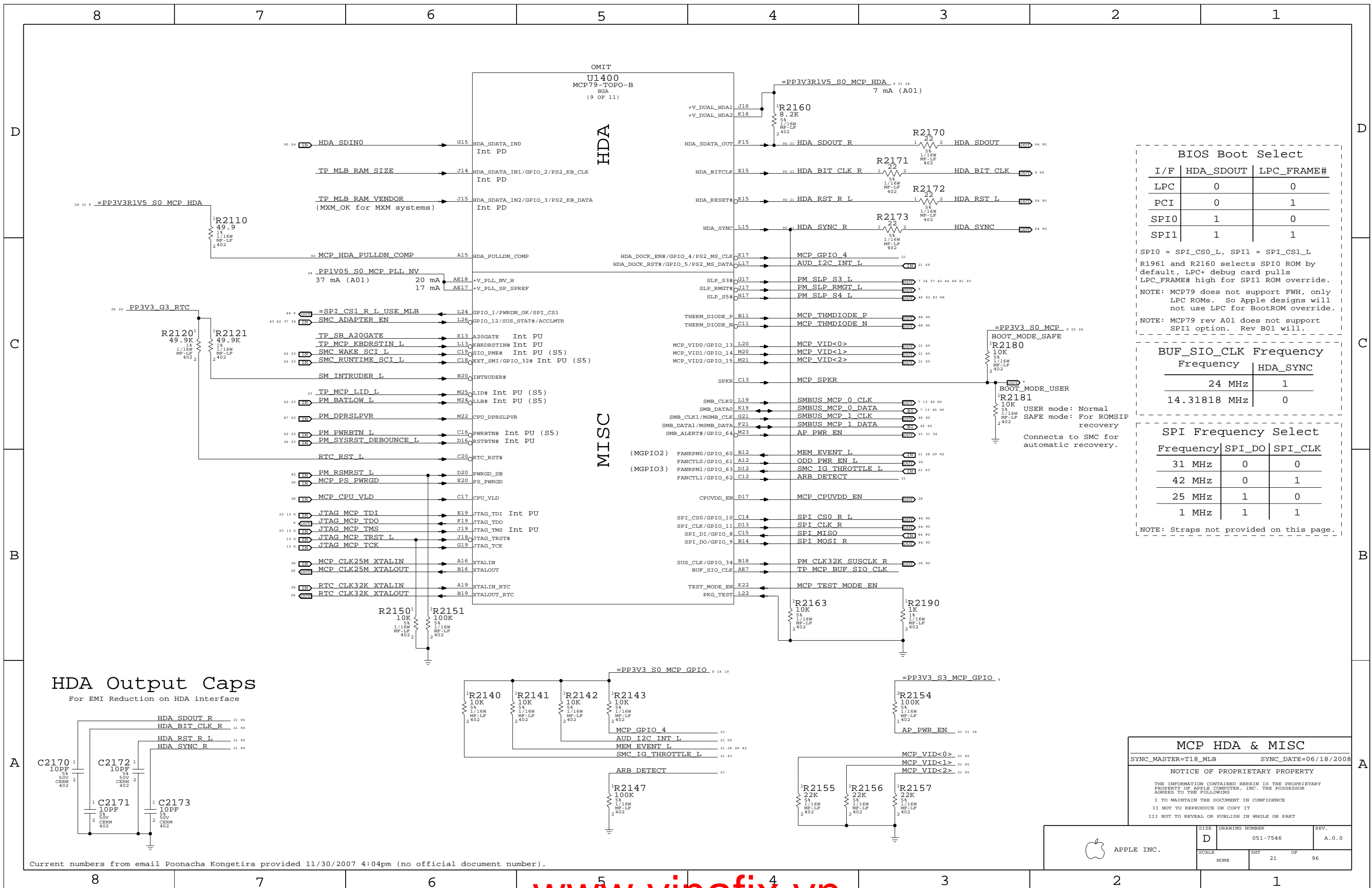
APPLE INC.	SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
	SCALE NONE	SHEET 19	OF 96



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MCP SATA & USB
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	20	96	



BIOS Boot Select

I/F	HDA_SDOUT	LPC_FRAME#
LPC	0	0
PCI	0	1
SPI0	1	0
SPI1	1	1

SPI0 = SPI_CS0_L, SPI1 = SPI_CS1_L
 R1961 and R2160 selects SPI0 ROM by default, LPC+ debug card pulls LPC_FRAME# high for SPI1 ROM override.
 NOTE: MCP79 does not support FWH, only LPC ROMs. So Apple designs will not use LPC for BootROM override.
 NOTE: MCP79 rev A01 does not support SPI1 option. Rev B01 will.

BUF_SIO_CLK Frequency

Frequency	HDA_SYNC
24 MHz	1
14.31818 MHz	0

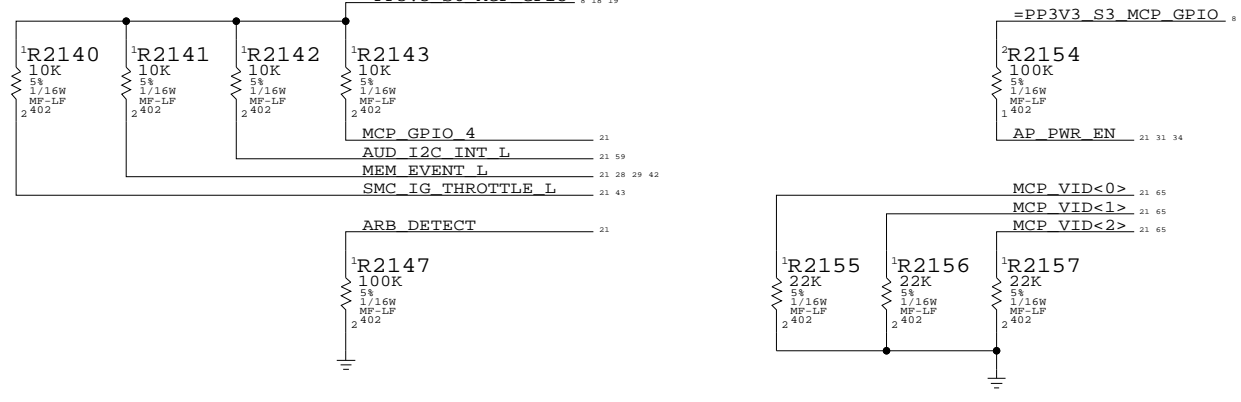
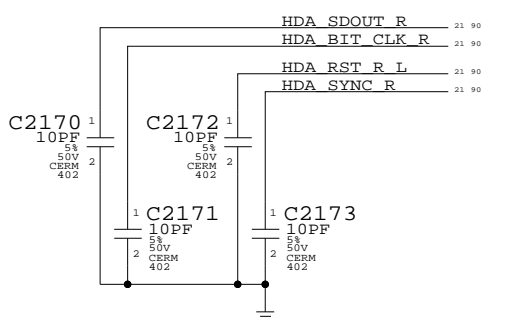
SPI Frequency Select

Frequency	SPI_DO	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

NOTE: Straps not provided on this page.

CONNECTS TO SMC FOR AUTOMATIC RECOVERY.

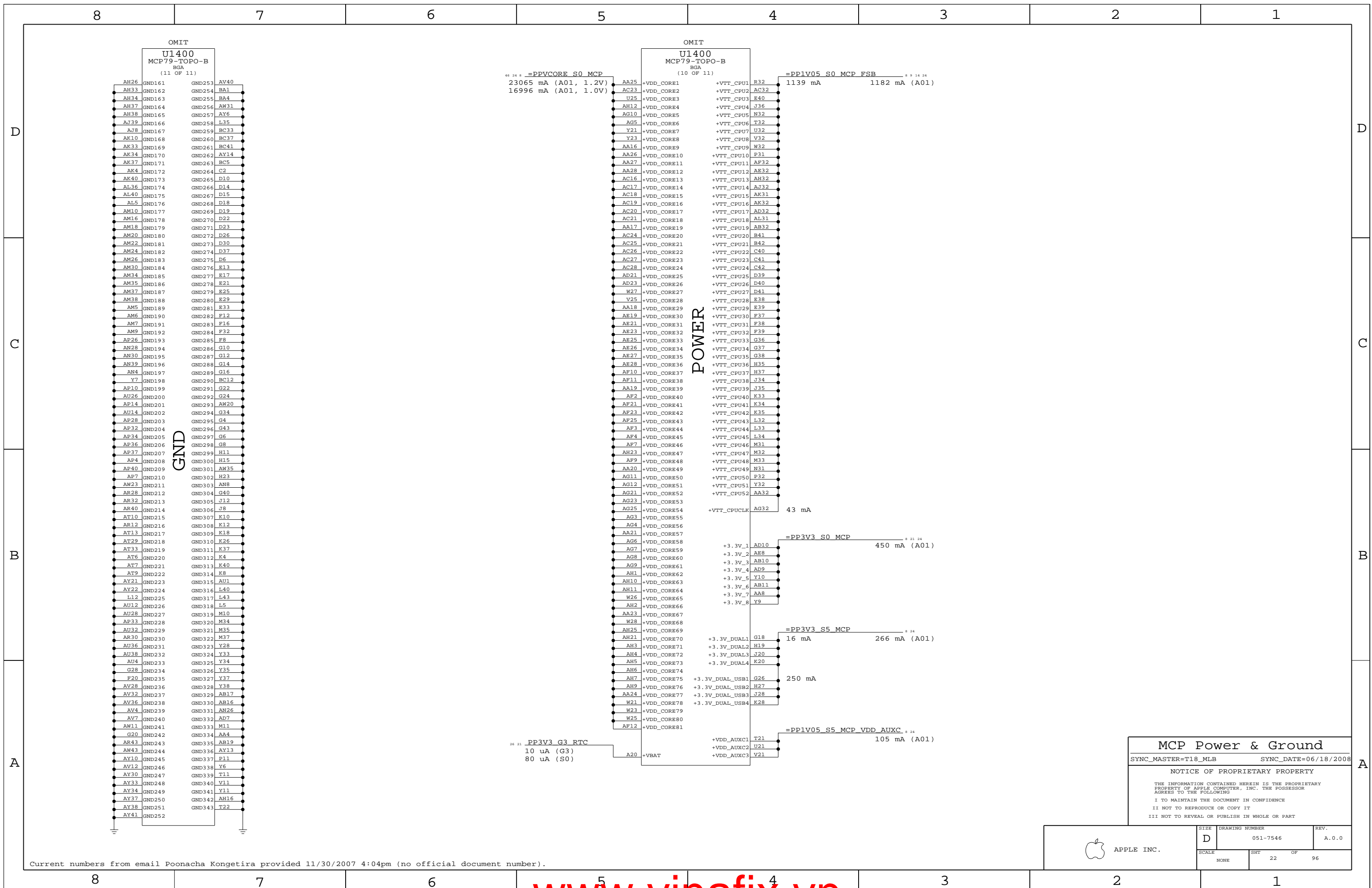
HDA Output Caps
For EMI Reduction on HDA interface



MCP HDA & MISC
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APPLE INC. DRAWING NUMBER: 051-7546 REV: A.0.0
 SCALE: NONE SHEET: 21 OF 96

Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Power & Ground	
SYNC_MASTER=T18_MLB	SYNC_DATE=06/18/2008
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	22		

8

7

6

5

4

3

2

1

D

D

C

C

B

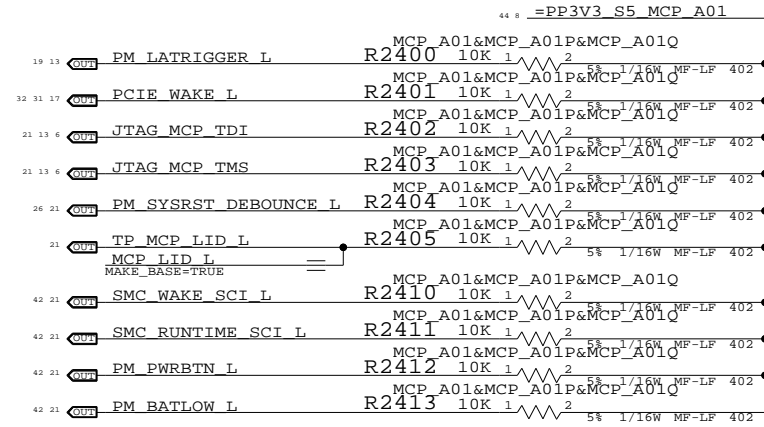
B

A

A

3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.



MCP79 A01 Silicon Support

SYNC_MASTER=T18_MLB SYNC_DATE=03/31/2008

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	23	96

8

7

6

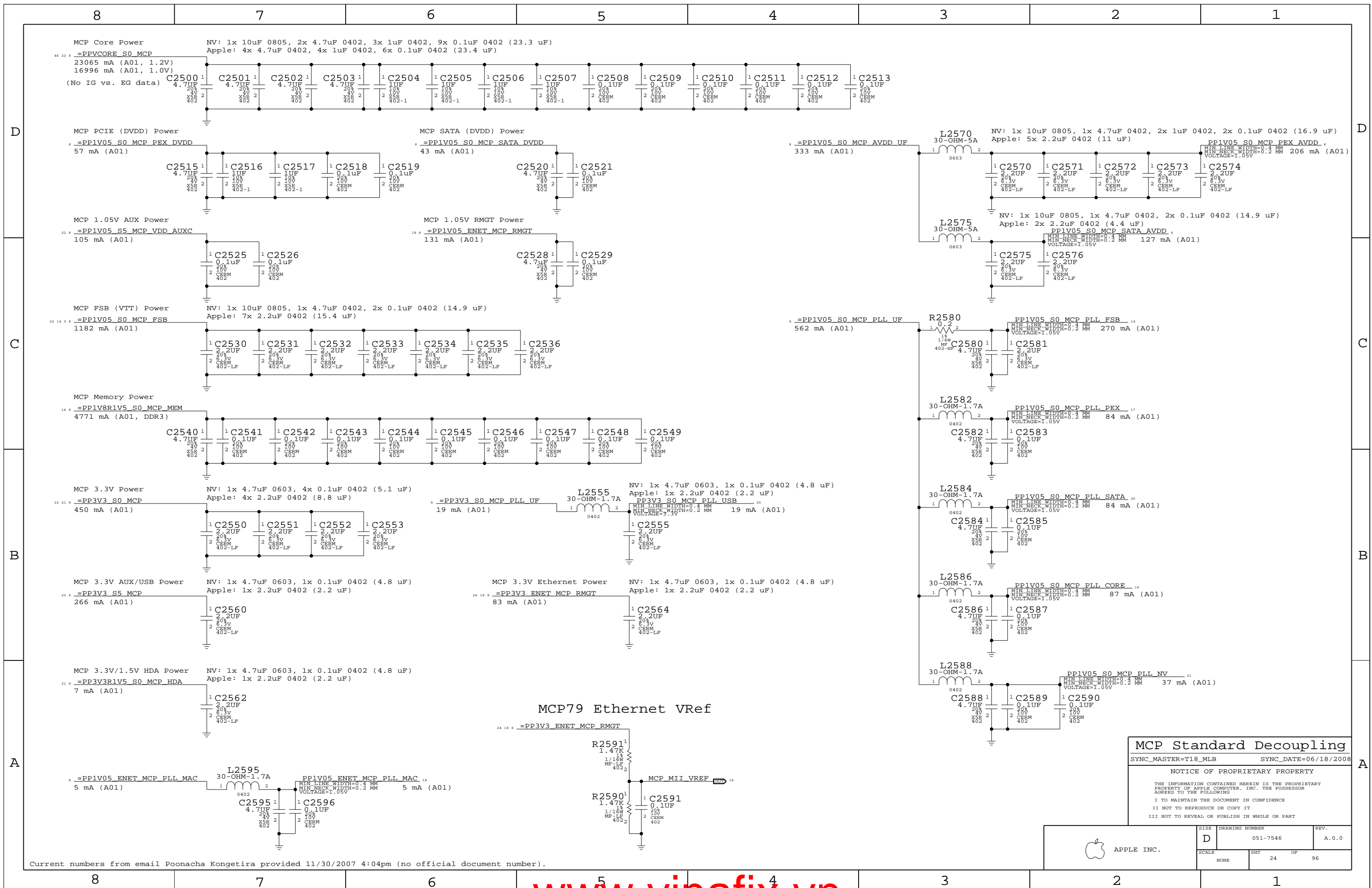
5

4

3

2

1



Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

MCP Standard Decoupling

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

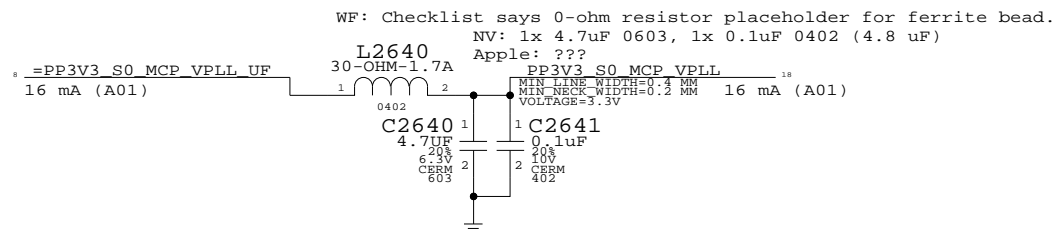
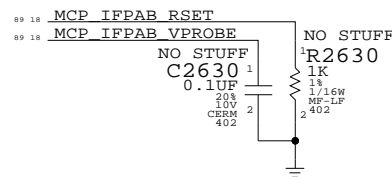
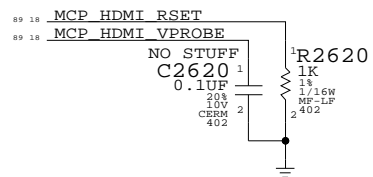
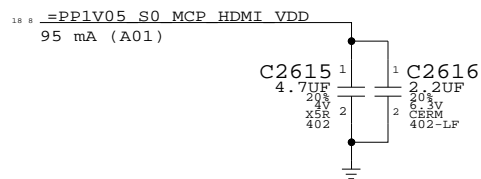
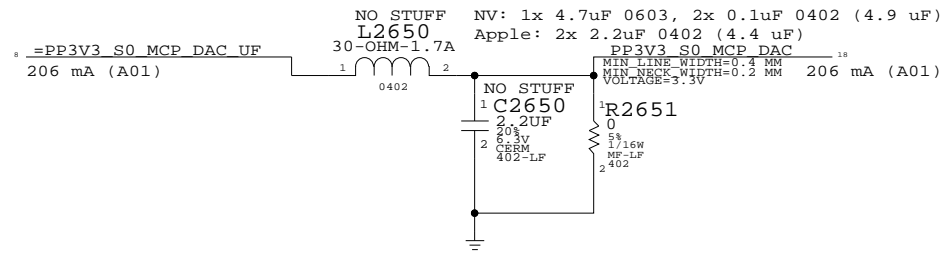
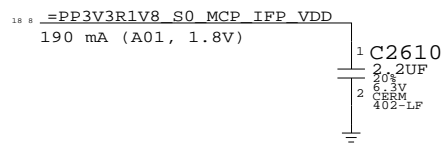
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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	24	96

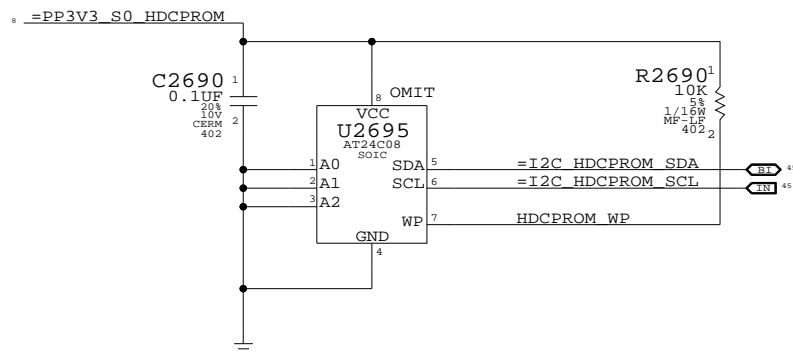
WF: Checklist says 0-ohm resistor placeholder for ferrite bead.
 NV: 1x 4.7uF 0603, 1x 0.1uF 0402 (4.8 uF)
 Apple: 1x 2.2uF 0402 (2.2 uF)



TP MCP RGB RED	==	NC MCP RGB RED
TP MCP RGB GREEN	==	NC MCP RGB GREEN
TP MCP RGB BLUE	==	NC MCP RGB BLUE
TP MCP RGB HSYNC	==	NC MCP RGB HSYNC
TP MCP RGB VSYNC	==	NC MCP RGB VSYNC
CRT IG R C PR	==	NC CRT IG R C PR
CRT IG G Y Y	==	NC CRT IG G Y Y
CRT IG B COMP PB	==	NC CRT IG B COMP PB
CRT IG HSYNC	==	NC CRT IG HSYNC
CRT IG VSYNC	==	NC CRT IG VSYNC
TP MCP RGB DAC RSET	==	NC MCP RGB DAC RSET
TP MCP RGB DAC VREF	==	NC MCP RGB DAC VREF
MCP TV DAC RSET	==	NC MCP TV DAC RSET
MCP TV DAC VREF	==	NC MCP TV DAC VREF
MCP CLK27M XTALIN	==	NC MCP CLK27M XTALIN
MCP CLK27M XTALOUT	==	NC MCP CLK27M XTALOUT

HDCP ROM

WF: Open question on which package option(s) nVidia can support.



MCP Graphics Support

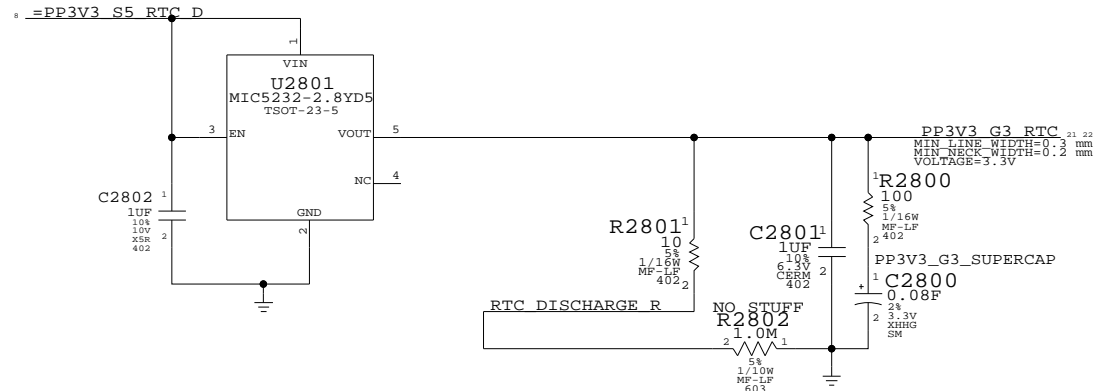
SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008

NOTICE OF PROPRIETARY PROPERTY

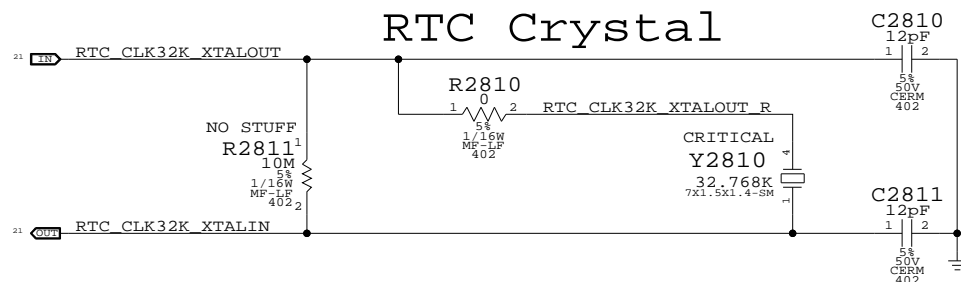
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	25		

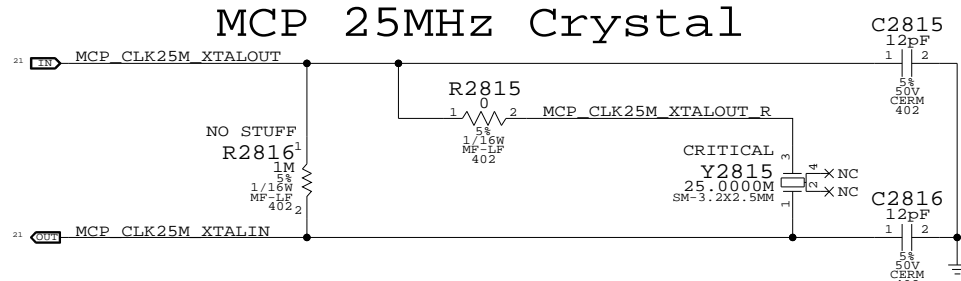
RTC Power Sources



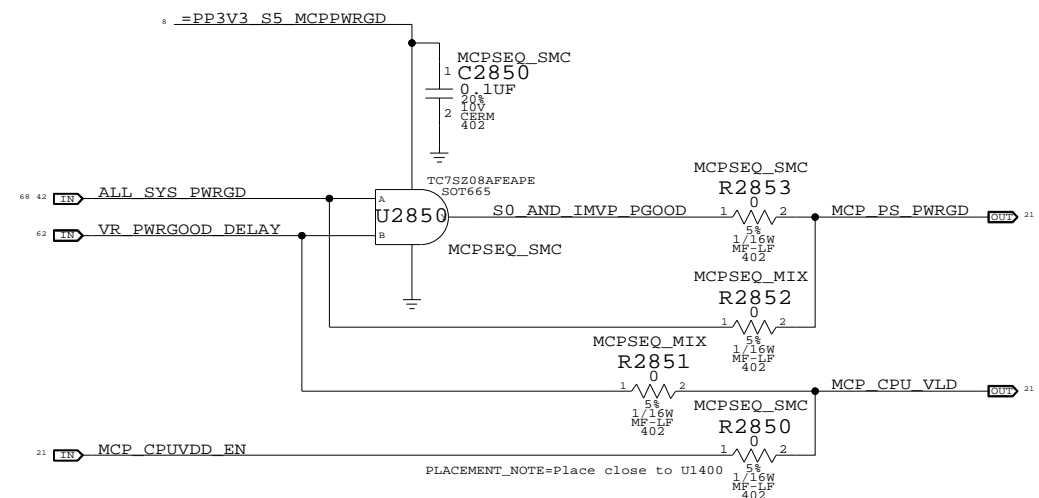
RTC Crystal



MCP 25MHz Crystal

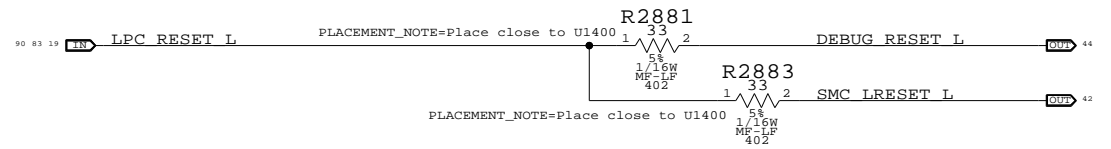


MCP S0 PWRGD & CPU_VLD

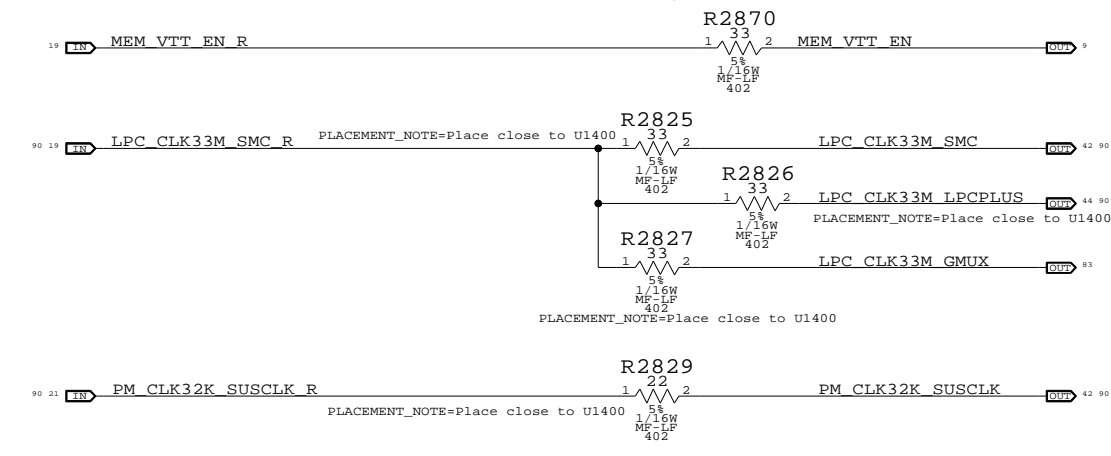
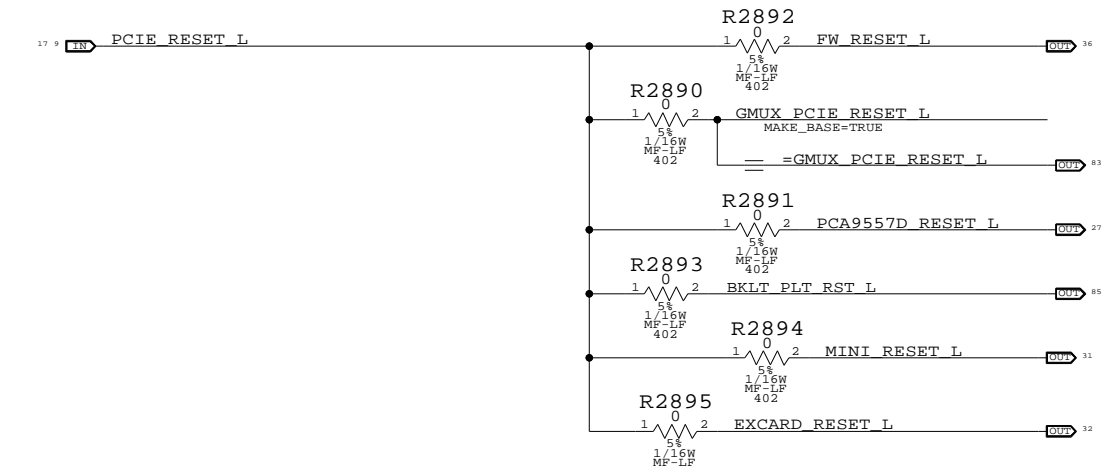


MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, but results in MCP79 ROMSIP sequence happening after CPU powers up. MCPSEQ_MIX is cross between MLB and internal power sequencing, which results in earlier ROMSIP and MCP FSB I/O interface initialization. SMC 99ms delay from ALL_SYS_PWRGD to IMVP_VR_ON plus IMVP6 delay for VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before CPUVDD_EN (which is 40-100ms after PS_PWRGD assertion).
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

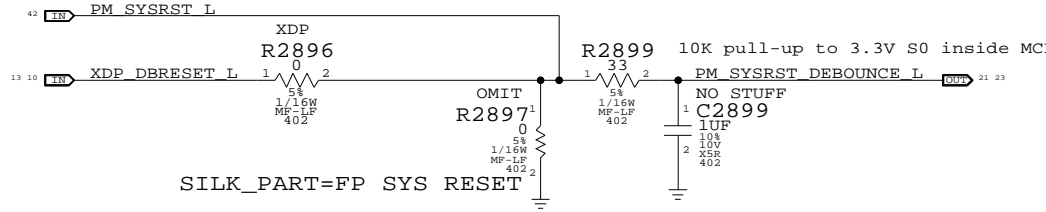
Platform Reset Connections LPC Reset (Unbuffered)



PCIE Reset (Unbuffered)



Reset Button



SB Misc		
SYNC_MASTER=T18_MLB	SYNC_DATE=12/17/2007	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	26		

Page Notes

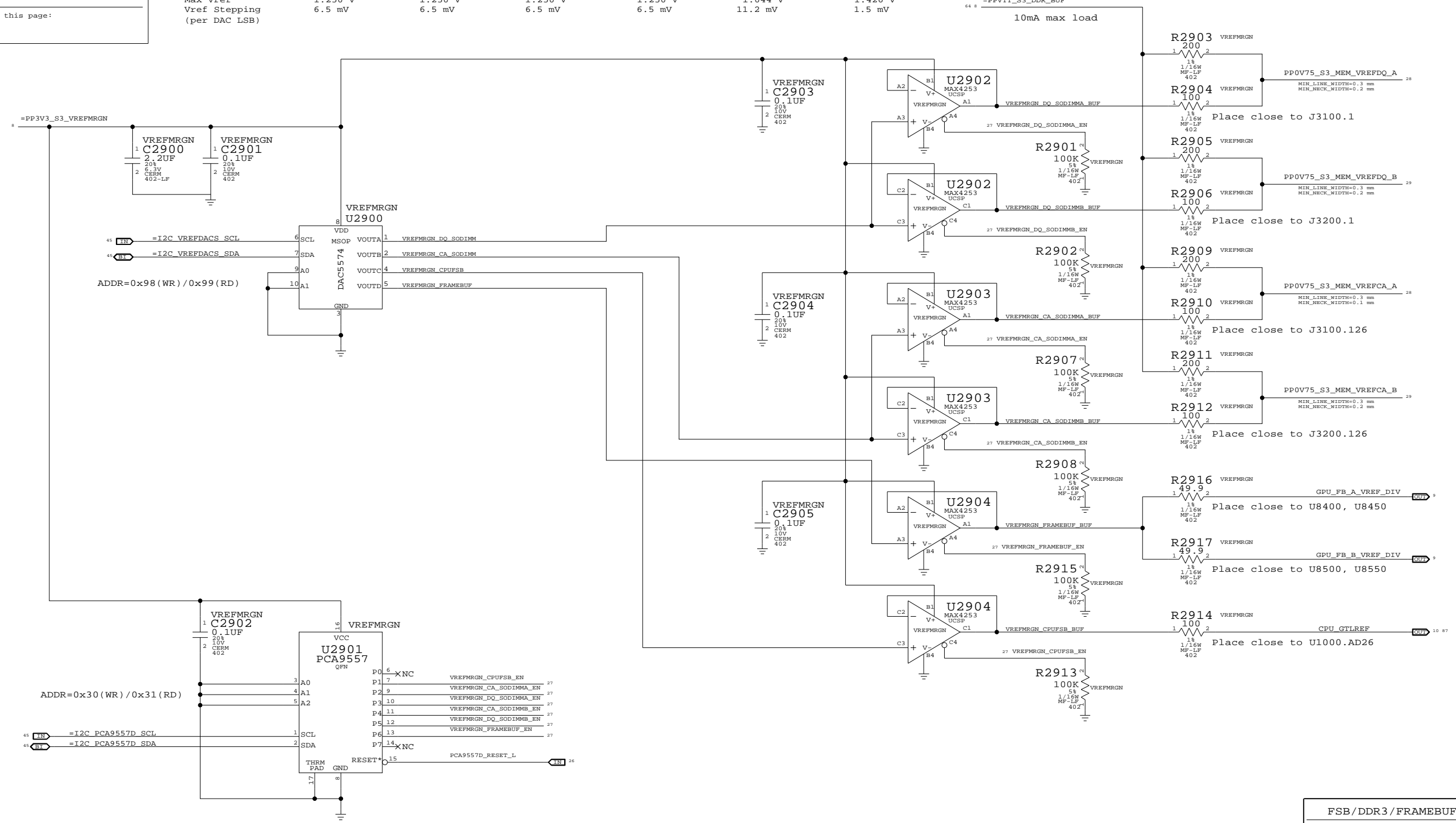
Power aliases required by this page:
 - =PP3V3_S3_VREFMRGN
 - =PP3V3_S5_VREFMRGN
 - =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
 - =I2C_VREFDACS_SCL
 - =I2C_VREFDACS_SDA
 - =I2C_PCA9557D_SCL
 - =I2C_PCA9557D_SDA

BOM options provided by this page:
 VREFMRGN
 NO_VREFMRGN

	MEM A VREF DQ	MEM A VREF CA	MEM B VREF DQ	MEM B VREF CA	CPU FSB VREF	FRAME BUFFER VREF
DAC channel	A	B	A	B	C	D
Min DAC code	0x00	0x00	0x00	0x00	0x00	0x00
Max DAC code	0x87	0x87	0x87	0x87	0x55	0xFF
Max sink I	-3.75 mA	-3.75 mA	-3.75 mA	-3.75 mA	-0.91 mA	-59.04 mA
Max source I	5 mA	5 mA	5 mA	5 mA	0.52 mA	51.15 mA
Nominal Vref	0.75 V	0.75 V	0.75 V	0.75 V	0.70 V	1.248 V
Min Vref	0.375 V	0.375 V	0.375 V	0.375 V	0.091 V	1.042 V
Max Vref	1.250 V	1.250 V	1.250 V	1.250 V	1.044 V	1.426 V
Vref Stepping (per DAC LSB)	6.5 mV	6.5 mV	6.5 mV	6.5 mV	11.2 mV	1.5 mV

SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2903	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2905	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2909	CRITICAL	NO_VREFMRGN
116S0004	1	RES.MTL FILM, 0,5%, 0402, SM, LF	R2911	CRITICAL	NO_VREFMRGN

FSB/DDR3/FRAMEBUF Vref Margining
 SYNC_MASTER=DDR SYNC_DATE=07/22/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	27		

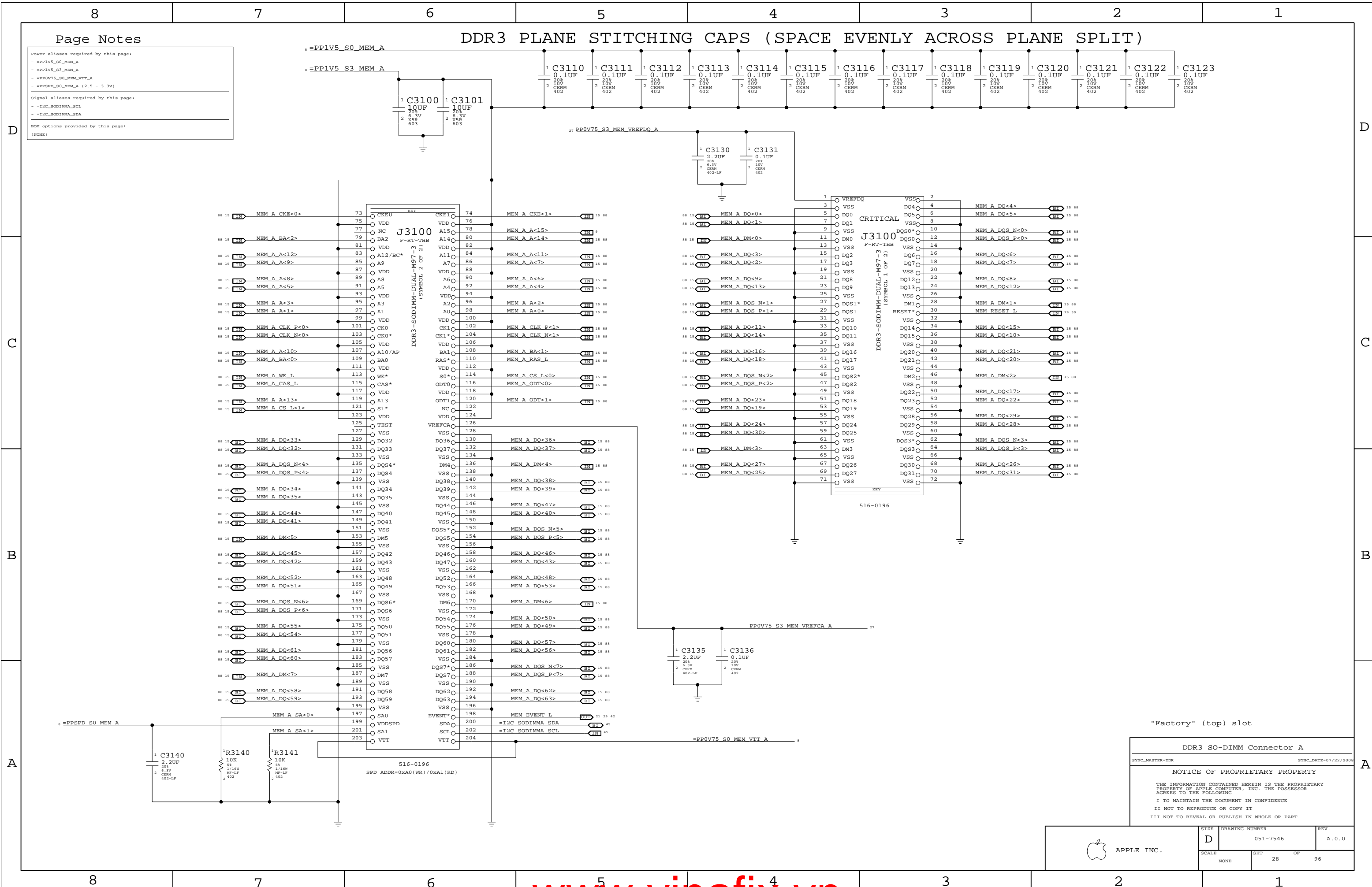
Page Notes

Power aliases required by this page:
 - =PP1V5_S0_MEM_A
 - =PP1V5_S3_MEM_A
 - =PP0V75_S0_MEM_VTT_A
 - =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMA_SCL
 - =I2C_SODIMMA_SDA

BOM options provided by this page:
 (NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)



"Factory" (top) slot

DDR3 SO-DIMM Connector A

SYNC_MASTER=DDR SYNC_DATE=07/22/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	28 OF 96

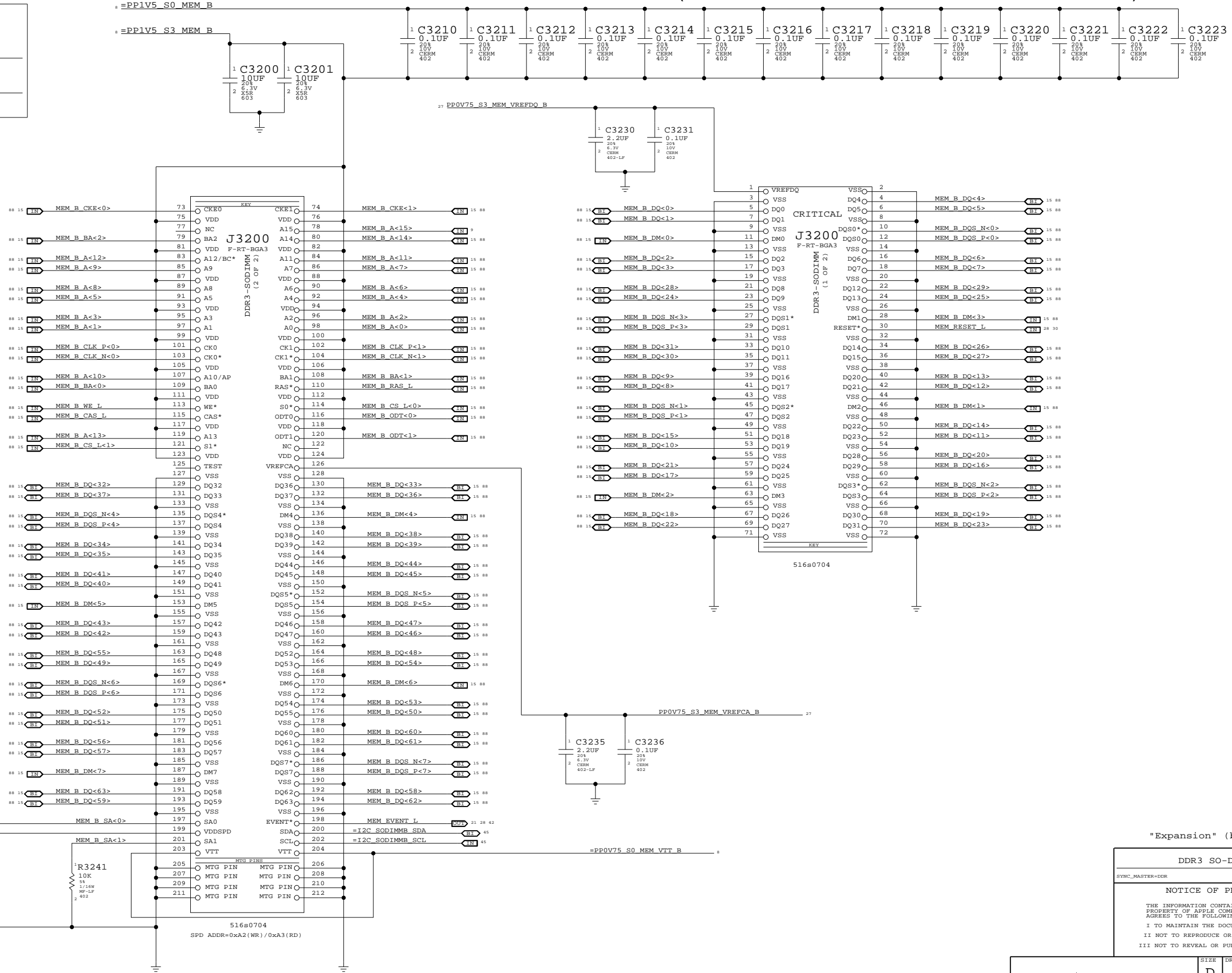
Page Notes

Power aliases required by this page:
 - =PP1V5_S0_MEM_B
 - =PP1V5_S3_MEM_B
 - =PP0V75_S0_MEM_VTT_B
 - =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
 - =I2C_SODIMMB_SCL
 - =I2C_SODIMMB_SDA

BOM options provided by this page:
 (NONE)

DDR3 PLANE STITCHING CAPS (SPACE EVENLY ACROSS PLANE SPLIT)



"Expansion" (bottom) slot

DDR3 SO-DIMM Connector B
 SYNC_MASTER=DDR SYNC_DATE=07/22/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	29		

8

7

6

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3

2

1

D

D

C

C

B

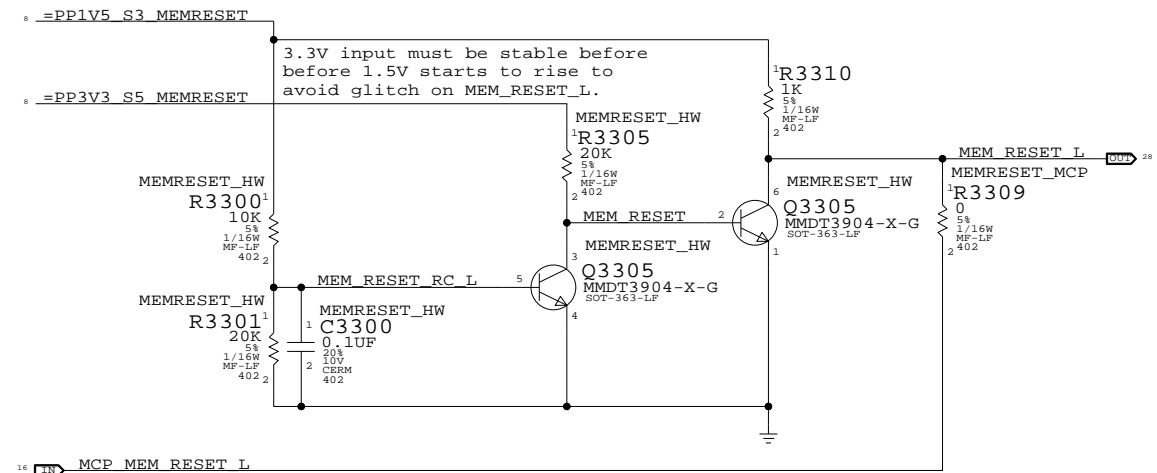
B

A

A

DDR3 RESET Support

MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.



DDR3 Support

SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008

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	SCALE	SHEET	OF	REV.
	NONE	30	96	A.0.0

8

7

6

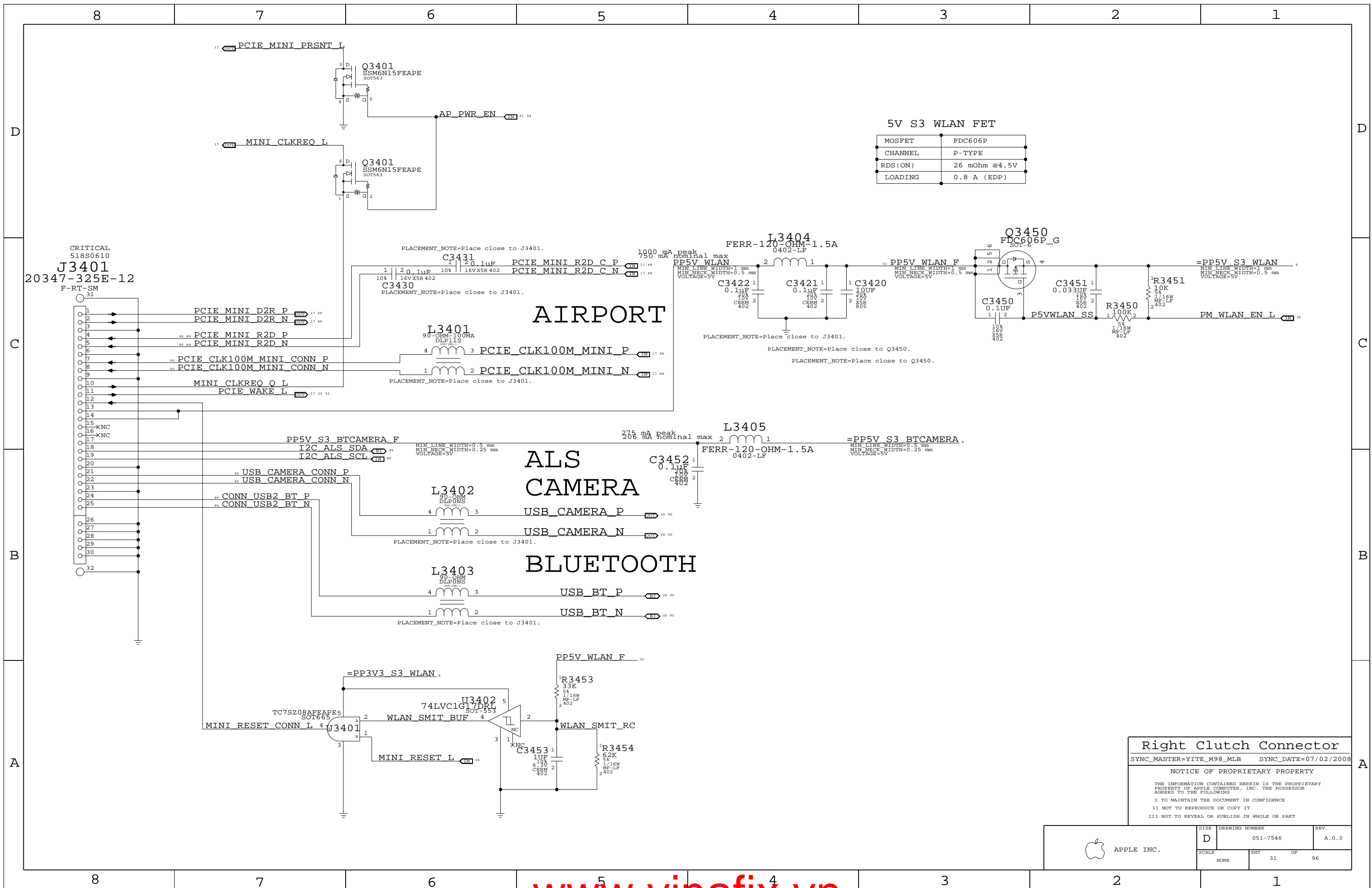
5

4

3

2

1



5V S3 WLAN FET

MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	0.8 A (EDP)

AIRPORT

ALS CAMERA

BLUETOOTH

Right Clutch Connector
 SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

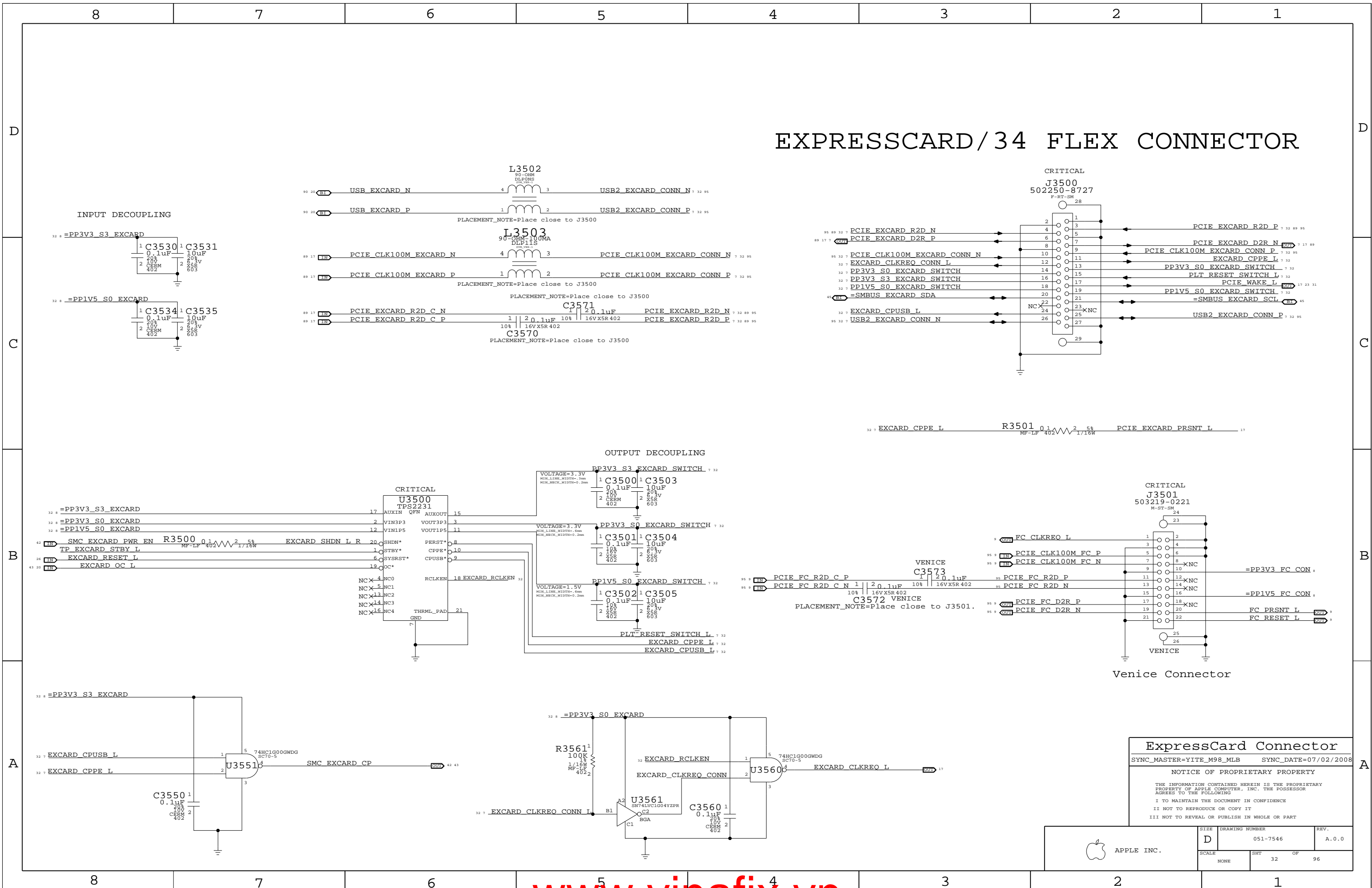
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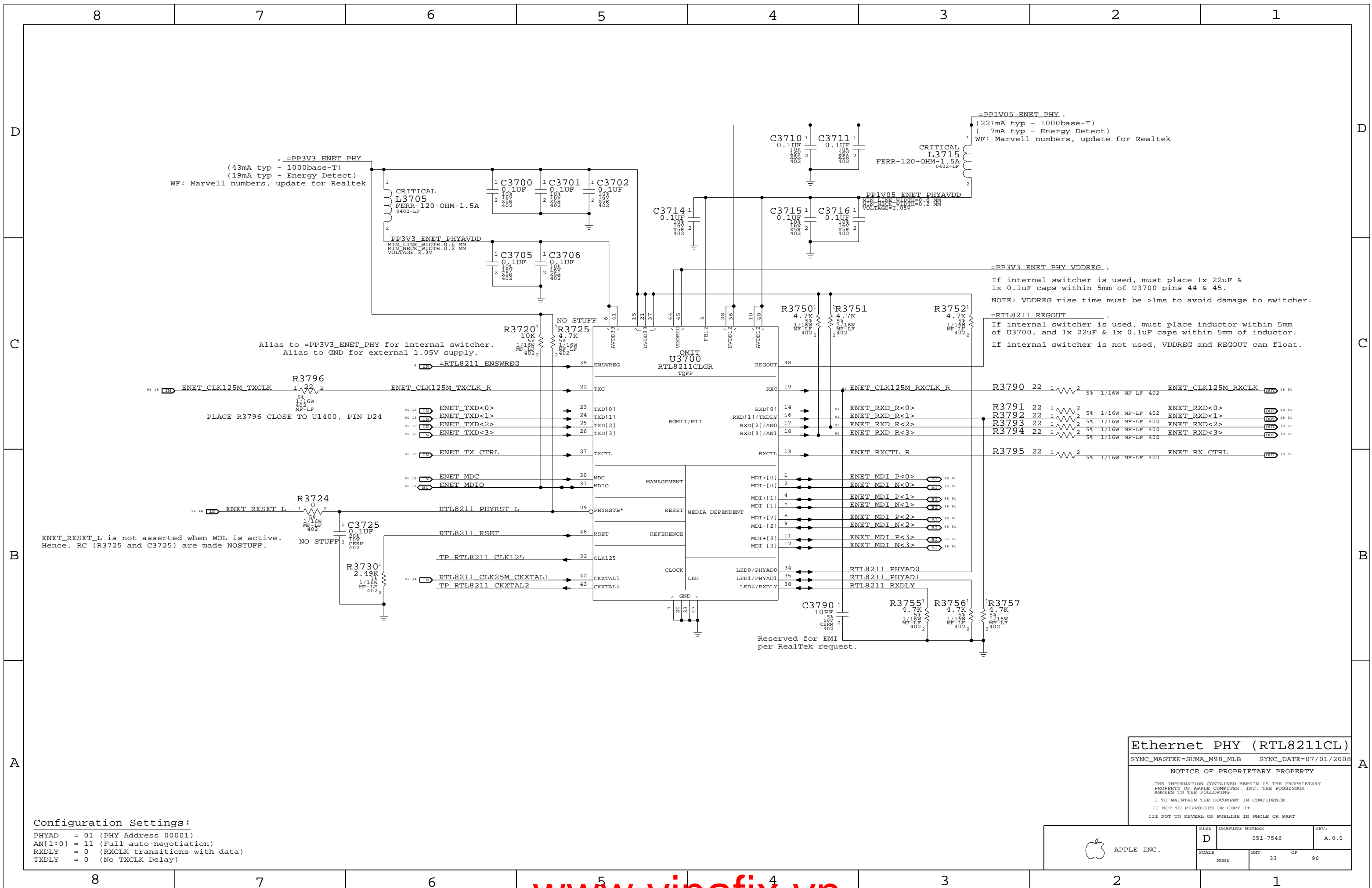
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	31	96	

EXPRESSCARD/34 FLEX CONNECTOR



ExpressCard Connector
 SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008
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	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	32		



=PP3V3_ENET_PHY
 (43mA typ - 1000base-T)
 (19mA typ - Energy Detect)
 WF: Marvell numbers, update for Realtek

=PP1V05_ENET_PHY.
 (221mA typ - 1000base-T)
 (7mA typ - Energy Detect)
 WF: Marvell numbers, update for Realtek

Alias to =PP3V3_ENET_PHY for internal switcher.
 Alias to GND for external 1.05V supply.

=PP3V3_ENET_PHY_VDDREG.
 If internal switcher is used, must place 1x 22uF & 1x 0.1uF caps within 5mm of U3700 pins 44 & 45.
 NOTE: VDDREG rise time must be >1ms to avoid damage to switcher.

=RTL8211_REGOUT.
 If internal switcher is used, must place inductor within 5mm of U3700, and 1x 22uF & 1x 0.1uF caps within 5mm of inductor.
 If internal switcher is not used, VDDREG and REGOUT can float.

ENET_RESET_L is not asserted when WOL is active.
 Hence, RC (R3725 and C3725) are made NOSTUFF.

Reserved for EMI per RealTek request.

Configuration Settings:
 PHYAD = 01 (PHY Address 00001)
 AN[1:0] = 11 (Full auto-negotiation)
 RXDLY = 0 (RXCLK transitions with data)
 TXDLY = 0 (No TXCLK Delay)

Ethernet PHY (RTL8211CL)
 SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

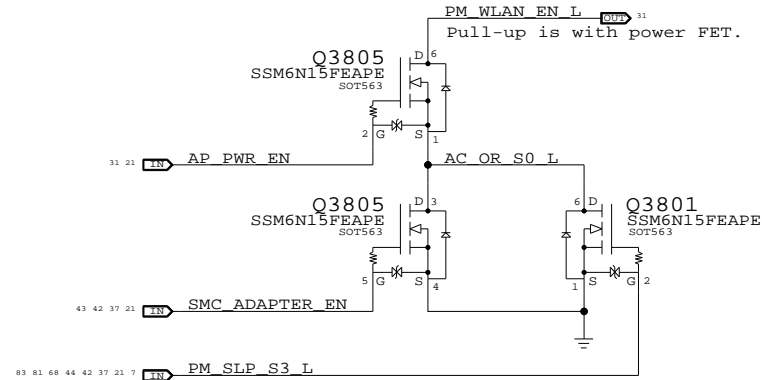
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	33	96	

WLAN Enable Generation

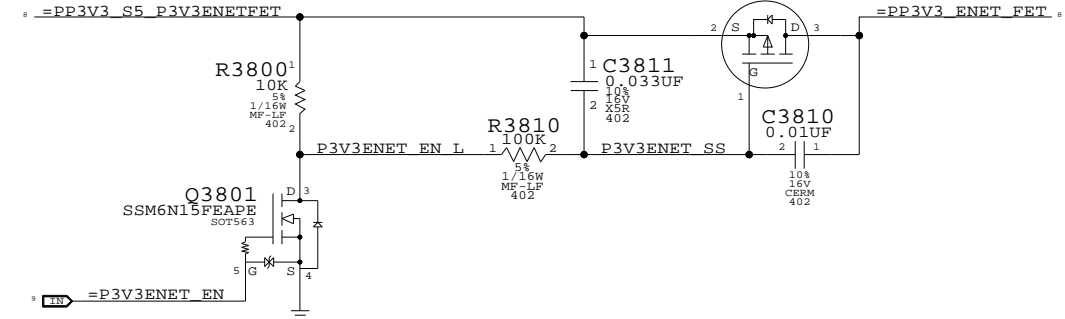
"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.



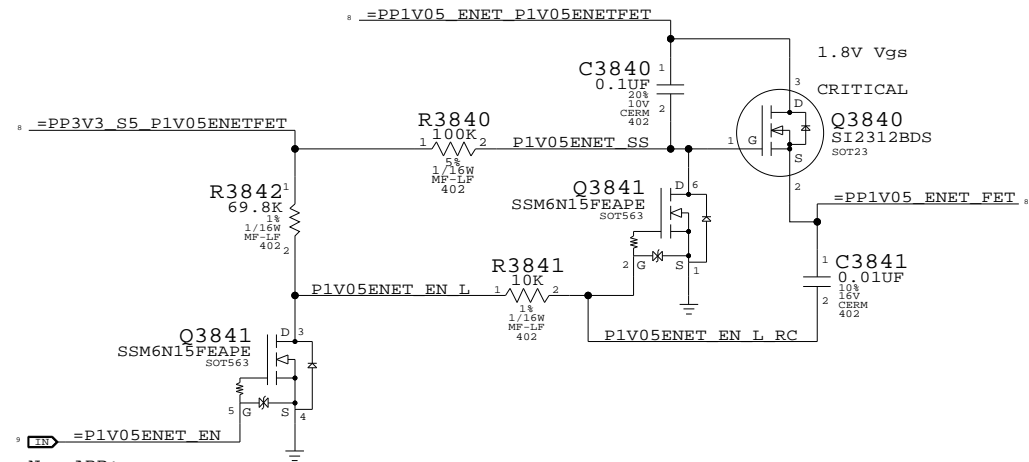
3.3V ENET FET

@ 2.5V Vgs: CRITICAL
 Rds(on) = 90mOhm max Q3810
 I(max) = 1.7A (85C) NTR4101P
 SOT-23-HP



MOBILE:
 Recommend aliasing PM_SLP_RMGT_L and =P3V3ENET_EN. Nets separated on ARB for alternate power options.

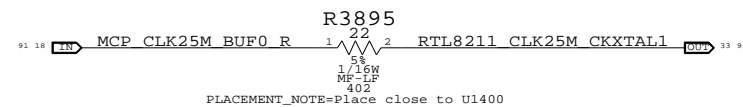
1.05V ENET FET



Non-ARB:
 Recommend aliasing PM_SLP_RMGT_L and =P1V05ENET_EN. Nets separated on ARB for alternate power options.

RTL8211 25MHz Clock

NOTE: MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.



PLACEMENT_NOTE=Place close to U1400

Ethernet & AirPort Support

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

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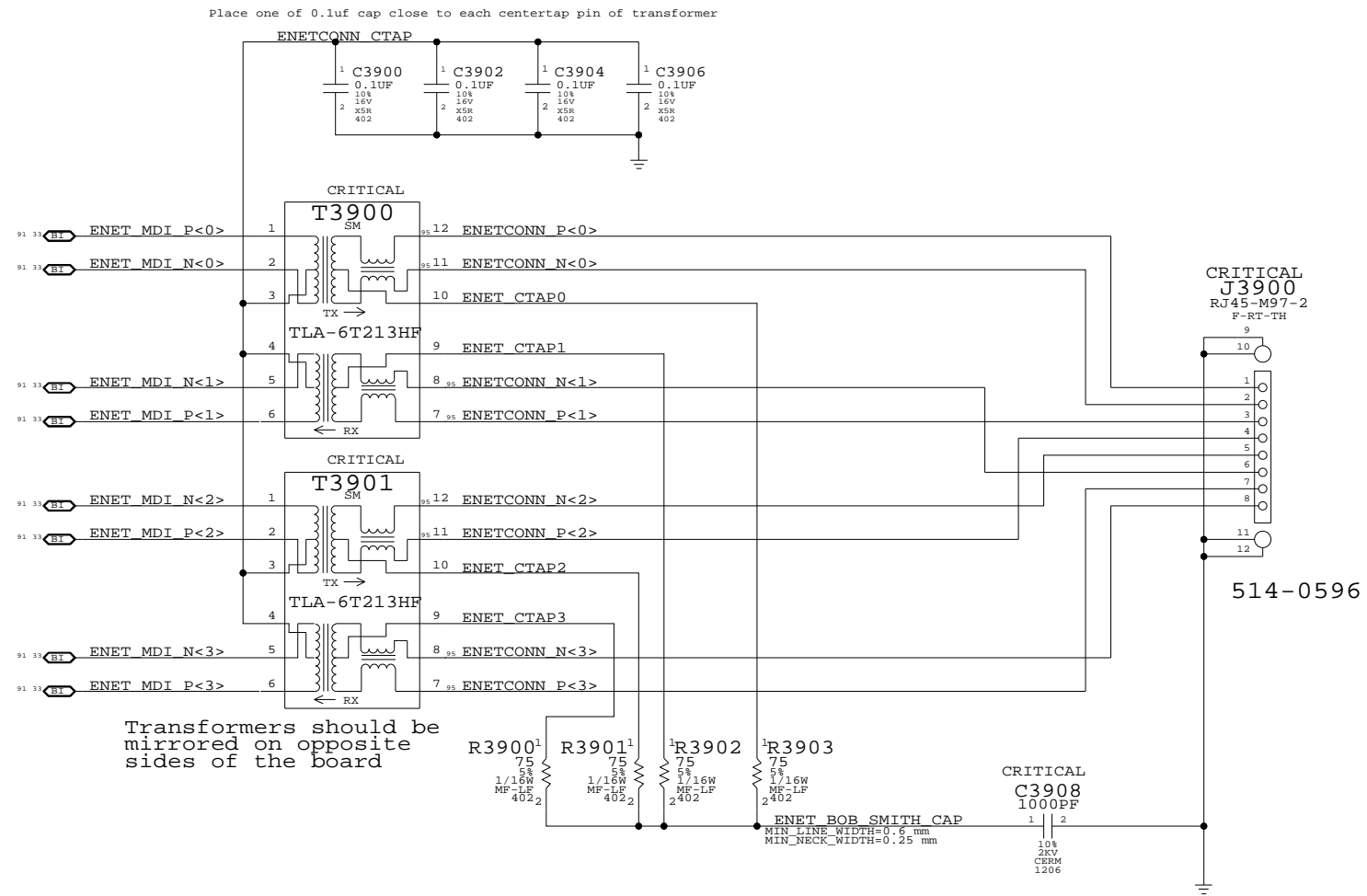
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	34	96	

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Ethernet Connector

SYNC_MASTER=SUMA_M98_MLB SYNC_DATE=07/01/2008

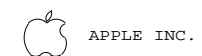
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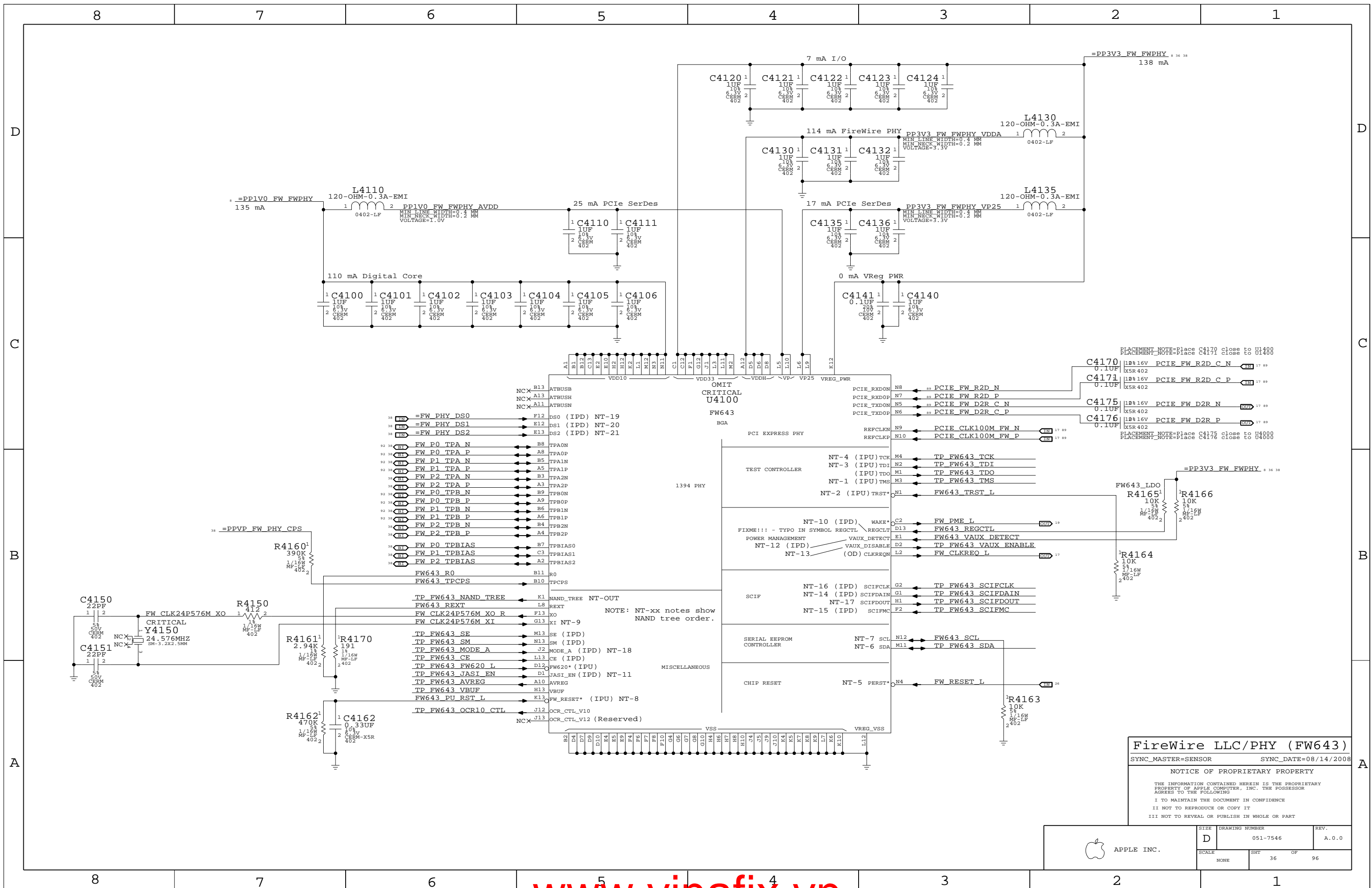
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APPLE INC.

SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	35	96



FireWire LLC/PHY (FW643)
 SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	36		

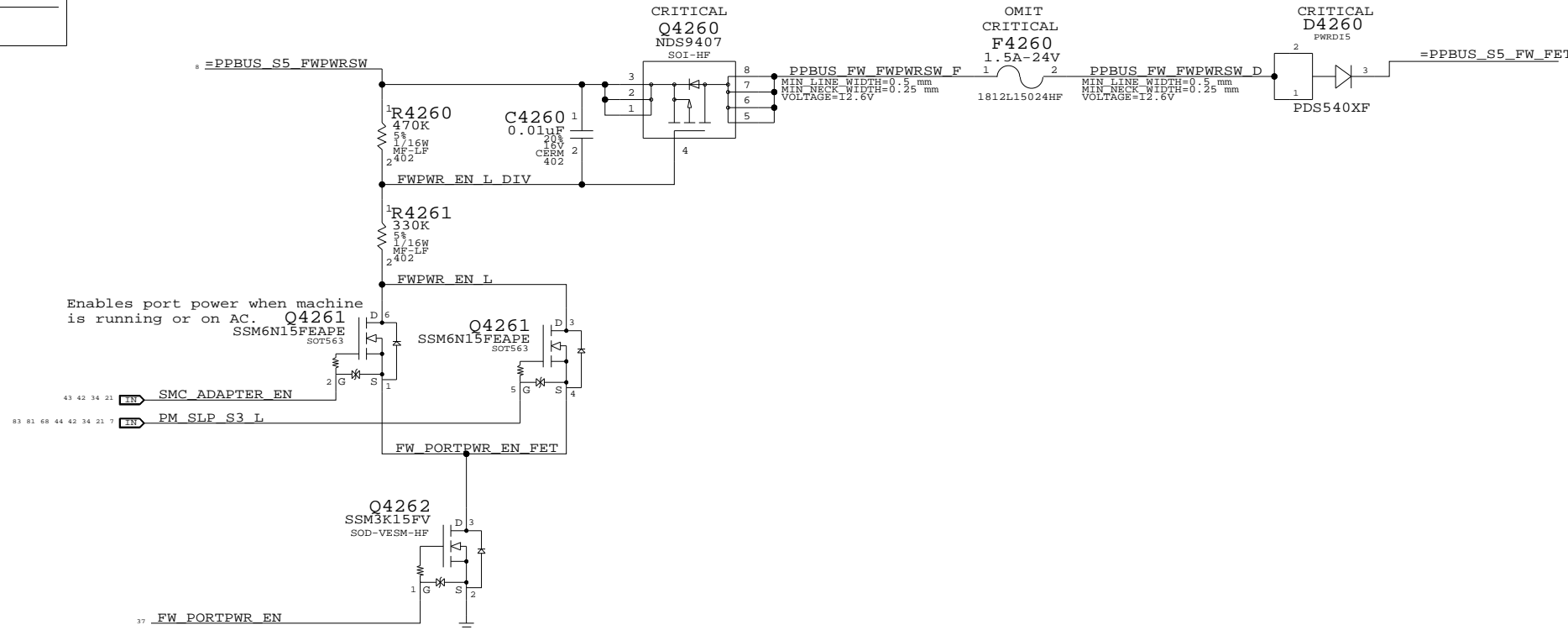
Page Notes

Power aliases required by this page:
 - =PPBUS_S5_FWPWSW (system supply for bus power)
 - =PP3V3_FW_LATEVG_ACTIVE
 - =PPVP_FW_SUMNODE (power passthru summation node)

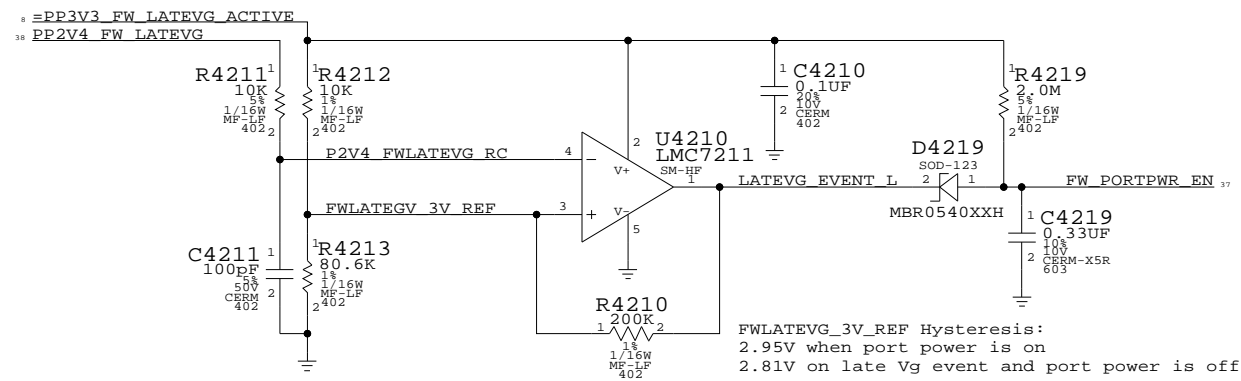
Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 - FW_PORT_FAULT_PU

FireWire Port Power Switch



Late-VG Event Detection



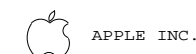
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
740S0080	1	LITTLEFUSE, 1.5A RESETTABLE 24V	F4260	CRITICAL	

FireWire Port Power

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	37	96

Page Notes

Power aliases required by this page:
 - =PPVP_FW_PORT1
 - =PP3V3_FW_LATEVG

Signal aliases required by this page:
 (NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

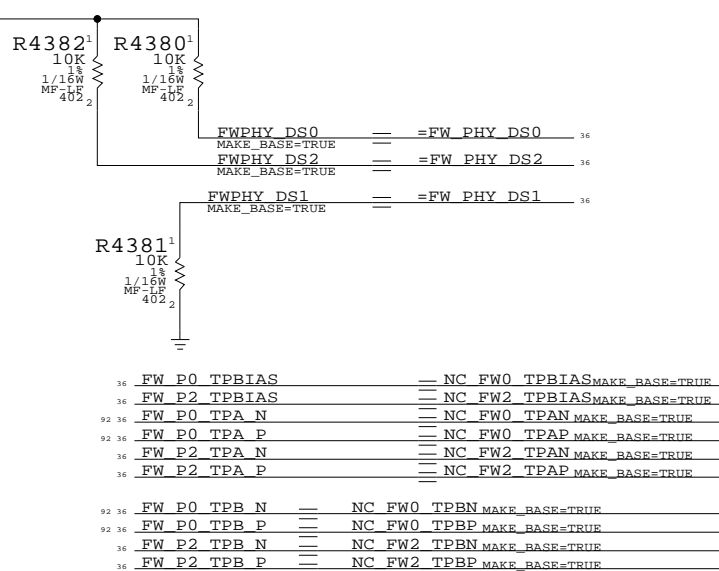
BOM options provided by this page:
 (NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

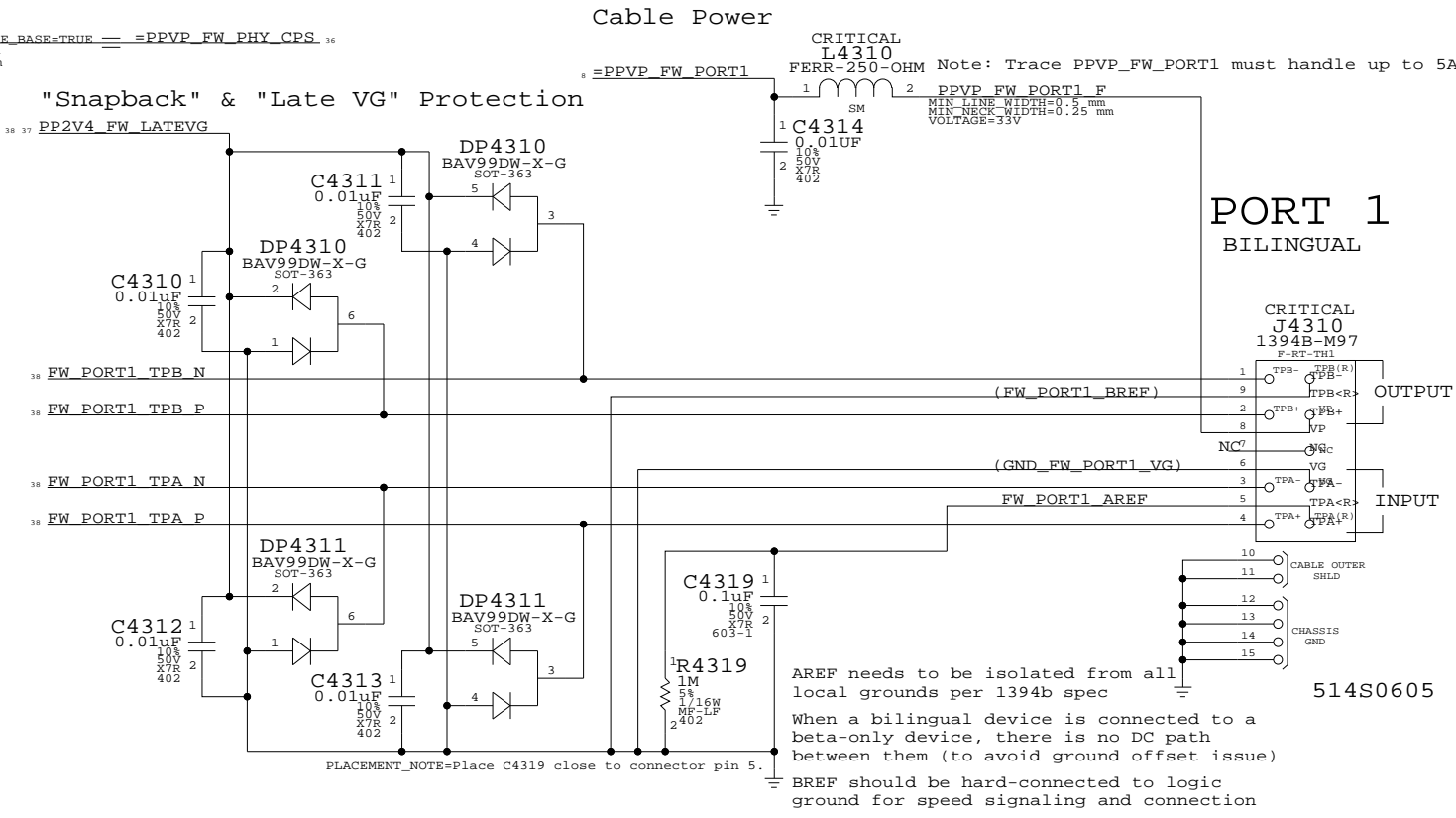
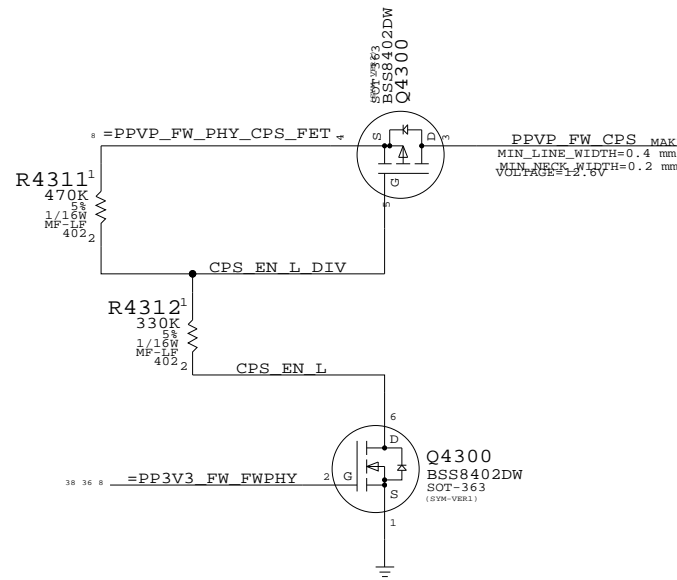
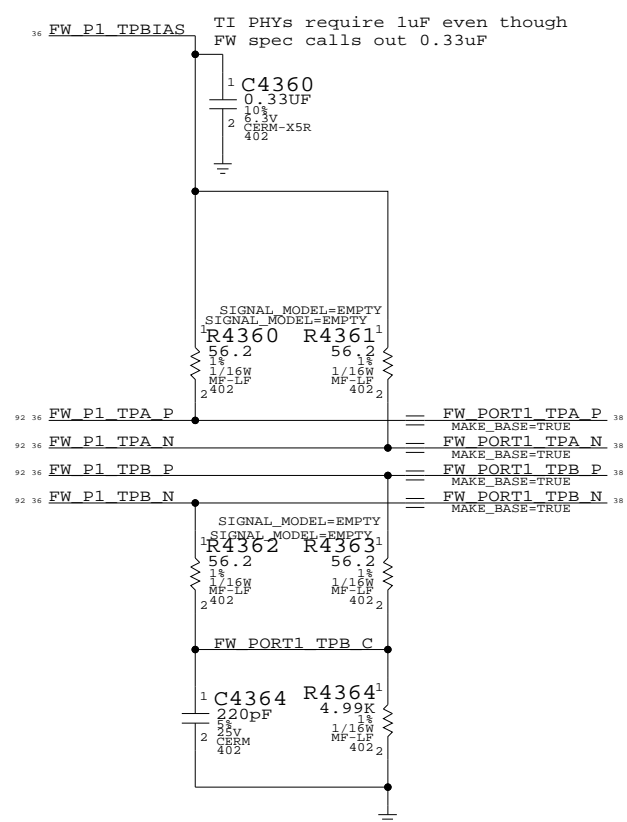
FireWire PHY Config Straps

Configures PHY for:
 - 1-port Portable Power Class (0)
 - Port "1" Bilingual (1394B)

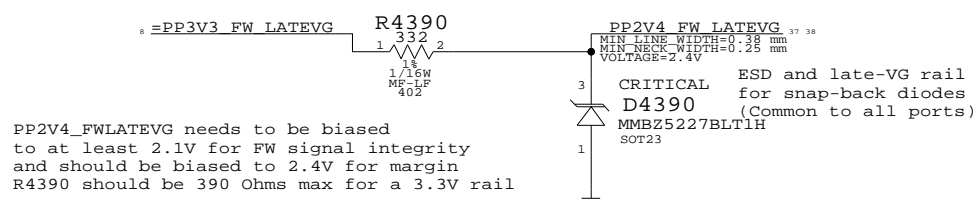


Termination

Place close to FireWire PHY



Late-VG Protection Power



FireWire Ports

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

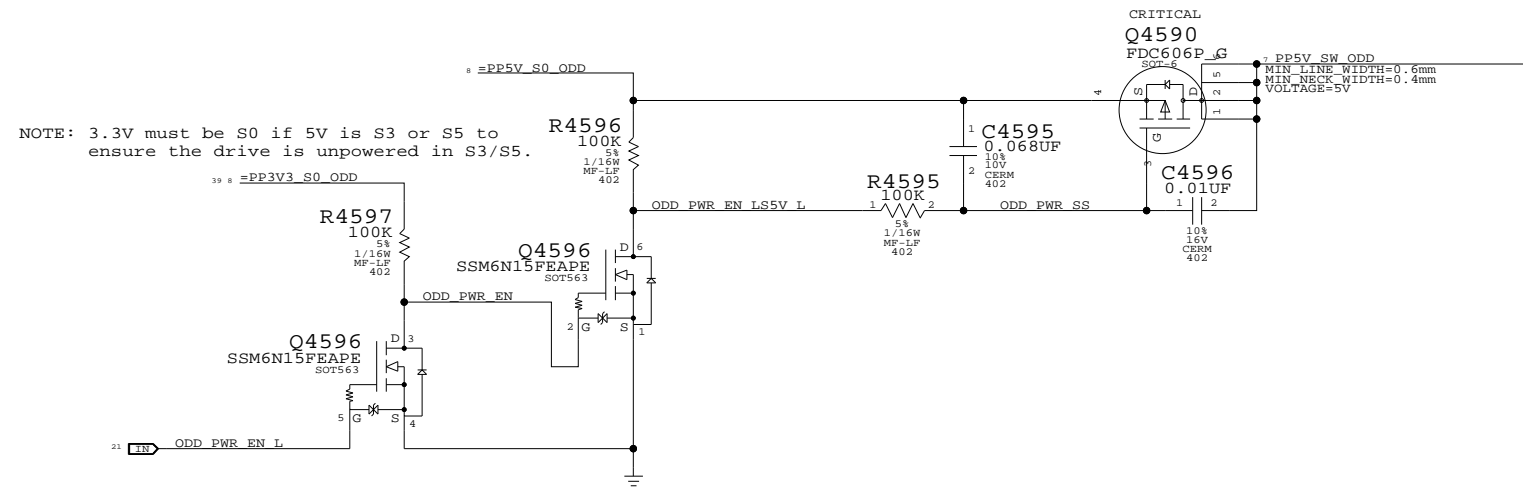
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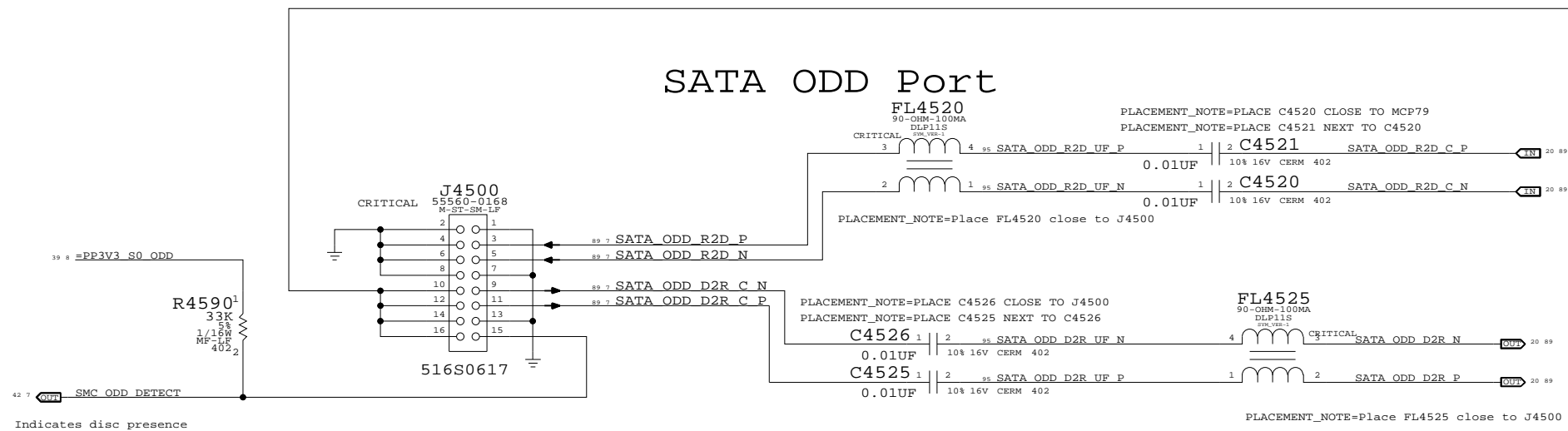
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	38		

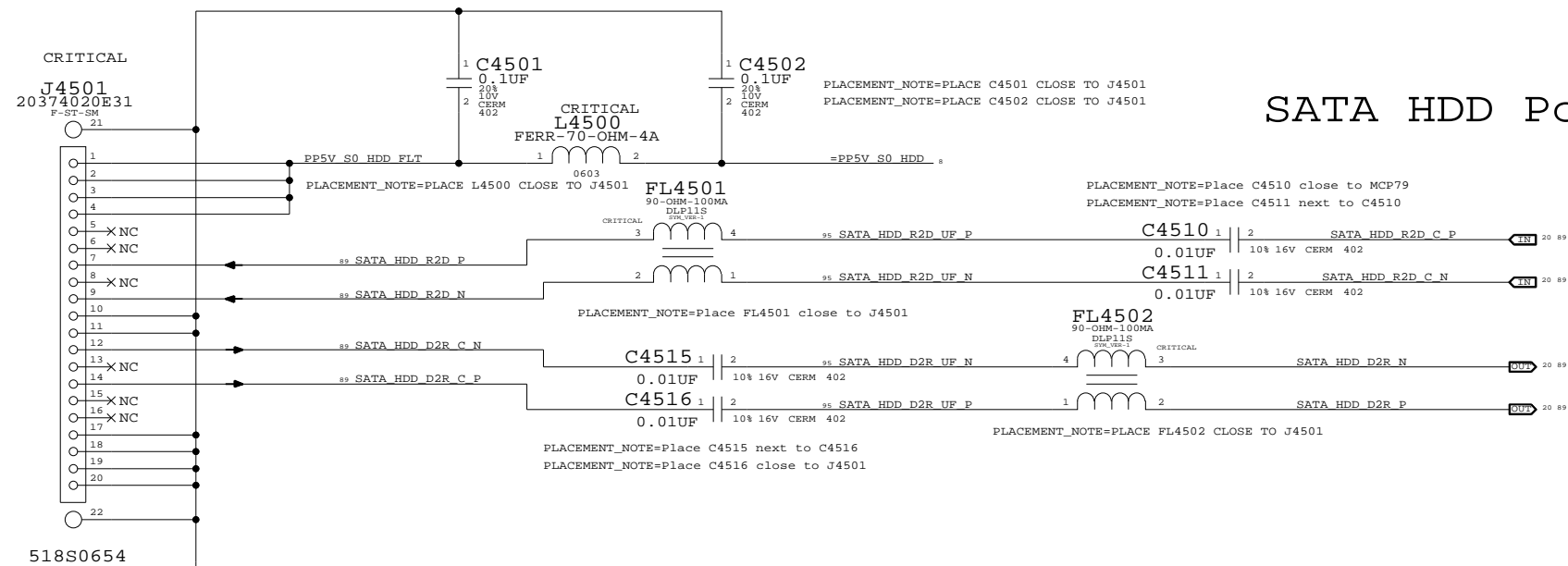
ODD Power Control



SATA ODD Port

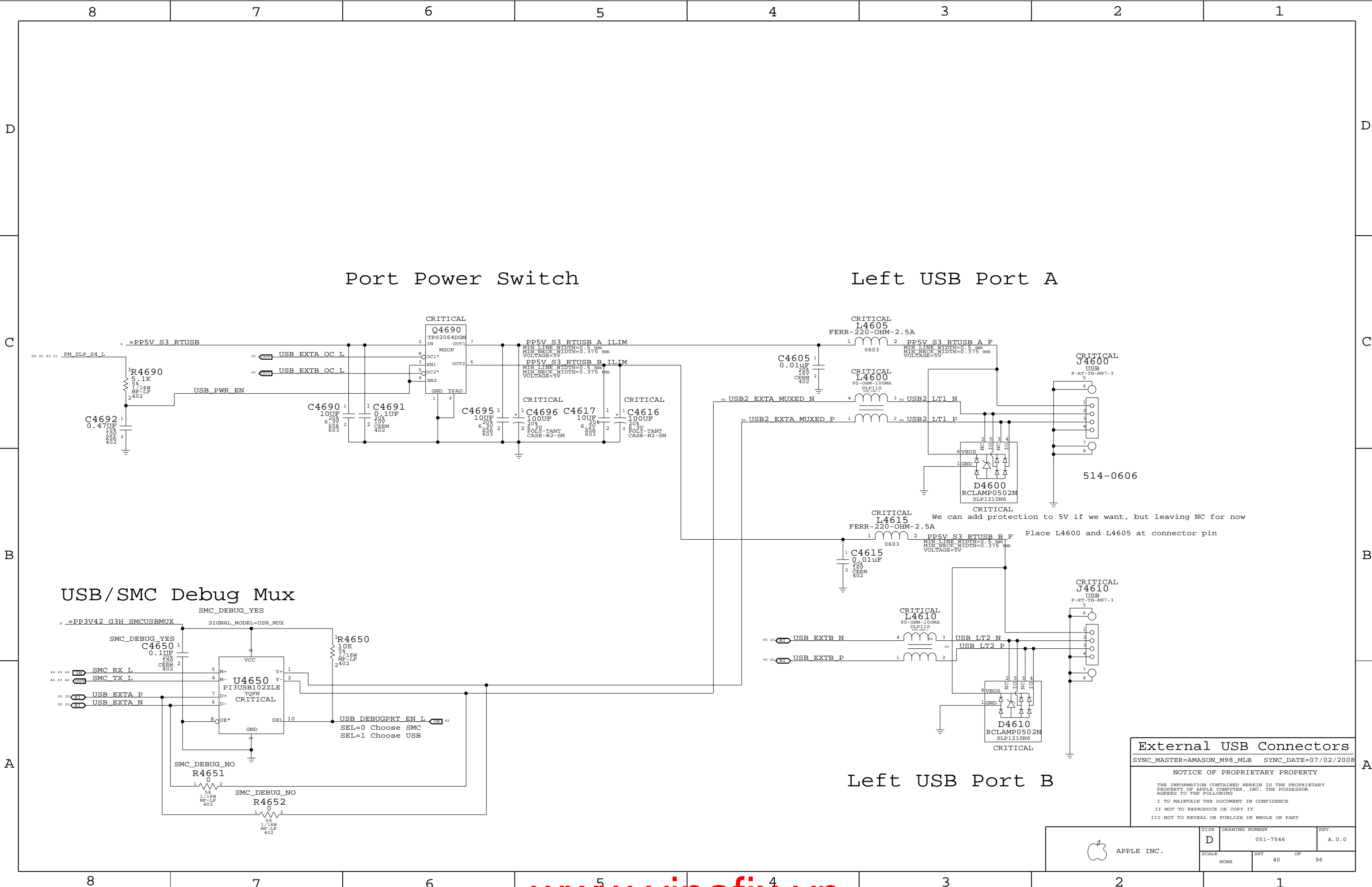


SATA HDD Port



SATA Connectors		
SYNC_MASTER=CHANG_M98_MLB	SYNC_DATE=07/01/2008	
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	39	96	



Port Power Switch

Left USB Port A

USB/SMC Debug Mux

Left USB Port B

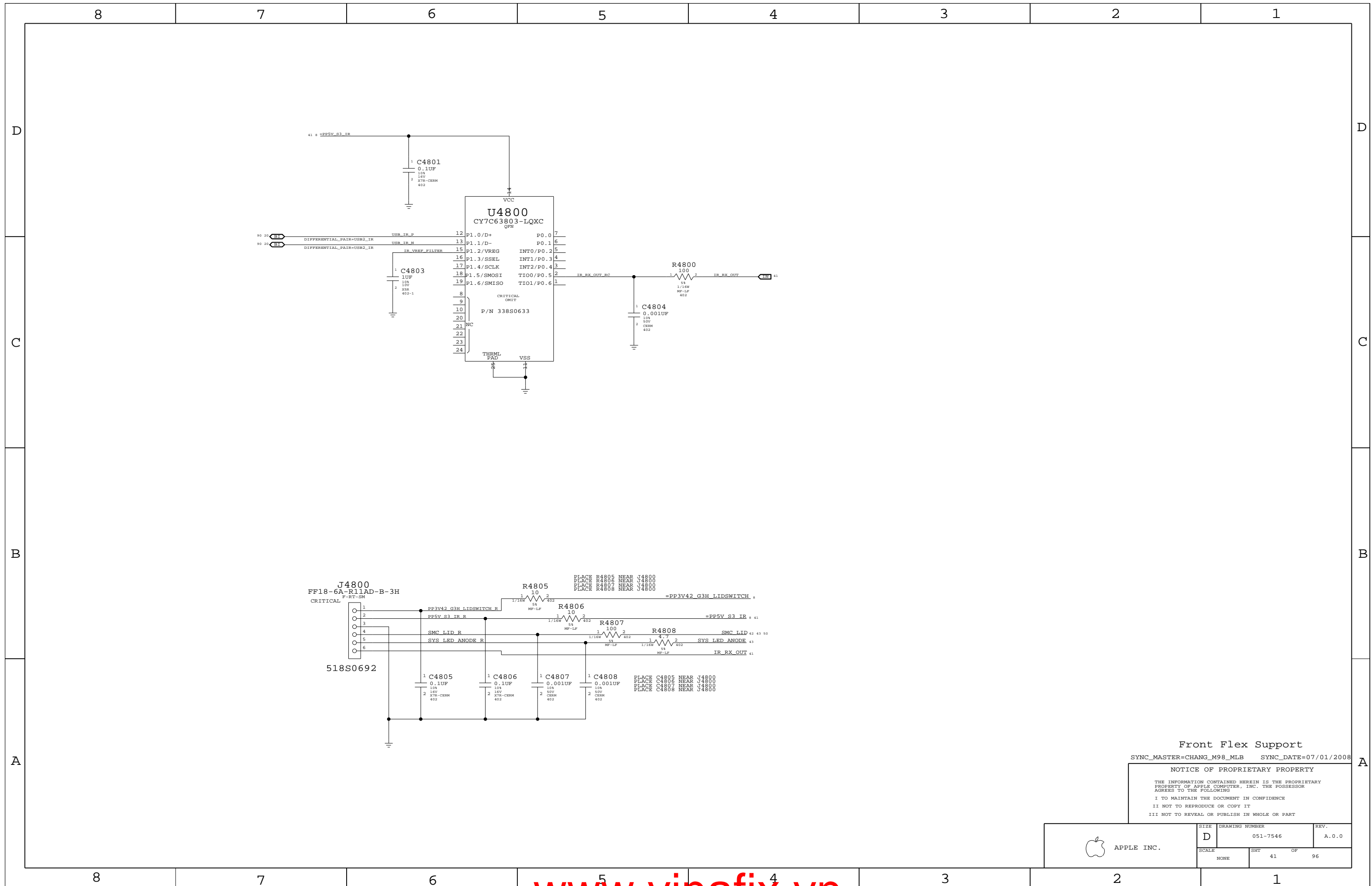
External USB Connectors

SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=07/02/2008

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SCALE	SHT		OF
NONE	40		96

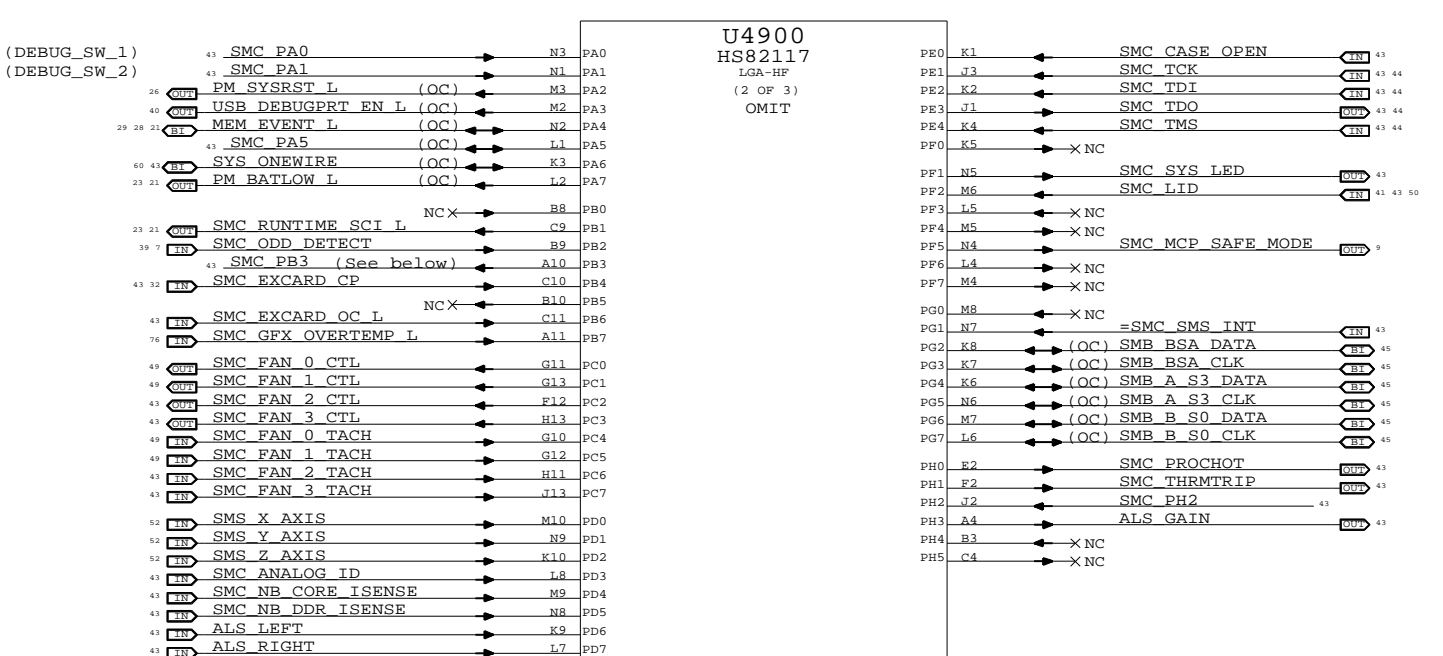
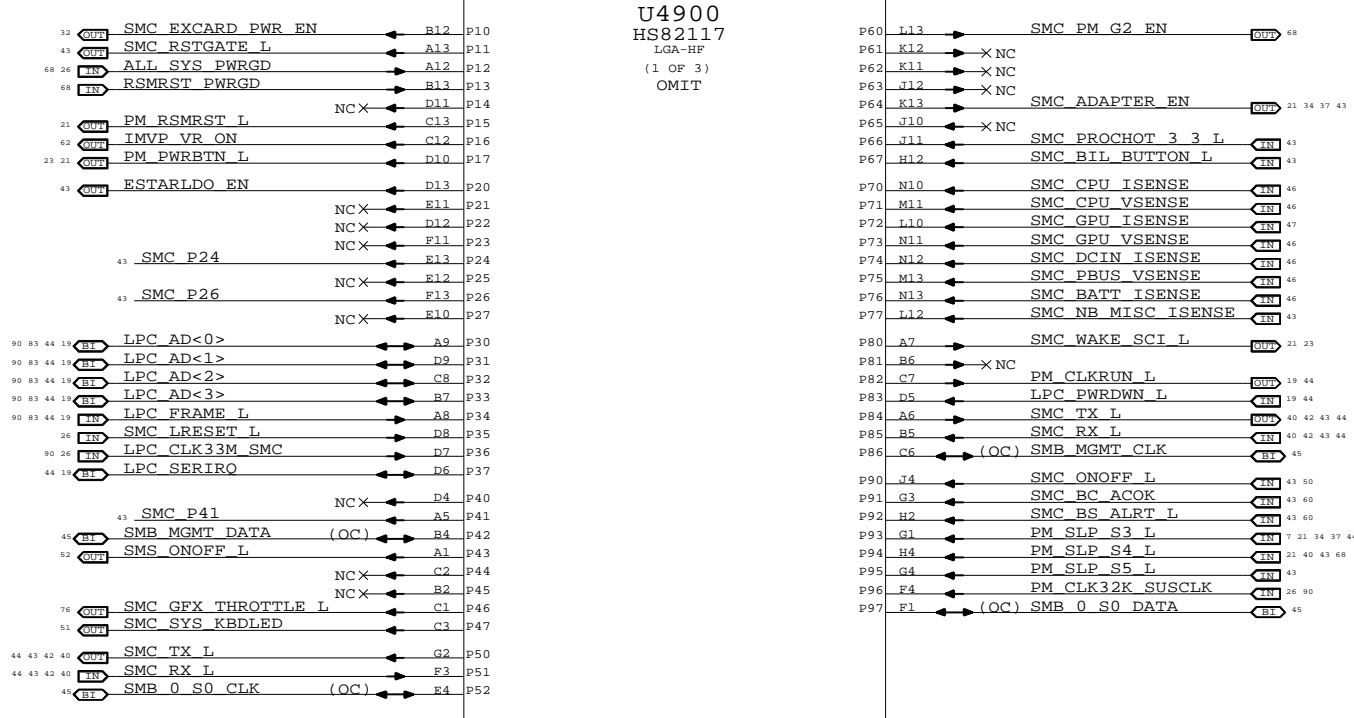


Front Flex Support
 SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

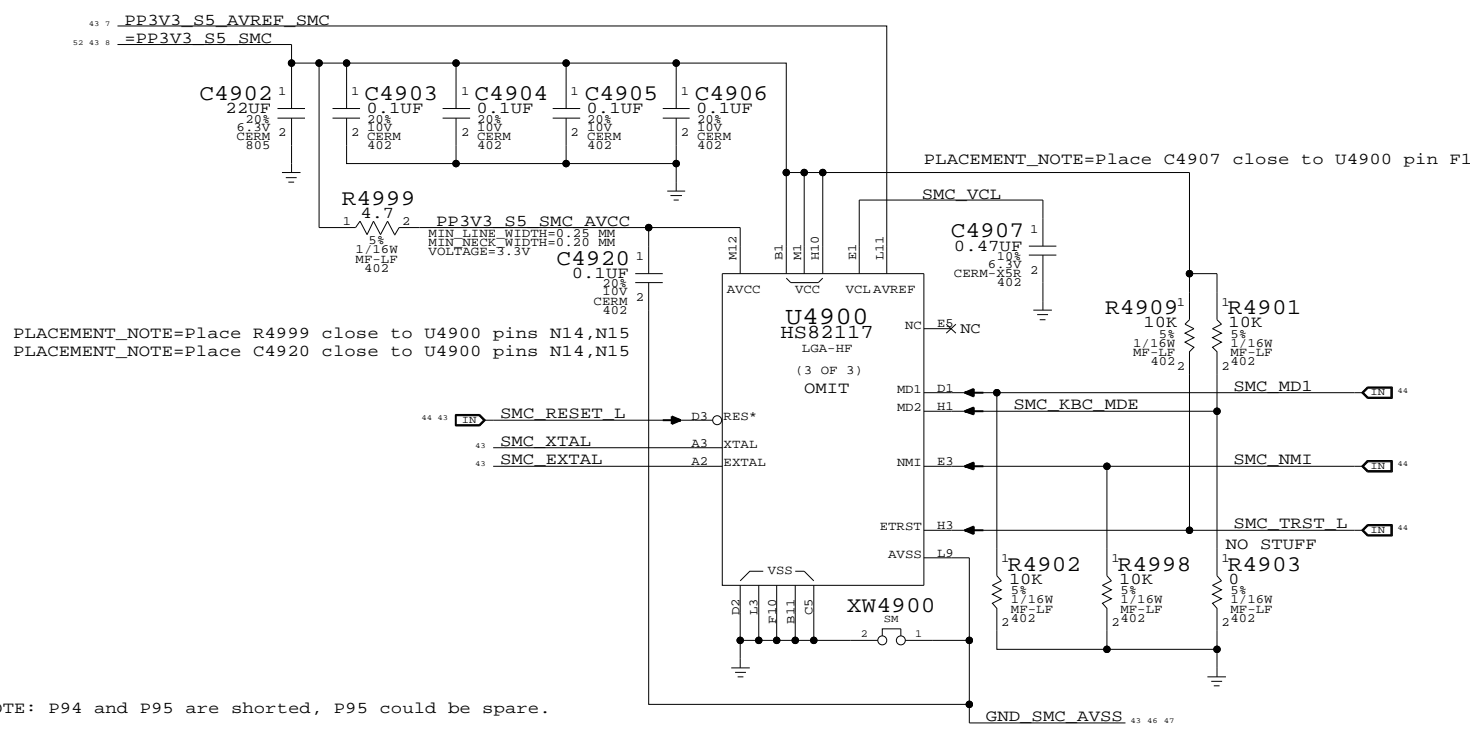
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	D	051-7546	A.0.0
SCALE	SHT		OF
NONE	41		96

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



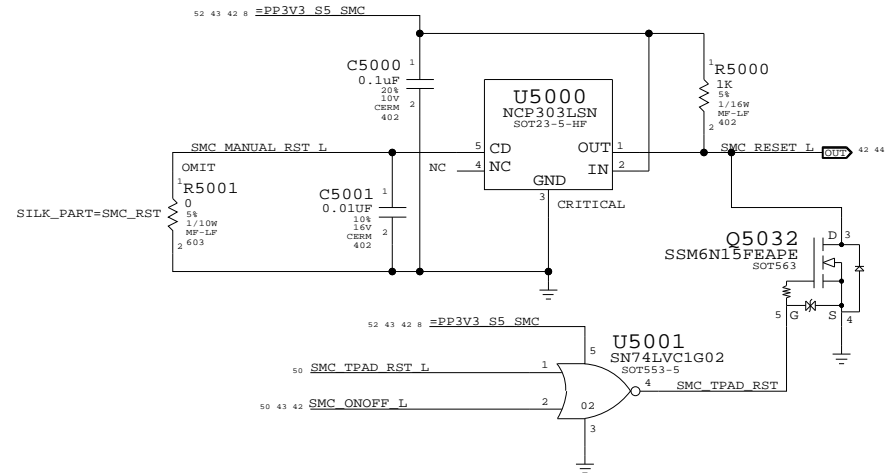
SMC_PB3:
SMC_IG_THROTTLE_L for MG systems.
Otherwise, TP/NC okay (was ISENSE_CAL_EN)



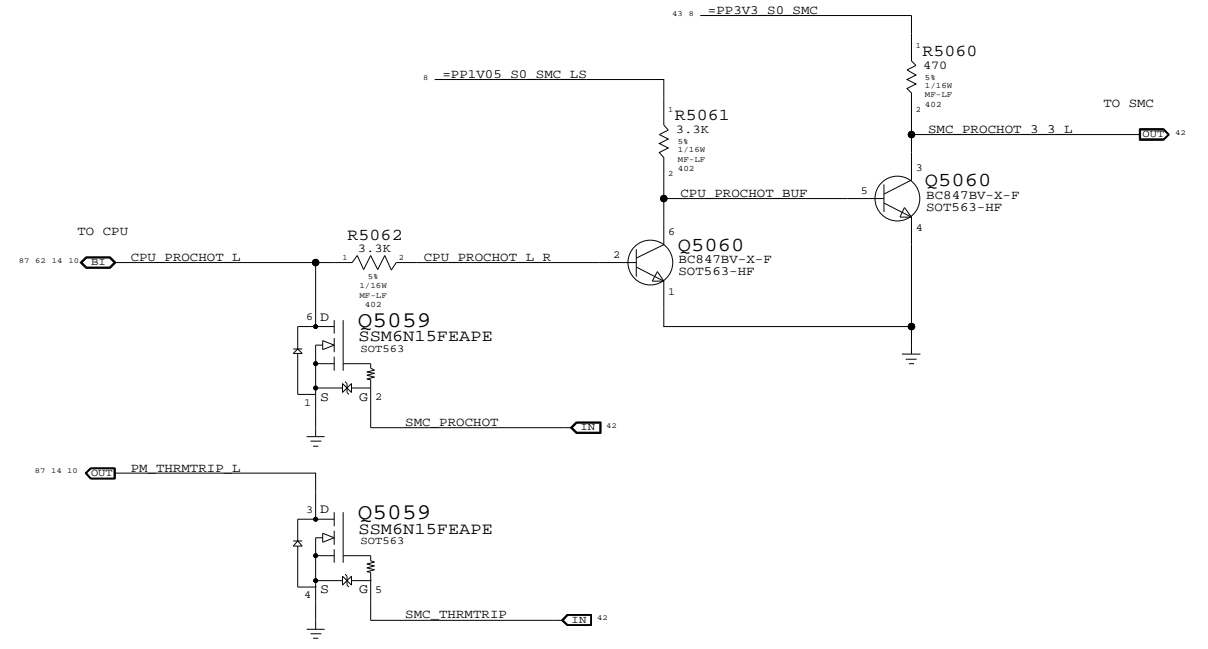
SMC
SYNC_MASTER=T18_MLB SYNC_DATE=06/18/2008
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
	SCALE NONE	SHT 42 OF 96	

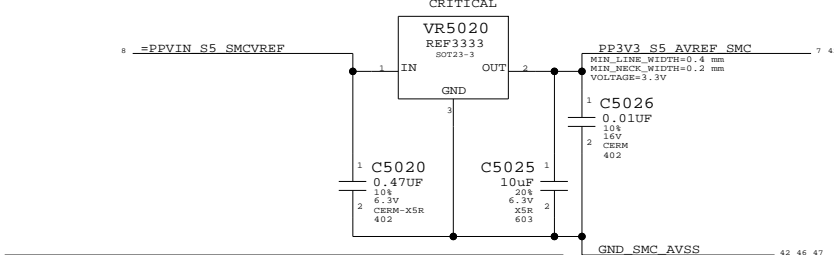
SMC Reset "Button" / Brownout Detect



SMC FSB to 3.3V Level Shifting

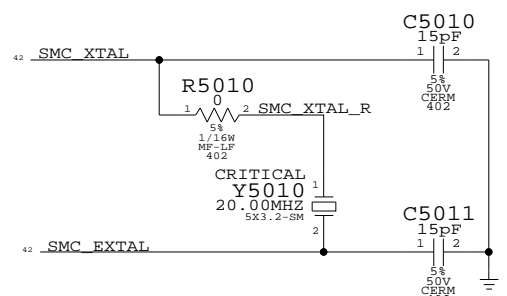


SMC AVREF Supply

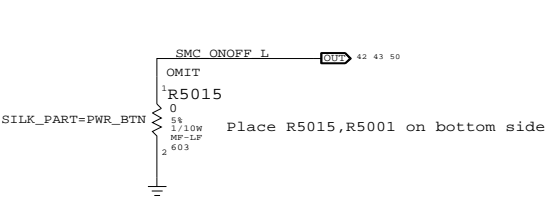


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
35381381	35381278		ALL	Inter@11 18L40002-33

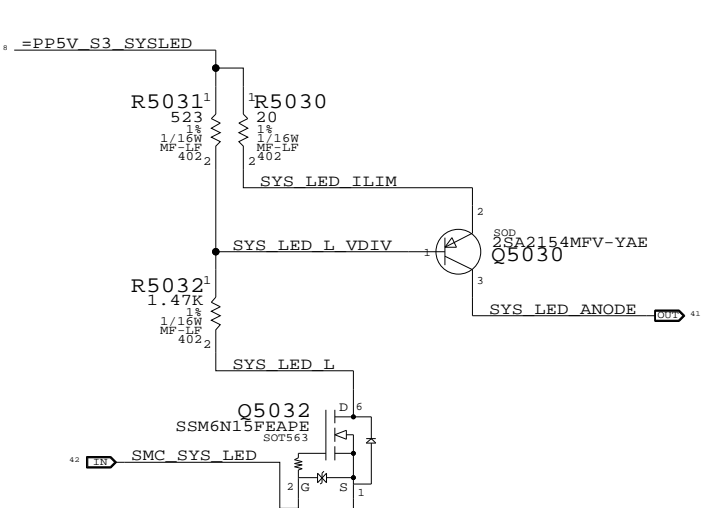
SMC Crystal Circuit



Debug Power "Button"



System (Sleep) LED Circuit



- 42 _SMC_FAN_2_CTL == NC_SMC_FAN_2_CTL
- 42 _SMC_FAN_2_TACH == MAKE_BASE=TRUE
- 42 _SMC_FAN_3_CTL == NC_SMC_FAN_3_CTL
- 42 _SMC_FAN_3_TACH == MAKE_BASE=TRUE
- 42 _ESTARLDO_EN == NC_ESTARLDO_EN
- 42 _SMC_BC_ACOK == =CHGR_ACOK
- 42 _ALS_LEFT == SMC_MCP_VSENSE
- 42 _ALS_RIGHT == SMC_CPU_HI_ISENSE
- 42 _SMC_NB_CORE_ISENSE == SMC_MCP_CORE_ISENSE
- 42 _SMC_NB_DDR_ISENSE == SMC_MCP_DDR_ISENSE
- 42 _SMC_NB_MISC_ISENSE == SMC_CPU_FSB_ISENSE
- 42 _SMC_ANALOG_ID == SMC_CPU_IV8_ISENSE
- 42 _SMC_P24 == TP_SMC_P24
- 42 _SMC_P26 == SMC_BMON_MUX_SEL
- 42 _SMC_P41 == TP_SMC_P41
- 42 _ALS_GAIN == NC_ALS_GAIN
- 42 _SMC_PB3 == SMC_IG_THROTTLE_L
- 42 _SMC_RSTGATE_L == TP_SMC_RSTGATE_L

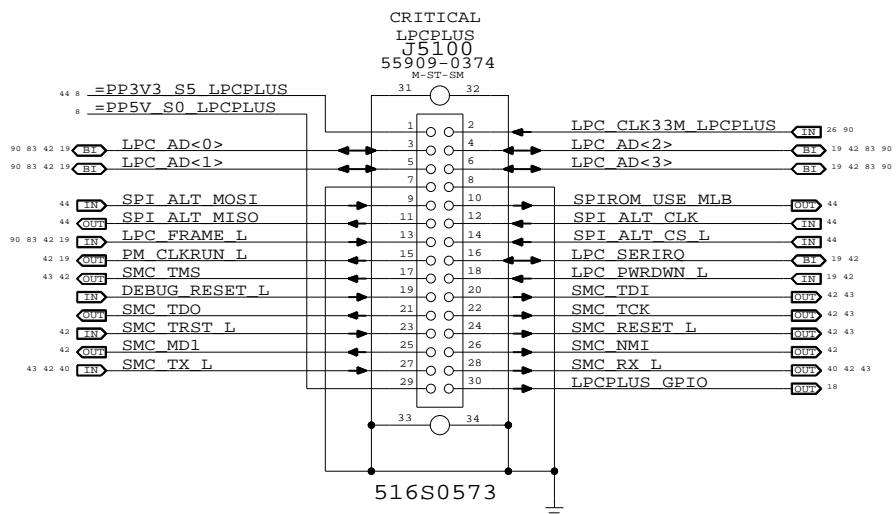
- 42 _SMC_PA0 R5091 100K
- 42 _SMC_PA1 R5092 100K
- 42 _SMC_ONOFF_L R5070 10K
- 42 _SMC_LID R5071 100K
- 42 _SMC_PH2 R5072 10K
- 42 _SMC_TX_L R5073 10K
- 42 _SMC_RX_L R5074 100K
- 42 _SYS_ONEWIRE R5075 2.0K
- 42 _SMC_BS_ALERT_L R5076 100K
- 42 _SMC_TMS R5077 10K
- 42 _SMC_TDO R5078 10K
- 42 _SMC_TDI R5079 10K
- 42 _SMC_TCK R5080 10K
- 42 _SMC_BIL_BUTTON_L R5081 10K
- 42 _SMC_BC_ACOK R5087 470K

- 42 37 34 21 _SMC_ADAPTER_EN R5085 10K
- 42 _SMC_CASE_OPEN R5086 10K
- 42 32 _SMC_EXCARD_CP R5088 10K
- 42 _PM_SLP_S5_L R5090 100K
- 42 _SMC_PA5 R5089 10K

SMC Support
 SYNC_MASTER=AMASON_M98_MLB SYNC_DATE=06/18/2008
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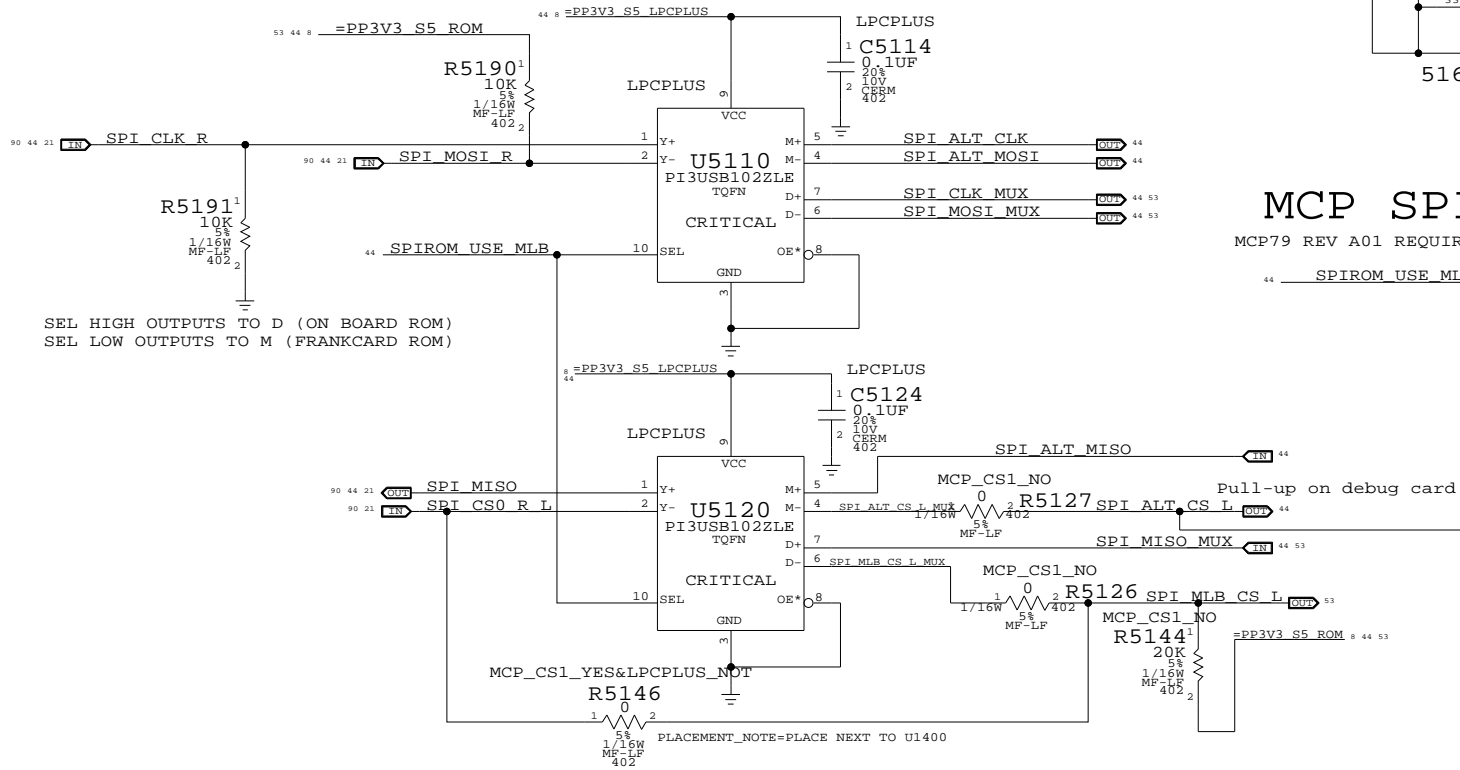
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	43 OF 96

LPC+SPI Connector



Alternate SPI ROM Support

MUX SEL CONTROLLED BY FRANKCARD SWITCH ONCE CS1 IS SUPPORTED IN MCP



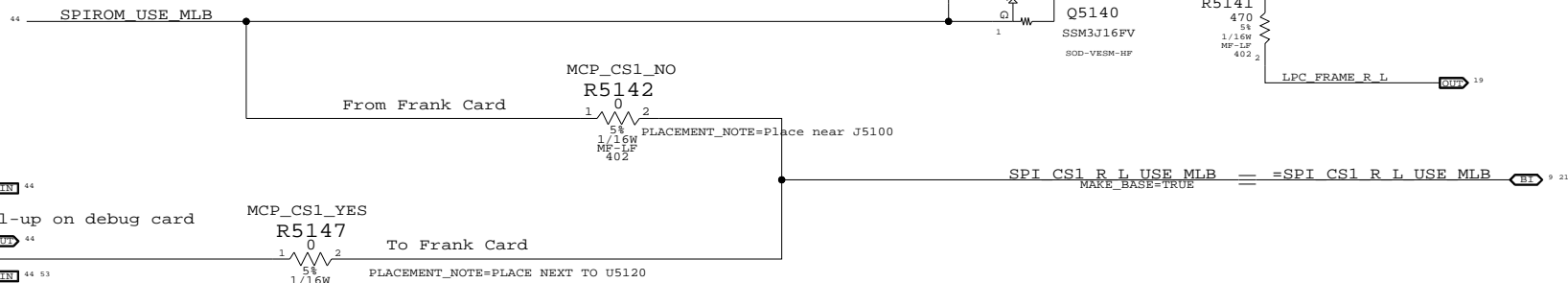
SEL HIGH OUTPUTS TO D (ON BOARD ROM)
SEL LOW OUTPUTS TO M (FRANKCARD ROM)

MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

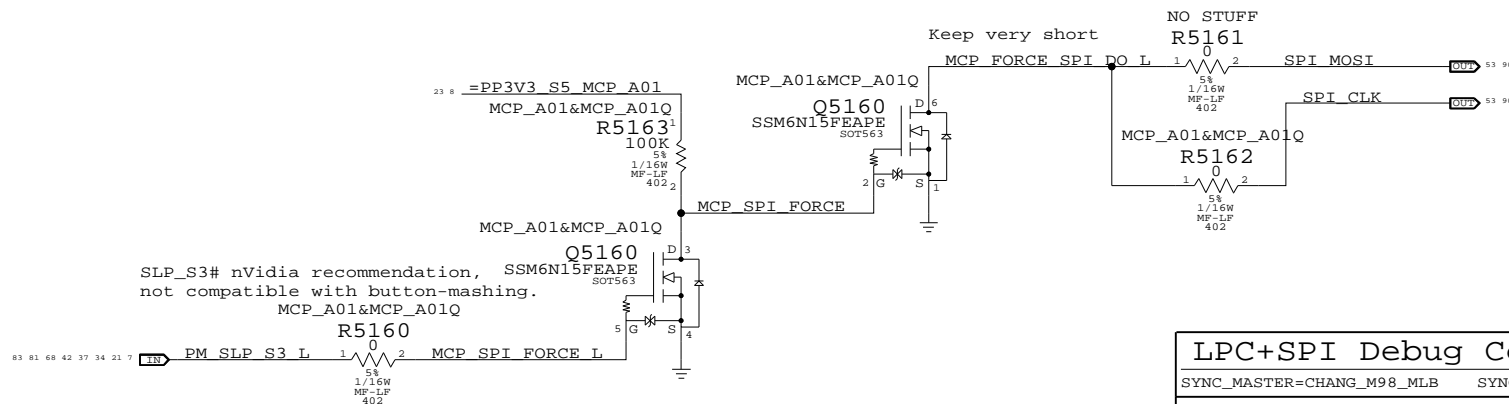
MCP SPI Override Options

MCP79 REV A01 REQUIRES EXTERNAL MUX, REV B01 STILL DOES NOT SUPPORT INTERNAL MUX

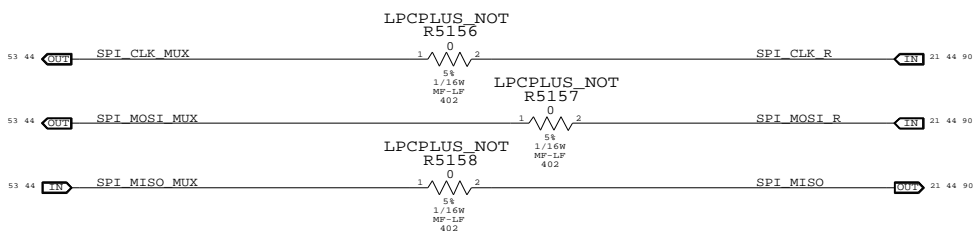


SPI Frequency Clamp

ENSURES MCP79 SPI_DO OR SPI_CLK INPUT IS LOW WHEN STRAP IS LATCHED. NOT NEEDED FOR B01 OR LATER.



SPI MUX BYPASS



LPC+SPI Debug Connector

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

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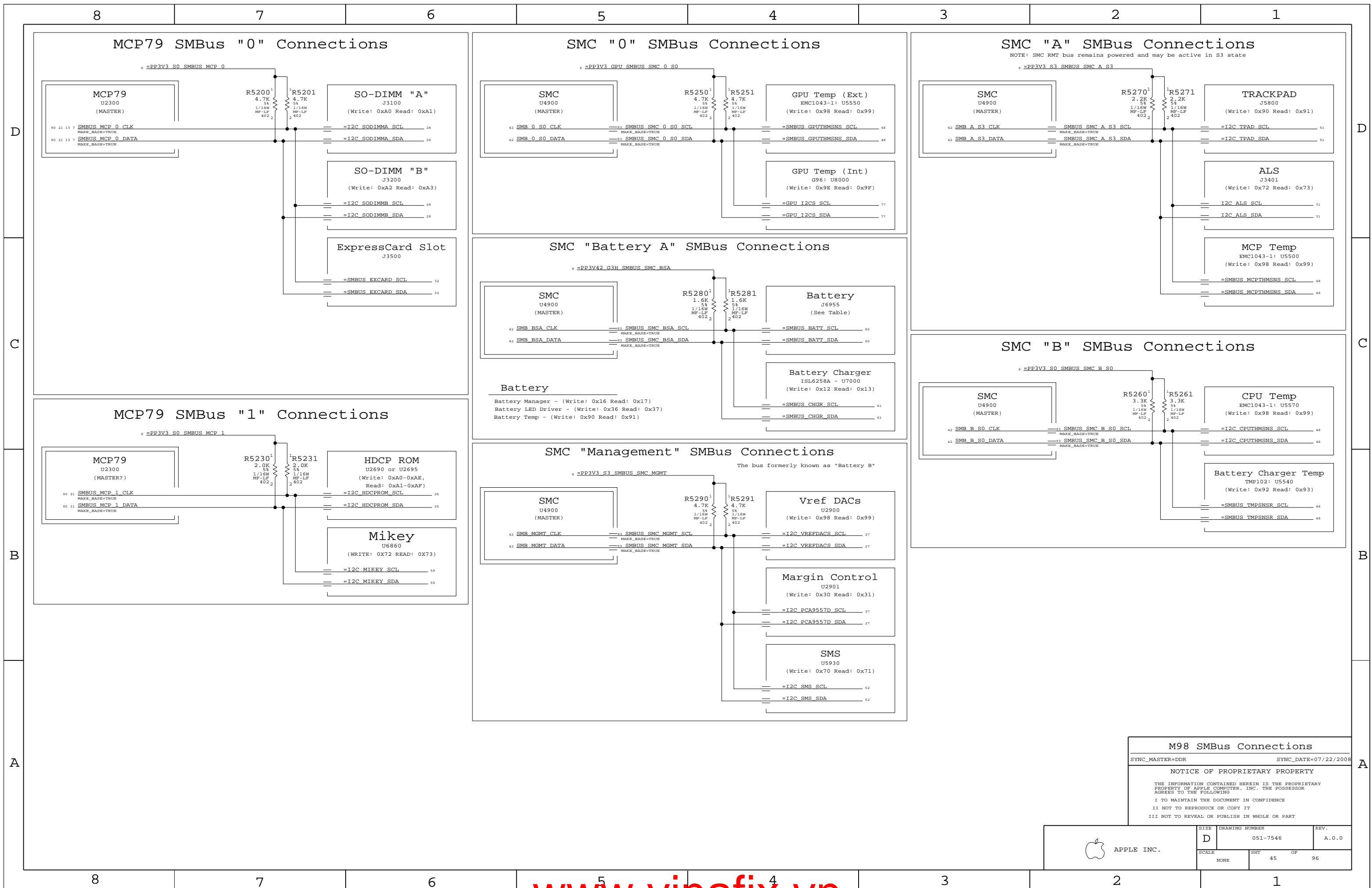
APPLE INC.

SIZE DRAWING NUMBER REV.

D 051-7546 A.0.0

SCALE SHEET OF

NONE 44 OF 96



D

D

C

C

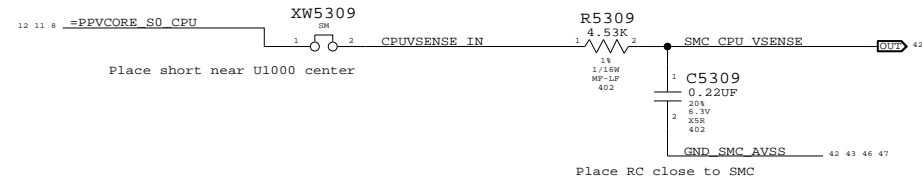
B

B

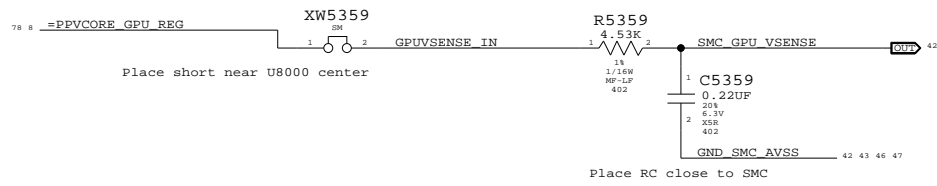
A

A

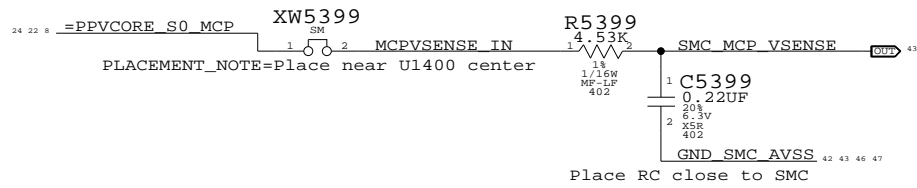
CPU Voltage Sense / Filter



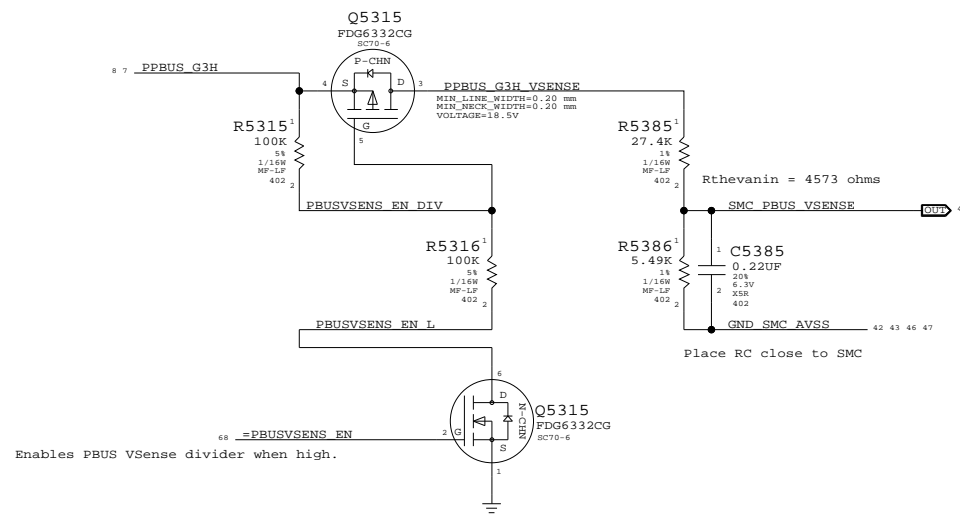
GPU Voltage Sense / Filter



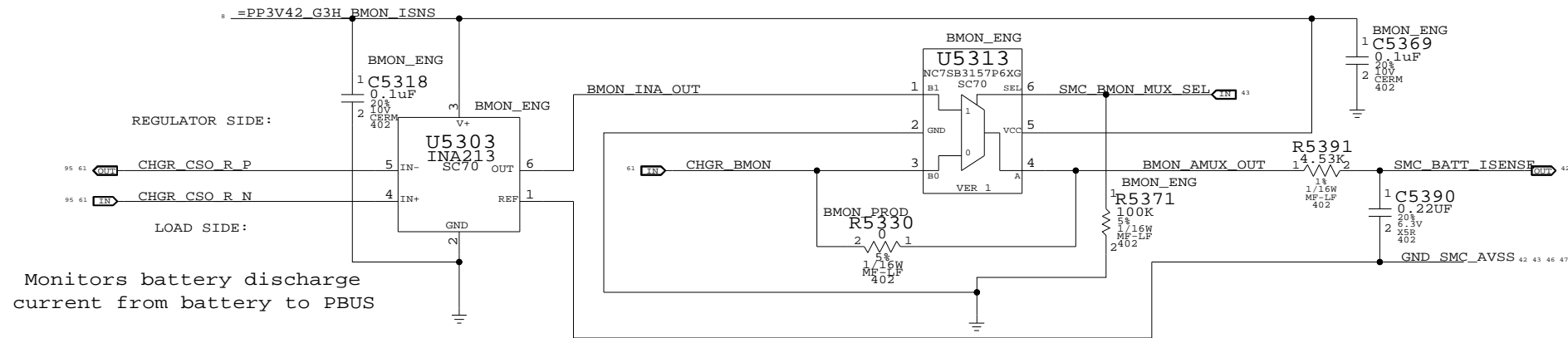
MCP Voltage Sense / Filter



PBUS Voltage Sense & Filter

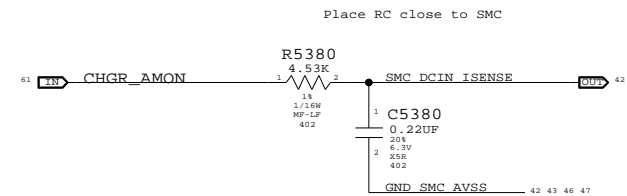


BMON Current Sense - Entire circuit must be near SMC (U4900)

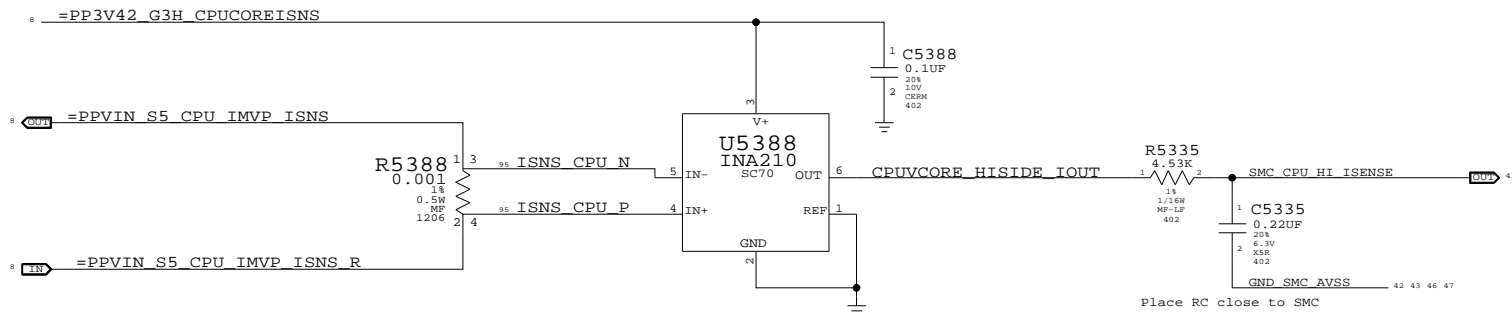


INA213 has gain of 50V/V

DCIN Current Sense Filter

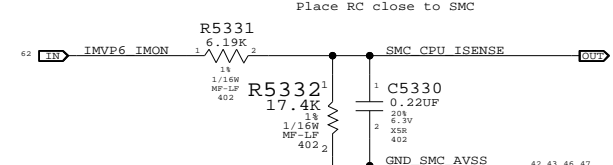


CPU VCore High Side Current Sensor



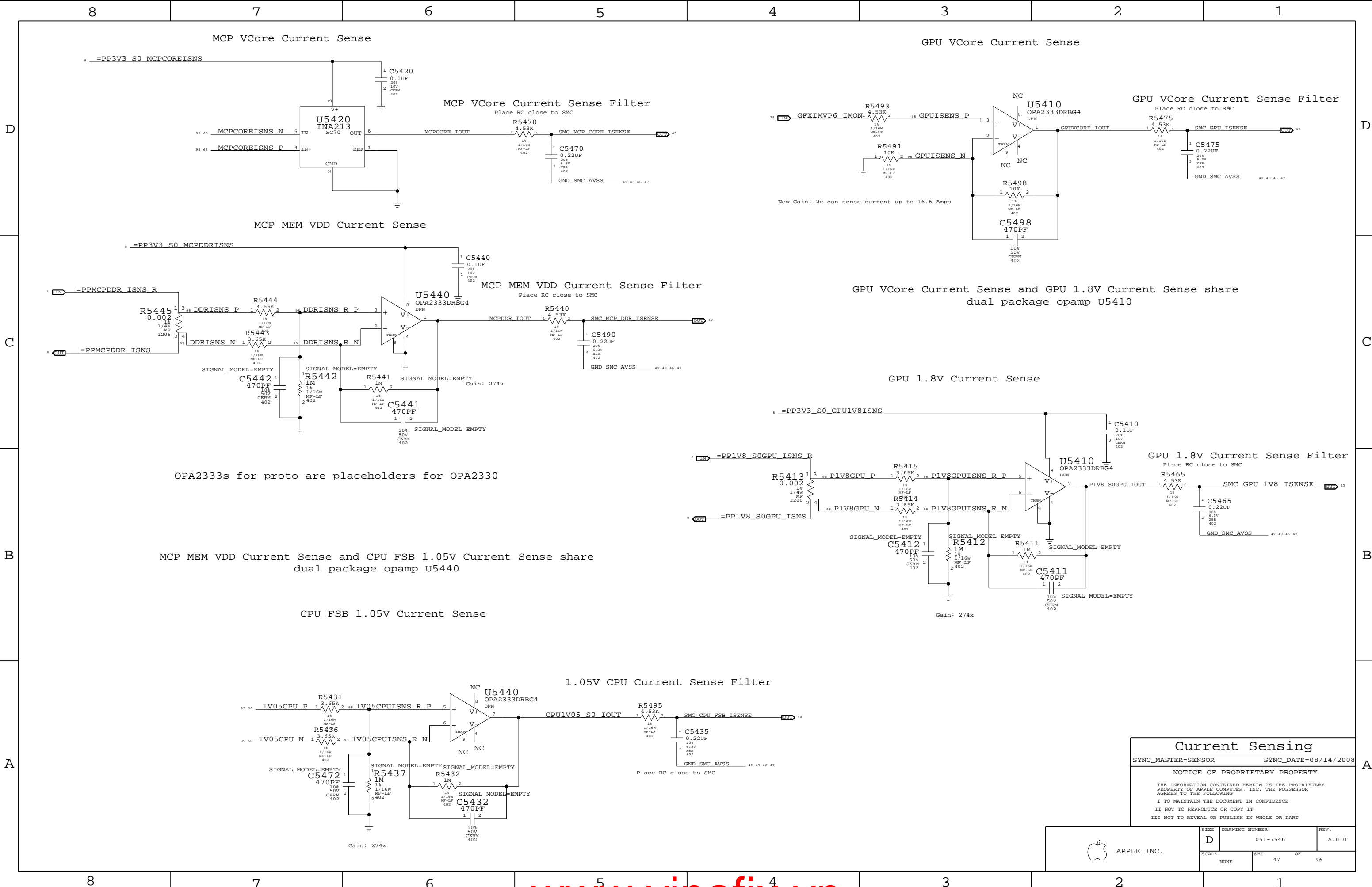
Consider INA211 (GAIN 500 version) since I=4.93 Amps across R5388

CPU VCore Load Side Current Sense / Filter



Current & Voltage Sensing
 SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008
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	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	46		



MCP VCore Current Sense

GPU VCore Current Sense

MCP MEM VDD Current Sense

GPU VCore Current Sense and GPU 1.8V Current Sense share dual package opamp U5410

MCP MEM VDD Current Sense and CPU FSB 1.05V Current Sense share dual package opamp U5440

OPA2333s for proto are placeholders for OPA2330

Current Sensing

SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

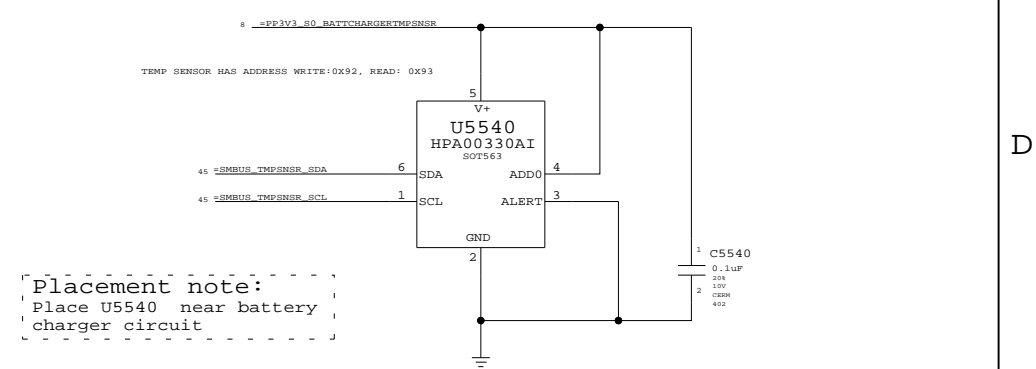
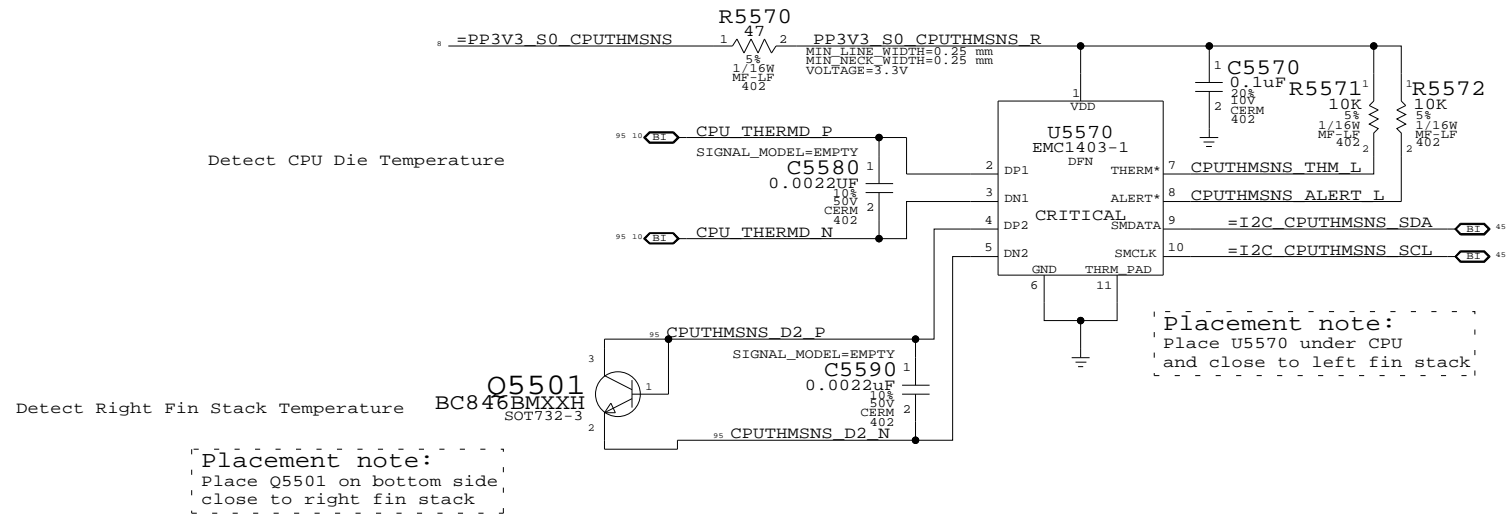
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	D	051-7546	A.0.0
SCALE	NONE	SHT	47 OF 96

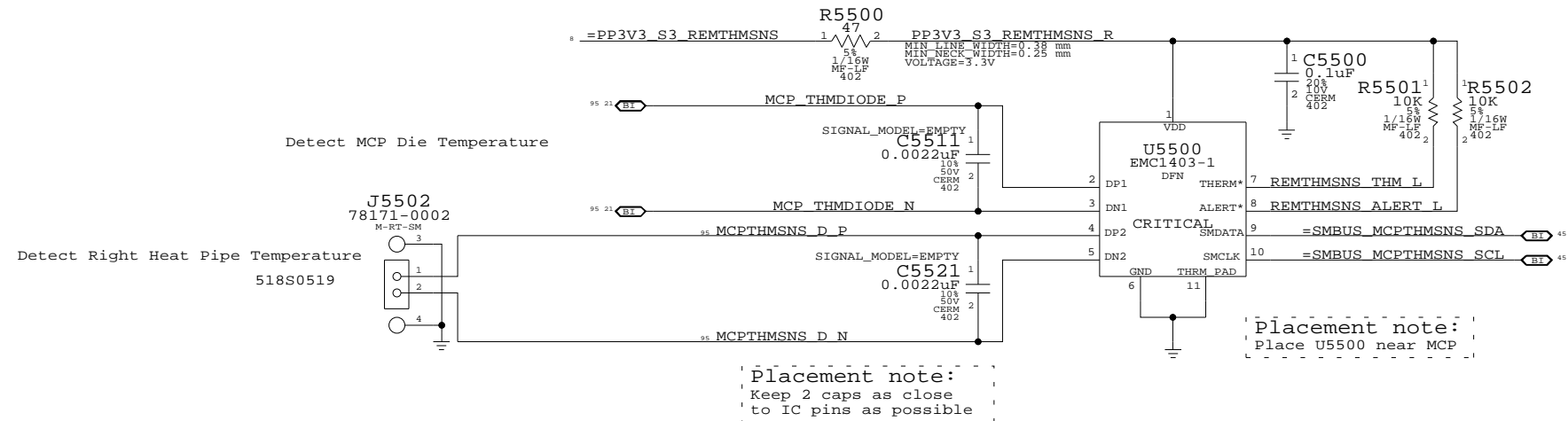
CPU Proximity/CPU Die/Right Fin Stack

Battery Charger Proximity

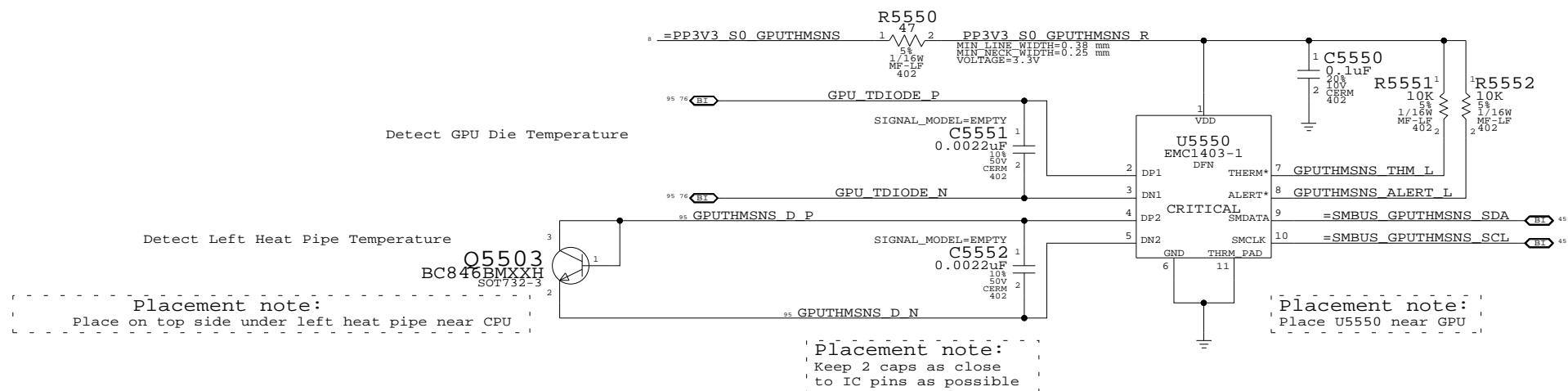


MCP Proximity/MCP Die/Right Heat Pipe

Note: EMC1403 can perform Beta Compensation for External Diode 1 only

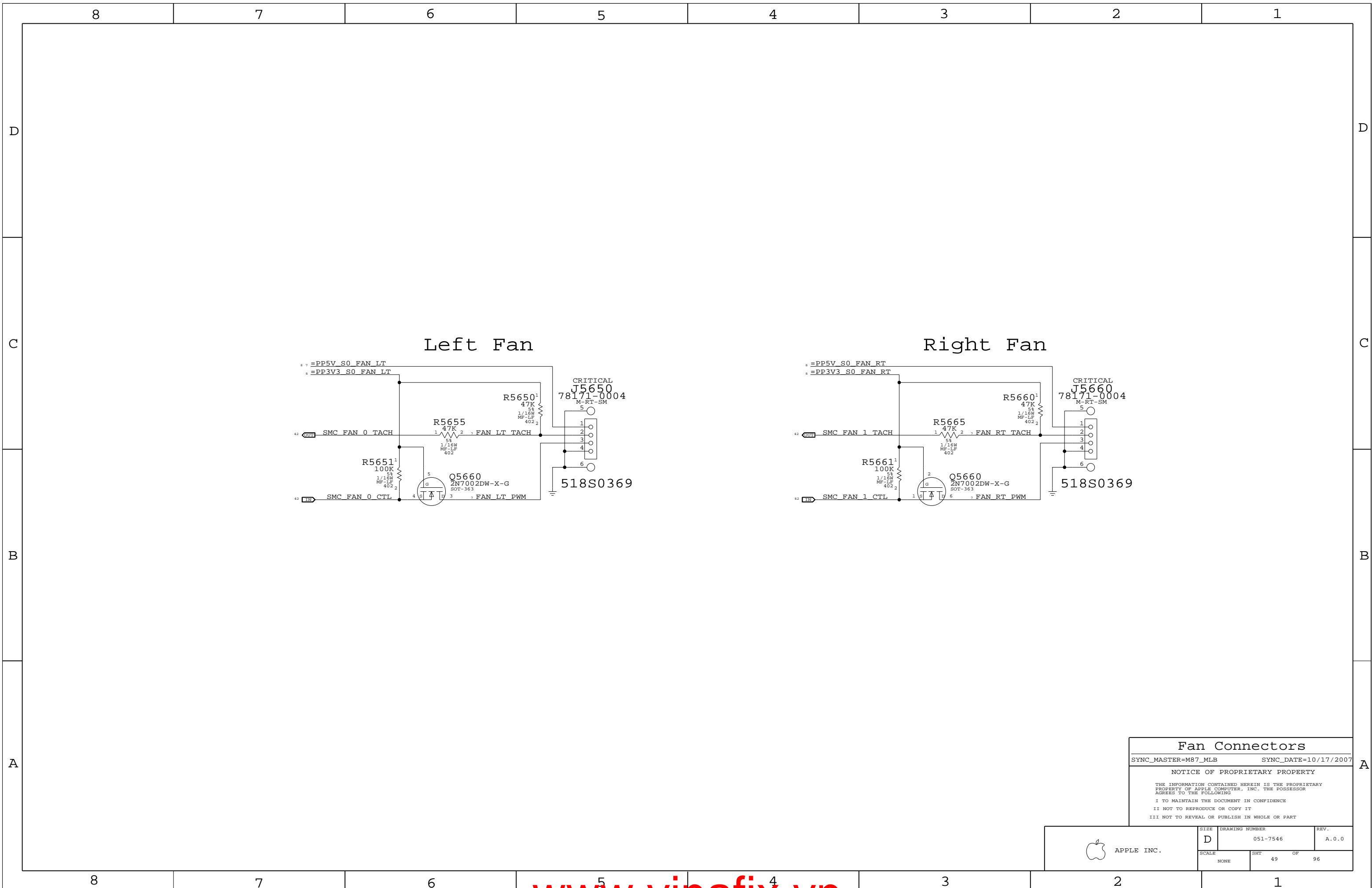


GPU Proximity/GPU Die/Left Heat Pipe



Thermal Sensors		
SYNC_MASTER=SENSOR	SYNC_DATE=08/14/2008	
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SCALE	SHT	OF	
NONE	48	96	



Fan Connectors

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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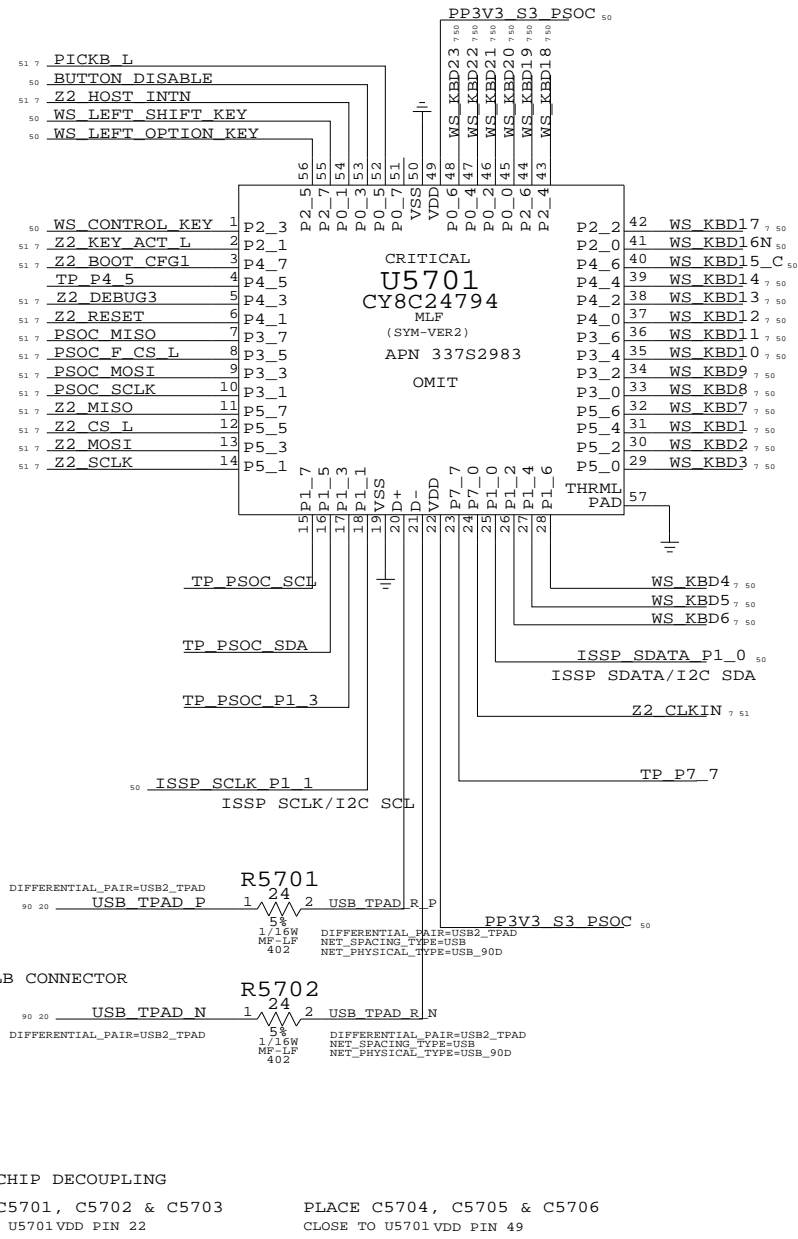
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

	SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
	SCALE NONE	SHT 49 OF 96	

PSOC USB CONTROLLER

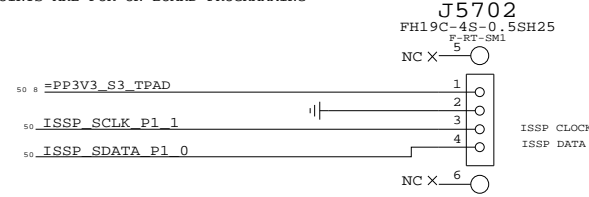
USB INTERFACES TO MLBACKPAD PICK BUTTONS
SPI HOST TO Z2
KEYBOARD SCANNER



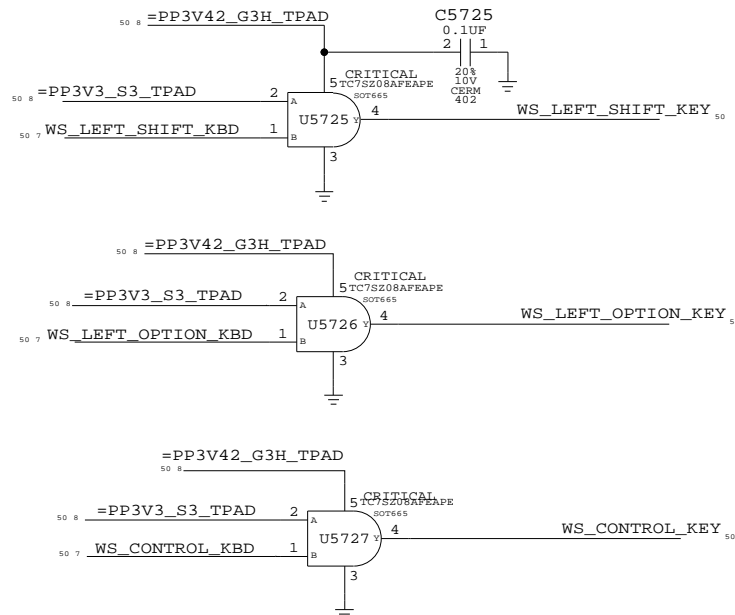
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.2555 V	0.255E-6 W
3V3 LDO	VDD	80UA	10 OHM	0.204 V	16.32E-6 W
PSOC	VOOUT	60MA MAX	0.2 OHM	0.012 V	0.72E-3 W
	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

PSOC PROGRAMMING CONNECTOR

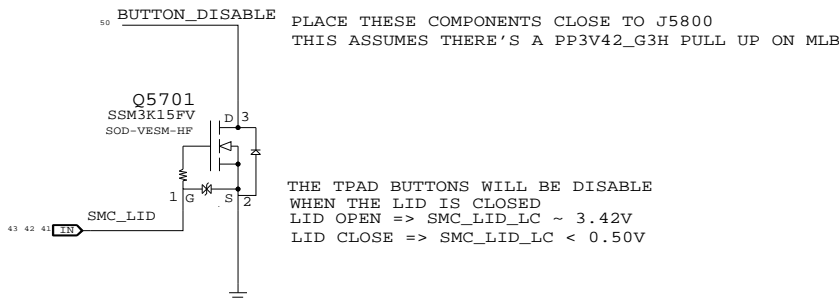
TEST POINTS ARE FOR ON BOARD PROGRAMMING



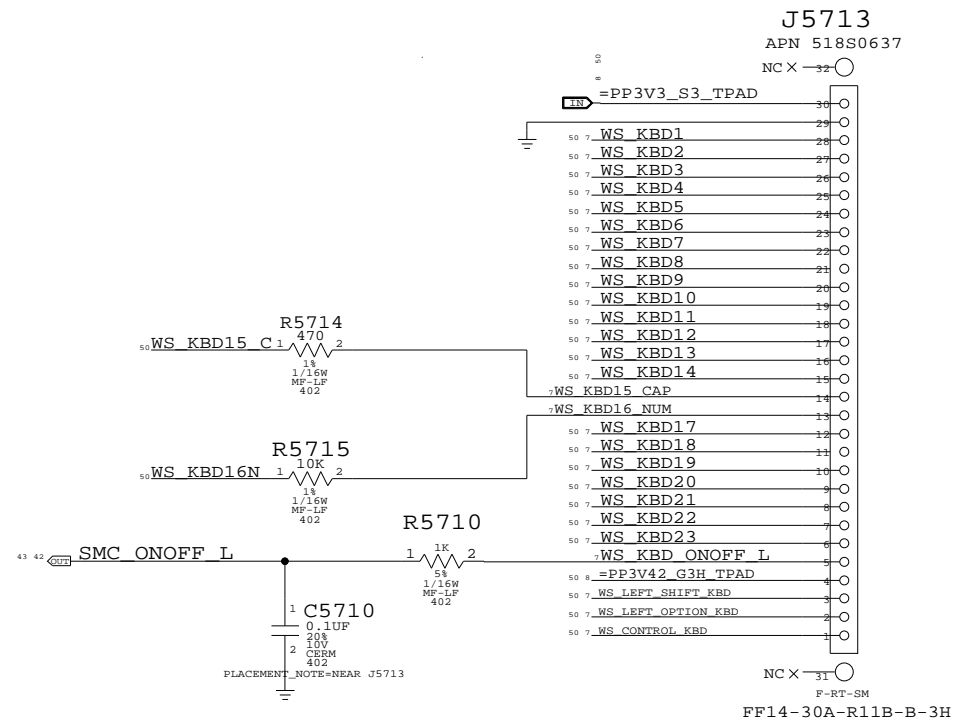
ISOLATION CIRCUIT



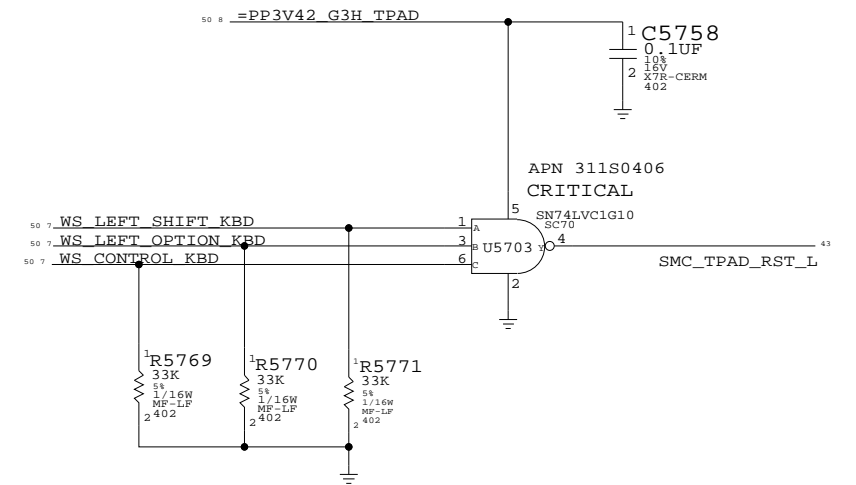
TPAD BUTTONS DISABLE



KEYBOARD CONNECTOR



SMC_MANUAL_RESET LOGIC



WELLSPRING 1

SYNC_MASTER=AMASON_M9SYNCDATE=06/18/2008

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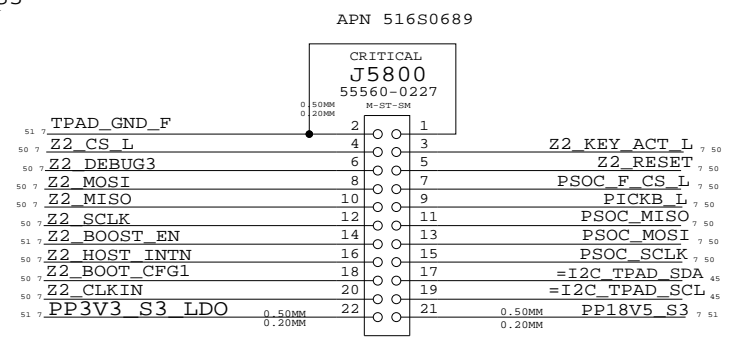
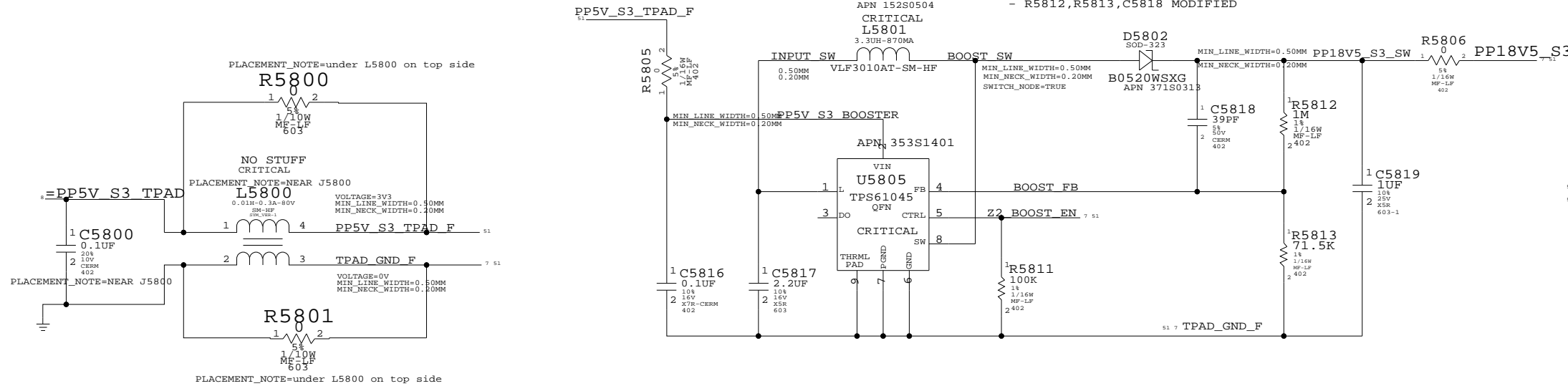


SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	50	96

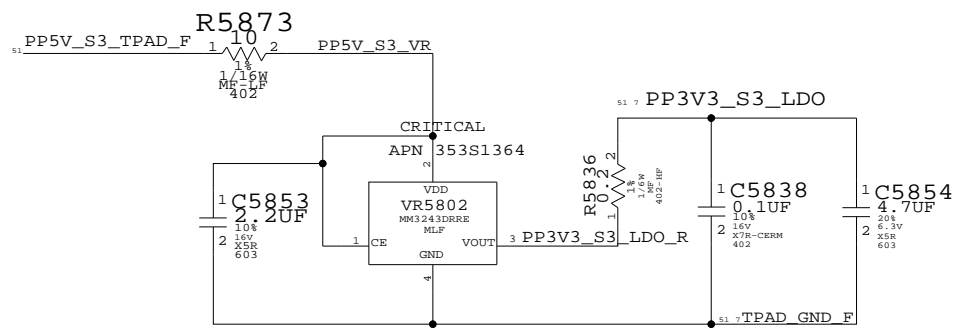
BOOSTER +18.5VDC FOR SENSORS

- BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
 - DROOP LINE REGULATION
 - RIPPLE TO MEET ERS
 - 100-300 KHZ CLEAN SPECTRUM
 - STARTUP TIME LESS THAN 2MS
 - R5812,R5813,C5818 MODIFIED

IPD FLEX CONNECTOR

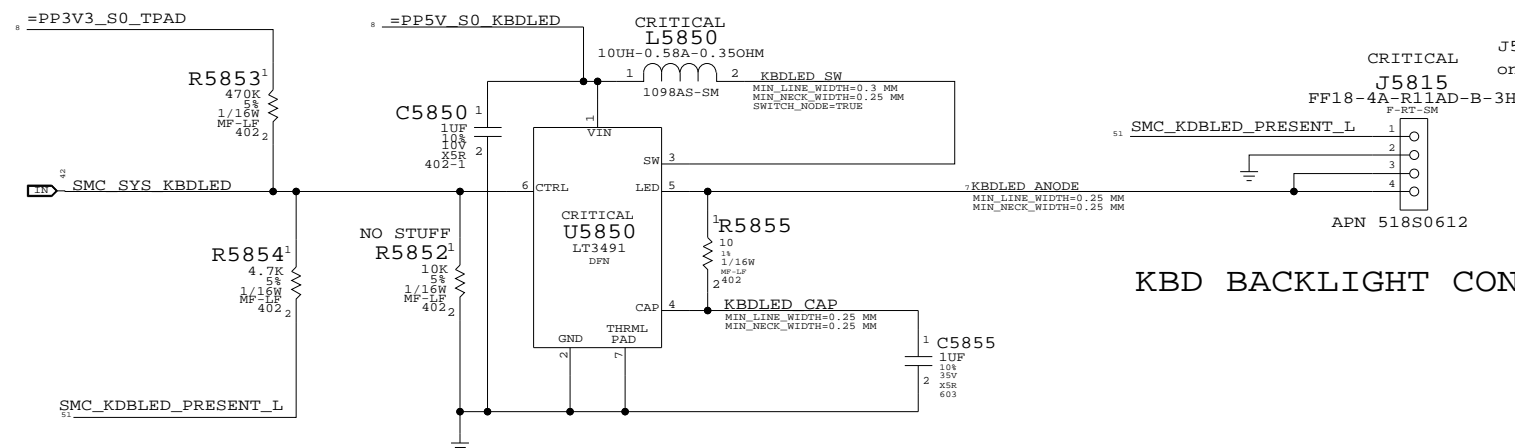


3V3 LDO FOR IPD



Keyboard LED Driver

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
 LOW = keyboard backlight present
 HIGH= keyboard backlight not present
 BOM OPTION: KBDLED_YES
 R5853 ALWAYS PRESENT

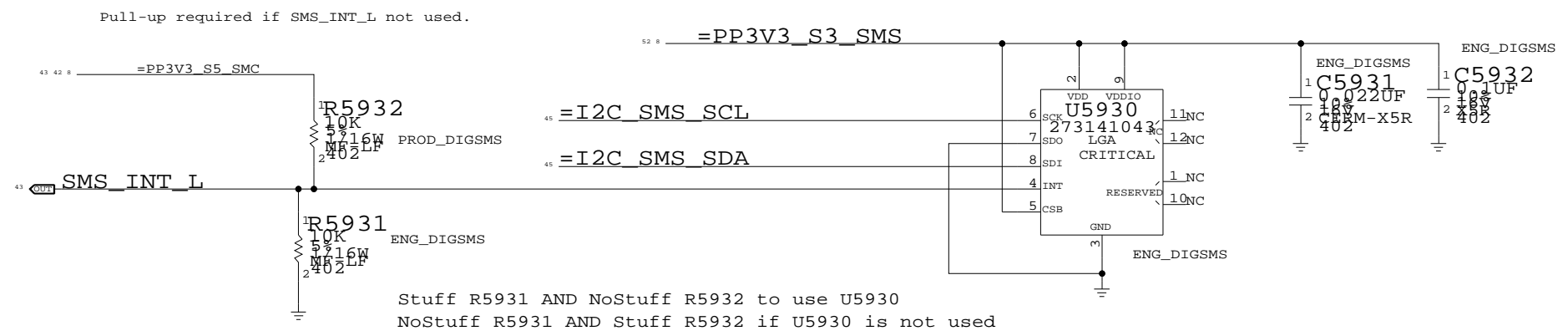


KBD BACKLIGHT CONNECTOR

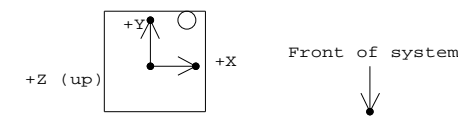
WELLSPRING 2
 SYNC_MASTER=PWRSONC SYNC_DATE=05/12/2008
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APPLE INC.	SIZE	D	DRAWING NUMBER	051-7546	REV.	A.0.0
	SCALE	NONE	SHT	51	OF	96

Digital SMS



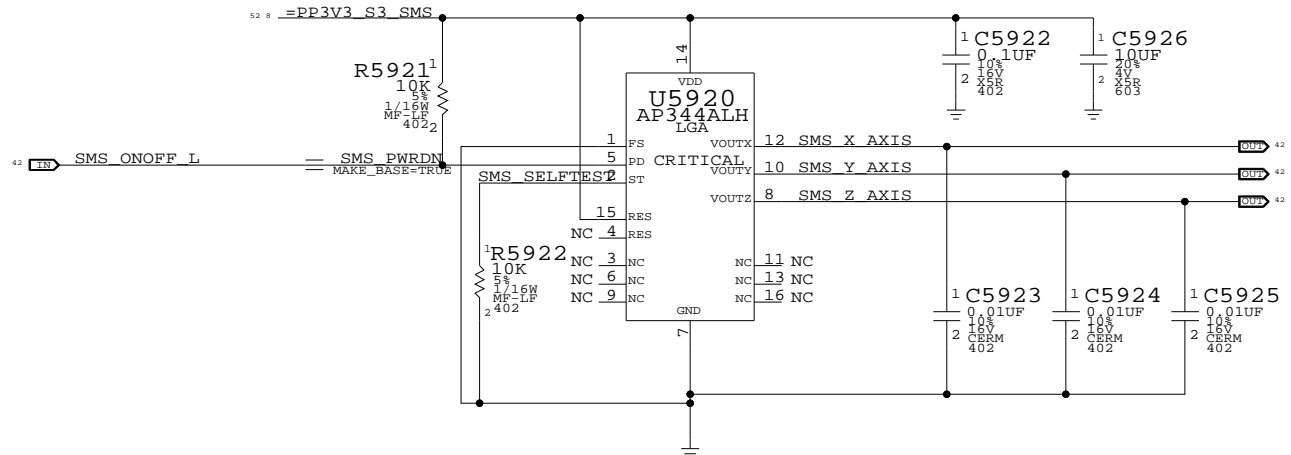
Desired orientation when placed on board top-side:



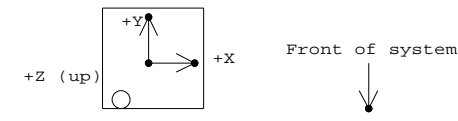
Circle indicates pin 1 location when placed in correct orientation

Analog SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC



Desired orientation when placed on board top-side:

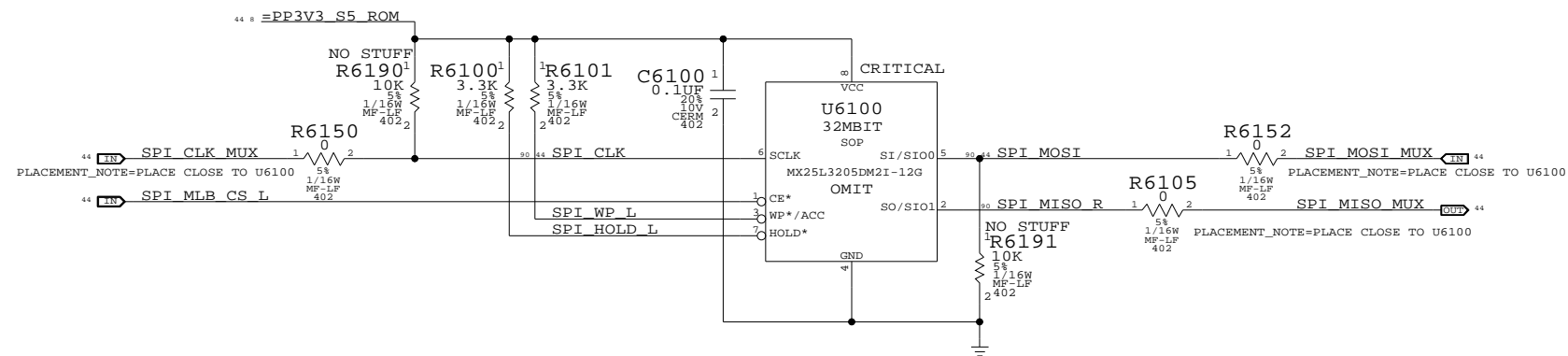


Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)
SYNC_MASTER=SENSOR SYNC_DATE=08/14/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	
NONE	52	96	



MCP79 SPI Frequency Select		
Frequency	SPI_MOSI	SPI_CLK
31 MHz	0	0
42 MHz	0	1
25 MHz	1	0
1 MHz	1	1

25MHz is selected with R5190 and R5191
 Any of the 4 frequencies can be selected
 with R6190, R6191, R5190 and R5191

SPI ROM

SYNC_MASTER=CHANG_M98_MLB SYNC_DATE=07/01/2008

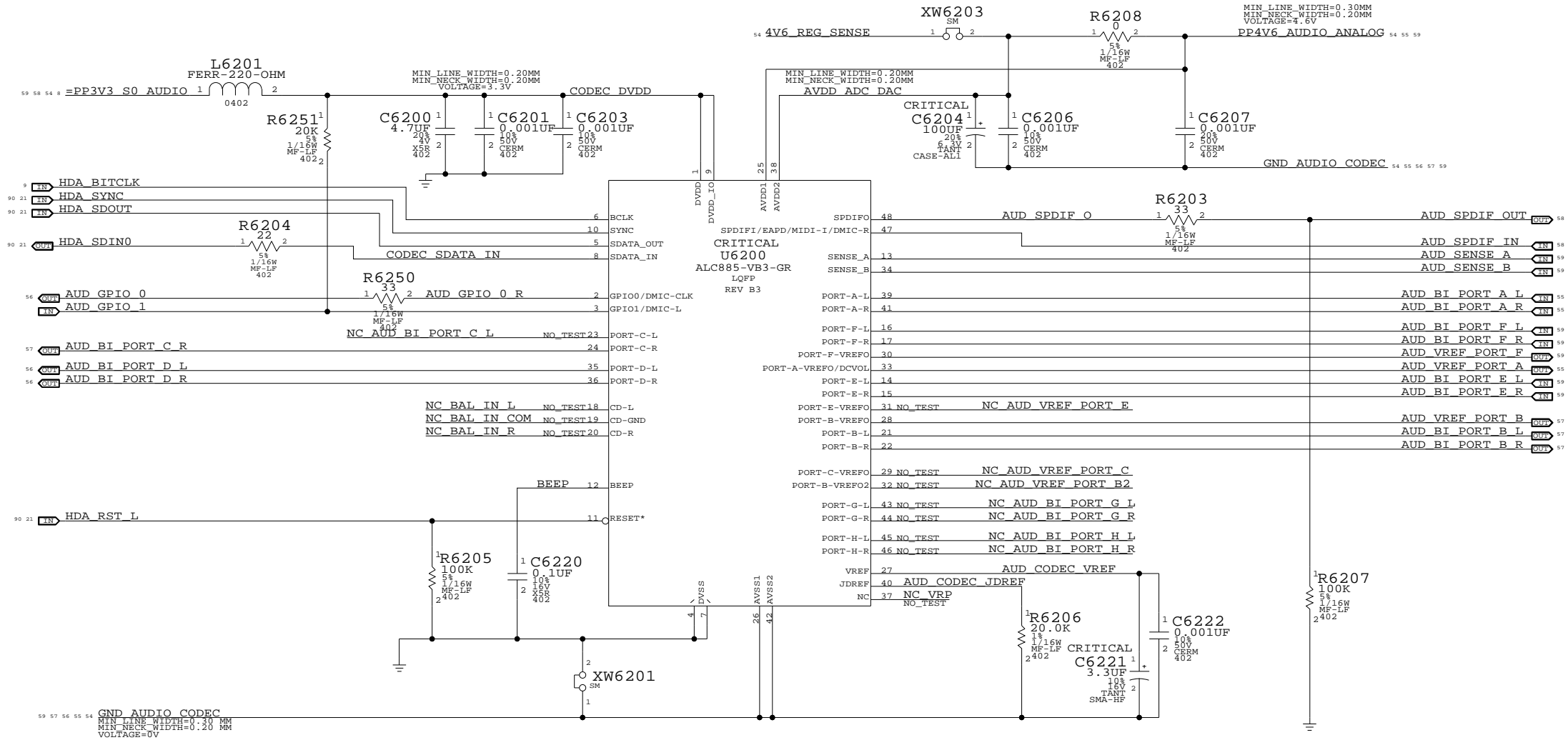
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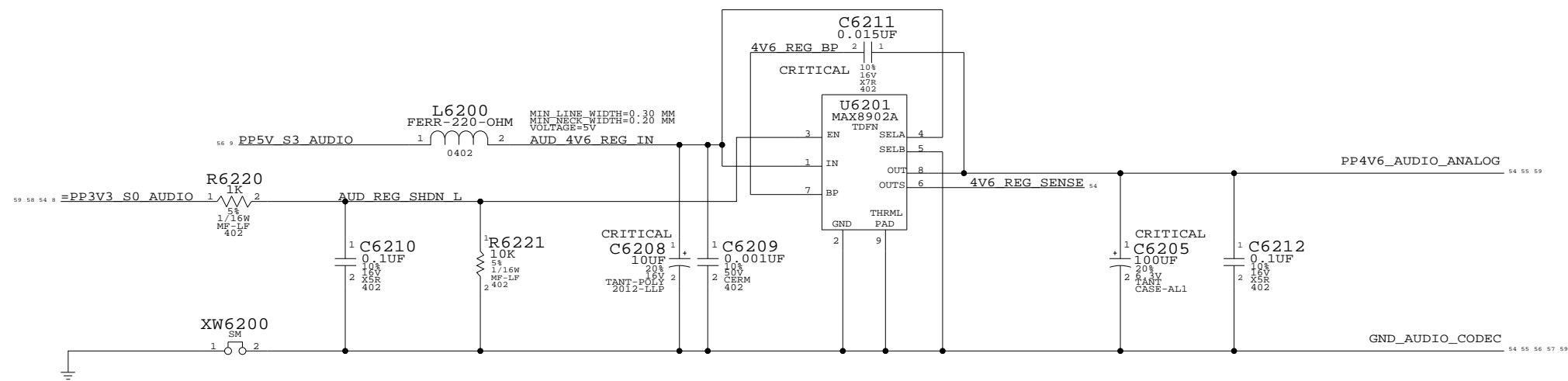
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	53	96	

AUDIO CODEC
APPLE P/N 353S1527



AUDIO 4.6V REGULATOR
APPLE P/N 353S1897



AUDIO:CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	54	96	

8

7

6

5

4

3

2

1

D

D

C

C

B

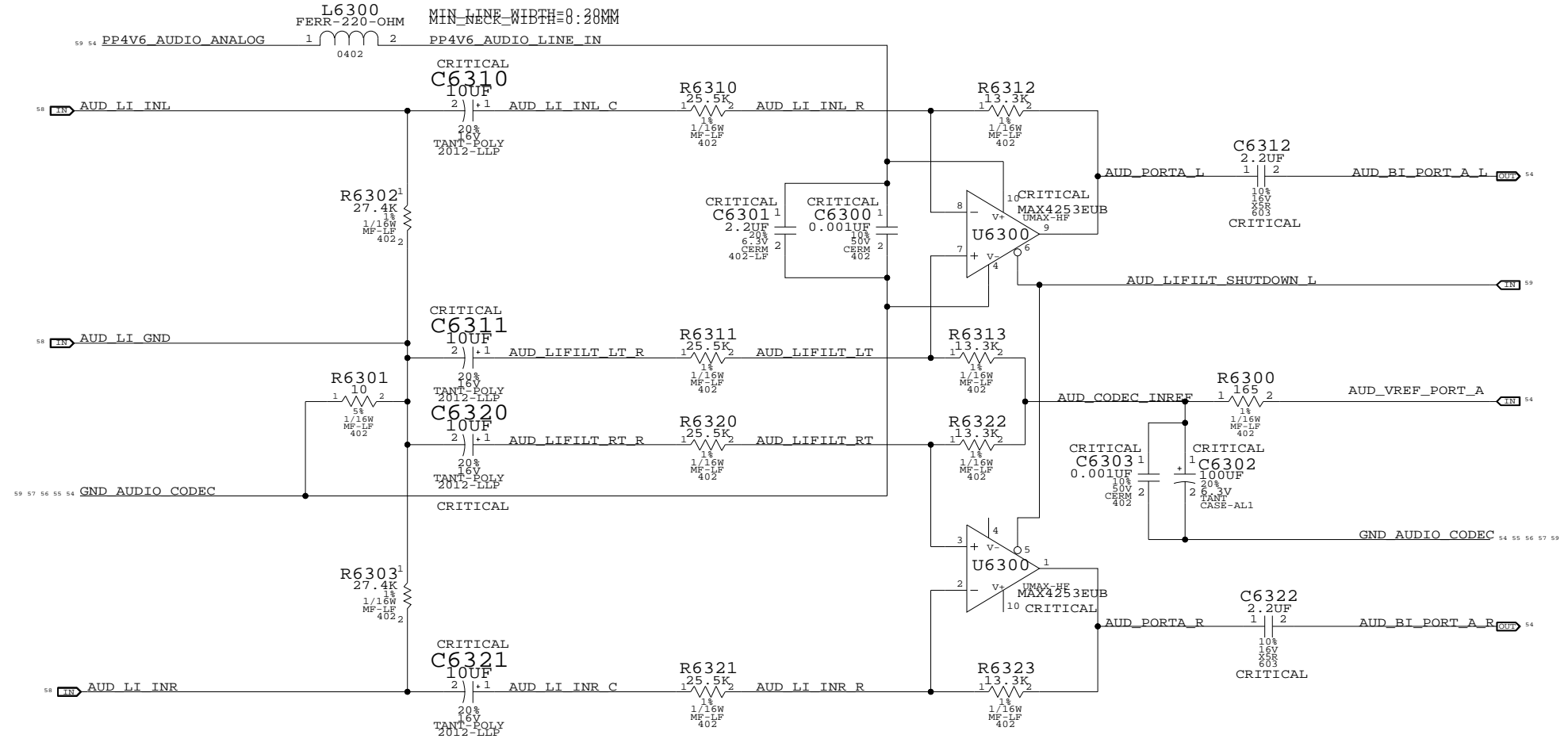
B

A

A

Pseudo-Diff Line-In Filter

GAIN = -5.4DB AV = 0.52
 FC = 1.8 HZ



AUDIO: LINE IN
 SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT		OF
NONE	55		96

8

7

6

5

4

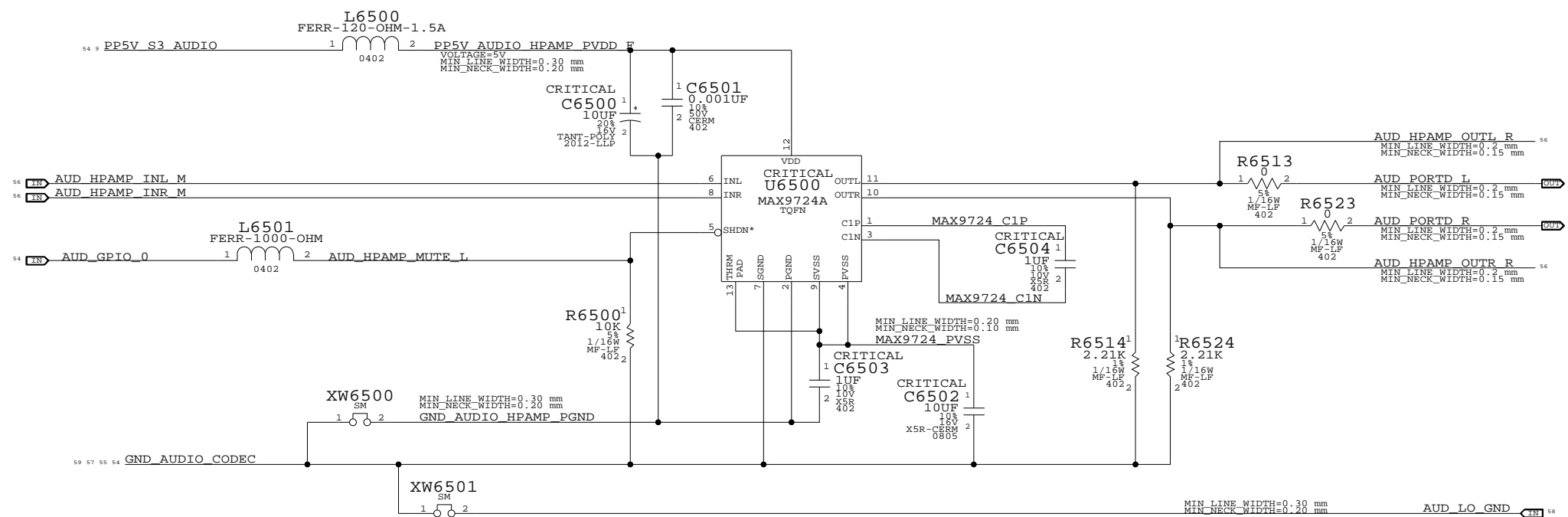
3

2

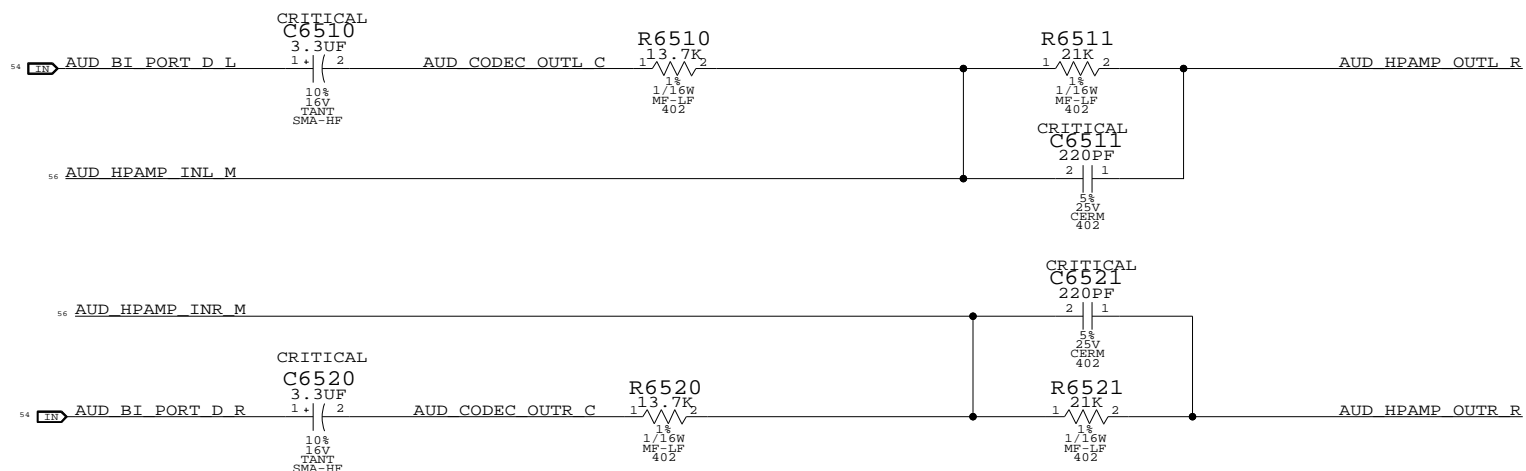
1

Headphone Amplifier (MAX9724A)

APN: 353S1637



1st Order DAC Filter
 HP:3.52 HZ LP:34 KHZ
 VOLTAGE GAIN:1.53



AUDIO: HEADPHONE AMP
 SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
	SCALE NONE	SHEET 56	OF 96

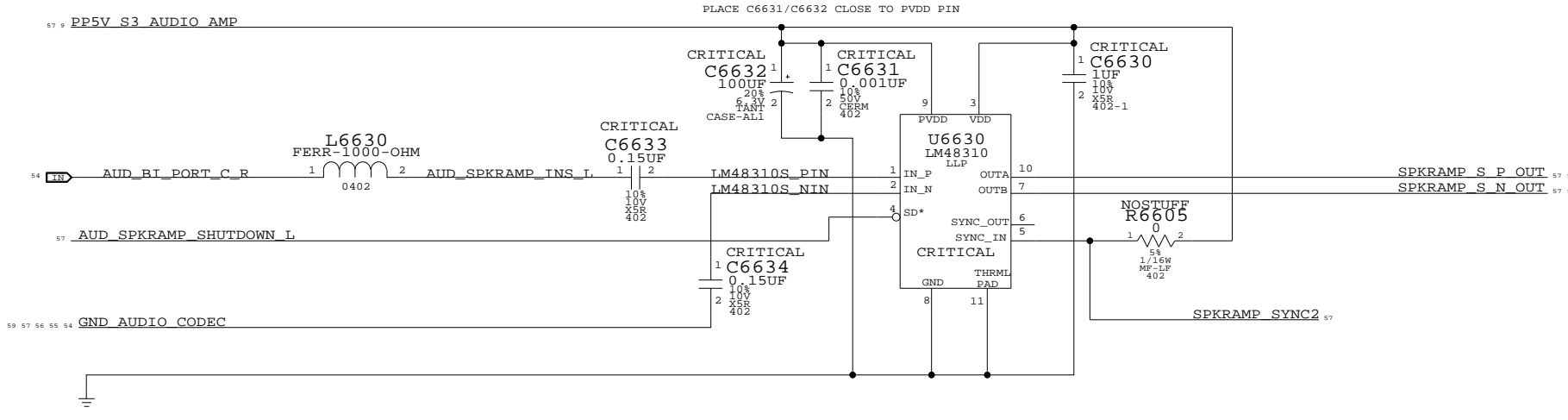
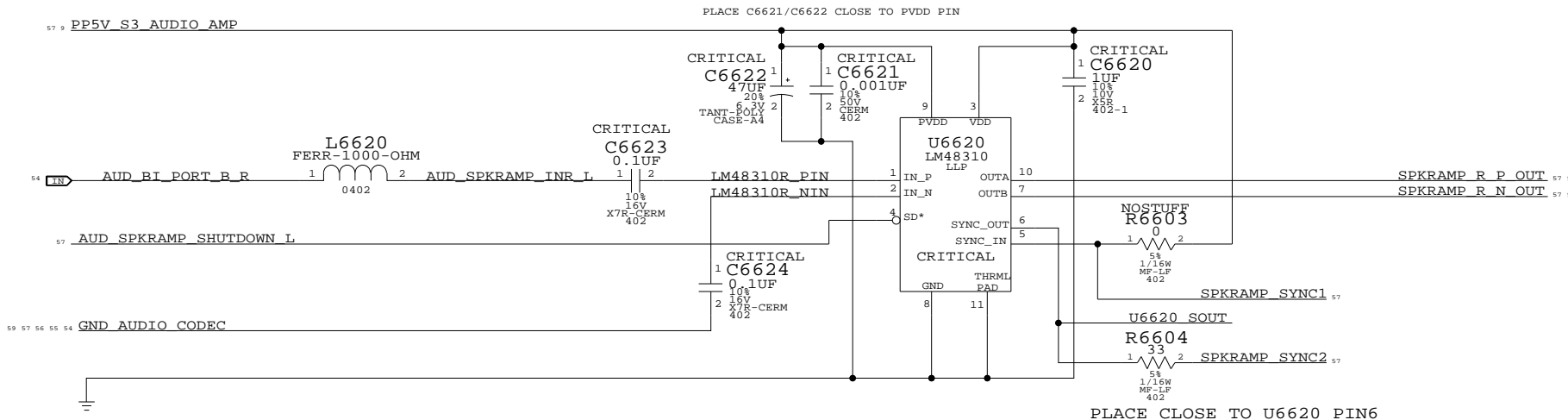
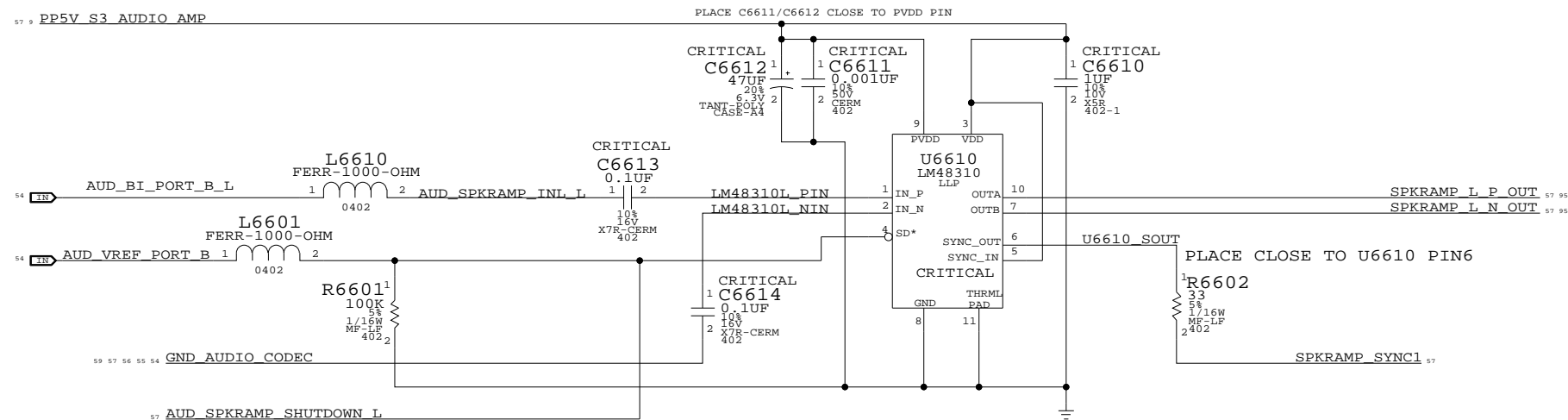
2X MONO SPEAKER AMPLIFIERS (LM48310)

APN: 353S1901

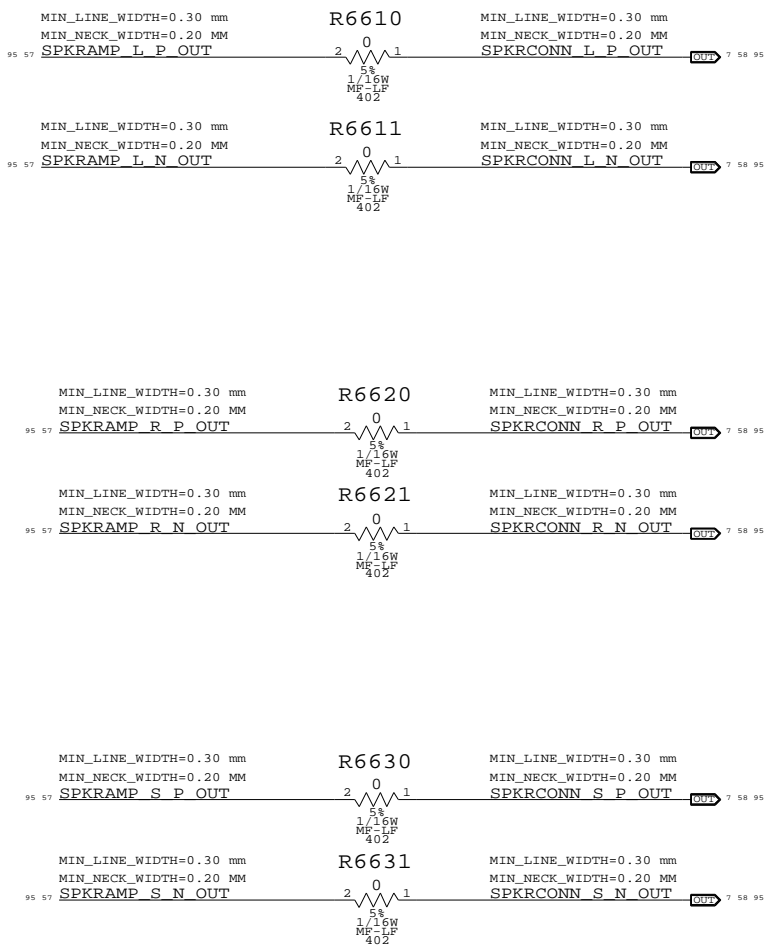
GAIN = 12DB

79Hz < FC (L&R) < 93Hz

53Hz < FC (SUB) < 62Hz



SPEAKER CHECKPOINTS



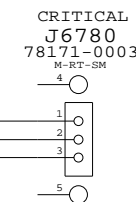
AUDIO: SPEAKER AMP
 SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	
NONE	57	96	

AUDIO JACK 1 LO/HP JACK, SPDIF TX

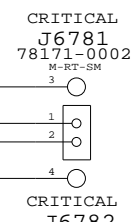
MIC CONNECTOR

APN: 518S0520

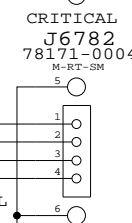


SPEAKER CONNECTOR

APN: 518S0519



APN: 518S0521



RETURN FOR HF NOISE

AUDIO JACK 2 LINE IN JACK, SPDIF RX

AUDIO: JACKS
 SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	58	96	

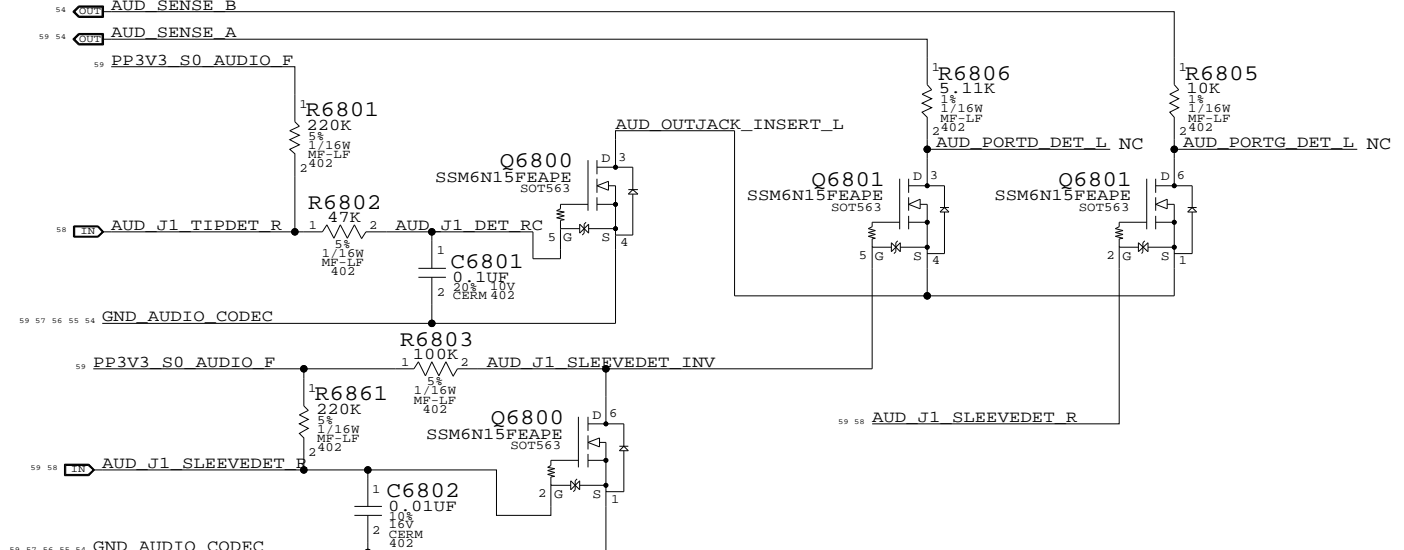
CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	MIXER(OUTPUT)	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X0C (12)	0X02 (2)	0X0C (12)	0X14 (20,D)	GPIO_0	0X14 (20,D)
SATELLITES	0X0D (13)	0X03 (3)	0X0D (13)	0X18 (24,B)	VREF_B (100%)	N/A
SUB	0X0F (15)	0X05 (05)	0X0F (15)	0X1A (26,C)	VREF_B (100%)	N/A
SPDIF OUT	N/A	0X06 (6)		0x1E (SPDIF OUT)	N/A	0X16 (22,G)

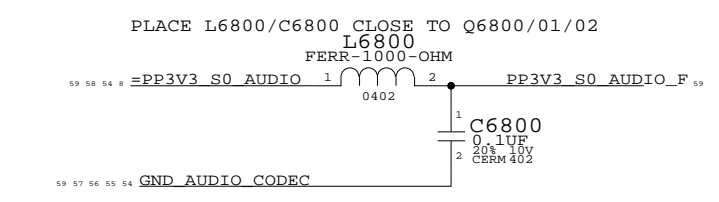
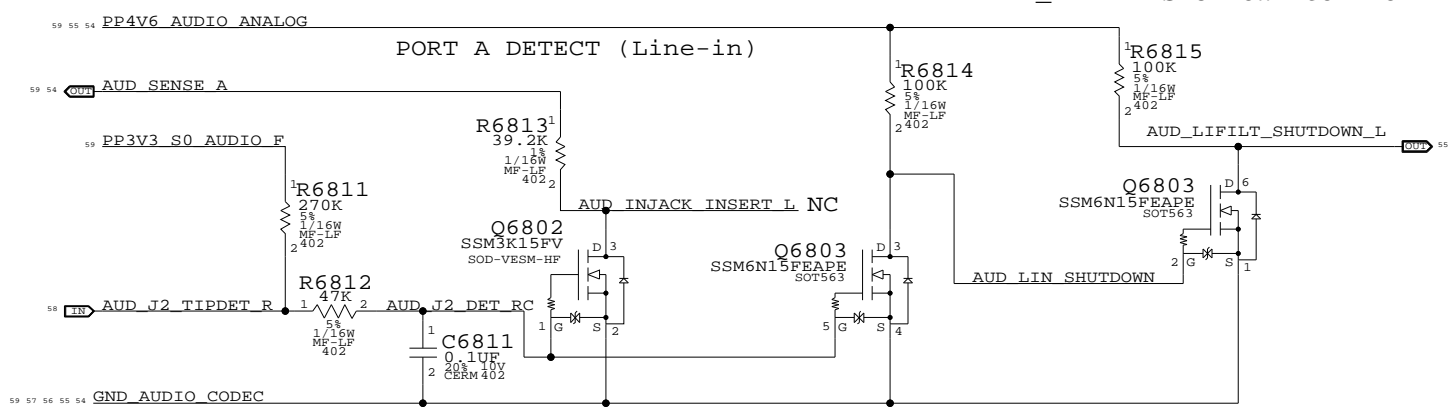
CODEC INPUT SIGNAL PATHS

FUNCTION	MIXER(INPUT)	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
LINE IN	0X23 (35)	0X08 (8)	0X15 (21,A)	VREF_A (50%)	0X15 (21,A)
SPDIF IN	N/A	0X0A (10)	0x1F (SPDIF IN)	N/A	N/A
BUILT-IN MIC	0X24 (36)	0X07 (7)	0X19 (25,F)	VREF_F (100%)	N/A
HEADSET MIC	0X24 (36)	0X07 (7)	0X1B (27,E)	MIKEY	MIKEY

PORT D DETECT (Line-out) PORT G DETECT (SPDIF DELEGATE)

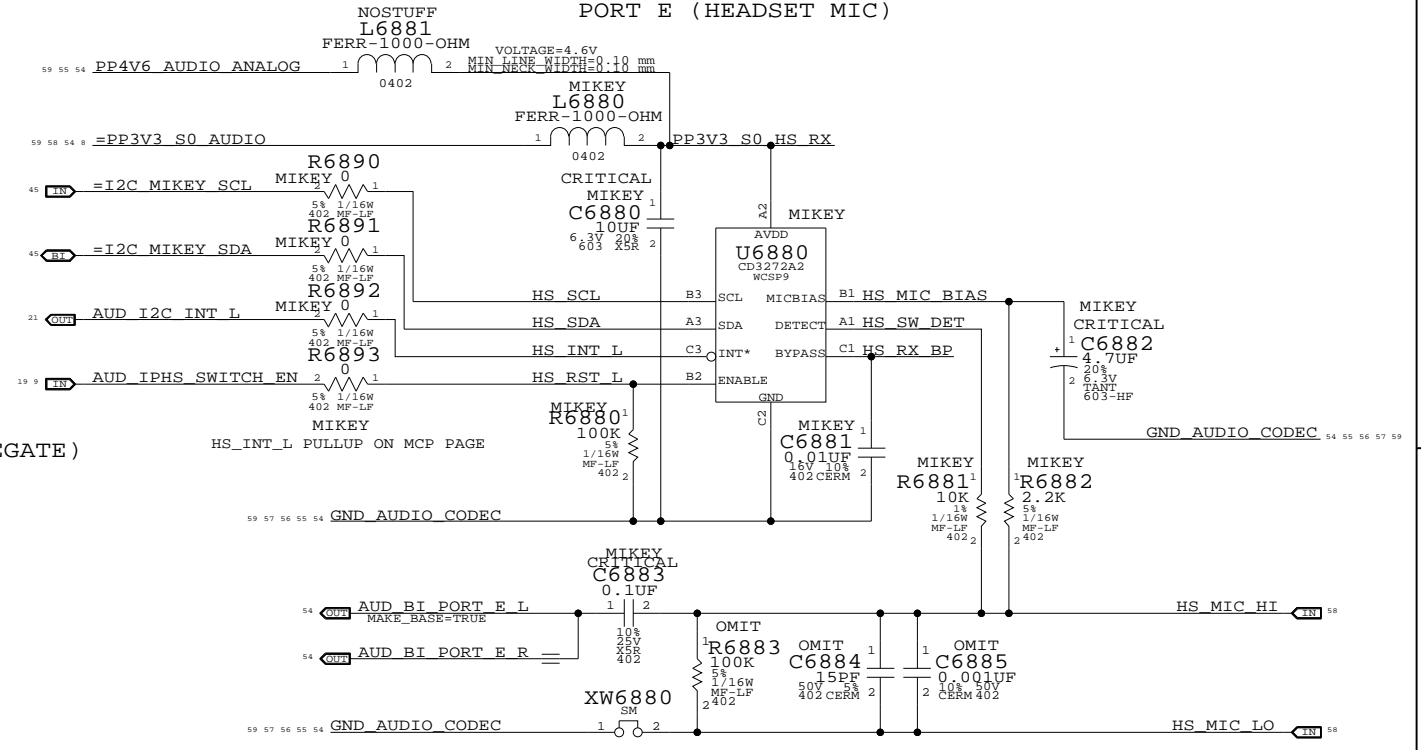


LINE_IN AMP SHUTDOWN CONTROL



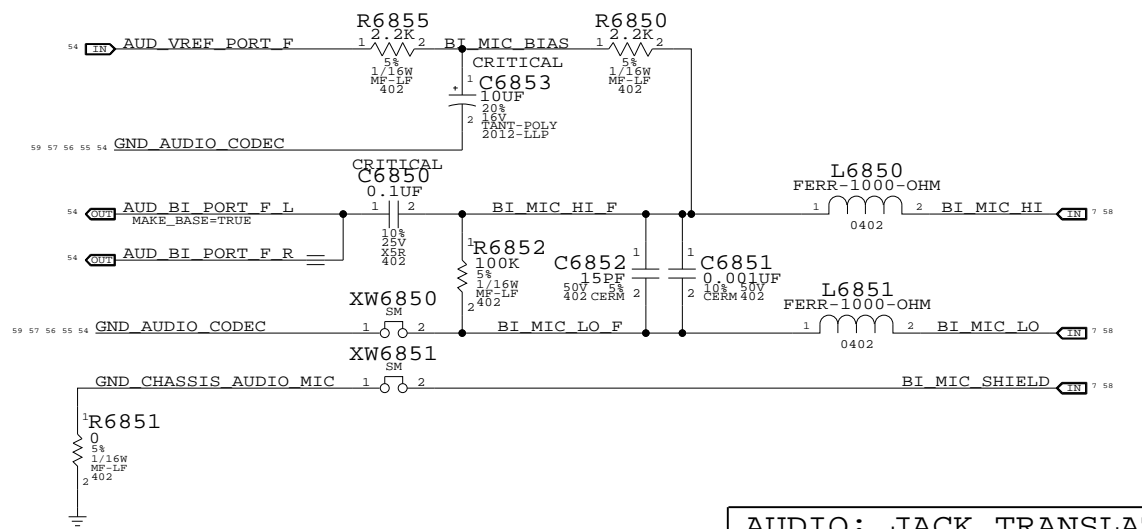
PLACE L6800/C6800 CLOSE TO Q6800/01/02

PORT E (HEADSET MIC)



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0114	1	100K 5% 0402 RESISTOR	R6883	MIKEY
131S1513	1	15PF 5% 0402 CAPACITOR	C6884	MIKEY
132S0045	1	100PF 10% 0402 CAPACITOR	C6885	MIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	R6883	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6884	NOMIKEY
116S0004	1	0 OHMS 5% 0402 RESISTOR	C6885	NOMIKEY

PORT F (BUILT-IN MIC)



AUDIO: JACK TRANSLATORS

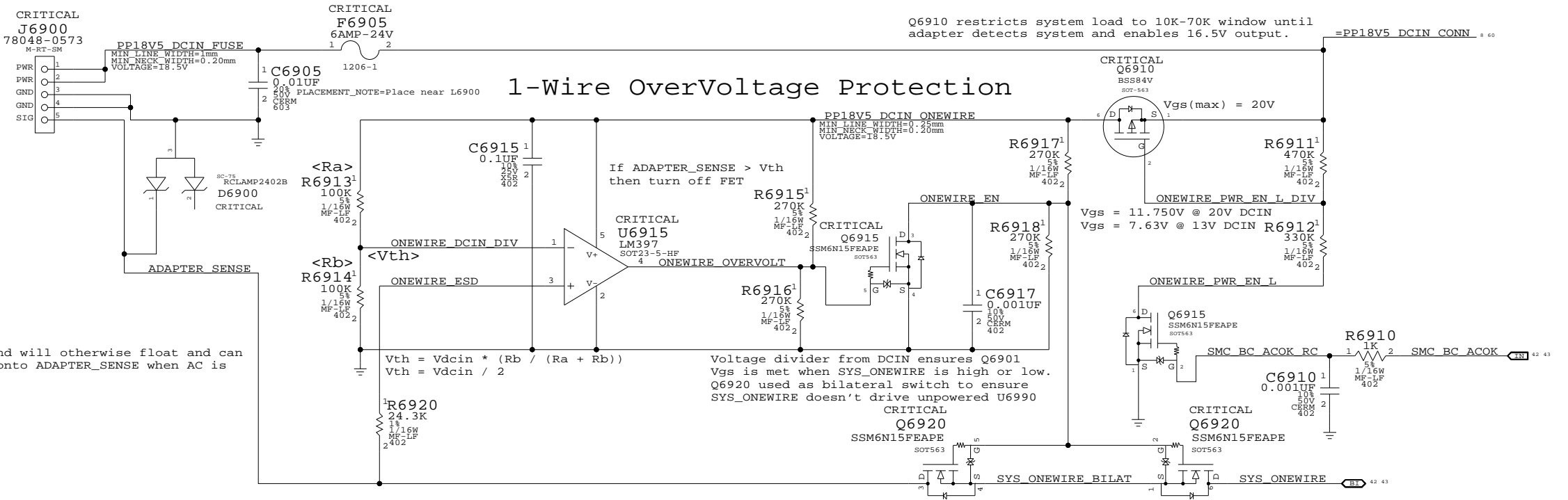
SYNC_MASTER=AUDIO SYNC_DATE=07/09/2008

NOTICE OF PROPRIETARY PROPERTY

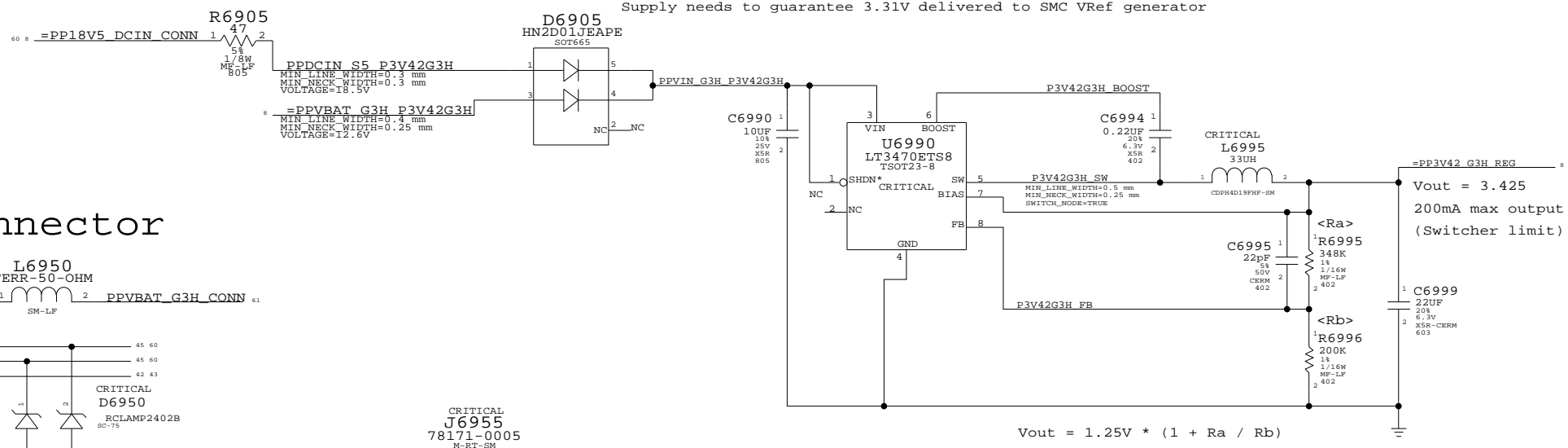
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	59		

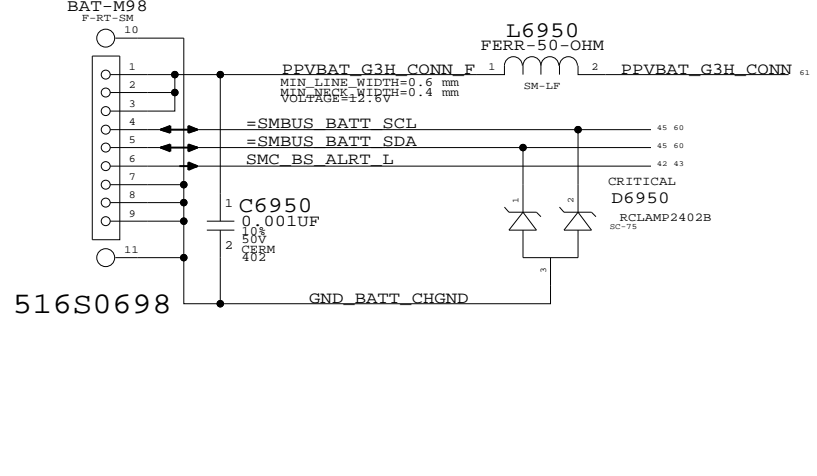
MagSafe DC Power Jack



3.425V "G3Hot" Supply



Battery Connector



DC-In & Battery Connectors

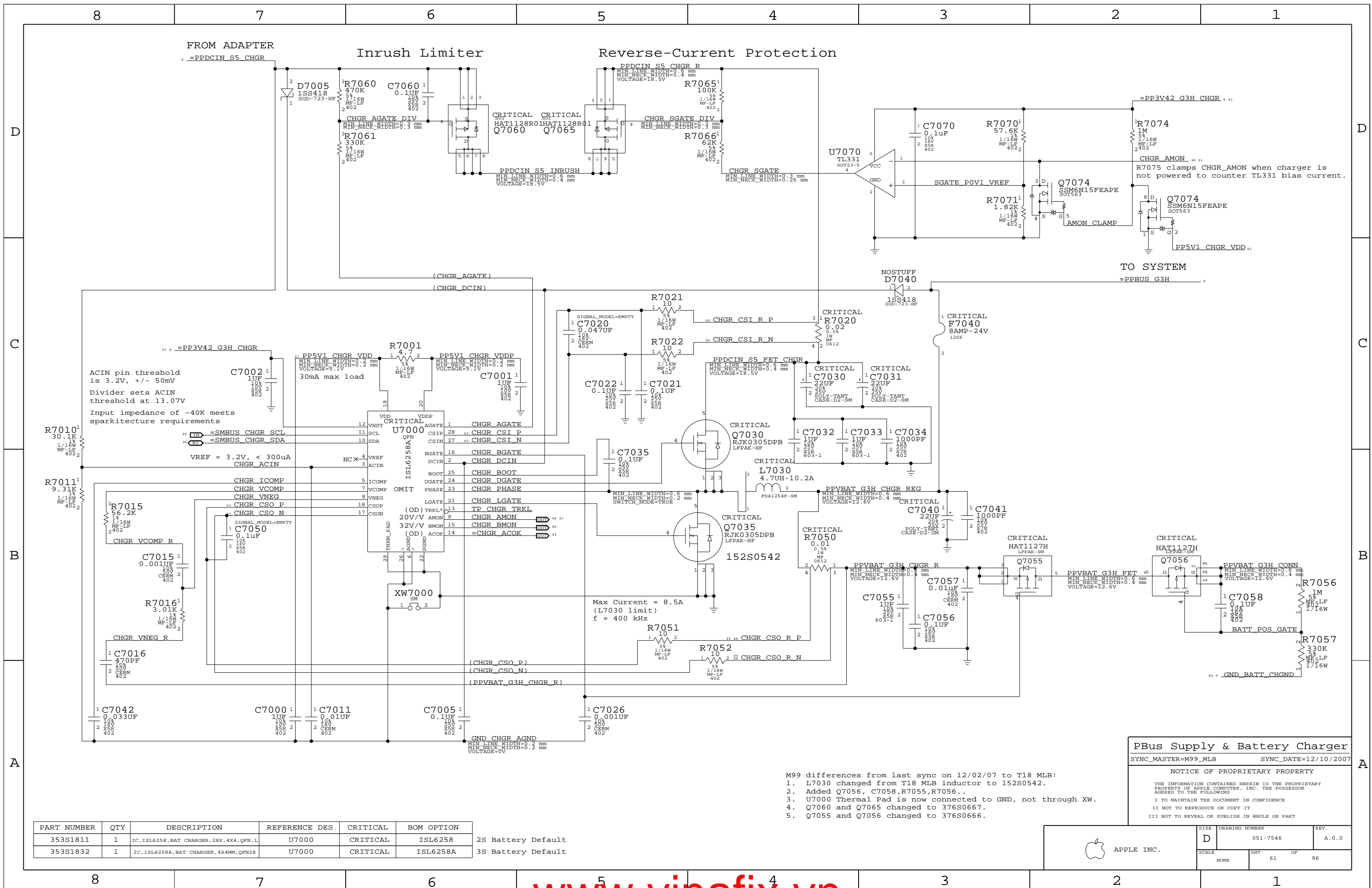
SYNC_MASTER=T18_MLB SYNC_DATE=12/06/2007

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	60 OF 96



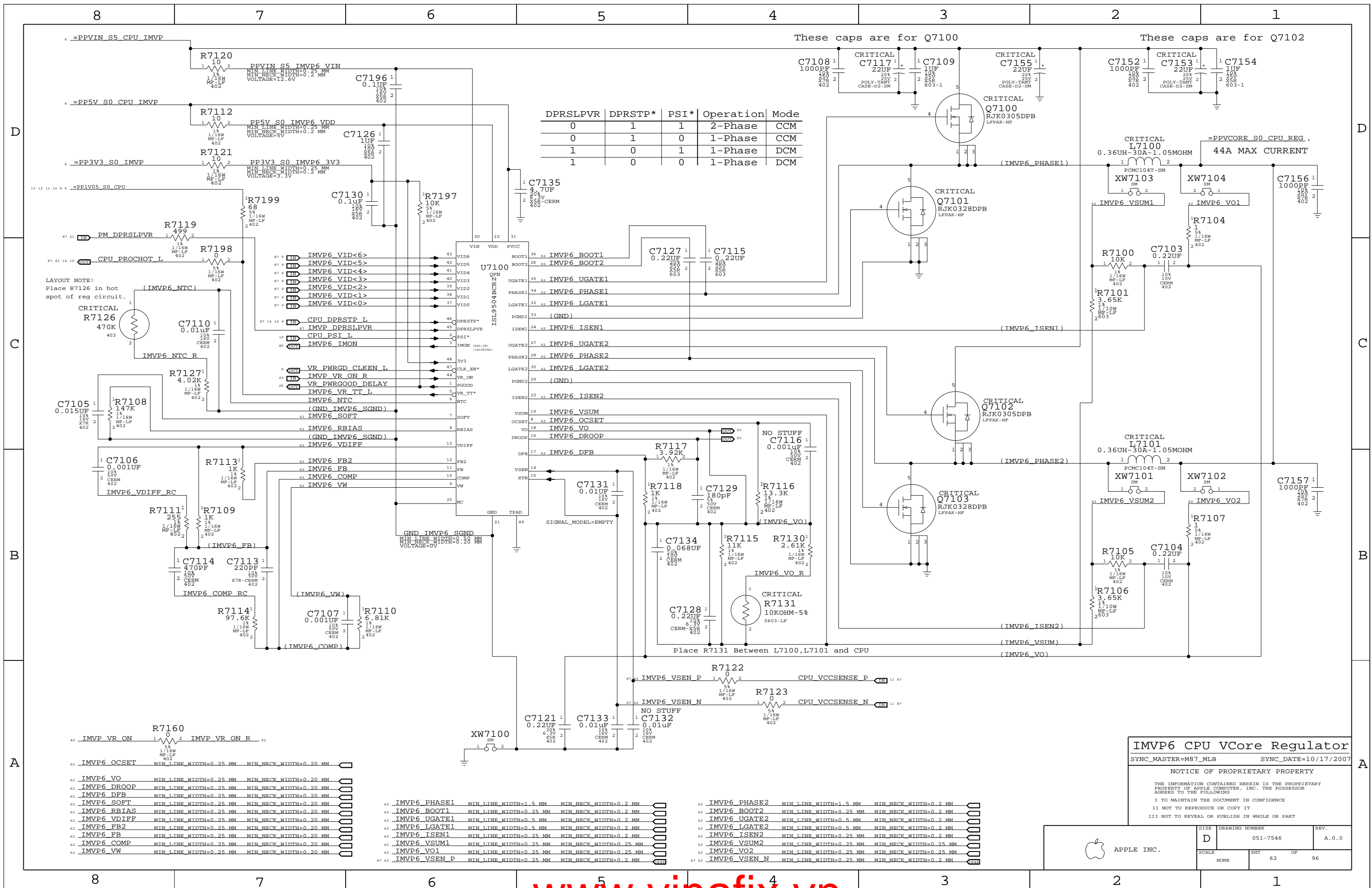
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S1811	1	IC, ISL6258, BAT CHARGER, 28P, 4X4, QFN, L	U7000	CRITICAL	2S Battery Default
353S1832	1	IC, ISL6258A, BAT CHARGER, 4X4MM, QFN28	U7000	CRITICAL	3S Battery Default

- M99 differences from last sync on 12/02/07 to T18 MLB:
- L7030 changed from T18 MLB inductor to 152S0542.
 - Added Q7056, C7058, R7055, R7056.
 - U7000 Thermal Pad is now connected to GND, not through XW.
 - Q7060 and Q7065 changed to 376S0667.
 - Q7055 and Q7056 changed to 376S0666.

PBus Supply & Battery Charger
 SYNC_MASTER=M99_MLB SYNC_DATE=12/10/2007

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APPLE INC.	SIZE: D	DRAWING NUMBER: 051-7546	REV.: A.0.0
	SCALE: NONE	SHEET: 61	OF: 96



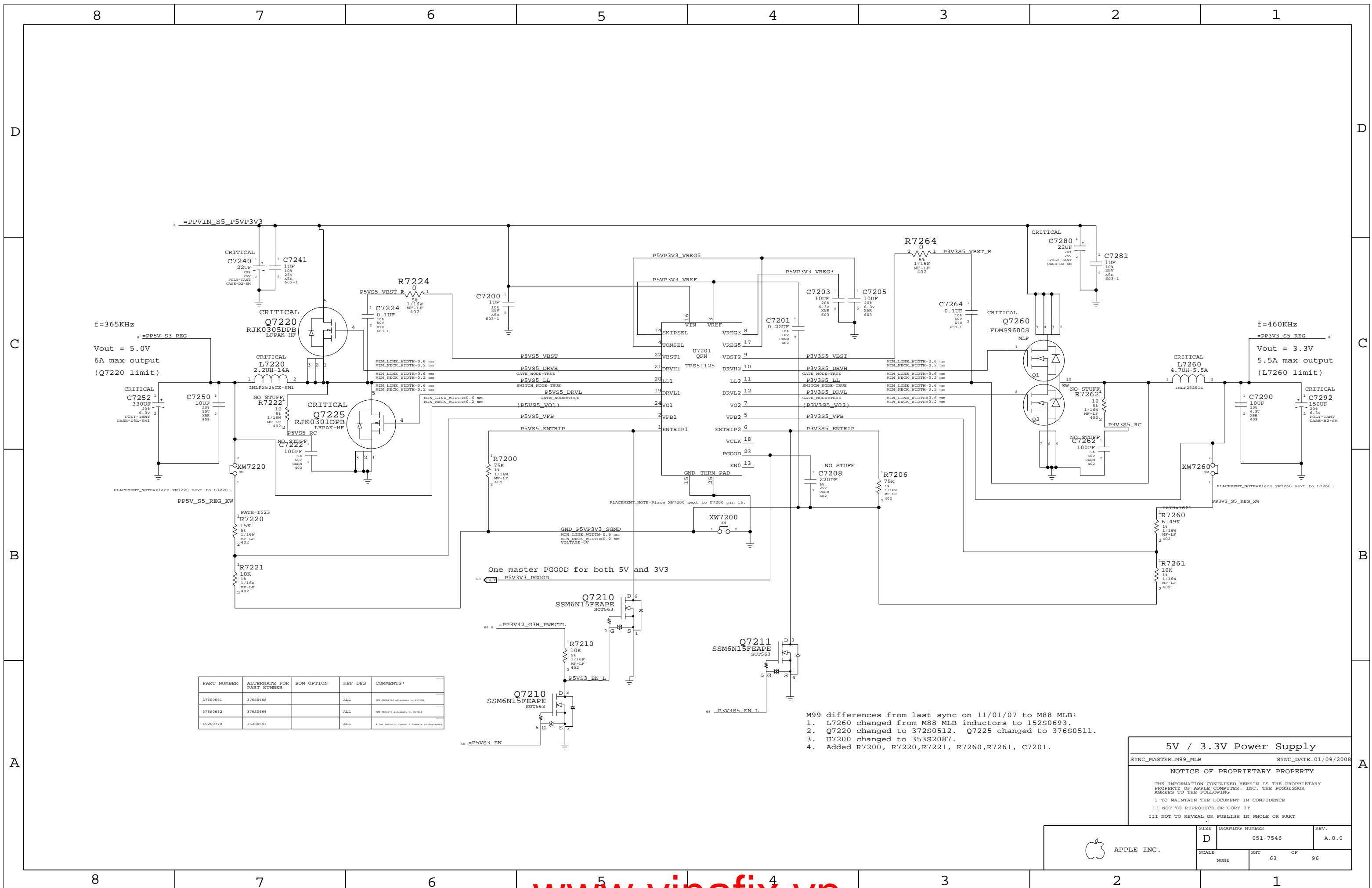
DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	0	0	1-Phase	DCM

87 62	IMVP6 VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	87 62	IMVP6 VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
87 62	IMVP6 VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM	87 62	IMVP6 VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.20 MM
87 62	IMVP6 PHASE1	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM	87 62	IMVP6 PHASE2	MIN_LINE_WIDTH=1.5 MM	MIN_NECK_WIDTH=0.2 MM
87 62	IMVP6 BOOT1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	87 62	IMVP6 BOOT2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
87 62	IMVP6 UGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	87 62	IMVP6 UGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
87 62	IMVP6 LGATE1	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM	87 62	IMVP6 LGATE2	MIN_LINE_WIDTH=0.5 MM	MIN_NECK_WIDTH=0.2 MM
87 62	IMVP6 ISEN1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	87 62	IMVP6 ISEN2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM
87 62	IMVP6 VSUM1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	87 62	IMVP6 VSUM2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
87 62	IMVP6 VO1	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM	87 62	IMVP6 VO2	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.25 MM
87 62	IMVP6 VSEN_P	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM	87 62	IMVP6 VSEN_N	MIN_LINE_WIDTH=0.25 MM	MIN_NECK_WIDTH=0.2 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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	D	051-7546	A.0.0
SCALE	SHEET	OF	
NONE	62	96	



f=365KHz
 =PP5V_S3_REG
 Vout = 5.0V
 6A max output
 (Q7220 limit)

f=460KHz
 =PP3V3_S5_REG
 Vout = 3.3V
 5.5A max output
 (L7260 limit)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680651	37680668		ALL	NOT PERMITTED ASSOCIATED TO DESIGN
37680652	37680669		ALL	NOT PERMITTED ASSOCIATED TO DESIGN
15280778	15280693		ALL	4-Top Inductor Option associated to Regulator

M99 differences from last sync on 11/01/07 to M88 MLB:
 1. L7260 changed from M88 MLB inductors to 152S0693.
 2. Q7220 changed to 372S0512. Q7225 changed to 376S0511.
 3. U7200 changed to 353S2087.
 4. Added R7200, R7220, R7221, R7260, R7261, C7201.

5V / 3.3V Power Supply

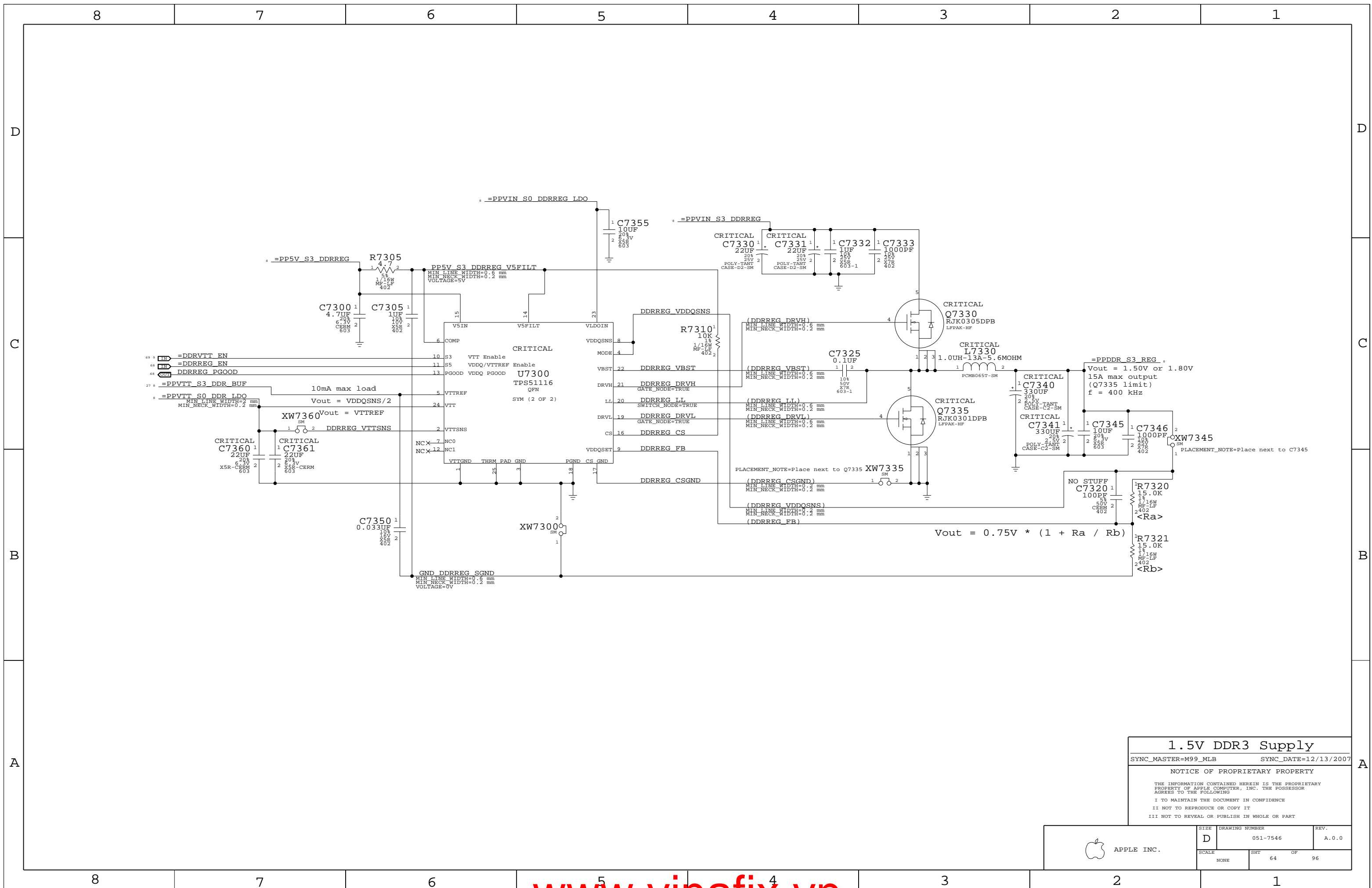
SYNC_MASTER=M99_MLB SYNC_DATE=01/09/2008

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SCALE	SHT	OF	REV.
NONE	63	96	



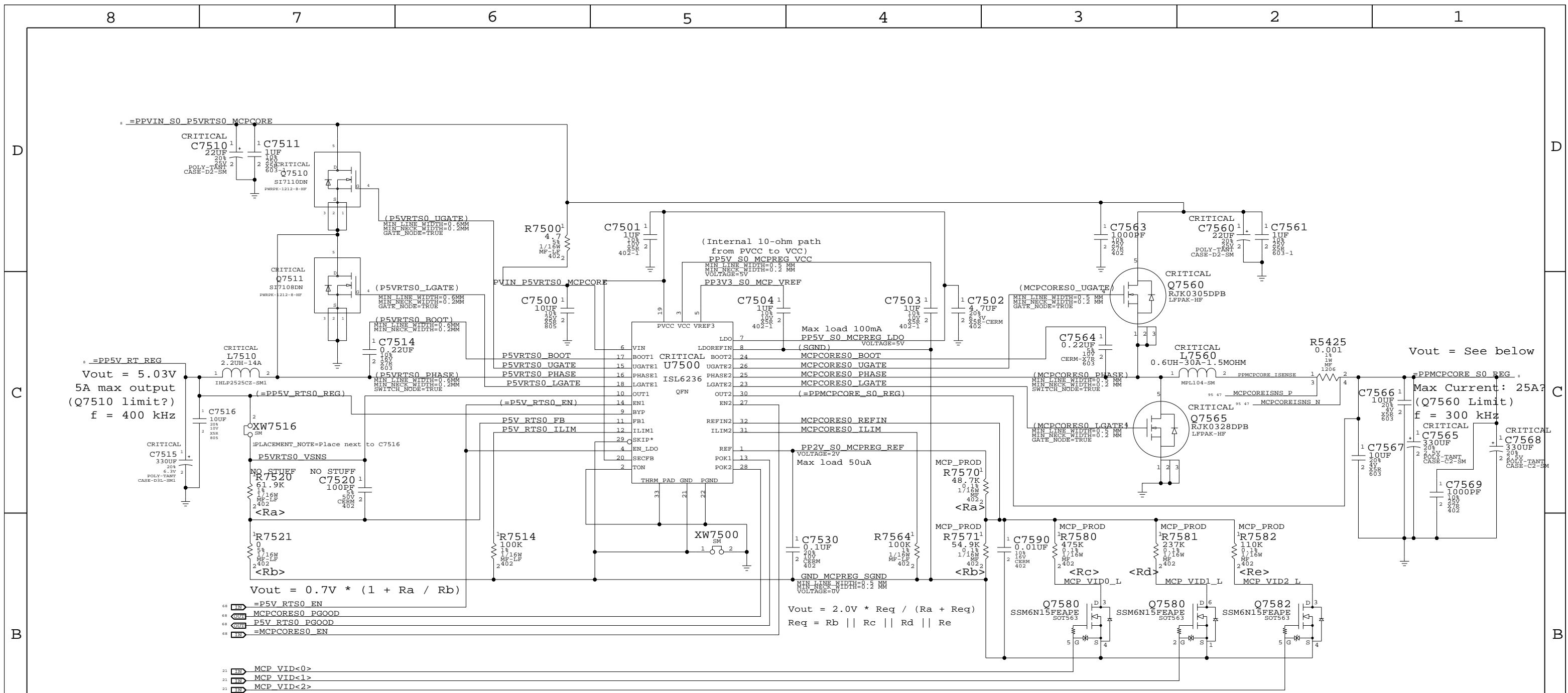
1.5V DDR3 Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/13/2007

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	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	
NONE	64	96	



MCP79 Rev A01 requires higher core & analog voltage

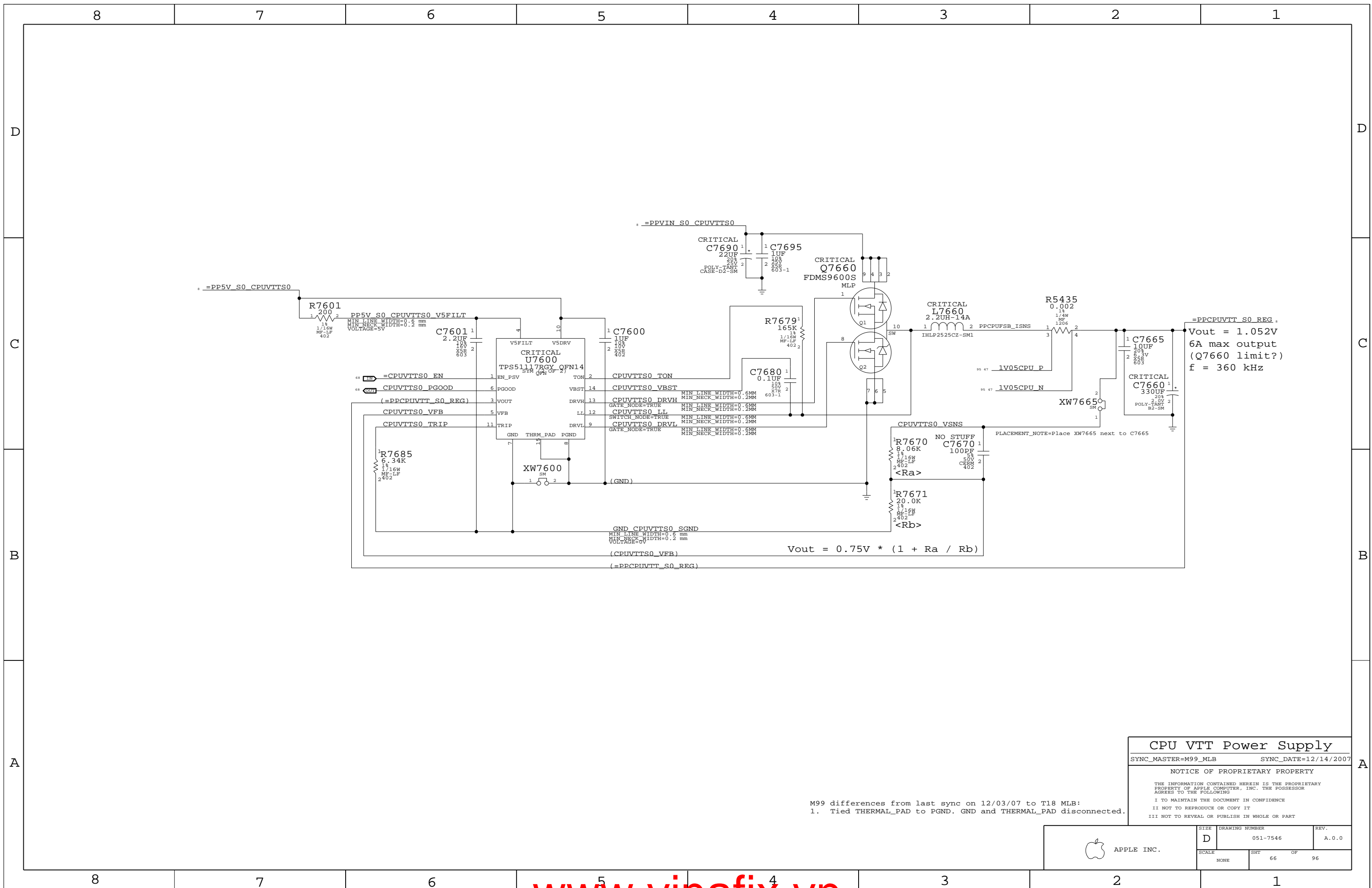
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0382	1	RES.MTL FILM,1/16W,48.7K,1,0402,SMD,LF	R7570		MCP_A01
114S0400	1	RES.MTL FILM,1/16W,76.8K,1,0402,SMD,LF	R7571		MCP_A01
114S0482	1	RES.MTL FILM,1/16W,523K,1,0402,SMD,LF	R7580		MCP_A01
114S0453	1	RES.MTL FILM,1/16W,267K,1,0402,SMD,LF	R7581		MCP_A01
114S0422	1	RES.MTL FILM,1/16W,130K,1,0402,SMD,LF	R7582		MCP_A01
114S0373	1	RES.MTL FILM,1/16W,40.2K,1,0402,SMD,LF	R7570		MCP_A01Q
114S0404	1	RES.MTL FILM,1/16W,84.5K,1,0402,SMD,LF	R7571		MCP_A01Q
114S0458	1	RES.MTL FILM,1/16W,301K,1,0402,SMD,LF	R7580		MCP_A01Q
114S0447	1	RES.MTL FILM,1/16W,237K,1,0402,SMD,LF	R7581		MCP_A01Q
114S0411	1	RES.MTL FILM,1/16W,100K,1,0402,SMD,LF	R7582		MCP_A01Q

VID<2:0>	Rev A01		Production	MCP Target
	Voltage	Voltage	Voltage	
000	+1.224V	+1.060V	+1.05V	
001	+1.159V	+0.994V	+1.00V	
010	+1.101V	+0.937V	+0.95V	
011	+1.049V	+0.885V	+0.90V	
100	+0.995V	+0.830V	+0.85V	
101	+0.952V	+0.789V	+0.80V	
110	+0.913V	+0.752V	+0.75V	
111	+0.876V	+0.719V	+0.70V	

1.05V / MCP Core Regulator
 SYNC_MASTER=M99_MLB SYNC_DATE=01/08/2008

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APPLE INC. DRAWING NUMBER: 051-7546 REV. A.0.0
 SCALE: NONE SHEET: 65 OF 96



CPU VTT Power Supply

SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007

NOTICE OF PROPRIETARY PROPERTY

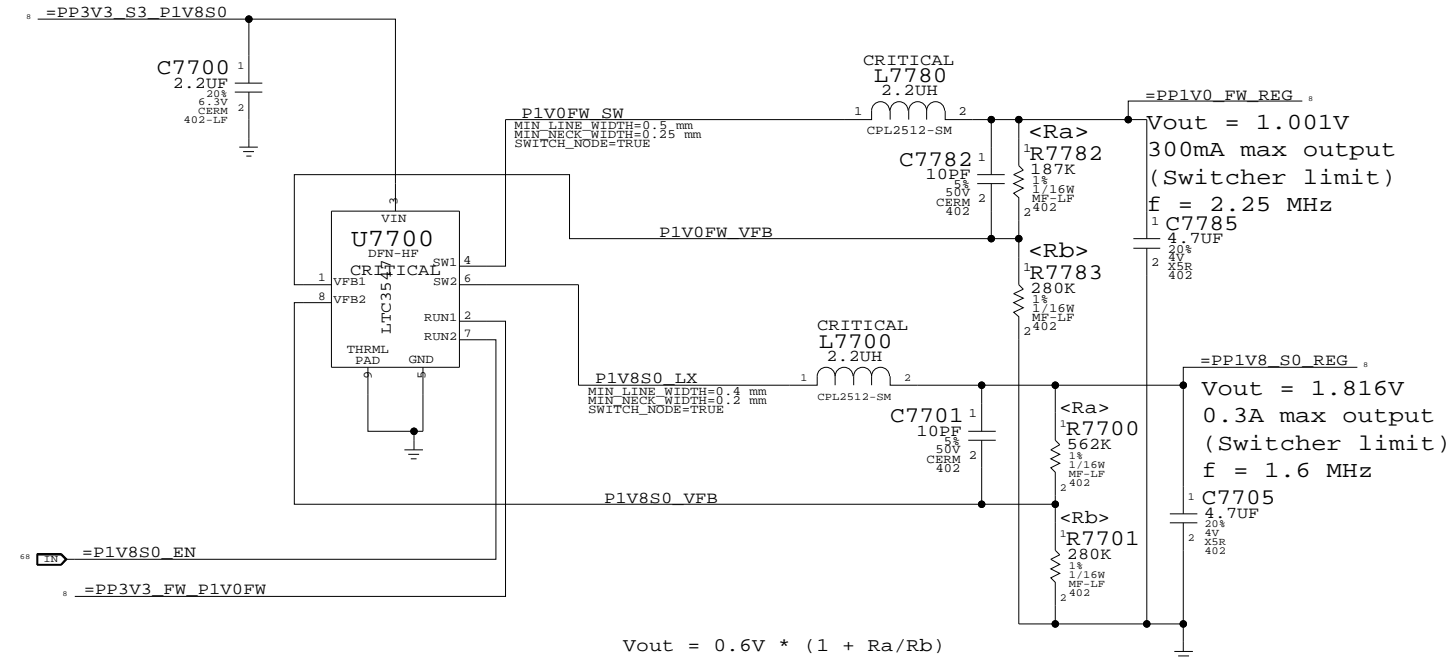
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M99 differences from last sync on 12/03/07 to T18 MLB:
 1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	66	96	

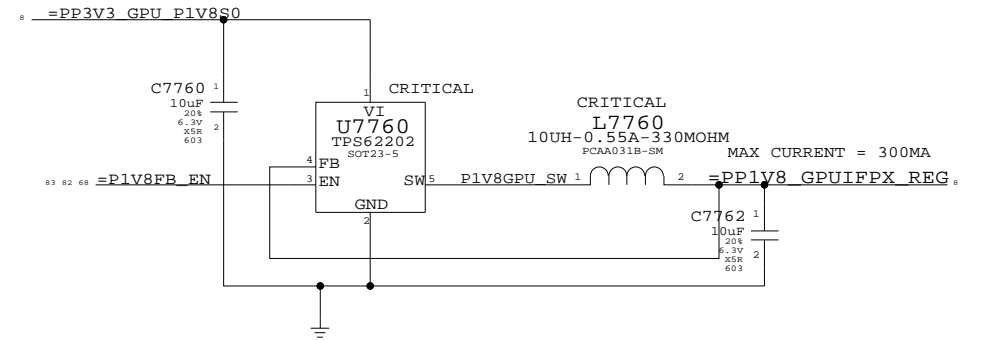
1.8V S0 Switcher / 1.0VFW SWITCHER

S5 power required for output discharge feature

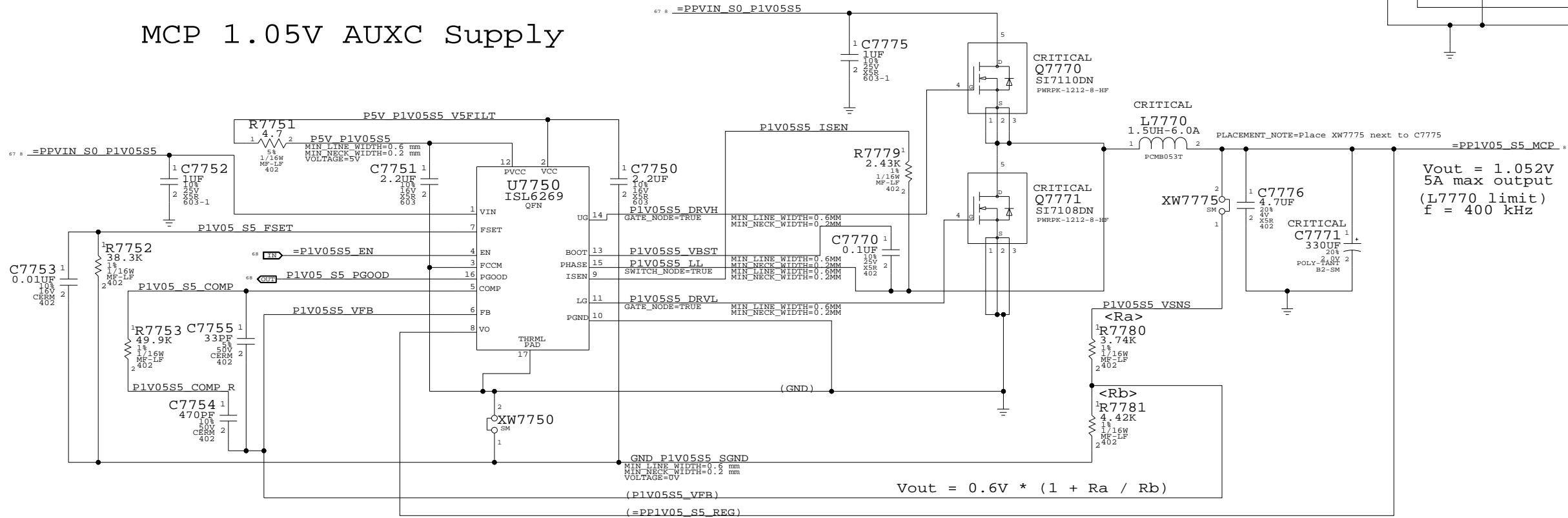


1.8V S0 Switcher

INPUT RAIL IS 3.3V S0



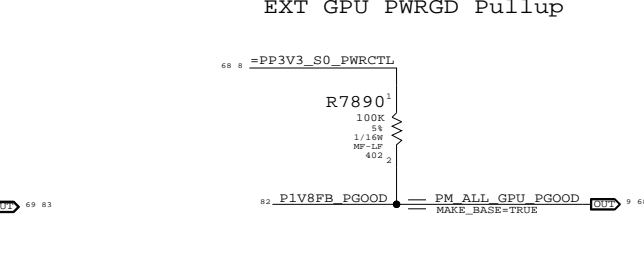
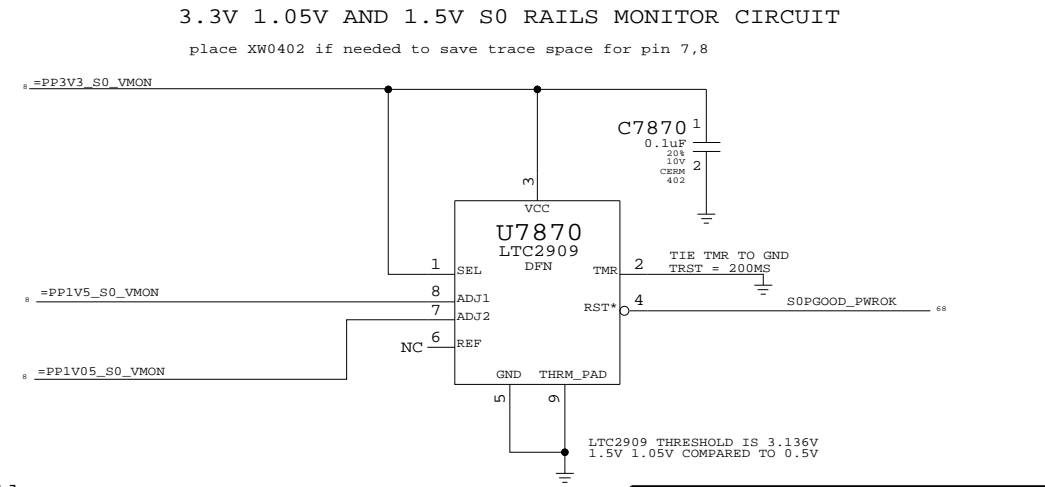
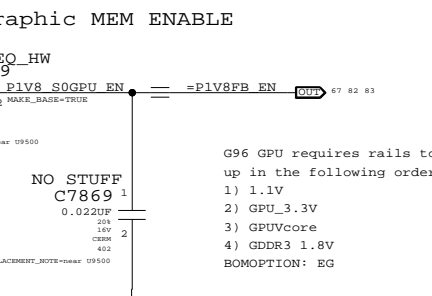
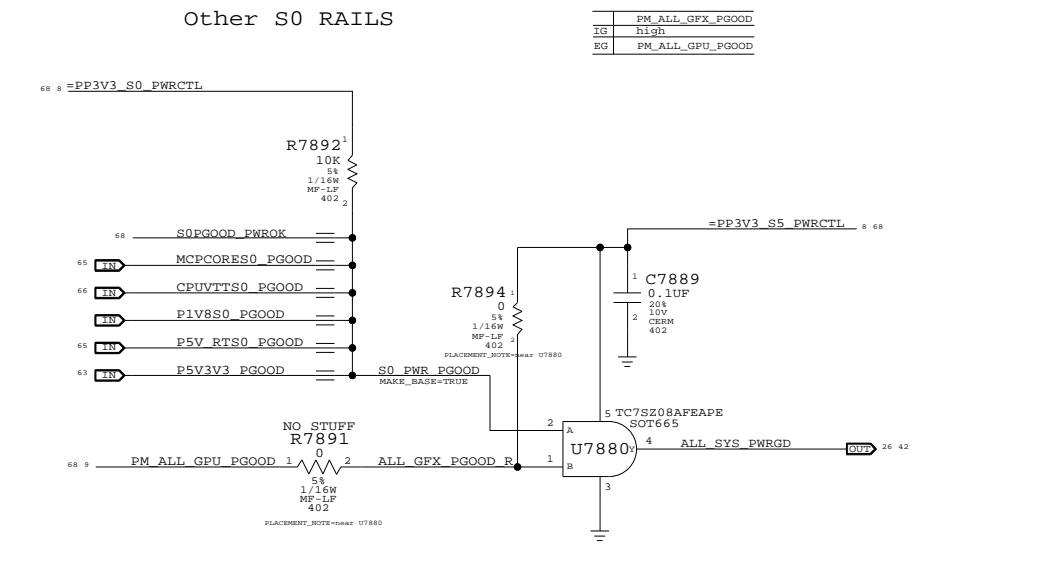
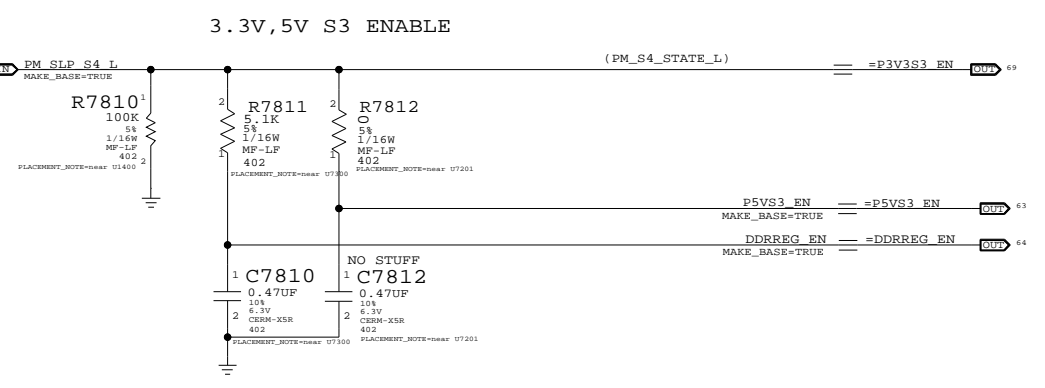
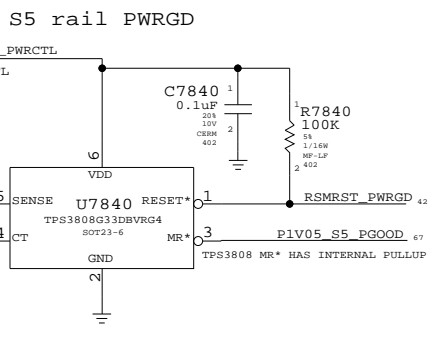
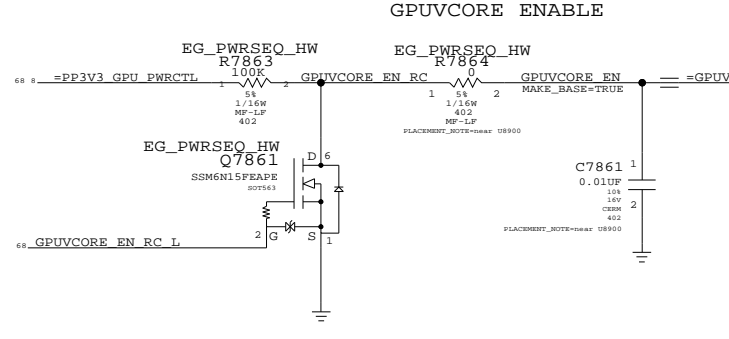
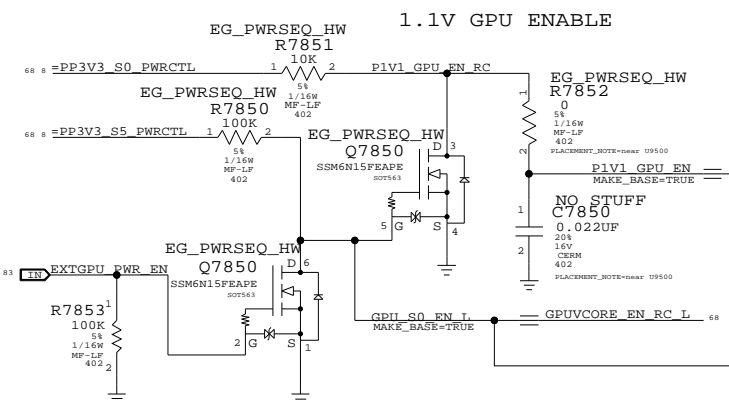
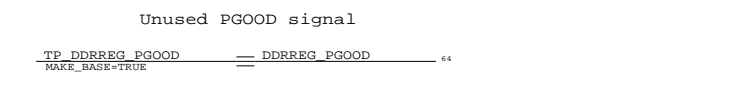
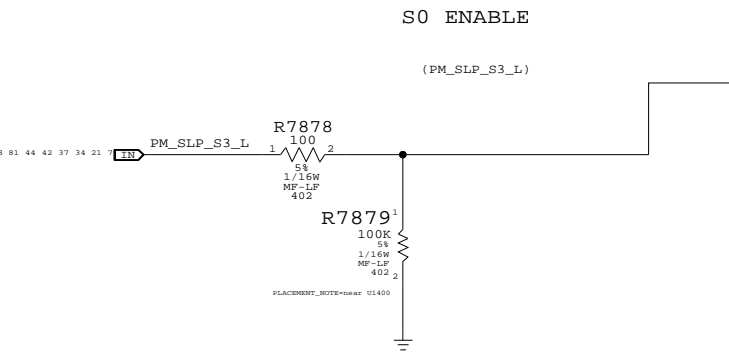
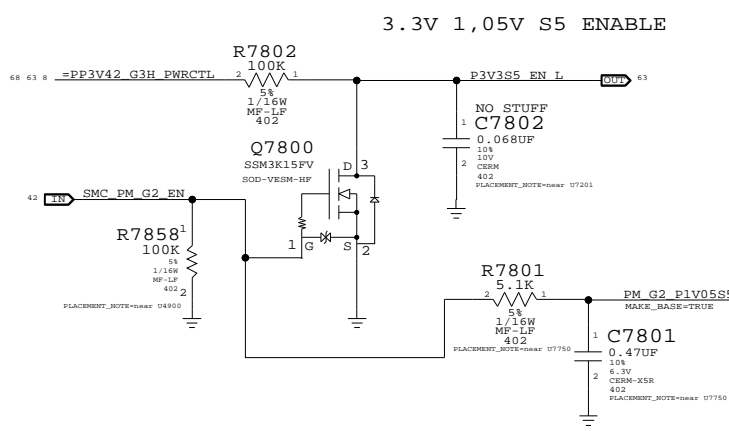
MCP 1.05V AUXC Supply



Misc Power Supplies
 SYNC_MASTER=M99_MLB SYNC_DATE=12/14/2007
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	67		

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

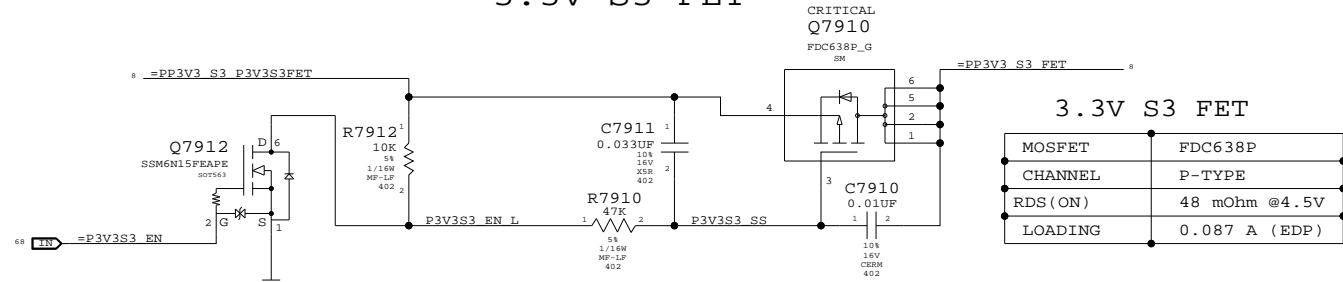


- G96 GPU requires rails to come up in the following order:
- 1) 1.1v
 - 2) GPU_3.3v
 - 3) GPUVcore
 - 4) GDDR3 1.8v
- BOMOPTION: EG

Power Control
 SYNC_MASTER=PWRSONC SYNC_DATE=05/12/2008

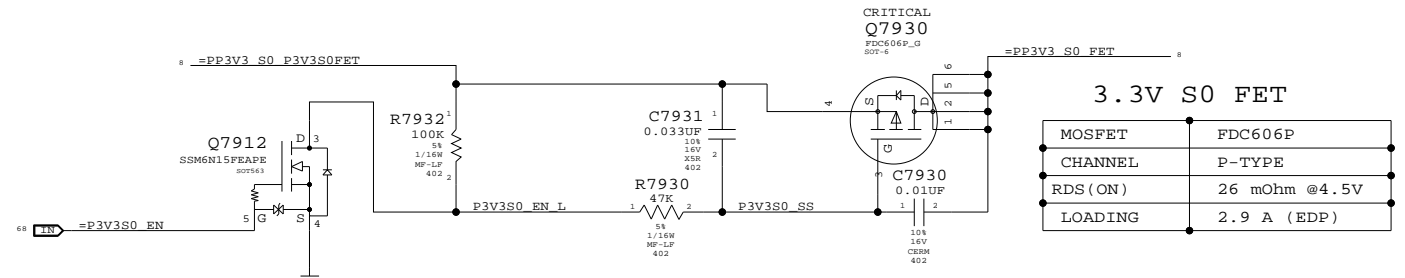
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3.3V S3 FET



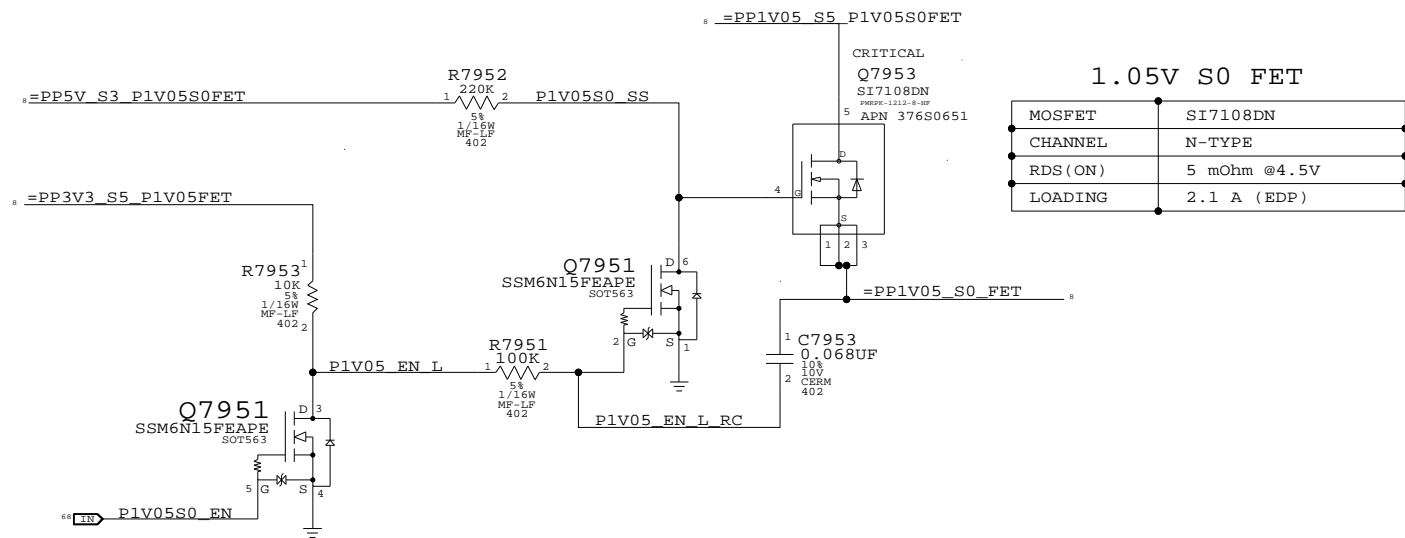
MOSFET	FDC638P
CHANNEL	P-TYPE
RDS(ON)	48 mOhm @4.5V
LOADING	0.087 A (EDP)

3.3V S0 FET



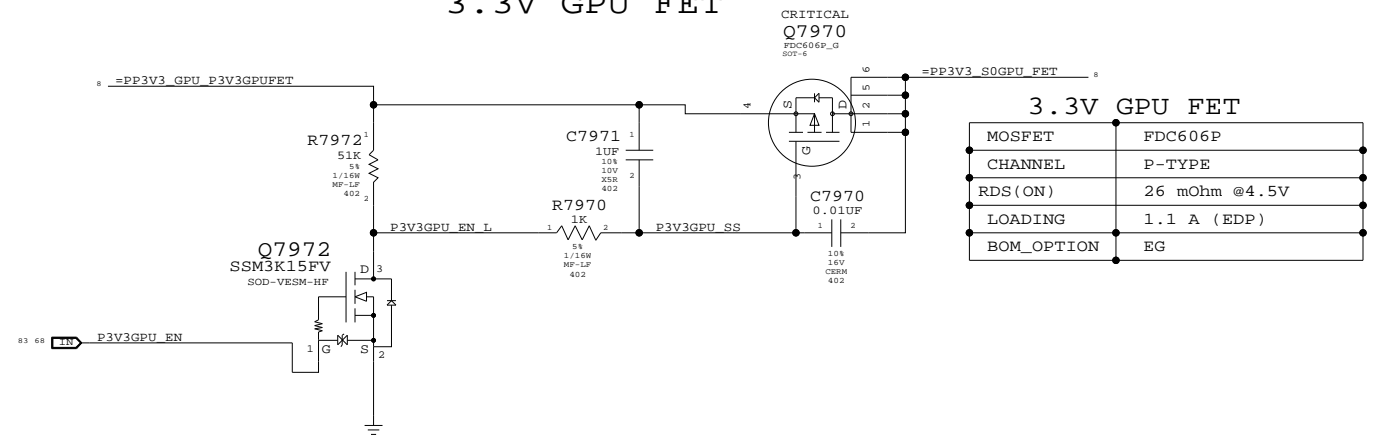
MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	2.9 A (EDP)

1.05V S0 FET



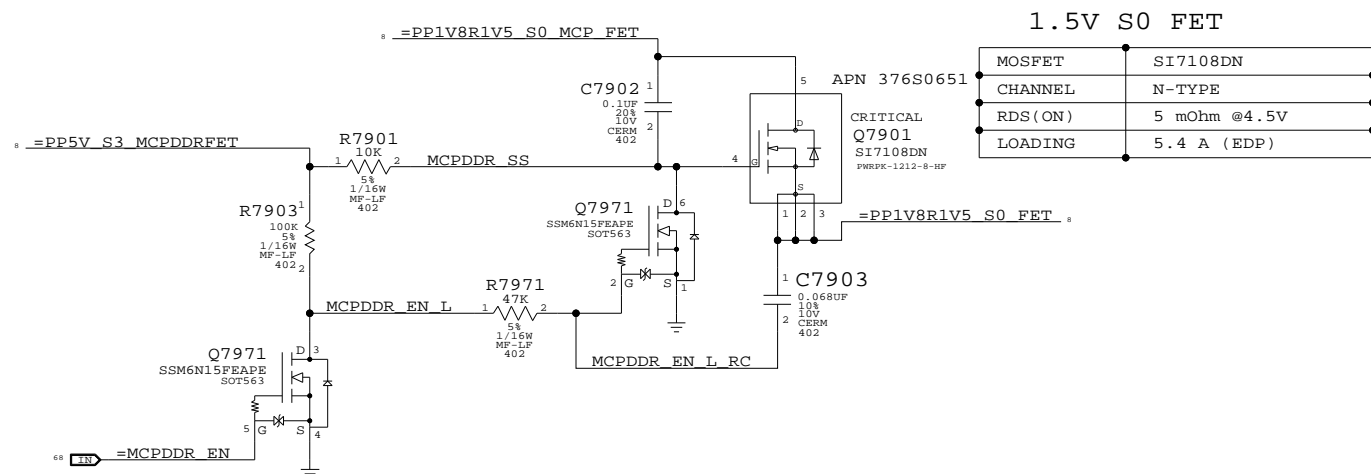
MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	2.1 A (EDP)

3.3V GPU FET



MOSFET	FDC606P
CHANNEL	P-TYPE
RDS(ON)	26 mOhm @4.5V
LOADING	1.1 A (EDP)
BOM_OPTION	EG

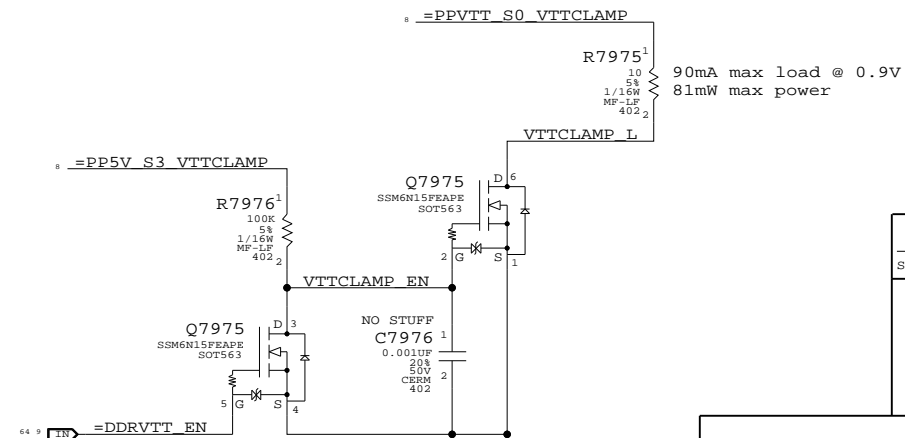
1.5V S0 FET



MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	5 mOhm @4.5V
LOADING	5.4 A (EDP)

MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low before rail is turned off, and remains low until after rail turns back on or DIMMs will exit self-refresh prematurely. MEM_VTT_EN output from MCP79 used to enable clamp on VTT rail, which pulls all CKE signals low through VTT termination resistors.



Power FETs	
SYNC_MASTER=PWRSONC	SYNC_DATE=05/12/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	69	96	

Page Notes

Power aliases required by this page:
 - =PPIV2_GPU_PEX_PLLXVDD
 - =PPIV2_GPU_PEX_IOVDDQ
 - =PPIV2_GPU_PEX_IOVDD

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

=PPIV1_GPU_PEX_PLLXVDD
 =PPIV1_GPU_PEX_IOVDDQ
 =PPIV1_GPU_PEX_IOVDD

PEX 1.1V Current = 2A

250mA

1500mA

180mA

PPIV1_GPU_PEX_PLLXVDD F
 MIN_LINE_WIDTH=0.25 mm
 MIN_DRILL_DIAMETER=0.25 mm
 VOLTAGE=1.2V

L8015
 10NH-600MA

NC_GPU_DFM

NO_TEST=TRUE

OMIT

U8000

NB9P-GS

BGA

SYMBOL 2 OF 9

AK16

AK17

AK21

AK24

AK27

AG11

AG12

AG13

AG15

AG16

AG17

AG18

AG22

AG23

AG24

AG25

AG26

AJ14

AJ15

AJ19

AJ21

AJ22

AJ24

AJ25

AJ27

AK18

AK20

AK23

AK26

AL16

AG14

AD20 GPU_VDD_SENSE 78

AD19 GPU_GND_SENSE 78

PEX_PLLXVDD

VDD_SENSE

GND_SENSE



NV G96 PCI-E
 SYNC_MASTER=MUXGFx SYNC_DATE=07/10/2008

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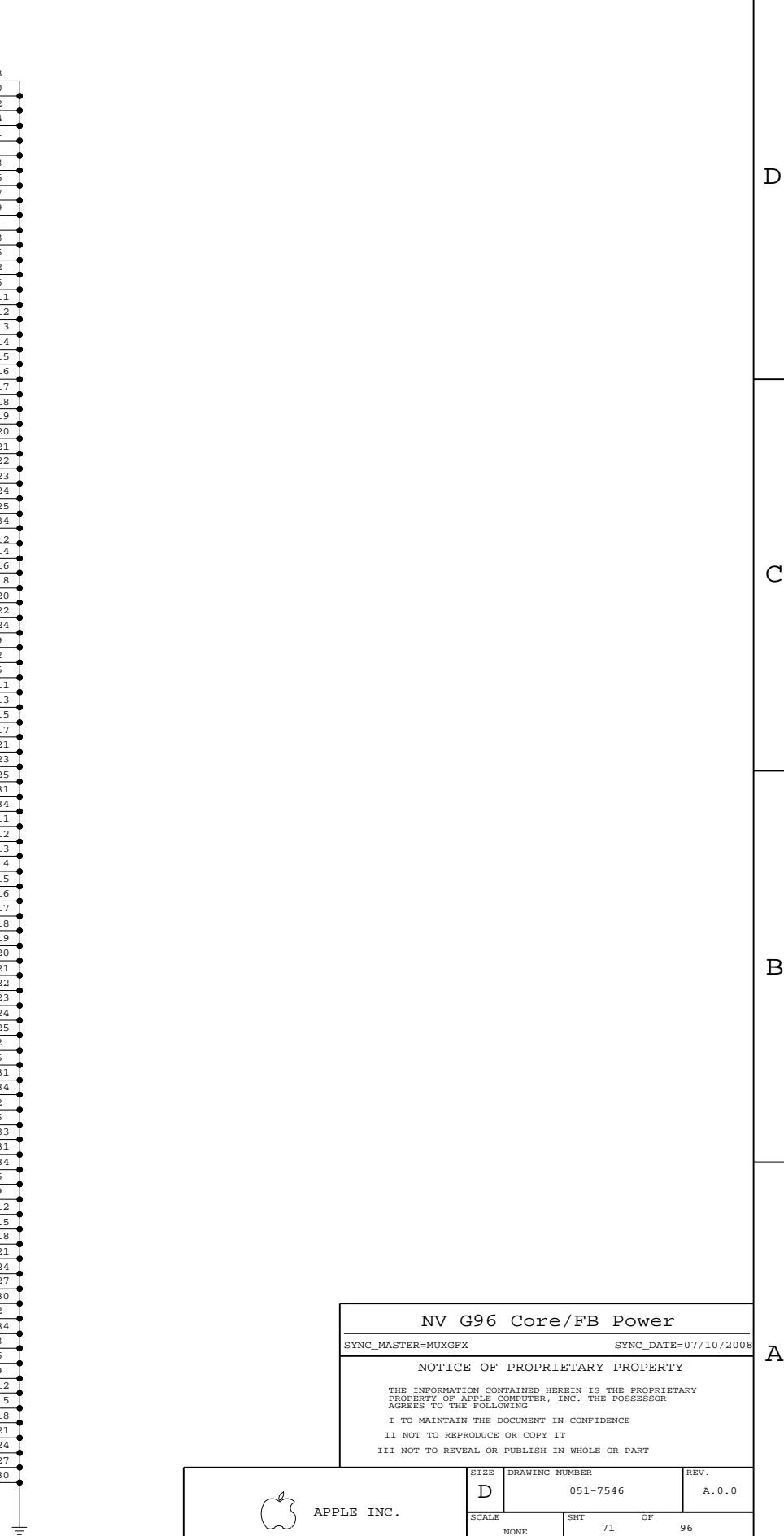
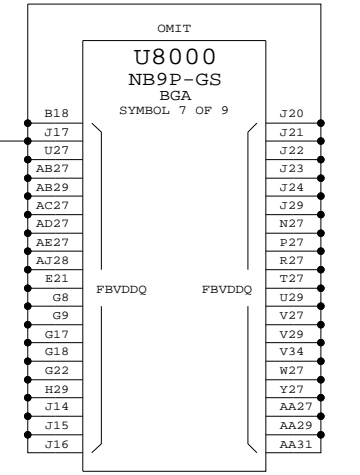
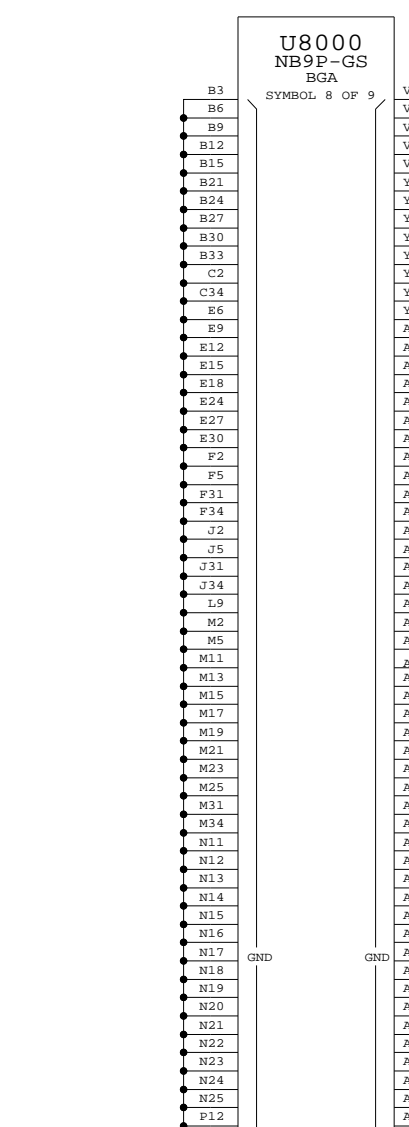
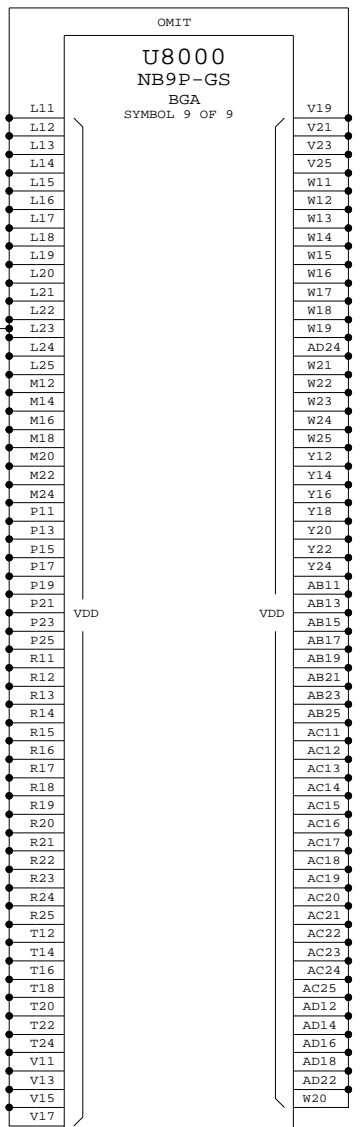
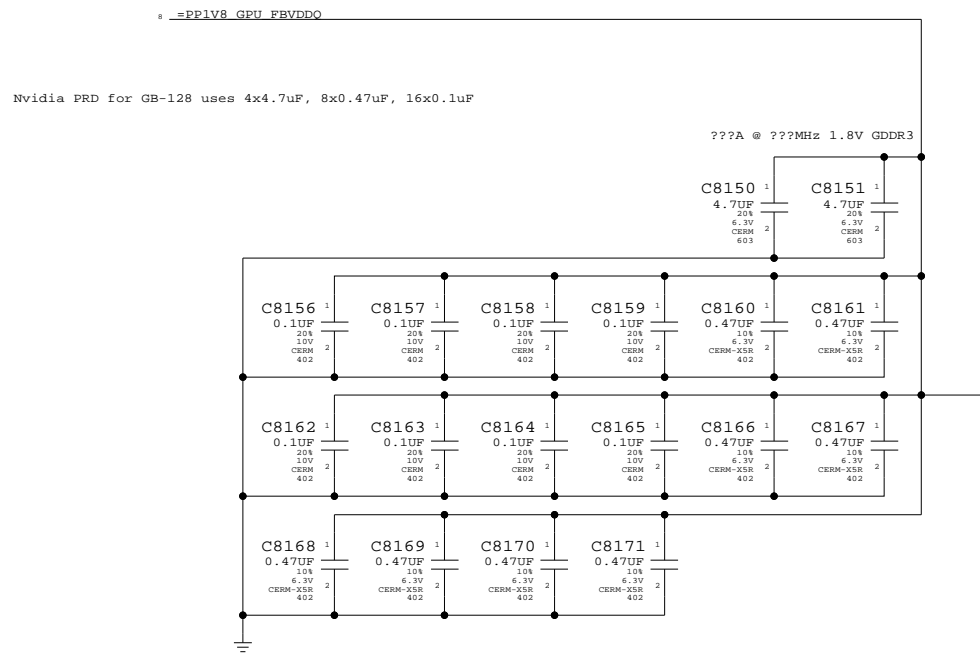
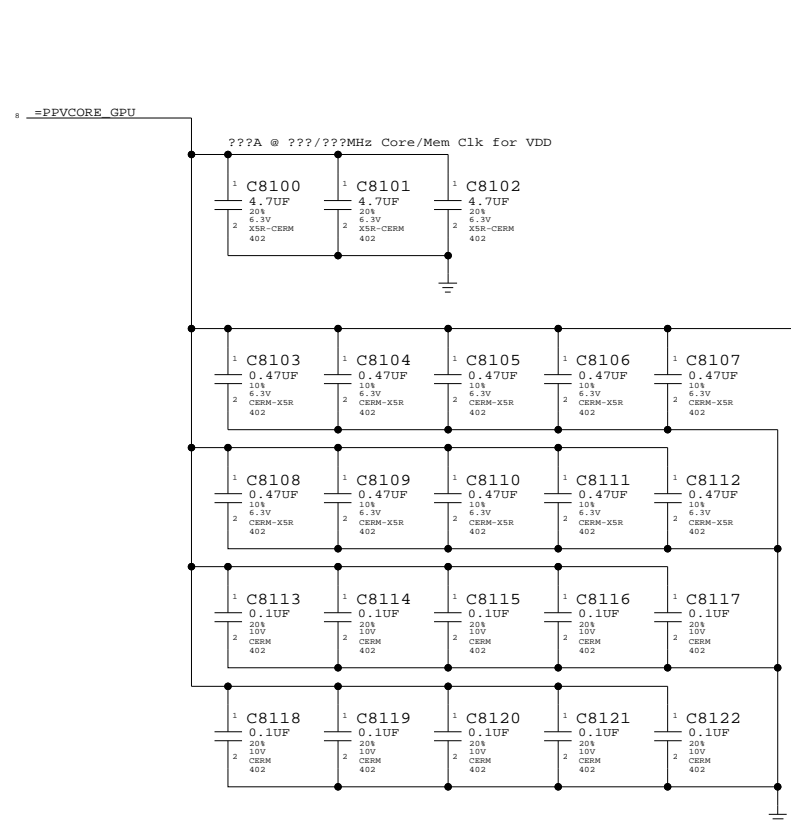
APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	70		

Page Notes

Power aliases required by this page:
 - =PPVCORE_GPU
 - =PP1V8_GPU_FBVDDQ

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



NV G96 Core/FB Power
 SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	71 OF 96

Page Notes

Power aliases required by this page:
- =PP1V2_GPU_FBPLLAVDD
- =PP1V8_GPU_FBIO
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
(NONE)

U8000
NB9P-GS
BGA
SYMBOL 3 OF 9

Table of pin connections for U8000, including signals like FBA_DQ<0>, FBA_CMD0, FBA_CLK0, FBA_DQM0, FBA_DQS_RN0, FBA_DQS_WP0, FBA_DQS_WP0, FBA_RFU0, FBA_DEBUG, FBCAL_PD_VDDQ, FBCAL_PU_GND, FBCAL_TERM_GND.

U8000
NB9P-GS
BGA
SYMBOL 4 OF 9

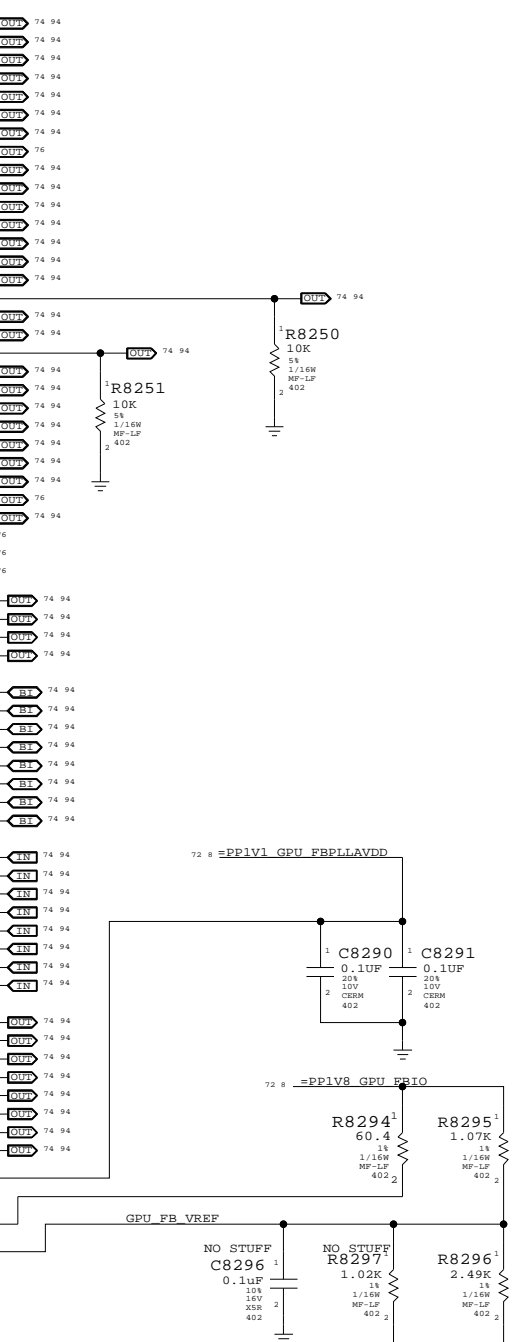
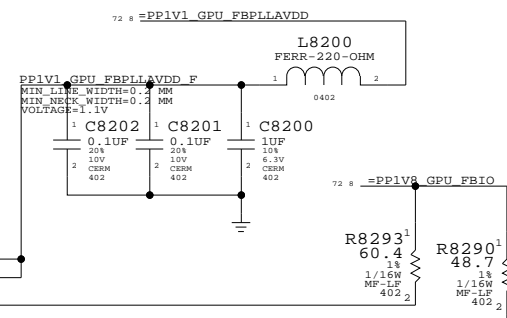
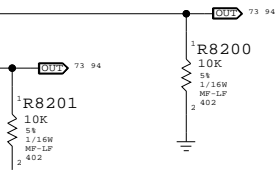
Table of pin connections for U8000, including signals like FBC_CMD0, FBC_CMD1, FBC_CMD2, FBC_CMD3, FBC_CMD4, FBC_CMD5, FBC_CMD6, FBC_CMD7, FBC_CMD8, FBC_CMD9, FBC_CMD10, FBC_CMD11, FBC_CMD12, FBC_CMD13, FBC_CMD14, FBC_CMD15, FBC_CMD16, FBC_CMD17, FBC_CMD18, FBC_CMD19, FBC_CMD20, FBC_CMD21, FBC_CMD22, FBC_CMD23, FBC_CMD24, FBC_CMD25, FBC_CMD26, FBC_CMD27, FBC_CMD28, FBC_CMD29, FBC_CMD30, FBC_CLK0, FBC_CLK1, FBC_CLK1*, FBC_DQM0, FBC_DQM1, FBC_DQM2, FBC_DQM3, FBC_DQM4, FBC_DQM5, FBC_DQM6, FBC_DQM7, FBC_DQS_RN0, FBC_DQS_RN1, FBC_DQS_RN2, FBC_DQS_RN3, FBC_DQS_RN4, FBC_DQS_RN5, FBC_DQS_RN6, FBC_DQS_RN7, FBC_DQS_WP0, FBC_DQS_WP1, FBC_DQS_WP2, FBC_DQS_WP3, FBC_DQS_WP4, FBC_DQS_WP5, FBC_DQS_WP6, FBC_DQS_WP7, FBC_DLLAVDD1, FBC_PLLAVDD1, FBC_DEBUG, FBC_RFU0, FBC_RFU1, FBC_RFU2, FBC_RFU3, FBC_RFU4, FBC_RFU5, FBC_RFU6, FBC_RFU7.

U8000
NB9P-GS
BGA
SYMBOL 3 OF 9

Table of pin connections for U8000, including signals like FBA_DQ<0>, FBA_DQ<1>, FBA_DQ<2>, FBA_DQ<3>, FBA_DQ<4>, FBA_DQ<5>, FBA_DQ<6>, FBA_DQ<7>, FBA_DQ<8>, FBA_DQ<9>, FBA_DQ<10>, FBA_DQ<11>, FBA_DQ<12>, FBA_DQ<13>, FBA_DQ<14>, FBA_DQ<15>, FBA_DQ<16>, FBA_DQ<17>, FBA_DQ<18>, FBA_DQ<19>, FBA_DQ<20>, FBA_DQ<21>, FBA_DQ<22>, FBA_DQ<23>, FBA_DQ<24>, FBA_DQ<25>, FBA_DQ<26>, FBA_DQ<27>, FBA_DQ<28>, FBA_DQ<29>, FBA_DQ<30>, FBA_DQ<31>, FBA_DQ<32>, FBA_DQ<33>, FBA_DQ<34>, FBA_DQ<35>, FBA_DQ<36>, FBA_DQ<37>, FBA_DQ<38>, FBA_DQ<39>, FBA_DQ<40>, FBA_DQ<41>, FBA_DQ<42>, FBA_DQ<43>, FBA_DQ<44>, FBA_DQ<45>, FBA_DQ<46>, FBA_DQ<47>, FBA_DQ<48>, FBA_DQ<49>, FBA_DQ<50>, FBA_DQ<51>, FBA_DQ<52>, FBA_DQ<53>, FBA_DQ<54>, FBA_DQ<55>, FBA_DQ<56>, FBA_DQ<57>, FBA_DQ<58>, FBA_DQ<59>, FBA_DQ<60>, FBA_DQ<61>, FBA_DQ<62>, FBA_DQ<63>.

U8000
NB9P-GS
BGA
SYMBOL 4 OF 9

Table of pin connections for U8000, including signals like FBA_DQ<0>, FBA_DQ<1>, FBA_DQ<2>, FBA_DQ<3>, FBA_DQ<4>, FBA_DQ<5>, FBA_DQ<6>, FBA_DQ<7>, FBA_DQ<8>, FBA_DQ<9>, FBA_DQ<10>, FBA_DQ<11>, FBA_DQ<12>, FBA_DQ<13>, FBA_DQ<14>, FBA_DQ<15>, FBA_DQ<16>, FBA_DQ<17>, FBA_DQ<18>, FBA_DQ<19>, FBA_DQ<20>, FBA_DQ<21>, FBA_DQ<22>, FBA_DQ<23>, FBA_DQ<24>, FBA_DQ<25>, FBA_DQ<26>, FBA_DQ<27>, FBA_DQ<28>, FBA_DQ<29>, FBA_DQ<30>, FBA_DQ<31>, FBA_DQ<32>, FBA_DQ<33>, FBA_DQ<34>, FBA_DQ<35>, FBA_DQ<36>, FBA_DQ<37>, FBA_DQ<38>, FBA_DQ<39>, FBA_DQ<40>, FBA_DQ<41>, FBA_DQ<42>, FBA_DQ<43>, FBA_DQ<44>, FBA_DQ<45>, FBA_DQ<46>, FBA_DQ<47>, FBA_DQ<48>, FBA_DQ<49>, FBA_DQ<50>, FBA_DQ<51>, FBA_DQ<52>, FBA_DQ<53>, FBA_DQ<54>, FBA_DQ<55>, FBA_DQ<56>, FBA_DQ<57>, FBA_DQ<58>, FBA_DQ<59>, FBA_DQ<60>, FBA_DQ<61>, FBA_DQ<62>, FBA_DQ<63>.



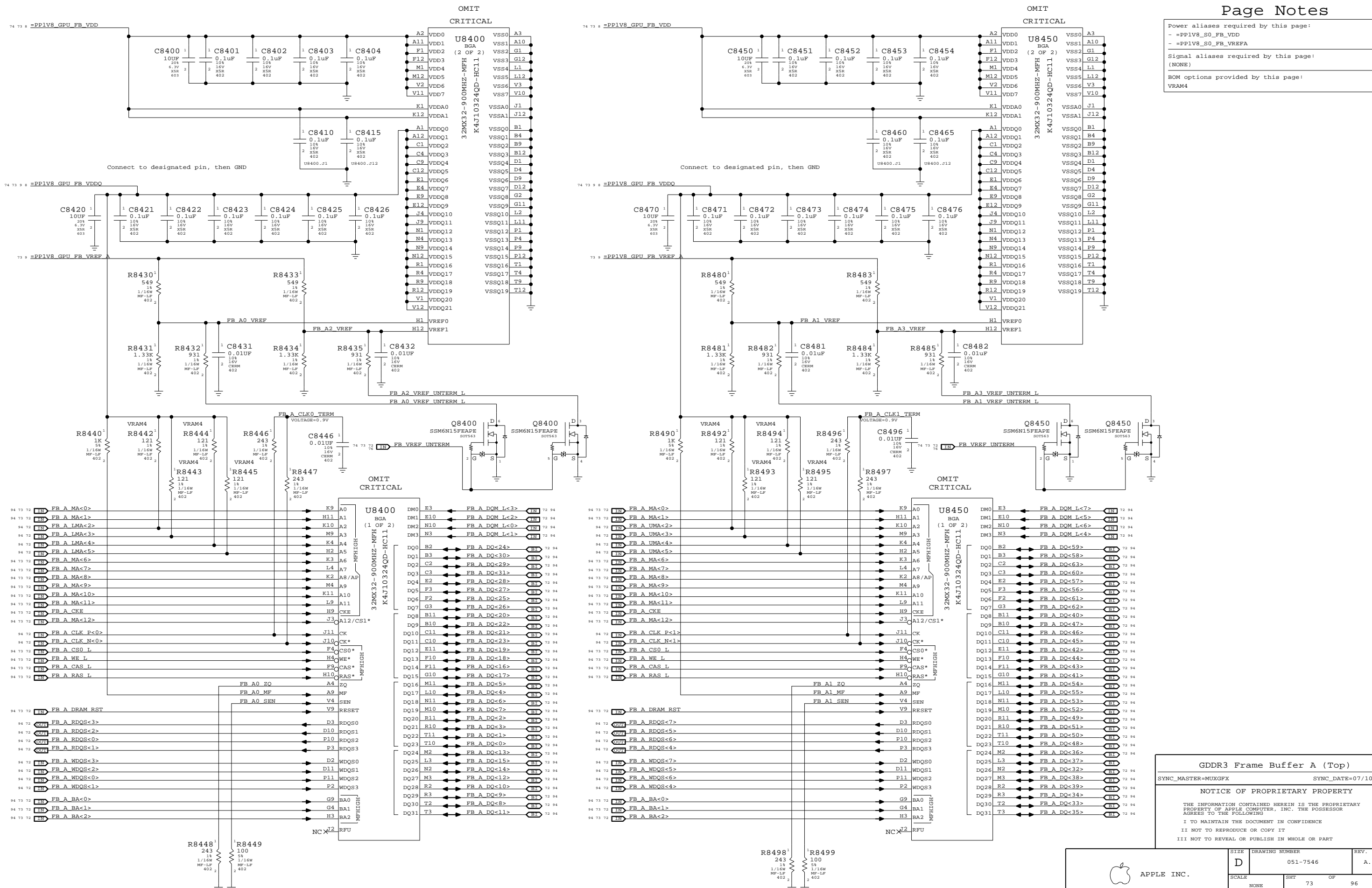
NV G96 Frame Buffer I/F
SYNC_MASTER=MUXGF
SYNC_DATE=07/10/2008
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Table with columns: SIZE, DRAWING NUMBER, REV., SCALE, SHEET, OF, PART.

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VREFA

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 VRAM4



GDDR3 Frame Buffer A (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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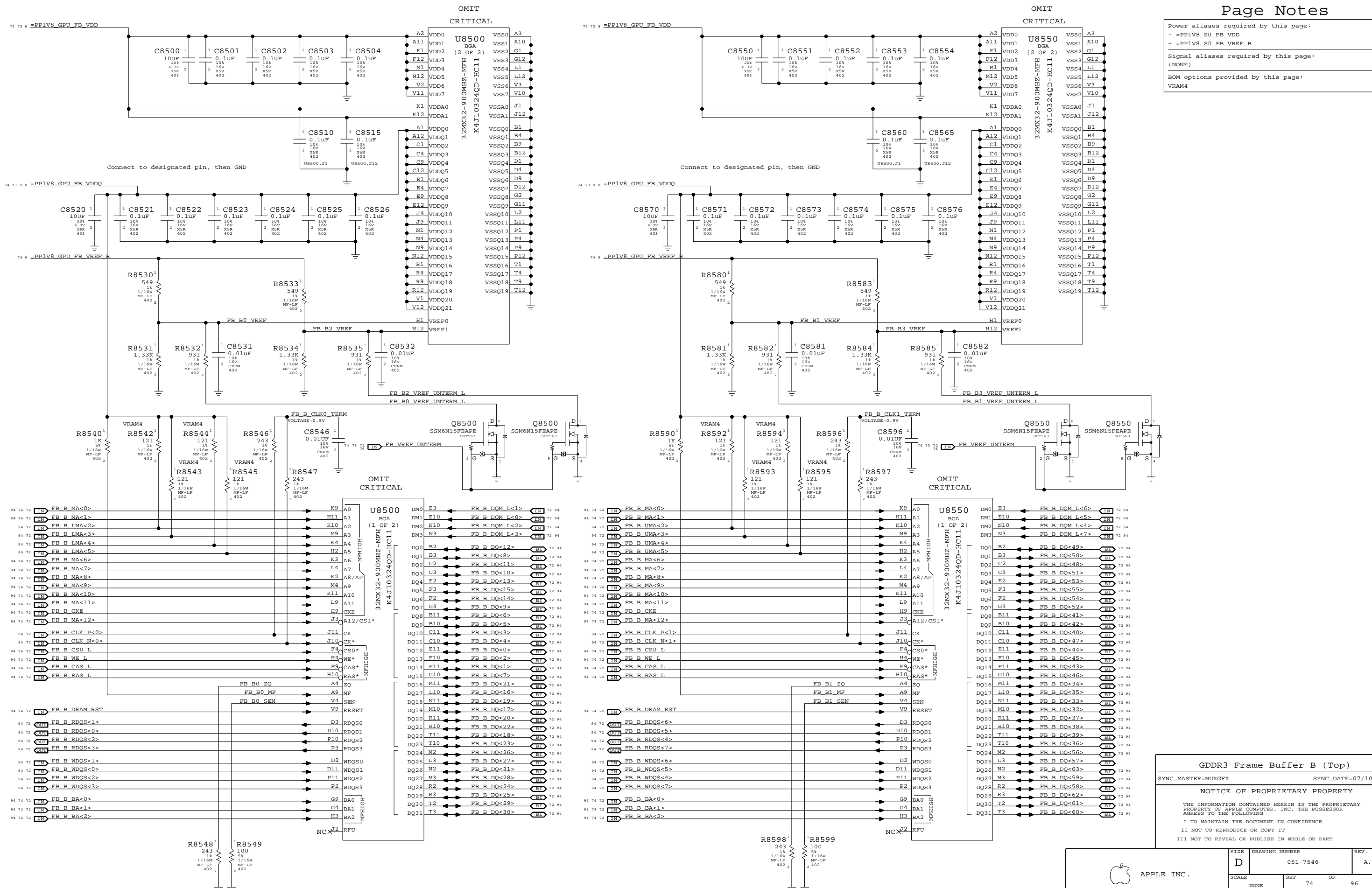


SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHEET	OF
NONE	73	96

Power aliases required by this page:
 - =PPIV8_S0_FB_VDD
 - =PPIV8_S0_FB_VREF_B

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 VRAM4



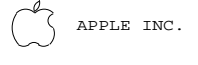
GDDR3 Frame Buffer B (Top)

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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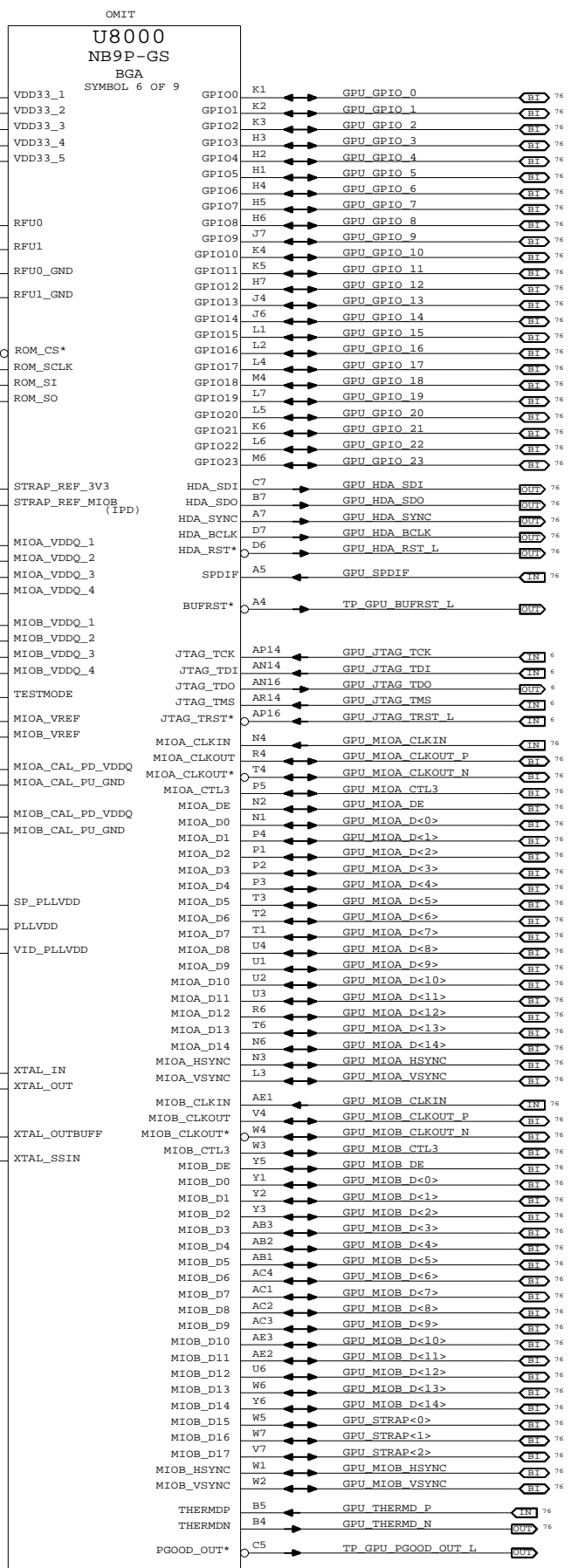
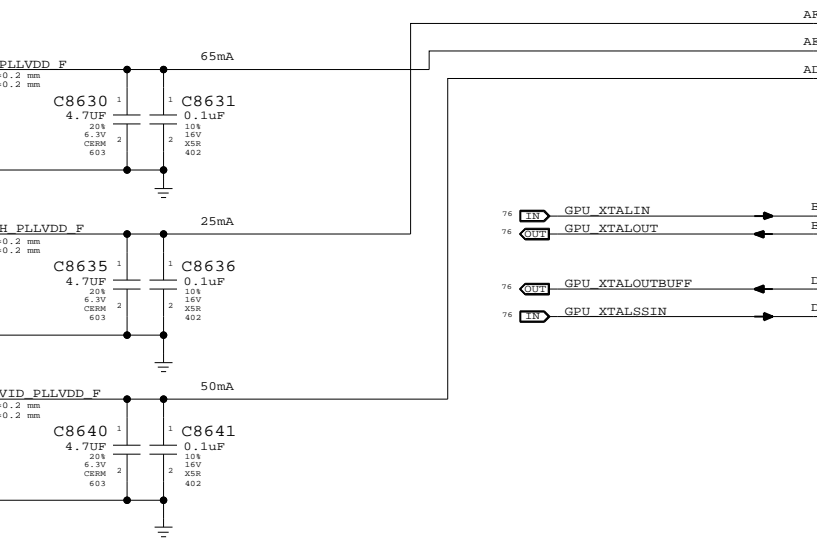
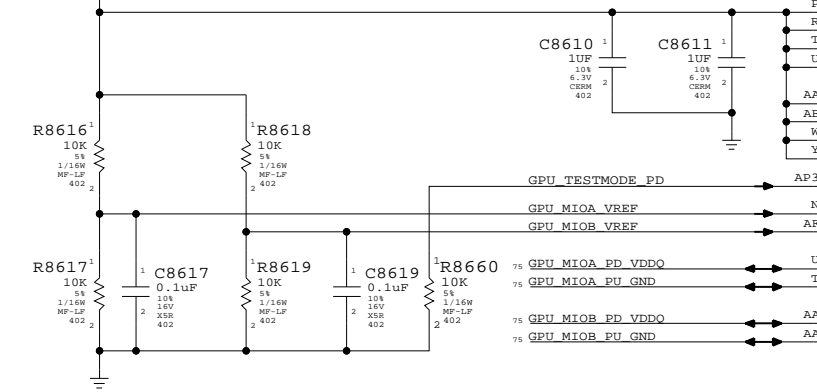
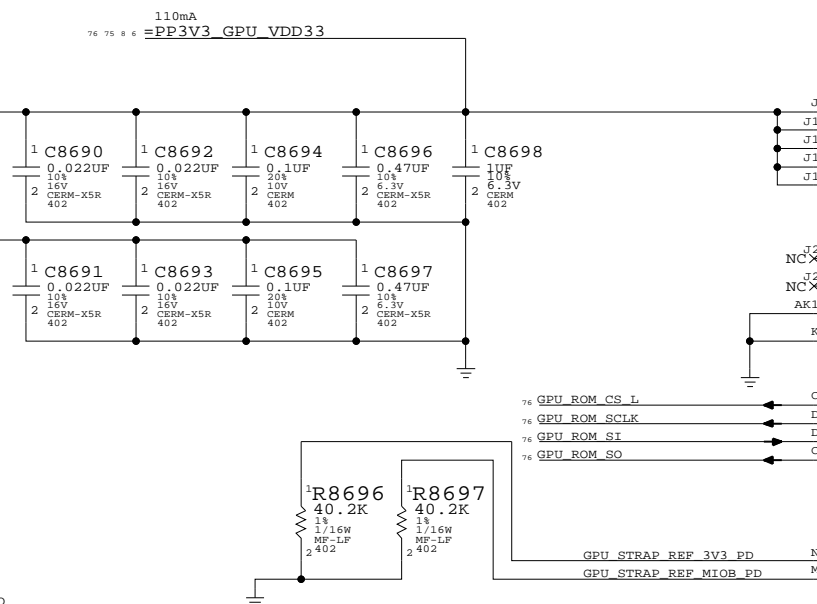
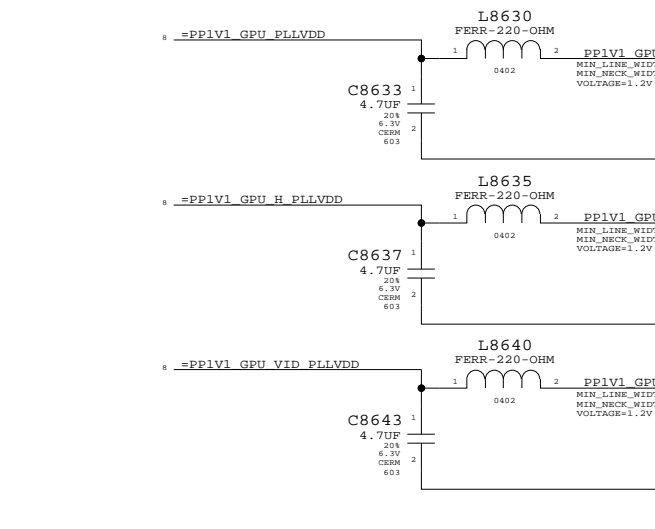
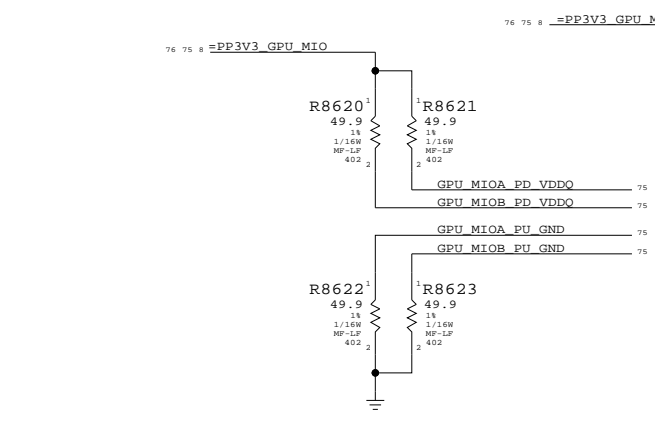
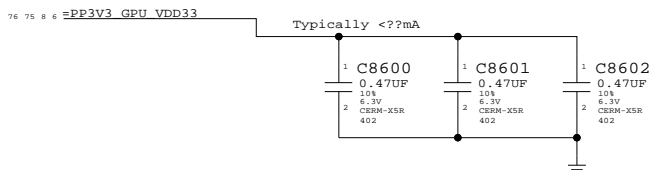
SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHEET	OF
NONE	74	96

Page Notes

Power aliases required by this page:
 - =PP3V3_GPU_VDD33
 - =PP3V3_GPU_MIO
 - =PP1V2_GPU_PLLVDD
 - =PP1V2_GPU_H_PLLVDD
 - =PP1V2_GPU_VID_PLLVDD

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)



Pin	Signal	Pin	Signal
GPU_GPIO_0	K1	GPU_HDA_SDI	C7
GPU_GPIO_1	K2	GPU_HDA_SDO	B7
GPU_GPIO_2	K3	GPU_HDA_SYNC	A7
GPU_GPIO_3	H3	GPU_HDA_BCLK	D7
GPU_GPIO_4	H2	GPU_HDA_RST_L	D6
GPU_GPIO_5	H1	GPU_SPDIF	A5
GPU_GPIO_6	H4	TP_GPU_BUFRST_L	A4
GPU_GPIO_7	H5	GPU_JTAG_TCK	AP14
GPU_GPIO_8	H6	GPU_JTAG_TDI	AN14
GPU_GPIO_9	J7	GPU_JTAG_TDO	AN16
GPU_GPIO_10	K4	GPU_JTAG_TMS	AR14
GPU_GPIO_11	K5	GPU_JTAG_TRST_L	AP16
GPU_GPIO_12	H7	GPU_MIOA_CLKIN	N4
GPU_GPIO_13	J4	GPU_MIOA_CLKOUT_P	R4
GPU_GPIO_14	J6	GPU_MIOA_CLKOUT_N	T4
GPU_GPIO_15	L1	GPU_MIOA_CTL3	P5
GPU_GPIO_16	L2	GPU_MIOA_DE	N2
GPU_GPIO_17	L4	GPU_MIOA_D<0>	N1
GPU_GPIO_18	M4	GPU_MIOA_D<1>	P4
GPU_GPIO_19	L7	GPU_MIOA_D<2>	P1
GPU_GPIO_20	L5	GPU_MIOA_D<3>	P2
GPU_GPIO_21	K6	GPU_MIOA_D<4>	P3
GPU_GPIO_22	L6	GPU_MIOA_D<5>	T3
GPU_GPIO_23	M6	GPU_MIOA_D<6>	T2
GPU_HDA_SDI	C7	GPU_MIOA_D<7>	T1
GPU_HDA_SDO	B7	GPU_MIOA_D<8>	U4
GPU_HDA_SYNC	A7	GPU_MIOA_D<9>	U1
GPU_HDA_BCLK	D7	GPU_MIOA_D<10>	U2
GPU_HDA_RST_L	D6	GPU_MIOA_D<11>	U3
GPU_SPDIF	A5	GPU_MIOA_D<12>	R6
TP_GPU_BUFRST_L	A4	GPU_MIOA_D<13>	T6
GPU_JTAG_TCK	AP14	GPU_MIOA_D<14>	N6
GPU_JTAG_TDI	AN14	GPU_MIOA_HSYNC	N3
GPU_JTAG_TDO	AN16	GPU_MIOA_VSYNC	L3
GPU_JTAG_TMS	AR14	GPU_MIOB_CLKIN	AE1
GPU_JTAG_TRST_L	AP16	GPU_MIOB_CLKOUT_P	V4
GPU_MIOA_CLKIN	N4	GPU_MIOB_CLKOUT_N	W4
GPU_MIOA_CLKOUT_P	R4	GPU_MIOB_CTL3	W3
GPU_MIOA_CLKOUT_N	T4	GPU_MIOB_DE	Y5
GPU_MIOA_CTL3	P5	GPU_MIOB_D<0>	Y1
GPU_MIOA_DE	N2	GPU_MIOB_D<1>	Y2
GPU_MIOA_D<0>	N1	GPU_MIOB_D<2>	Y3
GPU_MIOA_D<1>	P4	GPU_MIOB_D<3>	AB3
GPU_MIOA_D<2>	P1	GPU_MIOB_D<4>	AB2
GPU_MIOA_D<3>	P2	GPU_MIOB_D<5>	AB1
GPU_MIOA_D<4>	P3	GPU_MIOB_D<6>	AC4
GPU_MIOA_D<5>	T3	GPU_MIOB_D<7>	AC1
GPU_MIOA_D<6>	T2	GPU_MIOB_D<8>	AC2
GPU_MIOA_D<7>	T1	GPU_MIOB_D<9>	AC3
GPU_MIOA_D<8>	U4	GPU_MIOB_D<10>	AE3
GPU_MIOA_D<9>	U1	GPU_MIOB_D<11>	AE2
GPU_MIOA_D<10>	U2	GPU_MIOB_D<12>	U6
GPU_MIOA_D<11>	U3	GPU_MIOB_D<13>	W6
GPU_MIOA_D<12>	R6	GPU_MIOB_D<14>	Y6
GPU_MIOA_D<13>	T6	GPU_STRAP<0>	W5
GPU_MIOA_D<14>	N6	GPU_STRAP<1>	W7
GPU_MIOA_HSYNC	N3	GPU_STRAP<2>	V7
GPU_MIOA_VSYNC	L3	GPU_MIOB_HSYNC	W1
GPU_MIOB_CLKIN	AE1	GPU_MIOB_VSYNC	W2
GPU_MIOB_CLKOUT_P	V4	GPU_THERMD_P	B5
GPU_MIOB_CLKOUT_N	W4	GPU_THERMD_N	B4
GPU_MIOB_CTL3	W3	TP_GPU_PGOOD_OUT_L	C5
GPU_MIOB_DE	Y5		
GPU_MIOB_D<0>	Y1		
GPU_MIOB_D<1>	Y2		
GPU_MIOB_D<2>	Y3		
GPU_MIOB_D<3>	AB3		
GPU_MIOB_D<4>	AB2		
GPU_MIOB_D<5>	AB1		
GPU_MIOB_D<6>	AC4		
GPU_MIOB_D<7>	AC1		
GPU_MIOB_D<8>	AC2		
GPU_MIOB_D<9>	AC3		
GPU_MIOB_D<10>	AE3		
GPU_MIOB_D<11>	AE2		
GPU_MIOB_D<12>	U6		
GPU_MIOB_D<13>	W6		
GPU_MIOB_D<14>	Y6		
GPU_STRAP<0>	W5		
GPU_STRAP<1>	W7		
GPU_STRAP<2>	V7		
GPU_MIOB_HSYNC	W1		
GPU_MIOB_VSYNC	W2		
GPU_THERMD_P	B5		
GPU_THERMD_N	B4		
TP_GPU_PGOOD_OUT_L	C5		

NV G96 GPIO/MIO/Misc
 SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

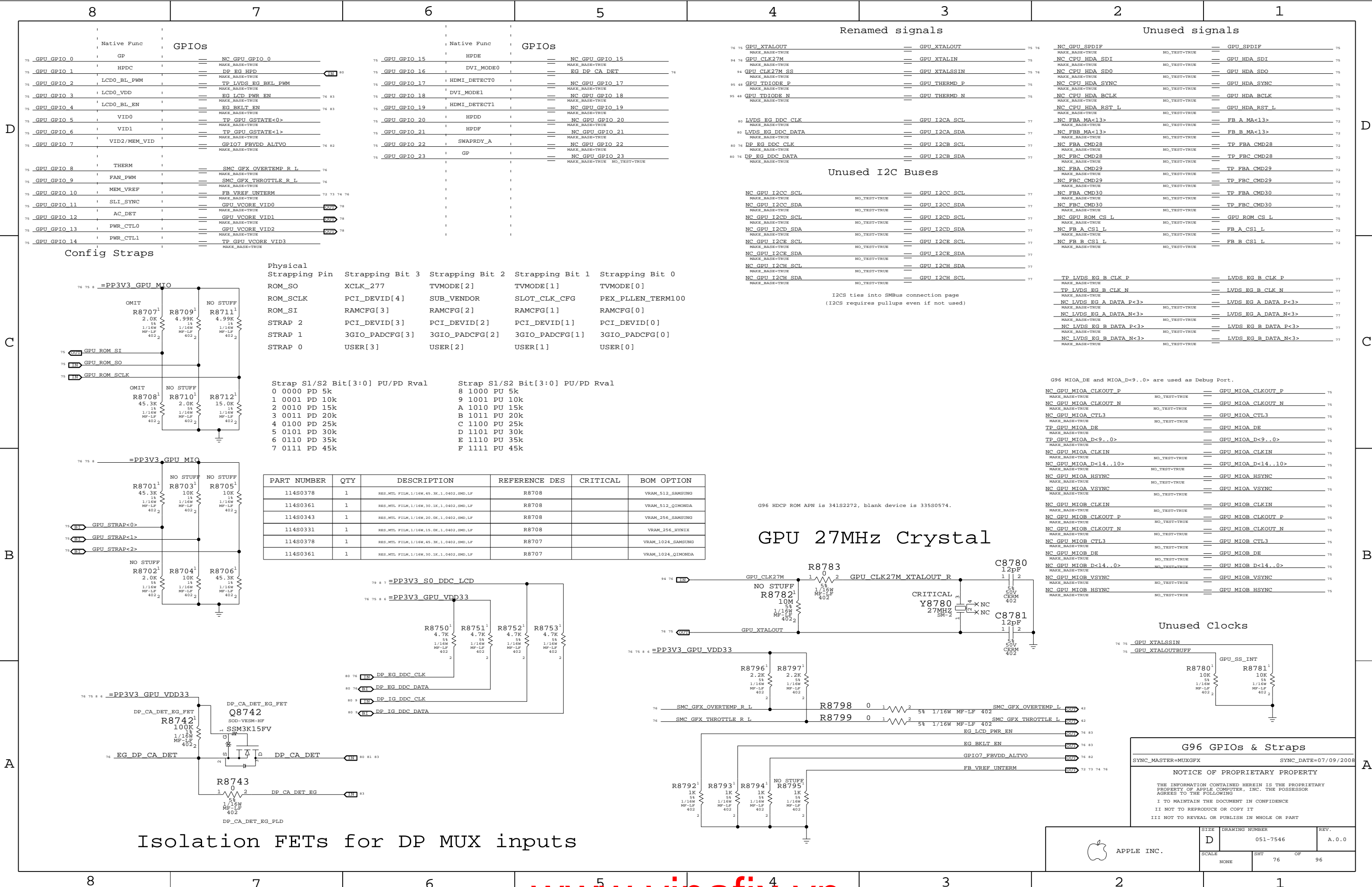
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Renamed signals Unused signals

75 GPU_GPIO_0	GP	NC_GPU_GPIO_0	GPU_SPDIF	GPU_SPDIF
75 GPU_GPIO_1	HPDC	DP_EG_HPD	GPU_HDA_SDI	GPU_HDA_SDI
75 GPU_GPIO_2	LCD0_BL_PWM	TP_LVDS_EG_BKL_PWM	GPU_HDA_SDO	GPU_HDA_SDO
75 GPU_GPIO_3	LCD0_VDD	EG_LCD_PWR_EN	GPU_HDA_SYNC	GPU_HDA_SYNC
75 GPU_GPIO_4	LCD0_BL_EN	EG_BKLT_EN	GPU_HDA_BCLK	GPU_HDA_BCLK
75 GPU_GPIO_5	VID0	TP_GPU_GSTATE<0>	GPU_HDA_RST_L	GPU_HDA_RST_L
75 GPU_GPIO_6	VID1	TP_GPU_GSTATE<1>	NC_FBA_MA<13>	FB_A_MA<13>
75 GPU_GPIO_7	VID2/MEM_VID	GPIO7_FBVDD_ALTVO	NC_FBA_MA<13>	FB_B_MA<13>
75 GPU_GPIO_8	THERM	SMC_GFX_OVERTEMP_R_L	NC_FBA_CMD28	TP_FBA_CMD28
75 GPU_GPIO_9	FAN_PWM	SMC_GFX_THROTTLE_R_L	NC_FBC_CMD28	TP_FBC_CMD28
75 GPU_GPIO_10	MEM_VREF	FB_VREF_UNTERM	NC_FBA_CMD29	TP_FBA_CMD29
75 GPU_GPIO_11	SLI_SYNC	GPU_VCORE_VID0	NC_FBC_CMD29	TP_FBC_CMD29
75 GPU_GPIO_12	AC_DET	GPU_VCORE_VID1	NC_FBA_CMD30	TP_FBA_CMD30
75 GPU_GPIO_13	PWR_CTL0	GPU_VCORE_VID2	NC_FBC_CMD30	TP_FBC_CMD30
75 GPU_GPIO_14	PWR_CTL1	TP_GPU_VCORE_VID3	NC_GPU_ROM_CS_L	GPU_ROM_CS_L

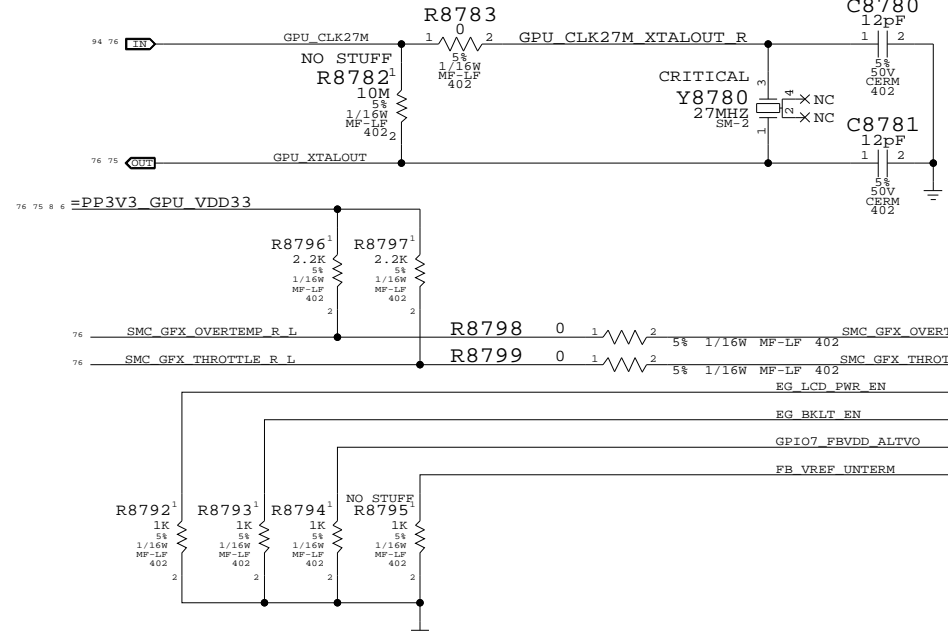
Config Straps

Strapping Pin	Strapping Bit 3	Strapping Bit 2	Strapping Bit 1	Strapping Bit 0
ROM_SO	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLLEN_TERM100
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP 1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP 0	USER[3]	USER[2]	USER[1]	USER[0]

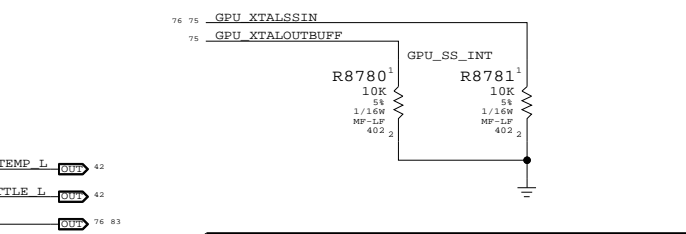
Strap S1/S2 Bit[3:0] PU/PD Rval	Strap S1/S2 Bit[3:0] PU/PD Rval
0 0000 PD 5k	8 1000 PU 5k
1 0001 PD 10k	9 1001 PU 10k
2 0010 PD 15k	A 1010 PU 15k
3 0011 PD 20k	B 1011 PU 20k
4 0100 PD 25k	C 1100 PU 25k
5 0101 PD 30k	D 1101 PU 30k
6 0110 PD 35k	E 1110 PU 35k
7 0111 PD 45k	F 1111 PU 45k

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0378	1	RES.MTL FILM,1/16W,45.3K,1.0402,SMD,LF	R8708		VRAM_512_SAMSUNG
114S0361	1	RES.MTL FILM,1/16W,30.1K,1.0402,SMD,LF	R8708		VRAM_512_QIMONDA
114S0343	1	RES.MTL FILM,1/16W,20.0K,1.0402,SMD,LF	R8708		VRAM_256_SAMSUNG
114S0331	1	RES.MTL FILM,1/16W,15.0K,1.0402,SMD,LF	R8708		VRAM_256_HYNIX
114S0378	1	RES.MTL FILM,1/16W,45.3K,1.0402,SMD,LF	R8707		VRAM_1024_SAMSUNG
114S0361	1	RES.MTL FILM,1/16W,30.1K,1.0402,SMD,LF	R8707		VRAM_1024_QIMONDA

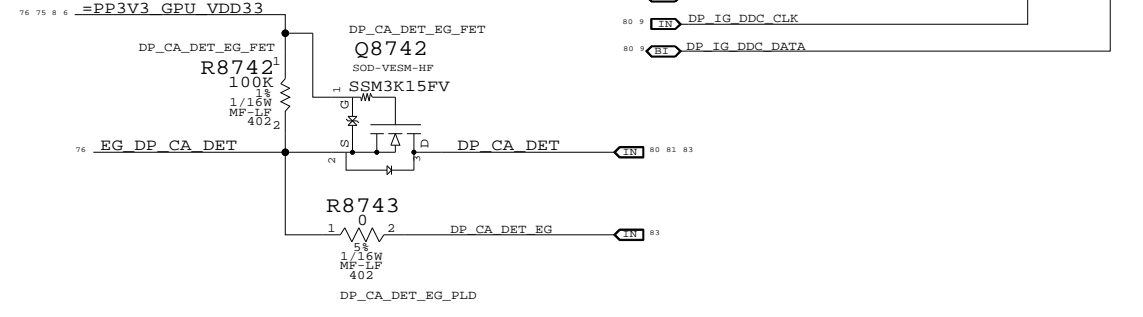
GPU 27MHz Crystal



Unused Clocks



Isolation FETs for DP MUX inputs



G96 GPIOs & Straps
 SYNC_MASTER=MUXGFX SYNC_DATE=07/09/2008
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	D	051-7546	A.0.0
SCALE	NONE	SHT	76 OF 96

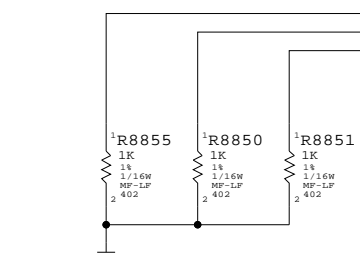
Page Notes

Power aliases required by this page:
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 - =PP3V3_GPU_IPFCD_IOVDD

Signal aliases required by this page:
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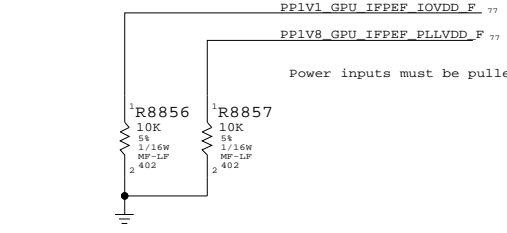
BOM options provided by this page:
 (NONE)

Sum of peak currents: 240mA
 =PP1V8_GPU_IPFX



GPU_IPFEF_RSET 77
 GPU_IPFCD_RSET 77
 GPU_IPFAB_RSET 77

=PP1V1_GPU_IPFCD_IOVDD



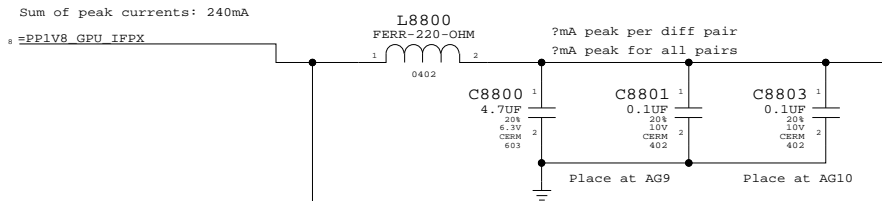
Power inputs must be pulled down if not used

=PP1V1_GPU_IPFCD_IOVDD

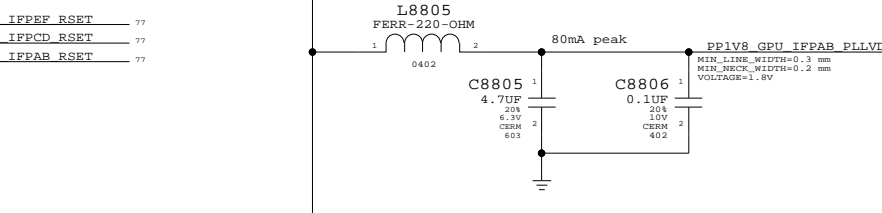
=PP1V8_GPU_IPFEF_PLLVDD_F

PP1V1_GPU_IPFEF_IOVDD_F 77

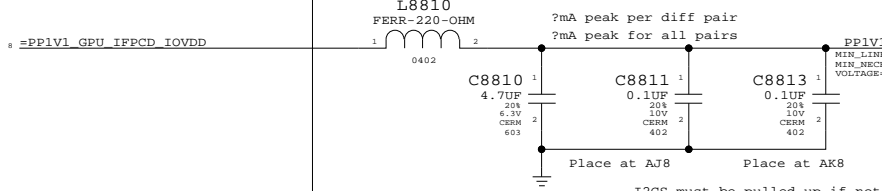
PP1V8_GPU_IPFEF_PLLVDD_F 77



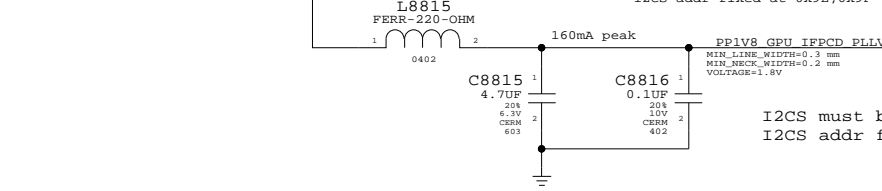
PP1V8_GPU_IPFAB_IOVDD_F
 MIN_LINE_WIDTH=0.4 mm
 MIN_NECK_WIDTH=0.2 mm
 VOLTAGE=1.8V



PP1V8_GPU_IPFAB_PLLVDD_F
 MIN_LINE_WIDTH=0.4 mm
 MIN_NECK_WIDTH=0.2 mm
 VOLTAGE=1.8V



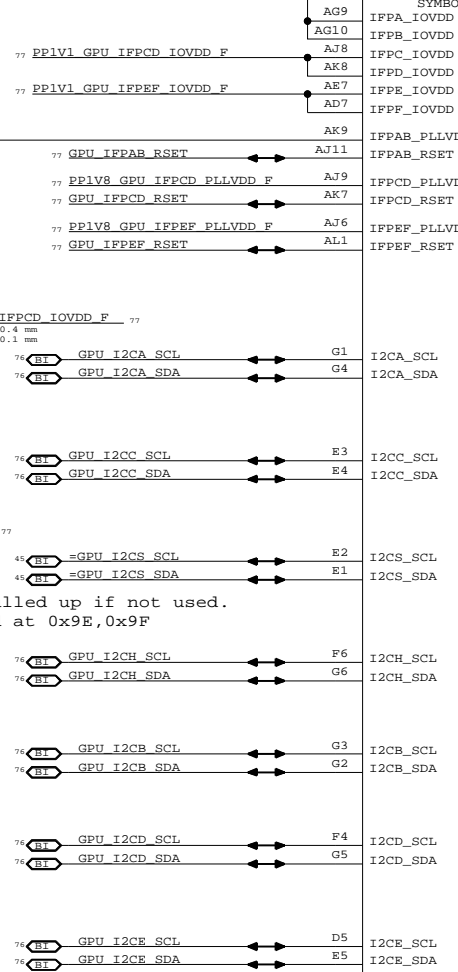
PP1V1_GPU_IPFCD_IOVDD_F 77
 MIN_LINE_WIDTH=0.4 mm
 MIN_NECK_WIDTH=0.2 mm
 VOLTAGE=1.1V



PP1V8_GPU_IPFCD_PLLVDD_F 77
 MIN_LINE_WIDTH=0.4 mm
 MIN_NECK_WIDTH=0.2 mm
 VOLTAGE=1.8V

I2CS must be pulled up if not used.
 I2CS addr fixed at 0x9E,0x9F

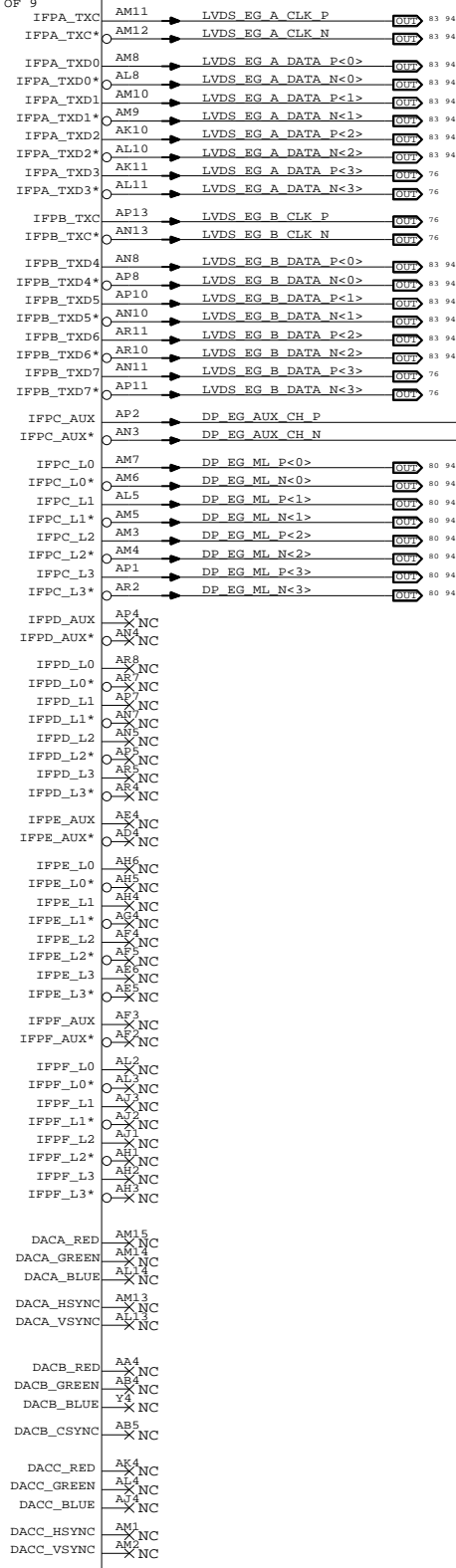
I2CS must be pulled up if not used.
 I2CS addr fixed at 0x9E,0x9F



OMIT

U8000
 NB9P-GS
 BGA

SYMBOL 5 OF 9



NV G96 Video Interfaces

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

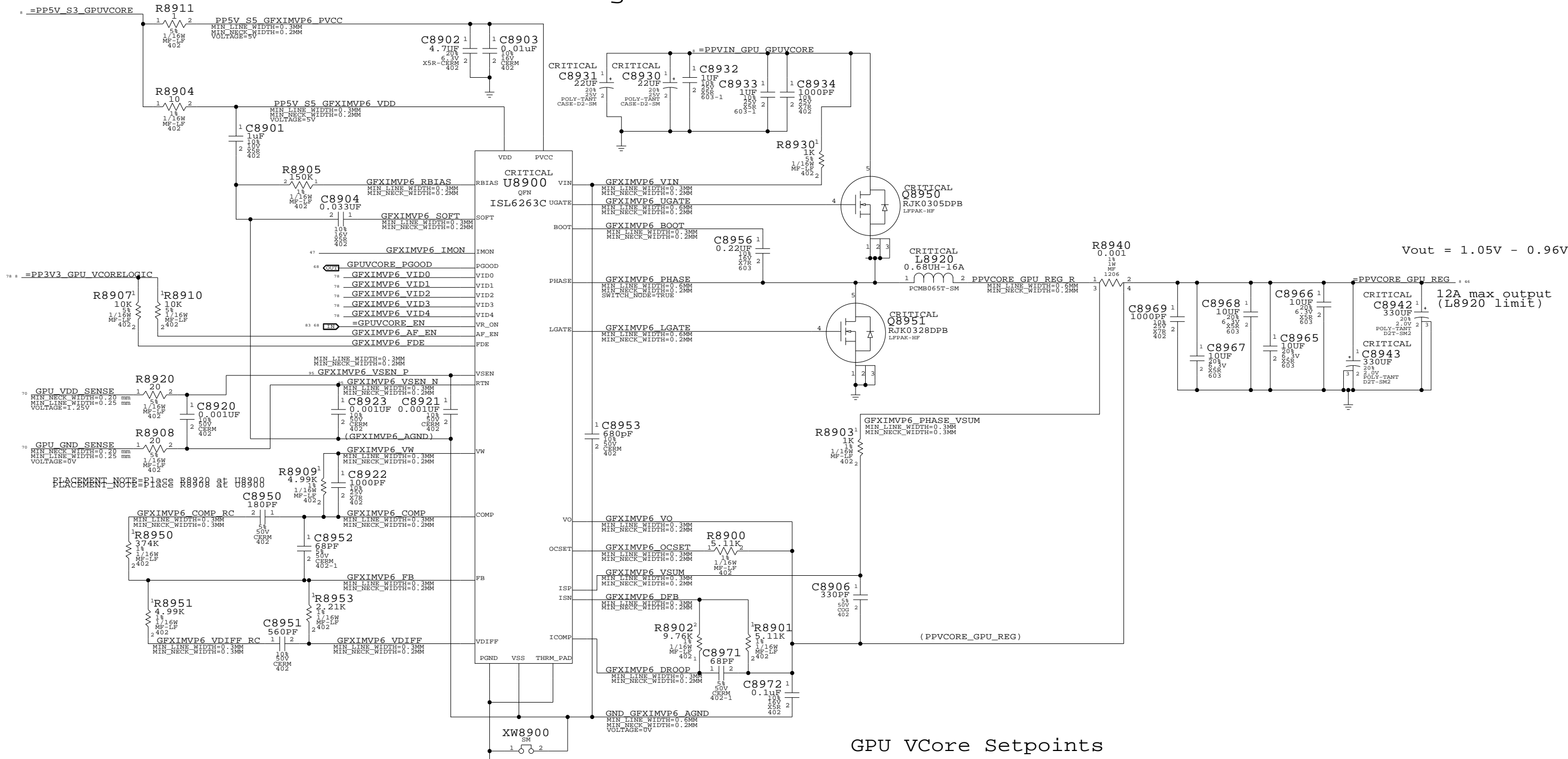
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D	051-7546	A.0.0
SCALE	SHT	OF
NONE	77	96

GPU VCore Regulator



GPU VCore Setpoints

VID3	VID2	VID1	VID0	Voltage	Max Batt	Balanced	Max perf
1	1	1	1	0.90125V	M98		-
1	1	1	0	0.92700V	-	M98	-
1	0	1	1	1.00425V	-	-	M98

Other VID states may not be valid

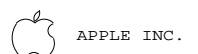
M98 Default Vcore Setpoints

BOM GROUP	BOM OPTIONS
GPUVID_0P90V	GPUVID2_1, GPUVID1_1, GPUVID0_1
GPUVID_1P00V	GPUVID2_0, GPUVID1_1, GPUVID0_1

GPU (G84M) Core Supply

SYNC_MASTER=M87_MLB SYNC_DATE=10/17/2007

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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	78	96

D

D

C

C

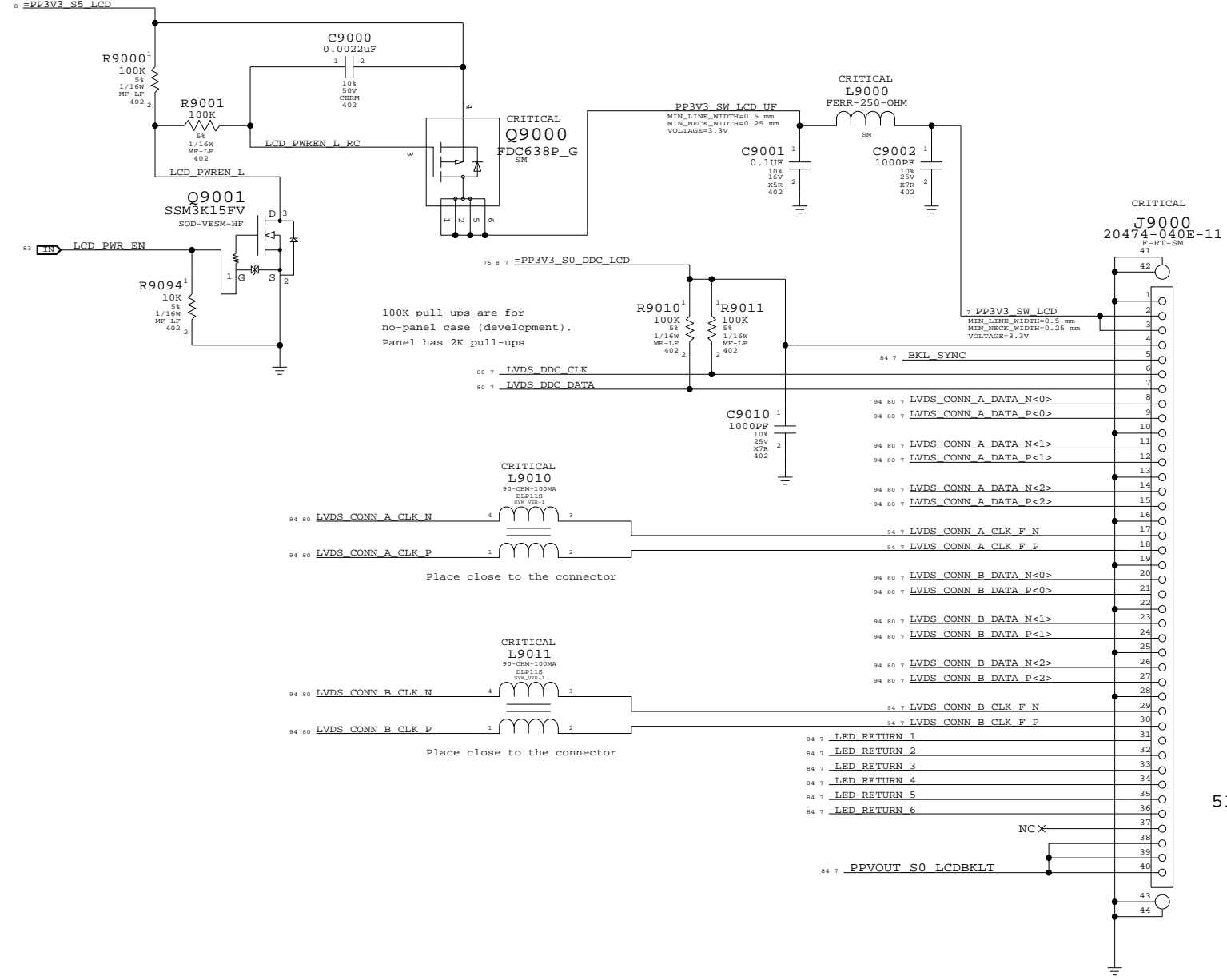
B

B

A

A

LCD (LVDS) INTERFACE



518S0651

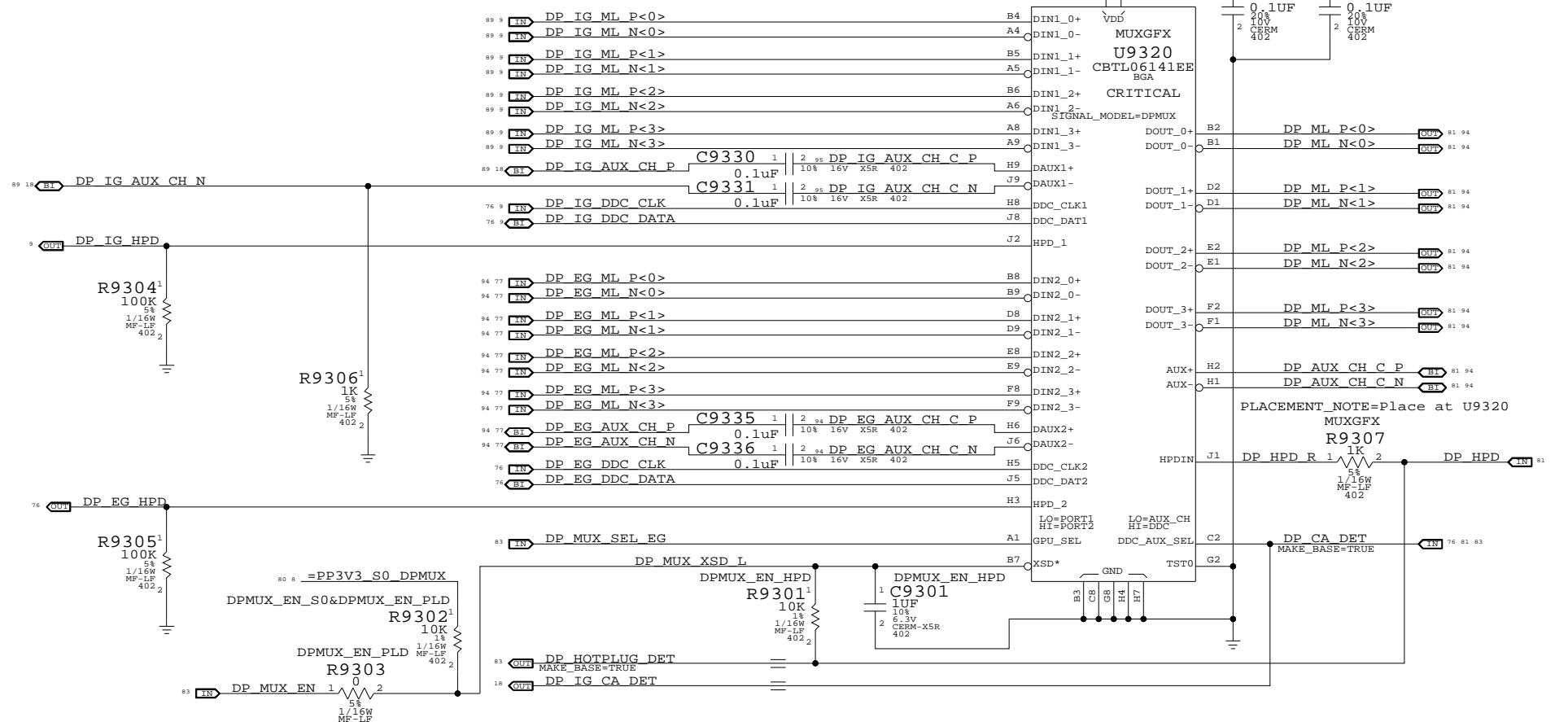
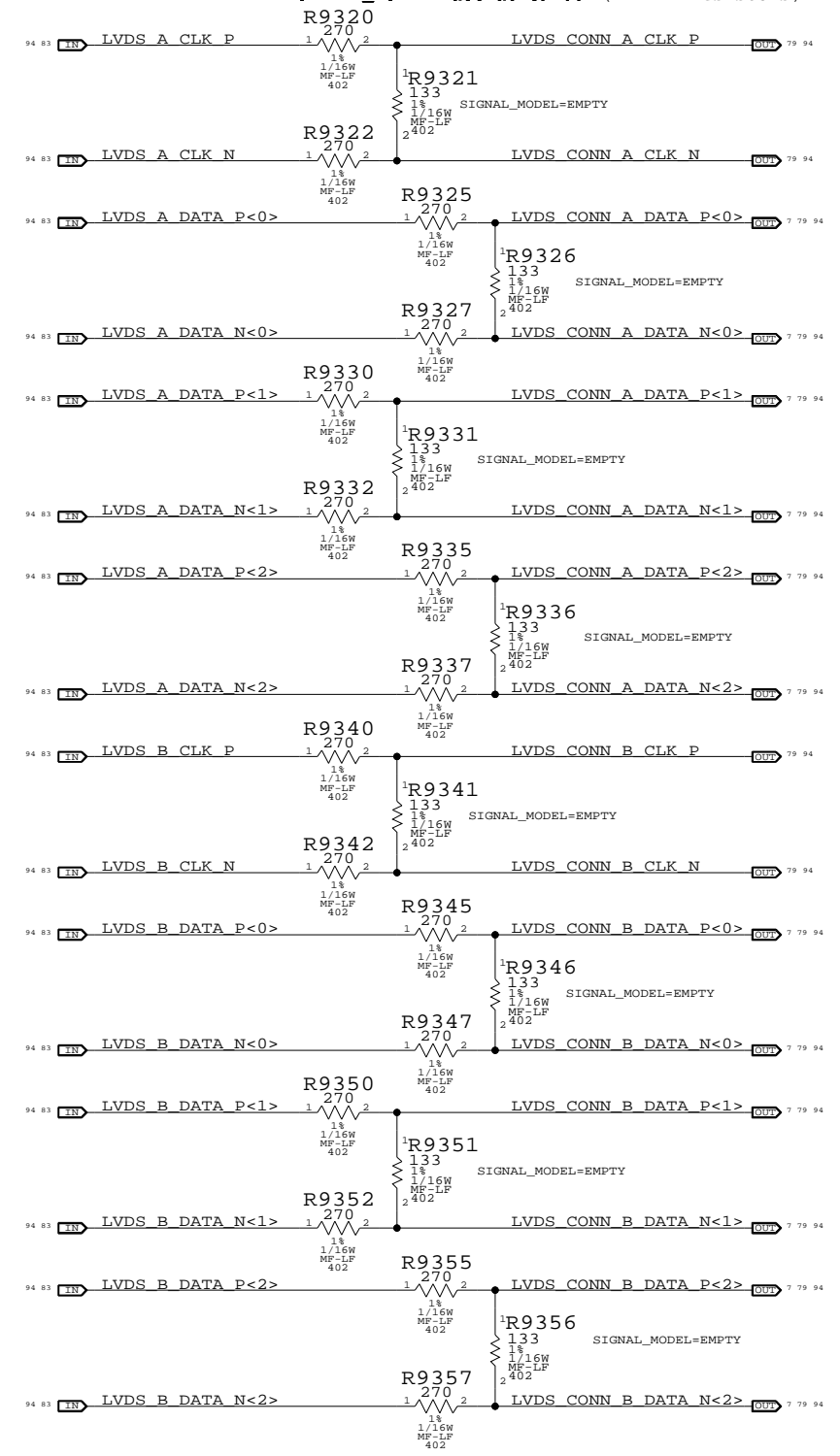
LVDS Display Connector
 SYNC_MASTER=MUXGFX SYNC_DATE=02/25/2008
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT 79 OF 96		
NONE			

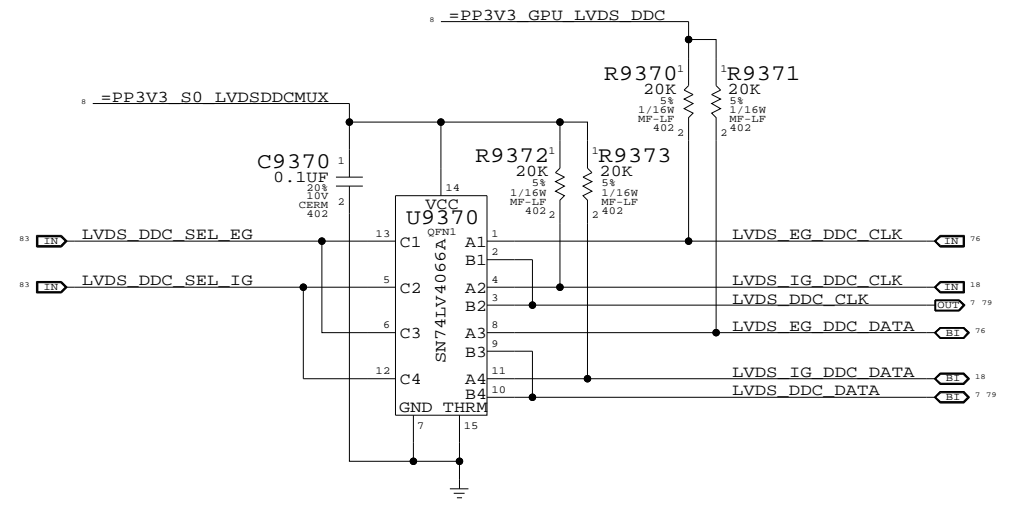
DisplayPort Mux

LVDS Transmitter Termination

All emulated LVDS outputs require this termination
PLACEMENT NOTE=Place at U9200 (All 24 resistors)



LVDS DDC MUX



Muxed Graphics Support

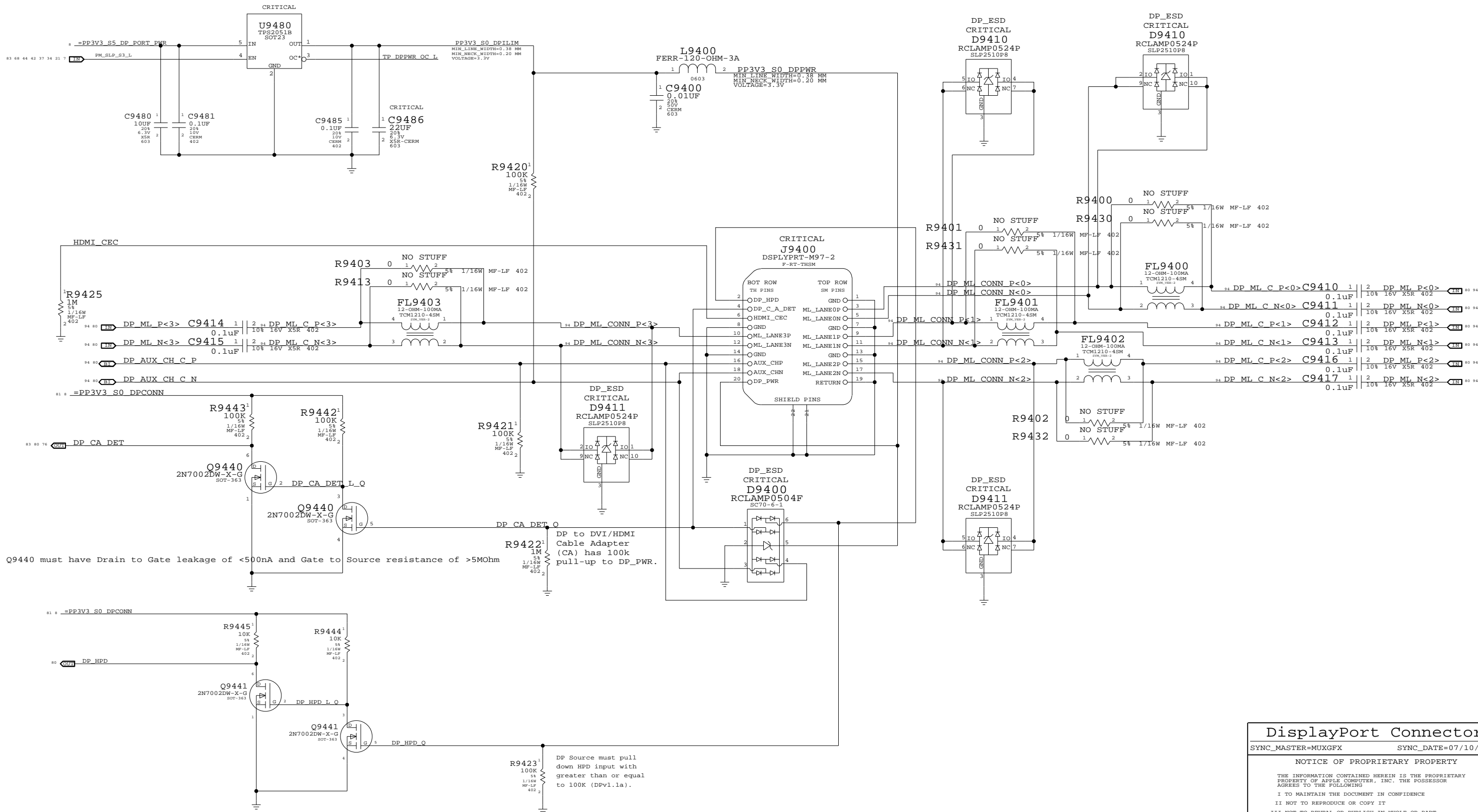
SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	80		

Port Power Switch



DisplayPort Connector

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

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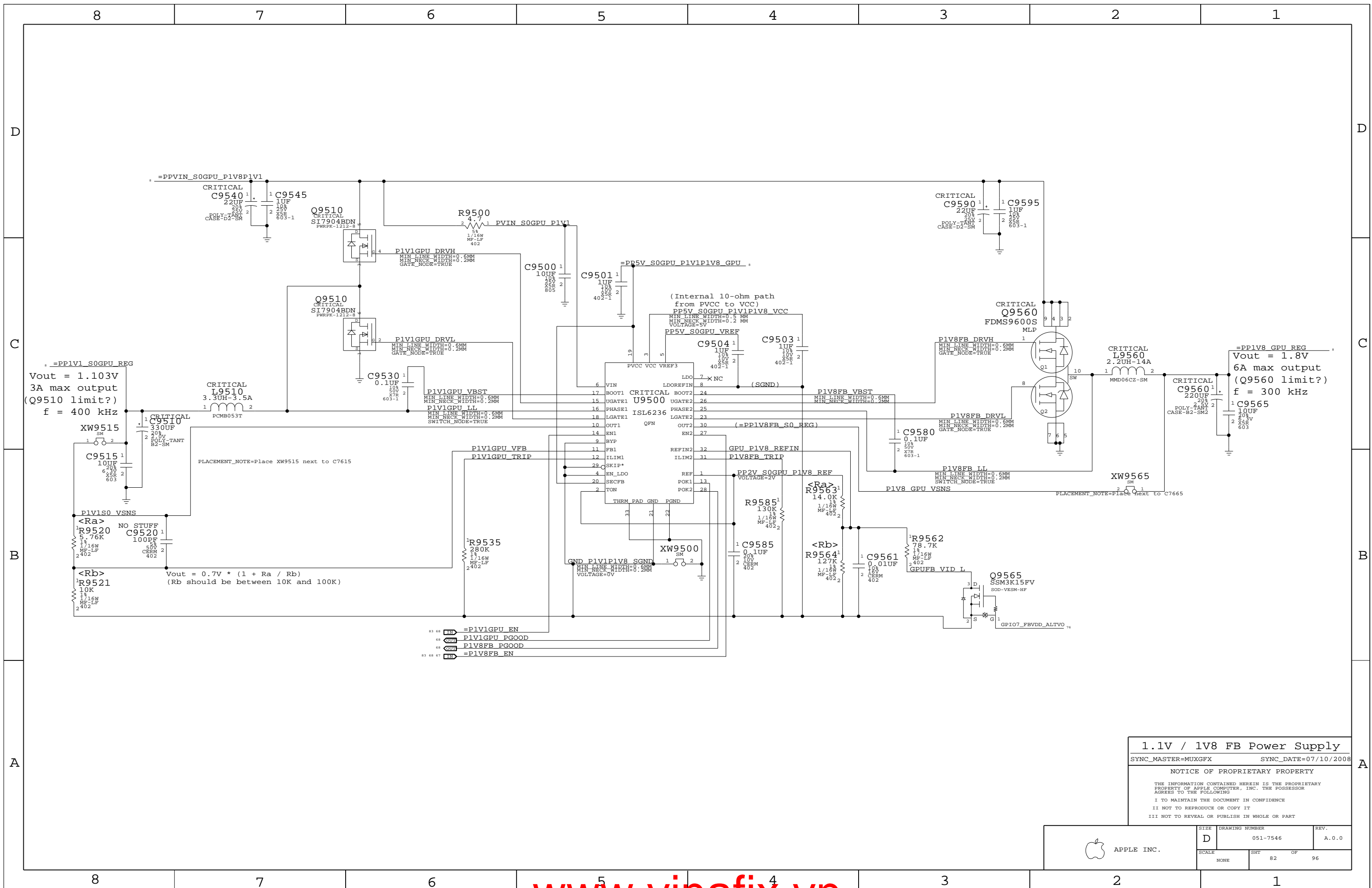
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APPLE INC.	SIZE D	DRAWING NUMBER 051-7546	REV. A.0.0
	SCALE NONE	SHEET 81	OF 96



1.1V / 1V8 FB Power Supply

SYNC_MASTER=MUXGFX SYNC_DATE=07/10/2008

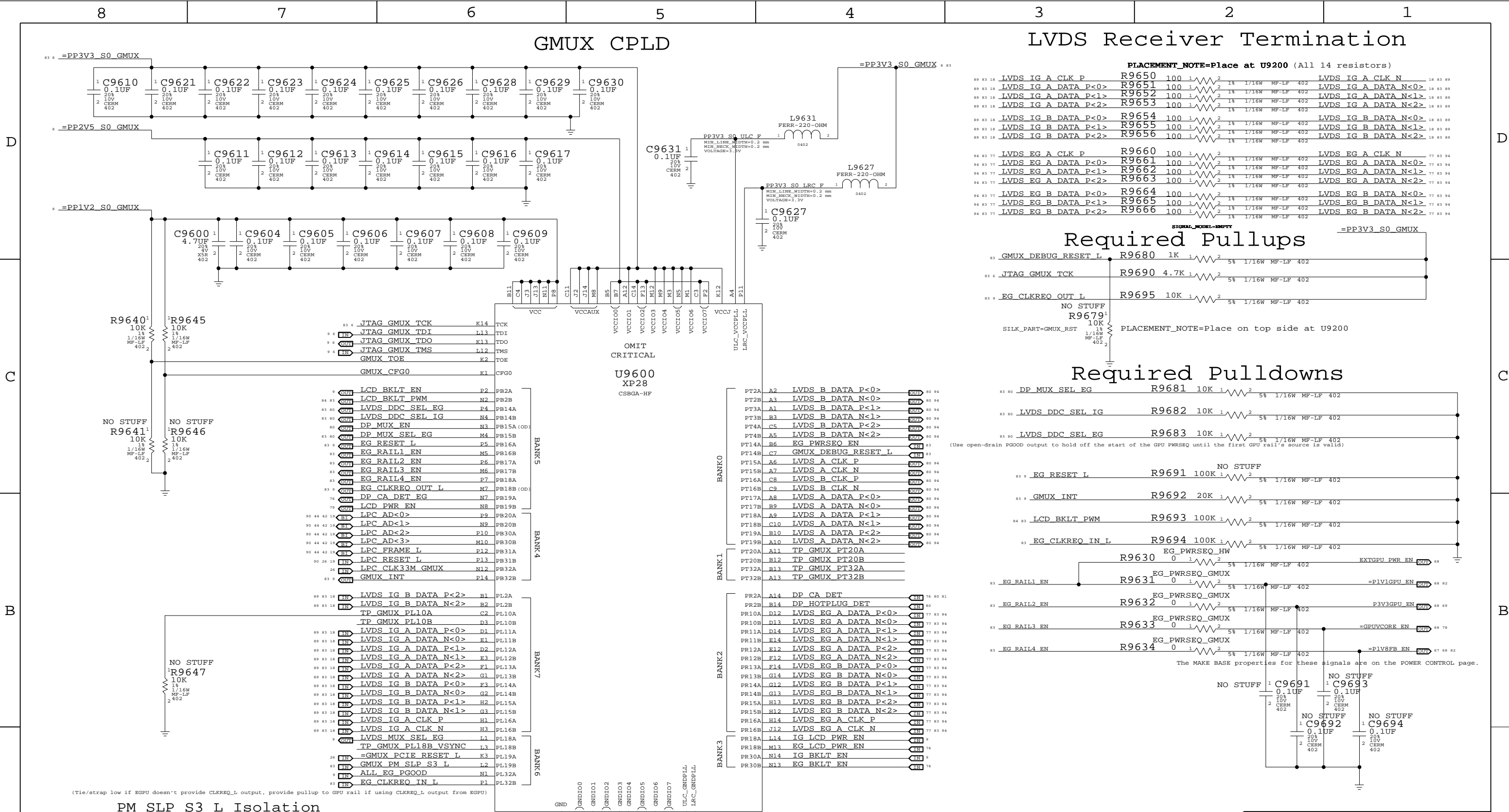
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	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	96
NONE	82		

GMUX CPLD

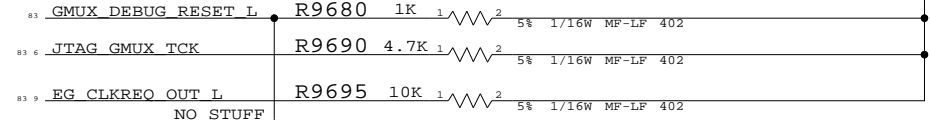
LVDS Receiver Termination



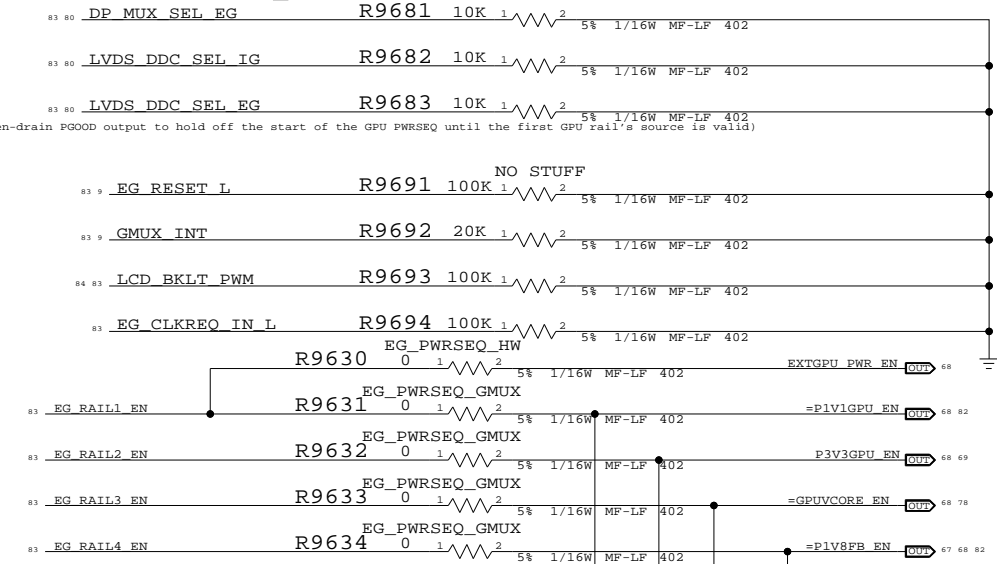
PLACEMENT_NOTE=Place at U9200 (All 14 resistors)

LVDS IG A CLK P	R9650	100	1	1/16W MF-LF 402	LVDS IG A CLK N	R9650	100	1	1/16W MF-LF 402
LVDS IG A DATA P<0>	R9651	100	1	1/16W MF-LF 402	LVDS IG A DATA N<0>	R9651	100	1	1/16W MF-LF 402
LVDS IG A DATA P<1>	R9652	100	1	1/16W MF-LF 402	LVDS IG A DATA N<1>	R9652	100	1	1/16W MF-LF 402
LVDS IG A DATA P<2>	R9653	100	1	1/16W MF-LF 402	LVDS IG A DATA N<2>	R9653	100	1	1/16W MF-LF 402
LVDS IG B DATA P<0>	R9654	100	1	1/16W MF-LF 402	LVDS IG B DATA N<0>	R9654	100	1	1/16W MF-LF 402
LVDS IG B DATA P<1>	R9655	100	1	1/16W MF-LF 402	LVDS IG B DATA N<1>	R9655	100	1	1/16W MF-LF 402
LVDS IG B DATA P<2>	R9656	100	1	1/16W MF-LF 402	LVDS IG B DATA N<2>	R9656	100	1	1/16W MF-LF 402
LVDS EG A CLK P	R9660	100	1	1/16W MF-LF 402	LVDS EG A CLK N	R9660	100	1	1/16W MF-LF 402
LVDS EG A DATA P<0>	R9661	100	1	1/16W MF-LF 402	LVDS EG A DATA N<0>	R9661	100	1	1/16W MF-LF 402
LVDS EG A DATA P<1>	R9662	100	1	1/16W MF-LF 402	LVDS EG A DATA N<1>	R9662	100	1	1/16W MF-LF 402
LVDS EG A DATA P<2>	R9663	100	1	1/16W MF-LF 402	LVDS EG A DATA N<2>	R9663	100	1	1/16W MF-LF 402
LVDS EG B DATA P<0>	R9664	100	1	1/16W MF-LF 402	LVDS EG B DATA N<0>	R9664	100	1	1/16W MF-LF 402
LVDS EG B DATA P<1>	R9665	100	1	1/16W MF-LF 402	LVDS EG B DATA N<1>	R9665	100	1	1/16W MF-LF 402
LVDS EG B DATA P<2>	R9666	100	1	1/16W MF-LF 402	LVDS EG B DATA N<2>	R9666	100	1	1/16W MF-LF 402

Required Pullups

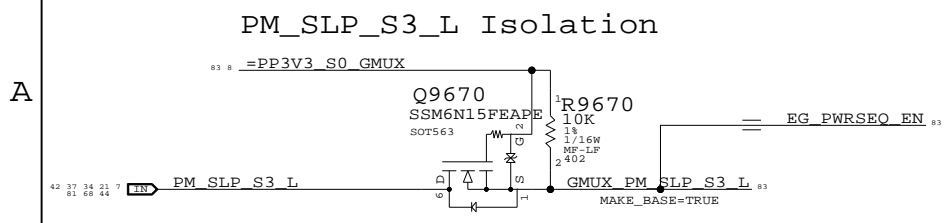
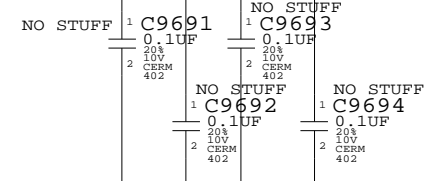


Required Pulldowns



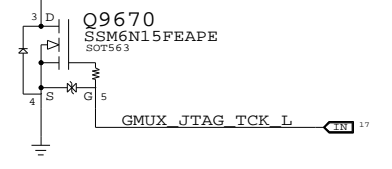
(Use open-drain PGOOD output to hold off the start of the GPU PWRSEQ until the first GPU rail's source is valid)

The MAKE_BASE properties for these signals are on the POWER CONTROL page.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
336S0027	1	IC,XP2-8,-HF,CPLD,BLANK	U9600	CRITICAL	GMUX_8K_BLANK
341S2350	1	IC,CPLD,LATTICE,132CSBGA,M98	U9600	CRITICAL	GMUX_PROG

GMUX_JTAG_TCK Inversion



Graphics MUX (GMUX)

SYNC_MASTER=MUXGFx SYNC_DATE=07/10/2008

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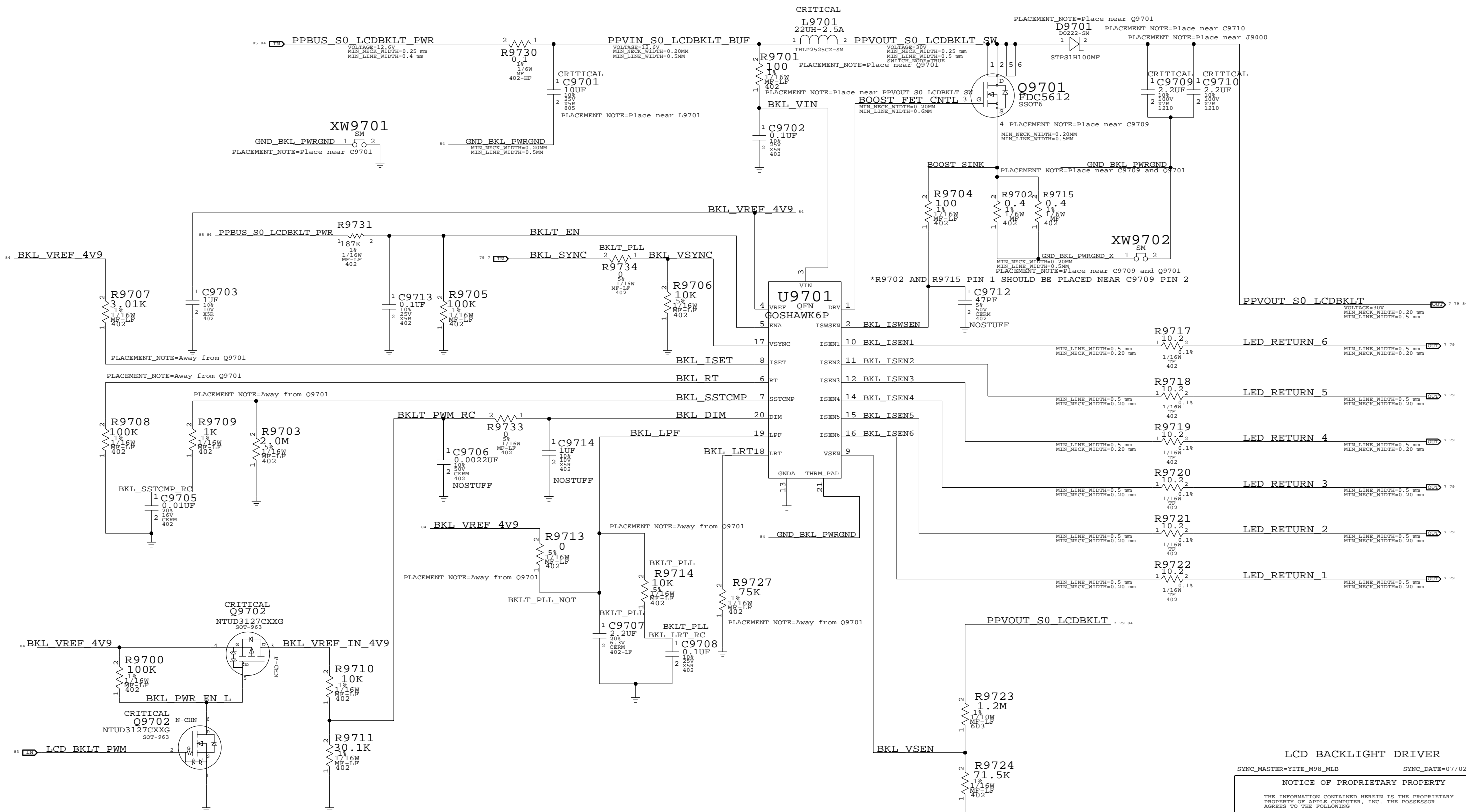
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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHEET	OF	
NONE	83	96	

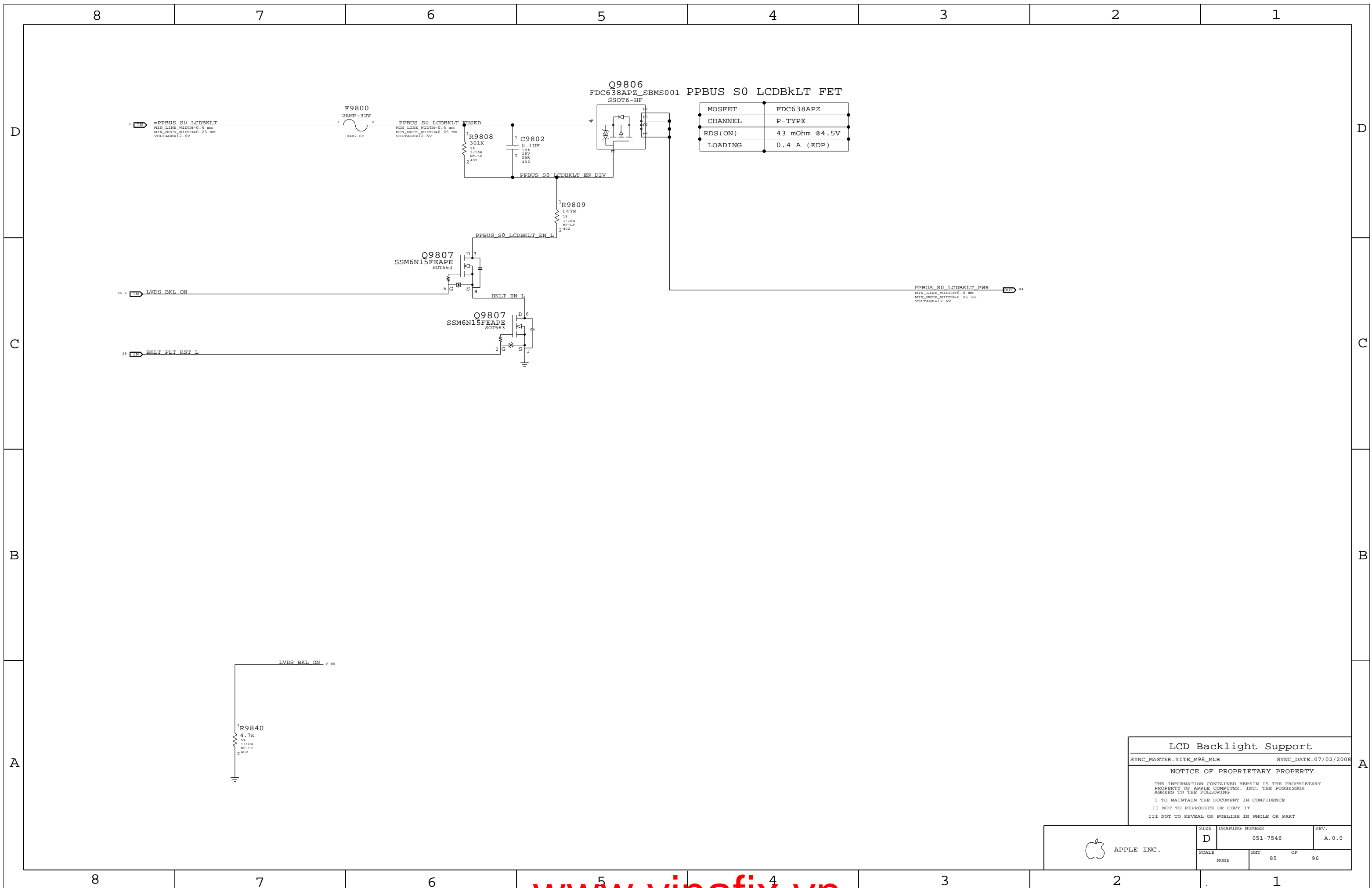
*Q9701, D9701, C9709, C9710, L9701, R9702, AND R9715 SHOULD ALL BE PLACED NEAR EACHOTHER.
 *BOOST_FET_CNTL AND PPVOUT_S0_LCDBKLT_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.



LCD BACKLIGHT DRIVER
 SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008
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*R9707, R9708, R9709, R9713, R9714, R9727, AND R9729 SHOULD AWAY FROM BOOST CIRCUIT

APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	REV.
NONE	84	96	



MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS (ON)	43 mOhm @4.5V
LOADING	0.4 A (EDP)

LCD Backlight Support

SYNC_MASTER=YITE_M98_MLB SYNC_DATE=07/02/2008

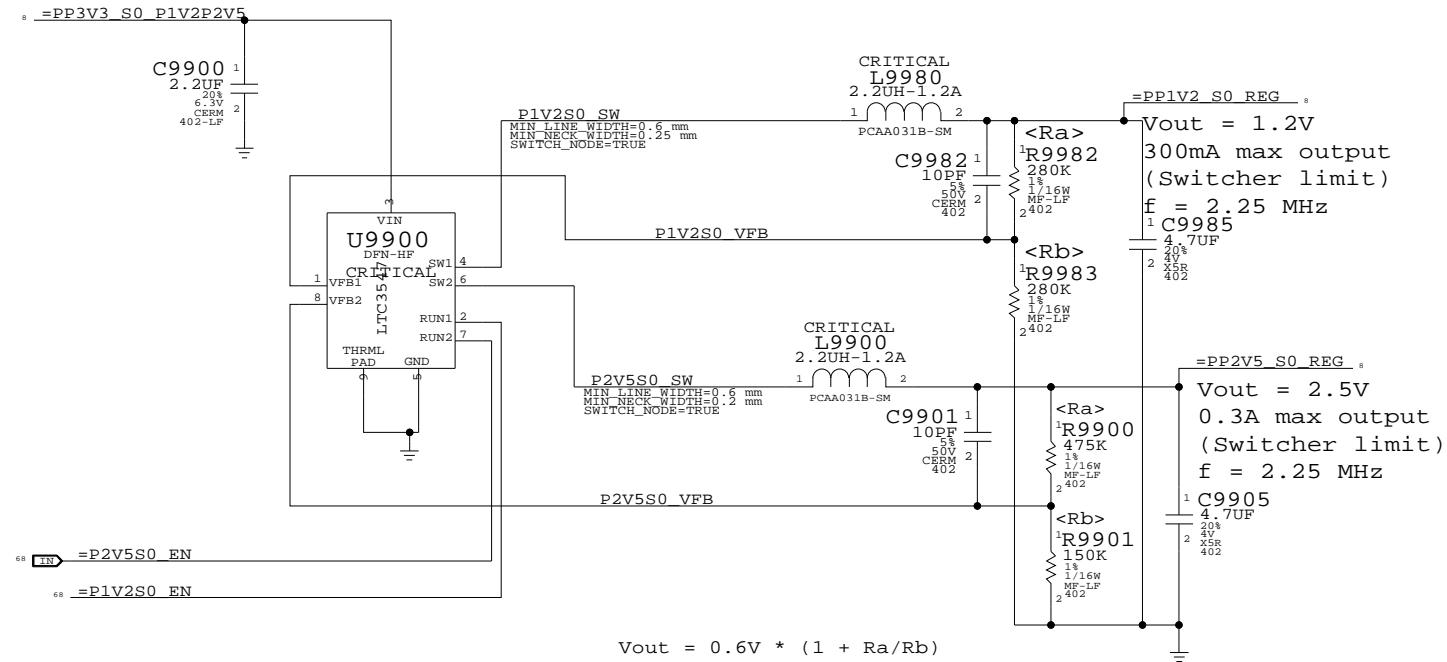
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 APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT	OF	
NONE	85	96	

2.5V/1.2V S3 Switcher



Misc Power Supplies

SYNC_MASTER=MUXGFX SYNC_DATE=02/01/2008

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	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	SHT		OF
NONE	86		96

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
FSB_DSTB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FSB_DATA	*	=2x_DIELECTRIC	?	FSB_DATA	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_DSTB	*	=3x_DIELECTRIC	?	FSB_DSTB	TOP,BOTTOM	=5x_DIELECTRIC	?
FSB_ADDR	*	=STANDARD	?	FSB_ADDR	TOP,BOTTOM	=3x_DIELECTRIC	?
FSB_ADSTB	*	=2x_DIELECTRIC	?	FSB_ADSTB	TOP,BOTTOM	=4x_DIELECTRIC	?
FSB_1X	*	=STANDARD	?	FSB_1X	TOP,BOTTOM	=3x_DIELECTRIC	?

All 4x/2x/1x FSB signals with impedance requirements are 50-ohm single-ended.

FSB 4X signals / groups shown in signal table on right.

Signals within each 4x group should be matched within 5 ps of strobe.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/- 300 ps.

Spacing is 2x dielectric between DATA#, DINV# signals, with 3x dielectric spacing to the DSTB#s.

DSTB# complementary pairs are spaced normally and are NOT routed as differential pairs.

FSB 2X signals / groups shown in signal table on right.

Signals within each 2x group should be matched within 20 ps. ADTSTB#s should be matched +/- 300 ps.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 1X signals shown in signal table on right.

Signals within each 1x group should be matched to CPU clock, +0/-1000 mils.

Design Guide recommends each strobe/signal group is routed on the same layer.

Intel Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.5 (#22294), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?	CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_8MIL	*	8 MIL	?				
CPU_COMP	*	25 MIL	?				
CPU_GTLREF	*	25 MIL	?				
CPU_ITP	*	=2:1_SPACING	?				
CPU_VCCSENSE	*	25 MIL	?				

SR DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.

Some signals require 27.4-ohm single-ended impedance.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

MCP FSB COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_FSB_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Clock Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_FSB	*	=3x_DIELECTRIC	?	CLK_FSB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		PROPERTY	VALUE	LAYER
	PHYSICAL	SPACING			
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB D L<15..0>	7	10 14
FSB_DATA_GROUP0	FSB_50S	FSB_DATA	FSB DINV L<0>	7	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<0>	7	10 14
FSB_DSTB0	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<0>	7	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB D L<31..16>	7	10 14
FSB_DATA_GROUP1	FSB_50S	FSB_DATA	FSB DINV L<1>	7	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<1>	7	10 14
FSB_DSTB1	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<1>	7	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB D L<47..32>	7	10 14
FSB_DATA_GROUP2	FSB_50S	FSB_DATA	FSB DINV L<2>	7	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<2>	7	10 14
FSB_DSTB2	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<2>	7	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB D L<63..48>	7	10 14
FSB_DATA_GROUP3	FSB_50S	FSB_DATA	FSB DINV L<3>	7	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L P<3>	7	10 14
FSB_DSTB3	FSB_DSTB_50S	FSB_DSTB	FSB DSTB L N<3>	7	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB A L<16..3>	7	10 14
FSB_ADDR_GROUP0	FSB_50S	FSB_ADDR	FSB REQ L<4..0>	7	10 14
FSB_ADSTB0	FSB_50S	FSB_ADSTB	FSB ADSTB L<0>	7	10 14
FSB_ADDR_GROUP1	FSB_50S	FSB_ADDR	FSB A L<35..17>	7	10 14
FSB_ADSTB1	FSB_50S	FSB_ADSTB	FSB ADSTB L<1>	7	10 14
FSB_1X	FSB_50S	FSB_1X	FSB ADS L	7	10 14
FSB_BREQ0_L	FSB_50S	FSB_1X	FSB_BREQ0_L	9	10 14
FSB_BREQ1_L	FSB_50S	FSB_1X	FSB_BREQ1_L	14	
FSB_1X	FSB_50S	FSB_1X	FSB BNR L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB BPRI L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB DBSY L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB DEFER L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB DRDY L	10	14
FSB_1X	FSB_50S	FSB_1X	FSB HIT L	7	10 14
FSB_1X	FSB_50S	FSB_1X	FSB HITM L	7	10 14
FSB_1X	FSB_50S	FSB_1X	FSB LOCK L	7	10 14
FSB_CPURST_L	FSB_50S	FSB_1X	FSB CPURST L	9	10 13 14
FSB_1X	FSB_50S	FSB_1X	FSB RS L<2..0>	10	14
FSB_1X	FSB_50S	FSB_1X	FSB TRDY L	10	14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU A20M L	10	14
CPU_BSEL	CPU_50S	CPU_AGTL	CPU BSEL<2..0>	9	10
CPU_FERR_L	CPU_50S	CPU_8MIL	CPU FERR L	10	14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU IGNE L	10	14
CPU_INIT_L	CPU_50S	CPU_AGTL	CPU INIT L	10	14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU INTR	9	10 14
CPU_ASYNC_R	CPU_50S	CPU_AGTL	CPU NMI	9	10 14
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU PROCHOT L	10	14 43 62
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU PWRGD	10	13 14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU SMI L	10	14
CPU_ASYNC	CPU_50S	CPU_AGTL	CPU STPCLK L	10	14
PM_THERMTRIP_L	CPU_50S	CPU_8MIL	PM_THERMTRIP L	10	14 43
FSB_CPUSLP_L	CPU_50S	CPU_AGTL	FSB CPUSLP L	10	14
CPU_PROM_SR	CPU_50S	CPU_AGTL	CPU DPSLP L	10	14
CPU_DPRSTP_L	CPU_50S	CPU_AGTL	CPU DPRSTP L	9	10 14 62
CPU_ASYNC	CPU_50S	CPU_AGTL	FSB DPWR L	10	14
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP VDD	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP BCLK VML COMP GND	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP VCC	14	
MCP_CPU_COMP	MCP_50S	MCP_FSB_COMP	MCP CPU COMP GND	14	
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU P	10	14
FSB_CLK_CPU	CLK_FSB_100D	CLK_FSB	FSB CLK CPU N	10	14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP P	13	14
FSB_CLK_ITP	CLK_FSB_100D	CLK_FSB	FSB CLK ITP N	13	14
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP P	14	
FSB_CLK_MCP	CLK_FSB_100D	CLK_FSB	FSB CLK MCP N	14	
CPU_IERR_L	CPU_50S		CPU IERR L	10	
PM_DPRSLEVR	CPU_50S	CPU_AGTL	PM_DPRSLEVR	21	62
(See above)	CPU_50S	CPU_AGTL	IMVP DPRSLEVR	62	
CPU_GTLREF	CPU_50S	CPU_GTLREF	CPU GTLREF	10	27
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<3>	10	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10	
CPU_COMP	CPU_50S	CPU_COMP	CPU_COMP<1>	10	
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10	
XDP_TDI	CPU_50S	CPU_ITP	XDP TDI	6	10 13
XDP_TDO	CPU_50S	CPU_ITP	XDP TDO	6	10
XDP_TMS	CPU_50S	CPU_ITP	XDP TMS	6	10 13
XDP_TCK	CPU_50S	CPU_ITP	XDP TCK	6	10 13
XDP_TRST_L	CPU_50S	CPU_ITP	XDP TRST L	6	10 13
XDP_BPM_L	CPU_50S	CPU_ITP	XDP BPM L<4..0>	10	13
XDP_BPM_L5	CPU_50S	CPU_ITP	XDP BPM L<5>	10	13
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP CPURST L	13	
	CPU_50S	CPU_8MIL	CPU VID<6..0>	9	11
	CPU_50S	CPU_8MIL	IMVP6 VID<6..0>	9	62
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE P	11	62
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU VCCSENSE N	11	62
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN P	62	
(CPU_VCCSENSE)	CPU_27P4S	CPU_VCCSENSE	IMVP6 VSEN N	62	

CPU/FSB Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	87	96

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_40S_VDD	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_70D_VDD	*	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=2:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MIL	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

Need to support MEM_*-style wildcards!

DDR2:

DQ signals should be matched within 20 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
 All DQS pairs should be matched within 100 ps of clocks.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.
 A/BA/cmd signals should be matched within 75 ps, no CLK matching requirement.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

DDR3:

DQ signals should be matched within 5 ps of associated DQS pair.
 DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps
 No DQS to clock matching requirement.
 CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.
 A/BA/cmd signals should be matched within 5 ps of CLK pairs.
 All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).
 DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3
 SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

MCP MEM COMP Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MEM_COMP	*	Y	7 MIL	7 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_MEM_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK P<5..0> 15 28
MEM_A_CLK	MEM_70D_VDD	MEM_CLK	MEM A CLK N<5..0> 15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CKE<3..0> 15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A CS L<3..0> 15 28
MEM_A_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM A ODT<3..0> 15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A A<14..0> 15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A BA<2..0> 15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A RAS L 15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A CAS L 15 28
MEM_A_CMD	MEM_40S_VDD	MEM_CMD	MEM A WE L 15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DQ<7..0> 15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DQ<15..8> 15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DQ<23..16> 15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DQ<31..24> 15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DQ<39..32> 15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DQ<47..40> 15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DQ<55..48> 15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DQ<63..56> 15 28
MEM_A_DQ_BYTE0	MEM_40S	MEM_DATA	MEM A DM<0> 15 28
MEM_A_DQ_BYTE1	MEM_40S	MEM_DATA	MEM A DM<1> 15 28
MEM_A_DQ_BYTE2	MEM_40S	MEM_DATA	MEM A DM<2> 15 28
MEM_A_DQ_BYTE3	MEM_40S	MEM_DATA	MEM A DM<3> 15 28
MEM_A_DQ_BYTE4	MEM_40S	MEM_DATA	MEM A DM<4> 15 28
MEM_A_DQ_BYTE5	MEM_40S	MEM_DATA	MEM A DM<5> 15 28
MEM_A_DQ_BYTE6	MEM_40S	MEM_DATA	MEM A DM<6> 15 28
MEM_A_DQ_BYTE7	MEM_40S	MEM_DATA	MEM A DM<7> 15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS P<0> 15 28
MEM_A_DQS0	MEM_70D	MEM_DQS	MEM A DQS N<0> 15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS P<1> 15 28
MEM_A_DQS1	MEM_70D	MEM_DQS	MEM A DQS N<1> 15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS P<2> 15 28
MEM_A_DQS2	MEM_70D	MEM_DQS	MEM A DQS N<2> 15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS P<3> 15 28
MEM_A_DQS3	MEM_70D	MEM_DQS	MEM A DQS N<3> 15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS P<4> 15 28
MEM_A_DQS4	MEM_70D	MEM_DQS	MEM A DQS N<4> 15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS P<5> 15 28
MEM_A_DQS5	MEM_70D	MEM_DQS	MEM A DQS N<5> 15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS P<6> 15 28
MEM_A_DQS6	MEM_70D	MEM_DQS	MEM A DQS N<6> 15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS P<7> 15 28
MEM_A_DQS7	MEM_70D	MEM_DQS	MEM A DQS N<7> 15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK P<5..0> 15 28
MEM_B_CLK	MEM_70D_VDD	MEM_CLK	MEM B CLK N<5..0> 15 28
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CKE<3..0> 15 28
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B CS L<3..0> 15 28
MEM_B_CNTRL	MEM_40S_VDD	MEM_CTRL	MEM B ODT<3..0> 15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B A<14..0> 15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B BA<2..0> 15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B RAS L 15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B CAS L 15 28
MEM_B_CMD	MEM_40S_VDD	MEM_CMD	MEM B WE L 15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DQ<7..0> 15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DQ<15..8> 15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DQ<23..16> 15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DQ<31..24> 15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DQ<39..32> 15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DQ<47..40> 15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DQ<55..48> 15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DQ<63..56> 15 28
MEM_B_DQ_BYTE0	MEM_40S	MEM_DATA	MEM B DM<0> 15 28
MEM_B_DQ_BYTE1	MEM_40S	MEM_DATA	MEM B DM<1> 15 28
MEM_B_DQ_BYTE2	MEM_40S	MEM_DATA	MEM B DM<2> 15 28
MEM_B_DQ_BYTE3	MEM_40S	MEM_DATA	MEM B DM<3> 15 28
MEM_B_DQ_BYTE4	MEM_40S	MEM_DATA	MEM B DM<4> 15 28
MEM_B_DQ_BYTE5	MEM_40S	MEM_DATA	MEM B DM<5> 15 28
MEM_B_DQ_BYTE6	MEM_40S	MEM_DATA	MEM B DM<6> 15 28
MEM_B_DQ_BYTE7	MEM_40S	MEM_DATA	MEM B DM<7> 15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS P<0> 15 28
MEM_B_DQS0	MEM_70D	MEM_DQS	MEM B DQS N<0> 15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS P<1> 15 28
MEM_B_DQS1	MEM_70D	MEM_DQS	MEM B DQS N<1> 15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS P<2> 15 28
MEM_B_DQS2	MEM_70D	MEM_DQS	MEM B DQS N<2> 15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS P<3> 15 28
MEM_B_DQS3	MEM_70D	MEM_DQS	MEM B DQS N<3> 15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS P<4> 15 28
MEM_B_DQS4	MEM_70D	MEM_DQS	MEM B DQS N<4> 15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS P<5> 15 28
MEM_B_DQS5	MEM_70D	MEM_DQS	MEM B DQS N<5> 15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS P<6> 15 28
MEM_B_DQS6	MEM_70D	MEM_DQS	MEM B DQS N<6> 15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS P<7> 15 28
MEM_B_DQS7	MEM_70D	MEM_DQS	MEM B DQS N<7> 15 28
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP VDD 16
MCP_MEM_COMP	MCP_MEM_COMP	MCP_MEM_COMP	MCP MEM COMP GND 16

Memory Constraints

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE		SHEET	OF
NONE		88	96

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	13.1 MM	=90_OHM_DIFF	=90_OHM_DIFF
CLK_PCIE_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?
MCP_PEX_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.4

Analog Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CRT_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CRT	*	=4:1_SPACING	?
CRT_2CRT	*	=STANDARD	?
CRT_2CLK	*	50 MIL	?
CRT_2SWITCHER	*	250 MIL	?
CRT_SYNC	*	16 MIL	?
MCP_DAC_COMP	*	=2:1_SPACING	?

CRT signal single-ended impedance varies by location:
 - 37.5-ohm from MCP to first termination resistor.
 - 50-ohm from first to second termination resistor.
 - 75-ohm from output of three-pole filter to connector (if possible).
 R/G/B signals should be matched as close as possible and < 10 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.1 & 2.5.2.

Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
MCP_DV_COMP	*	Y	20 MIL	20 MIL	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3X_DIELECTRIC	?
LVDS	*	=3X_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
 SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4X_DIELECTRIC	?
SATA_TERM	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
PEG_R2D	PCIE_90D	PCIE	PEG R2D P<15..0>	70
PEG_R2D	PCIE_90D	PCIE	PEG R2D N<15..0>	70
PEG_R2D	PCIE_90D	PCIE	PEG R2D C P<15..0>	9 70
PEG_R2D	PCIE_90D	PCIE	PEG R2D C N<15..0>	9 70
PEG_D2R	PCIE_90D	PCIE	PEG D2R P<15..0>	9 70
PEG_D2R	PCIE_90D	PCIE	PEG D2R N<15..0>	9 70
PEG_D2R	PCIE_90D	PCIE	PEG D2R C P<15..0>	70
PEG_D2R	PCIE_90D	PCIE	PEG D2R C N<15..0>	70
PCIE_MINI_R2D_P	PCIE_90D	PCIE	PCIE MINI R2D P	31 95
PCIE_MINI_R2D_N	PCIE_90D	PCIE	PCIE MINI R2D N	31 95
PCIE_MINI_R2D_C_P	PCIE_90D	PCIE	PCIE MINI R2D C P	17 31
PCIE_MINI_R2D_C_N	PCIE_90D	PCIE	PCIE MINI R2D C N	17 31
PCIE_MINI_D2R_P	PCIE_90D	PCIE	PCIE MINI D2R P	17 31
PCIE_MINI_D2R_N	PCIE_90D	PCIE	PCIE MINI D2R N	17 31
PCIE_FW_R2D_P	PCIE_90D	PCIE	PCIE FW R2D P	36
PCIE_FW_R2D_N	PCIE_90D	PCIE	PCIE FW R2D N	36
PCIE_FW_R2D_C_P	PCIE_90D	PCIE	PCIE FW R2D C P	17 36
PCIE_FW_R2D_C_N	PCIE_90D	PCIE	PCIE FW R2D C N	17 36
PCIE_FW_D2R_P	PCIE_90D	PCIE	PCIE FW D2R P	17 36
PCIE_FW_D2R_N	PCIE_90D	PCIE	PCIE FW D2R N	17 36
PCIE_FW_D2R_C_P	PCIE_90D	PCIE	PCIE FW D2R C P	36
PCIE_FW_D2R_C_N	PCIE_90D	PCIE	PCIE FW D2R C N	36
PCIE_EXCARD_R2D_P	PCIE_90D	PCIE	PCIE EXCARD R2D P	7 32 95
PCIE_EXCARD_R2D_N	PCIE_90D	PCIE	PCIE EXCARD R2D N	7 32 95
PCIE_EXCARD_R2D_C_P	PCIE_90D	PCIE	PCIE EXCARD R2D C P	17 32
PCIE_EXCARD_R2D_C_N	PCIE_90D	PCIE	PCIE EXCARD R2D C N	17 32
PCIE_EXCARD_D2R_P	PCIE_90D	PCIE	PCIE EXCARD D2R P	7 17 32
PCIE_EXCARD_D2R_N	PCIE_90D	PCIE	PCIE EXCARD D2R N	7 17 32
PEG_CLK100M_P	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M P	17 70
PEG_CLK100M_N	CLK_PCIE_100D	CLK_PCIE	PEG CLK100M N	17 70
PCIE_CLK100M_MINI_P	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI P	17 31
PCIE_CLK100M_MINI_N	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M MINI N	17 31
PCIE_CLK100M_FW_P	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW P	17 36
PCIE_CLK100M_FW_N	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M FW N	17 36
PCIE_CLK100M_EXCARD_P	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD P	17 32
PCIE_CLK100M_EXCARD_N	CLK_PCIE_100D	CLK_PCIE	PCIE CLK100M EXCARD N	17 32
MCP_PEX_CLK_COMP	MCP_PEX_COMP	MCP_PEX_COMP	MCP PEX CLK COMP	17
CRT_IG_R_C_PR	CRT_50S	CRT	CRT IG R C PR	18 25
CRT_IG_G_Y_Y	CRT_50S	CRT	CRT IG G Y Y	18 25
CRT_IG_B_COMP_PB	CRT_50S	CRT	CRT IG B COMP PB	18 25
CRT_IG_HSYNC	CRT_50S	CRT_SYNC	CRT IG HSYNC	18 25
CRT_IG_VSYNC	CRT_50S	CRT_SYNC	CRT IG VSYNC	18 25
MCP_TV_DAC_RSET	MCP_DAC_COMP	MCP_DAC_COMP	MCP TV DAC RSET	18 25
MCP_TV_DAC_VREF	MCP_DAC_COMP	MCP_DAC_COMP	MCP TV DAC VREF	18 25
TMDS_IG_TXC_P	DP_100D	DISPLAYPORT	TMDS IG TXC P	
TMDS_IG_TXC_N	DP_100D	DISPLAYPORT	TMDS IG TXC N	
TMDS_IG_TXD_P<2..0>	DP_100D	DISPLAYPORT	TMDS IG TXD P<2..0>	
TMDS_IG_TXD_N<2..0>	DP_100D	DISPLAYPORT	TMDS IG TXD N<2..0>	
DP_IG_ML_P<3..0>	DP_100D	DISPLAYPORT	DP IG ML P<3..0>	9 80
DP_IG_ML_N<3..0>	DP_100D	DISPLAYPORT	DP IG ML N<3..0>	9 80
DP_IG_AUX_CH_P	DP_100D	DISPLAYPORT	DP IG AUX CH P	18 80
DP_IG_AUX_CH_N	DP_100D	DISPLAYPORT	DP IG AUX CH N	18 80
MCP_HDMI_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP HDMI RSET	18 25
MCP_HDMI_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP HDMI VPROBE	18 25
LVDS_IG_A_CLK_P	LVDS_100D	LVDS	LVDS IG A CLK P	18 83
LVDS_IG_A_CLK_N	LVDS_100D	LVDS	LVDS IG A CLK N	18 83
LVDS_IG_A_DATA_P<2..0>	LVDS_100D	LVDS	LVDS IG A DATA P<2..0>	18 83
LVDS_IG_A_DATA_N<2..0>	LVDS_100D	LVDS	LVDS IG A DATA N<2..0>	18 83
LVDS_IG_A_DATA_P<3>	LVDS_100D	LVDS	LVDS IG A DATA P<3>	9 18
LVDS_IG_A_DATA_N<3>	LVDS_100D	LVDS	LVDS IG A DATA N<3>	9 18
LVDS_IG_B_CLK_P	LVDS_100D	LVDS	LVDS IG B CLK P	9 18
LVDS_IG_B_CLK_N	LVDS_100D	LVDS	LVDS IG B CLK N	9 18
LVDS_IG_B_DATA_P<2..0>	LVDS_100D	LVDS	LVDS IG B DATA P<2..0>	18 83
LVDS_IG_B_DATA_N<2..0>	LVDS_100D	LVDS	LVDS IG B DATA N<2..0>	18 83
LVDS_IG_B_DATA_P<3>	LVDS_100D	LVDS	LVDS IG B DATA P<3>	9 18
LVDS_IG_B_DATA_N<3>	LVDS_100D	LVDS	LVDS IG B DATA N<3>	9 18
MCP_IFPAB_RSET	MCP_DV_COMP	MCP_DV_COMP	MCP IFPAB RSET	18 25
MCP_IFPAB_VPROBE	MCP_DV_COMP	MCP_DV_COMP	MCP IFPAB VPROBE	18 25
SATA_HDD_R2D_C_P	SATA_100D	SATA	SATA HDD R2D C P	20 39
SATA_HDD_R2D_C_N	SATA_100D	SATA	SATA HDD R2D C N	20 39
SATA_HDD_R2D_P	SATA_100D	SATA	SATA HDD R2D P	39
SATA_HDD_R2D_N	SATA_100D	SATA	SATA HDD R2D N	39
SATA_HDD_D2R_P	SATA_100D	SATA	SATA HDD D2R P	20 39
SATA_HDD_D2R_N	SATA_100D	SATA	SATA HDD D2R N	20 39
SATA_HDD_D2R_C_P	SATA_100D	SATA	SATA HDD D2R C P	39
SATA_HDD_D2R_C_N	SATA_100D	SATA	SATA HDD D2R C N	39
SATA_ODD_R2D_C_P	SATA_100D	SATA	SATA ODD R2D C P	20 39
SATA_ODD_R2D_C_N	SATA_100D	SATA	SATA ODD R2D C N	20 39
SATA_ODD_R2D_P	SATA_100D	SATA	SATA ODD R2D P	7 39
SATA_ODD_R2D_N	SATA_100D	SATA	SATA ODD R2D N	7 39
SATA_ODD_D2R_P	SATA_100D	SATA	SATA ODD D2R P	20 39
SATA_ODD_D2R_N	SATA_100D	SATA	SATA ODD D2R N	20 39
SATA_ODD_D2R_C_P	SATA_100D	SATA	SATA ODD D2R C P	7 39
SATA_ODD_D2R_C_N	SATA_100D	SATA	SATA ODD D2R C N	7 39
MCP_SATA_TERM	SATA_TERM	SATA_TERM	MCP SATA_TERM	20

MCP Constraints 1
 SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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APPLE INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7546	A.0.0
SCALE	NONE	SHT	89 OF 96

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_PCI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCI	*	=STANDARD	?
CLK_PCI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.8.

LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.9.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_USB_RBIAIS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?	USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.10.1.

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.11.1.

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?
MCP_HDA_COMP	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.12.1.

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.13.

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.14.

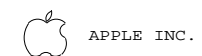
ELECTRICAL_CONSTRAINT_SET	NET_TYPE		MCP CONSTRAINT	PAGE
	PHYSICAL	SPACING		
MCP_DEBUG	PCI_55S	PCI	MCP_DEBUG<7..0>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<23..8>	13 19
PCI_AD24	PCI_55S	PCI	PCI_AD<24>	13 19
PCI_AD	PCI_55S	PCI	PCI_AD<31..25>	13 19
PCI_AD	PCI_55S	PCI	PCI_PAR	13 19
PCI_C_BE_L	PCI_55S	PCI	PCI_C_BE_L<3..0>	13 19
PCI_CNTRL	PCI_55S	PCI	PCI_IRDY_L	13 19
PCI_CNTRL	PCI_55S	PCI	PCI_DEVSEL_L	13 19
PCI_CNTRL	PCI_55S	PCI	PCI_PERR_L	13 19
PCI_CNTRL	PCI_55S	PCI	PCI_SERR_L	13 19
PCI_CNTRL	PCI_55S	PCI	PCI_STOP_L	13 19
PCI_CNTRL	PCI_55S	PCI	PCI_TRDY_L	13 19
PCI_CNTRL	PCI_55S	PCI	PCI_FRAME_L	13 19
PCI_REQ0_L	PCI_55S	PCI	PCI_REQ0_L	13 19
PCI_GNT0_L	PCI_55S	PCI	PCI_GNT0_L	13 19
PCI_REQ1_L	PCI_55S	PCI	PCI_REQ1_L	13 19
PCI_GNT1_L	PCI_55S	PCI	PCI_GNT1_L	13 19
PCI_INTW_L	PCI_55S	PCI	PCI_INTW_L	13 19
PCI_INTX_L	PCI_55S	PCI	PCI_INTX_L	13 19
PCI_INTY_L	PCI_55S	PCI	PCI_INTY_L	13 19
PCI_INTZ_L	PCI_55S	PCI	PCI_INTZ_L	13 19
MCP_PCI_CLK2	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP_R	19
CLK_PCI_55S	CLK_PCI_55S	CLK_PCI	PCI_CLK33M MCP	19
LPC_AD	LPC_55S	LPC	LPC_AD<3..0>	19 42 44 83
LPC_FRAME_L	LPC_55S	LPC	LPC_FRAME_L	19 42 44 83
LPC_RESET_L	LPC_55S	LPC	LPC_RESET_L	19 26 83
MCP_LPC_CLK0	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC_R	19 26
CLK_LPC_55S	CLK_LPC_55S	CLK_LPC	LPC_CLK33M SMC	26 42
CLK_LPC_55S	CLK_LPC_55S	CLK_LPC	LPC_CLK33M LPCPLUS	26 44
USB_EXTN	USB_90D	USB	USB_EXTN_P	20 40
USB_EXTN	USB_90D	USB	USB_EXTN_N	20 40
USB_EXTN	USB_90D	USB	USB_EXTN_MUXED_P	20 40
USB_EXTN	USB_90D	USB	USB_EXTN_MUXED_N	20 40
USB_MINI	USB_90D	USB	USB_MINI_P	9 20
USB_MINI	USB_90D	USB	USB_MINI_N	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_P	9 20
USB_EXTD	USB_90D	USB	USB_EXTD_N	9 20
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	9 20 31
USB_CAMERA	USB_90D	USB	USB_CAMERA_N	9 20 31
USB_BT	USB_90D	USB	USB_BT_P	20 31
USB_BT	USB_90D	USB	USB_BT_N	20 31
USB_TPAD	USB_90D	USB	USB_TPAD_P	20 50
USB_TPAD	USB_90D	USB	USB_TPAD_N	20 50
USB_IR	USB_90D	USB	USB_IR_P	20 41
USB_IR	USB_90D	USB	USB_IR_N	20 41
USB_EXTB	USB_90D	USB	USB_EXTB_P	20 40
USB_EXTB	USB_90D	USB	USB_EXTB_N	20 40
USB_EXCARD	USB_90D	USB	USB_EXCARD_P	20 32
USB_EXCARD	USB_90D	USB	USB_EXCARD_N	20 32
USB_EXTC	USB_90D	USB	USB_EXTC_P	9 20
USB_EXTC	USB_90D	USB	USB_EXTC_N	9 20
MCP_USB_RBIAIS	MCP_USB_RBIAIS		MCP_USB_RBIAIS_GND	20
SMBUS_MCP_0_CLK	SMB_55S	SMB	SMBUS_MCP_0_CLK	7 13 21 45
SMBUS_MCP_0_DATA	SMB_55S	SMB	SMBUS_MCP_0_DATA	7 13 21 45
SMBUS_MCP_1_CLK	SMB_55S	SMB	SMBUS_MCP_1_CLK	21 45
SMBUS_MCP_1_DATA	SMB_55S	SMB	SMBUS_MCP_1_DATA	21 45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	9 21
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK_R	21
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	21 54
HDA_SYNC	HDA_55S	HDA	HDA_SYNC_R	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_R_L	21
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	21 54
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	21 54
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN_CODEC	21 54
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	21 54
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT_R	21
MCP_HDA_PULLDN_COMP	MCP_HDA_COMP		MCP_HDA_PULLDN_COMP	21
MCP_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK_R	21 26
CLK_SLOW_55S	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	26 42
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	21 44
SPI_CLK	SPI_55S	SPI	SPI_CLK	44 53
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	21 44
SPI_MOSI	SPI_55S	SPI	SPI_MOSI	44 53
SPI_MISO	SPI_55S	SPI	SPI_MISO	21 44
SPI_MISO	SPI_55S	SPI	SPI_MISO_R	53
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	21 44
SPI_CS0	SPI_55S	SPI	SPI_CS0_L	21 44

MCP Constraints 2

SYNC_MASTER=MUXGFX SYNC_DATE=02/18/2008

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SCALE	SHT	OF
NONE	90	96

MCP RGMII (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MCP_MII_COMP	*	=STANDARD	7.5 MIL	7.5 MIL	=STANDARD	=STANDARD	=STANDARD
ENET_MII_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MCP_BUF0_CLK	*	=3:1_SPACING	?
ENET_MII	*	12 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Sections 2.7.2 & 2.7.4

88E1116R (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP VDD 18
MCP_MII_COMP	MCP_MII_COMP		MCP MII COMP GND 18
MCP_CLK25M_BUF0	ENET_MII_55S	MCP_BUF0_CLK	MCP CLK25M BUF0 R 18 34
	ENET_MII_55S	MCP_BUF0_CLK	RTL8211 CLK25M CKXTAL1 33 34
ENET_INTR_L	ENET_MII_55S	ENET_MII	ENET INTR L 18 33
ENET_MDIO	ENET_MII_55S	ENET_MII	ENET MDIO 18 33
ENET_MDC	ENET_MII_55S	ENET_MII	ENET MDC 18 33
ENET_PWRDWN_L	ENET_MII_55S	ENET_MII	ENET PWRDWN L 18 33
	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK R 33
ENET_RXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M RXCLK 18 33
	ENET_MII_55S	ENET_MII	ENET RXD R<3..0> 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET RXD<0> 18 33
ENET_RXD_STRAP	ENET_MII_55S	ENET_MII	ENET RXD<3..1> 18 33
ENET_RXD	ENET_MII_55S	ENET_MII	ENET RX CTRL 18 33
ENET_TXCLK	ENET_MII_55S	ENET_MII	ENET CLK125M TXCLK 18 33
ENET_TXD0	ENET_MII_55S	ENET_MII	ENET TXD<0> 18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TXD<3..1> 18 33
ENET_TXD	ENET_MII_55S	ENET_MII	ENET TX CTRL 18 33
	ENET_MII_55S	ENET_MII	ENET RESET L 18 33
ENET_MDI	ENET_MDI_100D	ENET_MDI	ENET MDI P<3..0> 33 35
	ENET_MDI_100D	ENET_MDI	ENET MDI N<3..0> 33 35

Ethernet Constraints

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SCALE	SHT	OF
NONE	91	96

8

7

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FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	
	PHYSICAL			
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	36 38
FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	36 38
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	36 38
FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	36 38
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	36 38
FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	36 38
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	36 38
FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	36 38
Port 2 Not Used				

D

D

C

C

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FireWire Constraints

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NONE	92	96

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7

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IT01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
SMBUS_SMC_A_S3_SCL	SMB_55S	SMB	SMBUS_SMC_A_S3_SCL	7 45
SMBUS_SMC_A_S3_SDA	SMB_55S	SMB	SMBUS_SMC_A_S3_SDA	7 45
SMBUS_SMC_B_S0_SCL	SMB_55S	SMB	SMBUS_SMC_B_S0_SCL	45
SMBUS_SMC_B_S0_SDA	SMB_55S	SMB	SMBUS_SMC_B_S0_SDA	45
SMBUS_SMC_0_S0_SCL	SMB_55S	SMB	SMBUS_SMC_0_S0_SCL	45
SMBUS_SMC_0_S0_SDA	SMB_55S	SMB	SMBUS_SMC_0_S0_SDA	45
SMBUS_SMC_BSA_SCL	SMB_55S	SMB	SMBUS_SMC_BSA_SCL	45
SMBUS_SMC_BSA_SDA	SMB_55S	SMB	SMBUS_SMC_BSA_SDA	45
SMBUS_SMC_MGMT_SCL	SMB_55S	SMB	SMBUS_SMC_MGMT_SCL	45
SMBUS_SMC_MGMT_SDA	SMB_55S	SMB	SMBUS_SMC_MGMT_SDA	45

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P	61
	1T01_DIFFPAIR		CHGR_CSI_N	61
CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P	61
	1T01_DIFFPAIR		CHGR_CSO_N	61

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C

C

B

B

A

A


SMC Constraints

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NONE	93		96

8

7

6

5

4

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GDDR3 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR3_40R55SE	*	=55_OHM_SE	=40_OHM_SE	0.095 MM	12.7 MM	=STANDARD	=STANDARD
GDDR3_40SE	*	=40_OHM_SE	=40_OHM_SE	0.095 MM	=40_OHM_SE	=STANDARD	=STANDARD
GDDR3_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	0.095 MM	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR3_CLK	*	=2.5:1_SPACING	?
GDDR3_CMD	*	=2.5:1_SPACING	?
GDDR3_DATA	*	=2.5:1_SPACING	?
GDDR3_DQS	*	=2.5:1_SPACING	?

From T18 MXM:
Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
LVDS_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT	SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?	DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?	LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length. DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps. DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals. Max length of LVDS/DisplayPort/TMDS traces: 12 inches. SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

MUXGFx Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
LVDS_A_CLK	LVDS_100p	LVDS	LVDS A CLK P
LVDS_A_CLK	LVDS_100p	LVDS	LVDS A CLK N
LVDS_A_DATA	LVDS_100p	LVDS	LVDS A DATA P<2..0>
LVDS_A_DATA	LVDS_100p	LVDS	LVDS A DATA N<2..0>
LVDS_B_CLK	LVDS_100p	LVDS	LVDS B CLK P
LVDS_B_CLK	LVDS_100p	LVDS	LVDS B CLK N
LVDS_B_DATA	LVDS_100p	LVDS	LVDS B DATA P<2..0>
LVDS_B_DATA	LVDS_100p	LVDS	LVDS B DATA N<2..0>
LVDS_CONN_A_CLK_F_P	LVDS_100p	LVDS	LVDS_CONN A CLK F P
LVDS_CONN_A_CLK_F_N	LVDS_100p	LVDS	LVDS_CONN A CLK F N
LVDS_CONN_B_CLK_F_P	LVDS_100p	LVDS	LVDS_CONN B CLK F P
LVDS_CONN_B_CLK_F_N	LVDS_100p	LVDS	LVDS_CONN B CLK F N
LVDS_CONN_A_CLK_P	LVDS_100p	LVDS	LVDS_CONN A CLK P
LVDS_CONN_A_CLK_N	LVDS_100p	LVDS	LVDS_CONN A CLK N
LVDS_CONN_A_DATA_P<2..0>	LVDS_100p	LVDS	LVDS_CONN A DATA P<2..0>
LVDS_CONN_A_DATA_N<2..0>	LVDS_100p	LVDS	LVDS_CONN A DATA N<2..0>
LVDS_CONN_B_CLK_P	LVDS_100p	LVDS	LVDS_CONN B CLK P
LVDS_CONN_B_CLK_N	LVDS_100p	LVDS	LVDS_CONN B CLK N
LVDS_CONN_B_DATA_P<2..0>	LVDS_100p	LVDS	LVDS_CONN B DATA P<2..0>
LVDS_CONN_B_DATA_N<2..0>	LVDS_100p	LVDS	LVDS_CONN B DATA N<2..0>
DP_ML	DP_100D	DISPLAYPORT	DP ML C P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP ML C N<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP ML P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP ML N<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP ML CONN P<3..0>
DP_ML	DP_100D	DISPLAYPORT	DP ML CONN N<3..0>
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX CH C P
DP_AUX_CH	DP_100D	DISPLAYPORT	DP_AUX CH C N

GDDR3 FB A/B Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
FB_A_CLK_P	gDDR3_80D	gDDR3_CLK	FB A CLK P<0>
FB_A_CLK_N	gDDR3_80D	gDDR3_CLK	FB A CLK N<0>
FB_B_CLK_P	gDDR3_80D	gDDR3_CLK	FB B CLK P<1>
FB_B_CLK_N	gDDR3_80D	gDDR3_CLK	FB B CLK N<1>
FB_A_MA<1..0>	gDDR3_40R55SE	gDDR3_CMD	FB A MA<1..0>
FB_B_MA<1..0>	gDDR3_40R55SE	gDDR3_CMD	FB B MA<1..0>
FB_A_BA<2..0>	gDDR3_40R55SE	gDDR3_CMD	FB A BA<2..0>
FB_B_BA<2..0>	gDDR3_40R55SE	gDDR3_CMD	FB B BA<2..0>
FB_A_RAS_L	gDDR3_40R55SE	gDDR3_CMD	FB A RAS L
FB_B_RAS_L	gDDR3_40R55SE	gDDR3_CMD	FB B RAS L
FB_A_CAS_L	gDDR3_40R55SE	gDDR3_CMD	FB A CAS L
FB_B_CAS_L	gDDR3_40R55SE	gDDR3_CMD	FB B CAS L
FB_A_WE_L	gDDR3_40R55SE	gDDR3_CMD	FB A WE L
FB_B_WE_L	gDDR3_40R55SE	gDDR3_CMD	FB B WE L
FB_A_CKE	gDDR3_40R55SE	gDDR3_CMD	FB A CKE
FB_B_CKE	gDDR3_40R55SE	gDDR3_CMD	FB B CKE
FB_A_CS0_L	gDDR3_40R55SE	gDDR3_CMD	FB A CS0 L
FB_B_CS0_L	gDDR3_40R55SE	gDDR3_CMD	FB B CS0 L
FB_A_DRAM_RST	gDDR3_40R55SE	gDDR3_CMD	FB A DRAM_RST
FB_B_DRAM_RST	gDDR3_40R55SE	gDDR3_CMD	FB B DRAM_RST
FB_A_IMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB A IMA<5..2>
FB_B_IMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB B IMA<5..2>
FB_A_UMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB A UMA<5..2>
FB_B_UMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB B UMA<5..2>
FB_A_WDOS<0>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<0>
FB_B_WDOS<0>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<0>
FB_A_WDOS<1>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<1>
FB_B_WDOS<1>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<1>
FB_A_WDOS<2>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<2>
FB_B_WDOS<2>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<2>
FB_A_WDOS<3>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<3>
FB_B_WDOS<3>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<3>
FB_A_RDQS<0>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<0>
FB_B_RDQS<0>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<0>
FB_A_RDQS<1>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<1>
FB_B_RDQS<1>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<1>
FB_A_RDQS<2>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<2>
FB_B_RDQS<2>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<2>
FB_A_RDQS<3>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<3>
FB_B_RDQS<3>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<3>
FB_A_DQ<7..0>	gDDR3_40SE	gDDR3_DATA	FB A DQ<7..0>
FB_B_DQ<7..0>	gDDR3_40SE	gDDR3_DATA	FB B DQ<7..0>
FB_A_DQ<15..8>	gDDR3_40SE	gDDR3_DATA	FB A DQ<15..8>
FB_B_DQ<15..8>	gDDR3_40SE	gDDR3_DATA	FB B DQ<15..8>
FB_A_DQ<23..16>	gDDR3_40SE	gDDR3_DATA	FB A DQ<23..16>
FB_B_DQ<23..16>	gDDR3_40SE	gDDR3_DATA	FB B DQ<23..16>
FB_A_DQ<31..24>	gDDR3_40SE	gDDR3_DATA	FB A DQ<31..24>
FB_B_DQ<31..24>	gDDR3_40SE	gDDR3_DATA	FB B DQ<31..24>
FB_A_DQM_L<0>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<0>
FB_B_DQM_L<0>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<0>
FB_A_DQM_L<1>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<1>
FB_B_DQM_L<1>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<1>
FB_A_DQM_L<2>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<2>
FB_B_DQM_L<2>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<2>
FB_A_DQM_L<3>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<3>
FB_B_DQM_L<3>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<3>
FB_A_WDOS<4>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<4>
FB_B_WDOS<4>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<4>
FB_A_WDOS<5>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<5>
FB_B_WDOS<5>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<5>
FB_A_WDOS<6>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<6>
FB_B_WDOS<6>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<6>
FB_A_WDOS<7>	gDDR3_40SE	gDDR3_PQS	FB A WDOS<7>
FB_B_WDOS<7>	gDDR3_40SE	gDDR3_PQS	FB B WDOS<7>
FB_A_RDQS<4>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<4>
FB_B_RDQS<4>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<4>
FB_A_RDQS<5>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<5>
FB_B_RDQS<5>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<5>
FB_A_RDQS<6>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<6>
FB_B_RDQS<6>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<6>
FB_A_RDQS<7>	gDDR3_40SE	gDDR3_PQS	FB A RDQS<7>
FB_B_RDQS<7>	gDDR3_40SE	gDDR3_PQS	FB B RDQS<7>
FB_A_DQ<39..32>	gDDR3_40SE	gDDR3_DATA	FB A DQ<39..32>
FB_B_DQ<39..32>	gDDR3_40SE	gDDR3_DATA	FB B DQ<39..32>
FB_A_DQ<47..40>	gDDR3_40SE	gDDR3_DATA	FB A DQ<47..40>
FB_B_DQ<47..40>	gDDR3_40SE	gDDR3_DATA	FB B DQ<47..40>
FB_A_DQ<55..48>	gDDR3_40SE	gDDR3_DATA	FB A DQ<55..48>
FB_B_DQ<55..48>	gDDR3_40SE	gDDR3_DATA	FB B DQ<55..48>
FB_A_DQ<63..56>	gDDR3_40SE	gDDR3_DATA	FB A DQ<63..56>
FB_B_DQ<63..56>	gDDR3_40SE	gDDR3_DATA	FB B DQ<63..56>
FB_A_DQM_L<4>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<4>
FB_B_DQM_L<4>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<4>
FB_A_DQM_L<5>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<5>
FB_B_DQM_L<5>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<5>
FB_A_DQM_L<6>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<6>
FB_B_DQM_L<6>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<6>
FB_A_DQM_L<7>	gDDR3_40SE	gDDR3_DATA	FB A DQM_L<7>
FB_B_DQM_L<7>	gDDR3_40SE	gDDR3_DATA	FB B DQM_L<7>

GDDR3 FB C/D Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
FB_C_CLK_P	gDDR3_80D	gDDR3_CLK	FB C CLK P<0>
FB_C_CLK_N	gDDR3_80D	gDDR3_CLK	FB C CLK N<0>
FB_D_CLK_P	gDDR3_80D	gDDR3_CLK	FB D CLK P<1>
FB_D_CLK_N	gDDR3_80D	gDDR3_CLK	FB D CLK N<1>
FB_C_MA<1..0>	gDDR3_40R55SE	gDDR3_CMD	FB C MA<1..0>
FB_D_MA<1..0>	gDDR3_40R55SE	gDDR3_CMD	FB D MA<1..0>
FB_C_BA<2..0>	gDDR3_40R55SE	gDDR3_CMD	FB C BA<2..0>
FB_D_BA<2..0>	gDDR3_40R55SE	gDDR3_CMD	FB D BA<2..0>
FB_C_RAS_L	gDDR3_40R55SE	gDDR3_CMD	FB C RAS L
FB_D_RAS_L	gDDR3_40R55SE	gDDR3_CMD	FB D RAS L
FB_C_CAS_L	gDDR3_40R55SE	gDDR3_CMD	FB C CAS L
FB_D_CAS_L	gDDR3_40R55SE	gDDR3_CMD	FB D CAS L
FB_C_WE_L	gDDR3_40R55SE	gDDR3_CMD	FB C WE L
FB_D_WE_L	gDDR3_40R55SE	gDDR3_CMD	FB D WE L
FB_C_CKE	gDDR3_40R55SE	gDDR3_CMD	FB C CKE
FB_D_CKE	gDDR3_40R55SE	gDDR3_CMD	FB D CKE
FB_C_CS0_L	gDDR3_40R55SE	gDDR3_CMD	FB C CS0 L
FB_D_CS0_L	gDDR3_40R55SE	gDDR3_CMD	FB D CS0 L
FB_C_DRAM_RST	gDDR3_40R55SE	gDDR3_CMD	FB C DRAM_RST
FB_D_DRAM_RST	gDDR3_40R55SE	gDDR3_CMD	FB D DRAM_RST
FB_C_IMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB C IMA<5..2>
FB_D_IMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB D IMA<5..2>
FB_C_UMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB C UMA<5..2>
FB_D_UMA<5..2>	gDDR3_40SE	gDDR3_CMD	FB D UMA<5..2>
FB_C_WDOS<0>	gDDR3_40SE	gDDR3_PQS	FB C WDOS<0>
FB_D_WDOS<0>	gDDR3_40SE	gDDR3_PQS	FB D WDOS<0>
FB_C_WDOS<1>	gDDR3_40SE	gDDR3_PQS	FB C WDOS<1>
FB_D_WDOS<1>	gDDR3_40SE	gDDR3_PQS	FB D WDOS<1>
FB_C_WDOS<2>	gDDR3_40SE	gDDR3_PQS	FB C WDOS<2>
FB_D_WDOS<2>	gDDR3_40SE	gDDR3_PQS	FB D WDOS<2>
FB_C_WDOS<3>	gDDR3_40SE	gDDR3_PQS	FB C WDOS<3>
FB_D_WDOS<3>	gDDR3_40SE	gDDR3_PQS	FB D WDOS<3>
FB_C_RDQS<0>	gDDR3_40SE	gDDR3_PQS	FB C RDQS<0>
FB_D_RDQS<0>	gDDR3_40SE	gDDR3_PQS	FB D RDQS<0>
FB_C_RDQS<1>	gDDR3_40SE	gDDR3_PQS	FB C RDQS<1>
FB_D_RDQS<1>	gDDR3_40SE	gDDR3_PQS	FB D RDQS<1>
FB_C_RDQS<2>	gDDR3_40SE	gDDR3_PQS	FB C RDQS<2>
FB_D_RDQS<2>	gDDR3_40SE	gDDR3_PQS	FB D RDQS<2>
FB_C_RDQS<3>	gDDR3_40SE	gDDR3_PQS	FB C RDQS<3>
FB_D_RDQS<3>	gDDR3_40SE	gDDR3_PQS	FB D RDQS<3>
FB_C_DQ<7..0>	gDDR3_40SE	gDDR3_DATA	FB C DQ<7..0>
FB_D_DQ<7..0>	gDDR3_40SE	gDDR3_DATA	FB D DQ<7..0>
FB_C_DQ<15..8>	gDDR3_40SE	gDDR3_DATA	FB C DQ<15..8>
FB_D_DQ<15..8>	gDDR3_40SE	gDDR3_DATA	FB D DQ<15..8>
FB_C_DQ<23..16>	gDDR3_40SE	gDDR3_DATA	FB C DQ<23..16>
FB_D_DQ<23..16>	gDDR3_40SE	gDDR3_DATA	FB D DQ<23..16>
FB_C_DQ<31..24>	gDDR3_40SE	gDDR3_DATA	FB C DQ<31..24>
FB_D_DQ<31..24>	gDDR3_40SE	gDDR3_DATA	FB D DQ<31..24>
FB_C_DQM_L<0>	gDDR3_40SE	gDDR3_DATA	FB C DQM_L<0>
FB_D_DQM_L<0>	gDDR3_40SE	gDDR3_DATA	FB D DQM_L<0>
FB_C_DQM_L<1>	gDDR3_40SE	gDDR3_DATA	FB C DQM_L<1>
FB_D_DQM_L<1>	gDDR3_40SE	gDDR3_DATA	FB D DQM_L<1>
FB_C_DQM_L<2>	gDDR3_40SE	gDDR3_DATA	FB C DQM_L<2>
FB_D_DQM_L<2>	gDDR3_40SE	gDDR3_DATA	FB D DQM_L<2>
FB_C_DQM_L<3>	gDDR3_40SE	gDDR3_DATA	FB C DQM_L<3>
FB_D_DQM_L<3>	gDDR3_40SE	gDDR3_DATA	FB D DQM_L<3>
FB_C_WDOS<4>	gDDR3_40SE	gDDR3_PQS	FB C WDOS<4>
FB_D_WDOS<4>	gDDR3_40SE	gDDR3_PQS	FB D WDOS<4>
FB_C_WDOS<5>	gDDR3_40SE	gDDR3_PQS	FB C WDOS<5>
FB_D_WDOS<5>	gDDR3_40SE	gDDR3_PQS	FB D WDOS<5>
FB_C_WDOS<6>	gDDR3_40SE	gDDR3_PQS	FB C WDOS<6>
FB_D_WDOS<6>	gDDR3_40SE	gDDR3_PQS	FB D WDOS<6>

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_LTO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_LTO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR		=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?
PP1V8_MEM	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	FSB_DSTB	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_70D	BOTTOM			0.127 MM	6.35 MM		

Graphics ,SATA Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	BGA	100_DIFF_BGA
DP_100D	BGA	100_DIFF_BGA
SATA_100D	BGA	100_DIFF_BGA

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
ENET_MDI_100D	ENETCONN	ENETCONN	
SATA_100D	SATA	SATA_ODD_R2D_UF_P	
SATA_100D	SATA	SATA_ODD_R2D_UF_N	
SATA_100D	SATA	SATA_ODD_D2R_UF_P	
SATA_100D	SATA	SATA_ODD_D2R_UF_N	
SATA_100D	SATA	SATA_HDD_D2R_UF_P	
SATA_100D	SATA	SATA_HDD_D2R_UF_N	
SATA_100D	SATA	SATA_HDD_R2D_UF_P	
SATA_100D	SATA	SATA_HDD_R2D_UF_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	GF_XIMVP6_VSEN_P	
SENSE_LTO1_55S	SENSE	GF_XIMVP6_VSEN_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	MCPCOREISNS_P	
SENSE_LTO1_55S	SENSE	MCPCOREISNS_N	
CPU_THERMD_DP	THERM_LTO1_55S	CPUTHMSNS_D2_P	
THERM_LTO1_55S	THERM	CPUTHMSNS_D2_N	
CPU_THERMD_DP	THERM_LTO1_55S	CPU_THERMD_P	
THERM_LTO1_55S	THERM	CPU_THERMD_N	
GPU_THERMD_DP	THERM_LTO1_55S	GPU_THERMD_P	
THERM_LTO1_55S	THERM	GPU_THERMD_N	
GPU_THERMD_DP	THERM_LTO1_55S	GPU_TDIODE_P	
THERM_LTO1_55S	THERM	GPU_TDIODE_N	
MCPTHMSNS_DP	THERM_LTO1_55S	MCPTHMSNS_D_P	
THERM_LTO1_55S	THERM	MCPTHMSNS_D_N	
MCP_THERMD_DP	THERM_LTO1_55S	MCP_THMDIODE_P	
THERM_LTO1_55S	THERM	MCP_THMDIODE_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	1V05CPUISNS_R_P	
SENSE_LTO1_55S	SENSE	1V05CPUISNS_R_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	DDRISNS_R_P	
SENSE_LTO1_55S	SENSE	DDRISNS_R_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	GPUISNS_P	
SENSE_LTO1_55S	SENSE	GPUISNS_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	1V05CPU_P	
SENSE_LTO1_55S	SENSE	1V05CPU_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	DDRISNS_P	
SENSE_LTO1_55S	SENSE	DDRISNS_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	P1V8GPU_P	
SENSE_LTO1_55S	SENSE	P1V8GPU_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	ISNS_CPU_P	
SENSE_LTO1_55S	SENSE	ISNS_CPU_N	
GND	GND	GND	
SB_POWER	PP3V3_S5	PP3V3_S5	
SB_POWER	PP3V3_S0	PP3V3_S0	
SB_POWER	PP1V5_S0	PP1V5_S0	
SENSE_DIFFPAIR	SENSE_LTO1_55S	P1V8GPUISNS_P	
SENSE_LTO1_55S	SENSE	P1V8GPUISNS_N	
SENSE_DIFFPAIR	SENSE_LTO1_55S	P1V8GPUISNS_R_P	
SENSE_LTO1_55S	SENSE	P1V8GPUISNS_R_N	

M99 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	NET_TYPE	SPACING
(PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_P
(PCIE_EXCARD)	PCIE_90D	PCIE	PCIE_EXCARD_R2D_N
(PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_P
(PCIE_MINI)	PCIE_90D	PCIE	PCIE_MINI_R2D_N
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_CONN_N
	LT01_DIFFPAIR		CHGR_CSI_R_P
	LT01_DIFFPAIR		CHGR_CSI_R_N
	LT01_DIFFPAIR		CHGR_CSO_R_P
	LT01_DIFFPAIR		CHGR_CSO_R_N
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_P
(USB_EXT_A)	USB_90D	USB	USB2_EXT_A_MUXED_N
(USB_EXT_A)	USB_90D	USB	USB2_LTI_P
(USB_EXT_A)	USB_90D	USB	USB2_LTI_N
(USB_EXT_D)	USB_90D	USB	CONN_TPAD_USB_P
(USB_EXT_D)	USB_90D	USB	CONN_TPAD_USB_N
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_P
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_CONN_N
	USB_90D	USB	CONN_USB2_BT_P
	USB_90D	USB	CONN_USB2_BT_N
	USB_90D	USB	USB_LT2_P
	USB_90D	USB	USB_LT2_N
	USB_90D	USB	USB2_EXCARD_CONN_P
	USB_90D	USB	USB2_EXCARD_CONN_N
DP_100D	DISPLAYPORT	DP	DP_IG_AUX_CH_C_P
DP_100D	DISPLAYPORT	DP	DP_IG_AUX_CH_C_N
MCP_PE4_REFCLK	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_P
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FC_N
PCIE_FC_R2D	PCIE_90D	PCIE	PCIE_FC_R2D_C_P
	PCIE_90D	PCIE	PCIE_FC_R2D_C_N
PCIE_FC_D2R	PCIE_90D	PCIE	PCIE_FC_D2R_P
	PCIE_90D	PCIE	PCIE_FC_D2R_N
	PCIE_90D	PCIE	PCIE_FC_R2D_P
	PCIE_90D	PCIE	PCIE_FC_R2D_N
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_N
	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_EXCARD_CONN_P
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_L_P_OUT
	DIFFPAIR	AUDIO	SPKRCONN_L_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_S_P_OUT
	DIFFPAIR	AUDIO	SPKRCONN_S_N_OUT
SPK_OUT	DIFFPAIR	AUDIO	SPKRCONN_R_P_OUT
	DIFFPAIR	AUDIO	SPKRCONN_R_N_OUT
	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT
	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT
	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT
	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT
	DIFFPAIR	AUDIO	SPKRAMP_S_P_OUT
	DIFFPAIR	AUDIO	SPKRAMP_S_N_OUT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	TOP	OVERWRITE	OVERWRITE	0.09 MM	5.8 MM	OVERWRITE	OVERWRITE
MEM_40S_VDD	TOP	OVERWRITE	OVERWRITE	0.09 MM	5.8 MM	OVERWRITE	OVERWRITE
MEM_70D	TOP	OVERWRITE	OVERWRITE	0.09 MM	5.8 MM	OVERWRITE	OVERWRITE
MEM_70D_VDD	TOP	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
PCIE_90D	TOP	OVERWRITE	OVERWRITE	0.09 MM	100 MIL	OVERWRITE	OVERWRITE
USB_90D	TOP	OVERWRITE	OVERWRITE	0.09 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_DV_COMP	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_MEM_COMP	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_MII_COMP	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_USB_RBIAIS	TOP	OVERWRITE	OVERWRITE	0.1 MM	500 MIL	OVERWRITE	OVERWRITE
MCP_DV_COMP	TOP	OVERWRITE	OVERWRITE	0.25 MM	250 MIL	OVERWRITE	OVERWRITE
CPU_27P4S	BOTTOM	OVERWRITE	OVERWRITE	0.23 MM	100 MIL	OVERWRITE	OVERWRITE

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	ISL4, ISL9	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE
MEM_40S_VDD	ISL3, ISL10	N	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE
MEM_70D	ISL4, ISL9	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE
MEM_70D_VDD	ISL3, ISL10	N	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE	OVERWRITE

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane)but not next to VDD island. Forces power-referenced memory signals (CLK,ADDR,CTRL) to not route on ISL3, ISL4 & ISL10(GND-referenced planes).

Project Specific Constraints	
SYNC_MASTER=MUXGFX	SYNC_DATE=02/21/2008
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SIZE	DRAWING NUMBER	REV.
D	051-7546	A.0.0
SCALE	SHT	OF
NONE	95	96

M99 Board-Specific Spacing & Physical Constraints

BOARD LAYERS				BOARD AREAS				BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM				NO_TYPE, BGA				MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	14 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP, BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.110 MM	0.095 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP, BOTTOM	Y	0.165 MM	0.095 MM			
40_OHM_SE	*	Y	0.135 MM	0.135 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP, BOTTOM	Y	0.310 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.250 MM	0.250 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3, ISL4	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL9, ISL10	Y	0.160 MM	0.160 MM		0.175 MM	0.175 MM
70_OHM_DIFF	ISL2, ISL11	Y	0.170 MM	0.170 MM		0.150 MM	0.150 MM
70_OHM_DIFF	TOP, BOTTOM	Y	0.170 MM	0.095 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3, ISL4	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9, ISL10	Y	0.125 MM	0.125 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL2, ISL11	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
80_OHM_DIFF	TOP, BOTTOM	Y	0.140 MM	0.095 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3, ISL4	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL9, ISL10	Y	0.102 MM	0.102 MM		0.220 MM	0.220 MM
90_OHM_DIFF	ISL2, ISL11	Y	0.115 MM	0.115 MM		0.230 MM	0.230 MM
90_OHM_DIFF	TOP, BOTTOM	Y	0.115 MM	0.095 MM		0.230 MM	0.230 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3, ISL4	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL9, ISL10	Y	0.080 MM	0.080 MM		0.200 MM	0.200 MM
100_OHM_DIFF	ISL2, ISL11	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM
100_OHM_DIFF	TOP, BOTTOM	Y	0.089 MM	0.089 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3, ISL4	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9, ISL10	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL2, ISL11	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP, BOTTOM	Y	0.077 MM	0.077 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
1.8:1_SPACING	*	0.18 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

NOTE: From T18 MLB, changed to reflect M99 stackup.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3, ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9, ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

PCB Rule Definitions

SYNC_MASTER=M99_MLB SYNC_DATE=01/22/2008


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	D	051-7546	A.0.0
SCALE	SHT	OF	
NONE	96	96	