3. All crystals & oscillator values are in hertz.

Part number: 820-3209

QTY: 1

SCHEM, MLB, J13

2/23/12
### BOM Variants

<table>
<thead>
<tr>
<th>BOM NUMBER</th>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>639-3795</td>
<td>607-9090</td>
<td>PCBA, MLB, 2.0GHZ, EL 4GB, J13</td>
</tr>
<tr>
<td>639-3793</td>
<td>639-3793</td>
<td>PCBA, MLB, 1.7GHZ, EL 4GB, J13</td>
</tr>
<tr>
<td>639-3792</td>
<td>639-3792</td>
<td>PCBA, MLB, 2.0GHZ, SA 8GB, J13</td>
</tr>
<tr>
<td>639-3791</td>
<td>639-3791</td>
<td>PCBA, MLB, 1.8GHZ, SA 8GB, J13</td>
</tr>
<tr>
<td>639-3790</td>
<td>639-3790</td>
<td>PCBA, MLB, 1.7GHZ, SA 8GB, J13</td>
</tr>
<tr>
<td>639-3767</td>
<td>639-3767</td>
<td>PCBA, MLB, 2.0GHZ, EL 8GB, J13</td>
</tr>
<tr>
<td>639-3766</td>
<td>639-3766</td>
<td>PCBA, MLB, 2.0GHZ, HY 4GB, J13</td>
</tr>
<tr>
<td>639-3765</td>
<td>639-3765</td>
<td>PCBA, MLB, 2.0GHZ, HY 8GB, J13</td>
</tr>
<tr>
<td>639-3764</td>
<td>639-3764</td>
<td>PCBA, MLB, 2.0GHZ, SA 4GB, J13</td>
</tr>
<tr>
<td>639-3762</td>
<td>639-3762</td>
<td>PCBA, MLB, 1.8GHZ, EL 8GB, J13</td>
</tr>
<tr>
<td>639-3760</td>
<td>639-3760</td>
<td>PCBA, MLB, 1.5GHZ, EL 8GB, J13</td>
</tr>
<tr>
<td>639-3757</td>
<td>639-3757</td>
<td>PCBA, MLB, 1.7GHZ, HY 4GB, J13</td>
</tr>
<tr>
<td>639-3755</td>
<td>639-3755</td>
<td>PCBA, MLB, 1.7GHZ, HY 8GB, J13</td>
</tr>
<tr>
<td>639-3754</td>
<td>639-3754</td>
<td>PCBA, MLB, 1.5GHZ, HY 8GB, J13</td>
</tr>
<tr>
<td>639-3557</td>
<td>639-3557</td>
<td>PCBA, MLB, 1.5GHZ, HY 4GB, J13</td>
</tr>
<tr>
<td>639-3555</td>
<td>639-3555</td>
<td>PCBA, MLB, 1.5GHZ, SA 4GB, J13</td>
</tr>
</tbody>
</table>

### Bar Code Labels / IEEE #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
<tr>
<td>825-7670</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6MM</td>
</tr>
</tbody>
</table>

### BOM Options

<table>
<thead>
<tr>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>J13_DEVEL:ENG</td>
</tr>
<tr>
<td>J13_COMMON</td>
</tr>
</tbody>
</table>

### Revision History

- **Sync Master:** J30_MLB
- **Sync Date:** 07/27/2011
- **Drawings:** 4 of 109
- **Branch:** 2.8.0
- **Sheet:** 4 of 73
### Programable Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### DRAM CFG CHART

![DRAM CFG CHART Image]

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### PC Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Therefore, an inverting level shifter is required on the motherboard.

NOTE: eDP_COMPIO and eDP_ICOMPO cannot be left floating.

Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.
Processor Load Line: \(-2.9\) mOhms
<table>
<thead>
<tr>
<th><strong>OUT</strong></th>
<th><strong>IN</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>R1855</td>
<td>R1848</td>
</tr>
<tr>
<td>R1843</td>
<td>R1814</td>
</tr>
<tr>
<td>R1833</td>
<td></td>
</tr>
</tbody>
</table>

**Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.**

1. If HDA = S0, must also ensure that signal cannot be high in S3.
2. Unused clock terminations for FCIM Mode
   - PCH_CLK100M_SATA_N
   - PCH_CLK33M_PCIIN
   - DMI_CLK100M_CPU_N
   - PCIE_CLK100M_FW_P
   - PCIE_CLK100M_FW_N

The diagram illustrates various electrical connections and terminations for a circuit, including:
- SPI_MOSI_R
- XDP_PCH_TMS
- JTAG_ISP_TMS
- TP_HDA_SDIN3
- HDA_RST_R_L
- PCH_INTVRMEN_L
- PCH_SRTCRST_L
- TP_SPI_CS1_L
- SPI_MISO
- SPI_CS0*
- JTAG_TDI
- JTAG_TCK
- ENET_MEDIA_SENSE_RDIV
- USB_EXTD_SEL_XHCI
- PEGCLKRQB_L_GPIO56
- AP_CLKREQ_L
- FW_CLKREQ_L
- PCH_SATALED_L
- INTRUDER*
- SRTCRST*
- SERIRQ
- M2
- AB12
- AJ1
- AC1
- AN6
- AN1
- Y4
- F37
- C39
- A37
- W46
- B8
- T4
- U8
- CLKOUT_ITPXDP_P
- CLKOUT_PCIE7P
- PCIECLKRQ6*/GPIO45
- CLKOUT_PCIE6P
- PCIECLKRQ4*/GPIO26
- CLKOUT_PCIE4N
- PCIECLKRQ3*/GPIO25
- PCIECLKRQ2*/GPIO20
- PERP4
- PERN3
- PERP1
- PERN1
- CL_CLK1
- CL_CLK2
- SML0CLK
- SMBALERT*/GPIO11
- SML0ALERT*/GPIO60
- SYSCLK_CLK25M_SB_R
- DOES THIS NEED LENGTH MATCH???

Additional notes and diagrams showing various components and connections are present in the image, but the text is not fully legible.
Systems with no chip-down memory should pull all & R2574 open high.
Systems with chip-down memory should add pull-up on another page and set straps per software.

NOTE: TDO from CR is Push-Pull CMOS

NOTE: TCK from PCH is Push-Pull CMOS

Table BOMGROUP HEAD

Apple Inc.

PCH GPIO/MISC/NCTF
R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to 2510 and path to non-XDP signal destination.

- R252x, R253x, R257x and R259x should be placed where signal path needs to split between route from PCH to 2510 and path to non-XDP signal destination.
- OUT: XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
- IN: XDP_CONN
- NR: NON-XDP SIGNALS
- R: R2500
- C: CPU_CFG<3>
- D: CPU_CFG<17>
- E: CPU_CFG<9>
- F: CPU_CFG<5>

**PCH Signals**

- XDP_OBSDATA_B1
- XDP_OBSDATA_B0
- XDP_OBSDATA_B3
- XDP_OBSDATA_A2
- XDP_OBSDATA_B1
- XDP_OBSDATA_C2
- XDP_OBSDATA_A0
- OBSFN_B1
- OBSFN_D1
- OBSFN_C1
- OBSFN_A0

**PCH Signals**

- XDP_PCH_TMS
- XDP_PCH_TDI
- XDP_PCH_TDO
- XDP_DBRESET_L
- XDPPCH_RETRST_L

**Non-XDP Signals**

- C2581
- TDO
- ITO
- TCK1
- XDP_PCH_TCK
- XDP_PCH_TDO

**PCB Signal Isolation Notes:**
- Following Intel's Debug PCB Design guide for MM and CN v1.1 dated 06/06.
- Initially, stuff both 23 and 0 holes and validate whether it is functional in that state, size and NOR options.
- Output - non-XDP signals require pull-up.
- Output: PCH/XDP signals require pull-up.

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
PROPRIETARY PROPERTY OF APPLE INC.
NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition.

S0 to S3 to S0 (*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

7           1              1             1            1              1          CPU_MEM_RESET_L      1          1          1
5           0              1             1            1              0 (*)             1             1          1
4           0              0             1            1              X                 1             0          1

Step  ISOLATE_CPU_MEM_L  PLT_RESET_L  PM_SLP_S3_L  PM_SLP_S4_L  CPU_MEM_RESET_L  MEM_RESET_L  MEMVTT_EN  P1V5CPU_EN

MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L
MEMVTT_EN   = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L

WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.

The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as

<p>| | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>26</td>
<td>23</td>
<td>8</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
</tbody>
</table>

26 = P5V_S3_MEMRESET
10 = 0.047UF X7R-CERM IN 0402 16V
CPUMEM_SLG: NO
2 = MEM_RESET_L
26 = PP3V3_S3_MEMRESET
100K 201 5%
R2890 201 SOT563 Q2815 1/20W SSM6N37FEAPE

62 = CPUMEM_SLG: NO
37 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO

Q2800 SSM6N37FEAPE 31 SOT563
R2802 100K 1/20W 5%
R2801 100K 1/20W 5%
C2816 X5R-CERM 0201

5 = P1V5_S3_MEMRESET
16V 10%
CPUMEM_SLG: NO
1K 201 1/20W
Q2810 SSM6N37FEAPE 3 SOT563

62 = CPUMEM_SLG: NO
37 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO
26 = CPUMEM_SLG: NO

Q2850 SSM6N37FEAPE 6 SOT563

4 = CPUMEM_SLG: NO
3 = CPUMEM_SLG: NO
2 = CPUMEM_SLG: NO
1 = CPUMEM_SLG: NO
0 = CPUMEM_SLG: NO

/NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Users will power-up or if from S1, but MEM_RESET_L will not properly power. Default must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

/NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Users will power-up or if from S1, but MEM_RESET_L will not properly power. Default must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.
SD Detect & Reset Logic

SD card detect logic converts SDCONN from active-low level signal to active-high pulses. SD detect & reset logic only function if reset logic is low.

1. SD card detect logic
2. SD detect reset logic

- SD card detect logic
- SD detect reset logic
PCIE/SATA GUMSTICK2 CONNECTOR

Per PCIe Spec, only TX side should have AC cap

GND_VOID=TRUE

VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6mm
PP3V3_S0_SSD_FLT

C4520
0.1UF
100UF
SMC_OOB1_TX_L
SMC_OOB1_RX_L
C4521
12
PCIE_SSD_D2R_N<1>
PCIE_SSD_D2R_P<1>
10%
C4503
0.1UF
10V
0201
CERM-X5R
16V

C4501
0.1UF
10V
0201
X5R-CERM
10%
C4502
0.1UF
10V
0201
X5R-CERM
10%
C4512
C4513
C4518
C4519
0.1UF
16V
0201
X5R-CERM
10%
C4514
0.1UF
16V
0201
X5R-CERM
10%

R4599
0603
1/20W
201
MF
5%
0
R4520
R4510
R4505
10K
470K
1/20W
5%
1/20W
5%

ISNS_SSD_N
ISNS_SSD_P
SATAMUX_EN_L
PP3V3_S0_SATAMUX

A1_N
A1_P
A0_P
CBTL02043ABQ
U4510
VQFN
VSS
VDD
11
20
21
THRM
PAD
C1_P
C0_N
C0_P
B1_P
B0_N
B0_P

R4500

PCIE_SSD_R2D_C_N<0>
PCIE_SSD_R2D_C_P<0>

SATA_SSD_R2D_MUX_IN_N
SATA_SSD_R2D_MUX_IN_P
PCIE_SSD_R2D_MUX_IN_N
PCIE_SSD_R2D_MUX_IN_P

SATA_SSD_D2R_MUX_OUT_N
SATA_SSD_D2R_MUX_OUT_P
PCIE_SSD_D2R_MUX_OUT_N
PCIE_SSD_D2R_MUX_OUT_P

PLACE_NEAR=J4501.1:3mm
PLACE_NEAR=U4510.6:2 mm
PLACE_NEAR=U4510.1:2 mm

SYNC_MASTER=J13_MLB_NON_POR

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
NOT TO REPRODUCE OR COPY IT
TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

IV ALL RIGHTS RESERVED
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
II NOT TO REPRODUCE OR COPY IT
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

Apple Inc.
Right USB Port A

USB Port Power Switch

Mojo SMC Debug Mux

Current limit per port (R4600): 2.18A min / 2.63A max

Mojo SMC Debug Mux
NOTE:
SMC interrupts can be active high or low, rename accordingly.
If SMI interrupt is not used, pull up to 3.3V rail.

NOTE:
Ground pins have "NC Pin" names. Unused pins designated as outputs can be left floating.
Thermal pads designated as inputs require pull-ups.
**CPU Proximity Sensor**

- **Q5510**: Place Q5510 next to DDR/5V/3.3V supply on TOP side
- **Placement note**: Detect DDR/5V/3.3V Proximity Temperature

**TBT, MLB Bottom & Inlet Proximity Sensors**

- **Q5530**: Place Q5530 between near rear vent on bottom side
- **Placement note**: Place Q5530 close to TBT on TOP side

**Replacing caps with 100K PD on ISENSE SMC inputs**

- **R5510**: Stuff R5540 & R5541, No Stuff R5550, R5551

**TBT Die**

- **Q5520**: Place Q5520 close to TBT on TOP side
- **Placement note**: Read Address: 0x99

**Thermal Sensors**

- **Q5540**: Place Q5540 on MLB bottom side opposite U5400
- **Placement note**: Write Address: 0x98

**Critical Warning**

- **I**: To maintain this document in confidence
- **II**: Not to reproduce or copy it
- **III**: Not to reveal or publish it in whole or part

**Notice of Proprietary Property**

Apple Inc. reserves all rights under copyright in this document. All information contained herein is proprietary to Apple Inc. and is provided under license for use only by authorized recipients in accordance with the terms of the license agreement. This document and anyCopy, reproduction, or disclosure to unauthorized recipients is strictly prohibited.
To detect keyboard backlight, the following conditions must be met:

1. J5815 pin 1 is grounded.
2. J5815 pin 2 is grounded.
3. J5815 pin 3 is not grounded.

If these conditions are met, the keyboard backlight is present. If not met, the keyboard backlight is not present.

Regarding the placement of components:
- Components placed near J5700.1:1.5MM: MIN_NECK_WIDTH=0.2 MM, MIN_LINE_WIDTH=0.25 MM
- Components placed near J5700.10:1.5MM: MIN_NECK_WIDTH=0.20 mm, MIN_LINE_WIDTH=0.3 MM
- Components placed near J5700.8:1.5MM: MIN_NECK_WIDTH=0.25 MM, MIN_LINE_WIDTH=0.5 mm

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
This document contains the proprietary and confidential property of Apple Inc. It is not to be reproduced or copied in whole or in part. All rights reserved.

Prohibitory Property of Apple Inc.

The information herein is the proprietary and confidential property of Apple Inc. It is not to be reproduced or copied in whole or in part. All rights reserved.

The Possessor agrees to the following:

I to maintain this document in confidence
II not to reproduce or copy it
III not to reveal or publish it in whole or part
High Speed CLK Frequency - 50MHz for fast read dual I/O

ROM will ignore SPI cycles.

NOTE: If HOLD* is asserted

=PP3V3_SUS_ROM

SPI_MLB_CLK

SPI_MLB_CS_L

SPI_WP_L

SPI_MLB_MISO

SPI_MLB_MOSI

X5R-CERM

0.1UF

16V

0201

SST25VF064C

OMIT_TABLE

64MBIT

WSON

CRITICAL

3.3K

5%

1/20W

MF

R6101

1

2

U6100

1

7

6

5

2

9

4

3

C6100

1

2

50 OF 73

61 OF 109

2.8.0

051-9277 D

60 OF 23

Apple Inc.
SPEAKER AMPLIFIERS

APD:11342686

SPEAKER LOWPASS 50 Hz < FC < 132 Hz

GAIN SUB
If LVDDR3_HW:NO is turned ON, switch R2821 & R7971 back to the original value for 1.5V DDR unless 1V5R1V35_SW is turned ON.
CPU=IV Bridge ULV, AXG=GT2
CPU VCCIO (1.05V S0) Regulator

OCP = R7641 x 8.5uA / R7640

Vout = 0.5V x (1 + Ra / Rb)

Vout = 1.05V

2A Max Output

f = 300 kHz

VSW

VIN

11V

L7630

CRITICAL

1000PF

NP0-C0G

2

1

62UF

POLY

11V

C7620

5%

12

7

72 45

72 45

R7644

3.01K

MF

1%

201

C7623

1000PF

NP0-C0G

2

1

1

2

5%

C7648

270UF

CASE-B2-SM

TANT

2V

20%

C7649

270UF

TANT

20%

6
Cougar Point requires JTAG pull-ups to be powered at 1.05V when SUS suspend well is active.

Pull-ups (3) must be 51 ohms to support XDP (not required in production).

70mA is required to support pull-ups. Alternative is strong voltage

\[
\text{Max Current} = 0.020\text{A} \\
\text{Vout} = 1.05\text{V} 
\]

\[
\text{Freq} = 1 \text{ MHz} \\
\text{Max Current} = 0.35\text{A} \\
\text{Vout} = 1.05\text{V} 
\]

\[
\text{<Ra>} \\
\text{Vout} = 0.8\text{V} \times (1 + \text{Ra} / \text{Rb}) \\
\text{Vout} = 1.794\text{V} \\
\text{Max Current} = 1.8\text{A} \\
\text{Vout} = 1.5\text{V} 
\]

\[
\text{<Rb>} \\
\text{Vout} = 1.8\text{V} \times \text{S0 Regulator} \\
\text{Max Current} = 0.02\text{A} \\
\text{Vout} = 1.05\text{V} \\
\text{Max Current} = 0.35\text{A} \\
\text{Vout} = 1.05\text{V} \times \text{S0 LDO} \\
\text{Pull-ups (3) must be 51 ohms to support XDP (not required in production).} \\
\text{70mA is required to support pull-ups. Alternative is strong voltage} \\
\text{dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.} \\
\text{1.05V S0 LDO} \\
\text{Max Current} = 0.02\text{A} \\
\text{Vout} = 1.05\text{V} \\
\text{Max Current} = 0.02\text{A} \\
\text{Vout} = 0.8\text{V} \times (1 + \text{Ra} / \text{Rb}) \\
\text{Vout} = 1.794\text{V} \\
\text{Max Current} = 1.8\text{A} \\
\text{Vout} = 1.5\text{V} \\
\text{Max Current} = 0.02\text{A} \\
\text{Vout} = 0.8\text{V} \times (1 + \text{Ra} / \text{Rb}) \\
\text{Vout} = 1.794\text{V} \\
\text{Max Current} = 1.8\text{A} \\
\text{Vout} = 1.5\text{V} 
\]
## CPU Signal Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Top Layer</th>
<th>Bottom Layer</th>
<th>Dielectric</th>
<th>Min Width</th>
<th>Min Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Top Layer</td>
<td>Bottom Layer</td>
<td>Dielectric</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
<tr>
<td>Name</td>
<td>Top Layer</td>
<td>Bottom Layer</td>
<td>Dielectric</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
<tr>
<td>Name</td>
<td>Top Layer</td>
<td>Bottom Layer</td>
<td>Dielectric</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
</tbody>
</table>

Note: DisplayPort tables are on Page 103

## PCI-Express Interface Constraints

<table>
<thead>
<tr>
<th>Name</th>
<th>Top Layer</th>
<th>Bottom Layer</th>
<th>Dielectric</th>
<th>Min Width</th>
<th>Min Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Top Layer</td>
<td>Bottom Layer</td>
<td>Dielectric</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
<tr>
<td>Name</td>
<td>Top Layer</td>
<td>Bottom Layer</td>
<td>Dielectric</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
<tr>
<td>Name</td>
<td>Top Layer</td>
<td>Bottom Layer</td>
<td>Dielectric</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
</tbody>
</table>

Note: CPU Москвы and CPU IEP can be connected back to 1/2/3/4 to 1/2/3/4

## CPU Net Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>Min Width</th>
<th>Min Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Name</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
<tr>
<td>Name</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
<tr>
<td>Name</td>
<td>Min Width</td>
<td>Min Spacing</td>
</tr>
</tbody>
</table>

Note: CPU Москва and CPU IEP can be connected back to 1/2/3/4 to 1/2/3/4

---

**Table of Contents**

- CPU Signal Constraints
- PCI-Express Interface Constraints
- CPU Net Properties

---

**Note:** DisplayPort tables are on Page 103.
### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Spacing Rule Set</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
</tr>
</tbody>
</table>

### Memory to Power Spacing

<table>
<thead>
<tr>
<th>Spacing Rule Set</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_2PWR</td>
<td>MEM_2PWR</td>
<td>MEM_2PWR</td>
<td>MEM_2PWR</td>
<td>MEM_2PWR</td>
<td>MEM_2PWR</td>
<td>MEM_2PWR</td>
</tr>
<tr>
<td>MEM_PWR</td>
<td>MEM_PWR</td>
<td>MEM_PWR</td>
<td>MEM_PWR</td>
<td>MEM_PWR</td>
<td>MEM_PWR</td>
<td>MEM_PWR</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Memory to Ground Spacing

<table>
<thead>
<tr>
<th>Spacing Rule Set</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_2GND</td>
<td>MEM_2GND</td>
<td>MEM_2GND</td>
<td>MEM_2GND</td>
<td>MEM_2GND</td>
<td>MEM_2GND</td>
<td>MEM_2GND</td>
</tr>
</tbody>
</table>

### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Spacing Rule Set</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
</tr>
</tbody>
</table>

### Memory Net Properties

<table>
<thead>
<tr>
<th>ELECTRICAL_CONSTRAINT_SET</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
<th>PHYSICAL_RULE</th>
</tr>
</thead>
<tbody>
<tr>
<td>NET_SPACING_TYPE1</td>
<td>NET_SPACING_TYPE1</td>
<td>NET_SPACING_TYPE1</td>
<td>NET_SPACING_TYPE1</td>
</tr>
<tr>
<td>NET_SPACING_TYPE2</td>
<td>NET_SPACING_TYPE2</td>
<td>NET_SPACING_TYPE2</td>
<td>NET_SPACING_TYPE2</td>
</tr>
<tr>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
<td>MEM_2OTHERMEM</td>
</tr>
<tr>
<td>MEM_CTRL2CTRL</td>
<td>MEM_CTRL2CTRL</td>
<td>MEM_CTRL2CTRL</td>
<td>MEM_CTRL2CTRL</td>
</tr>
<tr>
<td>MEM_B_DQS_3</td>
<td>MEM_B_DQS_3</td>
<td>MEM_B_DQS_3</td>
<td>MEM_B_DQS_3</td>
</tr>
<tr>
<td>MEM_B_DQS_1</td>
<td>MEM_B_DQS_1</td>
<td>MEM_B_DQS_1</td>
<td>MEM_B_DQS_1</td>
</tr>
<tr>
<td>MEM_A_DQS_6</td>
<td>MEM_A_DQS_6</td>
<td>MEM_A_DQS_6</td>
<td>MEM_A_DQS_6</td>
</tr>
<tr>
<td>MEM_A_DQS_4</td>
<td>MEM_A_DQS_4</td>
<td>MEM_A_DQS_4</td>
<td>MEM_A_DQS_4</td>
</tr>
<tr>
<td>MEM_A_DQS_3</td>
<td>MEM_A_DQS_3</td>
<td>MEM_A_DQS_3</td>
<td>MEM_A_DQS_3</td>
</tr>
<tr>
<td>MEM_A_DQS_1</td>
<td>MEM_A_DQS_1</td>
<td>MEM_A_DQS_1</td>
<td>MEM_A_DQS_1</td>
</tr>
<tr>
<td>MEM_B_DQS_3</td>
<td>MEM_B_DQS_3</td>
<td>MEM_B_DQS_3</td>
<td>MEM_B_DQS_3</td>
</tr>
<tr>
<td>MEM_B_DQS_1</td>
<td>MEM_B_DQS_1</td>
<td>MEM_B_DQS_1</td>
<td>MEM_B_DQS_1</td>
</tr>
</tbody>
</table>

### Memory to Power Spacing

- **PaSiFio Spacing**

  - "Real" Spacing

### Memory to Ground Spacing

- **DIFFPAIR NECK GAP**

### Memory Bus Spacing Group Assignments

- **TABLE_SPACING_ASSIGNMENT_ITEM**

### Memory Net Properties

- **TABLE_SPACING_ASSIGNMENT_ITEM**

### Memory Constraints

- **TABLE_SPACING_ASSIGNMENT_HEAD**

---

*NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART*

---

*NOT TO REPRODUCE OR COPY IT*

---

*NOTICE OF PROPRIETARY PROPERTY:*

---

Apple Inc. 051-5277 D
### SATA Interface Constraints

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Layer</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Reference</th>
<th>Min Line Width</th>
<th>Min Line-To-Line Spacer</th>
</tr>
</thead>
<tbody>
<tr>
<td>SATA3_PCH_TX</td>
<td>TOP</td>
<td>1</td>
<td>2</td>
<td>USB3</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>SATA3_PCH_RX</td>
<td>TOP</td>
<td>3</td>
<td>4</td>
<td>USB3</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>SATA3_2OTHER</td>
<td>TOP</td>
<td>5</td>
<td>6</td>
<td>USB3</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>SATA_80D</td>
<td>TOP</td>
<td>7</td>
<td>8</td>
<td>USB3</td>
<td>2.5x_DIELECTRIC</td>
<td>4x_DIELECTRIC</td>
</tr>
</tbody>
</table>

### USB 2.0 Interface Constraints

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Layer</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Reference</th>
<th>Min Line Width</th>
<th>Min Line-To-Line Spacer</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB_EXTB</td>
<td>TOP</td>
<td>9</td>
<td>10</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>USB_EXTB</td>
<td>TOP</td>
<td>11</td>
<td>12</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>USB_EXTD_XHCI</td>
<td>TOP</td>
<td>13</td>
<td>14</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>USB_EXTB_XHCI</td>
<td>TOP</td>
<td>15</td>
<td>16</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
</tbody>
</table>

### USB 3.0 Interface Constraints

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Layer</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Reference</th>
<th>Min Line Width</th>
<th>Min Line-To-Line Spacer</th>
</tr>
</thead>
<tbody>
<tr>
<td>USB_EXTA_N</td>
<td>TOP</td>
<td>17</td>
<td>18</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>USB_EXTA_P</td>
<td>TOP</td>
<td>19</td>
<td>20</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>USB_EXTB_N</td>
<td>TOP</td>
<td>21</td>
<td>22</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
<tr>
<td>USB_EXTB_P</td>
<td>TOP</td>
<td>23</td>
<td>24</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
</tbody>
</table>

### UART Interface Constraints

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Layer</th>
<th>Pin 1</th>
<th>Pin 2</th>
<th>Reference</th>
<th>Min Line Width</th>
<th>Min Line-To-Line Spacer</th>
</tr>
</thead>
<tbody>
<tr>
<td>UART</td>
<td>TOP</td>
<td>25</td>
<td>26</td>
<td>USB2</td>
<td>80_OHM_DIFF</td>
<td>2.5x_DIELECTRIC</td>
</tr>
</tbody>
</table>

---

**Notes:**
- For each set of constraints, the spacing rules are defined per Table 8.3 in the document. The table is not shown here for brevity.
- The spacing rules are specified in millimeters (mm) and are relevant to the particular design and application specified in the context of the design guidelines provided.
- The Reference column lists the specific reference used for the design, which may include designations such as TOP, BOTTOM, or specific layers as indicated.
- The Min Line Width and Min Line-To-Line Spacer columns specify the minimum allowed line widths and line-to-line spacing for each pair of pins specified.

---

**Source:** Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

**Proprietary Property of Apple Inc.**
DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

DisplayPort Physical/Spacing Constraints

PHYSICAL RULE SET

NET SPACING TYPE1 NET SPACING TYPE2

TBT_SPI_45S

TBTDP_80D

TBTDP_RX

TBTDP_TX

TBTDP_RX

TBTDP_TX

TBTDP_TX

TBTDP_TX

TBT_SPI

TBT_SPI_MOSI

TBT_SPI_CLK

TBT_SPI_45S

TBT_B_D2R

TBT_B_D2R_TBTDP_80D

TBT_B_R2D

TBT_B_R2D_TBTDP_80D

TBT_A_AUXCH

TBT_A_D2R

TBT_A_D2R_TBTDP_80D

TBT_A_R2D

TBT_A_R2D_TBTDP_80D

DP_TBTSRC_AUXCH_N

DP_TBTSRC_ML_C_P<3..0>

TBT_B_D2R_AUXDDC_N

DP_B_AUXCH_DDC_N

DP_B_AUXCH_DDC_P

TBT_B_D2R_P<1..0>

TBT_B_D2R_C_P<1..0>

TBT_B_R2D_P<1..0>

TBT_B_R2D_C_N<1..0>

TBT_A_D2R_AUXDDC_P

DP_A_AUXCH_DDC_N

DP_A_AUXCH_DDC_P

TBT_A_D2R1_AUXDDC_P

DP_TBTPB_ML_C_N<3..1:2>

DP_TBTPB_ML_C_P<3..1:2>

TBT_A_D2R_N<0>

TBT_A_D2R_P<0>

TBT_A_D2R_P<1>

TBT_A_D2R_C_N<1..0>

TBT_A_R2D_N<1..0>

TBT_A_R2D_P<1..0>

TBT_A_R2D_C_N<1..0>

TBT_A_R2D_C_P<1..0>

DP_TBTPA_ML_N<3..1:2>

DP_TBTPA_ML_C_N<3>

DP_TBTPA_ML_C_P<3>

DP_TBTPA_ML_C_N<1>

DP_TBTPA_ML_C_P<1>

TBT_A_R2D_C_N<1..0>

TBT_A_R2D_C_P<1..0>

DP_TBTPA_AUXCH_C_N

DP_TBTPA_AUXCH_C_P

DP_TBTPA_AUXCH_N

DP_TBTPA_AUXCH_P

Only used on hosts supporting Thunderbolt video-in

Thunderbolt/DP Net Properties

ELECTRICAL CONSTRAINTS

PHYSICAL

RESISTANCE=80_OHM_DIFF

MAXIMUM NECK LENGTH=6x_DIELECTRIC

MINIMUM NECK WIDTH=4x_DIELECTRIC

MINIMUM LINE WIDTH=2x_DIELECTRIC
### Single-ended Physical Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Rule Set</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>PHYSICAL_RULE_SET</td>
<td>0.125 MM</td>
<td>0.155 MM</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>PHYSICAL_RULE_SET</td>
<td>0.125 MM</td>
<td>0.155 MM</td>
</tr>
</tbody>
</table>

### Differential Pair Physical Constraints

<table>
<thead>
<tr>
<th>Layer</th>
<th>Rule Set</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>PHYSICAL_RULE_SET</td>
<td>0.125 MM</td>
<td>0.155 MM</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>PHYSICAL_RULE_SET</td>
<td>0.125 MM</td>
<td>0.155 MM</td>
</tr>
</tbody>
</table>

### Spacing Constraints

<table>
<thead>
<tr>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_PCIE</td>
<td>BGA_P2MM</td>
</tr>
</tbody>
</table>

### PCB Rule Definitions

- **PHYSICAL_RULE_SET**
- **SPACING_RULE_SET**
- **SPACING_ASSIGNMENT**

---

**Notice of Proprietary Property:**

This document contains confidential and proprietary information of Apple Inc. The holder of this document is advised that unauthorized reproduction or disclosure of this document is a violation of federal law and the holder assumes all risk of such unauthorized reproduction or disclosure. The holder of this document is further advised that all rights to its contents are reserved. The holder of this document agrees to hold Apple Inc. harmless from any and all claims, demands, or actions that may be asserted in connection with or arising out of the holder's possession or use of this document. All rights to this document are reserved by Apple Inc. Violation of the copyright is a violation of the law, subject to criminal and civil penalties.