THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING:

I. NOT TO REPRODUCE OR COPY IT
II. NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III. TO MAINTAIN THE DOCUMENT IN CONFIDENCE

Revision History

- 05/05/09: Added 128S0264 (SANYO) as alternate to 128S0257 (KEMET ELEC) per Radar# 6656624.
- 06/15/09: Added 107S0136 (DALE/VISHAY) as alternate to 107S0132 (CYNTEC) per Radar# 6971400.
- For U7871 P/N 353S2718 is made primary. P/N 353S2310 is added back as alternate.
- For Chill Locked ROM ROM 353S25185 replaces existing Unlock ROM P/N 353S2517.

- 04/29/09: Production Release Fab to rev A
- csa.9: Added PBUS VS 5V voltage selection resistors for keyboard backlight driver.
- csa.5: Changed K20A EFI ROM APN 341S2507 (BOM change only)
- csa.1: Changed rev to 1.0.0
- csa.0: Project copied from K20 mlb_pvt.
- Project released release 0 rev A
- csa.0: Changed kbd layout per Radar# 6723272.
- csa.70: No stuff 07399 per Radar# 672095.
- csa.138: Changed kbd layout per Radar# 672095.
- csa.9: No stuff 07399 per Radar# 672095.
- csa.138: Changed kbd layout per Radar# 672095.
- csa.9: No stuff 07399 per Radar# 672095.
- csa.5: Project copied from K20 mlb_pvt.
### BOM Variants

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PART NAME</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>639-0172</td>
<td>Module</td>
<td></td>
</tr>
<tr>
<td>639-0173</td>
<td>Module</td>
<td></td>
</tr>
<tr>
<td>639-0174</td>
<td>Module</td>
<td></td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PART NAME</th>
<th>BOM OPTIONS</th>
<th>BOM OPTIONS</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Folsten BOM GROUPS

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PART NAME</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>639-0172</td>
<td>Module</td>
<td></td>
</tr>
<tr>
<td>639-0173</td>
<td>Module</td>
<td></td>
</tr>
<tr>
<td>639-0174</td>
<td>Module</td>
<td></td>
</tr>
</tbody>
</table>

### Bar Code Labels / EEE #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### BOM Configuration

[Diagram of BOM Configuration]

---

**COMMENTS:**

- TI alt to National
- Inductor alternate
- Apple Inc.

**SCALE:**

- NONE

**SIZE:**

- D

**REV.:**

- B

**SYNC_DATE:**

- 04/01/2008

---

**II NOT TO REPRODUCE OR COPY IT TO MAINTAIN THE DOCUMENT IN CONFIDENCE PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR OF THIS DOCUMENT MUST NOT LEAVE ITS POSSESSION OR COPY IT WITHOUT THE EXPRESS WRITTEN CONSENT OF APPLE INC.**
1.05V TO 3.3V LEVEL TRANSLATOR (M98: ON ICT FIXTURE)

From XDP connector

U1000 CPU

To XDP connector

and/or level translator

From XDP connector

or via level translator

U1400 MCP

U8000 GPU

U9600 GMUX

PLACEMENT_NOTE=Place close to U0600

MAKE_BASE=TRUE

MATCHMENT_NOTE=Place near pin 81100.101

XDP_TDO_CONN

TP_GPU_JTAG_TDO

TP_GPU_JTAG_TMS

TP_GPU_JTAG_TDI

TP_GPU_JTAG_TCK

TP_JTAG_MCP_TDO

TP_JTAG_MCP_TMS

TP_JTAG_MCP_TDI

TP_JTAG_MCP_TCK

TP_JTAG_GMUX_TDO

TP_JTAG_GMUX_TDI

TP_JTAG_GMUX_TMS

TP_JTAG_ALLDEV

From XDP connector

or via level translator

10K 5%

0.1UF CERM

20%

www.vinafix.vn
PLACEMENT_NOTE: Place R1024 near ITP connector (if present)
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
See with XDP-320 adapter board to support CPU, XDP debugging.

MCP79-specific pinout

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300

Direction of XDP module

Use with 920-0620 adapter board to support CPU, MCP debugging.

Direction of XDP module

MCP79-specific pinout

NOTE: This is not the standard XDP pinout.
Current numbers from email Poonacha Kongetira provided 11/30/2007 4:04pm (no official document number).

Minimum 1.025V for Gen2 support

OUT
IN

8mA (A01)
1/16W
MF-LF

www.vinafix.vn
results in earlier ROMSIP and MCP FSB I/O interface initialization.
but results in MCP79 ROMSIP sequence happening after CPU powers up.
MCPSEQ_MIX is cross between MLB and internal power sequencing, which
NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.
VR_PWRGOOD_DELAY should guarantee CPU_VLD does not go high before
MCP_CLK25M_XTALIN

RTC Power Sources

RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

Reset Button

Platform Reset Connections

PCIE Reset (Unbuffered)

LPC Reset (Unbuffered)

RTC Power Sources

RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

Reset Button

Platform Reset Connections

PCIE Reset (Unbuffered)

LPC Reset (Unbuffered)

RTC Power Sources

RTC Crystal

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

Reset Button

Platform Reset Connections

PCIE Reset (Unbuffered)

LPC Reset (Unbuffered)
MCP cannot control this signal directly since it must be high in sleep and MEM rails are not powered in sleep.

Before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

$$M_{MEM\_RESET\_L} = PP_{1V5\_S3\_MEMRESET}$$

MEM_RESET_RC_L

$$M_{MEM\_RESET\_L} = PP_{3V3\_S5\_MEMRESET}$$

DDR3 Support

SYNC_DATE=04/01/2008

SYNC_MASTER=M98_MLB

29 98

B 051-8071

R3301 1\% 20K

MEMRESET_HW

SOT-363-LF

MMDT3904-X-G

Q3305

MEMRESET_HW

SOT-363-LF

MMDT3904-X-G

R3305 1\% 20K

MEMRESET_HW

SOT-363-LF

MMDT3904-X-G

R3309 MEMRESET_MCP

SOT-363-LF

MMDT3904-X-G

R3310 1\% 1K

MEMRESET_HW

SOT-363-LF

MMDT3904-X-G
**WLAN Enable Generation**

\[\text{WLAN} = (\text{S3} \land \text{AP_PWR_EN} \land (\text{AC} \lor \text{S0}))\]

**RTL8211 25MHz Clock**

Note: AP790 can provide 25MHz clock, but slight rate aberrations may occur.

\[\text{RTL8211}_{\text{CLK25M}} = \text{RTL8211}_{\text{CLK25M}}\]

**3.3V ENET FET**

\[\text{P3V3ENET_EN} = \text{P1V05ENET_EN} \land \text{PP3V3_S5} \land \text{PP3V3_S5_P1V05ENETFET}\]

**1.05V ENET FET**

\[\text{P3V3ENET_EN} = \text{P1V05ENET_EN} \land \text{PP3V3_S5} \land \text{PP3V3_S5_P1V05ENETFET}\]

Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm

Transformers should be placed on opposite sides of the board so there are no stubs all 8 caps.
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designated as input require pull-ups.

---

NOTE: Pins 201 and 205 are omitted. Pin 205 would be omitted.

---

NOTE: Some inputs can be active high or low, commence accordingly. If pin is not used, pull to GND or VCC.
Alternate SPI ROM Support

SEL HIGH OUTPUTS TO D (ON BOARD ROM)
SEL LOW OUTPUTS TO N (FRANKCARD ROM)

MCP SPI Override Options

MCP79 Internal SPI MUX Support

NOT SUPPORTED IN REV A01 OR B01 MCP79 SILICON

SPI MUX BYPASS
MM51214 has gain of 100V/V
US303 only senses current up to 6.6A

Consider MM211 (GAIN 500 version) since I=4.93 Amps across R5396
Detect Right Fin Stack Temperature

Placement note:
Close to right fin stack
Place Q5501 on bottom side

SOT732-3

Detect MCP Die Temperature

SIGNAL_MODEL=EMPTY

MF-LF
1/16W
402
5%

C5590
SOT732-3

Detect GPU Die Temperature

MIN_NECK_WIDTH=0.25 mm

MIN_LINE_WIDTH=0.25 mm

PP3V3_S0_CPUTHMSNS_R
CERM

Keep 2 caps as close to IC pins as possible

NOTE: U5500 Changed to EMC1403-2. Write Address: 0x9A

CRITICAL
DN2/DP3
DP2/DN3
DN1

SMDATA
ALERT*

THERM*

SMCLK
Digital SMS

Pull-up required if SMS_INT_L not used.

- R5931 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

Pull-up required if SMS_INT_L not used.

- SMS_INT_L

IN = PP3V3_S5_SMC

SMS_ONOFF_L

R5921

= PP3V3_S3_SMS

NoStuff R5931 AND Stuff R5932 if U5930 is not used

Stuff R5931 AND NoStuff R5932 to use U5930

PROD_DIGSMS

R5921

MF-LF

1/16W

5%

R5931

402

MF-LF

1/16W

5%

R5932

10K

5%

= I2C_SMS_SDA

= I2C_SMS_SCL

NC

NC

NC

NC

Digital SMS

R5921 PULLS UP SMS_PWRDN TO TURN OFF SMS WHEN PIN IS NOT BEING DRIVEN BY SMC

U5920

AP344ALH

SYNC_MASTER=YWU_K20

NOTICE OF PROPRIETARY PROPERTY

The information contained herein is the proprietary property of the Manufacturer.

It is intended for use of Manufacturer unless otherwise stated in the Agreement.

It is not to be reproduced or disclosed in whole or part without Manufacturer's written permission.

APPLE INC.

SYNC_DATE=06/17/2008

SIZE

SCALE

DRAWING NUMBER

OF

REV.

SHT

051-8071

D

C

B

A

www.vinafix.vn
The diagram shows a SPI ROM configuration with various components labeled and connected. The labels include:

- **C6100** - 0.1UF 10V CERM 402 20%
- **R6101** - 1/16W 5% 3.3K MF-LF 402 2
- **R6100** - 402 2 3.3K MF-LF 5%
- **R6190** - NO STUFF 402 0
- **R6191** - NO STUFF 402 0
- **R6150** - MF-LF 5% 1/16W 10K
- **R6152** - MF-LF 5% 1/16W 0
- **R6105** - MF-LF 5% 1/16W 0

The table indicates the SPI frequency select options:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>16 MHz</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>8 MHz</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>4 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

The diagram also includes a note to place R6150 and R6152 close to U6100 and R6190 and R6191 close to U6100.

The notice of proprietary property is present, indicating that the information is the proprietary property of Apple, Inc., and cannot be reproduced, copied, or published in whole or part without the consent of Apple, Inc.

www.vinafix.vn
Pseudo-Diff Line-In Filter

GAIN = -5.4 DB  AV = 0.52
FC = 1.89 HZ
Headphone Amplifier (MAX9724A)
APN:353S1637

1st Order DAC Filter
HP:3.52 Hz LP:34 kHz
VOLTAGE GAIN:1.53
MagSafe DC Power Jack

1-Wire OverVoltage Protection

Battery Connector

BIL Connector

3.425V "G3Hot" Supply

Supply needs to guarantee 3.1V delivered to G3Hot generator

DC-In & Battery Connectors

www.vinafix.vn
PLACEMENT_NOTE=PLACE XW7222 NEXT TO L7220.

C7271
C7250
X5R
20%

R7221
R7220
10K
1%

PATH=I623
1%

C7240
16V
33UF

XW7222
SM
603

RJK0305DPB

C7299
402
50V

CRITICAL

5
D
G

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
MCP79 DDR FETs

MCP79 DDR pad leakage is high enough that Nvidia recommends unpowering during sleep. In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low at all times. MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep. 

In order to support unpowering rail, hardware must guarantee MEM_CKE signals are low at all times. MCP79 DDR pad leakage is high enough that nVidia recommends unpowering during sleep.
Nvidia PRD for GB-128 uses 4x4.7uF, 8x0.47uF, 16x0.1uF = PP1V8_GPU_FBVDDQ

???A @ ???/???MHz Core/Mem Clk for VDD

???B @ ???/???MHz Core/Mem Clk for VDD
3.5A MAX OUTPUT

Vout = 1.103V

R9520 402 402 1% MF-LF 1/16W

XW9515 1

C9515 SM 20%

100PF

CERM 50V

330UF CRITICAL

B2-SM 20% POLY-TANT 5%

(Rb should be between 10K and 100K)

Vout = 0.7V \times \left(1 + \frac{R_a}{R_b}\right)

PCMB065T-SM

CRITICAL CASED2E-SM

L9510 POLY-TANT 33UF

76 67 66

C9545 PWRPK-1212-8-HF 1UF X5R 25V 603-1

SI7110DN PWRPK-1212-8-HF CRITICAL SI7108DN CRITICAL

Q9515

D G 4 G

P1V1GPU_DRVH MIN_LINE_WIDTH=0.6MM GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2MM

P1V1GPU_PGOOD

P1V1GPU_VFB P1V1GPU_TRIP

PVIN_S0GPU_P1V1

C9500 10UF 805 2

C9501 2 12 11 10 17 6

10% TON ILIM1 FB1 EN1 BOOT1 VIN EN_LDO LGATE1 UGATE1

ISL6236 U9500 OMIT VCC QFN 3

XW9500 22

VOLTAGE=5V

MIN_NECK_WIDTH=0.2 MM MIN_LINE_WIDTH=0.5 MM MIN_LINE_WIDTH=0.5 MM

REFIN2 LGATE2 UGATE2 ILIM2

P1V8FB_TRIP (=PP1V8FB_S0_REG)

VOLTAGE=2V

C9585 0.1UF

C9590 1% 2

R9564 2

<Ra>

127K 1/16W MF-LF 402

127K 1/16W MF-LF 402 1%

R9562 402 402 1% MF-LF 1%

C9561 1 402 16V 10%

C9565 603 1UF X5R 50V 10% 2

C9580 X7R 603

GPUFB_VID_L R9563

<Ra>

127K 1/16W MF-LF 402

127K 1/16W MF-LF 402 1%

R9562 402 402 1% MF-LF 1%

C9561 1 402 16V 10%

C9565 603 1UF X5R 50V 10% 2

C9580 X7R 603

GPUFB_VID_L R9563

www.vinafix.vn
FDC638APZ
43 mOhm @4.5V
0.4 A (EDP)
P-TYPE
MOSFET
LOADING
CHANNEL
PPBUS_S0_LCDBKLT_FET
PPBUS_S0_LCDBKLT_EN_L
BKLT_EN_L
PPBUS_S0_LCDBKLT_PWR
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=6V
PPBUS_S0_LCDBKLT_EN_DIV
PPBUS_S0_LCDBKLT_FUSED
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.375 MM
VOLTAGE=6V
LVDS_BKL_ON=PPBUS_S0_LCDBKLT
BKLT_PLT_RST_L
SYNC_DATE=07/18/2008
SYNC_MASTER=YLEE_K20
LCD Backlight Support
www.vinafix.vn
**FSB (Front-Side Bus) Constraints**

<table>
<thead>
<tr>
<th>Signal Type</th>
<th>Layer</th>
<th>Min. Line Width</th>
<th>Min. Neck Width</th>
<th>Line-To-Line Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_ITP</td>
<td>LAYER</td>
<td></td>
<td></td>
<td>3x_DIELECTRIC</td>
</tr>
<tr>
<td>CPU_BSEL</td>
<td></td>
<td></td>
<td></td>
<td>4x_DIELECTRIC</td>
</tr>
<tr>
<td>CPU_IERR_L</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_NMI</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_COMP&lt;0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_DPSLP_L</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_IGNNE_L</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CPU / FSB Net Properties**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Clock Speed</th>
<th>Rise/Fall Time</th>
<th>Propagation Delay</th>
</tr>
</thead>
<tbody>
<tr>
<td>FSB_CLK_CPU_N</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_ITP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_100D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_100S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_50S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FSB_CLK_27P4S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_50S</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CPU_AGTL</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CPU/FSB Constraints**

- **SCALE**: NONE
- **CPU Clocks**: CPU Clocks require 2:1 Line Signal-Size Expansion. For each clock, each signal requires a minimum of 2:1 line size expansion for the clock.
**CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 140 ps.**

DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

**DDR3:**
No DQS to clock matching requirement.

---

**Memory Bus Constraints**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Memory Bus Spacing Group Assignments**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Memory Net Properties**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**MCP MEM COMP Signal Constraints**

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Memory Constraints**

**NOTICE OF PROPRIETARY PROPERTY**

This data sheet contains proprietary property protected by the copyright laws of the United States and international treaty provisions. It is furnished to you for information purposes only, and no part of it may be reproduced, translated, or utilized in any form or by any means without the express written consent of Apple Inc. You are hereby licensed to use this data sheet in connection with the purchase, ownership, or operation of an Apple product, provided that you agree to use such data sheet only for such purpose. Copyright © 2008 Apple Inc. All rights reserved.
Analog Video Signal Constraints

Digital Video Signal Constraints

SATA Interface Constraints

PCI-Express

MCP Constraints 1

Note of Proprietary Property

No portion of this document may be reproduced in any form without the written consent of Apple, Inc.

I Do Not Own the Document or Any Part of It.
### SMBus Charger Net Properties

<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>SPACING</th>
<th>PHYSICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSI</td>
<td>0.1 MM</td>
<td>STANDARD</td>
</tr>
<tr>
<td>CHGR_CSI_P</td>
<td>0.1 MM</td>
<td>STANDARD</td>
</tr>
<tr>
<td>CHGR_CSI_N</td>
<td>0.1 MM</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

### SMBus Net Properties

<table>
<thead>
<tr>
<th>NET_TYPE</th>
<th>SPACING</th>
<th>PHYSICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMB_55S</td>
<td>60</td>
<td>60</td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SCL</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_BSA_SDA</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SDA</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_0_S0_SDA</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>44</td>
<td>44</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>44</td>
<td>44</td>
</tr>
</tbody>
</table>

### SMB Constraints

- SMBus Charger Net Properties
- SMBus Net Properties

**NOTICE OF PROPRIETARY PROPERTY**

The information contained herein is the proprietary property of APPLE COMPUTER, INC. The possessor agrees to the following:

I. To maintain the document in confidence.
II. Not to reproduce or copy it.
III. Not to reveal or publish in whole or part.

**SYNC_DATE=04/01/2008**
**SYNC_MASTER=M98_MLB**
**DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.**

**GDDR3 Frame Buffer Signal Constraints**

- **Max length of LVDS/DisplayPort/TMDS traces**: 12 inches.

**Physical Rule Set**

- **Spacing Rule Set**
  - **DisplayPort**
  - **GDDR3**
  - **LVDS_100D**

**Layer**

- **Line-to-line spacing**
  - **LVDS_A_CLK**
  - **LVDS_B_DATA**
  - **LVDS_A_DATA**
  - **LVDS_100D**
  - **LVDS_100D**
  - **LVDS_100D**
  - **LVDS_100D**

**Weight**

- **DP_100D**
  - **LVDS_100D**
  - **LVDS_100D**
  - **LVDS_100D**
  - **LVDS_100D**

**Electrical Constraint Set**

- **Minimum neck width**
  - **LVDS_CONN_B_DATA_N<2..0>**
  - **DP_ML_N<3..0>**
  - **DP_ML_P<3..0>**
  - **LVDS_B_CLK_N**
  - **LVDS_A_CLK_P**

- **Maximum neck length**
  - **FB_A_CLK_P**
  - **FB_A_DQM_L<7>**
  - **FB_B_DQM_L<7>**
  - **FB_B_DQM_L<5>**
  - **FB_B_DQM_L<4>**

**Table Spacing Rule Item**

- **Minimum neck width**
  - **LVDS_100D**
  - **LVDS_100D**
  - **LVDS_100D**
  - **LVDS_100D**

- **Maximum neck length**
  - **FB_A_CLK_P**
  - **FB_A_DQM_L<7>**
  - **FB_B_DQM_L<7>**
  - **FB_B_DQM_L<5>**
  - **FB_B_DQM_L<4>**

**Table Physical Rule Item**

- **Minimum neck width**
  - **LVDS_CONN_B_DATA_N<2..0>**
  - **DP_ML_N<3..0>**
  - **DP_ML_P<3..0>**
  - **LVDS_B_CLK_N**
  - **LVDS_A_CLK_P**

- **Maximum neck length**
  - **FB_A_CLK_P**
  - **FB_A_DQM_L<7>**
  - **FB_B_DQM_L<7>**
  - **FB_B_DQM_L<5>**
  - **FB_B_DQM_L<4>**
### PHYSICAL RULE SET

Ground-referenced memory signals (DQ,DQM,DQS) MAY route on ISL9 (VDD-referenced plane) but not next to VDD island.

### SPACING RULE SET

#### SENSE_1TO1_55S
- **MEM_P70D_VDD**
- **MEM_P40S_VDD**
- **MEM_CLK**
- **THERM**
- **SENSE**

#### OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE
- OVERRIDE

### AREA_TYPE

#### TOP
- GND
- GND
- GND
- GND

### LINE-TO-LINE SPACING

#### ON LAYER?
- =1:1_DIFFPAIR
- =2:1_SPACING

### MINIMUM LINE WIDTH

- 1000

### TABLE_SPACING_RULE_ITEM

- TABLE_SPACING_ASSIGNMENT_ITEM

### TABLE_PHYSICAL_RULE_ITEM

- TABLE_PHYSICAL_RULE_HEAD
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM
- TABLE_PHYSICAL_RULE_ITEM

### Graphics, SATA Constraint Relaxations

### Memory Constraint Relaxations

- Align 0.15m m space for 3.357 mm lanes for 4x4M lanes.

---

*www.vinafix.vn*
PHYSICAL RULE SET

<table>
<thead>
<tr>
<th>110_OHM_DIFF</th>
<th>ISL9, ISL10</th>
<th>TOP, BOTTOM</th>
<th>TOP, BOTTOM</th>
<th>ISL3, ISL4</th>
<th>ISL2, ISL11</th>
<th>TOP, BOTTOM</th>
<th>LAYER</th>
<th>LAYER</th>
<th>LAYER</th>
<th>LAYER</th>
<th>LAYER</th>
<th>LAYER</th>
</tr>
</thead>
<tbody>
<tr>
<td>110_OHM_DIFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100_OHM_DIFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>90_OHM_DIFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>80_OHM_DIFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>70_OHM_DIFF</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>55_OHM_SE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>55_OHM_SE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ALLOW ROUTE ON LAYER?

Y: Allow route on layer
N: Do not allow route on layer

MINIMUM LINE WIDTH

=50_OHM_SE =STANDARD =STANDARD

=0.089 MM 0.089 MM

=0.115 MM 0.115 MM

=0.140 MM 0.140 MM

=0.250 MM 0.250 MM

MINIMUM NECK WIDTH

=STANDARD

=0.077 MM 0.077 MM

=0.080 MM 0.080 MM

=0.095 MM 0.095 MM

MAXIMUM NECK LENGTH

=STANDARD

=10 MM

=NO_TYPE, BGA

DIFFPAIR PRIMARY GAP

=STANDARD

=0.200 MM 0.200 MM

=0.230 MM 0.230 MM

=0.150 MM 0.150 MM

DIFFPAIR NECK GAP

=STANDARD

=0.200 MM 0.200 MM

=0.190 MM 0.190 MM

=0.180 MM 0.180 MM

DIFFPAIR NECK GAP

=STANDARD

=0.200 MM 0.200 MM

=0.190 MM 0.190 MM

=0.180 MM 0.180 MM

DIFFPAIR NECK GAP

=STANDARD

=0.200 MM 0.200 MM

=0.190 MM 0.190 MM

=0.180 MM 0.180 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: From T18 MLB, changed to reflect M99 stackup.

www.vinafix.vn
Port Power Switch

LEFT USB PORT C

---

**Notice of Proprietary Property**

No license is granted under this document. Written permission is required to reproduce or to otherwise use this document. Use of this document in whole or part is strictly prohibited. The information contained herein is the proprietary property of Apple Computer, Inc. The possessor agrees to the following:

I. Not to reproduce or copy it
II. Not to reveal or publish in whole or part
III. To maintain the document in confidence.

---

**PROJECT SPECIFIC CONNS**

---

**TABLE**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DESC</th>
<th>CRITICAL</th>
<th>REV OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>