3. All crystals & oscillator values are in Hertz.
### BOM Variants

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>YES_DBG</td>
<td>XDP,XDP_CONN,XDP_CPU_BPM,MOJOMUX</td>
<td>YES</td>
<td>LPCPLUS</td>
<td>YES</td>
</tr>
<tr>
<td>BASIC2</td>
<td>AP,BT,IR,T29</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BASIC1</td>
<td>COMMON,ALTERNATE,MXM,FCIM,CPU_1V5_SENSE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DEV_GROUP</td>
<td>VREFMRGN_A,VREFMRGN_B,DIMM_1V5_SENSE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NO_DBG</td>
<td>MOJOMUX</td>
<td>NO</td>
<td>LPCPLUS</td>
<td>NO</td>
</tr>
</tbody>
</table>

### BOM GROUPS

<table>
<thead>
<tr>
<th>BOM GROUP</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>604-1161</td>
<td></td>
</tr>
</tbody>
</table>

### CPU SOCKET & ILM SUB-BOMS

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1000</td>
<td>MOLEX_SOCKET</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILM604-1474</td>
<td>TYCO_SOCKET_ASSY, PURCHASED, ILM, TYCO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CRITICAL</td>
<td>BOM OPTION</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### COMMON

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>K60,2P8GHZ_SNB_CPU_PRQ</td>
<td>BASIC1, BASIC2, CPUVCORE-3PH, ODD_SATA: P1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### CPUS

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T29</td>
<td>SERIAL EEPROM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### K60 PARTS

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<thead>
<tr>
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<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T29</td>
<td>SERIAL EEPROM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFLASH_ENET_2MBIT,CIV</td>
<td>341T0328</td>
<td>CRITICAL1</td>
<td></td>
</tr>
</tbody>
</table>

### K60 ALTERNATE PARTS

<table>
<thead>
<tr>
<th>PART#</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>REFERENCE DESIGNATOR(S)</th>
</tr>
</thead>
<tbody>
<tr>
<td>T29</td>
<td>SERIAL EEPROM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFLASH_ENET_2MBIT,CIV</td>
<td>341T0328</td>
<td>CRITICAL1</td>
<td></td>
</tr>
</tbody>
</table>

### BOARD STACK-UP

<table>
<thead>
<tr>
<th>SIGNAL</th>
<th>GROUND</th>
<th>POWER</th>
<th>SIGNAL</th>
<th>GROUND</th>
<th>POWER</th>
<th>SIGNAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>SIGNAL</td>
<td>GROUND</td>
<td>SIGNAL</td>
<td>GROUND</td>
<td>POWER</td>
<td>SIGNAL</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>SIGNAL</td>
<td>GROUND</td>
<td>POWER</td>
<td>SIGNAL</td>
<td>GROUND</td>
<td>POWER</td>
</tr>
</tbody>
</table>
S5 Led

ALL_SYS_PWRGD Led

MXM PWR GOOD Led

VIDEO ON Led

PROTO DEBUG LEDS ARE SHOWN BELOW
CPU VCORE DECOUPLING

- 16x 22uF, 0805 INTEL RECOMMENDATION for 220W 0805 (14 inside cavity and 4 North of processor)

- Place inside socket cavity

CPU VCCIO DECOUPLING

- 8x 22uF, 0805 INTEL RECOMMENDATION 8x 22uF 0805, 16x 0805 placeholders

- Place under socket cavity on secondary side

- INTEL RECOMMENDATION 9x 22uF 0805

- Place at edge of socket.

- Place inside socket cavity

- Place inside socket cavity

- Place inside socket cavity

- Place inside socket cavity

- Place inside socket cavity

- Place inside socket cavity

- Place inside socket cavity

PLACEMENT NOTE (C1600-C1613):
14x 22UF, 0805 INTEL RECOMMENDATION 18x 22UF 0805 (14 Inside cavity and 4 North of processor)

PLACEMENT NOTE (C1660-C1665):
Place under socket cavity on secondary side.

8X 22UF 0805, 6X 10UF 0805

CPU VCCIO DECOUPLING

- 22uF 6.3V 20%

- Place inside socket cavity

PLL (CPU VCCSFR) DECOUPLING

- 2x 47uF, 1x 22uF 0805, 1x 10uF 0805, 1x 4.7uF 0603, 1x 2.2uF 0603, 2x 1uF 0802, 2x 1uF 0802. INTEL RECOMMENDATION 10x 10uF 0805

- Place inside socket cavity

Note: VCCSA decoupling is on regulator page
PLACE THE RESISTOR VERY CLOSE TO COMMON POINT

SHORT THESE TWO PINS VERY NEAR THE PINS

TOTAL_ETCH_LENGTH=5 MM

SYSTEM POWER MANAGEMENT

CPU_PROC_SEL

PCH DMI/FDI/GRAPHICS

Apple Inc.
DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL A DIMM CONNECTOR

DECOUPLING CAPS FOR 1V5_S3_MEM AT CHANNEL B DIMM CONNECTOR

EXTRA DECOUPLING CAPS FOR 1V5_CPU_MEM RAIL

DIMM A (CLOSER TO CPU)  CAPS TO STITCH 1V5_CPU_MEM TO GND NEAR DIMM  DIMM B (FURTHER FROM CPU)

MEMORY CAPS

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I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
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SNB? CANNOT CONTROL THIS SIGNAL DIRECTLY SINCE IT MUST BE HIGH IN SLEEP AND CPU MEM RAILS ARE NOT POWERED IN SLEEP.
THIS PAGE DIFFERENT BETWEEN K60 and K62.
FW643 1.0V GENERATION

1394 PHY DATA/STROBE OPTIONS

2ND & 3RD TPA/TPB PAIR UNUSED

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

There are three firewire ports, but only one is used. The data strobe only mode, pull-ups are internal, long pull-downs, only pull-ups required.

NOTE: Q4200 collector connect to caps with 0.4 sq-in heat sink

NOTE: MULTIPLE VIAS TO DGND

Termination
Place close to FireWire PHY

FireWire: 1394B MISC

Apple Inc. 051-8115 11.1.0

BOM OPTION OPTIONS FOR SATA PORT A1 AND A2

SILKSCREEN:SATA0

SILKSCREEN:SATA1

SILKSCREEN:SATA2

SATA Port A0 for HDD

SATA Port A1 for SSD/ODD

SATA Port A2 for ODD

SATA Activity LED

HDD Power

SSD Power

ODD PWR CONTROL

SATA Connectors

Apple Inc. 051-8115 11.1.0

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IR RECEIVER CONNECTOR

SD Card Reader Board ( Lazarus )

CAMERA/ALS & BLUETOOTH (K37A) CONNECTOR

Skin Temp sense at upper Left Screen corner

Internal USB Connections
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

SDCONN DETECT DEBOUNCE, INVERSION, AND DETECT-CHANGED PCH GPIO CIRCUIT

SD CARD CONNECTOR

SD READER CONNECTOR
LPC+SPI Connector

Alternate SPI ROM Support

SPI Bus Series Resistance Option

Apple Inc.

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HDD OOB TEMPERATURE SENSING

Note: Will be connected to Data for connection for 11

Use HDD OOB for orientation of immediate derate (25%)

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Sync_master=K62
Sync_date=01/06/2011

HDD OOB sense = PP12V_S0_Sense
= PP3V3_S0_SMC_LS
SMC_HDD_OOB_TEMP
HDD_OOB_TEMP_FILT
HDD_OOB_1V00_REF
= PP3V3_S0_SMC_LS
HDD_OOB_1V00_REF
HDD_OOB_TEMP_R

Pull up 1.5V.
Trip point 1.0V.

Drive Active = valid signal protocol between 0-2.0V.

High: 1.2V to 2.0V

Drive Absent = OOB is pulled high unless PCH determines SSD present and drives USE_HDD_OOB_L low which then pulls HDD_OOB_TEMP low.

Low: 0.0V to 0.3V

Pull down 0.0V.
Trip point 0.5V.

Drive Asleep = HDD Drives HDD_OOB_TEMP low.

Both functions not used.
R & L CHANNELS SWAPPED TO MAKE LAYOUT MORE LOGICAL

CODEC REN SE RIN = 20K OHMS
EN = 3.62 MS
CODEC VIN = 1.14 VRMS
RIN RIN 1.14 OHMS

VIN = 2VRMS, CODEC VIN = 1.14 VRMS

MIN LINE WIDTH=.3MM
MIN NECK WIDTH=.2MM
MIN LINE WIDTH=0.5MM
MIN NECK WIDTH=0.2MM
MIN LINE WIDTH=0.5MM
3.425V "G3Hot" Supply
Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V * (1 + Ra / Rb)

Vout = 3.425
250mA max output
(Switcher limit)

R7911 = 2.1K
C7910 = 10UF X5R 10%
25V

C7900 = 6.3V20%
402X5R
0.22UF
21
L7900 = 33UH CDPH4D19FHF-SM
CRITICAL

R7901 = 402MF-LF1/16W 1%
200K
C7901 = 22pF 50V
402 5%
CERM

R7900 = 348K 402 1%/16W MF-LF
2

C7911 = 402 25VNP0-C0G 1000PF 5%

R7910 = 6.98K 402 2

SYNC_MASTER=K62
SYNC_DATE=01/06/2011

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### Page Notes

Power aliases required by this page:

Unused T29 Interfaces

Unused MXM Interfaces

unused T29 interfaces

Unused T29 Interfaces

Unused MXM Interfaces

### DDC/AUX ALIAS

- DDC/AUX ALIAS 1: DDC/AUX ALIAS 2

### T29 CONN POWER CONTROL ALIAS

- T29 Conn Power Control Alias 1: T29 Conn Power Control Alias 2

### T29 MXM DP ALIAS

- T29 MXM DP Alias 1: T29 MXM DP Alias 2

### UNUSED MXM CONTROL SIGNALS

- Unused MM Control Signals 1: Unused MM Control Signals 2

### Unused MXM Interfaces

- Unused MM Interfaces 1: Unused MM Interfaces 2

### Unused T29 Interfaces

- Unused T29 Interfaces 1: Unused T29 Interfaces 2
GreenCLK Implementation Notes:

For Caesar-IV (BCM57765): VDDIO = XTALVDDH (3.3V), Vclk = 3.3V Max. No Divider Necessary

For Cougar Point Mobile:  VDDIO = VCCVRM   (1.5V), Vclk = 1.1V Max, Divider: 332 / 1000

For Cougar Point Desktop: VDDIO = VCCVRM   (1.8V), Vclk = 1.1V Max, Divider: 604 / 1000

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.

For SB RTC Power

VDD_25M:     3.3V matching 'highest' VDDIO power state (ENET)
VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_C: T29 power rail for XTAL circuit.

VDD_RTC_OUT: System RTC Power Source & 32kHz / 25MHz Clock Generator

G3Hot Implementation Notes:

For Coin-Cell & G3Hot: 3.42V G3Hot
For Coin-Cell & No G3Hot: 3.3V S5

No Coin-Cell:         3.3V S5

NOTE: 30 PPM crystal required

- Voltage=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=1.05V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
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- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
- MIN_LINE_WIDTH=0.3 mm
- MIN_NECK_WIDTH=0.2 mm
- VOLTAGE=3.3V
T29 POWER

3.3V T29 Switch

1.05V T29 Switch

Supervisor & CLKREQ# Isolation

Page Notes

Signal aliases required by this page:

Power aliases required by this page:

BOM options provided by this page:

Pull-up provided by SB page.

Platform (PCIe) Reset

Make Base = TRUE

SYNC_DATE=01/06/2011

SYNC_MASTER=K62

Apple Inc.

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## PHYSICAL CONSTRAINTS

**K60/62 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS**

**PHYSICAL RULE SET**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**RULE DEFINITIONS**

- **LAYER MINIMUM NECK WIDTH**
- **LAYER MAXIMUM NECK LENGTH**
- **DIFFPAIR PRIMARY GAP**
- **DIFFPAIR NECK GAP**

### BOARD STACK-UP

- **TOP HALF OZ SIGNAL**
  - 2 TWO OZ GND
  - 3 ONE OZ SIGNAL
  - 4 TWO OZ POWER
  - 6 ONE OZ SIGNAL
  - 7 TWO OZ GND

- **BOTTOM HALF OZ SIGNAL**

**BOARD THICKNESS = 62 MIL (1.5748 mm)**

---

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11.1.0

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### Memory Bus Constraints

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_CMD2CMD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CTRL</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_2OTHER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_BYTE7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQS2MEM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_BYTE6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DQ_SAMEBYTE</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Memory Net Properties

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>MEM_A_DQS_N&lt;5&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;7&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ&lt;47..40&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ&lt;55..48&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQS_N&lt;3&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ&lt;15..8&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_CKE&lt;3..0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_A_DQ&lt;48..41&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ&lt;47..40&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ&lt;23..16&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;3&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_N&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_N&lt;3&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ&lt;15..8&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CAS_L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CKE&lt;3..0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CLK_P&lt;3..0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_N&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_N&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ&lt;23..16&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;3&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_P&lt;4&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ&lt;16..8&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CKE&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CLK_P&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CLK_P&lt;1&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CLK_P&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_CLK_P&lt;3&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ&lt;24..17&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_N&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS_N&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQ&lt;16..8&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CAS_L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CKE&lt;3..0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;3..0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CKE&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;0&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;1&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;2&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CLK_P&lt;3&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_DATA2MEM</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_CMD</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_2OTHER</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MEM_68D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>=68_OHM_DIFF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>=42_OHM_SE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0.1016 MM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Memory Bus Spacing Group Assignments

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>AREA_TYPE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPACING_RULE_SET</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NET_SPACING_TYPE1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NET_SPACING_TYPE2</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Memory Misc Properties

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_DIMM_VREF_A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREFMARGIN_DIMMA_DQ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VREFMARGIN_DIMMA_DACOUT</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table Spacing Rule Item

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TABLE_SPACING_RULE_ITEM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table Spacing Assignment Item

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TABLE_SPACING_ASSIGNMENT_ITEM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table Physical Rule Item

<table>
<thead>
<tr>
<th>Constraints</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TABLE_PHYSICAL_RULE_ITEM</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### SATA Interface Constraints

#### PCI-Express

<table>
<thead>
<tr>
<th>Layer</th>
<th>Width (mm)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.200</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

Note: Any other constraints not covered on pages 101 and 107 should go on this page as well.

---

**Table: Physical Spacing**

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Physical Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express</td>
<td>85_OHM_DIFF</td>
</tr>
</tbody>
</table>

---

**Table: Electrical Constraint Set**

- **Layer 1:**
  - XDP_CPU_TDI
  - XDP_CPU_TCK

- **Layer 2:**
  - CPU_50S
  - CPU_ITP

- **Layer 3:**
  - PCIE_USB3_1_D2R_C_P
  - PCIE_USB3_2_D2R_P

- **Layer 4:**
  - SATA_SSD_R2D_P
  - SATA_SSD_R2D_C_N

- **Layer 5:**
  - SATA_HDD_D2R_C_P
  - SATA_HDD_D2R_P

- **Layer 6:**
  - SATA_HDD_R2D_C_P

- **Layer 7:**
  - SATA_ODD_R2D_P
  - SATA_ODD_R2D_C_N

- **Layer 8:**
  - SATA_ODD_D2R_P

---

**Table: Spacing Rule Set**

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Spacing Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Express</td>
<td>85_OHM_DIFF</td>
</tr>
</tbody>
</table>

---

**Table: Physical Rule Set**

- **Layer 1:**
  - XDP_OBSDATA_B<3..0>
  - XDP_BPM_L<7..0>

- **Layer 2:**
  - CPU_50S
  - CPU_ITP

- **Layer 3:**
  - PCIE_USB3_2_D2R_C_P
  - PCIE_USB3_1_R2D_C_P

- **Layer 4:**
  - PCIE_USB3_2_R2D_N
  - PCIE_USB3_2_R2D_C_P

- **Layer 5:**
  - PCIE_USB3_2_R2D_N
  - PCIE_USB3_1_D2R_C_P

- **Layer 6:**
  - SATA_SSD_R2D_C_N
  - SATA_SSD_R2D_P

---

**Table: Electrical Constraint Set**

- **Layer 1:**
  - CPU_RCOMP_PHY

- **Layer 2:**
  - CPU_RCOMP

- **Layer 3:**
  - PCI_CLK100M_FW_P

- **Layer 4:**
  - PCI_CLK100M_FW_N

- **Layer 5:**
  - PCI_CLK100M_MINI_P

- **Layer 6:**
  - PCI_CLK100M_MINI_N

---

**Table: Electrical Constraint Set**

- **Layer 1:**
  - PCH_CLK96M_DOT_N
  - PCH_CLK100M_DMI_N

- **Layer 2:**
  - PCH_CLK100M_DMI_P

- **Layer 3:**
  - GPU_CLK100M_PCIE_P
  - GPU_CLK100M_PCIE_N

- **Layer 4:**
  - DMI_N2S_P<3..0>
  - DMI_S2N_N<3..0>

- **Layer 5:**
  - DMI_MIDBUS_CLK100M_P
  - DMI_MIDBUS_CLK100M_N

---

**Table: Electrical Constraint Set**

- **Layer 1:**
  - TP_CLK133M_PCH_P
  - TP_CLK133M_PCH_N

- **Layer 2:**
  - PCH_CLK96M_DOT_P
  - PCH_CLK100M_P

- **Layer 3:**
  - DMI_MIDBUS_CLK100M_P
  - DMI_MIDBUS_CLK100M_N

---

**Table: Electrical Constraint Set**

- **Layer 1:**
  - M2M_PCIE_R2D_N<8..15>

- **Layer 2:**
  - SATA_HDD_R2D_P

- **Layer 3:**
  - SATA_HDD_R2D_C_P

- **Layer 4:**
  - SATA_ODD_R2D_P
  - SATA_ODD_R2D_C_N

- **Layer 5:**
  - SATA_ODD_D2R_P
### Graphics Constraints

#### Table 1: DisplayPort/TMDS Intra-Pair Matching Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D MXM_DP_B_ML_P&lt;3..0&gt;</td>
<td>5 ps</td>
</tr>
<tr>
<td>DP_85D MXM_DP_D_AUX_P&lt;3..0&gt;</td>
<td>5 ps</td>
</tr>
</tbody>
</table>

#### Table 2: Deviation Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D MXM_DP_B_ML_P&lt;3..0&gt;</td>
<td>5 ps</td>
</tr>
<tr>
<td>DP_85D MXM_DP_D_AUX_P&lt;3..0&gt;</td>
<td>5 ps</td>
</tr>
</tbody>
</table>

#### Table 3: DisplayPort/TMDS Inter-Pair Matching Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DP_85D MXM_DP_B_ML_P&lt;3..0&gt;</td>
<td>150 ps</td>
</tr>
<tr>
<td>DP_85D MXM_DP_D_AUX_P&lt;3..0&gt;</td>
<td>150 ps</td>
</tr>
</tbody>
</table>

---

Date: 01/06/2011

Apple Inc.
# T29 ELECTRICAL ROUTES

<table>
<thead>
<tr>
<th>Logic Name</th>
<th>Route Width</th>
<th>Route Length</th>
<th>Min. Line Width</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>I431</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I428</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I424</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I422</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I421</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I440</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>I438</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# T29 PCI-EXPRESS (SAME RULE AS PCIe)

<table>
<thead>
<tr>
<th>Logic Name</th>
<th>Route Width</th>
<th>Route Length</th>
<th>Min. Line Width</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C_T29_SCL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T29_SMB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLK_25M_55S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# T29 SPI INTERFACE CONSTRAINTS

<table>
<thead>
<tr>
<th>Logic Name</th>
<th>Route Width</th>
<th>Route Length</th>
<th>Min. Line Width</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>T29_SPI_CLK</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T29_SPI_CS_L</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T29_SPI_MOSI</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>T29_SPI_55S</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# T29 XTL CONSTRAINTS

<table>
<thead>
<tr>
<th>Logic Name</th>
<th>Route Width</th>
<th>Route Length</th>
<th>Min. Line Width</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>T29_90D</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# T29 SMBUS INTERFACE CONSTRAINTS

<table>
<thead>
<tr>
<th>Logic Name</th>
<th>Route Width</th>
<th>Route Length</th>
<th>Min. Line Width</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td>T29_SMB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# GREEN CLOCK CONSTRAINTS

<table>
<thead>
<tr>
<th>Logic Name</th>
<th>Route Width</th>
<th>Route Length</th>
<th>Min. Line Width</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

# T29 BIAS CONSTRAINTS

<table>
<thead>
<tr>
<th>Logic Name</th>
<th>Route Width</th>
<th>Route Length</th>
<th>Min. Line Width</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**T29 CONSTRAINTS**

- **T29_SMB_55S** = STANDARD = 55_OHM_SE = 55_OHM_SE*
- **T29_XTAL_100D**
- **T29_SPI_55S** = STANDARD = 55_OHM_SE = 55_OHM_SE*
- **T29_XTAL** = 4X_DIELECTRIC
- **T29_90D** *
- **T29** *= 5X_DIELECTRIC
- **T29_90D** *
- **T29** *= 5X_DIELECTRIC

---

**T29 NET PROPERTIES**

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Type</th>
<th>Clocking</th>
<th>Electrical Constraint Set</th>
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**PHYSICAL SPACING**

- **T29_COMP**
- **T29_A_BIAS**
- **T29_COMP**
- **T29_COMPT29_55S**
- **T29_SMB**
- **T29_SPI**
FUNCTIONAL TEST POINTS FOR MAC-1 & ICT

- J5551 ODD TEMP SENSOR
  17 TP's

- J4780 IR BOARD
  1 PP3V3_S3 TESTPOINT NEAR J4700

- J5600 ODD FAN
  2 TP's

- J4700 USB CAMERA
  2 GROUND TESTPOINTS NEAR J4750

- J5400 HDD TEMP SENSOR
  1 GROUND TESTPOINT NEAR J5400

- J5560 SKIN TEMP SENSOR
  1 GROUND TESTPOINT NEAR J5700

- PP3V3_S3 Testpoint near J4750

- J6603 AUDIO LEFT SPEAKER
  4 GROUND TESTPOINTS NEAR J6600

- J6602 AUDIO RIGHT SPEAKER
  2 TP's

- J4520 SATA ODD (HIGH SPEED)
  1 GROUND TESTPOINTS NEAR J4520

- J6600 AUDIO AUXILIARY CONNECTOR
  4 GROUND TESTPOINTS NEAR J6600

- PP5V_S0 Testpoint near J4520

- AUD_HP_R_JACK
  FUNC_TEST=TRUE

- AUD_HP_GND_JACK
  FUNC_TEST=TRUE

- AUD_HP_TIPDET_JACK
  FUNC_TEST=TRUE

- AUD_HP_L_JACK
  FUNC_TEST=TRUE

- AUD_HP_TYPEDET_JACK
  FUNC_TEST=TRUE

- AUD_HP_R_JACK
  FUNC_TEST=TRUE

- AUD_LI_L_JACK
  FUNC_TEST=TRUE

- AUD_LI_GND_JACK
  FUNC_TEST=TRUE

- AUD_LI_DET_JACK
  FUNC_TEST=TRUE

- PP3V3_AUDIO_SPDIF_JACK
  MIN_ALLOWED_TPS=2

- PP5V_S0_IR_FLT
  USB_BT_L_P
  USB_BT_L_N

- PP5V_S3_IR_FLT
  USB_BT_L_P
  USB_BT_L_N

- PP5V_S0_FAN0_L
  PP5V_S0_FAN1_L
  PP5V_S0_FAN2_L

- FAN_0_PWR_L
  FAN_TACH0_L
  FAN_0_GND

- FAN_1_PWR_L
  FAN_TACH1_L
  FAN_1_GND

- SNS_AMB_P
  FAN_2_PWR_L
  FAN_TACH2_L
  FAN_2_GND

- SNS_AMB_N
  SNS_SKIN_LEFT_P
  SNS_SKIN_LEFT_N
  SNS_SKIN_RIGHT_P
  SNS_SKIN_RIGHT_N

- HDD_OOB_TEMP_FILT
  USB_CAMERA_L_P
  USB_CAMERA_L_N

- SNS_ODD_P
  USB_BT_L_P
  USB_BT_L_N

- SNS_ODD_N
  MIN_ALLOWED_TPS=1

- PP5V_S3
  MIN_ALLOWED_TPS=1

- PP5V_S3_IR_FLT
  MIN_ALLOWED_TPS=17

- PP5V_S3_AUDIO_SPDIF_JACK
  MIN_ALLOWED_TPS=1

- PP5V_S3
  MIN_ALLOWED_TPS=1

- PP12V_S0_FAN0_L
  PP12V_S0_FAN1_L
  PP12V_S0_FAN2_L

- FAN_TACH0_L
  FAN_TACH1_L
  FAN_TACH2_L

- AUD_HP_L_JACK
  AUD_HP_R_JACK

- AUD_SPK_OUTLO1L_POUT
  AUD_SPK_OUTLO1L_NOUT

- AUD_SPK_OUTLO2L_POUT
  AUD_SPK_OUTLO2L_NOUT

- AUD_SPK_OUTLO1R_POUT
  AUD_SPK_OUTLO1R_NOUT

- AUD_SPK_OUTLO2R_POUT
  AUD_SPK_OUTLO2R_NOUT

- MIN_ALLOWED_TPS=17

- SMCM ODD_DETECT
  MIN_ALLOWED_TPS=2

- PP12V_S0_FAN0_L
  PP12V_S0_FAN1_L
  PP12V_S0_FAN2_L

- FAN_0_PWR_L
  FAN_TACH0_L
  FAN_0_GND

- FAN_1_PWR_L
  FAN_TACH1_L
  FAN_1_GND

- SNS_AMB_N
  FNC_TEST=TRUE

- PP12V_S0_FAN2_L
  FNC_TEST=TRUE