1. All resistance values are in ohms, ±10% tolerance.
2. All capacitance values are in microfarads.
3. All crystal and oscillator values are in hertz.

**Table of Contents**

- System Block Diagram
- Power Block Diagram
- ROM Configuration
- Functional / JCT Test
- Signal Aliases
- CPU 1 OF 2-PEG
- CPU 2 OF 2-PEG/GND
- CPU Decoupling & VID
- CPU MISC1-2MP SENSOR
- CPU 1P0FLEX DEBUG
- NB CPU Interface
- NB Misc Interfaces
- NB DDR2 Interfaces
- NB Power 1
- NB Power 2
- NB Grounds
- NB (GR) Decoupling
- NB Config Straps
- SB 1 OF 4
- SB 2 of 4
- SB 3 OF 4
- SB 4 OF 4
- SB Decoupling
- SB Misc
- MI SMBus Connections
- DDR2 2D-DIMM Connector A
- DDR2 2D-DIMM Connector B
- Memory Active Termination
- Memory Vtt Supply
- DDR2 VMCF
- CLOCK
- Clock Termination
- Mobile Clocking
- PATA Connector
- FireWire PHY (7SB63AA22)
- Ethernet Controller
- EtherTherm CONTROLLER
- Ethernet Connectors
- Yukon Power Control
- FB PHY Power Supply
- FireWire Port Power

**FireWire Ports**

- FireWire Ports
- Internal USB Connections
- External USB Connector
- Left I/O Board Connector
- Functional & Thermal Sensors
- PCI-X Connections
- SMI
- SMI Support
- LPC+ Debug Connector
- Thermal Sensors
- Current & Voltage Sensing
- SPI BODPM
- ALS Support
- Fan Connectors
- Sudden Motion Sensor (SMS)
- TPM
- IME64 CPU VCore Regulator
- 1.5V / 1.5V Power Supplies
- 2.5V & 1.2V Regulators
- 1.8V Supply
- 1.1V/1.15V Power Supplies
- 1.3V GHOT Supply & Power Control
- Power Aliases
- DC-In & Battery Connectors
- FBus Supply & Batt. Charger
- ATI HSB PCI-E
- GPU (N56) Core Supplies
- ATI HSB Core Power
- ATI HSB Frame Buffer I/F
- GPU Straps
- DDR3 Frame Buffer A
- DDR3 Frame Buffer B
- ATI HSB GPO/DVD/Misc
- ATI HSB Video Interfaces
- Internal Display Connectors
- External Display Connector
- NB Specific Connectors
- LVDS Interface Pull-downs
- Revision History
- Napa Platform Constraints
- More System Constraints
- MI Spacing & Physical Constraints
- MI Net Properties

**Schematic / PCB #s**

- 501-7023 1 PBC,FULL,FINAL,MS

**ALIASES RESOLVED**
### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DEC</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>7999262950</td>
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<td>IC,DDR,32MB,168S32,JAM,70MHZ,72S</td>
<td>M56_REV_B24_LP</td>
<td>CRITICAL</td>
<td>BOM OPTION</td>
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<td>BOM OPTION</td>
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<td>BOM OPTION</td>
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<td>M56_REV_B24_LP</td>
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<td>BOM OPTION</td>
</tr>
</tbody>
</table>

### M9 Specific Aliases

```
- U7800
- U7800
- U7800
- U7800
```

---

**Note:** The information presented is a sample of the content from the image, focusing on the parts and specifications listed. The full document contains detailed technical specifications and diagrams relevant to the components involved in a specific project or design. The text includes part numbers, descriptions, quantities, and aliases specific to the project. The diagram also highlights various parts and connections, with annotations for clarity and understanding. The mention of “PROPERTY OF APPLE COMPUTER, INC. THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY” indicates the confidentiality of the information, emphasizing the need for controlled access and non-disclosure of proprietary data. The diagram and text are intended to facilitate the understanding and use of the components in the specified context. The image also includes a reference to “www.Vinafix.vn,” suggesting a source or additional resource related to the content. This representation adheres to the guidelines for natural text extraction and provides a comprehensive overview of the document's content.
CPU VCORE HF AND BULK DECOUPLING

4x 470uF, 20x 22uF 0805

VCCA (CPU AVdd) Decoupling

1x 10uF, 1x 0.01uF

VCCP (CPU I/O) Decoupling

1x 470uF, 6x 0.1uF 0402

NOTE: This cap is shared between CPU and NB.
CPU ZONE THERMAL SENSOR

PLACE U1001 NEAR THE U1200

C1001
1 2
CERM
50V
0.001uF
10%
402

R1002
12
499
1%
MF-LF
402
1/16W

C1002
1 2
X5R
0.1UF
16V
10%
402

R1005
1
1/16W
5%
402
10K
MF-LF

R1006
1
10K
1/16W
402
MF-LF
5%

ADT7461
U1001
6
2
3
5
8
7
4
1

CPU ITP700FLEX DEBUG SUPPORT

ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.
Both Function 2 & 3 of Device 30 are disabled. Internal 20K PD enabled during reset and when.

NOTE: EE_CS has internal PD, only enabled when LAN_RST#=L

NOTE: All IDE pins have internal 33-ohm series R's.

NOTE: Keyboards controller reset CPU rising-edge triggered at CPU.

NOTE: Keyboard controller reset CPU.

NOTE: All IDE pins have internal 33-ohm series R's.
RTC Battery Connector

SB RTC Crystal Circuit

Platform Reset Connections

Unbuffered

Buffered

SB Misc
The reference voltage must be provided by another page.

**NOTE:** This page does not supply VREF.

BOM options provided by this page:
- =I2C_SODIMMA_SDA
- =PPSPD_S0_MEM (2.5V - 3.3V)

"Lower" (surface-mount) slot

**DDR2 Bypass Caps**
(For return current)

**DDR2 SO-DIMM Connector A**

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SYNC_DATE=02/10/2006
One cap for each side of every RPAK, one cap for every two discrete resistors.

Ensure C23, L and OUT resistors are close to SO-DIMM connector.
Memory Vtt Supply

**DDR2 Vtt Regulator**

- If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.
- MEMVTT_EN can be used to leave 1.8V powered in S3.
- Okay to turn off 5V and leave 1.8V powered in S3.

**Power Aliases Required by This Page:**
- PP0V9_S0_MEMVTT_LDO
- PP1V8_S0_MEMVTT
- PP5V_S0_MEMVTT

**Signal Aliases Required by This Page:**
- (NONE)

**Power Aliases Required by This Page:**
- (NONE)

**BOM Options Provided by This Page:**
- (NONE)

**Page Notes:**
- **A**: PP1V8_S0_MEMVTT
- **B**: PP5V_S0
- **C**: MEMVTT_VREF
- **D**: MEMVTT_EN

**Memory Vtt Supply**

- **SYNC_DATE=02/10/2006**
- **SYNC_MASTER=M1_MLB**

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**APPLE COMPUTER INC.**

- 051-7023
- 06
- 31 86
Page Notes

Power aliases required by this page:
- PP2V5_S3_ENET

Signal aliases required by this page:

- ENET_CTAP0
- ENET_CTAP1
- ENET_CTAP2
- ENET_CTAP3

Transformers should be mirrored on opposite sides of the board

Place one cap at each pin of transformer

- Place close to connector
- Short shielded RJ-45

---

Ethernet Connector

- ENET_100D
- ENETCONN
- ENETCONN_P<0>
- ENETCONN_P<1>
- ENETCONN_P<2>
- ENETCONN_P<3>
- ENET_CONN_P<3>
- ENET_CONN_N<0>
- ENET_CONN_N<1>
- ENET_CONN_N<2>
- ENET_CONN_N<3>
- ENET_MDI_P<0>
- ENET_MDI_P<1>
- ENET_MDI_P<2>
- ENET_MDI_P<3>
- ENET_MDI_N<0>
- ENET_MDI_N<1>
- ENET_MDI_N<2>
- ENET_MDI_N<3>

---

Components:

- R4200
- R4201
- R4202
- R4203
- C4200
- C4201
- C4202
- C4203
- C4204
- J4200
- T4200
- T4201

---

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---

BOM options provided by this page:

- Place close to connector
- Short shielded RJ-45
Yukon Power Control

Allows powering Yukon down during battery sleep to save power.

Yukon Power Control

SYNC_DATE=02/10/2006
SYNC_MASTER=M1_MLB

www.Vinafix.vn
Vout = 1.22V \times (1 + \frac{Ra}{Rb}) + (I_{adj} \times Ra)

I_{adj} = 30nA @ 25 \text{ deg C}

165MA MAX LOAD

VOLTAGE=33V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

PP5VR33V_FWPHY3V3
PP1V95_FWPHY
PPBUS_S5_FW_FET
FWPHY_CORE_BYP
FWPHY_CORE_ADJ
PP3V3_FWPHY
FWPHY3V3_SW
BOM options provided by this page:
- FWPWR_PWRON (see related text note below)

Signal aliases required by this page:

Power aliases required by this page:

Page Notes

Current Limit/Active Late-VG Protection

Late-VG Event Detection

FireWire Port Current Sense

FireWire Port Power

---

Sync_Date=(11/03/2005)

APPLE COMPUTER INC.

D:

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NOTE: FireWire TPA/TPB pairs are NOT

**Signal aliases required by this page:**
- `**PPFW_PORT1**`
- `**PP3V3_FWPHY**`
- `**FW_110D**`

**Page Notes**

- **Power aliases required by this page:**
  - `**PPFW_PORT1**`
  - `**PP3V3_FWPHY**`
  - `**FW_110D**`

- **ELECTRICAL_CONSTRAINT_SET**
  - `**SPACING**` 402
  - `**FW**`

- **Page Notes**
  - **PROVIDED** BY
  - **GROUP**

**Termination**

Place close to Firewire PHY

**Late-VG Protection Power**

DF29 examined for snap-back and late-VG signal integrity (TPO#)

**Port 1**

- **BILINGUAL**
  - **CRITICAL**
  - **PPFW_PORT1**
  - **PPFW_PORT2**
  - **PPFW_PORTA**

**Port 2**

- **1394A**
  - **CRITICAL**
  - **PPFW_PORT1**
  - **PPFW_PORT2**
  - **PPFW_PORTA**

**FireWire Ports**

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- **PRODUCT**
  - **MAKERS**
  - **MQTY**

**Reference**

- **www.Vinafix.vn**

---

**Apple Computer Inc.**

- **051-7023 06**
Top-Case Connector LIO Temp Sensor Connector

Camera Connector

Internal USB Connections

www.Vinafix.vn
Port Power Switch

Right USB Port

Place L5200, L5205 and L5206 across moat
**GPU / Heat Pipe Thermal Sensor**

- Place near CPU center
- Placement note:

**CPU Back-Up Thermal Diode**

- Place near CPU center
- Placement note:

**Right-Side/Fin Stack Thermal Sensor**

- Place in between VRAM
- Placement note:

---

**Crucial Components**

- **CPU Back-Up Thermal Diode**
  - R6190
  - MF-LF 1/16W 402 5%
  - R6191
  - MF-LF 1/16W 402 5%

---

**Additional Notes**

- R1001 / R1002 are not currently BOM OPTIONED. Cannot programatically unstuff those parts to stuff these.
R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA (LAN CHIP).

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FROM ICH7M.

R6303 SHOULD BE PLACED LESS THAN 100 MILS FROM FLASH ROM.
Desired orientation when placed on board top-side:

Desired orientation when placed on board bottom-side:

Package Top

Top-through View

M1 placement: Bottom-side

Sudden Motion Sensor (SMS)

SYNC_MASTER=M1_MLB
SYNC_DATE=02/10/2006

PP3V3_S3
Connect to R7668 pins to control outputs.

If connected, powers up with VIN.

NOTE: Be aware of pull-ups to VIN on these signals.

Connect to RUNSS pins to control outputs.

Vout = 0.8V * (1 + Ra / Rb)
Power Control Signals

3.425V "G3Hot" Supply
Supply needs to guarantee 3.12V delivered to BMC Timer generator

1.5V / 1.05V PWRGD Circuit
Reports when 1.5V S0 and 1.05V S0 are in regulation

Other S0 Rails PWRGD Circuit
Reports when 5V S0, 2.7V S0, 2.5V S0, 1.6V S0, 1.2V S0 and 0.9V S0 are in regulation

3.3V G3Hot Supply & Power Control
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www.Vinafix.vn
As shown, \( I_{ch} = 3.9 \text{A max} \)

Using PWM drive

10A max, limited by L8300, Q8301

MIN_NECK_WIDTH = 0.2mm

MIN_LINE_WIDTH = 0.6mm

1%
TMDS Filtering
Place series R's and common-mode filtering close to GPU, common mode chokes near connector.

DVI DDC CURRENT LIMIT
(55A requirement per DVI spec)

DVI INTERFACE
Isolation required for DVI power switch

3V LEVEL SHIFTERS

External Display Connector

APPLE COMPUTER INC.
IR & Sleep LED Connector

Bluetooth (M13P) & SATA HDD Flex Connector

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ATTENTION TO M9 SPECIFIC CONNECTORS
SYNC_MASTER=(MASTER) SYC_DATE=(MASTER)

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LVDS Interface Pull-downs

NOTE: These parts are to counter an invalid state caused by the M56 part. Bias voltage is present on LVDS interface pins even when tri-stated to meet panel requirements. Resulting pump-up in LCD panel can cause startup and long-term reliability issues. Pull-down resistors reduce the pump-up in the panel, though some voltage will still be seen on LVDS signals when they should be IV.

LVDS_PD

RP9901
8.2K
SM-LF
LVDS_PD
1/16W
5%

RP9900
8.2K
SM-LF
LVDS_PD
1/16W
5%

RP9903
8.2K
SM-LF
LVDS_PD
1/16W
5%

RP9901
8.2K
SM-LF
LVDS_PD
1/16W
5%

RP9902
8.2K
SM-LF
LVDS_PD
1/16W
5%

RP9903
8.2K
SM-LF
LVDS_PD
1/16W
5%

RP9904
8.2K
SM-LF
LVDS_PD
1/16W
5%

LVDS_Interface_Pull-downs

SYNC_DATE=12/19/2005
SYNC_MASTER=M1_MLB

LVDS_L_DATA_CONN_N<2>
LVDS_L_DATA_CONN_P<2>
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_CLK_P
LVDS_L_CLK_N

LVDS_U_DATA_CONN_P<1>
LVDS_U_DATA_CONN_N<1>
LVDS_U_DATA_P<0>
LVDS_U_DATA_N<0>
LVDS_U_CLK_P
LVDS_U_CLK_N

MAKE_BASE=TRUE
Revision History

12-01-05: - Changed L4400 to Pb-free part
   - Changed J4620 to M9 part
   - Added PM_SUS_STAT_L and PM_SLP_S5_L pulldowns
   - Removed dual voltage support for trackpad
   - Added ESD/EMI protection to camera connector

12-01-05: - Changed IDE reset pulldown to 15K
11-30-05: - RC value changes on CPU Core current sense
11-29-05: - Turned on M56_REV_B24 BOMOPTION
11-28-05: - Added CRITICAL property to 3-pin caps, ESD diodes, and FW chokes
   - Added ITPCONN BOMOPTION

SYNC_MASTER=(MASTER)
SYNC_DATE=(MASTER)
### GDDR3 (Frame Buffer) Memory Bus Constraints

<table>
<thead>
<tr>
<th>Net Type</th>
<th>Line</th>
<th>Area_Type</th>
<th>Area_Type</th>
<th>Min_Width</th>
<th>Min_Width</th>
<th>Neck_Width</th>
<th>Neck_Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_35S_TO_55S</td>
<td>1</td>
<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
<td>55_OHM_SE</td>
</tr>
<tr>
<td>GDDR3_75S</td>
<td>1</td>
<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
<td>55_OHM_SE</td>
</tr>
<tr>
<td>GDDR3_40S</td>
<td>1</td>
<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
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<td>GDDR3_55S</td>
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<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
<td>55_OHM_SE</td>
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<tr>
<td>GDDR3_110S</td>
<td>1</td>
<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
<td>55_OHM_SE</td>
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</tbody>
</table>

### High-Speed I/O Interface Constraints

<table>
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<th>Net Type</th>
<th>Line</th>
<th>Area_Type</th>
<th>Area_Type</th>
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<th>Neck_Width</th>
<th>Neck_Width</th>
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<tbody>
<tr>
<td>ENET_100D</td>
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<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
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<tr>
<td>FW_110D</td>
<td>1</td>
<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
<td>55_OHM_SE</td>
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<tr>
<td>PCI</td>
<td>1</td>
<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
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### PCle Bus Constraints

<table>
<thead>
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<th>Net Type</th>
<th>Line</th>
<th>Area_Type</th>
<th>Area_Type</th>
<th>Min_Width</th>
<th>Min_Width</th>
<th>Neck_Width</th>
<th>Neck_Width</th>
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</thead>
<tbody>
<tr>
<td>PCle_110S</td>
<td>1</td>
<td>STandard</td>
<td>STandard</td>
<td>110_OHM_DIFF</td>
<td>110_OHM_DIFF</td>
<td>55_OHM_SE</td>
<td>55_OHM_SE</td>
</tr>
</tbody>
</table>

### More System Constraints

- **Items Related to GDDR3 Memory Bus**
  - GDDR3 signals are 110-ohm +/-15% differential impedance.
  - Ground shield can be used around each pair if spacing cannot be met.
  - Signals should be kept at least 15 mils from other traces.
  - Ground shield recommended around GDDR3 signals.

- **Items Related to High-Speed I/O Interface**
  - ENET and TMDS lines are 110-ohm single-ended.
  - Ground shield recommended around ENET signals.

- **Items Related to PCle Bus**
  - PCle signals are 110-ohm +/-15% differential impedance.
  - Ground shield recommended around PCle signals.

*Note: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close".*

---

**Video Signal Constraints**

**High-Speed I/O Interface Constraints**

**PCle Bus Constraints**

---

**More System Constraints**

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<table>
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<td>PHYSICAL_RULE_SET</td>
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<td>PHYSICAL_RULE_SET</td>
</tr>
</tbody>
</table>

**Table 1: Minimum Line Width**

<table>
<thead>
<tr>
<th>Area Type</th>
<th>MINIMUM LINE WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS_100D</td>
<td>0.18 MM</td>
</tr>
<tr>
<td>VGA_75S</td>
<td>0.15 MM</td>
</tr>
<tr>
<td>1.8:1_SPACING</td>
<td>0.12 MM</td>
</tr>
<tr>
<td>1.5:1_SPACING</td>
<td>0.12 MM</td>
</tr>
<tr>
<td>4:1_SPACING</td>
<td>0.12 MM</td>
</tr>
<tr>
<td>3:1_SPACING</td>
<td>0.12 MM</td>
</tr>
</tbody>
</table>

**Table 2: Minimum Neck Width**

<table>
<thead>
<tr>
<th>Area Type</th>
<th>MINIMUM NECK WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISL2,ISL11</td>
<td>0.105 MM</td>
</tr>
<tr>
<td>1.8:1_SPACING</td>
<td>0.099 MM</td>
</tr>
<tr>
<td>1.5:1_SPACING</td>
<td>0.099 MM</td>
</tr>
<tr>
<td>4:1_SPACING</td>
<td>0.099 MM</td>
</tr>
<tr>
<td>3:1_SPACING</td>
<td>0.099 MM</td>
</tr>
</tbody>
</table>

**Table 3: Maximum Neck Length**

<table>
<thead>
<tr>
<th>Area Type</th>
<th>MAXIMUM NECK LENGTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8:1_SPACING</td>
<td>30 MM</td>
</tr>
<tr>
<td>1.5:1_SPACING</td>
<td>30 MM</td>
</tr>
<tr>
<td>4:1_SPACING</td>
<td>30 MM</td>
</tr>
<tr>
<td>3:1_SPACING</td>
<td>30 MM</td>
</tr>
</tbody>
</table>

**Table 4: Diffpair Primary Gap**

<table>
<thead>
<tr>
<th>Area Type</th>
<th>DIFFPAIR PRIMARY GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8:1_SPACING</td>
<td>0.330 MM</td>
</tr>
<tr>
<td>1.5:1_SPACING</td>
<td>0.220 MM</td>
</tr>
<tr>
<td>4:1_SPACING</td>
<td>0.125 MM</td>
</tr>
<tr>
<td>3:1_SPACING</td>
<td>0.125 MM</td>
</tr>
</tbody>
</table>

**Table 5: Diffpair Neck Gap**

<table>
<thead>
<tr>
<th>Area Type</th>
<th>DIFFPAIR NECK GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8:1_SPACING</td>
<td>0 MM</td>
</tr>
<tr>
<td>1.5:1_SPACING</td>
<td>0 MM</td>
</tr>
<tr>
<td>4:1_SPACING</td>
<td>0 MM</td>
</tr>
<tr>
<td>3:1_SPACING</td>
<td>0 MM</td>
</tr>
</tbody>
</table>

**Table 6: Unsupported rule**

<table>
<thead>
<tr>
<th>Area Type</th>
<th>MINIMUM LINE WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>IL_002</td>
<td>0.077 MM</td>
</tr>
<tr>
<td>IL_068</td>
<td>0.099 MM</td>
</tr>
<tr>
<td>IL_114</td>
<td>0.102 MM</td>
</tr>
<tr>
<td>IL_159</td>
<td>0.102 MM</td>
</tr>
</tbody>
</table>

---

**Rules for "Topology #3" for PBB signals, Mega DC tables 6-7 & 6-12.**

**Table 7: Allowed Blind-to-Buried via Directions (Layers 2 & 5)**

<table>
<thead>
<tr>
<th>Layer</th>
<th>MINIMUM LINE WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>0.089 MM</td>
</tr>
<tr>
<td>5</td>
<td>0.077 MM</td>
</tr>
<tr>
<td>2</td>
<td>0.090 MM</td>
</tr>
<tr>
<td>5</td>
<td>0.124 MM</td>
</tr>
</tbody>
</table>

**Table 8: "Stale" physical / spacing types**

<table>
<thead>
<tr>
<th>Property</th>
<th>Area Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS</td>
<td>LVDS_100D</td>
</tr>
<tr>
<td>VGA</td>
<td>VGA_75S</td>
</tr>
</tbody>
</table>

---

**Title: M1 Spacing & Physical Constraints**

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