3. All crystals & oscillator values are in hertz.

1. All resistance values are in ohms, 0.1 watt +/- 5%.
### Production BOM

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PART NAME</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>335S0384</td>
<td></td>
<td></td>
</tr>
<tr>
<td>338S0274</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Development BOM

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PART NAME</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>335S0382</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### BOM Options

<table>
<thead>
<tr>
<th>BOM GROUP</th>
<th>BOM OPTIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1 COMMON</td>
<td>M1_DEVELOPMENT, M1 COMMON, M1 COMMON, ALTERNATE</td>
</tr>
</tbody>
</table>

### BarCode Label / EEE #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>825-6447</td>
<td>1</td>
<td>BAR CODE LABEL, MLB, M1</td>
<td>[EEE:V4K]</td>
<td>CRITICAL</td>
<td>EEE_V4K</td>
</tr>
<tr>
<td>825-6448</td>
<td>1</td>
<td>BAR CODE LABEL, MLB, M1</td>
<td>[EEE:V4K]</td>
<td>CRITICAL</td>
<td>EEE_V4K</td>
</tr>
</tbody>
</table>

### Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>338S0288</td>
<td>2</td>
<td>IN,1790,MLB,MLB,MLB</td>
<td>U1200</td>
<td>CRITICAL</td>
<td>U1200</td>
</tr>
</tbody>
</table>

### Misc. Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>820-2038</td>
<td>1</td>
<td>IO ALIGNMENT BOARD, M51</td>
<td></td>
<td>CRITICAL</td>
<td></td>
</tr>
</tbody>
</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>825-6447</td>
<td>1</td>
<td>BAR CODE LABEL, MLB, M1</td>
<td>[EEE:V4K]</td>
<td>CRITICAL</td>
<td>EEE_V4K</td>
</tr>
<tr>
<td>825-6448</td>
<td>1</td>
<td>BAR CODE LABEL, MLB, M1</td>
<td>[EEE:V4K]</td>
<td>CRITICAL</td>
<td>EEE_V4K</td>
</tr>
</tbody>
</table>

### BOM Config

- **CPU VREG NEW REV**
  - U7500
  - 353S1465
  - 353S1461
  - 359S0117 359S0101
  - U3301
  - SILEGO CK410 CLOCK
  - GREEN LED ALT.

- **Module Parts**
  - IC,CPU-SKT,479BGA
    - CRITICAL
    - U4101
    - 338S0270
  - IC,ENET LAN ROM
    - CRITICAL
    - U4102
  - IC,CY28445-5,CLK GEN,68PIN QFN
    - CRITICAL
    - U3301
  - IC,945PM,NORTHBRIDGE
    - CRITICAL
    - U1200
  - BAR CODE LABLE, MLB, M51
    - CRITICAL EEE_V4K
    - [EEE:V4K]
  - 825-6447
  - 126S0088
  - ALL
  - Sanyo alt for Nich.
  - 126S0078
  - Sanyo alt for Nich.
  - 126S0068

- **Misc. Parts**
  - 825-6447
  - 126S0088
  - ALL
  - Sanyo alt for Nich.
CPU ITP700FLEX DEBUG SUPPORT

ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU's FBO PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR's FBO PIN.

**Notice of Proprietary Property**

Agrees to the following:

I to maintain the document in confidence

I Not to reveal or publish in whole or part

II Not to reproduce or copy it

III Not to make unauthorized use thereof

Property of Apple Computer, Inc. the possessor

The information contained herein is the proprietary

D 051-7039 17

www.Vinafix.vn
**NOTICE OF PROPRIETARY PROPERTY**

I agree to the following:

I will maintain this document in confidence.

I will not reveal or publish in whole or part.

I will not reproduce or copy it.

The information contained herein is the proprietary property of Apple Computer, Inc. The possessor of this document.

---

**NB_CONFIG**

- **NB_CFG<11>**
  - High = Mobile CPU
  - Low = Reserved

- **NB_CFG<12>**
  - High = DMIx2
  - Low = DMIx2

- **NB_CFG<13>**
  - High = DMIx4
  - Low = Reserved

- **NB_CFG<14>**
  - High = DMI Lane Reversal
  - Low = Reserved

- **NB_CFG<15>**
  - High = CPU Strap
  - Low = Reserved

- **NB_CFG<16>**
  - High = PCIE Graphics
  - Low = Reserved

- **NB_CFG<17>**
  - High = Interop Mode
  - Low = Reserved

- **NB_CFG<18>**
  - High = PCIe Backward
  - Low = Reserved

- **NB_CFG<19>**
  - High = DMI x2 Select
  - Low = Reserved

- **NB_CFG<20>**
  - High = DMI Lane Reversal
  - Low = Reserved

---

**Internal pull-ups**

- **NB_CFG_DMI_X2**
  - **R2075**
  - **2.2K 5% 1/16W MF-LF**

- **NB_CFG_DYN_ODT_DISABLE**
  - **R2085**
  - **2.2K 5% 1/16W MF-LF**

- **NB_CFG_VCC_1V5**
  - **R2058**
  - **2.2K 5% 1/16W MF-LF**

- **NB_CFG_DMI_REVERSE**
  - **R2059**
  - **2.2K 5% 1/16W MF-LF**

- **NB_CFG_SDVO_AND_PCIE**
  - **R2060**
  - **2.2K 5% 1/16W MF-LF**

- **NB_CFG_PEG_REVERSE**
  - **R2079**
  - **2.2K 5% 1/16W MF-LF**

- **NBCFG_DMI_X2**
  - **R2077**
  - **2.2K 5% 1/16W MF-LF**

- **NBCFG_PEG_REVERSE**
  - **R2078**
  - **2.2K 5% 1/16W MF-LF**

---

**SYNC_MASTER**

- **M50_HENRY**

**SYNC_DATE**

- **05/19/2006**

---

**NB Config Straps**
The reference voltage must be provided by another page.

NOTE: This page does not supply VREF.

BOM options provided by this page:
- =I2C_MEM_SDA
- =I2C_MEM_SCL

Signal aliases required by this page:
- =PPSPD_S0_MEM (2.5V - 3.3V)

www.Vinafix.vn
 DDR2 Vtt Regulator

MEMVTT_EN can be used to disable MEMVTT in sleep.

If power inputs are not S0, MEMVTT_EN cannot be used to disable MEMVTT in sleep.

If S0 and S3 are both N, MEMVTT can be used to disable MEMVTT in sleep.

Can 5V be S0 if 1V8 is S3?

Page Notes

NOTICE OF PROPRIETARY PROPERTY
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III NOT TO REPRODUCE OR COPY IT

AGREES TO THE FOLLOWING

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

BOM options provided by this page:

- =PP0V9_S0_MEMVTT_LDO
- =PP1V8_S0_MEMVTT
- =PP5V_S0_MEMVTT

Signal aliases required by this page:

Power aliases required by this page:

(NONE)

(NONE)

SYNC_DATE=05/19/2006

SYNC_MASTER=M50_HENRY
NOTICE OF PROPRIETARY PROPERTY

I AGREE TO THE FOLLOWING

I NOT TO REPRODUCE OR COPY IT
II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
III TO MAINTAIN THE DOCUMENT IN CONFIDENCE

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

REV. 051-7039  17  42°  97

APPLE COMPUTER INC.
PCI-E X1 PORT "A" = ETHERNET (YUKON)
- PCIE_A_R2D_C_P = PCIE_R2D_C_P
- PCIE_A_D2R_N = PCIE_D2R_N
- PCIE_A_R2D_C_N = PCIE_R2D_C_N
- PCIE_A_D2R_P = PCIE_D2R_P

PCI-E X1 PORT "B" = MINI CARD (AIRPORT)
- PCIE_B_R2D_C_P = PCIE_R2D_C_P
- PCIE_B_D2R_N = PCIE_D2R_N
- PCIE_B_R2D_C_N = PCIE_R2D_C_N
- PCIE_B_D2R_P = PCIE_D2R_P

PCI-E X1 PORTS C, D, E, F = UNUSED
- PCIE_C_R2D_C_P = PCIE_R2D_C_P
- PCIE_C_D2R_N = PCIE_D2R_N
- PCIE_C_R2D_C_N = PCIE_R2D_C_N
- PCIE_C_D2R_P = PCIE_D2R_P
- PCIE_C_R2D_P = PCIE_R2D_P
- PCIE_C_D2R_N = PCIE_D2R_N
THEY ARE SET BY SOFTWARE TO BE SMC_XXX WHERE XXX IS THE PORT NUMBER.

OMIT (4 OF 4)
NOTICE OF PROPRIETARY PROPERTY

I AGREE TO THE FOLLOWING

PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY

NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

NOT TO REPRODUCE OR COPY IT

TO MAINTAIN THE DOCUMENT IN CONFIDENCE
R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100

R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301
www.Vinafix.vn
4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

MIC INPUT TO BOTH L&R

--- AUD_SBP AND_IO0 F_L --- AUD_SBP AND_IO0 F_R ---
--- AUD_IB_PORT F_L --- AUD_IB_PORT F_R ---
--- AUD_IB_PORT A_R --- AUD_IB_PORT A_L ---
--- AUD_IB_PORT B_R --- AUD_IB_PORT B_L ---
--- AUD_IB_PORT C_L --- AUD_IB_PORT C_R ---
--- AUD_IB_PORT D_R --- AUD_IB_PORT D_L ---
--- AUD_IB_PORT_E_L --- AUD_IB_PORT_E_R ---
--- NC AND_AUD_IB_PORT_H_L --- NC AND_AUD_IB_PORT_H_R ---
--- NC_AUD_IB_PORT_G_L --- NC_AUD_IB_PORT_G_R ---
--- NC_AUD_VREF_PORT_B --- NC_AUD_VREF_PORT_E ---
--- NC_AUD_VREF_PORT_D --- NC_AUD_VREF_PORT_C ---
--- AUD_IB_PORT_H_L --- AUD_IB_PORT_H_R ---
--- AUD_IB_PORT_G_L --- AUD_IB_PORT_G_R ---
--- NC_AUD_IB_PORT_F_L --- NC_AUD_IB_PORT_F_R ---

--- AUD_IB_PORT H_L --- AUD_IB_PORT H_R ---
--- MIC INPUT TO BOTH L&R ---

--- AUD_IB_PORT F_L --- AUD_IB_PORT F_R ---
--- AUD_IB_PORT_F_L --- AUD_IB_PORT_F_R ---
--- AUD_IB_PORT_A_L --- AUD_IB_PORT_A_R ---
--- AUD_IB_PORT_B_L --- AUD_IB_PORT_B_R ---
--- AUD_IB_PORT C_R --- AUD_IB_PORT C_L ---
--- AUD_IB_PORT D_L --- AUD_IB_PORT D_R ---
--- AUD_IB_PORT_E_R --- AUD_IB_PORT_E_L ---
--- NC_AUD_VREF_PORT_F --- NC_AUD_VREF_PORT_E ---
--- NC_AUD_VREF_PORT_D --- NC_AUD_VREF_PORT_C ---
--- NC_AUD_IB_PORT_G_R --- NC_AUD_IB_PORT_G_L ---
--- NC_AUD_IB_PORT_H_R --- NC_AUD_IB_PORT_H_L ---
--- NC_AUD_IB_PORT_F_R --- NC_AUD_IB_PORT_F_L ---

AUD_IB_PORT B_R --- AUD_IB_PORT_B_L ---
--- AUD_IB_PORT_A_R --- AUD_IB_PORT_A_L ---
--- AUD_IB_PORT C_L --- AUD_IB_PORT C_R ---
--- AUD_IB_PORT D_R --- AUD_IB_PORT D_L ---
--- AUD_IB_PORT_E_R --- AUD_IB_PORT_E_L ---
--- NC_AUD_VREF_PORT_B --- NC_AUD_VREF_PORT_E ---
--- NC_AUD_VREF_PORT_D --- NC_AUD_VREF_PORT_C ---
--- NC_AUD_IB_PORT_F_R --- NC_AUD_IB_PORT_F_L ---

--- AUD_IB_PORT A_L --- AUD_IB_PORT_A_R ---
--- AUD_IB_PORT C_R --- AUD_IB_PORT C_L ---
--- AUD_IB_PORT D_L --- AUD_IB_PORT D_R ---
--- AUD_IB_PORT_E_R --- AUD_IB_PORT_E_L ---
--- NC_AUD_VREF_PORT_B --- NC_AUD_VREF_PORT_E ---
--- NC_AUD_VREF_PORT_D --- NC_AUD_VREF_PORT_C ---
--- NC_AUD_IB_PORT_F_R --- NC_AUD_IB_PORT_F_L ---

--- AUD_IB_PORT A_R --- AUD_IB_PORT_A_L ---
--- AUD_IB_PORT C_L --- AUD_IB_PORT C_R ---
--- AUD_IB_PORT D_R --- AUD_IB_PORT_D_L ---
--- AUD_IB_PORT_E_L --- AUD_IB_PORT_E_R ---
--- NC_AUD_VREF_PORT_B --- NC_AUD_VREF_PORT_E ---
--- NC_AUD_VREF_PORT_D --- NC_AUD_VREF_PORT_C ---
--- NC_AUD_IB_PORT_F_R --- NC_AUD_IB_PORT_F_L ---

--- AUD_IB_PORT H_L --- AUD_IB_PORT_H_R ---
--- AUD_IB_PORT_G_L --- AUD_IB_PORT_G_R ---
--- NC_AUD_IB_PORT_F_L --- NC_AUD_IB_PORT_F_R ---
--- AUD_IB_PORT_F_L --- AUD_IB_PORT_F_R ---
--- AUD_IB_PORT_C_L --- AUD_IB_PORT_C_R ---
--- AUD_IB_PORT_D_R --- AUD_IB_PORT_D_L ---
CPU CURRENT SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits.
ALL AND GATE INPUTS ARE 7V TOLERANT REGARDLESS OF INPUT POWER
1.5V S0 AND 1.05V S0 RAILS
**LCD (LVDS) INTERFACE**

Panel Power sequencing:

- FERR-250-OHM
- (NONE)

Signal aliases required by this page:

- =PP3V3_S0_VIDEO
- =PP24V_INVERTER
- =PPV_S0_LCD
- LCD_PWREN_DIV
- =PP3V3_DDC_LCD
- =PP3V3_S0_VIDEO

Panel has 3.7K pull-ups

- PANEL POWER SEQUENCING

**INVERTER INTERFACE**

Port K (HDI) are connected to LCD conns:

- LCD_PWREN_L
- LCD_PWREN_L_RC
- LCD_PWM
- SYNC_MASTER=M51_DAVE

PINS 6-9 (GND) ARE CONNECTED TO LCD CHASSIS

- SYNC_DATE=(MASTER)

Internal Display Conns

APPLE COMPUTER INC.

www.Vinafix.vn