3. All crystals & oscillator values are in hertz.

2. All capacitance values are in microfarads.

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**ALIASES RESOLVED**

Schematic / PCB #’s

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OYORA
01/23/2007 - EVT

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### BOM Options

<table>
<thead>
<tr>
<th>BOM Number</th>
<th>BOM Name</th>
<th>BOM Options</th>
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<tr>
<td>12345678</td>
<td>Module 1</td>
<td>M75_COMMON1</td>
</tr>
<tr>
<td>12345678</td>
<td>Module 2</td>
<td>M75_COMMON2</td>
</tr>
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<td>12345678</td>
<td>Module 3</td>
<td>M75_COMMON3</td>
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### M75 BOM Groups

<table>
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<th>BOM Options</th>
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<tbody>
<tr>
<td>M75_COMMON1</td>
<td>M75_COMMON1</td>
</tr>
<tr>
<td>M75_COMMON2</td>
<td>M75_COMMON2</td>
</tr>
<tr>
<td>M75_COMMON3</td>
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</tr>
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### Bar Code Labels / EEE #'s

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference</th>
<th>Critical</th>
<th>BOM Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>D34567</td>
<td>Label, 2x2, 100x100</td>
<td>123456</td>
<td>Critical</td>
<td>M75_COMMON1</td>
</tr>
<tr>
<td>D7890</td>
<td>Label, 2x2, 100x100</td>
<td>123456</td>
<td>Critical</td>
<td>M75_COMMON2</td>
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### Module Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference</th>
<th>Critical</th>
<th>BOM Options</th>
</tr>
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<tr>
<td>12345678</td>
<td>IC, 16Mbit 8-PIN SPI Serial Flash, SOIC8</td>
<td>123456</td>
<td>Critical</td>
<td>M75_COMMON1</td>
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<td>IC, 16Mbit 8-PIN SPI Serial Flash, SOIC8</td>
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<td>Critical</td>
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</tbody>
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AGREES TO THE FOLLOWING:

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PLACE R1024 NEAR ITP CONNECTOR (IF PRESENT)
**CPU VCORE HF AND BULK DECOUPLING**

- 1x 330uF, 20x 22uF 0805

**CPU VCORE VID CONNECTIONS**

**VCCP (CPU I/O) DECOUPLING**

- 1x 470uF, 6x 0.1uF 0402

**VCCA (CPU AVdd) DECOUPLING**

- 1x 10uF, 1x 0.1uF
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.

Direction of XDP module

Please avoid any obstructions

on even-numbered side of J1300

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Leave GFX_VID<3..0> and GFX_VR_EN as NC.

Tie VCC_AXG and VCC_AXG_NCTF to GND.

Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).

Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and
Internal Graphics Disable

NOTE: Must keep VDDC_TVDAC powered
Can tie the following rails to GND:
VSYNC and CRT_TVO_IREF to GND.

rails must be filtered except for VCCA_CRT.
CRT Disable / TV-Out Enable

Tie CRT_DDC Data and L_CTRL_CLK to GND.
Must power all
TVDAC rails. VCCA TVDAC and VCC_TV_DAC can
share filtering with VCCA_CTRL.

CRT Disable / TV-Out Disable

Tie CRT_VSYNC, CRT_DDC_CLK, CRT_Green*, CRT_Blue*, SDVO_CTRL, and CRT_VTO_DCOK to GND.

SDVO Output Signal Usage:

---

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Current numbers from Crestline EDS, doc #21749.

HCTF balls are Not Critical To Function
These conditions can break without impacting part performance.
Crestline Thermal Diode Pins
Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: TDB = _N
NOTE: TDE = _P
NOTE: This filter is required even if using only external graphics. VCCD_TVDAC also powers internal thermal sensors.

Current numbers from Crestline EDS Addendum, doc #20127.

VOLTAGE=1.5V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.3 MM

PP1V5_S0_NB_VCCD_TVDAC

VOLTAGE=1.25V
MIN_NECK_WIDTH=0.2 MM
MIN_LINE_WIDTH=0.4 MM
"Factory" (thru-hole) slot

DDR2 Bypass Caps
(For return current)
One cap for each side of every RPAK, one cap for every two discrete resistors
Ensure C2 and G2 resistors are close to ED-SOM connector

Memory Active Termination

Sync date: 11/14/2006
Sync master: (T9_NOME)

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ENET Enable Generation

ENET = "S0" || ("S3" && "AC" && "WOL_EN")

NOTE: S3 term is guaranteed by source of R3800 & Q3810, MUST BE S3 RAIL.

3.3V ENET FET

Vout = 1.2246V * (1 + Ra / Rb) (U3850 limit)

500 mA max output

WLAN Enable Generation

"WLAN" = "S0" || ("S3" && "AC" && "WOW_EN")

Yukon AVDDL LDO

1.9V for Yukon Ultra, 2.5V for Yukon EC

Yukon Ultra requires 1.9V on its magnetics to pass compliance tests

EC: Vout = 2.510V

NOTE: S3 term is guaranteed by FET & pull-up source, MUST BE S3 RAIL.

Yukon Power Control

Ultra Vout = 1.912V

EC: Vout = 2.510V

500 mA max output (U3850 limit)

C3850, C3851 1UF 6.3V CERM

R3800, R3805 10K MF-LF 1/16W

Q3800, Q3801, Q3810 2N7002DW-X-F SOT-363

C3855, C3856 0.033UF 5%50V CERM

Q3805, Q3810 NTR4101P SOT-23

C3811 22PF 5%50V CERM

R3811 10K MF-LF 1/16W

C3810 0.01UF 16V 10% CERM

Q3806 NTR4101P SOT-23

R3810 100K MF-LF 5%1/16W

Yukon Crystal
Lo: Beta Mode enable (1394b).

DDx Straps: Implement 1k pull-up or pull-down on port page.

Power Class:
- Power Class 4 ('100')
- Multi-port Portable systems are Power Class 4 ('100').

C4131 with internal pull-up provides PHY power-up reset.
**FireWire Phy Config Straps**

Configured PHY for:

- 2-3 Port Portable Power Class (B) — Port 1-3 Data-Start only (1394A)
- Port 1-3 Bilingual (1394B)

**Termination**
Place close to FireWire PHY

- TI Ports require 1uF even though spec calls out 2.2uF

**Late-VG Protection Power**

PPV2 PW needs to be biased at 0.2V for PM signal integrity and should be biased to 2.4V for power

PPV8 PW should be 3.3V then and for 3.0V rail

GND_CHASSIS_FW_PORT0L
GND_CHASSIS_FW_PORT1L
NOTE: Unused pins have "UNUSED" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
CPU T-Diode Thermal Sensor

GPU/Heat Pipe & Bottom Case Skin Thermal Sensor

GPU Die Thermal Sensor

Thermal Sensors

NB Thermal Diodes Not Used
Left ALS Filter
Left ALS circuit has 1K series-R
RTALS_OP_In and RTALS_OP_COMP need to be matched

Keyboard LED Driver
RM: This circuit does not use return, can tie cathode to GND on topcase flex
I2C addresses:
ADDR low => 0x30, 0x31
ADDR high => 0x32, 0x33
Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
Package Top
Desired orientation when placed on board bottom-side:
Top-through View

Sudden Motion Sensor (SMS)
SYNC_MASTER=M76_MLB
SYNC_DATE=01/18/2007
SMS_ONOFF_L
SMS_Y_AXIS
SMS_X_AXIS
SMS_MOT_EN
SMC_SMS_INT
PP3V3_S3
SMBUS_SMC_MGMT_SCL
SMBUS_SMC_MGMT_SDA
1.5V Power Supply

Vout = 1.50V
8A max output (L7620 limit)

Vout = 0.75V * (1 + Ra / Rb)

C7610
1 2
NO STUFF
100PF
50V
402
5%
CERM

R7615
1 2
1/16W
MF-LF
402
5%
0
C7615
1 2
10V
0.1UF
CERM402
20%

C7620
1 2
CASE-D2-LF
22UF
25V
20%
POLY

C7632
1 2
CRITICAL
2.5V
330UF
CASE-D2E-LF
20%
POLY

C7600
1 2
10%
10V
1UF
X5R
402

R7601
1 2
200
1/16W
MF-LF
402
1%

C7601
1 2
16V
2.2UF
10%
603X5R

R7619
1 2
1/16W
MF-LF
402
1%
200K

U7600
13 9
1
7
12
8
11
5
3
15
10
4
14
6

Q7620
5 4
1 2 3
PWRPK-1212-8
SI7114DN
CRITICAL

Q7625
5 4
1 2 3
SI7108DNS
PWRPK-1212-8
CRITICAL

X7620
1 2
SM

PLACEMENT NOTE=Place XW7620 close to L7620.

R7602
1 2
6.04K
MF-LF
1%

C7630
1 2
603X5R
10UF
20%6.3V

R7610
1 2
1/16W 1%
10K
402MF-LF

R7611
1 2
1/16W
MF-LF
402
10K
1%

L7620
1 2
CRITICAL
IHLP2525CZ-SM
1.0UH-11A

SYNC_MASTER=M76_MLB
SYNC_DATE=01/23/2007

1.5V Power Supply

GATE_NODE=TRUE
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

P1V5S0_DRVL
P1V5S0_VFB
P1V5S0_TON
P1V5S0_VBST
P1V5S0_DRVH
P1V5S0_LL
PP5V_S5
PP1V5_S0
P1V5S0_TRIP
PP1V5_S0_VDDQSNS

VOLTAGE=5V
VOLTAGE=0V
GND_P1V5S0_SGND
PPBUS_G3H
PP1V5_S0
PP1V05S0_PGOOD
P1V5P1V05S0_P5FILT

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm
GATE_NODE=TRUE

MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.6 mm

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3.3V FW PHY Supply

Vout = 3.316V
200mA max output
(Switcher limit)

Vout = 3.316V * (1 + Ra / Rb)

1.95V FW PHY Supply

Vout = 3.316V
200mA max output
(Switcher limit)
LTC2900 provides programmable reset delay which is required to play nice with ICHx PGOOD circuit. Fast wake condition is worst case. ICM can create an SS duration of 1 sec. clock (12 ms). If reset is in one well and NS+ gate is implemented, glitch filter or Other PGOOD assertion time is required for PGOODs to be valid at end of 99 ms SMC timer. If set to select on resume well, then associated PGOOD will not change during 99 ms SMC timer whatever PGOOD delays are provided.

PGOOD Monitor for GPU Rails

LTC2900 typical threshold is 90.70 (9.350%, 1.320%, 1.290%)

Mux Select Conditioning

GPU LVDS I/F

LVDS Data Mux Power Supply

Panel/Backlight Control Mux

LVDS Interface Mux

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NOTE: SEL = LOW selects port B

NOTE: New H/W and S/W challenge since NB gfx might
be powered off if using external GPU. S/W will have
decisions that is the "meat" decision. In the end, before
all decisions, PGOOD needs to be either in one well, this could mean powering off GPU supply will
be necessary before going to sleep to keep PGOODS valid.
Left ALS Connector

White colored version of 5180369

SATA HDD & IR & SIL Flex Connector

NOTE: SATA _UF_ nets cross DDR2 signals and are to remove this noise from SATA signals.

Top-Case Connector

NOTE: SATA _UF_ nets cross DDR2 signals and are to remove this noise from SATA signals.
Most CPU signals with impedance requirements are 55-ohm single-ended.

**CPU Signal Constraints**

- **Design Guide recommends FSB signals be routed only on internal layers.**
- **Design Guide recommends each strobe/signal group is routed on the same layer.**
- **DSTB complementary pairs are spaced 1:1 and routed as differential pairs.**
- **Design Guide recommends FSB signals be routed only on internal layers.**

**Note:** Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

**Source:** Santa Rosa Platform DD, Rev 0.9 (#20517), Sections 4.4 & 4.5

---

**CPU / FSB Net Properties**

- **SOURCE:** Santa Rosa Platform DD, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

---

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**PCI-Express / DMI Bus Constraints**

<table>
<thead>
<tr>
<th>signal</th>
<th>min. spacing</th>
<th>max. spacing</th>
<th>net type</th>
<th>net type</th>
<th>net type</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRT_HSYNC_L</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
<tr>
<td>CRT_HSYNC_R</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
<tr>
<td>CRT_VSYNC_L</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
<tr>
<td>CRT_VSYNC_R</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
</tbody>
</table>

**Video Signal Constraints**

<table>
<thead>
<tr>
<th>signal</th>
<th>min. spacing</th>
<th>max. spacing</th>
<th>net type</th>
<th>net type</th>
<th>net type</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRT_50S</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
<tr>
<td>CRT_55S</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
</tbody>
</table>

**Notes:**
- CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.
- CRT_50S, CRT_55S from second termination resistor to connector is 50-ohm +/- 15%.
- CRT_50S, CRT_55S from first to second termination resistor is 37.5-ohm +/- 15%.

LVDS signals are 100-ohm +/- 20% differential impedance.

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3, CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedance.

**Video Signal Constraints**

<table>
<thead>
<tr>
<th>signal</th>
<th>min. spacing</th>
<th>max. spacing</th>
<th>net type</th>
<th>net type</th>
<th>net type</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRT_50S</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
<tr>
<td>CRT_55S</td>
<td>30 mil</td>
<td>40 mil</td>
<td>L1</td>
<td>L1</td>
<td>L1</td>
</tr>
</tbody>
</table>

**Notes:**
- LVDS_100D signals are 100-ohm +/- 20% differential impedance.
- CRT & TVDAC signals single-ended impedance varies by location.

**Source:** Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5
## DDR2 Memory Bus Constraints

<table>
<thead>
<tr>
<th>Memory Net</th>
<th>Minimum Line Width</th>
<th>Allow Route</th>
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</thead>
<tbody>
<tr>
<td>MEM_CLK</td>
<td>85_OHM_SPACING</td>
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</tr>
<tr>
<td>MEM_DATA</td>
<td>85_OHM_SPACING</td>
<td></td>
</tr>
<tr>
<td>MEM_B_DQS</td>
<td>85_OHM_SPACING</td>
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## Memory Net Properties

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### Memory Constraints

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### Ethernet (Yukon) Constraints

<table>
<thead>
<tr>
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<tr>
<td>Controller Link (AMT) Constraints</td>
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<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Description</th>
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### Controller Link (AMT) Constraints

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APPLE COMPUTER INC.

SYNC_MASTER=T9_NOME
SYNC_DATE=01/17/2007

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Port 2 Not Used

FireWire Interface Constraints

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FireWire Constraints

Sync Date: 01/17/2007
Sync Master: T9_NOME

Port 2 Not Used
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### G84M Net Properties

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### GPU (G84M) Constraints

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### Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

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<td>PP1V8_MEM</td>
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<td>PWR_P2MM</td>
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Allow 0.1 mm necks for >0.1 mm lines between thru-hole SD-D1090 pins.

<table>
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<th>Net Type</th>
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### M75 Specific Net Properties

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### M75 Specific Constraints

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### M75 Rule Definitions

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