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40. ALS Sensor
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### Schematic / PCB #’s

<table>
<thead>
<tr>
<th>Description</th>
<th>Reference</th>
<th>Critical</th>
<th>SW</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVT - ENG</td>
<td>051-7261</td>
<td>01/26/07</td>
<td>Critical</td>
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</table>

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<th>Critical</th>
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<td>051-7261</td>
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<td>Critical</td>
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---

1. All resistance values are in Ohms, 0.1 Watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystals & Oscillator values are in units.
### BOM Variants

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>ALTERNATE FOR</th>
<th>DESCRIPTION</th>
<th>CRITICAL</th>
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<tbody>
<tr>
<td>530-7072</td>
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<td>530-7061</td>
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<td>530-7073</td>
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<td>530-7071</td>
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### M76 BOM Groups

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>76.01459</td>
<td></td>
</tr>
<tr>
<td>76.01456</td>
<td></td>
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<tr>
<td>76.01453</td>
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### Bar Code Labels / EEE #’s

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE EEE</th>
<th>CRITICAL</th>
<th>ROM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>826-4393</td>
<td>1</td>
<td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td>
<td>CRITICAL</td>
<td></td>
<td></td>
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</table>

### Module Parts

<table>
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<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE EEE</th>
<th>CRITICAL</th>
<th>ROM OPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>338S0386</td>
<td>1</td>
<td>IC, 88E8058, GIGABIT ENET XCVR, 64-PIN QFN</td>
<td>CRITICAL</td>
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</table>

### Alternate Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE EEE</th>
<th>CRITICAL</th>
<th>ROM OPTION</th>
</tr>
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<tbody>
<tr>
<td>335S0384</td>
<td>1</td>
<td>IC, 16MBIT 8-PIN SPI SERIAL FLASH, SOIC8</td>
<td>CRITICAL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

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**PRELIMINARY**

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3/19/07 -- Battery charge current limit circuit changes for max charge current of 4.5A.
- Deleted R8915 and made C8915 0603 size, still 0.1uF (132S0100).

3/19/07 -- Added three 0603 0 ohm resistors R4740-R4742 for EMC return current path.

- Power Control: Added U7858 to level shift PM_G2_EN to 3.42V to 5V

3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.

3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.

14.0.0

Page 15: Sync from main-line (renamed LVDS_VREFx nets).

Quick submit of T9 noME branch.  Major release will follow once changes are properly documented in Radar and revision history.

3/19/07 -- Integrated m75/mlb CSA pg. 55 & 78 through:

- L9950 changed from 152S0527 (15uH, 2.8A, 115mOhm) to 152S0585 (22uH, 2.8A, 129mOhm).

3/19/07 -- Changes to low voltage inverter for M76 piezo.
- Deleted R7525 and made C7525 0805 size, still 0.1uF (132S0201).
- Deleted R7420 and R7470 and made C7420 and C7470 0603 size, still 0.1uF (132S0100).

3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.

3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.

14.2.0

Page 15: Sync from main-line (renamed LVDS_VREFx nets).

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3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.

14.3.0

Page 15: Sync from main-line (renamed LVDS_VREFx nets).

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3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.

3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.

14.4.0

Page 15: Sync from main-line (renamed LVDS_VREFx nets).

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3/19/07 -- SMBus: moved Remote Temps from SMC B to SMC A in order to use EMC1043-5.

3/19/07 -- Added BOM table with 0 Ohm 0603 resistors at L4731,L4741.
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 929-0651 adapter board to support CPU, NB & SB debugging.

NOTE: XDP_DBRESET_L must be pulled-up to 3.3V.

Direction of XDP module

Please avoid any obstructions on non-referenced side of J1300

Direction of XDP module
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.

TV_DCONSELx to GND.

Follow instructions for LVDS and CRT & TV-Out Disable above.

Internal Graphics Disable

NOTE: Must keep VDDC_TVDAC powered

CRT & TV-Out Disable

Tie VDDC_TVDAC and VDDC_TVDAC to GND. Must power all TDAC rails. VDDC_TVDAC and VDDC_TVDAC can share filtering with VDDC_CRT.

CRT & TV-Out Disable

Tie VDDC_TV to GND and VDDC_TV to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VDDC_CRT.

CRT & TV-Out Disable

TV DCONSELx to GND. Must keep VDDC_TVDAC powered and filtered at all times.

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above. Can also tie CRT_DIN_1, CRT_DIN_2, CRT_DIN_3, SDVO_CTRL_1, and TV_SCH_1 to GND. Tie CRT_DIN_4 and CRT_DIN_5 to VDDC_TV to GND.

S-Video: DACB & DACC only

LVDS Disable

Can leave all signals NC if LVDS is not implemented.

Tie VCC_LVDS and VCCA_LVDS to GND.

If LVDS is used, VCCA_LVDS must remain powered with proper decoupling. Otherwise, tie VCC_LVDS to GND also.

Note: SR 27 says to tie LVDS_VREFP/L to GND. This causes a glitch during wake-up on LVDS data/clock pairs. A recommendation is to float both signals, see Radar P867836.

TV-Out signal usage:

S-Video: S-1 & S-2 only

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs must remain powered to avoid R-star feedbacks.

TV-Out disabled / CRT enabled

Tie VDDC_TVDAC and VDDC_TVDAC to GND. Must power all TVDAC rails. VDDC_TVDAC and VDDC_TVDAC can share filtering with VDDC_CRT.

CRT enabled / TV-Out enabled

Tie VDDC_TV to GND and VDDC_TV to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VDDC_CRT.
HCTF balls are Not Critical To Function

These connections can break without impacting part performance.
Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

NOTE: TDB = _N
NOTE: TDE = _P
Current numbers from Crestline EDS Addendum, doc #20127.

NOTE: This filter is required even if using only external graphics. 
SCE_C076A also powers internal thermal sensors.

22000pF-1000mA C2201

These 2 caps should be
VOLTAGE=1.5VMIN_NECK_WIDTH=0.2 MM

C2206

NO STUFF

100 mA

(1.7V - 5.5V) 100 mA

C2265

1UF 10%

CERM6.3V

19

OUT

C2265

1

SOT23-5 U2265

19

VOLTAGE=1.25VMIN_NECK_WIDTH=0.2 MM

C2210

0.01UF 402

16V 15%

CERM402

C2211

2.5V 220UF

POLY6.3V

C2226

402

10%

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84 15

6.3V 10%

CERM402

C2262

L2220

22UF

PLACEMENT_NOTE=Place in GMCH cavity

PLACEMENT_NOTE=Place in GMCH cavity

PLACEMENT_NOTE=Place in GMCH cavity

PLACEMENT_NOTE=Place in GMCH cavity

C2213

603

1

C2260

1

0.01UF 402

1/16W 5%

F4 1/10W 5%

GND_DPLL_ESR

R2299

NO_TEST=TRUE

NO_TEST=TRUE

NO_TEST=TRUE

NO_TEST=TRUE

C2214

0.47UF 402

1/16W 5%

402MF-LF

CERM402

C2215

84 15

6.3V 10%

CERM402

C2261

0.1uF 402

1/16W 5%

CERM402

C2216

0.1uF 402

10%

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Current numbers from Crestline EDS Addendum, doc #20127.
**NOTE: DPRSLPVR HAS INT 20K PD ENABLED**

**FOR STRAPPING FUNCTION**

**AT BOOT/RESET FOR STRAPPING FUNCTION**

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**SIZE**

**REV.**

**SYNC_DATE=04/02/2007SYNC_MASTER=M75_MLB**

**SB Pwr Mgt, GPIO, Clink**

**SYNC_DATE=04/02/2007**

**PREFIX DATE=04/02/2007**

**OFSHT**

**NONE**

**051-7261**

**C2501 C2500**

**0.1uF 0.1uF**

**2 1**

**R2525 16V X5R 10%**

**R2529 16V X5R 10%**

**402 402 402 402**

**1/16W 1/16W 1/16W 1/16W**

**1% 1% 1% 1%**

**C2501 C2500**

**0.1uF 0.1uF**

**2 1**

**R2525 16V X5R 10%**

**R2529 16V X5R 10%**

**402 402 402 402**

**1/16W 1/16W 1/16W 1/16W**

**1% 1% 1% 1%**

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<table>
<thead>
<tr>
<th>Component</th>
<th>Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCSUS1_5</td>
<td>1130</td>
</tr>
<tr>
<td>VCCSUS3_3</td>
<td>1130</td>
</tr>
<tr>
<td>VCCSUS1_05</td>
<td>1130</td>
</tr>
<tr>
<td>VCCSUS1_5</td>
<td>1130</td>
</tr>
<tr>
<td>VCCDMIPLL</td>
<td>1130</td>
</tr>
<tr>
<td>VCC1_5_A</td>
<td>1130</td>
</tr>
<tr>
<td>VCC1_5_A24</td>
<td>1130</td>
</tr>
<tr>
<td>VCCSATAPLL</td>
<td>1130</td>
</tr>
<tr>
<td>VCC1_5_A</td>
<td>1130</td>
</tr>
<tr>
<td>VCC1_5_A</td>
<td>1130</td>
</tr>
</tbody>
</table>

**Note:**
- VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
- VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.
- Current figures provided assume 1.5V.

**Scale:**
- Current numbers from IC Summit Max Power Estimates Rev 2.0, also #611194.
RTC Power Sources

Platform Reset Connections
Unbuffered

SB RTC Crystal

System Reset "Button"

VRMPWRGD Inverter

PWROK Circuit

CPU VCore ForcePSI

Platform Reset Connections

Unbuffered

SB Misc

SB Misc
CLK Termination

(Notes: Host/DMI/GFX clock termination removed. Silego SL8GLP534 or equiv. support only)

CLKREQ Controls

(R3046 - R3047)

CPU Clock Select

(R3034 - R3035)

(Reserved for TPM PCI 33Mhz)

Unused Clocks

(Apple Computer Inc.)

Clock Termination

(April 2007)

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One cap for each side of every SPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector
Lo: Beta Mode enable (1394b).

Strap via alias on port page.

Hi: Data-Strobe only (1394a).

Implement 1K pull-up or pull-down on port page.

Multi-port Portable systems are Power Class 4 ('100').

Single-port / Desktop systems are Power Class 0 ('000').

VOLTAGE=3.3V

MIN_NECK_WIDTH=0.22 mm

MIN_LINE_WIDTH=0.38 mm
FireWire Port Power Switch

Current Limit/Active Late-VG Protection

Late-VG Event Detection

FireWire Port Power Switch

Current Limit/Active Late-VG Protection

Late-VG Event Detection

FireWire Port Power Switch

Current Limit/Active Late-VG Protection

Late-VG Event Detection
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

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Battery Current Sense

Battery Charger Thermal Sensor

DCIn Current Sense

(Tm0P) R:0x93, W:0x92
Left ALS Filter

Left ALS circuit has 1K series-R

Right ALS Circuit

RTALS_OP_IN and RTALS_OP_COMP need to be matched

Keyboard LED Driver

WF: This circuit does not use return, can tie cathode to GND on topcase flex
I2C addresses:
A0/A9 low -> 0x30, 0x31
A0/A9 high -> 0x32, 0x33
Aliased SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:
Package Top

Desired orientation when placed on board bottom-side:
Top-through View

Sudden Motion Sensor (SMS)
SYNC_MASTER=M75_MLB SYNC_DATE=12/04/2006
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

EN3 can float or tie to VREG5 for automatic 3.3V LDO enable

=PP5V_S5_P5VP3V3

=PP3V3_S5_REG

VOLTAGE=0V

5.5A max output

Vout = 3.3V

5.5A max load when EN5 high

50uA max load when EN5 & EN3 high

VOLTAGE=5V

MIN_NECK_WIDTH=0.20 mm
MIN_LINE_WIDTH=0.25 mm

VOLTAGE=2V

MIN_NECK_WIDTH=0.20 mm

50V / 3.3V Power Supply

MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.6 mm

CRITICAL

GATE_NODE=TRUE
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
MIN_LINE_WIDTH=0.6 mm

GATE_NODE=TRUE

SWITCH_NODE=TRUE

TIP

NOTE: EN & EN3 can float or tie to VIN for automatic 5V LDO mode

EN can float or tie to VIN for automatic 3.3V LDO mode

When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.
3.3V FW PHY Supply

1.95V FW PHY Supply

Backup power in case of FW bus VP short to keep PHY powered.

Vout = 3.316V
200mA max output (Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)

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Backup power in case of FW bus
VP short to keep PHY powered.

Vout = 3.316V
200mA max output (Switcher limit)

Vout = 1.25V * (1 + Ra / Rb)
3.425V "G3Hot" Supply

Supply needs to guarantee 3.15V delivered to SMC VRef generator.

1.5V / 1.05V PWRGD Circuit

Required when 1.5V R0 and 1.05V SO are in regulation.

Other S0 Rails PWRGD Circuit

Does not include SPO rails.

NOTE: 0.9V/2.5V is not checked!

Other S0 Rails PWRGD Circuit

Does not include SPO rails.
LTC2900 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V) = PP2V5_GPU_LTC2900

= PP3V3_GPU

= RSVD_EXTGPU_LVDS_EN

= EXTGPU_LVDS_EN

LTD29000 typical threshold is 93.5% (3.055V, 2.325V, 1.685V, 1.120V)

Fast wake condition is worst case. ICHx can wake in 12 Location of 1 sec clock (24 us). If mux select is on core well and N/NR gate is implemented, glitch filter or other FGOOD assertion time (see for PGOODs for be valid at end of 99 us 2 sec timers. If mux select on resume well, then observed PGOOD will not change during 30 second period of whatever PGOOD delay is provided.

NOTE: New H/W and S/W challenge since NB gfx might be necessary before going to sleep to keep PGOODs valid.
IR & Sleep LED Connector

Top-Case Connector

Inverter Connectors

Bluetooth (M13P) & SATA HDD Flex Connector

M76 Specific Connectors

Apple Computer Inc.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

Design Guide recommends FSB signals be routed only on internal layers.

DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Intel says to route with 7 mil spacing without noting: 7 mil gap is for VCCSense pair, which

Preliminary
Video Signal Constraints

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5

PCI-Express / DMI Bus Constraints
**Clock Signal Constraints**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Min Neck Width</th>
<th>Max Neck Length</th>
<th>Diffpair</th>
<th>Primary Gap</th>
<th>Neck Gap</th>
<th>Physical Rule Set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>100_OHM_DIFF</td>
<td>STANDARD</td>
</tr>
</tbody>
</table>

**Clock Net Properties**

**SMC SMBus Net Properties**

**Clock & SMC Constraints**

---

*SOURCE: Santa Rosa Platform DD, Rev 1.0 (#21112), Sections 14.1 - 14.6*
### GDDR3 Frame Buffer Signal Constraints

<table>
<thead>
<tr>
<th>Net</th>
<th>Clock Type</th>
<th>Layer</th>
<th>Width</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_50SE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GDDR3_40R50SE</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Video Signal Constraints

<table>
<thead>
<tr>
<th>Net</th>
<th>Clock Type</th>
<th>Layer</th>
<th>Width</th>
<th>Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB_A_DQ_BYTE1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB_A_WDQS0</td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

### GDDR3 FB A/B Net Properties

<table>
<thead>
<tr>
<th>Net</th>
<th>Operation</th>
<th>Position</th>
<th>Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_50SE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GDDR3_40R50SE</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### GDDR3 FB C/D Net Properties

<table>
<thead>
<tr>
<th>Net</th>
<th>Operation</th>
<th>Position</th>
<th>Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB_B_DQM_L&lt;7&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB_B_DQM_L&lt;6&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### GB4M Net Properties

<table>
<thead>
<tr>
<th>Net</th>
<th>Operation</th>
<th>Position</th>
<th>Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>GDDR3_50SE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>GDDR3_40R50SE</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### GPU (G84M) Constraints

<table>
<thead>
<tr>
<th>Net</th>
<th>Operation</th>
<th>Position</th>
<th>Timing</th>
</tr>
</thead>
<tbody>
<tr>
<td>FB_B_DQM_L&lt;7&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB_B_DQM_L&lt;6&gt;</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Note:** The table and diagram are placeholders and not actual content from the document. The document appears to be a technical specification sheet for electronic components and signals, detailing signal constraints, net properties, and other technical data.
Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for GMCH fanout.

Allow 0.1 mm necks for >0.1 mm lines between thru-hole SO-DIMM pins.

Graphics Constraint Relaxations

Alternate diffpair width/gap through BGA fanout areas (95-ohm diff)

SIM Card Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Width (mm)</th>
<th>Gap (mm)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min.</td>
<td>0.03</td>
<td>0.15</td>
<td>No</td>
</tr>
<tr>
<td>Max.</td>
<td>0.05</td>
<td>0.18</td>
<td>No</td>
</tr>
</tbody>
</table>

M76 Specific Net Properties

<table>
<thead>
<tr>
<th>Net Name</th>
<th>Net Type</th>
<th>Min. Width (mm)</th>
<th>Max. Width (mm)</th>
<th>Min. Gap (mm)</th>
<th>Max. Gap (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGA_SYNC</td>
<td>TMDS</td>
<td>0.20</td>
<td>0.25</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>VGA_55S</td>
<td>LVDS</td>
<td>0.20</td>
<td>0.25</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>TMDS_100D</td>
<td>LVDS</td>
<td>0.20</td>
<td>0.25</td>
<td>0.25</td>
<td>0.30</td>
</tr>
<tr>
<td>LVDS_100D</td>
<td>LVDS</td>
<td>0.20</td>
<td>0.25</td>
<td>0.25</td>
<td>0.30</td>
</tr>
</tbody>
</table>

M76 Specific Constraints

<table>
<thead>
<tr>
<th>Constraint Type</th>
<th>Min. Value</th>
<th>Max. Value</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIM Card Width</td>
<td>0.03</td>
<td>0.05</td>
<td>No</td>
</tr>
<tr>
<td>SIM Card Gap</td>
<td>0.15</td>
<td>0.18</td>
<td>No</td>
</tr>
</tbody>
</table>

**NOTE:** The above constraints and relaxations are preliminary and subject to change.
### M75/M76 Board-Specific Spacing & Physical Constraints

#### Table: Physical Rule Set

<table>
<thead>
<tr>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>DiffPair Primary Gap</th>
<th>DiffPair Neck Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td></td>
<td></td>
<td>100_OHM_DIFF</td>
<td></td>
</tr>
<tr>
<td>BOTTOM</td>
<td></td>
<td></td>
<td>100_OHM_DIFF</td>
<td></td>
</tr>
</tbody>
</table>

#### Table: Spacing & Assignment

<table>
<thead>
<tr>
<th>Layer</th>
<th>ON LAYER?</th>
<th>Min Width</th>
<th>Min Width Allow Route</th>
<th>Min Width Allow Route</th>
<th>Max Width</th>
<th>Max Width Allow Route</th>
<th>Max Width Allow Route</th>
<th>Min Space</th>
<th>Min Space Allow Route</th>
<th>Min Space Allow Route</th>
<th>Max Space</th>
<th>Max Space Allow Route</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP</td>
<td>YES</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
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<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
</tr>
<tr>
<td>BOTTOM</td>
<td>YES</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
<td>0.125 MM</td>
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<tr>
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<td>0.100 MM</td>
<td>0.100 MM</td>
<td>0.100 MM</td>
<td>0.100 MM</td>
<td>0.100 MM</td>
</tr>
</tbody>
</table>

---

**Note:** 100_OHM_DIFF is for select 100-ohm differential pairs with custom difficulties through Rules. Default width/spacing is 100-ohm differential, but pairs can stack 95-ohm without DRC.

---

**Default width/spacing is 100-ohm differential, but pairs can neck to 95-ohms without DRC.**