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3. All crystals & oscillator values are in hertz.

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</table>

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11. CPU Debugging & VID
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13. MCP CPU Interface
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For any questions or concerns, please contact Apple Inc.

Power Block Diagram

Apple Inc.

www.vinafix.vn
Module Parts

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>QTY</th>
<th>DESCRIPTION</th>
<th>REFERENCE DES</th>
<th>CRITICAL</th>
<th>BOM OPTION</th>
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<td>1</td>
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Bar Code Labels / EEE #'s

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M98 BOM Groups

<table>
<thead>
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<th>BOM OPTION</th>
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<tr>
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<td>M98_COMMON, EEE_0ZB, CPU_2_4GHZ, FB_256_HYNIX</td>
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<td>630-9337</td>
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M98 COMMON ALTERNATE, COMMON, M98_COMMON1, M98_COMMON2, M98_COMMON3, M98_DEBUG, M98_PROGPARTS

<table>
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M98 COMMON, EEE_0ZC, CPU_2_5GHZ, FB_256_QIMONDA

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M98 COMMON, EEE_2NJ, CPU_2_8GHZ, FB_512_QIMONDA

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M98_COMMON, EEE_2NH, CPU_2_8GHZ, FB_512_SAMSUNG

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</tbody>
</table>

Part number 826-4393 is marked as CRITICAL in the BOM configuration.
1.05V to 3.3V Level Translator (M98: On ICT Fixture)

From XDP connector or via level translator

U1000 CPU

To XDP connector and/or level translator

U1400 MCP

U8000 GPU

U9200 GMUX

GMUX CPLD Programming Port

Critical 1909782 M-RT-SM

JTAG Scan Chain

APPLE INC.
Functional Test Points

Fan Connectors

LVDS Connectors

Speaker Connectors

SATA ODD Connectors

EXCARD Connector

POWER RAILS

KEYBOARD CONN

IPD_FLEX_CONN

ICT Test Points

CPU FSB NO_TESTs

-3
-2
-1
CPU VCORE HF AND BULK DECOUPLING

- 1x 330μF, 25x 22μF 0805

VCCP (CPU I/O) DECOUPLING

- 1x 470μF, 6x 0.1μF 0402

VCCA (CPU AVdd) DECOUPLING

- 1x 470μF, 6x 0.1μF 0402
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 920-0620 adapter board to support CPU, MCP debugging.

MCP79-specific pinout

Direction of XDP module

Please avoid any obstructions on even-numbered side of J1300
3.3V Interface Pull-ups

These internal pull-ups are missing in Revs A01 & A01P.

- JTAG_MCP_TMS
- JTAG_MCP_TDI
- PM_LATRIGGER_L
- PM_SYSRST_DEBOUNCE_L
- SMC_WAKE_SCI_L
- PM_BATLOW_L
- PM_PWRBTN_L
- SMC_RUNTIME_SCI_L
- PCIE_WAKE_L
- JTAG_MCP_TMS
- JTAG_MCP_TDI
- PM_LATRIGGER_L
- PM_SYSRST_DEBOUNCE_L
- SMC_WAKE_SCI_L
- PM_BATLOW_L
- PM_PWRBTN_L
- SMC_RUNTIME_SCI_L
- PCIE_WAKE_L

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MCP79 A01 Silicon Support
RTC Power Sources

MCP 25MHz Crystal

MCP S0 PWRGD & CPU_VLD

RTC Crystal

Reset Button

Platform Reset Connections

LPC Reset (Unbuffered)

PCIE Reset (Unbuffered)

RTC Power Sources represents the power sequencing connections to the RTC and CPU.

MCPSEQ_SMC represents MCP79 'MLB' power sequencing connections, which results in earlier POWER and CPU if it is enabled.

MCPSEQ_SMC should guarantee CPU_VLD does not go high before CPU power up (which is 50-100ms after CPU power up connection).

NOTE: If CPU_VLD deasserts during S0 MCP79 will take system to S5 immediately.

Reset Button represents the reset button connections to the CPU and LPC.
SO-DIMM A and SO-DIMM B Vref settings should be margined separately (i.e. not simultaneously) due to current limitation of TPS51116 regulator.
**DDR3 RESET Support**

MCP's cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

1. 0.7V input must be stable before 1.5V starts to rise to avoid glitch on MEM_RESET_L.

3. 3.3V input must be stable before MCP79 cannot control this signal directly since it must be high in sleep and MCP MEM rails are not powered in sleep.

**DDR3 Support**

WWW.VINAFIX.VN
**WLAN Enable Generation**

"WLAN" = (!S2) && "AP_PWR_EN" is (!S0) || (!S1). 

**NOTE:** S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

**NOTE:** MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

**RTL8211 25MHz Clock**

**NOTE:** MCP79 can provide 25MHz clock, but clock runs whenever RMGT rails are powered. Designs must ensure PHY is powered whenever RMGT rails are, or use separate crystal.

**Ethernet & AirPort Support**

**SYNC_MASTER** = SUMA_M98_MLB 
**SYNC_DATE** = 07/01/2008

---

**3.3V ENET FET**

- Pull-up to +3.3V power FET.

**1.05V ENET FET**

- Pull-up to +1.05V power FET.

---

**R3800**

S3805

S3801

---

**C3810**

R3810

---

**Q3805**

C3805

---

**R3895**

Q3801

---

**C3840**

Q3840

---

**R3800**

Q3805

---

**C3841**

Q3841

---

**R3800**

Q3805

---

www.vinafix.vn
Place one of 0.1uf cap close to each center tap pin of transformer.

Transformers should be mirrored on opposite sides of the board.
Page Notes

Power aliases required by this page:
- PPBUS_S5_FWPWRSW (system supply for bus power)
- PPV3_FW_SUMNODE (power passthru summation node)

Input aliases required by this page:
NONE

BOM options provided by this page:
- FWLATEGV_3V_REF Hysteresis:
  - 2.95V when port power is on
  - 2.81V on late Vg event and port power is off

FireWire Port Power Switch

Late-VG Event Detection

Enable this port when machine is running or on AC.

Part Number | Qty | Description | Reference | Critical | Bom Option
--- | --- | --- | --- | --- | ---
R4210 | 1 | 10K | MF-LF | 1% | 1/16W
C4210 | 2 | 0.1UF | CERM10V20% | 5% | 402

www.vinafix.vn
We can add protection to 5V if we want, but leaving NC for now

USB/SMC Debug Mux

Port Power Switch

Left USB Port A

Place L4600 and L4605 at connector pin 514-0606

External USB Connectors

Www.vinafix.vn
NOTE: Unused pins have "SMC_PWM" names. Unused pins designated as outputs can be left floating, those designated as inputs require pull-ups.

NOTE: F34 and F35 are shorted. F35 could be spared.

NOTE: SMS interrupt can be active high or low, rename not accordingly. If SMS interrupt is not used, pull up to SMS rail.
**CURRENT FROM BATTERY TO PBUS**

**MCP Voltage Sense / Filter**

- **LOAD SIDE:**
  - XW5399 = PP3V42_G3H_CPUCOREISNS
  - XW5359 = PP3V42_G3H_BMON_ISNS

- **REGULATOR SIDE:**
  - CHGR_CSO_R_N
  - CHGR_CSO_R_P

**MCP Voltage Sense / Filter**

- **LOAD SIDE:**
  - XW5309 = PP3V42_G3H_BMON_ISNS

**Current & Voltage Sensing**

- **SHT OF**
  - 46 96

**Monitors Battery Discharge Current from Battery to PBUS**

- **INA213** has gain of 50V/V

- **CPU VCore High Side Current Sensor**

- **CPU VCore Load Side Current Sensor / Filter**

- **Consider INA211 (Gain 500 version) since I=4.93 Amps across R5388**

**DCIN Current Sense Filter**

- From DC close to SMC

**BMON Current Sense** - Entire circuit must be near SMC (U4900)

- Place near U4900 center

**Current & Voltage Sensing**

- II NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
- II NOT TO REPRODUCE OR COPY IT
- III TO MAINTAIN THE DOCUMENT IN CONFIDENCE
- MIN NECK WIDTH = 0.20 mm
- VOLTAGE = 18.5V
- MIN LINE WIDTH = 0.20 mm

**www.vinafix.vn**
**CPU Proximity/CPU Die/Right Fin Stack**

- Detect CPU Die Temperature
  - Place U5501 near GPU
  - Placement note:

- Detect Right Fin Stack Temperature
  - Place Q5501 on bottom side
  - Placement note:

**Battery Charger Proximity**

- Battery Charger Proximity
  - Placement note:

**MCP Proximity/MCP Die/Right Heat Pipe**

- Detect MCP Die Temperature
  - Place U5500 near battery
  - Placement note:

**GPU Proximity/GPU Die/Left Heat Pipe**

- Detect GPU Die Temperature
  - Place U5550 near GPU
  - Placement note:

**Thermal Sensors**

- TEMP SENSOR HAS ADDRESS WRITE:0X92, READ: 0X93
- Note: EMC1403 can perform Beta Compensation for External Diode 1 only
- TEMP SENSOR HAS ADDRESS WRITE:0X92, READ: 0X93
- Note: EMC1403 can perform Beta Compensation for External Diode 1 only

**Note:** EMC1403 can perform Beta Compensation for External Diode 1 only.
**BOOBOOSTER +18.5VDC FOR SENSORS**

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- RIPPLE TO MEET ERC
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 7MS
- R5812,R5813,R5815 MODIFIED

**IPD FLEX CONNECTOR**

**3V3 LDO FOR IPD**

**Keyboard LED Driver**

To detect Keyboard backlight, SMC will tristate SMC_SYS_KBDLED:
- LOW = keyboard backlight present
- HIGH = keyboard backlight not present
- BOM OPTION: KBDLED, YES
- R5853 ALWAYS PRESENT

**KBD BACKLIGHT CONNECTOR**
Digital SMS

Pull-up required if SMS_INT_L not used.

-1V3V3_SMS

R5932
-1V3_SMS_SCL
-1V3_SMS_SDA

SMS_INT_L

R5931
-1V3_SMS_INT

Stuff R5931 and NoStuff R5932 to use U5930

NoStuff R5931 AND Stuff R5932 if U5930 is not used

Analog SMS

R5921 Pulls up SMS_PWRDN to turn off SMS when pin is not being driven by SMC

Desired orientation when placed on board top-side:

Circle indicates pin 1 location when placed in correct orientation

Sudden Motion Sensor (SMS)

www.vinafix.vn
 SPI_CLK
<table>
<thead>
<tr>
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<th>SPI_MOSI</th>
<th>SPI_CLK</th>
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<td>0</td>
</tr>
<tr>
<td>42 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>25 MHz</td>
<td>1</td>
<td>0</td>
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25MHz is selected with R6190 and R6191
Any of the 8 frequencies can be selected
with R6190, R6191, R6192 and R6193

SPI_ROM

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www.vinafix.vn
Pseudo-Diff Line-In Filter

GAIN = -5.4DB  AV = 0.52
FC = 1.8 HZ

FC = 1.8 HZ
GAIN = -5.4DB  AV = 0.52

www.vinafix.vn
Headphone Amplifier (MAX9724A)
APN: 353S1637

1st Order DAC Filter
HP: 3.52 HZ LP: 34 KHZ
VOLTAGE GAIN: 1.53

---
MagSafe DC Power Jack

1-Wire OverVoltage Protection

3.425V "G3Hot" Supply

Supply needs to guarantee 3.21V delivered to SMC Vref generator

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3.425V "G3Hot" Supply

Supply needs to guarantee 3.21V delivered to SMC Vref generator
MCP79 Rev A01 requires higher core & analog voltage
Vout = 0.75V * (1 + Ra / Rb)

6A max output

(f = 360 kHz)

M99 differences from last sync on 12/03/07 to MLB:

1. Tied THERMAL_PAD to PGND. GND and THERMAL_PAD disconnected.

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Misc Power Supplies

1.8V S0 Switcher / 1.0VFW Switcher

MCP 1.05V AUXC Supply
In order to support suspending rail, hardware must guarantee that MEM_CKE signals are low when VTT rail is turned off, and remains low until after rail turns back on or DIMMs are powered. MCP79 DDR pad leakage is high enough that nvidia recommends unpowering during sleep.

MCP79 DDR FETs
MCP79 DDR pad leakage is high enough that nvidia recommends unpowering during sleep.

1.05V S0 FET
In order to support suspending rail, hardware must guarantee that MEM_CKE signals are low when VTT rail is turned off, and remains low until after rail turns back on or DIMMs are powered. MCP79 DDR pad leakage is high enough that nvidia recommends unpowering during sleep.

1.5V S0 FET
In order to support suspending rail, hardware must guarantee that MEM_CKE signals are low when VTT rail is turned off, and remains low until after rail turns back on or DIMMs are powered. MCP79 DDR pad leakage is high enough that nvidia recommends unpowering during sleep.

3.3V GPU FET
In order to support suspending rail, hardware must guarantee that MEM_CKE signals are low when VTT rail is turned off, and remains low until after rail turns back on or DIMMs are powered. MCP79 DDR pad leakage is high enough that nvidia recommends unpowering during sleep.

Power FETs
MCP79 DDR pad leakage is high enough that nvidia recommends unpowering during sleep.

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Power inputs must be pulled down if not used.

Sum of peak currents: 240mA

Place at AG9

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I2CS addr fixed at 0x9E,0x9F

I2CS must be pulled up if not used.
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LVDS Display Connector

- VOLTAGE = 3.3V
- MIN LINE WIDTH = 0.5 mm
- MIN NECK WIDTH = 0.25 mm

- PP3V3_SW_LCD
- PP3V3_S0_DDC_LCD

- C9010 1 2
- C9001 1 2
- R9000 1 2
- Q9000 1 2 3 4
- J9000

- SMD_FDC638P_G

- 518S0651

- CRITICAL DLP11S 90-OHM-100MA

- Panel has 2k pull-ups
- 100K pull-ups are for no-panel case (development).

- 0.1UF X5R 16V 402
- 100K 1/16W 5%
- SS M3K15FV SOD-VESM-HF
LVDS Transmitter Termination

All isolated LVDS outputs require this termination.

PLACEMENT_NOTE=Place at U9200 (All 24 resistors)

LVDS A_CLK_P
LVDS_B_DATA_N<0>
LVDS_B_DATA_N<2>
LVDS_B_DATA_P<1>
LVDS A_DATA_N<0>
LVDS A_DATA_N<1>

All emulated LVDS outputs require this termination.

PLACEMENT_NOTE=Place at U9200

LVDS_CONN_A_DATA_P<2>
LVDS_CONN_B_DATA_N<0>
LVDS_CONN_B_CLK_P
LVDS_CONN_A_DATA_P<1>
LVDS_CONN_A_CLK_P
LVDS_CONN_A_DATA_N<0>
LVDS_CONN_A_DATA_P<0>
LVDS_CONN_A_CLK_P

DisplayPort Mux

LVDS DDC MUX

Muxed Graphics Support

REV. C

SYNC_DATE=07/10/2008

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Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm pull-up to DP_PWR.
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DRAWING NUMBER
SHEET OF
SIZE

MOSFET
CHANNEL
RDS(ON)
FDC638APZ
P-TYPE
0.4 A (EDP)
LOADING
43 mOhm @ 4.5V

2AMP-32V
0402-HF

84

402
1/16W
MF-LF

301K
1%

147K
402
1/16W
MF-LF

0.1UF
402
X5R
10%
16V

SSOT6-HF
FDC638APZ_SBMS001

5%
402
MF-LF
1/16W
4.7K

SOT563
SSM6N15FEAPE

9 85
26

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2.5V/1.2V S3 Switcher

Vout = 0.6V * (1 + Ra/Rb)

- Switcher limit
- Switcher limit
- 0.25 MHz
- 2.25 MHz

Misc Power Supplies
SYNC_MASTER=MUXGFX
SYNC_DATE=02/01/2008

=PP3V3_S0_P1V2P2V5
=PP2V5_S0_REG
P1V2S0_VFB
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
SWITCH_NODE=TRUE
P1V2S0_SW
P2V5S0_VFB
P2V5S0_EN
P2V5S0_SW
P2V5S0_EN
=PP1V2_S0_REG

apple.com
Some signals require 27.4-ohm single-ended impedance. 

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

Intel Design Guide recommends FSB signals be routed only on internal layers.

Design Guide recommends each strobe/signal group be routed on the same layer.

Signals within each 1x group should be matched to CPU clock, +/-1000 mils.

Signals within each 2x group should be matched within 20 ps. ADTSB#s should be matched +/-300 ps.

DSTB# complementary pairs should be matched within 1 ps of each other, all DSTB#s matched to +/-300 ps.

Signals within each 4x group should be matched within 5 ps of strobe.

FSB 4X signals / groups shown in signal table on right.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

MCP FSB COMP Signal Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.5

FSB Clock Constraints

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

CPU Design Guide recommends each strobe/signal group is routed on the same layer.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#22254), Sections 4.2 & 4.3

CPU Signal Constraints

MCP FSB COMP Signal Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v01), Section 2.2.4

FSB Interface DG (DG-03328-001_v01), Section 2.2.5
DQ/A/BA/cmd signal spacing is 3x dielectric, DQS/CLK is 4x dielectric.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

MCP MEM COMP Signal Constraints

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.3.4

- A/BA/cmd signals should be matched within 5 ps of CLK pairs.
- DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.
- DQ signals should be matched within 5 ps of associated DQS pair.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.

Memory Net Properties

- DQS intra-pair matching should be within 1 ps, no inter-pair matching requirement.
- DQ signals should be matched within 5 ps of associated DQS pair.

All memory signals maximum length is 1.005 ps. CLK minimum length is 594 ps (lengths include substrate).

DQS intra-pair matching should be within 1 ps, inter-pair matching should be within 180 ps.
### SATA Interface Constraints

Source: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

- Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
- DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
- DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
- 50-ohm from first to second termination resistor.

### Analog Video Signal Constraints

- LVDS intra-pair matching should be 3 ps. Pairs should be within 150 nm of clock length.
- DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
- Max length of LVDS/DisplayPort/TMDS traces: 32 inches.

### Digital Video Signal Constraints

- LVDS intra-pair matching should be 3 ps. Pairs should be within 150 nm of clock length.
- DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
- Max length of LVDS/DisplayPort/TMDS traces: 32 inches.

### SATA Interface Constraints

Source: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.
### FireWire Interface Constraints

<table>
<thead>
<tr>
<th>Port</th>
<th>FW_TP</th>
<th>FW_P0_TPA</th>
<th>FW_P0_TPB</th>
<th>FW_P1_TPA</th>
<th>FW_P1_TPB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td></td>
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### FireWire Net Properties

<table>
<thead>
<tr>
<th>FIREWIRE_NET</th>
<th>NETgetProperty</th>
<th>MAXDIFF</th>
<th>DIFFPAIR</th>
<th>DIFFPAIR</th>
<th>NECK</th>
<th>NECK</th>
<th>MIN_WIDTH</th>
<th>MAX_LENGTH</th>
<th>PHYSICAL_RULE_SET</th>
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</thead>
<tbody>
<tr>
<td>Port 2 Not Used</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<th>DIFFPAIR</th>
<th>DIFFPAIR</th>
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<th>MAX_LENGTH</th>
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<tr>
<td>Port 2 Not Used</td>
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</tbody>
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### SMBus Net Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>MIN. LINE W.</th>
<th>ALLOW ROUTE</th>
<th>MIN. NECK WIDTH</th>
<th>MAX. NECK LENGTH</th>
<th>DIFFPAIR PRIMARY</th>
<th>GAP</th>
<th>DIFFPAIR NECK</th>
<th>GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSO</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
<td>0.1 MM</td>
<td></td>
</tr>
<tr>
<td>CHGR_CSI</td>
<td>0.1 MM</td>
<td>1TO1 DIFFPAIR</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
<td>0.1 MM</td>
<td></td>
</tr>
</tbody>
</table>

### SMBus Charger Net Properties

<table>
<thead>
<tr>
<th>Name</th>
<th>MIN. LINE W.</th>
<th>ALLOW ROUTE</th>
<th>MIN. NECK WIDTH</th>
<th>MAX. NECK LENGTH</th>
<th>DIFFPAIR PRIMARY</th>
<th>GAP</th>
<th>DIFFPAIR NECK</th>
<th>GAP</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
<td>0.1 MM</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
<td>0.1 MM</td>
<td>STANDARD</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
<td>0.1 MM</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>0.1 MM</td>
<td>1TO1 DIFFPAIR</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
<td>0.1 MM</td>
<td></td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SDA</td>
<td>0.1 MM</td>
<td>1TO1 DIFFPAIR</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
<td></td>
<td>0.1 MM</td>
<td></td>
</tr>
</tbody>
</table>

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**SMC Constraints**

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DisplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
### PCB Rule Definitions

**NOTE:** PCB rules in 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

<table>
<thead>
<tr>
<th>LINE-TO-LINE SPACING</th>
<th>LAYERS</th>
<th>WEIGHT</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.140 MM</td>
<td>5X</td>
<td></td>
</tr>
<tr>
<td>0.150 MM</td>
<td>4X</td>
<td></td>
</tr>
<tr>
<td>0.160 MM</td>
<td>3X</td>
<td></td>
</tr>
<tr>
<td>0.170 MM</td>
<td>2X</td>
<td></td>
</tr>
<tr>
<td>0.180 MM</td>
<td>1X</td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** From this PCB rule definition, the following rule has been removed:

- 1.5:1 SPACING = 0.15 MM

<table>
<thead>
<tr>
<th>SPACING RULE SET</th>
<th>AREA_TYPE</th>
<th>NET_SPACING_TYPE1</th>
<th>NET_SPACING_TYPE2</th>
</tr>
</thead>
</table>
| 4:1ENSION
| 5X_DIELECTRIC    | 0.350 MM  |                   |                   |
| 2X_DIELECTRIC    | 0.210 MM  |                   |                   |
| 3X_DIELECTRIC    | 0.140 MM  |                   |                   |
| 4X_DIELECTRIC    | 0.120 MM  |                   |                   |
| 5X_DIELECTRIC    | 0.100 MM  |                   |                   |

**NOTE:** PCB rule definition has been updated to reflect the following changes:

- PCB rule definition has been updated to reflect the following changes:

<table>
<thead>
<tr>
<th>PCB RULE DEFINITION</th>
<th>RULE NUMBER</th>
<th>RULE</th>
<th>RULE DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>100_OHM_DIFF</td>
<td></td>
<td></td>
<td>100-ohms differential impedance on outer layers and 95-ohms on inner layers.</td>
</tr>
<tr>
<td>1.5:1_SPACING</td>
<td></td>
<td></td>
<td>1:1_DIFFPAI</td>
</tr>
</tbody>
</table>