1. All resistance values are in ohms; 0.1 watt 1/4W.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.

Schematic / PCB #'s

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<table>
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<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>QTY</th>
<th>CRITICAL</th>
</tr>
</thead>
<tbody>
<tr>
<td>M87_COMMON,EEE_Z3H</td>
<td>CPU_2_6GHZ</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>M87_COMMON,EEE_Z3J</td>
<td>CPU_2_6GHZ</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
<tr>
<td>M87_COMMON,EEE_Z3F</td>
<td>CPU_2_5GHZ</td>
<td>1</td>
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<tr>
<td>M87_COMMON,EEE_Z3H</td>
<td>CPU_2_5GHZ</td>
<td>1</td>
<td>CRITICAL</td>
</tr>
</tbody>
</table>

- M87 BOM Groups

- Bar Code Labels / EEE #’s

- Module Parts

- BOM Configuration

Please note that the image contains a large table with details about BOM variants, BOM groups, and module parts, along with descriptions and reference designations. The table includes columns for part numbers, descriptions, quantities, and criticality, with each item being referenced to different BOM options and groups.
### Functional Test Points

#### Fan Connectors
- **FUNC_TEST**
- TP_NB_NC<1..16>
- 10 additional GND test points are called out separately in these notes.

#### Battery Digital Connector
- **FUNC_TEST**
- TP_NB_NC<1..16>

#### Left I/O Power Connector
- **FUNC_TEST**
- TP_NB_NC<1..16>

#### Left ALS Connector
- **FUNC_TEST**
- TP_NB_NC<1..16>

#### Thermal Diode Connectors
- **FUNC_TEST**
- TP_NB_NC<1..16>

#### System Validation TPs
- **FUNC_TEST**
- TP_NB_NC<1..16>

### ICT Test Points

#### GPU NO_TESTS
- TP_NB_NC<1..16>

#### CPU FSB NO_TESTS
- TP_NB_NC<1..16>

#### NB NO_TESTS
- TP_NB_NC<1..16>

### Functional / ICT Test

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**Thermal Module Holes**

- Left CPU TM Hole
- Right CPU TM Hole
- Bottom Left CPU TM Hole
- Right GPU TM Hole

**RAM Door (Torx) Holes**

- Top CPU TM Notch
- Bottom Right GPU TM Hole

**Frame Holes**

- Board Edge Notches (Can't be PTH)
- Tooling Holes (Can't be PTH)

**Signal Aliases**

- Digital Ground
- HOLE-VIA-P5RP25
- HOLE-VIA-P5RP25
- HOLE-VIA-P5RP25
- BOARD CHASSIS LINDACARD HOLE
- BOARD CHASSIS DVI HOLE
- BOARD CHASSIS DIMM NOTCH
- BOARD CHASSIS LIOFLEX HOLE
- BOARD CHASSIS BATTCONN HOLE
- BOARD CHASSIS RAMDOOR HOLE_0
- BOARD CHASSIS RAMDOOR HOLE_1

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**Sync Date**

- Sync Date = 08/23/2006
- Sync Master = (T9_MLB)

**MIN_LINE_WIDTH**

- 0.6MM

**MIN_NECK_WIDTH**

- 0.2MM

**VOLTAGE**

- 0V

**MAKE_BASE**

- TRUE
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**CPU Vcore HF and Bulk Decoupling**
- 1x 330μF, 20x 22μF 0805

**CPU Vcore VID Connections**

**VCCP (CPU I/O) Decoupling**
- 1x 470μF, 6x 0.1μF 0402

**VCCA (CPU AVdd) Decoupling**
- 1x 10μF, 1x 0.01μF

**Notes:**
- Place near CPU pin B26.
- Place in CPU center cavity.
- Place in CPU center cavity.

**Critical Components:**
- CRITICAL
- CRITICAL
- CRITICAL
Mini-XDP Connector

NOTE: This is not the standard XDP pinout.
Use with 910-0451 adapter board to support CPU, NB & IM debugging.

Direction of XDP module
Please avoid any obstructions on even-numbered side of J1300

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Tie VCC_AXG and VCC_AXG_NCTF to GND.
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
TV_DCONSELx to GND.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and CRT & TV-Out Disable above.
Follow instructions for LVDS and CRT & TV-Out Disable above.

Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and CRT & TV-Out Disable above.
Follow instructions for LVDS and CRT & TV-Out Disable above.

Notes:
- CRT & TV-Out Disable: When both CRT & TV-Out Disable are enabled, all signals are tied to GND. If only CRT or TV-Out Disable is enabled, signals are tied to VCC (VCore). Always ensure proper decoupling.
- LVDS: Ensure proper filtering and decoupling. Use 75-ohm resistors where necessary.
- CRT_DDC_CLK and CRT_DDC_DATA: Always connect to GND through 75-ohm resistors.
- SDVO TVCLKIN and SDVO_TVCLKIN#: Connect to GND through 75-ohm resistors.
- LVDS_A_DATA_P<2> = TV_C_RTN and LVDS_A_DATA_P<0> = CRT_RED_L.
- TS_LVDS_VREFL and TP_LVDS_VREFL: Ensure proper filtering and decoupling.

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Current numbers from Crestline EDS, doc #21749.

8 7 6 5 4 3 2 1

550 mA (533MHz DDR)
640 mA (667MHz DDR)
150 mA
250 mA
100 mA
0.4 mA
150 mA
100 mA
40 mA
60 mA
60 mA
40 mA
40 mA
35 mA
10 mA
50 mA
80 mA
30 mA
5 mA

S0 or S3M is acceptable

PP3V3_S0_NB_VCCA_TVDACK
PP3V3_S0_NB_VCCA_TVDACB
= GND_NB_VSSA_PEG_BG
PP1V25_S0M_NB_VCCA_SM_CK
= PP1V25_S0M_NB_VCCA_HPLL
PP1V25_S0M_NB_VCCA_SM
PP1V25_S0M_NB_VCCA_DPLLB
PP1V25_S0M_NB_VCCA_DPLLA
= GND_NB_VSSA_DAC_BG
PP3V3_S0_NB_VCCA_CRTDAC
PP1V25_S0M_NB_PEGPLL
= PP3V3_S0_NB_VCCA_PEG_BG
PP1V25_S0M_NB_VCCD_HPLL
PP1V5_S0_NB_VCCD_TVDAC
=PP1V5_S0_NB_VCCD_CRT
PP1V8_S0_NB_VCCD_LVDS
= PP1V8_S0_NB_VCCD_LVDS2
VCCD_LVDS1
VCCD_PEG_PLL
VCCD_HPLL
VCCD_QDAC
VCCD_TVDAC
VCCA_TVC_DAC2
VCCD_CRT
VCCA_TVB_DAC2
VCCA_TVB_DAC1
VCCA_TVA_DAC2
VCCA_TVA_DAC1
VCCA_SM_CK1
VCCA_SM_CK2
VCC_TX_LVDS
VCCA_SM_NCTF2
VCCA_SM_NCTF1
VCCA_SM11
VCCA_SM10
VCCA_SM9
VCCA_SM8
VCCA_SM7
VCCA_SM5
VCCA_SM4
VCCA_SM3
VCCA_SM2
VCCA_SM1
VCCA_PEG_PLL
VSSA_PEG_BG
VCCA_LVDS
VCCA_MPLL
VTT16
VCCA_DPLLB
VCCA_DPLLA
VSSA_DAC_BG
VCCA_CRT_DAC2
VCCA_CRT_DAC1
VCC_SYNC

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Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

---

NB Grounds

---

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---

=NB_TDB_FORCE

=NB_TDE_SENSE

---

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NOTE: This filter is required even if using only external graphics.

VCCD_TVDAC also powers internal thermal sensors.

Current numbers from Crestline EDS Addendum, doc #20127.

These 2 caps should be 22000pF-1000mA

C2200 22000pF-1000mA
C2201 22000pF-1000mA

C2200 22000pF-1000mA
C2201 22000pF-1000mA

C2200 22000pF-1000mA
C2201 22000pF-1000mA

C2200 22000pF-1000mA
C2201 22000pF-1000mA
"Factory" (thru-hole) slot

DDR2 Bypass Caps
(For return current)
One cap for each side of every RPAK, one cap for every two discrete resistors.

Ensure CS_L and ODT resistors are close to SO-DIMM connector.
- Place one cap at each pin of transformers.

Transformers should be mirrored on opposite sides of the board.

Place close to connector.

Short shielded RJ-45 514-0277

- New Series Rs required for European Telecom Compliance

- Place near each pin of transformer

- R3900 through R3903

- Place close to connector

Ethernet Connector

C3900, C3901, C3902, C3903

R3900, R3901, R3902, R3903
Lo: Beta Mode enable (1394b).

Single-port / Desktop systems are Power Class 0 ('000').
If power source is S3, can tie EN to IN.

SEL=0 Choose SMC
SEL=1 Choose USB

Place L4600 and L4605 at connector pin.
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CRITICAL

FERR-220-OHM-2A

1.0UF

X7R

50V

0603

CRITICAL

3944

200V

525

Mar-10

51450171

Left Clutch Barrel Interconnect
NOTE: Unused pins have "SMC_Fan" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.
I2C addresses:

- Addr low -> 0x30, 0x31
- Addr high -> 0x32, 0x33

Alias SCL/SDA to GND if using analog outputs only

Desired orientation when placed on board top-side:

1. Package Top
2. Frame Y
3. Frame X
4. Frame Z

Desired orientation when placed on board bottom-side:

1. Top-through View
2. Frame Y
3. Frame X
4. Frame Z

---

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---

**Sudden Motion Sensor (SMS)**

APN: 338S0354

---

**Sync Date:** 03/19/2007

---

**SHT of Size D**

---

**Sync Master:** M76_MLB

---

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Left I/O Power Connector

CRITICAL
35900
0713
0962

Battery Connector (Digital Signals)

CRITICAL
SM04B-ACH
M-RT-SM
87438-0663

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Power FETs

DRAWING NUMBER

REV.

SYNC_DATE=03/19/2007

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APPLE INC.

051-7413

15.0.0

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When both are low TPS51120 VIN current drops from 100-150uA to 10-20uA.

EN3 can float or tie to VREG5 for automatic 3.3V LDO enable

=PP5V_S5_EN5

=PP3V3S5_EN

=PP3V3S5_PGOOD

=PP5VS5_PGOOD

=PP5VS5_EN

NOTE: EN5 can float or tie to VIN for automatic 5V LDO enable

5V Fixed

P5VS5_VO

GND_P5VS5_PGND

P5VS5_CS

P5VS5_LL

P5VS5_DRVH

P5VS5_VBST

VOLTAGE=2V

MIN_NECK_WIDTH=0.20 mm

MIN_LINE_WIDTH=0.20 mm

VOLTAGE=0V

MIN_NECK_WIDTH=0.20 mm

MIN_LINE_WIDTH=0.6 mm

MIN_LINE_WIDTH=0.6 mm

SWITCH_NODE=TRUE

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.6 mm

 Quando ambos forem baixos, a corrente do TPS51120 VIN cai de 100-150uA para 10-20uA.

EN3 pode flutuar ou estar ligada a VREG5 para habilitação automática do LDO 3.3V.

=PP5V_S5_EN5

=PP3V3S5_EN

=PP3V3S5_PGOOD

=PP5VS5_PGOOD

=PP5VS5_EN

NOTA: EN5 pode flutuar ou estar ligada a VIN para habilitação automática do LDO 5V.

Corrente fixa de 5V

P5VS5_VO

GND_P5VS5_PGND

P5VS5_CS

P5VS5_LL

P5VS5_DRVH

P5VS5_VBST

VOLTAGE=0V

MIN_NECK_WIDTH=0.20 mm

MIN_LINE_WIDTH=0.6 mm

MIN_LINE_WIDTH=0.6 mm

SWITCH_NODE=TRUE

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.6 mm

 Quando ambos forem baixos, a corrente do TPS51120 VIN cai de 100-150uA para 10-20uA.

EN3 pode flutuar ou estar ligada a VREG5 para habilitação automática do LDO 3.3V.

=PP5V_S5_EN5

=PP3V3S5_EN

=PP3V3S5_PGOOD

=PP5VS5_PGOOD

=PP5VS5_EN

NOTA: EN5 pode flutuar ou estar ligada a VIN para habilitação automática do LDO 5V.

Corrente fixa de 5V

P5VS5_VO

GND_P5VS5_PGND

P5VS5_CS

P5VS5_LL

P5VS5_DRVH

P5VS5_VBST

VOLTAGE=0V

MIN_NECK_WIDTH=0.20 mm

MIN_LINE_WIDTH=0.6 mm

MIN_LINE_WIDTH=0.6 mm

SWITCH_NODE=TRUE

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.6 mm

 Quando ambos forem baixos, a corrente do TPS51120 VIN cai de 100-150uA para 10-20uA.

EN3 pode flutuar ou estar ligada a VREG5 para habilitação automática do LDO 3.3V.

=PP5V_S5_EN5

=PP3V3S5_EN

=PP3V3S5_PGOOD

=PP5VS5_PGOOD

=PP5VS5_EN

NOTA: EN5 pode flutuar ou estar ligada a VIN para habilitação automática do LDO 5V.

Corrente fixa de 5V

P5VS5_VO

GND_P5VS5_PGND

P5VS5_CS

P5VS5_LL

P5VS5_DRVH

P5VS5_VBST

VOLTAGE=0V

MIN_NECK_WIDTH=0.20 mm

MIN_LINE_WIDTH=0.6 mm

MIN_LINE_WIDTH=0.6 mm

SWITCH_NODE=TRUE

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.6 mm

 Quando ambos forem baixos, a corrente do TPS51120 VIN cai de 100-150uA para 10-20uA.

EN3 pode flutuar ou estar ligada a VREG5 para habilitação automática do LDO 3.3V.

=PP5V_S5_EN5

=PP3V3S5_EN

=PP3V3S5_PGOOD

=PP5VS5_PGOOD

=PP5VS5_EN

NOTA: EN5 pode flutuar ou estar ligada a VIN para habilitação automática do LDO 5V.

Corrente fixa de 5V

P5VS5_VO

GND_P5VS5_PGND

P5VS5_CS

P5VS5_LL

P5VS5_DRVH

P5VS5_VBST

VOLTAGE=0V

MIN_NECK_WIDTH=0.20 mm

MIN_LINE_WIDTH=0.6 mm

MIN_LINE_WIDTH=0.6 mm

SWITCH_NODE=TRUE

GATE_NODE=TRUE

MIN_NECK_WIDTH=0.2 mm

MIN_LINE_WIDTH=0.6 mm

 Quando ambos forem baixos, a corrente do TPS51120 VIN cai de 100-150uA para 10-20uA.
3.3V FW PHY Supply

1.95V FW PHY Supply

Vout = 1.25V * (1 + Ra / Rb)

Backup power in case of FW bus VP short to keep PHY powered.

VP short to keep PHY powered.

Vout = 3.316V
200mA max output
(Switcher limit)

Vout = 3.316V
200mA max output
(Switcher limit)
1.8V Frame Buffer Regulator

Vout = 0.6V * (1 + Ra / Rb)

Vout = 1.8V

10A max output

1.8V Frame Buffer Regulator

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Left ALS Connector

White colored version of 518S0369

SATA HDD & IR & SIL Flex Connector

NOTE: SATA _UF_ nets cross DDR2 signals and pick up significant noise. Common-mode chokes are to remove this noise from SATA signals.
Design Guide recommends each strobe/signal group is routed on the same layer.

Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.

CPU_VCCSENSE = 25 MIL
FSB_DSTB_55S = 7 MIL 7 MIL
CPU_COMP = 27P4_OHM_SEC
FSB_ADDR = 3:1_SPACING

All FSB signals with impedance requirements are 55-ohm single-ended.

Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the ADDRs.

DSTB complimentary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group be routed on the same layer.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.

SOURCE: Santa Rosa Platform DG, Rev D.9 (#20517), Sections 4.2 & 4.3

---

CPU / FSB Net Properties

---

CPU/FSB Constraints

---

SOURCE: Santa Rosa Platform DG, Rev D.9 (#20517), Sections 4.4 & 4.9.2.4
## DDR2 Memory Bus Constraints

<table>
<thead>
<tr>
<th>SPACING</th>
<th>MEM_CTRL2MEM * =3:1_SPACING</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MEM_DATA2MEM =3:1_SPACING *</td>
</tr>
<tr>
<td></td>
<td>MEM_DQS2MEM * =3:1_SPACING</td>
</tr>
<tr>
<td></td>
<td>MEM_CMD2CMD * =1.5:1_SPACING</td>
</tr>
</tbody>
</table>

- **MEM_CLK2MEM** = 70_OHM_DIFF
- **MEM_DATA2DATA** *
- **MEM_2OTHER** = 25_MIL
- **MEM_2OTHER** MEM_DATA *
- **MEM_2OTHER** MEM_CMD **
- **MEM_2OTHER** MEM_CTRL * *

### Memory Net Properties

- **MEM_B_DQ<7..0>**
- **MEM_A_DQ<15..8>**
- **MEM_B_DQS_P<4>**
- **MEM_B_DQS_P<3>**
- **MEM_B_DQS_P<2>**
- **MEM_B_DQS_P<1>**
- **MEM_B_DQS_P<0>**
- **MEM_B_DM<7>**
- **MEM_B_DM<6>**
- **MEM_B_DM<2>**
- **MEM_B_DM<0>**
- **MEM_B_DQ<47..40>**
- **MEM_B_DQ<39..32>**
- **MEM_B_DQ<23..16>**
- **MEM_B_DQ<15..8>**
- **MEM_B_CMD**
- **MEM_B_CNTL**
- **MEM_B_CNTL**
- **MEM_B_CLK**
- **MEM_A_DQS7**
- **MEM_A_DQS_P<6>**
- **MEM_A_DQS5**
- **MEM_A_DQS4**
- **MEM_A_DQS_P<4>**
- **MEM_A_DQS3**
- **MEM_A_DQS2**
- **MEM_A_DM<2>**
- **MEM_A_DM<0>**
- **MEM_A_DQ_BYTE7**
- **MEM_A_DQ<63..56>**
- **MEM_A_A<14..0>**
- **MEM_A_CNTL**
- **MEM_A_CNTL MEM_45S**
- **MEM_55S MEM_CTRL**
- **MEM_CS_L<3..2>**
- **MEM_55S**
- **MEM_55S MEM_DATAMEM_A_DM6**
- **MEM_55S MEM_DATAMEM_A_DM5**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE4**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE3**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE1**
- **MEM_55S MEM_CMD**
- **MEM_55S MEM_CMD**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE2**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE0**
- **MEM_55S MEM_DATAMEM_A_DM6**
- **MEM_55S MEM_DATAMEM_A_DM3**
- **MEM_55S MEM_DATAMEM_A_DM2**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE2**
- **MEM_55S MEM_CMD**
- **MEM_55S MEM_CMD**

### Table Spacing Rules

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### Table Physical Rules

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</thead>
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<td>MEM_B_DQS_N&lt;5&gt; MEM_B_DQS_N&lt;3&gt; MEM_B_DQS_N&lt;1&gt; MEM_B_DQS_N&lt;0&gt;</td>
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<tr>
<td></td>
<td>MEM_B_CAS_L MEM_B_A&lt;14..0&gt; MEM_A_DQ&lt;63..56&gt; MEM_A_A&lt;14..0&gt;</td>
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<tr>
<td></td>
<td>MEM_A_DQ_BYTE7 MEM_A_CNTL MEM_A_CNTL MEM_45S MEM_CTRL</td>
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<tr>
<td></td>
<td>MEM_55S MEM_DATAMEM_A_DM6 MEM_55S MEM_DATAMEM_A_DM3</td>
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### Memory Bus Constraints

- **MEM_B_DQS_P<4>**
- **MEM_B_DQS_P<3>**
- **MEM_B_DQS_P<2>**
- **MEM_B_DQS_P<1>**
- **MEM_B_DQS_P<0>**
- **MEM_B_DM<7>**
- **MEM_B_DM<6>**
- **MEM_B_DM<2>**
- **MEM_B_DM<0>**
- **MEM_B_DQ<47..40>**
- **MEM_B_DQ<39..32>**
- **MEM_B_DQ<23..16>**
- **MEM_B_DQ<15..8>**
- **MEM_B_CMD**
- **MEM_B_CNTL**
- **MEM_B_CNTL**
- **MEM_B_CLK**
- **MEM_A_DQS7**
- **MEM_A_DQS_P<6>**
- **MEM_A_DQS5**
- **MEM_A_DQS4**
- **MEM_A_DQS_P<4>**
- **MEM_A_DQS3**
- **MEM_A_DQS2**
- **MEM_A_DM<2>**
- **MEM_A_DM<0>**
- **MEM_A_DQ_BYTE7**
- **MEM_A_DQ<63..56>**
- **MEM_A_A<14..0>**
- **MEM_A_CNTL**
- **MEM_A_CNTL MEM_45S**
- **MEM_55S MEM_CTRL**
- **MEM_55S MEM_DATAMEM_A_DM6**
- **MEM_55S MEM_DATAMEM_A_DM5**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE4**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE3**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE1**
- **MEM_55S MEM_CMD**
- **MEM_55S MEM_CMD**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE2**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE0**
- **MEM_55S MEM_DATAMEM_A_DM6**
- **MEM_55S MEM_DATAMEM_A_DM3**
- **MEM_55S MEM_DATAMEM_A_DM2**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE2**
- **MEM_55S MEM_DATAMEM_A_DQ_BYTE0**
Internal Interface Constraints

USB 2.0 Interface Constraints

HD Audio Interface Constraints
### Ethernet (Yukon) Constraints

**Controller Link (AMT) Constraints**

**PCI Bus Constraints**

**SOURCE:** Santa Rosa Platform DG, Rev 1.0 ($21112$), Sections 10.18.1 & 10.19

---

### Controller Link (AMT) Constraints

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<tr>
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<td>VREF</td>
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<td>NET</td>
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<tr>
<td>MIN</td>
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<td>Standard</td>
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<tr>
<td>MAX</td>
<td>55 ohm</td>
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### PCI Bus Constraints

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<tr>
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<tr>
<td>MIN</td>
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<td>MAX</td>
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### Electrical Constraint Set

- **ENET_MDI**
- **ENET_MDI_P<0>**
- **ENET_MDI_N<1>**
- **ENET_MDI_P<1>**
- **ENET_MDI_P<2>**
- **ENET_MDI_P<3>**
- **ENET_100D**
- **PCIE_100D**
- **PCIE_MINI_R2D_C_P**
- **PCIE_MINI_D2R_P**
- **PCIE_MINI_R2D_C_N**
- **PCIE_MINI_D2R_C_N**
- **PCIE_ENV_D2R_C_P**
- **PCIE_ENV_D2R_N**
- **PCIE_ENV_R2D_P**
- **PCIE_ENV_R2D_C_P**
- **PCIE_ENV_R2D_N**
- **PCIE_ENV_R2D_P**
- **PCIE_ENV_R2D_C_N**
- **PCIE_ENV_R2D_C_P**
- **PCIE_ENV_R2D_C_N**
- **PCIE_ENV_R2D_P**

---

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**SOURCE:** Based on Santa Rosa Platform DG, Rev 1.0 ($21112$), Sections 10.27.1.5-7, 10.29 & 10.30

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**www.vinafix.vn**
Clock Signal Constraints

| Clock Signal | Min. Width | Max. Length | Differential Pair | Primary Gap | Neck Gap | Physical Rule
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<td>100_OHM_DIFF</td>
<td>STANDARD</td>
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<td>=100_OHM_DIFF</td>
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<tr>
<td>CLK_PCIE_100D</td>
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<td>STANDARD</td>
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Clock Net Properties

| Clock Net | Min. Width | Max. Length | Differential Pair | Primary Gap | Neck Gap | Physical Rule
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<td>20_MIL</td>
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<td>SMB_55S</td>
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<td>SMBUS_SMC_BSA_SDA</td>
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<td>SMBUS_SMC_BSA_SCL</td>
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</table>

SMC SMBus Net Properties

| Clock Net | Min. Width | Max. Length | Differential Pair | Primary Gap | Neck Gap | Physical Rule
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<td>20_MIL</td>
<td>20_MIL</td>
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<td>SMB</td>
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</table>

Clock & SMC Constraints

| Clock Net | Min. Width | Max. Length | Differential Pair | Primary Gap | Neck Gap | Physical Rule
<table>
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Source: Santa Rosa Platform Design Rev 1.0 (Design ID 321), Sections 14.1 - 14.6
FireWire Interface Constraints

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<th>Net Type</th>
<th>Net Property</th>
<th>Layer</th>
<th>Minimum Neck Width</th>
<th>Maximum Neck Length</th>
<th>Diffpair Primary Gap</th>
<th>Diffpair Neck Gap</th>
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FireWire Net Properties

<table>
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<th>Port</th>
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<th>Layer</th>
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<td>Port B</td>
<td>FW_55S</td>
<td>=55_OHM_SE</td>
<td>2</td>
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Port 2 Not Used

FireWire Constraints

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### Memory Constraint Relaxations

Allow 0.127 mm nails for >0.127 mm lines for GNRH fanout.

<table>
<thead>
<tr>
<th>Device</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
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</thead>
<tbody>
<tr>
<td>VGA</td>
<td>0.127 mm</td>
<td>0.15 mm</td>
</tr>
</tbody>
</table>

Allow 0, mm nails for >0.1 mm lines between thru-hole 50-DIP8 pins.

<table>
<thead>
<tr>
<th>Device</th>
<th>Minimum Width</th>
<th>Maximum Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGA</td>
<td>0.1 mm</td>
<td>0.15 mm</td>
</tr>
</tbody>
</table>

### Graphics, SATA Constraint Relaxations

Alternate difpair width/gap through BGA fanout areas (90°-mcm dif)

<table>
<thead>
<tr>
<th>Device</th>
<th>Minimum Width</th>
<th>Maximum Gap</th>
</tr>
</thead>
<tbody>
<tr>
<td>VGA</td>
<td>0.127 mm</td>
<td>0.15 mm</td>
</tr>
</tbody>
</table>

### Project Specific Constraints

- **Switches, Connectors**
- **And, Data-Drivers**
- **Threshold of preamp properties**
- **The switch for switches properties in the appropriate channels**
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