1. All resistance values are in ohms, 0.1 watt +/- 5%.
2. All capacitance values are in microfarads.
3. All crystals & oscillator values are in hertz.

<table>
<thead>
<tr>
<th>Page</th>
<th>Contents</th>
<th>Sync</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Table of Contents</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>System Block Diagram</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Power Block Diagram</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>SMC Configuration</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Revision History</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Port Table</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Power Aliases</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>SIGNAL Alias</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>CPU PMU</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>CPU Power &amp; Ground</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>CPU Decoupling</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>Extended Debug Port (xint-MDP)</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>MCP CPU Interface</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>MCP Memory Interface</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>MCP Misc Interface</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>MCP Graphics</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>MCP DATA, USB &amp; Ethernet</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>MCP SMU, LNA &amp; MISC</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>MCP Power &amp; Ground</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>MCP Power Sequencing</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>MCP GPU Core &amp; 1L 2L</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>MCP standard Decoupling</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>MCP Graphic Support</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>SMI Misc</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>DSK 80-DIM Connector A</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>DSK 80-DIM Connector B</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>DSK EPF/KV BUS 2AP96</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>FUNCTION 3D Way Modeling</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>REFLECTOR 2D CONNECTOR</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>Heterogeneous Card Reader</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Ethernet Port 11.10V</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Ethernet Ports</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>Firewire Connector</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>Firewire Port &amp; MV Power</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>Firewire Connector</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>DATA Connectors</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>External USB Connectors</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>Internal USB Support</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>HDMI</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>SMC Support</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>EXTERNAL DECK CONNECTOR</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td>AS DWELL CONNECTIONS</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td>Voltage sensing</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td>Current sensing</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>Thermal sensors</td>
<td></td>
</tr>
</tbody>
</table>

---

**Schematic / PCB #'s**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>REFERENCE NO.</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>051-8563</td>
<td>n/a</td>
<td>Schematic / PCB #1</td>
</tr>
<tr>
<td>051-8579</td>
<td>n/a</td>
<td>Schematic / PCB #2</td>
</tr>
</tbody>
</table>

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**Apple Inc.**

PVT, 3/18/10

---

**URL:** www.vinafix.vn
# K6 BOARD STACK-UP

## Top

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>ROM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Bottom

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>ROM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Programmer Board

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>ROM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

## Alternate Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Reference Des</th>
<th>Critical</th>
<th>ROM Option</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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**Notes:**
- **Part Number**: 128S0093
- **Description**: 128S0093
- **Reference Des**: 128S0093
- **Critical**: Yes
- **ROM Option**: 128S0093

---

**ROM Configuration**

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![Apple](https://via.placeholder.com/150)

**Revision:** A.13.0

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**Drawing Number:** 051-85623

**Sheet:** 2 of 109

**Title:** Apple Inc.

**Date:** 05/04/01

---

**Website:** www.vinafix.vn
CPU VCore HF and Bulk Decoupling
4x 330µF, 20x 22µF 0805

Placement note: C1240-C1241.

VCCA (CPU AVdd) Decoupling
ix 10µF, ix 0.1µF

VCCP (CPU I/O) Decoupling
ix 330µF, ix 0.1µF 0402

- PE1 ports are Gen1-only. 1 RCs: x1, x1
- PE0 ports are Gen2-capable. 4 RCs: 4x, x2, x1, x1
- +VIO_PE_AVDD1 and +VIO_PE_DVDD1 can be GND
- If PE0[4:5] and PE1[0:1] are not used, +VIO_PE_AVDD0 and +VIO_PE_DVDD0 can be GND

MCP PCIe Interfaces

Apple Inc.

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A.13.0

SIZE A

DRAWING NUMBER 051-8563

REV 05/21/09

PAGE 16 OF 109

www.vinafix.vn
Current numbers from MCP89 A01 Bring-up Support document (MCP89_TDP_EDP_Bringup_Targets_Apple.pdf, dated August 5, 2009).

**DDC Mode Pull-downs**

- **GPIO Pull-Ups**
  - DP0_0_N/TMDS0_TX2_N
  - DP0_1_N/TMDS0_TX1_N
  - DP0_3_N/TMDS0B_TXD_N
  - DP1_3_N/TMDS0B_TXD_N
  - DP1_2_N/TMDS0_TX3_N
  - DP1_1_N/TMDS0_TX4_N

- **DDC Mode Pull-downs**
  - DDC_DATA0/GPIO_39
  - DDC_CLK0/GPIO_38

**GPIO Pull-Ups**

- PP3V3_S0_MCP_PLL_DP_USB
  - PP1V05_S0_MCP_PLL_IFP
  - PP3V3R1V8_S0_MCP_IFP_VDD

**DDC Mode Pull-downs**

- DDC_DATA2/DP_AUX_CH0_N
  - DDC_CLK2/DP_AUX_CH0_P

**GPIO Pull-Ups**

- TP_MCP_RGB_DAC_VREF
  - TP_MCP_RGB_BLUE
  - TP_MCP_RGB_GREEN
  - TP_MCP_RGB_RED

**DDC Mode Pull-downs**

- LVDS_IG_B_DATA_P/N<0>
  - LVDS_IG_B_DATA_P/N<1>
  - LVDS_IG_B_DATA_P/N<2>
  - LVDS_IG_B_DATA_P/N<3>

**GPIO Pull-Ups**

- AUD_IP_PERIPHERAL_DET
  - IFPB_TXD6_P
  - IFPA_TXD3_P
  - IFPA_TXD2_N
  - IFPA_TXD1_N
  - IFPA_TXD1_P
  - IFPA_TXD0_P

**DDC Mode Pull-downs**

- TMDS_IG_DDC_DATA
  - TMDS_IG_DDC_CLK
  - TMDS_IG_TXD_P/N<0>
  - TMDS_IG_TXD_P/N<1>
  - TMDS_IG_TXD_P/N<2>
  - TMDS_IG_TXD_P/N<3>
  - TMDS_IG_TXC_P/N

**GPIO Pull-Ups**

- LCD_BKL_CTL/GPIO_57
  - LCD_BKL_ON/GPIO_59

**DDC Mode Pull-downs**

- TMDS0_VPROBE
  - IFPAB_VPROBE
  - LCD_IG_PWR_EN
  - LCD_IG_BKLT_EN
  - LCD_IG_BKLT_PWM

**GPIO Pull-Ups**

- FBGA
  - OMIT
  - SATARDRVR_A_EN

**DDC Mode Pull-downs**

- +VDD_IFPA
  - +VIO_PLL_NV_1
  - +VIO_PLL_NV_2
  - +VIO_PLL_V
  - +VIO_PLL_SPPLL0_1
  - +VIO_PLL_SPPLL0_2
  - +3.3V_PLL_DP0_2
  - +3.3V_PLL_USB_2
  - =MCP_IFPAB_DDC_CLK
  - =MCP_IFPB_TXD_P/N<0>
  - =MCP_IFPB_TXD_P/N<1>
  - =MCP_IFPB_TXD_P/N<2>
  - =MCP_IFPB_TXD_P/N<3>
  - =TP_MCP_RGB_HSYNC
  - =TP_MCP_RGB_RED
  - =TP_MCP_RGB_BLUE
  - =TP_MCP_RGB_GREEN

**GPIO Pull-Ups**

- TP_MCP_RGB_HSYNC
  - TP_MCP_RGB_BLUE
  - TP_MCP_RGB_GREEN
  - TP_MCP_RGB_RED

**DDC Mode Pull-downs**

- LVDS: Power +VDD_IFPA at 1.8V
  - TMDS: Power +VDD_IFPA at 3.1V

**GPIO Pull-Ups**

- VSUPP
  - VSUPP
  - VSUPP
  - VSUPP
  - VSUPP
  - VSUPP
  - VSUPP

**DDC Mode Pull-downs**

- RGB_DAC_DISABLE:
  - MOY to float all RGB DAC signals.
  - DCCable(DCCable pull-ups still required) (or use an OPD).
  - Connect +3.1V to RDC to GND.

**GPIO Pull-Ups**

- RGB_DAC_DISABLE:
  - RGB_DAC_DISABLE:
  - RGB_DAC_DISABLE:
  - RGB_DAC_DISABLE:
  - RGB_DAC_DISABLE:
  - RGB_DAC_DISABLE:
  - RGB_DAC_DISABLE:

**DDC Mode Pull-downs**

- HPLUG_DET0/GPIO_20
  - HPLUG_DET1/GPIO_21
  - HPLUG_DET2/GPIO_22

**GPIO Pull-Ups**

- RGB_DAC_VSYNC
  - RGB_DAC_HSYNC
  - RGB_DAC_GREEN
  - RGB_DAC_BLUE

**DDC Mode Pull-downs**

- TMDS: Power +VDD_IFPA at 3.1V
  - TMDS: Power +VDD_IFPA at 3.1V

**GPIO Pull-Ups**

- VSUPP
  - VSUPP
  - VSUPP
  - VSUPP
  - VSUPP
  - VSUPP
  - VSUPP

**DDC Mode Pull-downs**

- TMDS: Power +VDD_IFPA at 3.1V
  - TMDS: Power +VDD_IFPA at 3.1V
NOTE: "SW" rails are dynamically switched in the SO state as needed, controlled by MCP89 GPIOs.

- **+200 mA**
- **+2000 mA**

POWER I

+VDD_MEM_26
+VDD_MEM_23
+VDD_MEM_12
+VDD_MEM_8
+VDD_MEM_4
+VDD_MEM_2

AL5
AM3
AF18
AL7

=PP1V5R1V35_SW_MCP_MEM

6
14 20 22

(PE0[5:4], PE1[1:0])

+3.3V_3
+3.3V_HVDD_3
+VIO_PE_AVDD0_3

GND_COREA_SENSE
+VDD_COREA_29
+VDD_COREA_25
+VDD_COREA_11
+VDD_COREA_10
+VDD_COREA_8

+VIO_SATA_DVDD_12
+VDD_DUAL_RMGT_1
+VIO_SATA_DVDD_7
+VIO_SATA_DVDD_5
+VIO_SATA_DVDD_3
+VIO_SATA_DVDD_2

+VDD_DUAL_AUXC_3
+VDD_DUAL_AUXC_2

+3.3V_DUAL_2
+VDD_COREB_39
+VDD_COREB_38
+VDD_COREB_32
+VDD_COREB_23
+VDD_COREB_14
+VDD_COREB_12
+VDD_COREB_11
+VDD_COREB_8

AG34
AP24
AC27
AU37

B12
AD7

(11 OF 11)

GND_6
GND_12
GND_11
GND_63
GND_52
GND_39
GND_35
GND_21
GND_12
GND_114
GND_113
GND_99
GND_98
GND_96
GND_91
GND_90
GND_84
GND_82
GND_81
GND_77
GND_73

(8 OF 11)

 TP_MCP_VDDCOREA_SENSEP

+VDD_MEM_26
+VDD_MEM_23
+VDD_MEM_12
+VDD_MEM_8
+VDD_MEM_4
+VDD_MEM_2

AL5
AM3
AF18
AL7

=PP1V5R1V35_SW_MCP_MEM

6
14 20 22

(PE0[5:4], PE1[1:0])

+3.3V_3
+3.3V_HVDD_3
+VIO_PE_AVDD0_3

GND_COREA_SENSE
+VDD_COREA_29
+VDD_COREA_25
+VDD_COREA_11
+VDD_COREA_10
+VDD_COREA_8

+VIO_SATA_DVDD_12
+VDD_DUAL_RMGT_1
+VIO_SATA_DVDD_7
+VIO_SATA_DVDD_5
+VIO_SATA_DVDD_3
+VIO_SATA_DVDD_2

+VDD_DUAL_AUXC_3
+VDD_DUAL_AUXC_2

+3.3V_DUAL_2
+VDD_COREB_39
+VDD_COREB_38
+VDD_COREB_32
+VDD_COREB_23
+VDD_COREB_14
+VDD_COREB_12
+VDD_COREB_11
+VDD_COREB_8

AG34
AP24
AC27
AU37

B12
AD7

(11 OF 11)

GND_6
GND_12
GND_11
GND_63
GND_52
GND_39
GND_35
GND_21
GND_12
GND_114
GND_113
GND_99
GND_98
GND_96
GND_91
GND_90
GND_84
GND_82
GND_81
GND_77
GND_73
NV Requirements:
Q2355/Q2356 chosen for low output capacitance.
CKE must be held low to keep memory in self-refresh.
Clamps also discharge VTT rail via termination resistor on each CKE signal on DIMM.
Clamps release after MCP89 MEMVDD is up and CKEs are driven by MCP89.
Clamps enable before MCP89 MEMVDD rail switched off.

NO STUBS on CKE signals!

Approx. Ramp Time (EN to 1.35V, uS): 7.91 + 0.0678 * R1 (Kohms)

Gated Rail Savings: 120mW

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.

- Min Ramp-Up Time: 20 uS (10% to 90%)
- Max Ramp-Up Time: 65 uS (ENABLE to 90%)
- FET Ron <= 3.8 mOhms

4250 mA (OR 1.35V)

44
44

405x394

R2305
MF
560K
402
1/16W
1%

C2305
0.1UF
402
CERM
10V
20%

C2300
CRITICAL
PLACE_NEAR=Q2300.9:2 mm
1206-1
CERM-X5R
6.3V
20%
100UF

Q2300 helps reduce input rail droop during Q2300 turn-on.

DIMM CKE Clamps

cke must be held low to keep memory in self-refresh.
clamps enable when MCP89 MEMVDD rail is enabled.
clamps release when MCP89 MEMVDD is up and CKEs are driven by MCP89.
clamps discharge VTT rail via termination resistor on each CKE signal on DIMM.
Q2355/Q2356 chosen for low output capacitance.

NOTE: nVidia recommends Infineon BSC030N03MS for Q2300.
C2405 helps reduce input rail drop during Q2400 turn-on.

Approx. Ramp Time (EN to 1V, μs): $43.9 + 0.6943 \times C1(pF)$

- Min Ramp-Up Time: 100 μs (10% to 90%)
- Max Ramp-Up Time: 1500 μs (90% to 99%)
- FET Ron ≤ 2.5 mΩms

Gated Rail Savings: 860mW

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.

C2400 helps reduce input rail droop during Q2400 turn-on.

Max Ramp-Up Time: 1500 μs (ENABLE to 90%)

C2405 helps reduce input rail drop during Q2400 turn-on.

Approx. Ramp Time (EN to 1V, μs): $43.9 + 0.6943 \times C1(pF)$

- Min Ramp-Up Time: 100 μs (10% to 90%)
- Max Ramp-Up Time: 1500 μs (90% to 99%)
- FET Ron ≤ 2.5 mΩms

Gated Rail Savings: 860mW

NOTE: nVidia recommends Infineon BSC020N03MS for Q2400.
DAC step size: 8.59mV / step @ output

Margined target:
- 0.000V - 1.191V (0x00 - 0x5C)
- 0.200V - 1.050V (+/- 500mV)

Margined target (when no VREF margining circuit stuffed):
- 0.000V - 1.501V (0x00 - 0x74)
- 0.75V (DAC: 0x3A)

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

VREFMRGN_CPUGTLREF_BUF:
- VREFMRGN_SODIMMS_CA
- VREFMRGN_SODIMMB_CA
- VREFMRGN_SODIMMA_CA

VREFMRGN_SODIMMB_BUF:
- VREFMRGN_CA_SODIMMB_EN
- VREFMRGN_CA_SODIMMB

VREFMRGN_CA_SODIMMA_BUF:
- VREFMRGN_CA_SODIMMA_EN
- VREFMRGN_CA_SODIMMA

Required zero ohm resistors when no VREF margining circuit stuffed:

**Page Notes**

Power aliases required by this page:
- PPVTT_S3_DDR_BUF
- VREFMRGN_CPUGTLREF_BUF

Signal aliases required by this page:
- =PPVTT_S3_DDR_BUF
- =VREFMRGN_CPUGTLREF_BUF
- =PCA9557D_SDA

Reference options provided by this page:
- =PPVTT_S3_DDR_BUF
- =VREFMRGN_CPUGTLREF_BUF

NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

Required zero ohm resistors when no VREF margining circuit stuffed:

Page dimensions: 1224.0x792.0

Page Notes

Signal aliases required by this page:

- FW_PME_L
- FW_CLKREQ_L

Power aliases required by this page:

- PP1V0_FW_FWPHY
- PP1V05_FW_P1V0FWFET
- PP3V3_FW_P3V3FWFET
- PPBUS_FW_FET

Page Notes

FireWire Port Power Switch

FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TP pairs.
Host can detect as load on TPEA# signal.
Current source only active when FW_PWR_EN is low.

FireWire PHY WAKE# Support

When PHY is powered, FW_PHY_WAKEN# acts as legacy PME# signal.

Test Note for 3.3V Rail Current Changed to EDP Number.

NONE

- FW_CLKREQ_PHY_L
- FW_PME_L

Critical

Apple Inc.
**ODD Power Control**

- Ensure the drive is unpowered in S3/S5.

**NOTE:**
- 3.3V must be S0 if 5V is S3 or S5 to support analog sense resistor.
- Also together if no sense n.

**SATA HDD Port**

- SATA_HDD_R2D_N
- SATA_HDD_D2R_P
- SATA_HDD_D2R_RDRV_OUT_N
- SATA_HDD_D2R_RDRV_IN_N
- SATA_HDD_D2R_RDRV_IN_P
- SATA_HDD_D2R_C_P

**SATA ODD Port**

- SATA_HDD_R2D_C_P
- SATA_HDD_R2D_UF_P
- SATA_HDD_R2D_UF_N

**PS8511A / PS8515A Straps**

- SATA_HDD_D2R_N
- SATA_HDD_R2D_P
- SATA_HDD_R2D_UF_P

**SATA Redriver**

- SATA_HDD_R2D_UF_N

---

**U4510 ADD NO STUFF IN PRODUCTION!!!!**

---

**SATA Connectors**

Apple Inc. 051-3662 A13.0

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those designated as inputs require pull-ups.

pins designed as outputs can be left floating,
Debug Power "Buttons"

SMC Reset "Button", Supervisor & AVREF Supply

System (Sleep) LED Circuit

SMC Crystal Circuit

SMC FSB to 3.3V Level Shifting

SMC Pull-ups

SMC Pull-downs

Unused Pins

Apple Support

www.vinafix.vn
Enables PBUS VSense
Place RC close to SMC
divider when high.

MCP Voltage Sense / Filter

CPU Voltage Sense / Filter

- CPUVSENSE_IN
- SMCPU_VSENSE
- GND_SMC_AVSS
- SMC_PBUS_VSENSE
- GND_SMC_AVSS
- SMC_MCP_VSENSE
- PPVCORE_S0_MCP
- PPVCORE_S0_CPU
- PBUS_G3H_VSENSE
- PBUSVSENS_EN_L_DIV
- PBUSVSENS_EN_L
- =PBUSVSENS_EN

- R5316
- 100K
- 402
- MF-LF
- 1/16W
- 1%
- 1%
- 1%

- C5309
- 20%
- 6.3V
- X5R
- 402
- 0.22UF

- R5309
- 20%
- 6.3V
- X5R
- 402
- 0.22UF

- R5315
- 402
- MF-LF
- 1/16W
- 1%
- 1%
- 1%

- R5385
- 402
- MF-LF
- 1/16W
- 1%
- 1%
- 1%

- R5386
- 402
- MF-LF
- 1/16W
- 1%
- 1%
- 1%

- XW5309
- SM
- PLACE_NEAR=L7400.2:5 MM

- XW5359
- SM
- PLACE_NEAR=R7525.2:5 MM
CPU T-Diode Thermal Sensor

MCP T-Diode Thermal Sensor

**Thermal Sensors**

Apple Inc.

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PAGE 21

PAGE TITLE

DRAWING NUMBER

SIZE

BRANCH

REVISION

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BOoster +18.5VDC fOr Sensors

To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED.
If LOW, keyboard backlight present. If none, keyboard backlight not present. R5853 always stubbed, stubs only grounded when KB BL flex connected.

Keyboard Backlight Driver & Detection

Keyboard Backlight Connector

J5815 pin 1 is grounded on keyboard backlight flex
MCP89 SPI Frequency Select:

<table>
<thead>
<tr>
<th>Frequency</th>
<th>SPI_MOSI</th>
<th>SPI_CLK</th>
</tr>
</thead>
<tbody>
<tr>
<td>25.0 MHz</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>31.2 MHz</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>41.7 MHz</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>62.5 MHz</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

*Note: 42 & 62 MHz use FAST_READ command.*

**NOTE:**
- SPI ROM
- SPI ROM will ignore SPI cycles.
- SPI ROM will not use FAST_READ command.
LINE INPUT VOLTAGE DIVIDER

CODEC VIN = 2.0 VRMS
RX DET VIN = 1.14 VRMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
PC-HP = 3.6 HZ
PC-HP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS
Supply needs to guarantee 3.31V delivered to SMC VRef generator

Vout = 1.25V \times (1 + \frac{R_a}{R_b})

1-Wire OverVoltage Protection

1206-1
FOUR GROUND VIAS SHOULD BE DISTRIBUTED ALONG THE GROUND SHAPE THAT BOUND THE CONNECTOR BODY.

NOT TO REPRODUCE OR COPY IT

NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

THE POSSESSOR AGREES TO THE FOLLOWING:

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Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

SYNC_DATE=07/20/2009

MIN_LINE_WIDTH=0.30 MM

VOLTAGE=3.3V

PP3V3_LCDVDD_SW

MIN_NECK_WIDTH=0.20 MM

PPVOUT_SW_LCDBKLT

LVDS_DDC_DATA

LVDS_DDC_CLK

LVDS_CONN_A_CLK_F_N

PP3V3_S0_LCD_F

MIN_LINE_WIDTH=0.25 MM

MIN_NECK_WIDTH=0.20 MM

VOLTAGE=3.3V

PP3V3_LCDVDD_SW_F

90 OF 109

A.1.3.0

051-8563

67 OF 80

www.vinafix.vn
Q9440 must have Drain to Gate leakage of <500nA and Gate to Source resistance of >5MOhm.
Some signals require 27.4-ohm single-ended impedance.

NOTE: Intel Design Guide allows closer spacing if signal lengths can be shortened.

Spacing is 1x dielectric between ADDR#, REQ# signals, with 2x dielectric spacing to ADSTB#.

FSB 2X signals / groups shown in signal table on right.

FSB 4X signals / groups shown in signal table on right.

FSB (Front-Side Bus) Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_GTLREF</td>
<td>...</td>
</tr>
<tr>
<td>CPU_COMP</td>
<td>...</td>
</tr>
<tr>
<td>CPU_ITP</td>
<td>...</td>
</tr>
<tr>
<td>CPU_50S</td>
<td>...</td>
</tr>
<tr>
<td>CPU_27P4S</td>
<td>...</td>
</tr>
<tr>
<td>CPU_8MIL</td>
<td>...</td>
</tr>
<tr>
<td>...</td>
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</tbody>
</table>

CPU Signal Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>FSB_1X</td>
<td>...</td>
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<tr>
<td>FSB_CPURST_L</td>
<td>...</td>
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<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

CPU / FSB Net Properties

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>...</td>
<td>...</td>
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MCP FSB COMP Signal Constraints

<table>
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<tr>
<th>Constraint</th>
<th>Description</th>
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<tbody>
<tr>
<td>...</td>
<td>...</td>
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</table>

FSB Clock Constraints

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

www.vinafix.vn
All memory signals maximum length is 1.030 ps.

CLK intra-pair matching should be within 1 ps, inter-pair matching should be within 2 ps.

### Memory Bus Spacing Group Assignments

#### PHYSICAL_RULE_SET

#### SPACING_RULE_SET

#### NET_SPACING_TYPE1 NET_SPACING_TYPE2

#### MCP_MEM_COMP

#### MCP_MEM_COMP

### TABLE_PHYSICAL_RULE_ITEM

#### TABLE_PHYSICAL_RULE_HEAD

#### TABLE_SPACING_RULE_ITEM

#### TABLE_SPACING_ASSIGNMENT_ITEM

- **TABLE_SPACING_ASSIGNMENT_HEAD**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**
- **TABLE_SPACING_ASSIGNMENT_ITEM**

- **MEM_DQS**
- **MEM_CLK**
- **MEM_CMD**
- **MEM_DQ**
- **MEM_DATA**

#### ELECTRICAL_CONSTRAINT_SET

#### MEM_A_DQ_BYTE6

#### MEM_B_DQS7

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE3

#### MEM_A_DQS6

#### MEM_A_DQ_BYTE5

#### MEM_A_DQ_BYTE4

#### MEM_A_DQ_BYTE3

#### MEM_A_DQ_BYTE1

#### MEM_A_DQ_BYTE0

#### MEM_A_DQ_BYTE7

#### MEM_A_DQ_BYTE6

#### MEM_A_DQ_BYTE5

#### MEM_A_DQ_BYTE2

#### MEM_A_DQ_BYTE0

#### MEM_A_CMD

#### MEM_A_CNTL

#### MEM_A_CLK

#### MEM_B_DQS2

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE3

#### MEM_B_DQ_BYTE1

#### MEM_B_DQ_BYTE0

#### MEM_B_DQ_BYTE7

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE2

#### MEM_B_DQ_BYTE0

#### MEM_B_CMD

#### MEM_B_CNTL

#### MEM_B_CLK

#### MEM_B_DQS7

#### MEM_B_DQS2

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE3

#### MEM_B_DQ_BYTE1

#### MEM_B_DQ_BYTE0

#### MEM_B_DQ_BYTE7

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE2

#### MEM_B_DQ_BYTE0

#### MEM_B_CMD

#### MEM_B_CNTL

#### MEM_B_CLK

#### MEM_B_DQS7

#### MEM_B_DQS2

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE3

#### MEM_B_DQ_BYTE1

#### MEM_B_DQ_BYTE0

#### MEM_B_DQ_BYTE7

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE2

#### MEM_B_DQ_BYTE0

#### MEM_B_CMD

#### MEM_B_CNTL

#### MEM_B_CLK

#### MEM_B_DQS7

#### MEM_B_DQS2

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE3

#### MEM_B_DQ_BYTE1

#### MEM_B_DQ_BYTE0

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#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE2

#### MEM_B_DQ_BYTE0

#### MEM_B_CMD

#### MEM_B_CNTL

#### MEM_B_CLK

#### MEM_B_DQS7

#### MEM_B_DQS2

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE3

#### MEM_B_DQ_BYTE1

#### MEM_B_DQ_BYTE0

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#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE2

#### MEM_B_DQ_BYTE0

#### MEM_B_CMD

#### MEM_B_CNTL

#### MEM_B_CLK

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#### MEM_B_DQS2

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE3

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#### MEM_B_DQ_BYTE0

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#### MEM_B_DQ_BYTE5

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#### MEM_B_DQ_BYTE1

#### MEM_B_DQ_BYTE0

#### MEM_B_DQ_BYTE7

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE2

#### MEM_B_DQ_BYTE0

#### MEM_B_CMD

#### MEM_B_CNTL

#### MEM_B_CLK

#### MEM_B_DQS7

#### MEM_B_DQS2

#### MEM_B_DQS0

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE3

#### MEM_B_DQ_BYTE1

#### MEM_B_DQ_BYTE0

#### MEM_B_DQ_BYTE7

#### MEM_B_DQ_BYTE6

#### MEM_B_DQ_BYTE5

#### MEM_B_DQ_BYTE2

#### MEM_B_DQ_BYTE0

#### MEM_B_CMD

#### MEM_B_CNTL

#### MEM_B_CLK
**NEED PCIe Gen1/Gen2 notes!**

**Analog Video Signal Constraints**

**Digital Video Signal Constraints**

**SATA Interface Constraints**

**MCP89 Net Properties**

**MCP Constraints 1**

---

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### SD Card Interface Constraints

<table>
<thead>
<tr>
<th>Constraint Item</th>
<th>Min Length</th>
<th>Min Width</th>
<th>Min Spacing</th>
<th>Min Neck Width</th>
<th>Min Neck Length</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD_INTERFACE</td>
<td>100_OHM</td>
<td>7.5</td>
<td>25</td>
<td>7.5</td>
<td>7.5</td>
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<tr>
<td>SD_INTERFACE</td>
<td></td>
<td>3X_DIELECTRIC</td>
<td>3:1_SPACING</td>
<td></td>
<td>12</td>
</tr>
</tbody>
</table>

### SD Card Net Properties

- **SD_CMD**: 55_OHM_SE
- **SD_CLK**: 55_OHM_SE
- **SD_DATA_R**: 55_OHM_SE
- **SD_DATA**: 55_OHM_SE

### MCP RGMII (Ethernet) Constraints

- **SD_55S**: 100_OHM_DIFF
- **ENET_MDI**: 100_OHM_DIFF
- **ENET_MII**: 55_OHM_SE

### Ethernet Constraints

- **ENET_MDI**: 100_OHM_DIFF
- **ENET_MII**: 55_OHM_SE
- **ENET_TXD**: 55_OHM_SE
- **ENET_RXD**: 55_OHM_SE

### RGMII Net Properties

- **ENET_TXD**
- **ENET_RXD**
- **ENET_TXD**: 55_OHM_SE
- **ENET_RXD**: 55_OHM_SE

### SD Command Interface

- **BCM57765_CR_DATA<7..5>**: 30
- **SDCONN_DATA<7..5>**: 30
- **SD_D<7..5>**: 30

### SD Clock Interface

- **BCM57765_CR_DATA<4>**: 30
- **SDCONN_DATA<4..0>**: 30
- **SD_D<4..0>**: 30

### Ethernet Net Properties

- **ENET_CLK125M_TXCLK**: 17
- **ENET_CLK125M_RXCLK**: 17
- **ENET_CLK125M_RXCLK_R**: 17
- **ENET_PWRDWN_L**: 17
- **ENET_MDC**: 17
- **ENET_MDIO**: 17
- **ENET_INTR_L**: 17

### SDENET Constraints

- **BCM5764M/BCM57765 co-layout.

### Notes

- SD<0>..<4> are different to support BCM5744M/BCM57445 co-layout.
### SMBus Net Properties

<table>
<thead>
<tr>
<th>SMBus</th>
<th>Electrical</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMBUS_SMC_A_S3_SCL</td>
<td>1TO1_DIFFPAIR</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
<td>1TO1_DIFFPAIR</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_MGMT_SCL</td>
<td>1TO1_DIFFPAIR</td>
<td>0.1 MM</td>
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<tr>
<td>SMBUS_SMC_0_S0_SCL</td>
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<tr>
<td>SMBUS_SMC_BSA_SCL</td>
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</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
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<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_A_S3_SDA</td>
<td>1TO1_DIFFPAIR</td>
<td>0.1 MM</td>
<td>0.1 MM</td>
</tr>
<tr>
<td>SMBUS_SMC_B_S0_SCL</td>
<td>1TO1_DIFFPAIR</td>
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</tr>
</tbody>
</table>

### SMBus Charger Net Properties

<table>
<thead>
<tr>
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<th>Electrical</th>
<th>Physical</th>
<th>Spacing</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHGR_CSI</td>
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<td>1TO1_DIFFPAIR</td>
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<tr>
<td>CHGR_CSI_N</td>
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<tr>
<td>CHGR_CSI_R_P</td>
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<td>CHGR_CSO_R_N</td>
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<tr>
<td>CHGR_CSO_N</td>
<td>1TO1_DIFFPAIR</td>
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<td>CHGR_CSO_P</td>
<td>1TO1_DIFFPAIR</td>
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<td>0.1 MM</td>
</tr>
<tr>
<td>CHGR_CSO</td>
<td>1TO1_DIFFPAIR</td>
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<tr>
<td>CHGR_CSI_R_N</td>
<td>1TO1_DIFFPAIR</td>
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<tr>
<td>CHGR_CSO_R_P</td>
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<td>0.1 MM</td>
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</tr>
</tbody>
</table>
# K6/K69 Board-Specific Physical & Spacing Constraints

## Table of Contents
- PHYSICAL RULE SET
  - PHYSICAL RULE SET
  - PHYSICAL RULE SET
  - PHYSICAL RULE SET
  - PHYSICAL RULE SET
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